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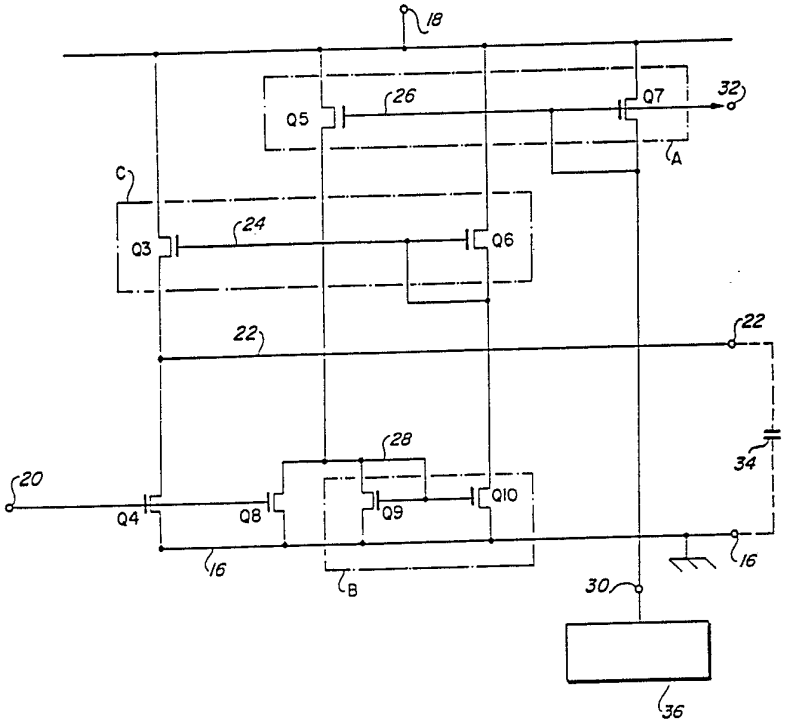
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(54) Title: TTL COMPATIBLE CMOS INPUT CIRCUIT

(57) Abstract

A TTL compatible CMOS input circuit comprising a series of current mirror circuits (A, B, C) arranged so that the input transistor (Q_4) is used to discharge the capacitive load (34) and one of a pair of transistors (Q_4) in one of the mirror circuits (C) provides charging current for the load (34). Only one of the charging (Q_3) and discharging (Q_4) transistor switches is 'on' at any one time, thus reducing circuit power consumption and reducing required device sizes. The input switching level is also independent of the supply voltage (18).



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TTL COMPATIBLE CMOS INPUT CIRCUIT

FIELD OF THE INVENTION

The invention relates to a TTL compatible input circuit for CMOS devices.

BACKGROUND OF THE INVENTION

Prior art TTL compatible input circuits for CMOS devices are typified by the circuit of Figure 1. Devices Q_1 (a P-type MOSFET) and Q_2 (an N-type) must be ratioed for a specific supply voltage, V_{CC}; that is, the ratio of the width to length of the gate of transistor Q_1 with respect to the same ratio of transistor Q_2 must be adjusted to attain the desired result for any particular supply voltage.

With a minimal high logic level TTL input voltage (V_{IH}) at input node 10 equal to 2.1 volts (which must be assumed for the purpose of reliable design), Q_1 is always conducting (independent of whether Q_2 is in an "on" or "off" state) and for a supply of 12 volts, the supply current drain is about 60uA (or higher, depending upon the speed requirements of the circuit) with Q_2 "on." For Q_2 to sink the current from Q1 and drive the output to ground with V_{IN} = 2.1 volts, Q2 must be very large.

The prior art circuit of Figure 1 is subject to problems due to supply line voltage shifts (since the required ratio of gate sizes is dependent upon that voltage), requires relatively high DC current supply drain and has a relatively long propagation delay time, in addition to the aforementioned large area requirement of transistor Q_2.

United States Patent No. 4,350,710, by Cohen et al., discloses a TTL to CMOS interface circuit which utilizes a FET inverter with its N channel being a part of a first current mirror and its P channel being part of a second current mirror. The inverter output is the reference signal input to the current mirrors. The current sources for each control leg of the two current mirror circuits are variable; in the first case to compensate for variations in the input signal, in the second case to compensate the inverter for manufacturing tolerances.

United States Patent No. 4,472,647, by Allgood et al., also employs current mirror circuits in a design which accepts either CMOS or TTL level input signals. Neither of these patents discloses a circuit such as the one described, infra.

SUMMARY OF THE INVENTION

Problems of prior art circuits are resolved by means of the TTL compatible CMOS input circuit of the invention. A band-gap or other voltage regulator means is used to provide a constant current through a series current limiting resistance; such constant current being supplied to one or more of the circuits of the invention. A series of MOSFET device pairs, connected in well known current mirror relationship, are used to provide input "turn on" and "turn-off" levels which are independent of supply voltage variations. One of the series of current mirror circuits is used to charge the output load capacitance at approximately a 100 microampere rate while the input transistor is used to discharge the same load at nearly the same rate. This arrangement provides for a balanced high speed circuit while consuming lower power from the system power supply since only one of the two (charging and discharging) transistors is drawing current at any one time.

It is, therefore, an object of the invention to provide a TTL compatible CMOS input circuit which has an improved (reduced) propagation delay time.

It is another object of the invention to provide a TTL compatible CMOS input circuit with improved (smaller) device sizes.

It is yet another object of the invention to provide a TTL compatible CMOS input circuit which requires improved (lower) current drain from a power source.

It is still another object of the invention to provide a TTL compatible CMOS input circuit which operates reliably within a wide range of supply line voltages.

These and other objects of the invention will be more readily understood upon review of the Detailed Description of the Preferred Embodiment of the Invention in view of the drawings in which:

Figure 1 depicts, in schematic form, a prior art TTL compatible CMOS input circuit; and

Figure 2 is a schematic diagram of the preferred embodiment of the TTL compatible CMOS circuit of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT OF THE INVENTION

(It should be noted that wherever in this specification like reference numerals are used they refer to like features.)

Referring to the schematic diagram of the invention in Figure 2, it should be understood that Q_3, Q_5, Q_6 and Q_7 are P-channel and Q_4, Q_8, Q_9 and Q_{10} are N-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices. Circuit input terminal 20 is connected to the gates of devices Q_4 and Q_8. The source electrodes of Q_4 and Q_8 are connected to ground. The drain electrode of Q_4 is connected to the drain electrode of Q_3 and to output node 22. The drain electrodes of Q_8 and Q_9 are connected to the gate of Q_9, the gate of Q_{10} and the drainelectrode of Q_5. Q_9 and Q_{10} comprise current mirror circuit B.

The source electrodes of Q_3 and Q_5 are connected to V_{CC} 18, the supply voltage. The source electrode of Q_{10} is connected to ground. The drain electrode of Q_{10} is connected to the drain electrode of Q_6, to the gate electrode of Q_6 and to the gate electrode of Q_3. Q_3 and Q_6 comprise current mirror circuit C. The source electrode of Q_6 is connected to V_{CC} 18, voltage supply. The gate electrode of Q_5 is connected to the gate electrode of Q_7, to the source electrode of Q_7, to output terminal 32 and to input terminal 30, which is adapted for connection to the output of constant current generator 36. The source electrode of Q_7 is connected to V_{CC} 18, voltage supply. Q_5 and Q_7 comprise current mirror circuit A.

Load capacitance, 34 (shown in phantom), is connected between output and charge/discharge node 22 and ground 16.

Constant current generator 36 is used to supply on the order of from one to five microamperes of current to the source electrode of MOSFET Q_7. The constant current generator 36 may

take the form of a band-gap voltage regulator with a series current limiting resistor (or one of many other possible forms), as will be well understood by one of ordinary skill in this art. This completes the detailed description of the circuit connections of the invention.

OPERATION OF THE PREFERRED EMBODIMENT OF THE INVENTION

If, for example, the constant current generator 36, connected to input terminal 30 of the invention is designed to produce a constant current of five microamperes through Q_7, a first current mirror A, comprising Q_7 and Q_5, may be adjusted so that Q_5 also passes five microamperes of current by making the ratios of the width to length of the gates of each of Q_7 and Q_5 equal (a 1:1 ratio of these ratios). When transistors Q_4 and Q_8 are turned off by a low input logic voltage appearing on input terminal 20, transistor Q_5 provides the required five microamperes electron flow to the drain electrode of transistor Q_9.

MOSFET transistors Q_9 and Q_{10} comprise a second current mirror circuit. Therefore, Q_{10} provides five microamperes to transistor Q_6, if the ratio of the ratios of gate widths to lengths of Q_9 and Q_{10}, respectively, are equal. Transistors Q_6 and Q_3 comprise still a third current mirror C, but with a difference. The gate size ratio between these two transistors may be 20:1 so that transistor Q_3 may provide 100 microamperes for the purpose of charging load capacitor 34. The electron charging path for the 100 microampere charging current is from ground, through capacitor 34 and transistor Q_3 to the positive supply, V_{CC} 18, thereby charging capacitor 34 negative on its grounded side and positive on its upper side.

When MOSFET transistors Q_4 and Q_8 are turned on by a "high" logic signal on input terminal 20, Q_8 provides the required five microamperes to transistor Q_5, shunts Q_9, turning it off and therefore transistors Q_9 and Q_{10} are also turned off. Transistor Q_6 is turned off and its mirror transistor, Q_3 is also turned off. Input MOSFET transistor Q_4 is then effectively a low impedance shunt switch across load capacitor 34 and provides

approximately 100 microamperes of discharge current to load capacitor 34.

Since only one of the two high current carrying transistors Q_3 and Q_4 are turned on at any one time, the maximum current drawn by these two transistors does not exceed that drawn by either of them. Furthermore, since the charge and discharge currents for capacitor 34 are essentially equal, the charge and discharge times are also essentially equal and the propagation delay time in either case may be made to be equal or nearly so. The input turn on and turn off voltages are not affected by variations in supply voltage 18, since both turn on and turn off voltages are controlled a constant current, ultimately controlled by constant current generator 36.

While the invention has been particularly shown and described herein with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various other modifications and changes may be made to the present invention from the principles of the invention as herein described without departing from the spirit and scope as encompassed in the accompanying claims. Therefore, it is intended in the appended claims to cover all such equivalent variations which may come within the scope of the invention as described.

WHAT IS CLAIMED IS:

1. A TTL compatible CMOS input circuit for providing a charging and a discharging current to an essentially capacitive load connected to an output terminal of the CMOS input circuit, the CMOS input circuit characterized by:

a plurality of current mirror transistor pair circuits for providing a charging current to the capacitive load, each of said plurality of current mirror transistor pair circuits having a constant current input terminal and a mirror current terminal, said constant current input terminal of a first of said plurality of current mirror transistor pair circuits being connected for accepting a reference current from a constant current generator, said constant current input terminal of a second of said plurality of current mirror transistor pair circuits being connected to said mirror current terminal of said first of said plurality of current mirror transistor pair circuits, said mirror current terminal of said second of said plurality of current mirror transistor pair circuits being connected to said constant current input terminal of a third of said plurality of current mirror transistor pair circuits, said mirror current terminal of said third of said plurality of current mirror transistor pair circuits being connected to said load capacitance; and

a switching circuit, said switching circuit being connected for switching at least one of said plurality of current mirror transistor pair circuits from a first state to a second state in response to a TTL logic level shift at an input terminal of said switching circuit, wherein said first state is one of an "off" and "on" state and said second state is the other of said "off" and "on" state, said switching circuit having a first and a second output terminal, said first output terminal of said switching circuit being connected to said constant current input terminal of said second of said plurality of said current mirror transistor pair circuits, said second output terminal of said switching circuit being connected to said current

mirror terminal of said third of said plurality of said current mirror transistor pair circuits for discharging said capacitive load.

2. The CMOS input circuit according to the circuit of claim 1 wherein said plurality of current mirror transistor pair circuits are further characterized by:

a first and a second MOSFET transistor, both of said first and second MOSFET transistors being of a single type chosen from the group, N-type and P-type, each of said first MOSFET transistors having a gate electrode thereof connected to a drain electrode thereof and to a gate electrode of said second MOSFET transistor of said current mirror transistor pair circuit.

3. A compatible circuit for translating a TTL input signal level to a CMOS circuit signal level for driving a CMOS circuit load, the CMOS circuit load comprising an essentially capacitive load, the input TTL signal having one of two states, in which:

the capacitive load being charged in response to a first of the two TTL input states, said charging being accomplished by means of a plurality of current mirror circuits each of said plurality of current mirror circuits comprising a transistor pair, each of said transistor pairs being of a single type chosen from N-type and P-type MOSFETs, each of said plurality of current mirror circuits having a constant current input terminal and a mirror current terminal, a first of said constant current input terminals of a first of said plurality of current mirror circuits for connection to a constant current generator, a corresponding first mirror current terminal of said first of said plurality of current mirror circuits being connected to a second constant current input terminal of a second of said plurality of current mirror circuits, a corresponding second mirror current terminal of said second of said plurality of current mirror circuits being connected to a third constant current input terminal of a third of said plurality of current mirror circuits, a corresponding third mirror

current terminal of said third of said plurality of current mirror circuits being connected to the capacitive load; and

the capacitive load is discharged in response to a second of the two TTL input states, said discharging being accomplished by means of a switching circuit, said switching circuit having two output terminals, a first of said two output terminals being utilized to control turn on and turn off of at least one of the plurality of current mirror circuits, a second of said two output terminals being utilized to discharge the capacitive load.

4. The circuit according to claim 3 including a circuit for providing that only one of said switching circuit and said at least one of said plurality of current mirror circuits is turned on at any one point in time.

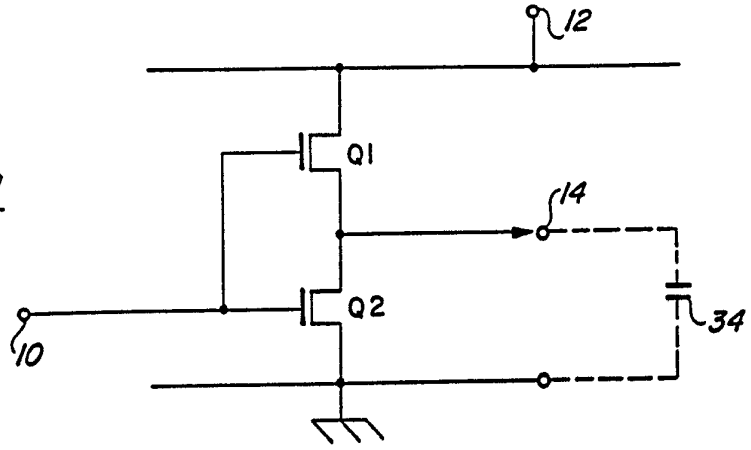


FIG. 1
(PRIOR ART)

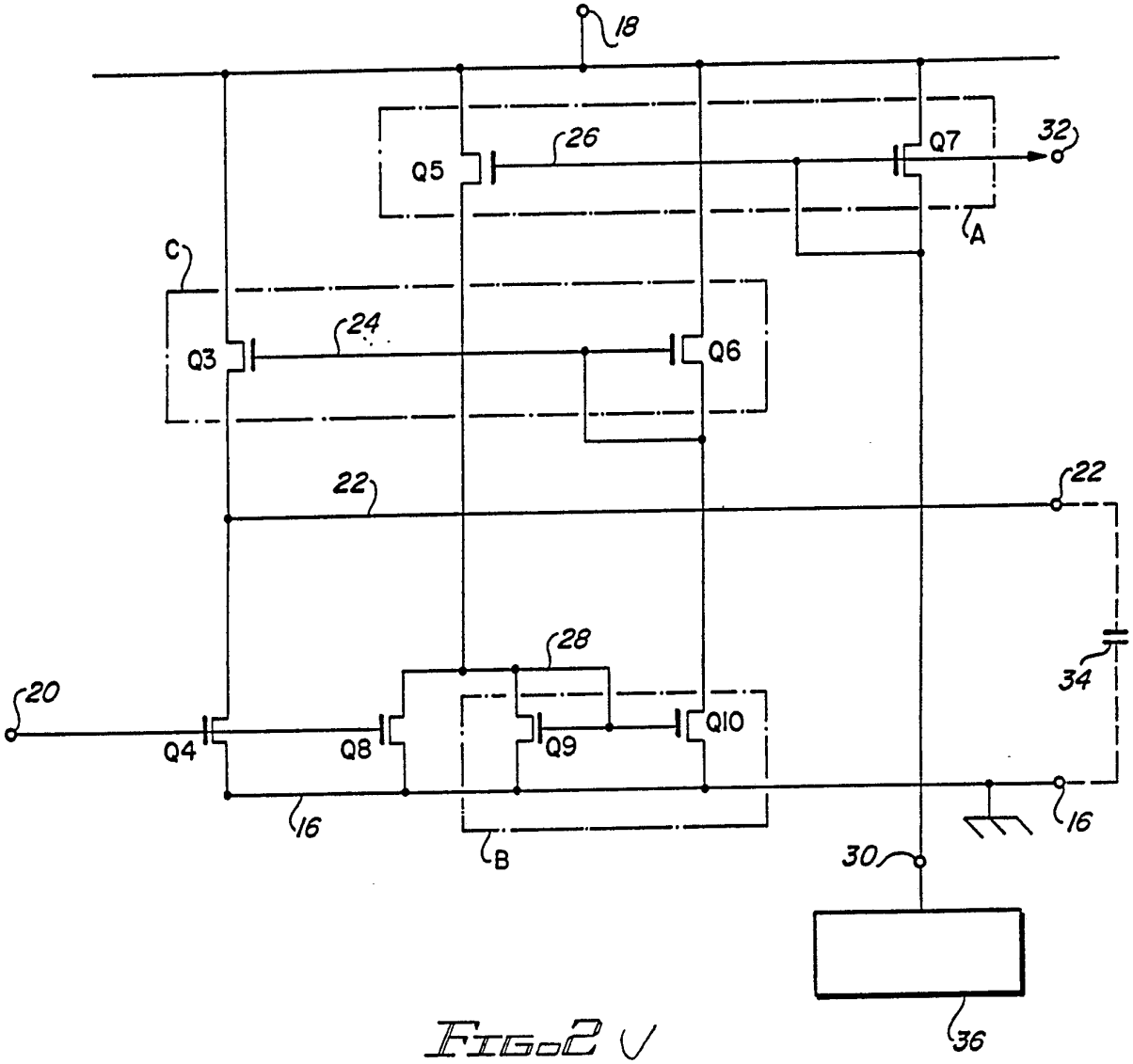


FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No PCT/US87/03166

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(4): H03K 19/092, 17/687, 19/094; G05F 3/16
U.S Cl. 307/475, 451, 576, 579, 585; 270; 323/315

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System [5]	Classification Symbols
U.S.	307/110, 443; 323/316, 317; 320/1

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [6]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [15]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 4,587,447 (Baehring) 06 May 1986	
A	US, A, 4584491 (Ulmer) 22 April 1986	
A	US, A, 4578600 (Magee) 25 March 1986	
A	US, A, 4555642 (Morales) 26 November 1985	
A	US, A, 4490633 (Noufer et al) 25 December 1984	
A	US, A, 4485317 (Davies, Jr) 27 November 1984	
A	US, A, 4475050 (Noufer et al) 02 October 1984	
A	US, A, 4471242 (Noufer et al) 11 September 1984	
A	US, A, 4469959 (Luke et al) 04 September 1984	
A	US, A, 4438352 (Mardkha) 20 March 1984	
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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
21 January 1988	28 MAR 1988
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Trong Quang Phan