



(51) International Patent Classification:

H10K 59/126 (2023.01)

(21) International Application Number:

PCT/CN2023/096999

(22) International Filing Date:

30 May 2023 (30.05.2023)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicants: BOE TECHNOLOGY GROUP CO., LTD.

[CN/CN]; No.10 Jiuxianqiao Rd., Chaoyang District, Beijing 100015 (CN). CHENGDU BOE OPTOELECTRONICS TECHNOLOGY CO., LTD. [CN/CN]; No.1188 Hezuo Rd., (West Zone), Hi-Tech Development Zone, Chengdu, Sichuan 611731 (CN). BEIJING BOE TECHNOLOGY DEVELOPMENT CO., LTD. [CN/CN]; Room 407, Building I, No.9 Dize Road, BDA, Daxing District, Beijing 100176 (CN).

(72) Inventors: GAO, Feifei; No.9 Dize Rd., BDA, Daxing District, Beijing 100176 (CN). HUANG, Yao; No.9 Dize Rd., BDA, Daxing District, Beijing 100176 (CN). LIU, Tingliang; No.9 Dize Rd., BDA, Daxing District, Beijing 100176 (CN). LIU, Lang; No.9 Dize Rd., BDA, Daxing District, Beijing 100176 (CN).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) Title: ARRAY SUBSTRATE AND DISPLAY APPARATUS

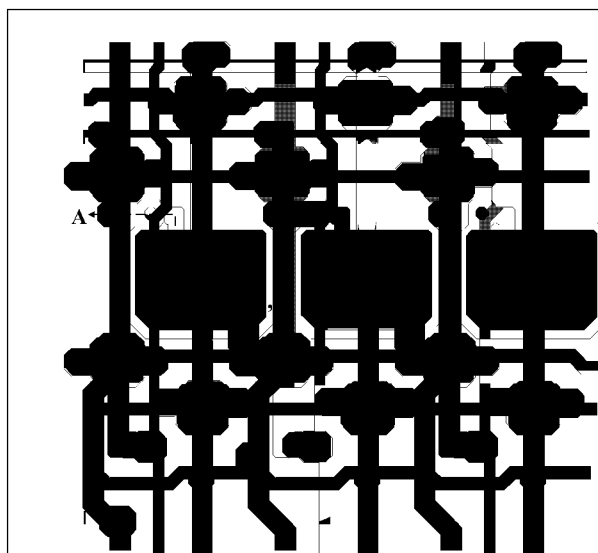


FIG. 3A

(57) Abstract: An array substrate is provided. The array substrate includes a plurality of pixel driving circuits. A respective pixel driving circuit of the plurality of pixel driving circuits comprises a driving transistor, a light shield, and a node connecting line. An orthographic projection of the light shield on a base substrate substantially covers an orthographic projection of an active layer of the driving transistor on the base substrate. The light shield is electrically connected to a gate electrode of the driving transistor through the node connecting line. The light shield, the node connecting line, and the gate electrode of the driving transistor are in three different layers.



(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

ARRAY SUBSTRATE AND DISPLAY APPARATUS

TECHNICAL FIELD

[0001] The present invention relates to display technology, more particularly, to an array substrate and a display apparatus.

BACKGROUND

[0002] Organic Light Emitting Diode (OLED) display is one of the hotspots in the field of flat panel display research today. Unlike Thin Film Transistor-Liquid Crystal Display (TFT-LCD), which uses a stable voltage to control brightness, OLED is driven by a driving current required to be kept constant to control illumination. The OLED display panel includes a plurality of pixel units configured with pixel-driving circuits arranged in multiple rows and columns. Each pixel-driving circuit includes a driving transistor having a gate terminal connected to one gate line per row and a drain terminal connected to one data line per column. When the row in which the pixel unit is gated is turned on, the switching transistor connected to the driving transistor is turned on, and the data voltage is applied from the data line to the driving transistor via the switching transistor, so that the driving transistor outputs a current corresponding to the data voltage to an OLED device. The OLED device is driven to emit light of a corresponding brightness.

SUMMARY

[0003] In one aspect, the present disclosure provides an array substrate, comprising a plurality of pixel driving circuits; wherein a respective pixel driving circuit of the plurality of pixel driving circuits comprises a driving transistor, a light shield, and a node connecting line; wherein an orthographic projection of the light shield on a base substrate substantially covers an orthographic projection of an active layer of the driving transistor on the base substrate; the light shield is electrically connected to a gate electrode of the driving transistor through the node connecting line; the light shield, the node connecting line, and the gate electrode of the driving transistor are in three different layers.

[0004] Optionally, the respective pixel driving circuit further comprises a first reset transistor; wherein the light shield is electrically connected to a second electrode of the first reset transistor through the node connecting line.

[0005] Optionally, the respective pixel driving circuit further comprises a storage capacitor; wherein the orthographic projection of the light shield on the base substrate substantially covers an orthographic projection of a gate electrode of the driving transistor on the base substrate, and substantially covers an orthographic projection of a second capacitor electrode of the storage capacitor on the base substrate.

[0006] Optionally, the array substrate further comprises a plurality of third voltage supply lines; wherein the respective pixel driving circuit further comprises a light emitting control transistor, and a second reset transistor; an orthographic projection of a respective third voltage supply line of the plurality of third voltage supply lines on the base substrate substantially covers an orthographic projection of an active layer of the light emitting control transistor in the respective pixel driving circuit on the base substrate, substantially covers an orthographic projection of an active layer of the second reset transistor on the base substrate, and at least partially overlaps with the orthographic projection of the active layer of the driving transistor on the base substrate.

[0007] Optionally, the orthographic projection of a respective third voltage supply line of the plurality of third voltage supply lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the light emitting control transistor in the respective pixel driving circuit on the base substrate; substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the second reset transistor on the base substrate; substantially covers an orthographic projection of a combination of a first electrode and a second electrode of the driving transistor on the base substrate; and at least partially overlaps with an orthographic projection of an active layer of the driving transistor on the base substrate.

[0008] Optionally, the array substrate further comprises a plurality of fourth voltage supply lines; wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor; in a first column of pixel driving circuits, an orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate.

[0009] Optionally, in the first column of pixel driving circuits, the orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the first reset transistor in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of a combination of an active layer and a second electrode of the data write transistor in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate.

[0010] Optionally, the array substrate further comprises a plurality of fourth reset signal lines; wherein the respective pixel driving circuit further comprises a data write transistor and a first

reset transistor; in a second column of pixel driving circuits, an orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate.

[0011] Optionally, in the second column of pixel driving circuits, the orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the first reset transistor in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate; and substantially covers an orthographic projection of a combination of an active layer and a second electrode of the data write transistor in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate.

[0012] Optionally, the array substrate further comprises a plurality of third reset signal lines; wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor; in a third column of pixel driving circuits, an orthographic projection of a respective third reset signal line of the plurality of third reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate.

[0013] Optionally, in the third column of pixel driving circuits, the orthographic projection of a respective third reset signal line of the plurality of third reset signal lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the first reset transistor in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate; and substantially covers an orthographic projection of a combination of an active layer and a second electrode of the data write transistor in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate.

[0014] Optionally, the array substrate further comprises a plurality of fourth voltage supply lines; wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor; pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; in the $(3k-2)$ -th column of pixel driving circuits, an

orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a first respective pixel driving circuit in the $(3k-2)$ -th column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the first respective pixel driving circuit in the $(3k-2)$ -th column of pixel driving circuits on the base substrate.

[0015] Optionally, the array substrate further comprises a plurality of fourth reset signal lines; wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor; pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; in the $(3k-1)$ -th column of pixel driving circuits, an orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a second respective pixel driving circuit in the $(3k-1)$ -th column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the second respective pixel driving circuit in the $(3k-1)$ -th column of pixel driving circuits on the base substrate.

[0016] Optionally, the array substrate further comprises a plurality of third reset signal lines; wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor; pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; in the $(3k)$ -th column of pixel driving circuits, an orthographic projection of a respective third reset signal line of the plurality of third reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a third respective pixel driving circuit in the $(3k)$ -th column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the third respective pixel driving circuit in the $(3k)$ -th column of pixel driving circuits on the base substrate.

[0017] Optionally, the array substrate further comprises a plurality of fourth voltage supply lines, a plurality of fourth reset signal lines, and a plurality of third reset signal lines in a same layer;

wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; the $(3k-2)$ -th column comprises a fourth voltage supply line of the plurality of fourth voltage supply lines; the $(3k-1)$ -th column comprises a fourth reset signal line of the plurality of fourth reset signal lines; and the $(3k)$ -th column comprises a third reset signal line of the plurality of third reset signal lines.

[0018] Optionally, the plurality of fourth voltage supply lines are absent in the $(3k-1)$ -th column and absent in the $(3k)$ -th column; the plurality of fourth reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k)$ -th column; and the plurality of third reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k-1)$ -th column.

[0019] Optionally, the array substrate further comprises a first voltage supply network and a second voltage supply network; wherein the first voltage supply network comprises a plurality of first voltage supply lines and a plurality of third voltage supply lines interconnected to each other; the plurality of first voltage supply lines extend along a direction substantially parallel to a first direction; the plurality of third voltage supply lines extend along a direction substantially parallel to a second direction; a respective first voltage supply line of the plurality of first voltage supply lines is connected to one or more third voltage supply lines of the plurality of third voltage supply lines; a respective third voltage supply line of the plurality of third voltage supply lines is connected to one or more first voltage supply lines of the plurality of first voltage supply lines; and wherein the second voltage supply network comprises a plurality of second voltage supply lines and a plurality of fourth voltage supply lines interconnected to each other; the plurality of second voltage supply lines extend along a direction substantially parallel to the first direction; the plurality of fourth voltage supply lines extend along a direction substantially parallel to the second direction; a respective second voltage supply line of the plurality of second voltage supply lines is connected to one or more fourth voltage supply lines of the plurality of fourth voltage supply lines; and a respective fourth voltage supply line of the plurality of fourth voltage supply lines is connected to one or more second voltage supply lines of the plurality of second voltage supply lines; wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; the plurality of third voltage supply lines are present in the $(3k-2)$ -th column, present in the $(3k-1)$ -th column, and present in the $(3k)$ -th column; the plurality of fourth voltage supply lines are absent in the $(3k-1)$ -th column and absent in the $(3k)$ -th column.

[0020] Optionally, the array substrate further comprises a first reset signal network; wherein the first reset signal network comprises a plurality of first reset signal lines and a plurality of third reset signal lines interconnected to each other; the plurality of first reset signal lines extend along a direction substantially parallel to a first direction; the plurality of third reset signal lines extend along a direction substantially parallel to a second direction; a respective first reset signal line of the plurality of first reset signal lines is connected to one or more third reset signal lines of the plurality of third reset signal lines; and a respective third reset signal line of the plurality of third reset signal lines is connected to one or more first reset signal lines of the plurality of first reset signal lines; wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column

of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; and the plurality of third reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k-1)$ -th column.

[0021] Optionally, the array substrate further comprises a second reset signal network; wherein the second reset signal network comprises a plurality of second reset signal lines and a plurality of fourth reset signal lines interconnected to each other; the plurality of second reset signal lines extend along a direction substantially parallel to a first direction; the plurality of fourth reset signal lines extend along a direction substantially parallel to a second direction; a respective second reset signal line of the plurality of second reset signal lines is connected to one or more fourth reset signal lines of the plurality of fourth reset signal lines; and a respective fourth reset signal line of the plurality of fourth reset signal lines is connected to one or more second reset signal lines of the plurality of second reset signal lines; wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; and the plurality of fourth reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k)$ -th column.

[0022] In another aspect, the present disclosure provides a display apparatus, comprising the array substrate described herein, and one or more integrated circuits connected to the array substrate.

BRIEF DESCRIPTION OF THE FIGURES

[0023] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present invention.

[0024] FIG. 1 is a plan view of an array substrate in some embodiments according to the present disclosure.

[0025] FIG. 2A is a circuit diagram illustrating the structure of a pixel driving circuit in some embodiments according to the present disclosure.

[0026] FIG. 2B is a timing diagram illustrating the operation of a pixel driving circuit in some embodiments according to the present disclosure.

[0027] FIG. 3A is a diagram illustrating the structure of a portion of an array substrate in some embodiments according to the present disclosure.

[0028] FIG. 3B is a schematic diagram illustrating an arrangement of a plurality of pixel driving circuits in a portion of an array substrate depicted in FIG. 3A.

[0029] FIG. 3C is a diagram illustrating the structure of a light shield layer in the portion of the array substrate depicted in FIG. 3A.

[0030] FIG. 3D is a diagram illustrating the structure of a first conductive layer in the portion of the array substrate depicted in FIG. 3A.

[0031] FIG. 3E is a diagram illustrating the structure of a first gate insulating layer in the portion of the array substrate depicted in FIG. 3A.

[0032] FIG. 3F is a diagram illustrating the structure of a semiconductor material layer in the portion of the array substrate depicted in FIG. 3A.

[0033] FIG. 3G is a diagram illustrating the structure of a second conductive layer in the portion of the array substrate depicted in FIG. 3A.

[0034] FIG. 3H is a diagram illustrating the structure of a passivation layer in the portion of the array substrate depicted in FIG. 3A.

[0035] FIG. 3I is a diagram illustrating the structure of a first signal line layer in the portion of the array substrate depicted in FIG. 3A.

[0036] FIG. 3J is a diagram illustrating the structure of a first planarization layer in the portion of the array substrate depicted in FIG. 3A.

[0037] FIG. 3K is a diagram illustrating the structure of a second signal line layer in the portion of the array substrate depicted in FIG. 3A.

[0038] FIG. 3L is a diagram illustrating the structure of a second planarization layer in the portion of the array substrate depicted in FIG. 3A.

[0039] FIG. 4A is a cross-sectional view along an A-A' line in FIG. 3A.

[0040] FIG. 4B is a cross-sectional view along a B-B' line in FIG. 3A.

[0041] FIG. 5 is a diagram illustrating the structure of a first voltage supply network in a portion of an array substrate in some embodiments according to the present disclosure.

[0042] FIG. 6 is a diagram illustrating the structure of a second voltage supply network in a portion of an array substrate in some embodiments according to the present disclosure.

[0043] FIG. 7 is a diagram illustrating the structure of a first reset signal network in a portion of an array substrate in some embodiments according to the present disclosure.

[0044] FIG. 8 is a diagram illustrating the structure of a second reset signal network in a portion of an array substrate in some embodiments according to the present disclosure.

[0045] FIG. 9 is a diagram illustrating the structure of a semiconductor material layer and a second signal line layer in the portion of the array substrate depicted in FIG. 3A.

DETAILED DESCRIPTION

[0046] The disclosure will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of some embodiments are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

[0047] The present disclosure provides, *inter alia*, an array substrate and a display apparatus that substantially obviate one or more of the problems due to limitations and disadvantages of the related art. In one aspect, the present disclosure provides an array substrate. In some embodiments, the array substrate includes a plurality of pixel driving circuits. Optionally, a respective pixel driving circuit of the plurality of pixel driving circuits comprises a driving transistor, a light shield, and a node connecting line. Optionally, an orthographic projection of the light shield on a base substrate substantially covers an orthographic projection of an active layer of the driving transistor on the base substrate. Optionally, the light shield is electrically connected to a gate electrode of the driving transistor through the node connecting line. Optionally, the light shield, the node connecting line, and the gate electrode of the driving transistor are in three different layers.

[0048] Various appropriate pixel driving circuits may be used in the present array substrate. Examples of appropriate driving circuits include 3T1C, 2T1C, 4T1C, 4T2C, 5T2C, 6T1C, 7T1C, 7T2C, 8T1C, and 8T2C. In some embodiments, the respective one of the plurality of pixel driving circuits is a 5T1C driving circuit. In alternative embodiments, the respective one of the plurality of pixel driving circuits is a 5T2C driving circuit. Various appropriate light emitting elements may be used in the present array substrate. Examples of appropriate light emitting elements include organic light emitting diodes, quantum dots light emitting diodes, and micro light emitting diodes. Optionally, the light emitting element is micro light emitting diode. Optionally, the light emitting element is an organic light emitting diode including an organic light emitting layer.

[0049] FIG. 1 is a plan view of an array substrate in some embodiments according to the present disclosure. Referring to FIG. 1, the array substrate includes an array of subpixels Sp. Each subpixel includes an electronic component, e.g., a light emitting element. In one example, the light emitting element is driven by a respective pixel driving circuit PDC. The array substrate includes a plurality of gate lines GL, a plurality of data lines DL, a plurality of voltage supply lines Vdd (e.g., a plurality of first voltage supply lines or a plurality of third voltage supply lines). Light emission in a respective subpixel Sp is driven by a respective pixel driving circuit PDC. In one example, a high voltage signal (e.g., a VDD signal) is input, through a respective voltage supply line of the plurality of voltage supply line Vdd, to the respective pixel driving circuit PDC connected to an anode of the light emitting element; a low voltage signal (e.g., a VSS signal) is input, through a low voltage supply line, to a cathode of

the light emitting element. A voltage difference between the high voltage signal (e.g., the VDD signal) and the low voltage signal (e.g., the VSS signal) is a driving voltage ΔV that drives light emission in the light emitting element.

[0050] FIG. 2A is a circuit diagram illustrating the structure of a pixel driving circuit in some embodiments according to the present disclosure. Referring to FIG. 2A, in some embodiments, the pixel driving circuit includes a driving transistor Td; a storage capacitor Cst having a first capacitor electrode Ce1 and a second capacitor electrode Ce2; a data write transistor Tw having a gate electrode connected to a respective gate line of a plurality of gate lines GL, a first electrode connected to a respective data line of a plurality of data lines DL, and a second electrode connected to a gate electrode of the driving transistor Td; a first reset transistor Tr1 having a gate electrode connected to a respective first reset control signal line of a plurality of first reset control signal lines rst1, a first electrode connected to a respective first reset signal line of a plurality of first reset signal lines Vint1, and a second electrode connected to a first capacitor electrode Ce1 of the storage capacitor Cst, the second electrode of the data write transistor Tw, and the gate electrode of the driving transistor Td; a second reset transistor Tr2 having a gate electrode connected to a second reset control signal line of a plurality of second reset control signal lines rst2, a first electrode connected to a respective second reset signal line of a plurality of second reset signal lines Vint2, and a second electrode connected to the second electrode of the driving transistor, the second capacitor electrode Ce2 of the storage capacitor Cst, and an anode of a respective light emitting element LE; and a light emitting control transistor Te having a gate electrode connected to a respective light emitting control signal line of a plurality of light emitting control signal lines em, a first electrode connected to a respective voltage supply line of a plurality of voltage supply lines Vdd, and a second electrode connected to the first electrode of the driving transistor Td.

[0051] The pixel driving circuit further include a first node N1, a second node N2, and a third node N3. The first node N1 is connected to the gate electrode of the driving transistor Td, the first capacitor electrode Ce1, the second electrode of the data write transistor Tw, and the second electrode of the first reset transistor Tr1. The second node N2 is connected to the second electrode of the driving transistor Td, the second electrode of the second reset transistor Tr2, the second capacitor electrode Ce2 of the storage capacitor Cst, and the anode of the respective light emitting element LE. The third node N3 is connected to the second electrode of the light emitting control transistor Te and the first electrode of the driving transistor Td.

[0052] As used herein, a first electrode or a second electrode refers to one of a first terminal and a second terminal of a transistor, the first terminal and the second terminal being connected to an active layer of the transistor. A direction of a current flowing through the transistor may be configured to be from a first electrode to a second electrode, or from a second electrode to a first electrode. Accordingly, depending on the direction of the current flowing through the

transistor, in one example, the first electrode is configured to receive an input signal and the second electrode is configured to output an output signal; in another example, the second electrode is configured to receive an input signal and the first electrode is configured to output an output signal.

[0053] FIG. 2B is a timing diagram illustrating the operation of a pixel driving circuit in some embodiments according to the present disclosure. Referring to FIG. 2A and FIG. 2B, during one frame of image, the operation of the pixel driving circuit includes a reset sub-phase t1, a compensating sub-phase t2, a data write sub-phase t3, and a light emitting sub-phase t4.

[0054] In the reset sub-phase t1, a turning-on reset control signal is provided through the respective first reset control signal line of the plurality of first reset control signal lines rst1 to the gate electrode of the first reset transistor Tr1 to turn on the first reset transistor Tr1; allowing an initialization voltage signal from the respective first reset signal line of the plurality of first reset signal lines Vint1 to pass from a first electrode of the first reset transistor Tr1 to a second electrode of the first reset transistor Tr1, and in turn to the first capacitor electrode Ce1, the gate electrode of the driving transistor Td, and the node N1. The gate electrode of the driving transistor Td is initialized. A turning-on reset control signal is provided through the respective second reset control signal line of the plurality of second reset control signal line rst2 to the gate electrode of the second reset transistor Tr2 to turn on the second reset transistor Tr2; allowing an initialization voltage signal from the respective second reset signal line of the plurality of second reset signal lines Vint2 to pass from a first electrode of the second reset transistor Tr2 to a second electrode of the second reset transistor Tr2; and in turn to the node N2. The anode of the light emitting element LE is initialized.

[0055] In the compensating sub-phase t2, a turning-on light emitting control signal is provided through the respective light emitting control signal line of the plurality of light emitting control signal lines em to the gate electrode of the light emitting control transistor Te to turn on the light emitting control transistor Te. The second electrode of the driving transistor Td (e.g., the N2 node denoted in FIG. 2A) is charged until the voltage level at the second electrode of the driving transistor Td reaches a level of a reset signal provided by the respective first reset signal line of the plurality of first reset signal lines Vint1 minus a voltage level of a threshold voltage V_{th} of the driving transistor Td.

[0056] In the data write sub-phase t3, a turning-on gate scanning signal is provided through the respective gate line of the plurality of gate lines GL to the gate electrode of the data write transistor Tw to turn on the data write transistor Tw; allowing a data signal to pass from the first electrode of the data write transistor Tw to the second electrode of the data write transistor Tw, and in turn to the node N1. a voltage level at the gate electrode of the driving transistor Td reaches a voltage level of the data signal written to the gate electrode of the driving transistor Td. A capacitance of the storage capacitor Cst is far less than a capacitance of parasitic

capacitance between a cathode of the light emitting element and the second capacitor electrode Ce2. The change in the voltage level at the gate electrode of the driving transistor Td does not affect the voltage level at the second electrode of the driving transistor Td (e.g., the N2 node). The voltage level at the second electrode of the driving transistor Td remains at the level of the reset signal provided by the respective first reset signal line of the plurality of first reset signal lines Vint1 minus the voltage level of the threshold voltage Vth of the driving transistor Td.

[0057] In the light emitting sub-phase t4, a turning-on light emitting control signal is provided through the respective light emitting control signal line of the plurality of light emitting control signal lines em to the gate electrode of the light emitting control transistor Te to turn on the light emitting control transistor Te. In the light emitting sub-phase t4, the driving transistor Td remains turned on. The light emitting element emits light. The voltage level at the N2 node changes to (Voled + Vss), wherein Voled stands for a voltage level for driving the light emitting element to emit light, Vss stands for a voltage level at the cathode of the light emitting element. Thus, the change in the voltage level at the N2 node is (Voled + Vss – (Vint1 – Vth)), wherein Vint1 stands for the level of the reset signal provided by the respective first reset signal line of the plurality of first reset signal lines Vint1, and Vth stands for the voltage level of the threshold voltage Vth of the driving transistor Td. Due to the bootstrapping effect of the storage capacitor Cst, the voltage level at the N1 node (the gate electrode of the driving transistor Td) becomes (Vdata + Vn2), wherein Vdata stands for the voltage level of the data signal, Vn2 stands for the change in the voltage level at the N2 node. The voltage level at the N1 node is Vdata + Voled + Vss – Vint1 + Vth. A voltage difference Vgs between the gate electrode and the second electrode of the driving transistor Td is (Vdata – Vint1 + Vth). A driving current I flowing through the driving transistor is correlated to (Vdata – Vint1)².

[0058] The present disclosure may be implemented in pixel driving circuit having transistors of various types, including a pixel driving circuit having p-type transistors, a pixel driving circuit having n-type transistors, and a pixel driving circuit having one or more p-type transistors and one or more n-type transistors. For a p-type transistor, an effective control signal (e.g., a turn-on control signal) is a low voltage signal, and an ineffective control signal (e.g., a turn-off control signal) is a high voltage signal. For an n-type transistor, an effective control signal (e.g., a turn-on control signal) is a high voltage signal, and an ineffective control signal (e.g., a turn-off control signal) is a low voltage signal. Referring to FIG. 2A, in some embodiments, all transistors in the pixel driving circuit are n-type transistors such as a metal oxide transistor.

[0059] The array substrate in some embodiments includes a plurality of subpixels. In some embodiments, the plurality of subpixels includes a respective first subpixel, a respective second subpixel, and a respective third subpixel. Optionally, a respective pixel of the array substrate includes the respective first subpixel, the respective second subpixel, and the respective third

subpixel. The plurality of subpixels in the array substrate are arranged in an array. In one example, the array of the plurality of subpixels includes a S1-S2-S3 format repeating array, in which S1 stands for the respective first subpixel, S2 stands for the respective second subpixel, and S3 stands for the respective third subpixel. In another example, the S1-S2-S3 format is a C1-C2-C3 format, in which C1 stands for the respective first subpixel of a first color, C2 stands for the respective second subpixel of a second color, and C3 stands for the respective third subpixel of a third color. In another example, the C1-C2-C3 format is an R-G-B format, in which the respective first subpixel is a red subpixel, the respective second subpixel is a green subpixel, and the respective third subpixel is a blue subpixel.

[0060] In another example, the array of the plurality of subpixels includes a S1-S2-S3-S4 format repeating array, in which S1 stands for the respective first subpixel, S2 stands for the respective second subpixel, S3 stands for the respective third subpixel, and S4 stands for the respective fourth subpixel. In another example, the S1-S2-S3-S4 format is a C1-C2-C3-C4 format, in which C1 stands for the respective first subpixel of a first color, C2 stands for the respective second subpixel of a second color, C3 stands for the respective third subpixel of a third color, and C4 stands for the respective fourth subpixel of a fourth color. In another example, the S1-S2-S3-S4 format is a C1-C2-C3-C2' format, in which C1 stands for the respective first subpixel of a first color, C2 stands for the respective second subpixel of a second color, C3 stands for the respective third subpixel of a third color, and C2' stands for the respective fourth subpixel of the second color. In another example, the C1-C2-C3-C2' format is a R-G-B-G format, in which the respective first subpixel is a red subpixel, the respective second subpixel is a green subpixel, the respective third subpixel is a blue subpixel, and the respective fourth subpixel is a green subpixel.

[0061] In some embodiments, a minimum repeating unit of the plurality of subpixels of the array substrate includes a respective first subpixel, a respective second subpixel, and a respective third subpixel. Optionally, each of the respective first subpixel, the respective second subpixel, and the respective third subpixel, includes the data write transistor Tw, the first reset transistor Tr1, the second reset transistor Tr2, the light emitting control transistor Te, the driving transistor Td, and the storage capacitor Cst.

[0062] In alternative embodiments, a minimum repeating unit of the plurality of subpixels of the array substrate includes a respective first subpixel, a respective second subpixel, a respective third subpixel, and a respective fourth subpixel. Optionally, each of the respective first subpixel, the respective second subpixel, the respective third subpixel, and the respective fourth subpixel, includes the data write transistor Tw, the first reset transistor Tr1, the second reset transistor Tr2, the light emitting control transistor Te, the driving transistor Td, and the storage capacitor Cst.

[0063] FIG. 3A is a diagram illustrating the structure of a portion of an array substrate in some embodiments according to the present disclosure. FIG. 3B is a schematic diagram illustrating an arrangement of a plurality of pixel driving circuits in a portion of an array substrate depicted in FIG. 3A. FIG. 3A and FIG. 3B depicts a portion of the array substrate having three pixel driving circuits, including PDC1, PDC2, and PDC3.

[0064] FIG. 3C is a diagram illustrating the structure of a light shield layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3D is a diagram illustrating the structure of a first conductive layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3E is a diagram illustrating the structure of a first gate insulating layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3F is a diagram illustrating the structure of a semiconductor material layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3G is a diagram illustrating the structure of a second conductive layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3H is a diagram illustrating the structure of a passivation layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3I is a diagram illustrating the structure of a first signal line layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3J is a diagram illustrating the structure of a first planarization layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3K is a diagram illustrating the structure of a second signal line layer in the portion of the array substrate depicted in FIG. 3A. FIG. 3L is a diagram illustrating the structure of a second planarization layer in the portion of the array substrate depicted in FIG. 3A. FIG. 4A is a cross-sectional view along an A-A' line in FIG. 3A. FIG. 4B is a cross-sectional view along a B-B' line in FIG. 3A.

[0065] Referring to FIG. 3A to FIG. 3L, and FIG. 4A to FIG. 4B, in some embodiments, the array substrate includes a base substrate BS, a light shield layer LSL on the base substrate BS, an insulating layer IN on a side of the light shield layer LSL away from the base substrate BS, a first conductive layer CT1 on a side of the insulating layer IN away from the light shield layer LSL, a first gate insulating layer GI1 on a side of the first conductive layer CT1 away from the insulating layer IN, a semiconductor material layer SML on a side of the first gate insulating layer GI1 away from the first conductive layer CT1, a second gate insulating layer GI2 on a side of the semiconductor material layer SML away from the first gate insulating layer GI1, a second conductive layer CT2 on a side of the second gate insulating layer GI2 away from the semiconductor material layer SML, a passivation layer PVX on a side of the second conductive layer CT2 away from the second gate insulating layer GI2, a first signal line layer SD1 on a side of the passivation layer PVX away from the second conductive layer CT2, a first planarization layer PLN1 on a side of the first signal line layer SD1 away from the passivation layer PVX, a second signal line layer SD2 on a side of the first planarization layer PLN1 away from the first signal line layer SD1, and a second planarization layer PLN2 on a side of the second signal line layer SD2 away from the first planarization layer PLN1.

[0066] Referring to FIG. 2A, FIG. 3A, and FIG. 3C, in some embodiments, the light shield layer LSL includes a light shield LS. Various appropriate materials and various appropriate fabricating methods may be used for making the light shield layer LSL. For example, a metallic material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process. Examples of appropriate metallic materials for making the light shield layer LSL include, but are not limited to, aluminum, chromium, tungsten, titanium, tantalum, molybdenum, copper, and alloys or laminates containing the same.

[0067] In some embodiments, the array substrate includes a plurality of light shields respectively in a plurality of pixel driving circuits. The plurality of light shields are spaced apart from each other.

[0068] In some embodiments, referring to FIG. 2A, FIG. 3A, FIG. 3C, and FIG. 4A, an orthographic projection of the light shield LS on a base substrate BS substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of the active layer ACTd of the driving transistor Td on the base substrate BS. The inventors of the present disclosure discover that, by having this structure, the active layer ACTd of the driving transistor Td can be protected from irradiation and stabilized.

[0069] In some embodiments, the light shield LS is electrically connected to the gate electrode of the driving transistor Td (e.g., the first capacitor electrode Ce1 of the storage capacitor Cst which functions as the light shield LS). Optionally, the light shield LS is electrically connected to the gate electrode of the driving transistor Td through a node connecting line Cln in the first signal line layer SD1. The inventors of the present disclosure discover that, surprisingly and unexpectedly, by having the light shield LS electrically connected to the gate electrode of the driving transistor Td, the low grayscale driving capability of the driving transistor Td can be significantly improved, resulting in enhanced performance of the driving transistor Td.

[0070] In some embodiments, the light shield LS is electrically connected to the second electrode Dr1 of the first reset transistor Tr1. Optionally, the light shield LS is electrically connected to the second electrode Dr1 of the first reset transistor Tr1 through the node connecting line Cln in the first signal line layer SD1.

[0071] In some embodiments, an orthographic projection of the light shield LS on a base substrate BS substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of the gate electrode of the driving transistor Td on the base substrate BS.

[0072] In some embodiments, an orthographic projection of the light shield LS on a base substrate BS substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90%

covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of the second capacitor electrode Ce2 of the storage capacitor Cst on the base substrate BS.

[0073] Referring to FIG. 2A, FIG. 3A, and FIG. 3D, the first conductive layer in some embodiments includes a second capacitor electrode Ce2 of the storage capacitor Cst, a first gate electrode portion Gw-1 of the gate electrode of the data write transistor Tw, a first gate electrode portion Gr1-1 of the gate electrode of the first reset transistor Tr1, a first gate electrode portion Gr2-1 of the gate electrode of the second reset transistor Tr2, and a first gate electrode portion Ge-1 of the gate electrode of the light emitting control transistor Te. Various appropriate electrode materials and various appropriate fabricating methods may be used to make the first conductive layer. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the first conductive layer include, but are not limited to, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. Optionally, the second capacitor electrode Ce2 of the storage capacitor Cst, a first gate electrode portion Gw-1 of the gate electrode of the data write transistor Tw, the first gate electrode portion Gr1-1 of the gate electrode of the first reset transistor Tr1, the first gate electrode portion Gr2-1 of the gate electrode of the second reset transistor Tr2, and the first gate electrode portion Ge-1 of the gate electrode of the light emitting control transistor Te are in a same layer.

[0074] As used herein, the term “same layer” refers to the relationship between the layers simultaneously formed in the same step. In one example, the second capacitor electrode Ce2 and the first gate electrode portion Gw-1 are in a same layer when they are formed as a result of one or more steps of a same patterning process performed in a same layer of material. In another example, the second capacitor electrode Ce2 and the first gate electrode portion Gw-1 can be formed in a same layer by simultaneously performing the step of forming the second capacitor electrode Ce2, and the step of forming the first gate electrode portion Gw-1. The term “same layer” does not always mean that the thickness of the layer or the height of the layer in a cross-sectional view is the same.

[0075] Referring to FIG. 2A, FIG. 3A, FIG. 3D, and FIG. 3I, in some embodiments, the gate electrode of the data write transistor Tw includes one or more portions. In some embodiments, the first gate electrode portion Gw-1 of the gate electrode of the data write transistor Tw is connected to a respective gate line of the plurality of gate lines GL.

[0076] Referring to FIG. 2A, FIG. 3A, FIG. 3D, and FIG. 3I, in some embodiments, the gate electrode of the first reset transistor Tr1 includes one or more portions. In some embodiments,

the first gate electrode portion Gr1-1 of the gate electrode of the first reset transistor Tr1 is connected to a respective first reset control signal line of the plurality of first reset control signal lines rst1.

[0077] Referring to FIG. 2A, FIG. 3A, FIG. 3D, and FIG. 3I, in some embodiments, the gate electrode of the second reset transistor Tr2 includes one or more portions. In some embodiments, the first gate electrode portion Gr2-1 of the gate electrode of the second reset transistor Tr2 is connected to a respective second reset control signal line of the plurality of second reset control signal lines rst2.

[0078] Referring to FIG. 2A, FIG. 3A, FIG. 3D, and FIG. 3I, in some embodiments, the gate electrode of the light emitting control transistor Te includes one or more portions. In some embodiments, the first gate electrode portion Ge-1 of the gate electrode of the light emitting control transistor Te is connected to a respective light emitting control signal line of the plurality of light emitting control signal lines em.

[0079] Vias extending through the first gate insulating layer GI1 are depicted in FIG. 3E.

[0080] Referring to FIG. 2A, FIG. 3A, and FIG. 3F, the semiconductor material layer SML in some embodiments includes at least an active layer ACTd of the driving transistor Td, an active layer ACTr1 of the first reset transistor Tr1, an active layer ACTr2 of the second reset transistor Tr2, an active layer ACTw of the data write transistor Tw, and an active layer ACTe of the light emitting control transistor Te. Optionally, the semiconductor material layer SML further includes at least a portion of a first electrode Sd of the driving transistor Td, at least a portion of a first electrode Sr1 of the first reset transistor Tr1, at least a portion of a first electrode Sr2 of the second reset transistor Tr2, at least a portion of a first electrode Sw of the data write transistor Tw, and at least a portion of a first electrode Se of the light emitting control transistor Te. Optionally, the semiconductor material layer SML further includes at least a portion of a second electrode Dd of the driving transistor Td, at least a portion of a second electrode Dr1 of the first reset transistor Tr1, at least a portion of a second electrode Dr2 of the second reset transistor Tr2, at least a portion of a second electrode Dw of the data write transistor Tw, and at least a portion of a second electrode De of the light emitting control transistor Te. Optionally, the semiconductor material layer SML includes the active layer ACTd, the first electrode Sd, and the second electrode Dd of the driving transistor Td; the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1 of the first reset transistor Tr1; the active layer ACTr2, the first electrode Sr2, and the second electrode Dr2 of the second reset transistor Tr2; the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw; and the active layer ACTe, the first electrode Se, and the second electrode De of the light emitting control transistor Te. Various appropriate semiconductor materials may be used for making the semiconductor material layer SML. Examples of the semiconductor materials for making the semiconductor material layer SML

include metal oxide-based semiconductor material such as indium gallium zinc oxide and metal oxynitride-based semiconductor materials such as zinc oxynitride.

[0081] As used herein, the active layer refers to a component of the transistor comprising at least a portion of the semiconductor material layer whose orthographic projection on the base substrate overlaps with an orthographic projection of a gate electrode on the base substrate. A first electrode refers to a component of the transistor connected to one side of the active layer, and a second electrode refers to a component of the transistor connected to another side of the active layer. In the context of a double-gate type transistor, the active layer refers to a component of the transistor comprising a first portion of the semiconductor material layer whose orthographic projection on the base substrate overlaps with an orthographic projection of a first gate on the base substrate, a second portion of the semiconductor material layer whose orthographic projection on the base substrate overlaps with an orthographic projection of a second gate on the base substrate, and a third portion between the first portion and the second portion. In the context of a double-gate type transistor, a first electrode refers to a component of the transistor connected to a side of the first portion distal to the third portion, and a second electrode refers to a component of the transistor connected to a side of the second portion distal to the third portion.

[0082] FIG. 3F is annotated with labels indicating components of transistors in the pixel driving circuit. For example, the driving transistor Td includes an active layer ACTd, a first electrode Sd, and a second electrode Dd; the data write transistor Tw includes an active layer ACTw, a first electrode Sw, and a second electrode Dw; the light emitting control transistor Tw includes an active layer ACTe, a first electrode Se, and a second electrode De; the first reset transistor Tr1 includes an active layer ACTr1, a first electrode Sr1, and a second electrode Dr1; and the second reset transistor Tr2 includes an active layer ACTr2, a first electrode Sr2, and a second electrode Dr2. Optionally, the active layer ACTd of the driving transistor Td, the active layer ACTe of the light emitting control transistor Te, and the active layer ACTr2 of the second reset transistor Tr2 are parts of a first unitary structure. Optionally, the active layer ACTd, the first electrode Sd, and the second electrode Dd of the driving transistor Td; the active layer ACTe, the first electrode Se, and the second electrode De of the light emitting control transistor Te; and the active layer ACTr2, the first electrode Sr2, and the second electrode Dr2 of the second reset transistor Tr2 are parts of the first unitary structure. Optionally, the active layer ACTw of the data write transistor Tw and the active layer ACTr1 of the first reset transistor Tr1 are parts of a second unitary structure. Optionally, the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw and the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1 of the first reset transistor Tr1 are parts of the second unitary structure.

[0083] Referring to FIG. 2A, FIG. 3A, and FIG. 3G, the second conductive layer in some embodiments includes a first capacitor electrode Ce1 of the storage capacitor Cst, a second gate electrode portion Gw-2 of the gate electrode of the data write transistor Tw, a second gate electrode portion Gr1-2 of the gate electrode of the first reset transistor Tr1, a second gate electrode portion Gr2-2 of the gate electrode of the second reset transistor Tr2, and a second gate electrode portion Ge-2 of the gate electrode of the light emitting control transistor Te. Various appropriate electrode materials and various appropriate fabricating methods may be used to make the second conductive layer. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the second conductive layer include, but are not limited to, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. Optionally, the first capacitor electrode Ce1 of the storage capacitor Cst, the second gate electrode portion Gw-2 of the gate electrode of the data write transistor Tw, the second gate electrode portion Gr1-2 of the gate electrode of the first reset transistor Tr1, the second gate electrode portion Gr2-2 of the gate electrode of the second reset transistor Tr2, and the second gate electrode portion Ge-2 of the gate electrode of the light emitting control transistor Te are in a same layer.

[0084] Referring to FIG. 2A, FIG. 3A, FIG. 3G, and FIG. 3I, in some embodiments, the gate electrode of the data write transistor Tw includes one or more portions. In some embodiments, the second gate electrode portion Gw-2 of the gate electrode of the data write transistor Tw is connected to a respective gate line of the plurality of gate lines GL.

[0085] Referring to FIG. 2A, FIG. 3A, FIG. 3G, and FIG. 3I, in some embodiments, the gate electrode of the first reset transistor Tr1 includes one or more portions. In some embodiments, the second gate electrode portion Gr1-2 of the gate electrode of the first reset transistor Tr1 is connected to a respective first reset control signal line of the plurality of first reset control signal lines rst1.

[0086] Referring to FIG. 2A, FIG. 3A, FIG. 3G, and FIG. 3I, in some embodiments, the gate electrode of the second reset transistor Tr2 includes one or more portions. In some embodiments, the second gate electrode portion Gr2-2 of the gate electrode of the second reset transistor Tr2 is connected to a respective second reset control signal line of the plurality of second reset control signal lines rst2.

[0087] Referring to FIG. 2A, FIG. 3A, FIG. 3G, and FIG. 3I, in some embodiments, the gate electrode of the light emitting control transistor Te includes one or more portions. In some embodiments, the second gate electrode portion Ge-2 of the gate electrode of the light emitting

control transistor Te is connected to a respective light emitting control signal line of the plurality of light emitting control signal lines em.

[0088] Vias extending through the passivation layer PVX are depicted in FIG. 3H.

[0089] Referring to FIG. 2A, FIG. 3A, and FIG. 3I, the first signal line layer in some embodiments includes a node connecting line Cln, a plurality of first voltage supply lines Vdd1, a plurality of second voltage supply lines Vss1, a plurality of first reset signal lines Vint1, a plurality of second reset signal lines Vint2, a plurality of first reset control signal lines rst1, a plurality of second reset control signal lines rst2, a plurality of gate lines GL, a plurality of light emitting control signal lines em, a relay electrode RE, and a data signal connecting pad DCP.

[0090] Various appropriate conductive materials and various appropriate fabricating methods may be used to make the first signal line layer. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the first signal line layer include, but are not limited to, titanium, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. In some embodiments, the first signal line layer includes a plurality of sub-layers stacked together. In one example, the first signal line layer includes a stacked titanium/aluminum/titanium multi-layer structure. In another example, the first signal line layer includes a stacked molybdenum/aluminum/molybdenum multi-layer structure. Optionally, the node connecting line Cln, the plurality of first voltage supply lines Vdd1, the plurality of second voltage supply lines Vss1, the plurality of first reset signal lines Vint1, the plurality of second reset signal lines Vint2, the plurality of first reset control signal lines rst1, the plurality of second reset control signal lines rst2, the plurality of gate lines GL, and the plurality of light emitting control signal lines em, the relay electrode RE, and the anode connecting pad ACP are in a same layer.

[0091] In some embodiments, the plurality of first voltage supply lines Vdd1, the plurality of second voltage supply lines Vss1, the plurality of first reset signal lines Vint1, the plurality of second reset signal lines Vint2, the plurality of first reset control signal lines rst1, the plurality of second reset control signal lines rst2, the plurality of gate lines GL, and the plurality of light emitting control signal lines em extend along a direction substantially parallel to the first direction DR1, respectively. As used herein, the term “substantially parallel” means that an angle is in the range of 0 degree to approximately 45 degrees, e.g., 0 degree to approximately 5 degrees, 0 degree to approximately 10 degrees, 0 degree to approximately 15 degrees, 0 degree to approximately 20 degrees, 0 degree to approximately 25 degrees, 0 degree to approximately 30 degrees.

[0092] In some embodiments, the plurality of first voltage supply lines Vdd1 are configured to provide a first reference voltage signal (e.g., a high reference voltage signal); and the plurality of second voltage supply lines Vss1 are configured to provide a second reference voltage signal (e.g., a low reference voltage signal). Optionally, the first reference voltage signal is a constant voltage signal, the second reference voltage signal is a constant voltage signal, the first reference voltage signal has a voltage level higher than a voltage level of the second reference voltage signal.

[0093] The node connecting line Cln connects the gate electrode of the driving transistor Td in a respective pixel driving circuit with the second electrode of the first reset transistor Tr1 and the light shield in the respective pixel driving circuit together. Referring to FIG. 4A, in some embodiments, the node connecting line Cln is connected to the second electrode Dr1 of the first reset transistor Tr1 through a first via v1, to the light shield LS through a second via v2, and to the gate electrode of the driving transistor Td through a third via v3. Optionally, the first node connecting line Cln1 corresponds to the node N1 depicted in FIG. 2A.

[0094] In one example, the first via v1 extends through the passivation layer PVX and the second gate insulating layer GI2; the second via v2 extends through the passivation layer PVX, the second gate insulating layer GI2, the first gate insulating layer GI1, and the insulating layer IN; and the third via v3 extends through the passivation layer PVX.

[0095] The data signal connecting pad DCP connects a respective data line of the plurality of data lines DL to a first electrode of the data write transistor Tw.

[0096] The relay electrode RE connects an anode connecting pad with the second capacitor electrode Ce2 and/or the second electrode Dd of the driving transistor Td in a respective pixel driving circuit. The anode connecting pad is connected to an anode of a respective light emitting element. Referring to FIG. 4B, in some embodiments, the relay electrode RE is connected to the second capacitor electrode Ce2 through a fourth via v4, to the second electrode Dd of the driving transistor Td through a fifth via v5. The anode connecting pad ACP is connected to the relay electrode RE through a sixth via v6. Optionally, the relay electrode RE corresponds to the node N2 depicted in FIG. 2A.

[0097] In one example, the fourth via v4 extends through the passivation layer PVX, the second gate insulating layer GI2, and the first gate insulating layer GI1; the fifth via v5 extends through the passivation layer PVX and the second gate insulating layer GI2; and the sixth via v6 extends through the first planarization layer PLN1.

[0098] In some embodiments, a respective first voltage supply line of the plurality of first voltage supply lines Vdd1 is connected to first electrodes of multiple light emitting control transistors, e.g., multiple light emitting control transistors in a same row.

[0099] In some embodiments, the plurality of second voltage supply lines Vss1 are electrically connected to a cathode of a plurality of light emitting elements.

[0100] In some embodiments, a respective first reset signal line of the plurality of first reset signal lines Vint1 is connected to first electrodes of multiple first reset transistors, e.g., multiple first reset transistors in a same row.

[0101] In some embodiments, a respective second reset signal line of the plurality of second reset signal lines Vint2 is connected to first electrodes of multiple second reset transistors, e.g., multiple second reset transistors in a same row.

[0102] In some embodiments, a respective gate line of the plurality of gate lines GL includes a third gate electrode portion Gw-3 of the gate electrode of the data write transistor Tw. Optionally, an orthographic projection of the third gate electrode portion Gw-3 of the gate electrode of the data write transistor Tw on a base substrate at least partially overlaps with an orthographic projection of the second gate electrode portion Gw-2 of the gate electrode of the data write transistor Tw on the base substrate; and at least partially overlaps with an orthographic projection of the first gate electrode portion Gw-1 of the gate electrode of the data write transistor Tw on the base substrate. Optionally, the orthographic projection of the second gate electrode portion Gw-2 of the gate electrode of the data write transistor Tw on the base substrate at least partially overlaps with the orthographic projection of the first gate electrode portion Gw-1 of the gate electrode of the data write transistor Tw on the base substrate.

[0103] In some embodiments, a respective second reset control signal line of the plurality of second reset control signal lines rst2 includes a third gate electrode portion Gr2-3 of the gate electrode of the second reset transistor Tr2. Optionally, an orthographic projection of the third gate electrode portion Gr2-3 of the gate electrode of the second reset transistor Tr2 on a base substrate at least partially overlaps with an orthographic projection of the second gate electrode portion Gr2-2 of the gate electrode of the second reset transistor Tr2 on the base substrate; and at least partially overlaps with an orthographic projection of the first gate electrode portion Gr2-1 of the gate electrode of the second reset transistor Tr2 on the base substrate. Optionally, the orthographic projection of the second gate electrode portion Gr2-2 of the gate electrode of the second reset transistor Tr2 on the base substrate at least partially overlaps with the orthographic projection of the first gate electrode portion Gr2-1 of the gate electrode of the second reset transistor Tr2 on the base substrate.

[0104] Vias extending through the first planarization layer PLN1 are depicted in FIG. 3J.

[0105] Referring to FIG. 2A, FIG. 3A, and FIG. 3K, the second signal line layer in some embodiments includes a plurality of third voltage supply lines Vdd2, a plurality of fourth voltage supply lines Vss2, a plurality of data line DL, a plurality of third reset signal lines Vint3, a plurality of fourth reset signal lines Vint4, and an anode connecting pad ACP. A

respective data line of the plurality of data lines DL is electrically connected to a first electrode of the data write transistor Tw through a data signal connecting pad. The anode connecting pad ACP is connected to the second capacitor electrode and/or the second electrode of the driving transistor in a respective pixel driving circuit through the relay electrode, and is connected to an anode of a respective light emitting element.

[0106] Various appropriate conductive materials and various appropriate fabricating methods may be used to make the second signal line layer. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the second signal line layer include, but are not limited to, titanium, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. In some embodiments, the second signal line layer includes a plurality of sub-layers stacked together. In one example, the second signal line layer includes a stacked titanium/aluminum/titanium multi-layer structure. In another example, the second signal line layer includes a stacked molybdenum/aluminum/molybdenum multi-layer structure. Optionally, the plurality of third voltage supply lines Vdd2, the plurality of fourth voltage supply lines Vss2, the plurality of data line DL, the plurality of third reset signal lines Vint3, the plurality of fourth reset signal lines Vint4, and the anode connecting pad ACP are in a same layer.

[0107] In some embodiments, the plurality of third voltage supply lines Vdd2 are configured to provide a first reference voltage signal (e.g., a high reference voltage signal); and the plurality of fourth voltage supply lines Vss2 are configured to provide a second reference voltage signal (e.g., a low reference voltage signal). Optionally, the first reference voltage signal is a constant voltage signal, the second reference voltage signal is a constant voltage signal, the first reference voltage signal has a voltage level higher than a voltage level of the second reference voltage signal.

[0108] Referring to FIG. 3I and FIG. 3K, in some embodiments, the plurality of third voltage supply lines Vdd2 in the second signal line layer are connected to a plurality of first voltage supply lines Vdd1 in the first signal line layer. A respective first voltage supply line of the plurality of first voltage supply lines Vdd1 is connected to first electrodes of multiple light emitting control transistors, e.g., multiple light emitting control transistors in a same row. Optionally, the plurality of third voltage supply lines Vdd2 extend along a direction substantially parallel to a second direction DR2; and the plurality of first voltage supply lines Vdd1 extend along a direction substantially parallel to the first direction DR1.

[0109] In some embodiments, the plurality of fourth voltage supply lines Vss2 in the second signal line layer are connected to a plurality of second voltage supply lines Vss1 in the first

signal line layer. Optionally, the plurality of fourth voltage supply lines Vss2 extend along a direction substantially parallel to a second direction DR2; and the plurality of second voltage supply lines Vss1 extend along a direction substantially parallel to the first direction DR1.

[0110] In some embodiments, the plurality of third reset signal lines Vint3 in the second signal line layer are connected to a plurality first reset signal lines Vint1 in the first signal line layer. Optionally, a respective first reset signal line of the plurality of first reset signal lines Vint1 is connected to first electrodes of multiple first reset transistors, e.g., multiple first reset transistors in a same row. Optionally, the plurality of third reset signal lines Vint3 extend along a direction substantially parallel to a second direction DR2; and the plurality first reset signal lines Vint1 extend along a direction substantially parallel to the first direction DR1.

[0111] In some embodiments, the plurality of fourth reset signal lines Vint4 in the second signal line layer are connected to a plurality second reset signal lines Vint2 in the first signal line layer. Optionally, a respective second reset signal line of the plurality of second reset signal lines Vint2 is connected to first electrodes of multiple second reset transistors, e.g., multiple second reset transistors in a same row. Optionally, the plurality of fourth reset signal lines Vint4 extend along a direction substantially parallel to a second direction DR2; and the plurality second reset signal lines Vint2 extend along a direction substantially parallel to the first direction DR1.

[0112] In some embodiments, the first column of pixel driving circuits, the second column of pixel driving circuits, and the third column of pixel driving circuits are three adjacent columns of pixel driving circuits. Optionally, the first column of pixel driving circuits, the second column of pixel driving circuits, and the third column of pixel driving circuits are sequentially arranged along the first direction DR1.

[0113] In some embodiments, a respective data line of the plurality of data lines DL in the second signal line layer is connected to a data signal connecting pad DCP in the first signal line layer, and the data signal connecting pad DCP is connected to a first electrode of the data write transistor Tw. Optionally, the plurality of data lines DL extend along a direction substantially parallel to a second direction DR2.

[0114] Vias extending through the second planarization layer PLN2 are depicted in FIG. 3L. An anode of a light emitting element is connected to an anode connecting pad in the second signal line layer through a via extending through the second planarization layer PLN2.

[0115] FIG. 5 is a diagram illustrating the structure of a first voltage supply network in a portion of an array substrate in some embodiments according to the present disclosure. Referring to FIG. 5, the first voltage supply network in some embodiments includes a plurality of first voltage supply lines Vdd1 and a plurality of third voltage supply lines Vdd2 interconnected to each other. Optionally, the plurality of first voltage supply lines Vdd1 extend

along a direction substantially parallel to a first direction DR1. Optionally, the plurality of third voltage supply lines Vdd2 extend along a direction substantially parallel to a second direction DR2. Optionally, a respective first voltage supply line of the plurality of first voltage supply lines Vdd1 is connected to one or more third voltage supply lines of the plurality of third voltage supply lines Vdd2. Optionally, a respective third voltage supply line of the plurality of third voltage supply lines Vdd2 is connected to one or more first voltage supply lines of the plurality of first voltage supply lines Vdd1.

[0116] In one example, the plurality of first voltage supply lines Vdd1 are in the first signal line layer. Optionally, the plurality of third voltage supply lines Vdd2 are in the second signal line layer.

[0117] FIG. 6 is a diagram illustrating the structure of a second voltage supply network in a portion of an array substrate in some embodiments according to the present disclosure. Referring to FIG. 6, the second voltage supply network in some embodiments includes a plurality of second voltage supply lines Vss1 and a plurality of fourth voltage supply lines Vss2 interconnected to each other. Optionally, the plurality of second voltage supply lines Vss1 extend along a direction substantially parallel to a first direction DR1. Optionally, the plurality of fourth voltage supply lines Vss2 extend along a direction substantially parallel to a second direction DR2. Optionally, a respective second voltage supply line of the plurality of second voltage supply lines Vss1 is connected to one or more fourth voltage supply lines of the plurality of fourth voltage supply lines Vss2. Optionally, a respective fourth voltage supply line of the plurality of fourth voltage supply lines Vss2 is connected to one or more second voltage supply lines of the plurality of second voltage supply lines Vss1.

[0118] In one example, the plurality of second voltage supply lines Vss1 are in the first signal line layer. Optionally, the plurality of fourth voltage supply lines Vss2 are in the second signal line layer.

[0119] FIG. 7 is a diagram illustrating the structure of a first reset signal network in a portion of an array substrate in some embodiments according to the present disclosure. Referring to FIG. 7, the first reset signal network in some embodiments includes a plurality of first reset signal lines Vint1 and a plurality of third reset signal lines Vint3 interconnected to each other. Optionally, the plurality of first reset signal lines Vint1 extend along a direction substantially parallel to a first direction DR1. Optionally, the plurality of third reset signal lines Vint3 extend along a direction substantially parallel to a second direction DR2. Optionally, a respective first reset signal line of the plurality of first reset signal lines Vint1 is connected to one or more third reset signal lines of the plurality of third reset signal lines Vint3. Optionally, a respective third reset signal line of the plurality of third reset signal lines Vint3 is connected to one or more first reset signal lines of the plurality of first reset signal lines Vint1.

[0120] In one example, the plurality of first reset signal lines Vint1 are in the first signal line layer. Optionally, the plurality of third reset signal lines Vint3 are in the second signal line layer.

[0121] FIG. 8 is a diagram illustrating the structure of a second reset signal network in a portion of an array substrate in some embodiments according to the present disclosure. Referring to FIG. 8, the second reset signal network in some embodiments includes a plurality of second reset signal lines Vint2 and a plurality of fourth reset signal lines Vint4 interconnected to each other. Optionally, the plurality of second reset signal lines Vint2 extend along a direction substantially parallel to a first direction DR1. Optionally, the plurality of fourth reset signal lines Vint4 extend along a direction substantially parallel to a second direction DR2. Optionally, a respective second reset signal line of the plurality of second reset signal lines Vint2 is connected to one or more fourth reset signal lines of the plurality of fourth reset signal lines Vint4. Optionally, a respective fourth reset signal line of the plurality of fourth reset signal lines Vint4 is connected to one or more second reset signal lines of the plurality of second reset signal lines Vint2.

[0122] In one example, the plurality of second reset signal lines Vint2 are in the first signal line layer. Optionally, the plurality of fourth reset signal lines Vint4 are in the second signal line layer.

[0123] Referring to FIG. 3A to FIG. 3L, in some embodiments, the pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column C(3k-2), a $(3k-1)$ -th column C(3k-1), and a $(3k)$ -th column C(3k) of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$.

[0124] As used herein, the terms “ $(3k-2)$ -th column”, “ $(3k-1)$ -th column”, and “ $(3k)$ -th column” are used in the context of the K columns. The array substrate may or may not include additional column(s) before the first column of the K columns and/or additional columns after the last column of the K columns. In the context of the array substrate, the term “ $(3k-1)$ -th column” does not necessarily denote an odd-numbered column, and the term “ $(3k-2)$ -th column” or “ $(3k)$ -th column” does not necessarily denote an even-numbered column. In one example, the $(3k-2)$ -th column is an even-numbered column in the context of the K columns, but may be an odd-numbered column in the context of the array substrate. In another example, the $(3k-2)$ -th column is an even-numbered column in the context of the K columns, and also an even-numbered column in the context of the array substrate. In one example, the $(3k-1)$ -th column is an odd-numbered column in the context of the K columns, but may be an even-numbered column in the context of the array substrate. In another example, the $(3k-1)$ -th column is an odd-numbered column in the context of the K columns, and also an odd-numbered column in the context of the array substrate. In one example, the $(3k)$ -th column is an even-numbered column in the context of the K columns, but may be an odd-numbered column in the context of

the array substrate. In another example, the (3k)-th column is an even-numbered column in the context of the K columns, and also an even-numbered column in the context of the array substrate.

[0125] In some embodiments, the (3k-2)-th column C(3k-2) includes a (3k-2)-th pixel driving circuit, the (3k-1)-th column C(3k-1) includes a (3k-1)-th pixel driving circuit, and the (3k)-th column C(3k) includes a (3k)-th pixel driving circuit. The (3k-2)-th pixel driving circuit, the (3k-1)-th pixel driving circuit, and the (3k)-th pixel driving circuit are in a same row.

[0126] In some embodiments, the (3k-2)-th column C(3k-2) includes a fourth voltage supply line of the plurality of fourth voltage supply lines Vss2; the (3k-1)-th column C(3k-1) includes a fourth reset signal line of the plurality of fourth reset signal lines Vint4; and the (3k)-th column C(3k) includes a third reset signal line of the plurality of third reset signal lines Vint3.

[0127] Optionally, the plurality of fourth voltage supply lines Vss2 are absent in the (3k-1)-th column C(3k-1) and absent in (3k)-th column C(3k).

[0128] Optionally, the plurality of fourth reset signal lines Vint4 are absent in the (3k-2)-th column C(3k-2) and absent in (3k)-th column C(3k).

[0129] Optionally, the plurality of third reset signal lines Vint3 are absent in the (3k-2)-th column C(3k-2) and absent in (3k-1)-th column C(3k-1).

[0130] In some embodiments, the (3k-2)-th column C(3k-2) of pixel driving circuits are configured to drive light emission of a (3k-2)-th column C(3k-2) of subpixels of a first color, the (3k)-th column C(3k) of pixel driving circuits are configured to drive light emission of a (3k)-th column C(3k) of subpixels of a second color, and the (3k-1)-th column C(3k-1) of pixel driving circuits are configured to drive light emission of a (3k-1)-th column C(3k-1) of subpixels of a third color. Optionally, the first color, the second color, and the third color are three different colors selected from a red color, a green color, and a blue color.

[0131] FIG. 9 is a diagram illustrating the structure of a semiconductor material layer and a second signal line layer in the portion of the array substrate depicted in FIG. 3A. In some embodiments, referring to FIG. 3A to FIG. 3K, and FIG. 9, an orthographic projection of a respective third voltage supply line of a plurality of third voltage supply lines Vdd2 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTe of the light emitting control transistor Te in the respective pixel driving circuit on the base substrate, substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTr2 of the second reset transistor Tr2 on the base substrate, and at least partially overlaps with an orthographic projection of an active layer ACTd of the driving transistor Td on the base substrate. The inventors of the

present disclosure discover that, by having this structure, the active layer ACTe of the light emitting control transistor Te, the active layer ACTr2 of the second reset transistor Tr2, and the active layer ACTd of the driving transistor Td can be protected from irradiation and stabilized.

[0132] In some embodiments, the orthographic projection of a respective third voltage supply line of a plurality of third voltage supply lines Vdd2 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTe, a first electrode Se, and a second electrode De of the light emitting control transistor Te in the respective pixel driving circuit on the base substrate; substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTr2, a first electrode Sr2, and a second electrode Dr2 of the second reset transistor Tr2 on the base substrate; substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of a first electrode Sd and a second electrode Dd of the driving transistor Td on the base substrate; and at least partially overlaps with an orthographic projection of an active layer ACTd of the driving transistor Td on the base substrate.

[0133] In some embodiments, the active layer ACTd, the first electrode Sd, and the second electrode Dd of the driving transistor Td; the active layer ACTe, the first electrode Se, and the second electrode De of the light emitting control transistor Te; and the active layer ACTr2, the first electrode Sr2, and the second electrode Dr2 of the second reset transistor Tr2 are parts of a first unitary structure. Optionally, the first unitary structure extends along a direction substantially parallel to an extension direction of the respective third voltage supply line of a plurality of third voltage supply lines Vdd2.

[0134] In some embodiments, in a first column of pixel driving circuits, an orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines Vss2 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTr1 of the first reset transistor Tr1 in a first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTw of the data write transistor Tw in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate. The inventors of the present disclosure discover that, by having this structure, the active layer ACTr1 of the first reset

transistor Tr1 and the active layer ACTw of the data write transistor Tw can be protected from irradiation and stabilized.

[0135] In some embodiments, in the first column of pixel driving circuits, the orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines Vss2 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTr1, a first electrode Sr1, and a second electrode Dr1 of the first reset transistor Tr1 in a first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTw and a second electrode Dw of the data write transistor Tw in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate.

[0136] In some embodiments, in the first column of pixel driving circuits, the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw and the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1 of the first reset transistor Tr1 are parts of a second unitary structure in the first column of pixel driving circuits. Optionally, the second unitary structure in the first column of pixel driving circuits extends along a direction substantially parallel to an extension direction of the respective fourth voltage supply line of the plurality of fourth voltage supply lines Vss2.

[0137] In some embodiments, in a second column of pixel driving circuits, an orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines Vint4 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTr1 of the first reset transistor Tr1 in a second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTw of the data write transistor Tw in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate. The inventors of the present disclosure discover that, by having this structure, the active layer ACTr1 of the first reset transistor Tr1 and the active layer ACTw of the data write transistor Tw can be protected from irradiation and stabilized.

[0138] In some embodiments, in the second column of pixel driving circuits, the orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines Vint4 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an

orthographic projection of a combination of an active layer ACTr1, a first electrode Sr1, and a second electrode Dr1 of the first reset transistor Tr1 in a second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate; and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTw and a second electrode Dw of the data write transistor Tw in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate.

[0139] In some embodiments, in the second column of pixel driving circuits, the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw and the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1 of the first reset transistor Tr1 are parts of a second unitary structure in the second column of pixel driving circuits. Optionally, the second unitary structure in the second column of pixel driving circuits extends along a direction substantially parallel to an extension direction of the respective fourth reset signal line of the plurality of fourth reset signal lines Vint4.

[0140] In some embodiments, in a third column of pixel driving circuits, an orthographic projection of a respective third reset signal line of the plurality of third reset signal lines Vint3 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTr1 of the first reset transistor Tr1 in a third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTw of the data write transistor Tw in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate. The inventors of the present disclosure discover that, by having this structure, the active layer ACTr1 of the first reset transistor Tr1 and the active layer ACTw of the data write transistor Tw can be protected from irradiation and stabilized.

[0141] In some embodiments, in the third column of pixel driving circuits, the orthographic projection of a respective third reset signal line of the plurality of third reset signal lines Vint3 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTr1, a first electrode Sr1, and a second electrode Dr1 of the first reset transistor Tr1 in a third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate; and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer

ACTw and a second electrode Dw of the data write transistor Tw in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate.

[0142] In some embodiments, in the third column of pixel driving circuits, the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw and the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1 of the first reset transistor Tr1 are parts of a second unitary structure in the third column of pixel driving circuits. Optionally, the second unitary structure in the third column of pixel driving circuits extends along a direction substantially parallel to an extension direction of the respective third reset signal line of the plurality of third reset signal lines Vint3.

[0143] In some embodiments, in the (3k-2)-th column C(3k-2) of pixel driving circuits, an orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines Vss2 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTr1 of the first reset transistor Tr1 in a first respective pixel driving circuit in the (3k-2)-th column C(3k-2) of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTw of the data write transistor Tw in the first respective pixel driving circuit in the (3k-2)-th column C(3k-2) of pixel driving circuits on the base substrate. The inventors of the present disclosure discover that, by having this structure, the active layer ACTr1 of the first reset transistor Tr1 and the active layer ACTw of the data write transistor Tw can be protected from irradiation and stabilized.

[0144] In some embodiments, in the (3k-2)-th column C(3k-2) of pixel driving circuits, the orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines Vss2 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTr1, a first electrode Sr1, and a second electrode Dr1 of the first reset transistor Tr1 in a first respective pixel driving circuit in the (3k-2)-th column C(3k-2) of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTw and a second electrode Dw of the data write transistor Tw in the first respective pixel driving circuit in the (3k-2)-th column C(3k-2) of pixel driving circuits on the base substrate.

[0145] In some embodiments, in the (3k-2)-th column C(3k-2) of pixel driving circuits, the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw and the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1

of the first reset transistor Tr1 are parts of a second unitary structure in the (3k-2)-th column C(3k-2) of pixel driving circuits. Optionally, the second unitary structure in the (3k-2)-th column C(3k-2) of pixel driving circuits extends along a direction substantially parallel to an extension direction of the respective fourth voltage supply line of the plurality of fourth voltage supply lines Vss2.

[0146] In some embodiments, in the (3k-1)-th column C(3k-1) of pixel driving circuits, an orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines Vint4 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTr1 of the first reset transistor Tr1 in a second respective pixel driving circuit in the (3k-1)-th column C(3k-1) of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTw of the data write transistor Tw in the second respective pixel driving circuit in the (3k-1)-th column C(3k-1) of pixel driving circuits on the base substrate. The inventors of the present disclosure discover that, by having this structure, the active layer ACTr1 of the first reset transistor Tr1 and the active layer ACTw of the data write transistor Tw can be protected from irradiation and stabilized.

[0147] In some embodiments, in the (3k-1)-th column C(3k-1) of pixel driving circuits, the orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines Vint4 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTr1, a first electrode Sr1, and a second electrode Dr1 of the first reset transistor Tr1 in a second respective pixel driving circuit in the (3k-1)-th column C(3k-1) of pixel driving circuits on the base substrate; and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTw and a second electrode Dw of the data write transistor Tw in the second respective pixel driving circuit in the (3k-1)-th column C(3k-1) of pixel driving circuits on the base substrate.

[0148] In some embodiments, in the (3k-1)-th column C(3k-1) of pixel driving circuits, the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw and the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1 of the first reset transistor Tr1 are parts of a second unitary structure in the (3k-1)-th column C(3k-1) of pixel driving circuits. Optionally, the second unitary structure in the (3k-1)-th column C(3k-1) of pixel driving circuits extends along a direction substantially parallel to an

extension direction of the respective fourth reset signal line of the plurality of fourth reset signal lines Vint4.

[0149] In some embodiments, in the (3k)-th column C(3k) of pixel driving circuits, an orthographic projection of a respective third reset signal line of the plurality of third reset signal lines Vint3 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTr1 of the first reset transistor Tr1 in a third respective pixel driving circuit in the (3k)-th column C(3k) of pixel driving circuits on the base substrate, and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of an active layer ACTw of the data write transistor Tw in the third respective pixel driving circuit in the (3k)-th column C(3k) of pixel driving circuits on the base substrate. The inventors of the present disclosure discover that, by having this structure, the active layer ACTr1 of the first reset transistor Tr1 and the active layer ACTw of the data write transistor Tw can be protected from irradiation and stabilized.

[0150] In some embodiments, in the (3k)-th column C(3k) of pixel driving circuits, the orthographic projection of a respective third reset signal line of the plurality of third reset signal lines Vint3 on a base substrate substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTr1, a first electrode Sr1, and a second electrode Dr1 of the first reset transistor Tr1 in a third respective pixel driving circuit in the (3k)-th column C(3k) of pixel driving circuits on the base substrate; and substantially covers (e.g., at least 80% covers, at least 85% covers, at least 90% covers, at least 95% covers, at least 99% covers, or completely covers) an orthographic projection of a combination of an active layer ACTw and a second electrode Dw of the data write transistor Tw in the third respective pixel driving circuit in the (3k)-th column C(3k) of pixel driving circuits on the base substrate.

[0151] In some embodiments, in the (3k)-th column C(3k) of pixel driving circuits, the active layer ACTw, the first electrode Sw, and the second electrode Dw of the data write transistor Tw and the active layer ACTr1, the first electrode Sr1, and the second electrode Dr1 of the first reset transistor Tr1 are parts of a second unitary structure in the (3k)-th column C(3k) of pixel driving circuits. Optionally, the second unitary structure in the (3k)-th column C(3k) of pixel driving circuits extends along a direction substantially parallel to an extension direction of the respective third reset signal line of the plurality of third reset signal lines Vint3.

[0152] In another aspect, the present invention provides a display apparatus, including the array substrate described herein or fabricated by a method described herein, and one or more integrated circuits connected to the array substrate. Examples of appropriate display

apparatuses include, but are not limited to, an electronic paper, a mobile phone, a tablet computer, a television, a monitor, a notebook computer, a digital album, a GPS, etc.

Optionally, the display apparatus is an organic light emitting diode display apparatus.

Optionally, the display apparatus is a micro light emitting diode display apparatus. Optionally, the display apparatus is a mini light emitting diode display apparatus.

[0153] In another aspect, the present disclosure provides a method of fabricating an array substrate. In some embodiments, the method includes forming a plurality of pixel driving circuits. Optionally, forming a respective pixel driving circuit of the plurality of pixel driving circuits includes forming a driving transistor, forming a light shield, and forming a node connecting line. Optionally, an orthographic projection of the light shield on a base substrate substantially covers an orthographic projection of an active layer of the driving transistor on the base substrate. Optionally, the light shield is electrically connected to a gate electrode of the driving transistor through the node connecting line. Optionally, the light shield, the node connecting line, and the gate electrode of the driving transistor are formed in three different layers.

[0154] The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term “the invention”, “the present invention” or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the invention does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is limited only by the spirit and scope of the appended claims. Moreover, these claims may refer to use “first”, “second”, etc. following with noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may not apply to all embodiments of the invention. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended

to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. An array substrate, comprising a plurality of pixel driving circuits;
wherein a respective pixel driving circuit of the plurality of pixel driving circuits comprises a driving transistor, a light shield, and a node connecting line;
wherein an orthographic projection of the light shield on a base substrate substantially covers an orthographic projection of an active layer of the driving transistor on the base substrate;
the light shield is electrically connected to a gate electrode of the driving transistor through the node connecting line;
the light shield, the node connecting line, and the gate electrode of the driving transistor are in three different layers.
2. The array substrate of claim 1, wherein the respective pixel driving circuit further comprises a first reset transistor;
wherein the light shield is electrically connected to a second electrode of the first reset transistor through the node connecting line.
3. The array substrate of claim 1, wherein the respective pixel driving circuit further comprises a storage capacitor;
wherein the orthographic projection of the light shield on the base substrate substantially covers an orthographic projection of a gate electrode of the driving transistor on the base substrate, and substantially covers an orthographic projection of a second capacitor electrode of the storage capacitor on the base substrate.
4. The array substrate of any one of claims 1 to 3, further comprising a plurality of third voltage supply lines;
wherein the respective pixel driving circuit further comprises a light emitting control transistor, and a second reset transistor;
an orthographic projection of a respective third voltage supply line of the plurality of third voltage supply lines on the base substrate substantially covers an orthographic projection of an active layer of the light emitting control transistor in the respective pixel driving circuit on the base substrate, substantially covers an orthographic projection of an active layer of the second reset transistor on the base substrate, and at least partially overlaps with the orthographic projection of the active layer of the driving transistor on the base substrate.
5. The array substrate of claim 4, wherein the orthographic projection of a respective third voltage supply line of the plurality of third voltage supply lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the light emitting control transistor in the respective pixel driving circuit on the base substrate; substantially covers an orthographic projection of a

combination of an active layer, a first electrode, and a second electrode of the second reset transistor on the base substrate; substantially covers an orthographic projection of a combination of a first electrode and a second electrode of the driving transistor on the base substrate; and at least partially overlaps with an orthographic projection of an active layer of the driving transistor on the base substrate.

6. The array substrate of any one of claims 1 to 3, further comprising a plurality of fourth voltage supply lines;

wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor;

in a first column of pixel driving circuits, an orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate.

7. The array substrate of claim 6, wherein, in the first column of pixel driving circuits, the orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the first reset transistor in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of a combination of an active layer and a second electrode of the data write transistor in the first respective pixel driving circuit in the first column of pixel driving circuits on the base substrate.

8. The array substrate of any one of claims 1 to 3, further comprising a plurality of fourth reset signal lines;

wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor;

in a second column of pixel driving circuits, an orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate.

9. The array substrate of claim 8, wherein, in the second column of pixel driving circuits, the orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the first reset transistor in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate; and substantially covers an orthographic projection of a combination of an active layer and a second electrode of the data write transistor in the second respective pixel driving circuit in the second column of pixel driving circuits on the base substrate.

10. The array substrate of any one of claims 1 to 3, further comprising a plurality of third reset signal lines;

wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor;

in a third column of pixel driving circuits, an orthographic projection of a respective third reset signal line of the plurality of third reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate.

11. The array substrate of claim 10, wherein, in the third column of pixel driving circuits, the orthographic projection of a respective third reset signal line of the plurality of third reset signal lines on the base substrate substantially covers an orthographic projection of a combination of an active layer, a first electrode, and a second electrode of the first reset transistor in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate; and substantially covers an orthographic projection of a combination of an active layer and a second electrode of the data write transistor in the third respective pixel driving circuit in the third column of pixel driving circuits on the base substrate.

12. The array substrate of any one of claims 1 to 3, further comprising a plurality of fourth voltage supply lines;

wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor;

pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$;

in the $(3k-2)$ -th column of pixel driving circuits, an orthographic projection of a respective fourth voltage supply line of the plurality of fourth voltage supply lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a first respective pixel driving circuit in the $(3k-2)$ -th column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the first respective pixel driving circuit in the $(3k-2)$ -th column of pixel driving circuits on the base substrate.

13. The array substrate of any one of claims 1 to 3, further comprising a plurality of fourth reset signal lines;

wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor;

pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$;

in the $(3k-1)$ -th column of pixel driving circuits, an orthographic projection of a respective fourth reset signal line of the plurality of fourth reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a second respective pixel driving circuit in the $(3k-1)$ -th column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the second respective pixel driving circuit in the $(3k-1)$ -th column of pixel driving circuits on the base substrate.

14. The array substrate of any one of claims 1 to 3, further comprising a plurality of third reset signal lines;

wherein the respective pixel driving circuit further comprises a data write transistor and a first reset transistor;

pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$;

in the $(3k)$ -th column of pixel driving circuits, an orthographic projection of a respective third reset signal line of the plurality of third reset signal lines on the base substrate substantially covers an orthographic projection of an active layer of the first reset transistor in a third respective pixel driving circuit in the $(3k)$ -th column of pixel driving circuits on the base substrate, and substantially covers an orthographic projection of an active layer of the data write transistor in the third respective pixel driving circuit in the $(3k)$ -th column of pixel driving circuits on the base substrate.

15. The array substrate of claim 1, further comprising a plurality of fourth voltage supply lines, a plurality of fourth reset signal lines, and a plurality of third reset signal lines in a same layer;

wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$;

the $(3k-2)$ -th column comprises a fourth voltage supply line of the plurality of fourth voltage supply lines;

the $(3k-1)$ -th column comprises a fourth reset signal line of the plurality of fourth reset signal lines; and

the $(3k)$ -th column comprises a third reset signal line of the plurality of third reset signal lines.

16. The array substrate of claim 15, wherein the plurality of fourth voltage supply lines are absent in the $(3k-1)$ -th column and absent in the $(3k)$ -th column;

the plurality of fourth reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k)$ -th column; and

the plurality of third reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k-1)$ -th column.

17. The array substrate of claim 1, further comprising a first voltage supply network and a second voltage supply network;

wherein the first voltage supply network comprises a plurality of first voltage supply lines and a plurality of third voltage supply lines interconnected to each other;

the plurality of first voltage supply lines extend along a direction substantially parallel to a first direction;

the plurality of third voltage supply lines extend along a direction substantially parallel to a second direction;

a respective first voltage supply line of the plurality of first voltage supply lines is connected to one or more third voltage supply lines of the plurality of third voltage supply lines;

a respective third voltage supply line of the plurality of third voltage supply lines is connected to one or more first voltage supply lines of the plurality of first voltage supply lines; and

wherein the second voltage supply network comprises a plurality of second voltage supply lines and a plurality of fourth voltage supply lines interconnected to each other;

the plurality of second voltage supply lines extend along a direction substantially parallel to the first direction;

the plurality of fourth voltage supply lines extend along a direction substantially parallel to the second direction;

a respective second voltage supply line of the plurality of second voltage supply lines is connected to one or more fourth voltage supply lines of the plurality of fourth voltage supply lines; and

a respective fourth voltage supply line of the plurality of fourth voltage supply lines is connected to one or more second voltage supply lines of the plurality of second voltage supply lines;

wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$;

the plurality of third voltage supply lines are present in the $(3k-2)$ -th column, present in the $(3k-1)$ -th column, and present in the $(3k)$ -th column;

the plurality of fourth voltage supply lines are absent in the $(3k-1)$ -th column and absent in the $(3k)$ -th column.

18. The array substrate of claim 1, further comprising a first reset signal network;

wherein the first reset signal network comprises a plurality of first reset signal lines and a plurality of third reset signal lines interconnected to each other;

the plurality of first reset signal lines extend along a direction substantially parallel to a first direction;

the plurality of third reset signal lines extend along a direction substantially parallel to a second direction;

a respective first reset signal line of the plurality of first reset signal lines is connected to one or more third reset signal lines of the plurality of third reset signal lines; and

a respective third reset signal line of the plurality of third reset signal lines is connected to one or more first reset signal lines of the plurality of first reset signal lines;

wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; and

the plurality of third reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k-1)$ -th column.

19. The array substrate of claim 1, further comprising a second reset signal network;

wherein the second reset signal network comprises a plurality of second reset signal lines and a plurality of fourth reset signal lines interconnected to each other;

the plurality of second reset signal lines extend along a direction substantially parallel to a first direction;

the plurality of fourth reset signal lines extend along a direction substantially parallel to a second direction;

a respective second reset signal line of the plurality of second reset signal lines is connected to one or more fourth reset signal lines of the plurality of fourth reset signal lines; and

a respective fourth reset signal line of the plurality of fourth reset signal lines is connected to one or more second reset signal lines of the plurality of second reset signal lines;

wherein pixel driving circuits of the array substrate are arranged in columns, including a $(3k-2)$ -th column, a $(3k-1)$ -th column, and a $(3k)$ -th column of K columns, K and k being positive integers, $1 \leq k \leq (K/3)$; and

the plurality of fourth reset signal lines are absent in the $(3k-2)$ -th column and absent in the $(3k)$ -th column.

20. A display apparatus, comprising the array substrate of any one of claims 1 to 19, and one or more integrated circuits connected to the array substrate.

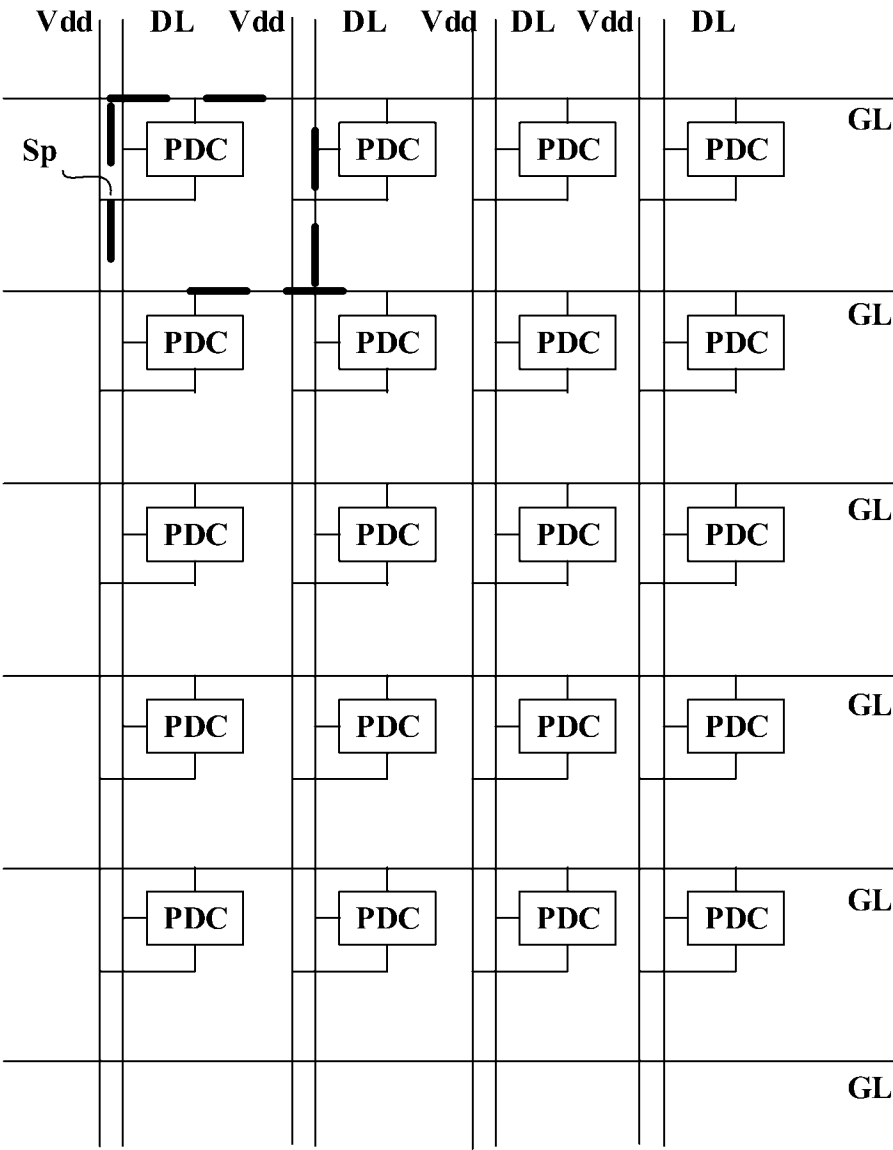


FIG. 1

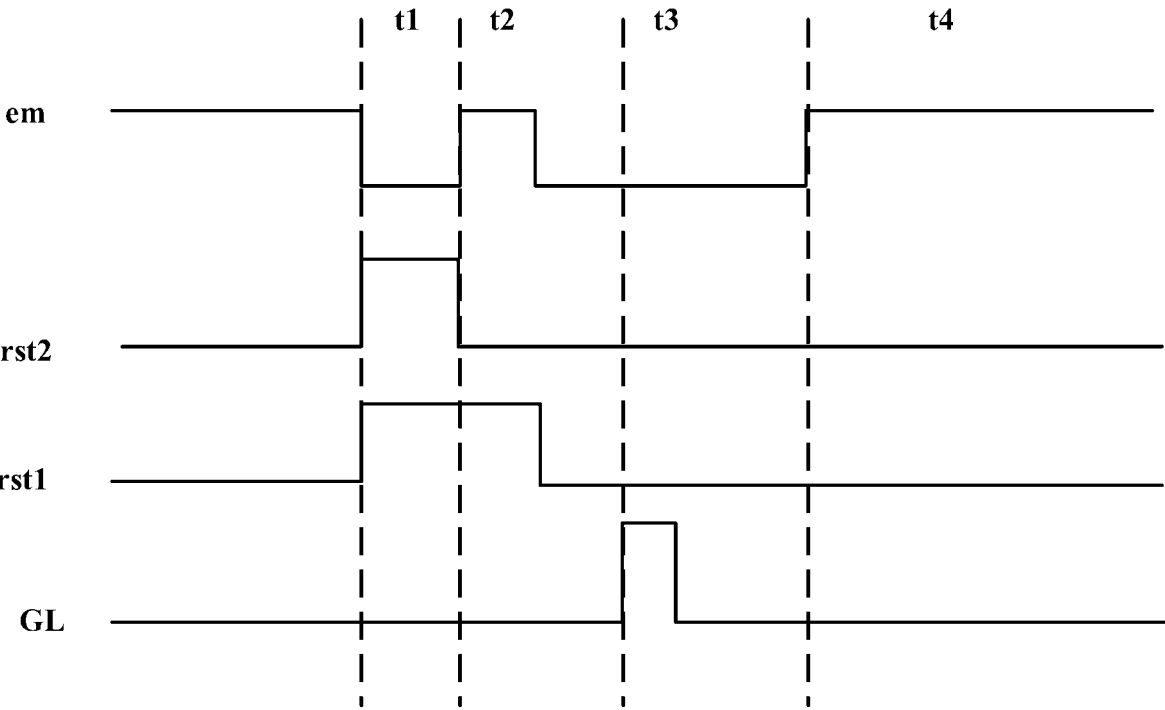


FIG. 2B

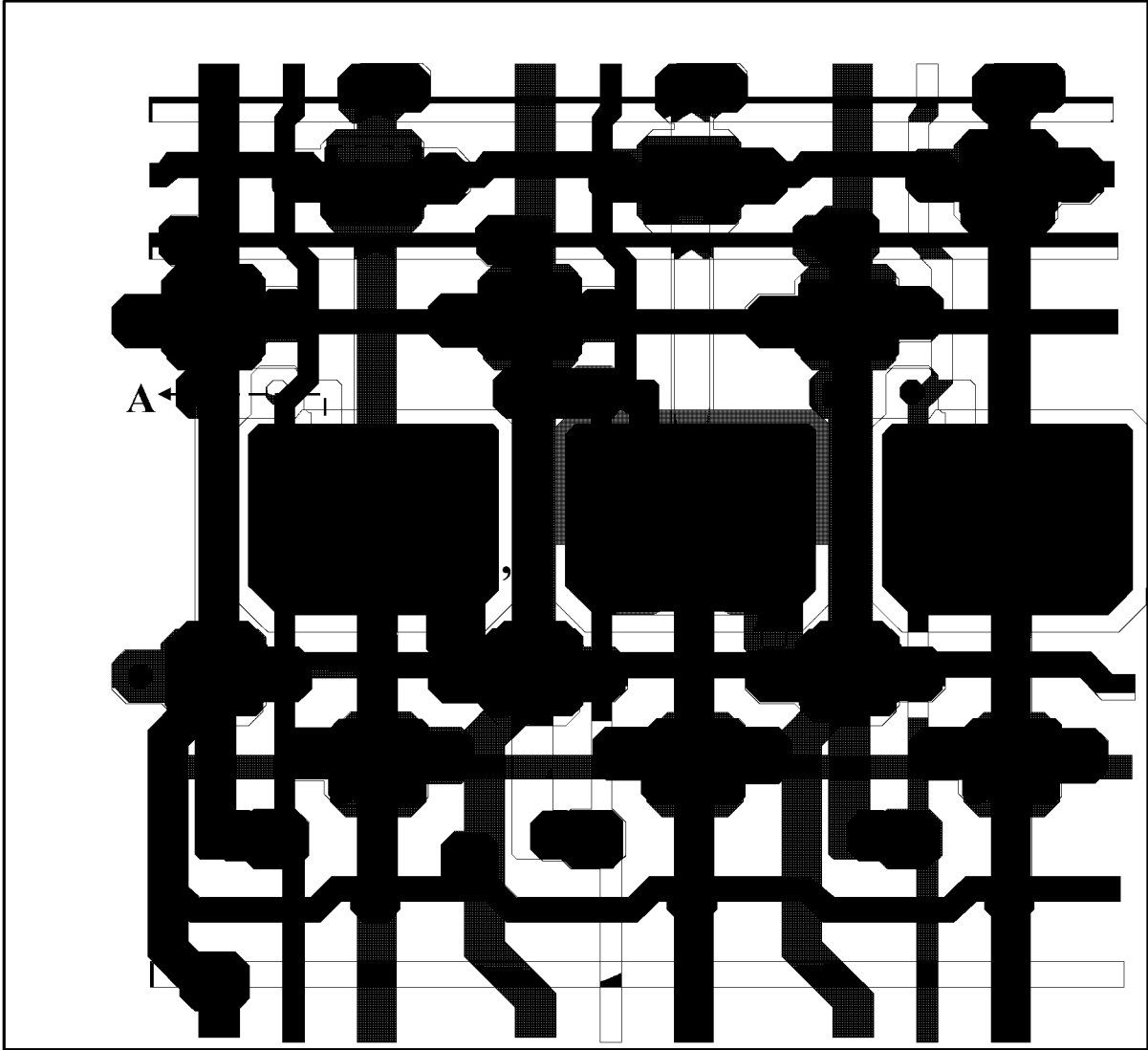


FIG. 3A

5/21

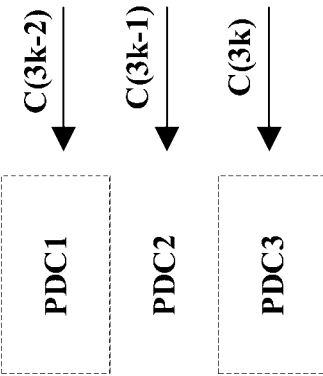


FIG. 3B

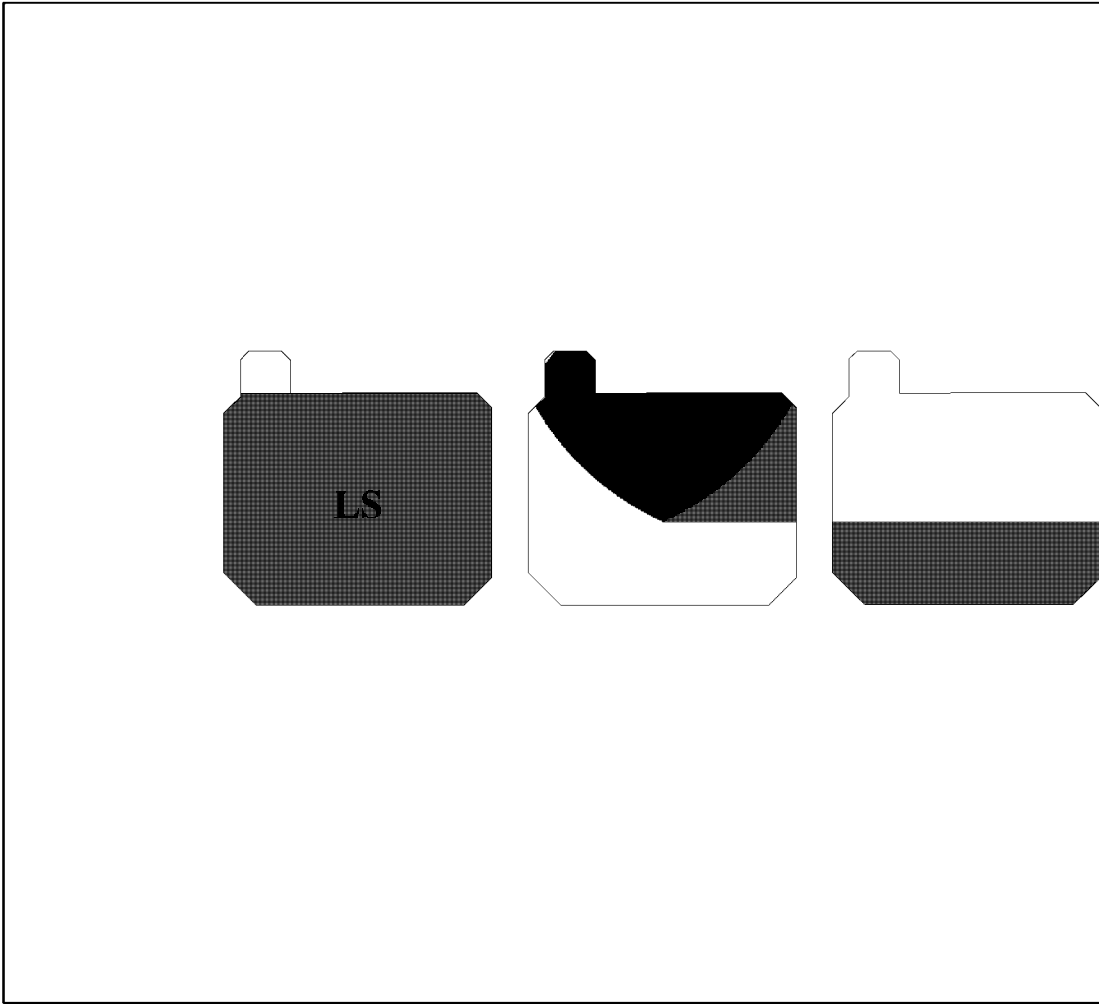


FIG. 3C

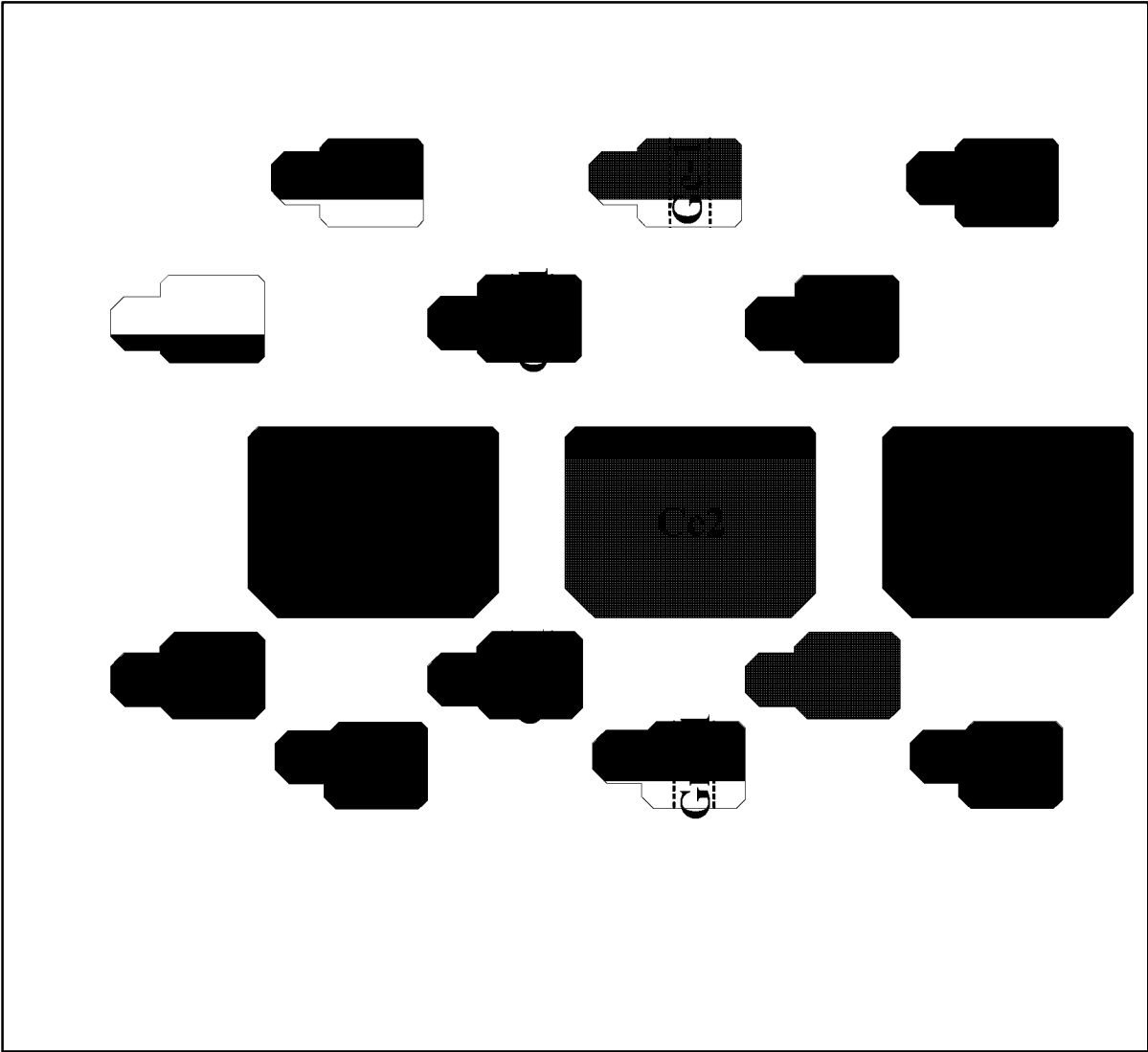


FIG. 3D

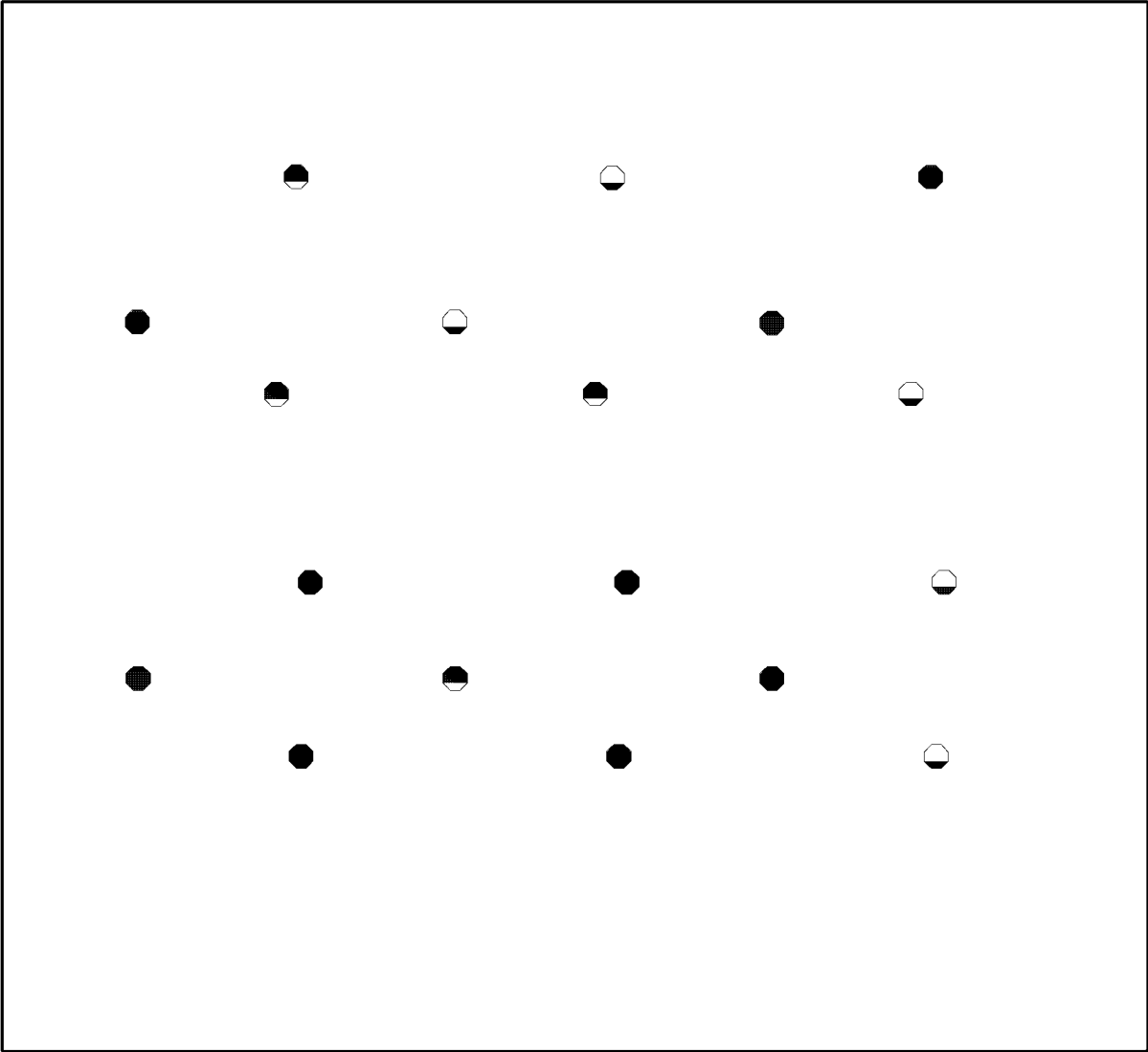


FIG. 3E

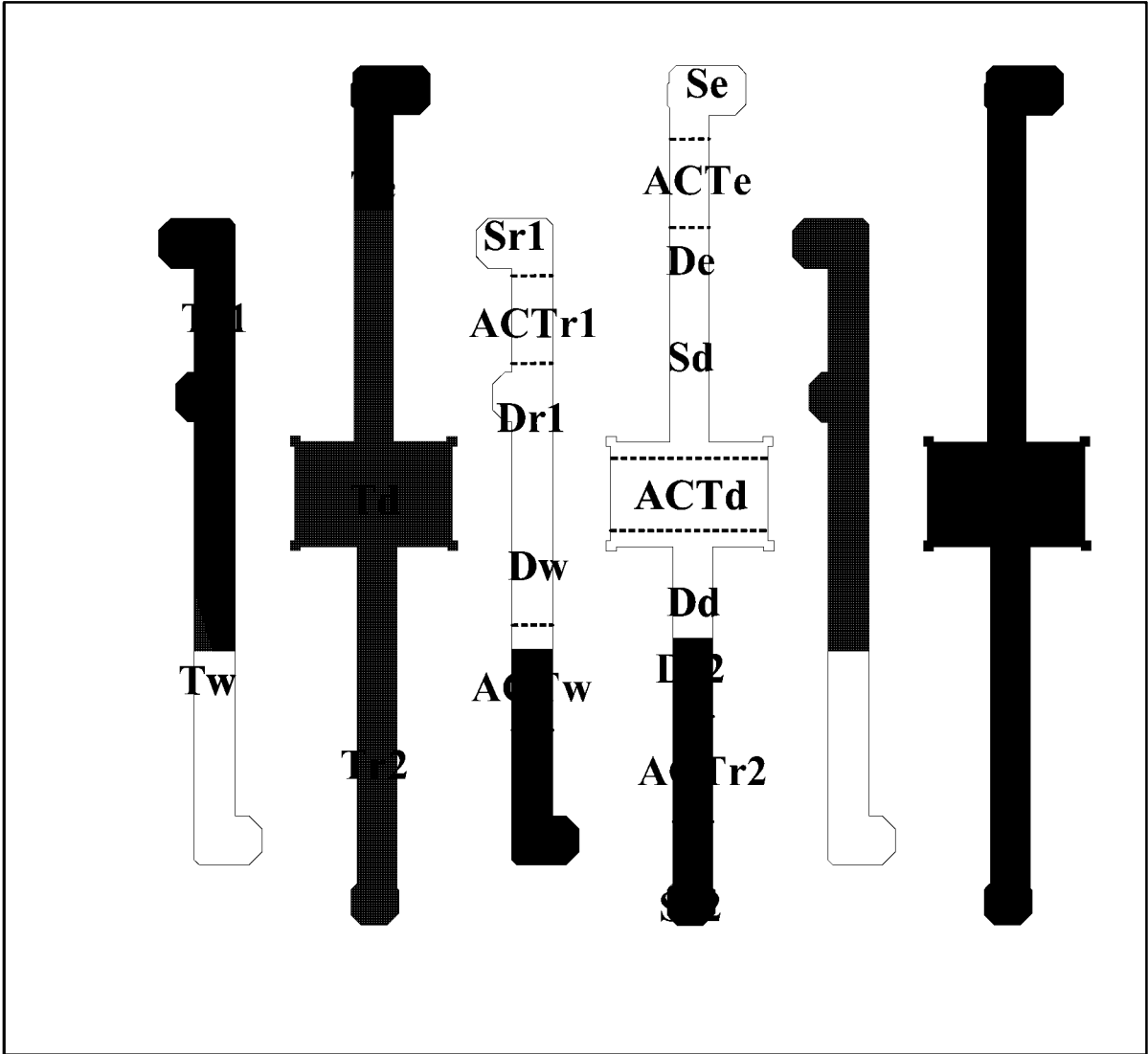


FIG. 3F

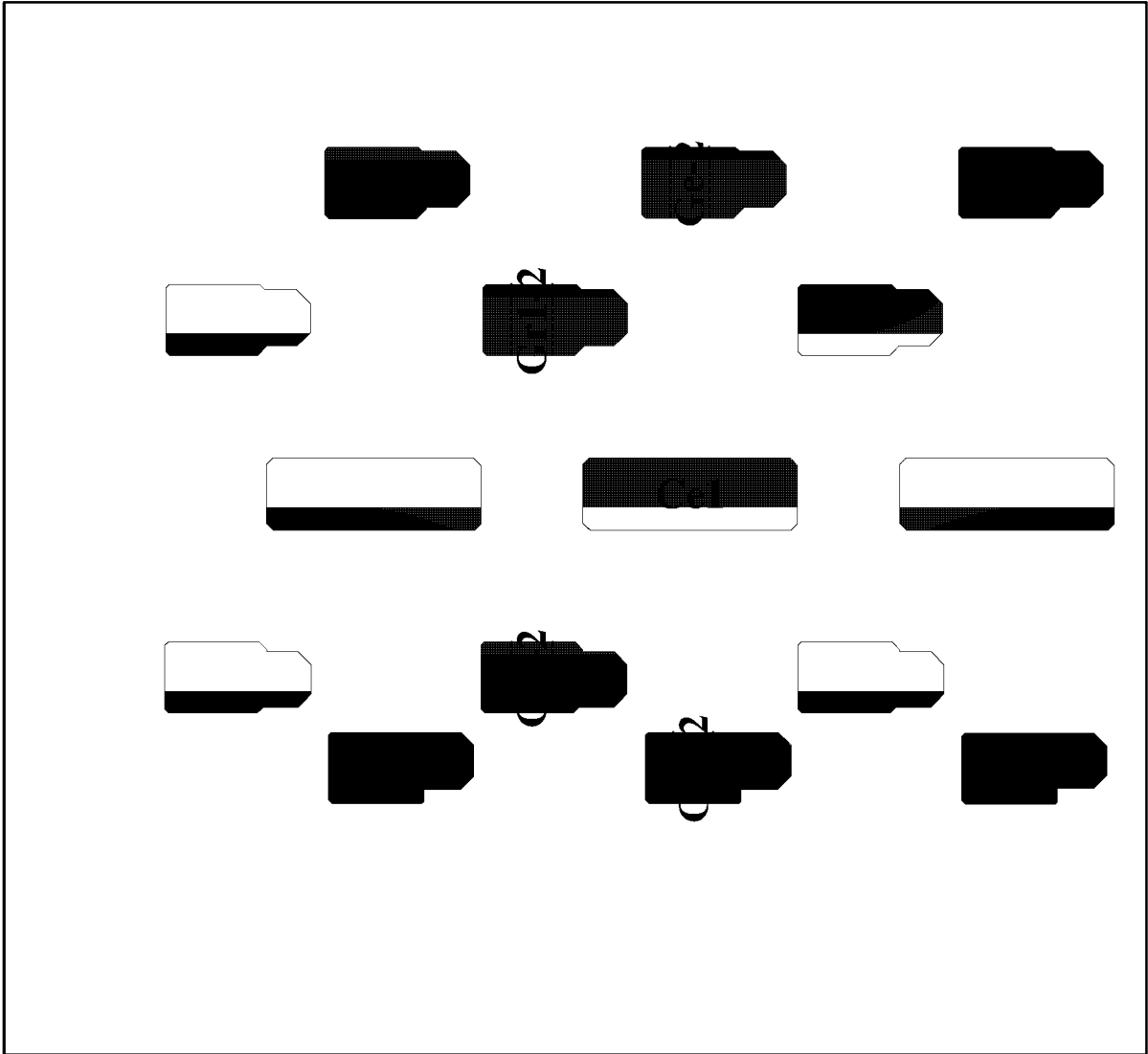


FIG. 3G

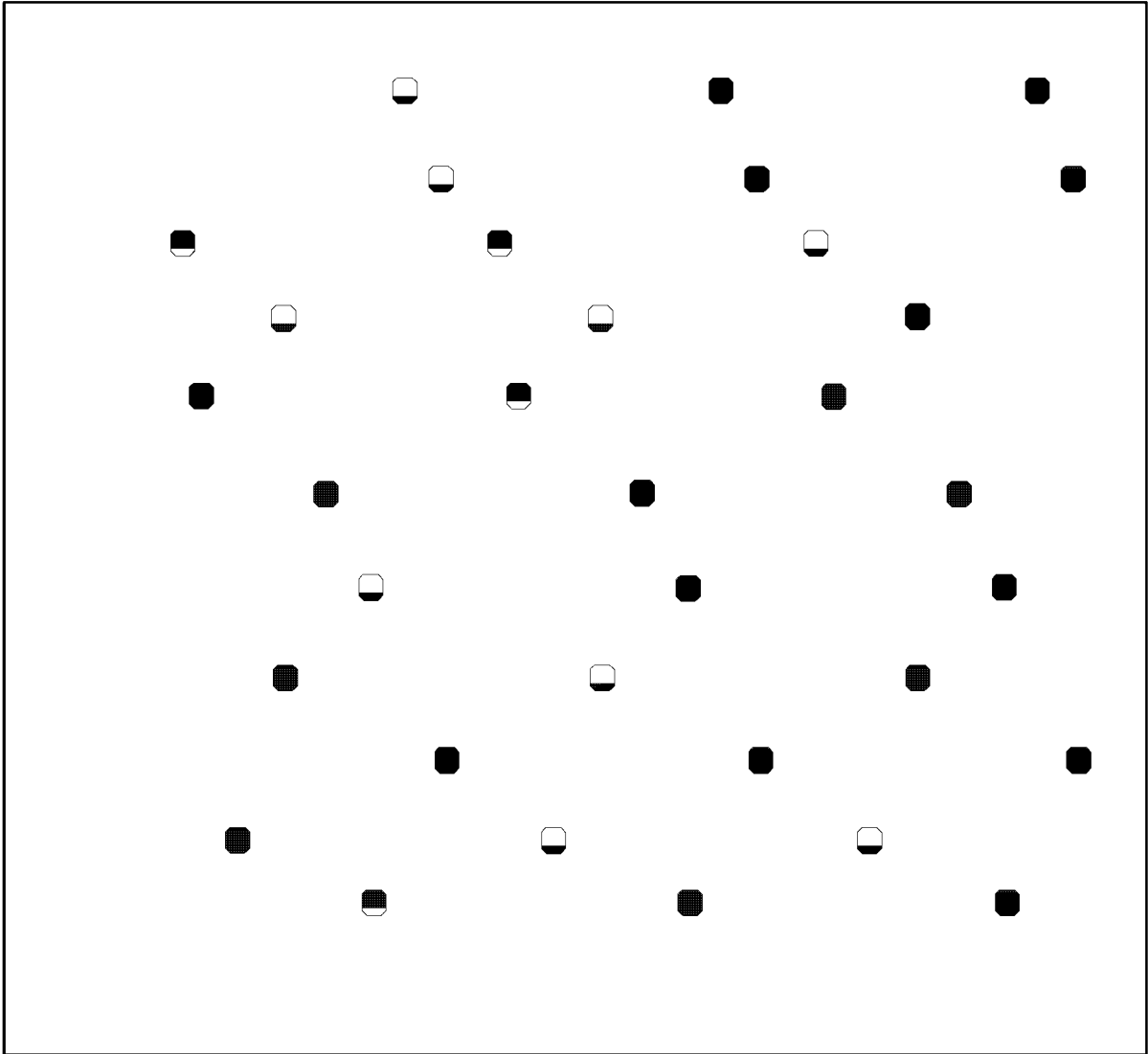


FIG. 3H

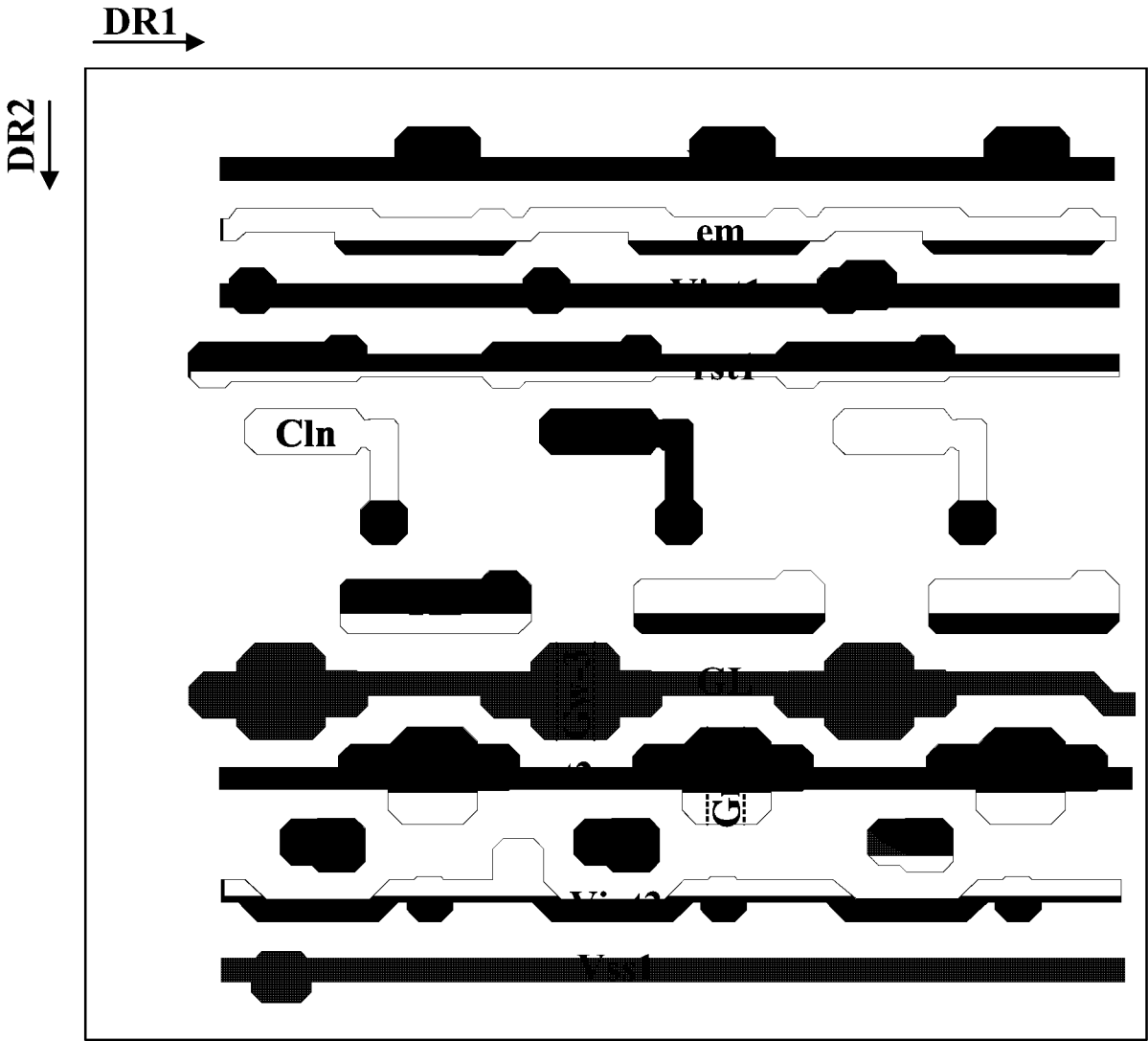


FIG. 3I

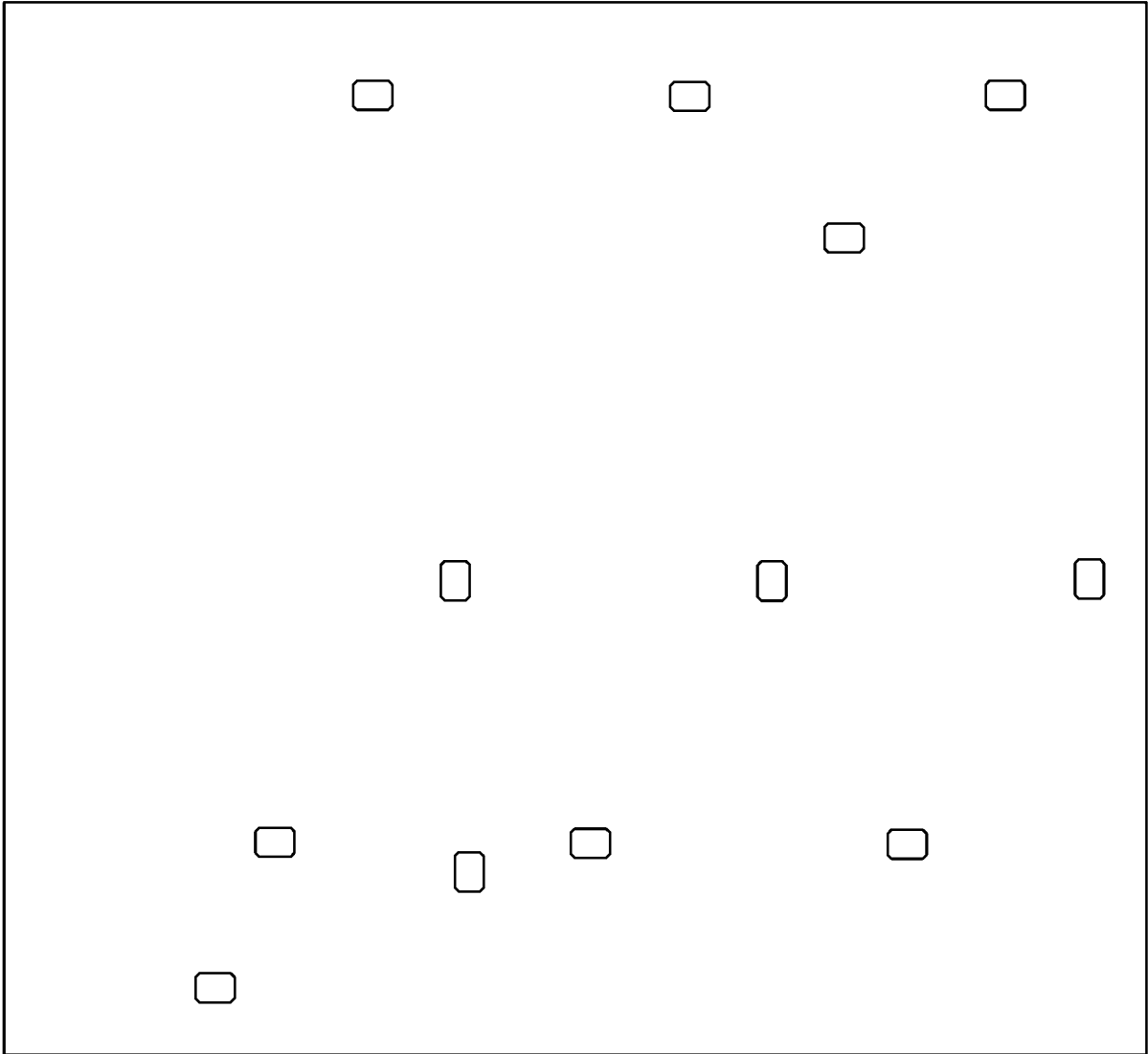


FIG. 3J

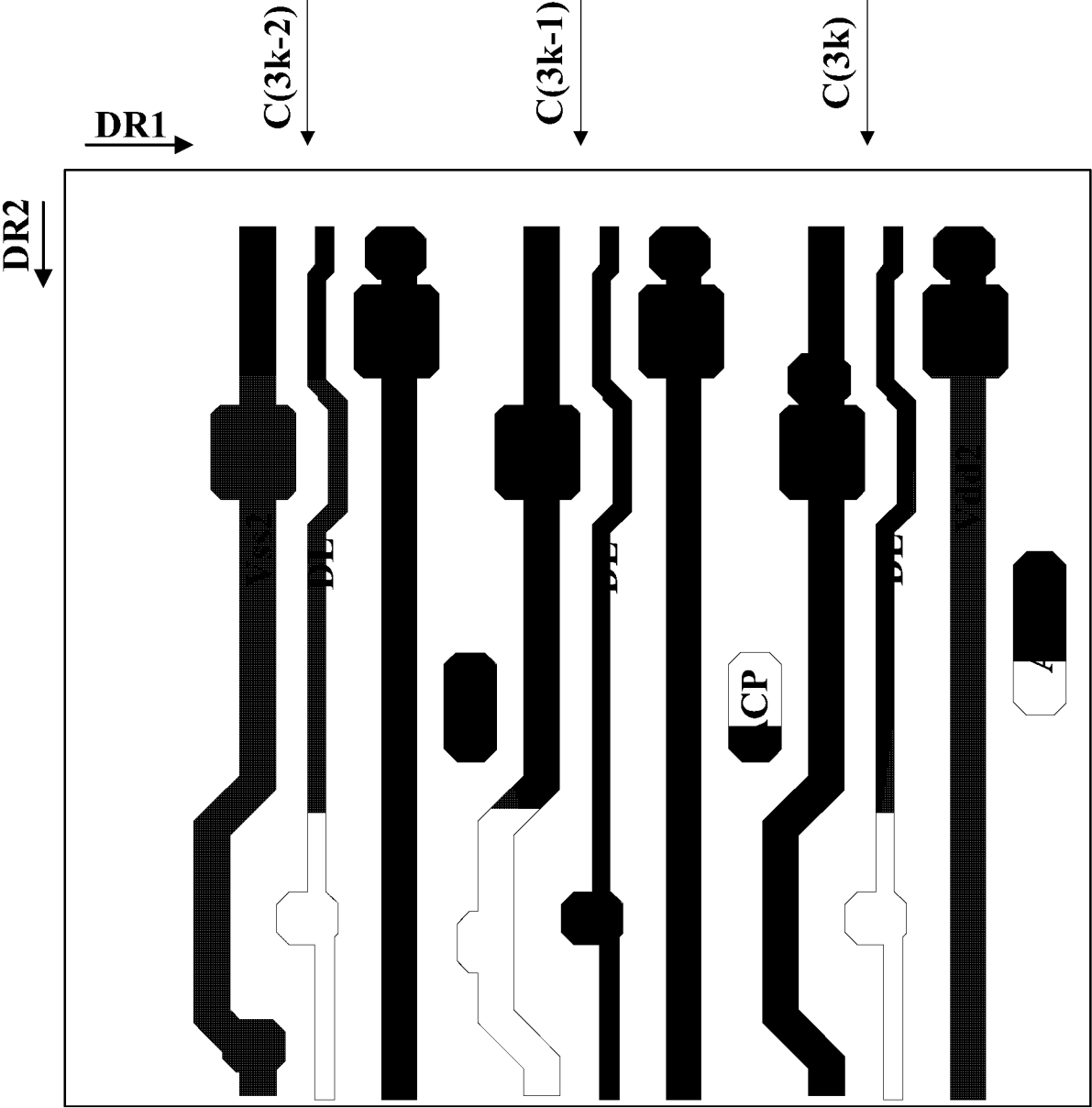


FIG. 3K

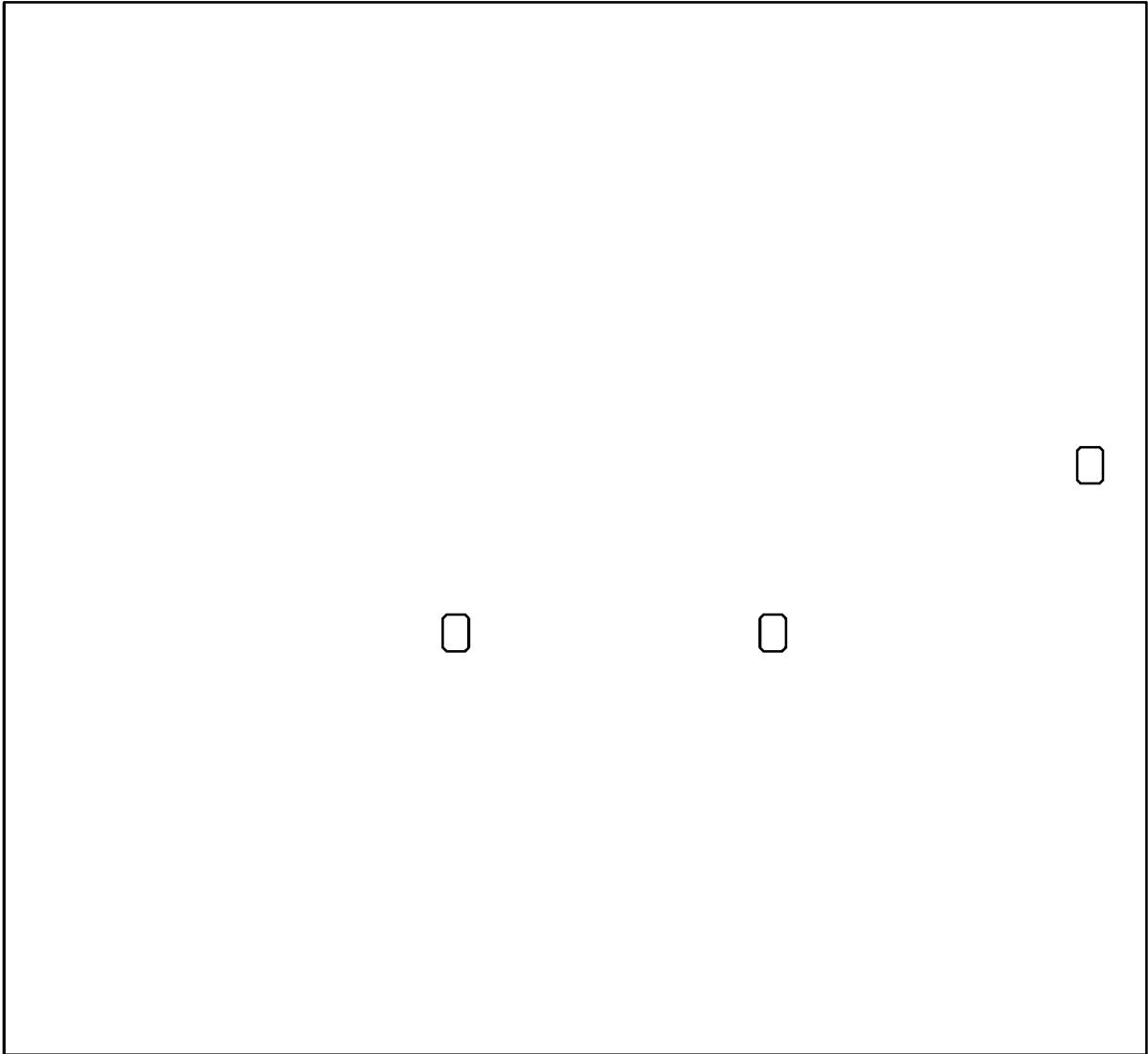


FIG. 3L

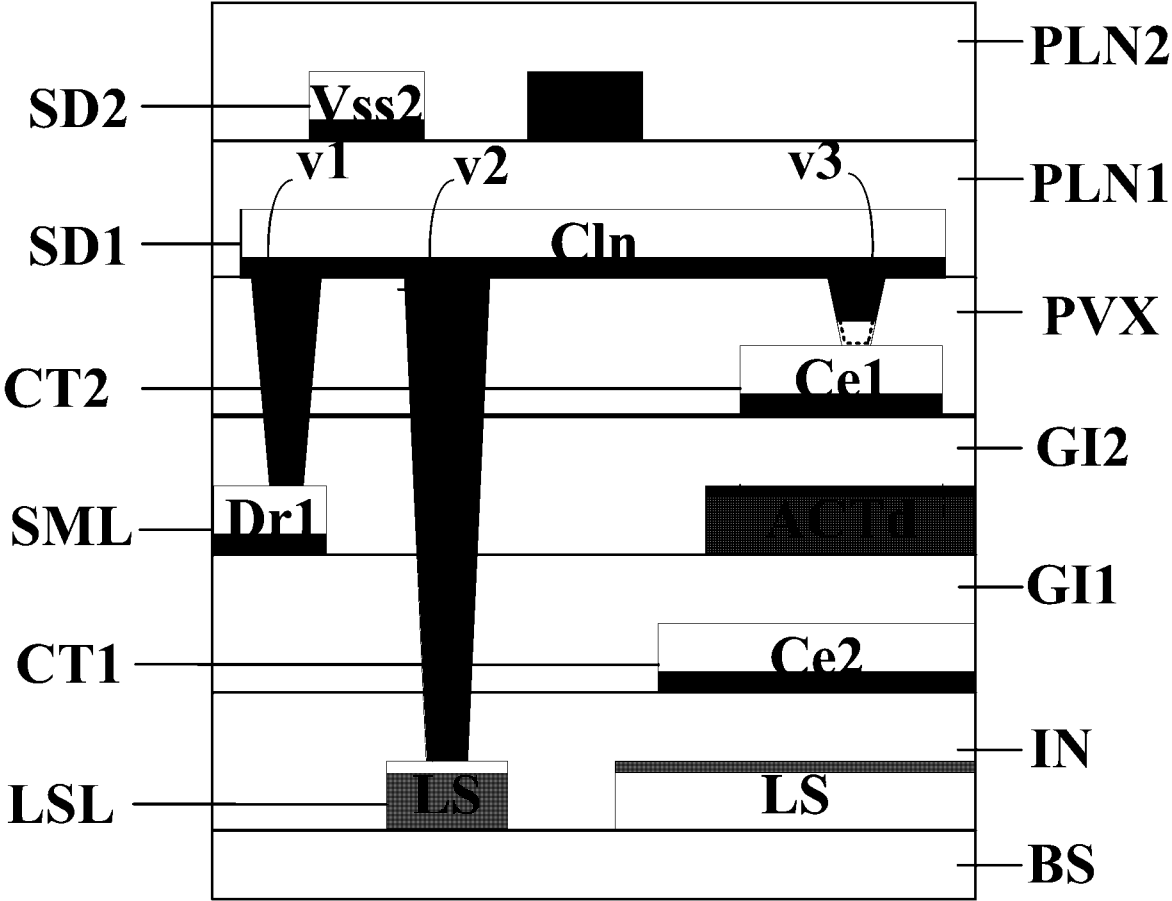


FIG. 4A

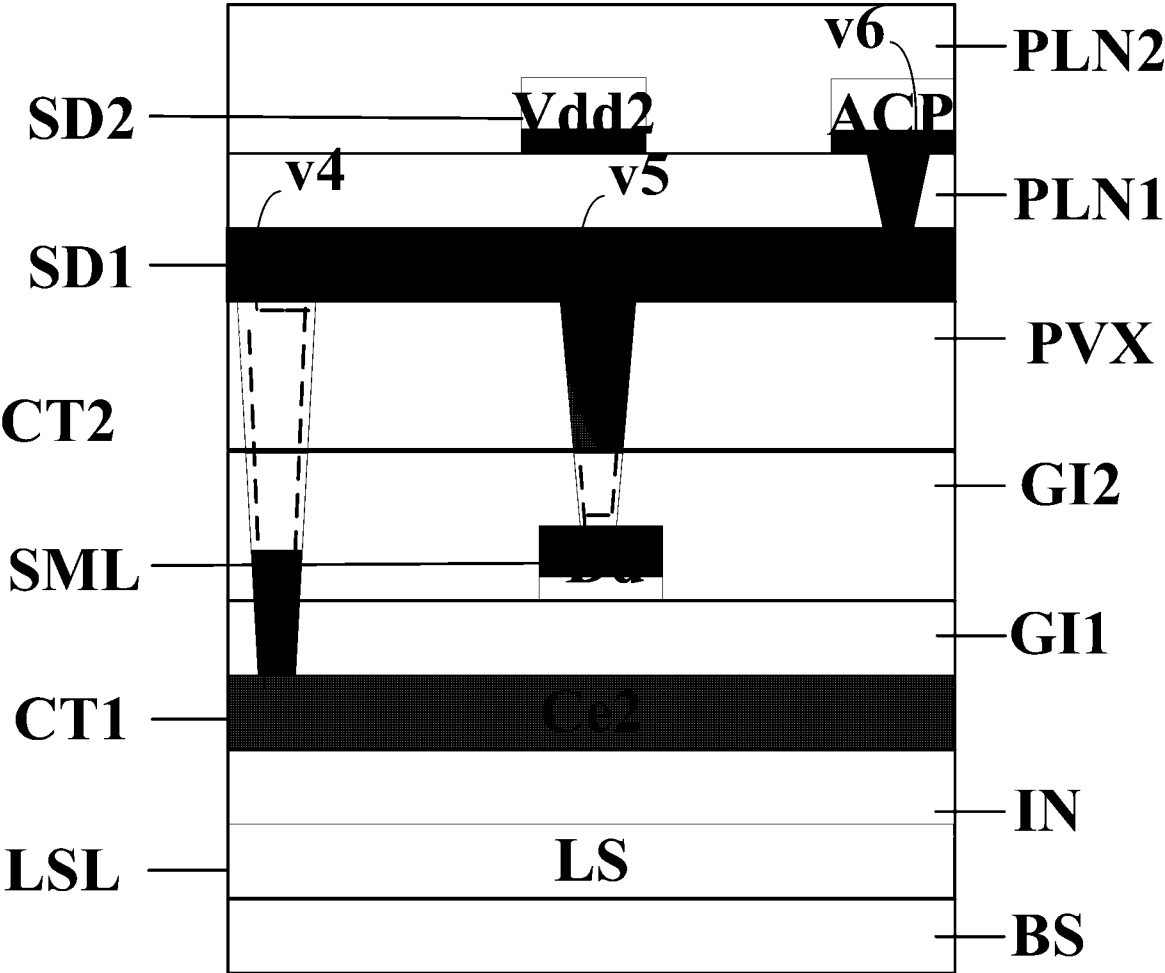


FIG. 4B

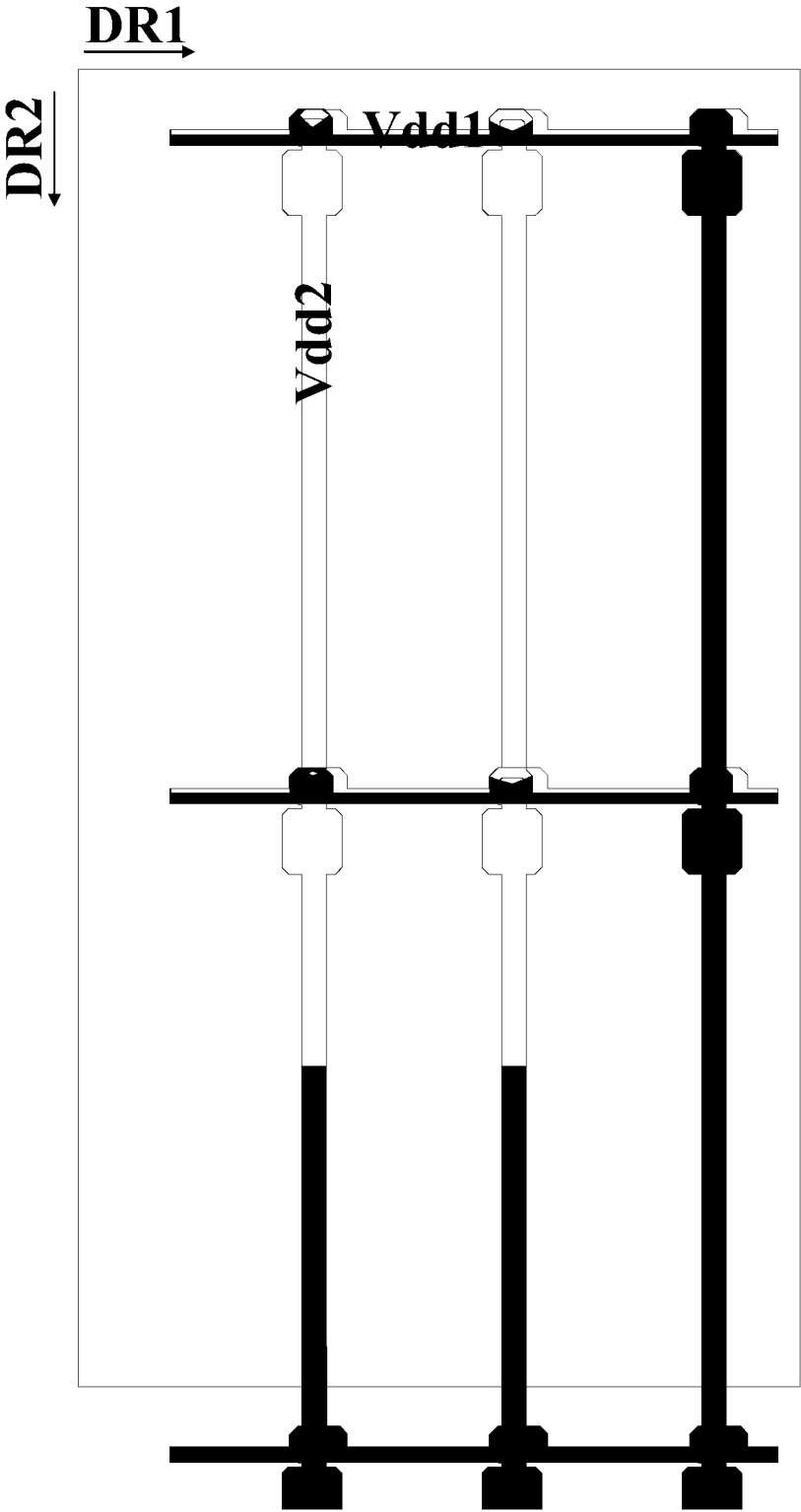


FIG. 5

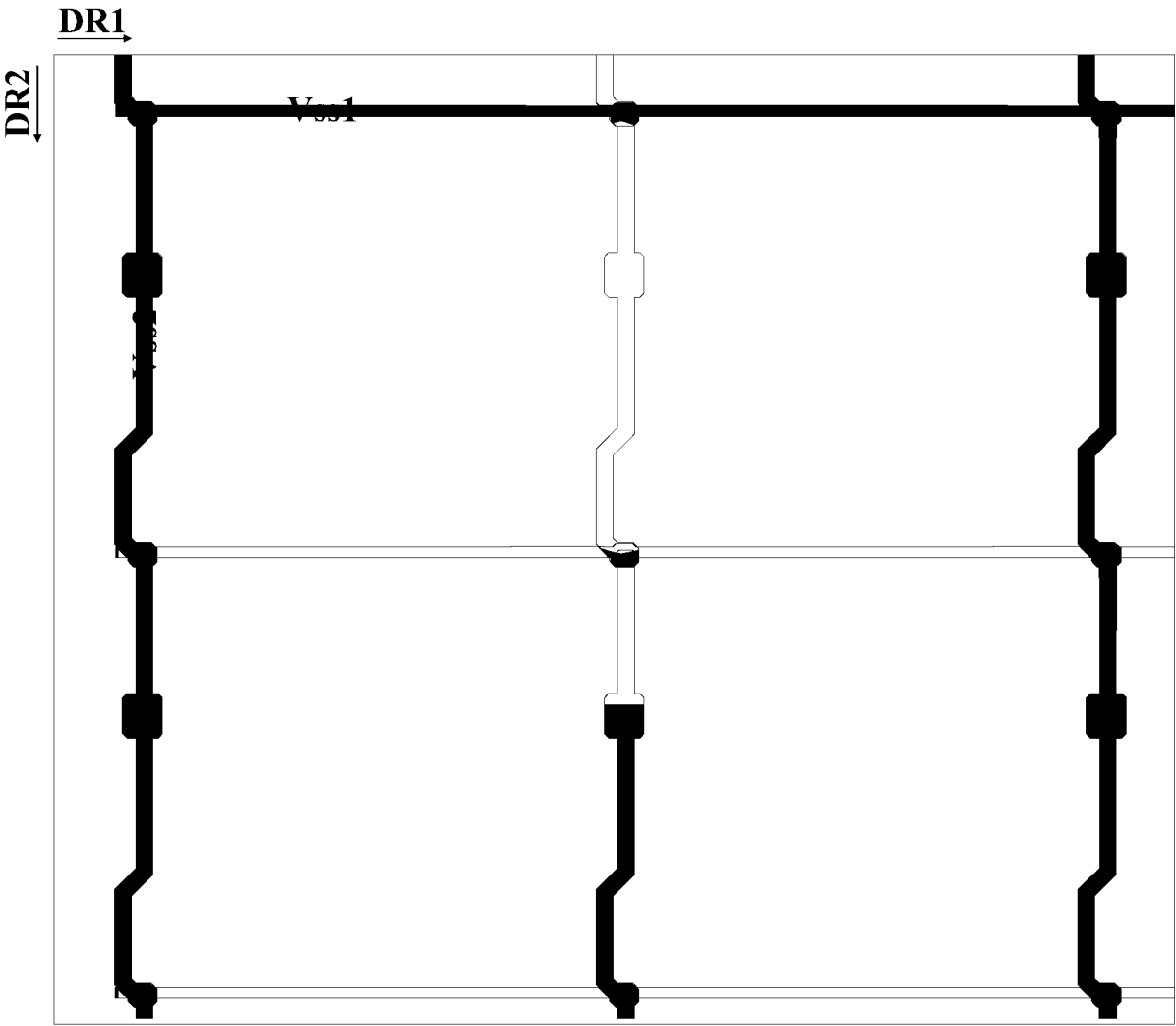


FIG. 6

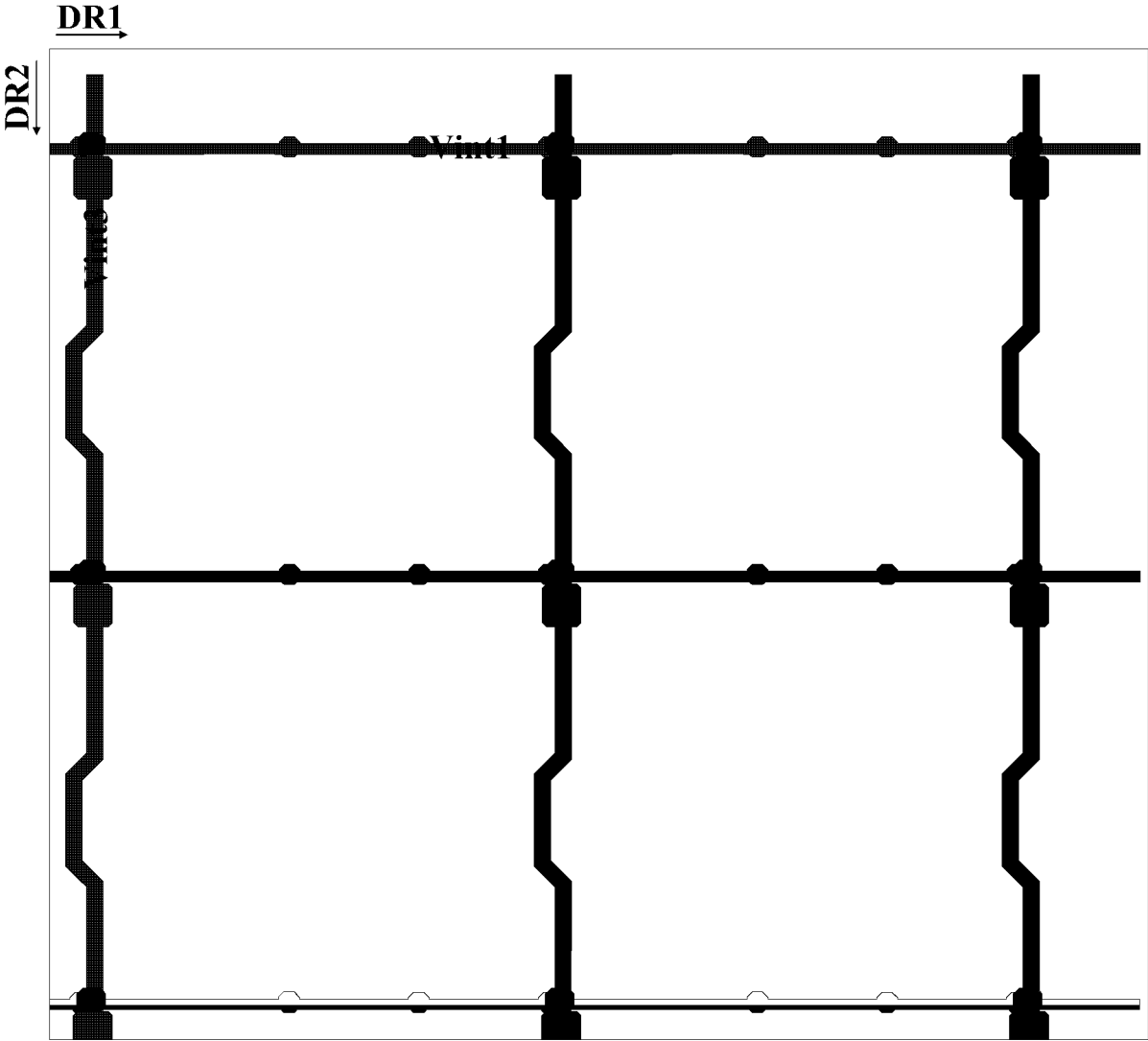


FIG. 7

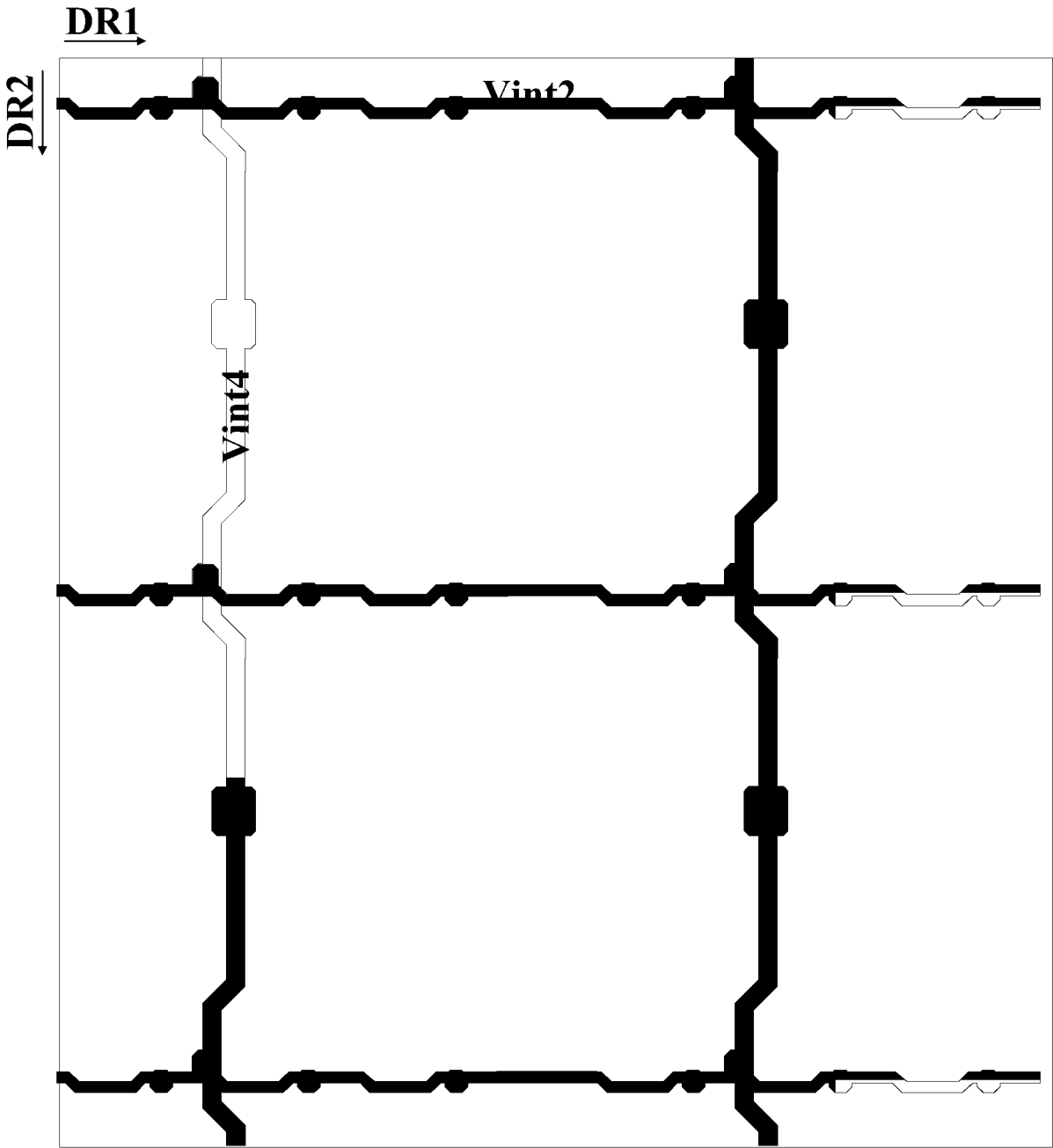


FIG. 8

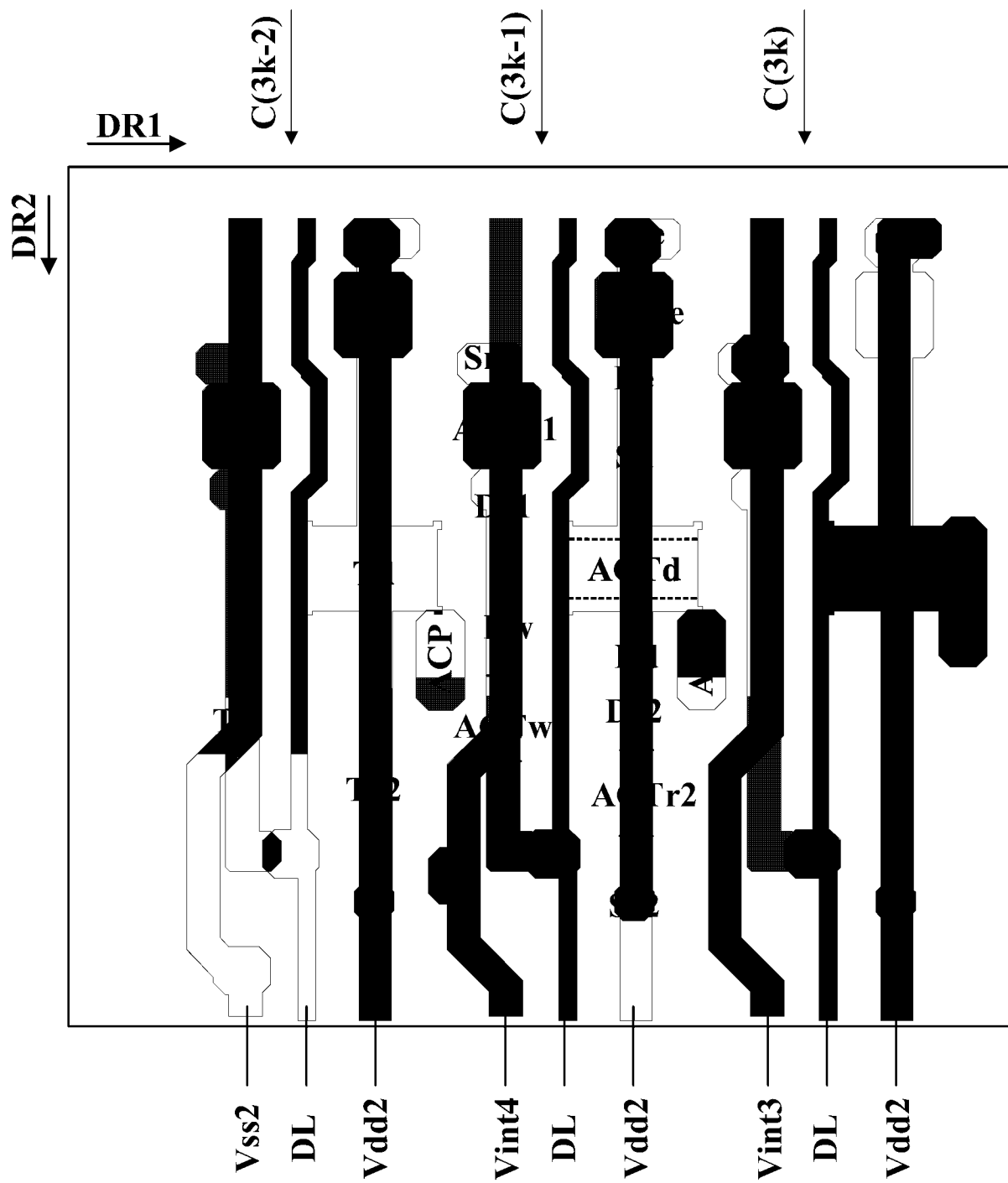


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2023/096999

A. CLASSIFICATION OF SUBJECT MATTER

H10K 59/126(2023.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H10K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT, DWPI, ENTXT, ENTXTC, CNKI: 阵列基板, 驱动电路, 像素驱动电路, 驱动三极管, 遮光, 节点, 电连接, 正投影, 覆盖, array substrate, driving circuits, pixel driving circuits, driving transistor, light shield, node, electrically connect, orthographic, cover

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 110190072 A (BOE TECHNOLOGY GROUP CO LTD ;et al.) 30 August 2019 (2019-08-30) description, paragraph [0037]-[0100], figure 2-12	1-20
Y	CN 114256296 A (BOE TECHNOLOGY GROUP CO LTD) 29 March 2022 (2022-03-29) description, paragraph [0079]-[0115], figure 1-4	1-20
A	CN 116034645 A (BOE TECHNOLOGY GROUP CO LTD ;et al.) 28 April 2023 (2023-04-28) whole document	1-20
A	US 2022320243 A1 (CHENGDU BOE OPTOELECT TECH CO;et al.) 06 October 2022 (2022-10-06) whole document	1-20
A	US 2022102459 A1 (CHENGDU BOE OPTOELECT TECH CO;et al.) 31 March 2022 (2022-03-31) whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“D” document cited by the applicant in the international application

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

10 October 2023

Date of mailing of the international search report

03 January 2024

Name and mailing address of the ISA/CN

**CHINA NATIONAL INTELLECTUAL PROPERTY
ADMINISTRATION**
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088, China

Authorized officer

YANG,WanLi

Telephone No. (+86) 62089917

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2023/096999

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	110190072	A	30 August 2019	US	2021343757	A1	04 November 2021
				WO	2020253813	A1	24 December 2020
CN	114256296	A	29 March 2022	None			
CN	116034645	A	28 April 2023	None			
US	2022320243	A1	06 October 2022	WO	2022087789	A1	05 May 2022
US	2022102459	A1	31 March 2022	US	11744112	B2	29 August 2023