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(54) **ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

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USPC **257/88**; 438/34; 257/E51.018

(57) **ABSTRACT**

An organic light emitting diode display device includes: a semiconductor layer on a substrate and including source and drain regions; a first insulating layer on the semiconductor layer; a gate electrode and a first storage electrode on the first insulating layer; a second insulating layer on the gate electrode and the first storage electrode; source and drain electrodes connected with the source and drain regions, respectively; a second storage electrode on the second insulating layer at a location corresponding to the first storage electrode; a third insulating layer on the source and drain electrodes and the second storage electrode; a first metal layer on the third insulating layer and connecting the drain electrode to an anode; and a second metal layer on the third insulating layer at a location corresponding to the second storage electrode.

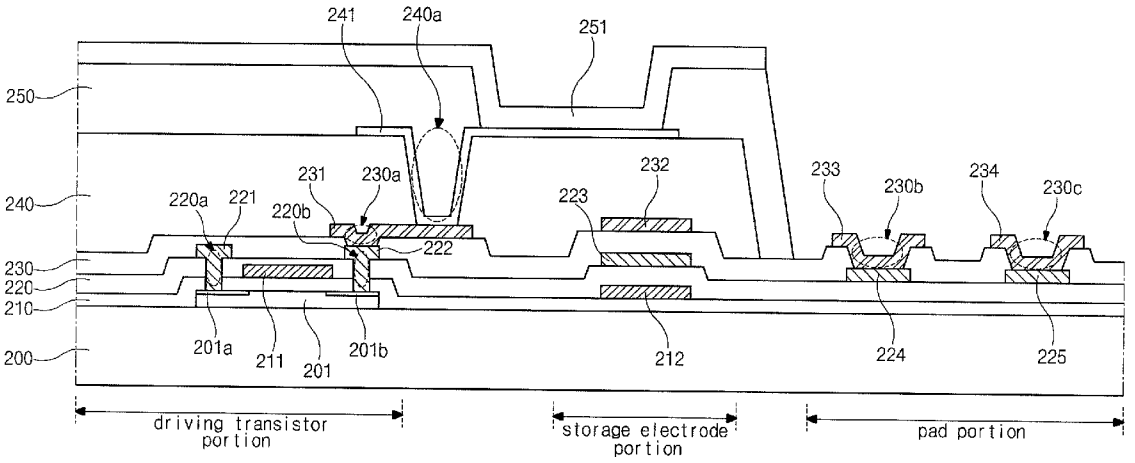


FIG. 1
RELATED ART

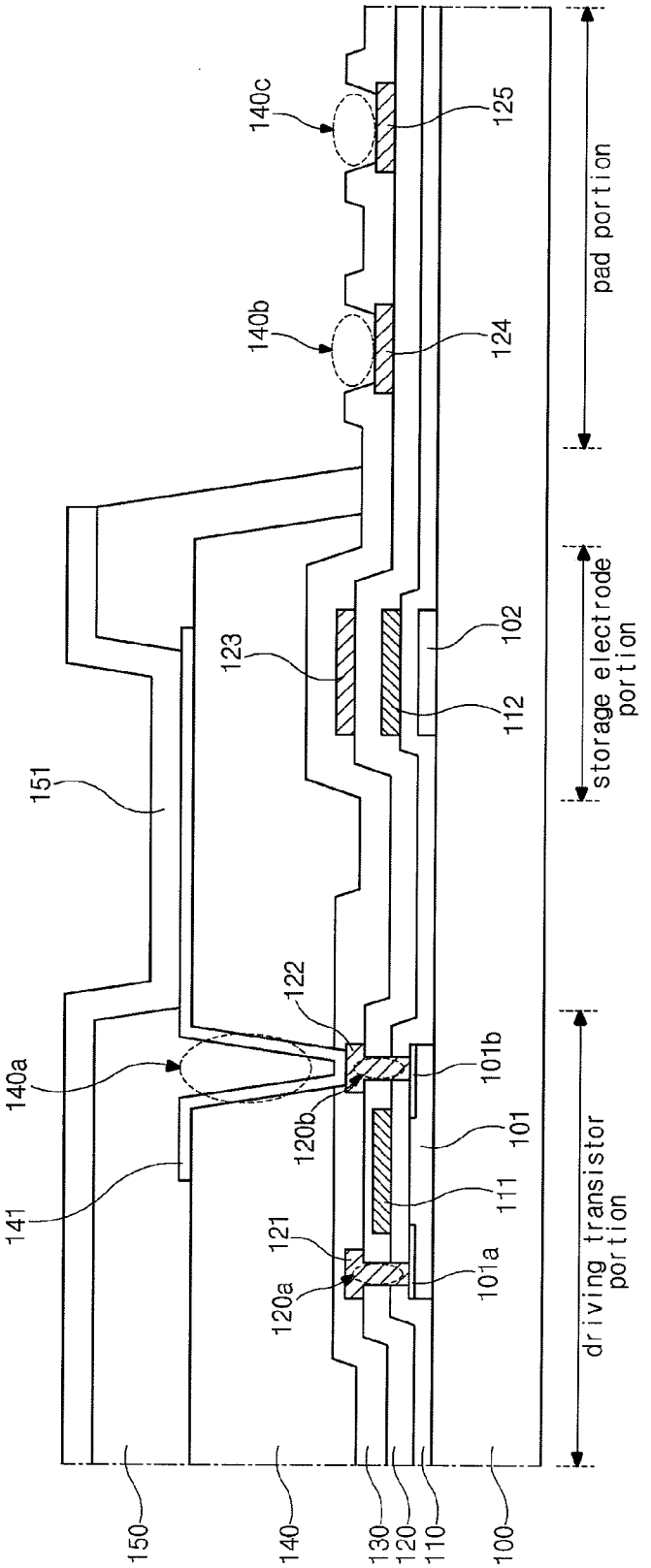


FIG. 2

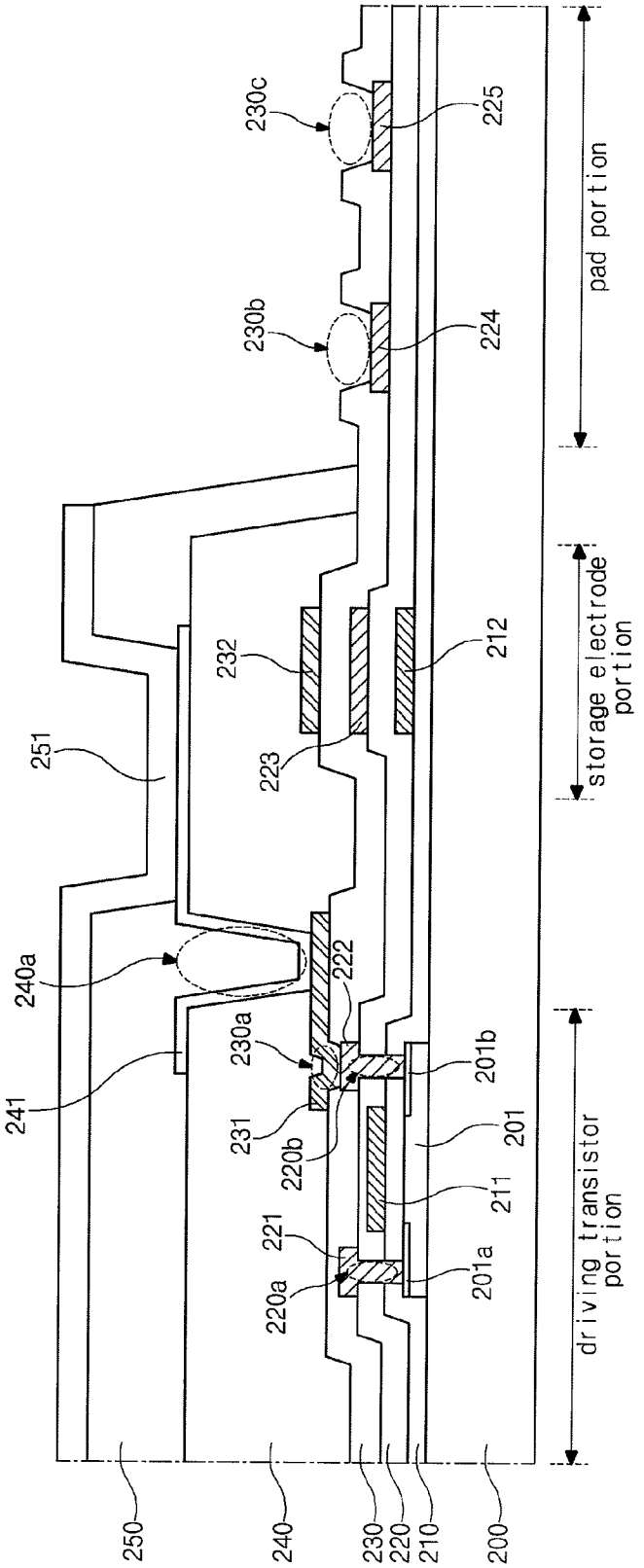

230c
225
230b
224
pad portion
232
212
251
223
storage electrode portion
240a
222
230a
201b
241
231
220b
201
211
221
201a
220a
driving transistor portion
250
240
230
220
210
200

FIG. 3

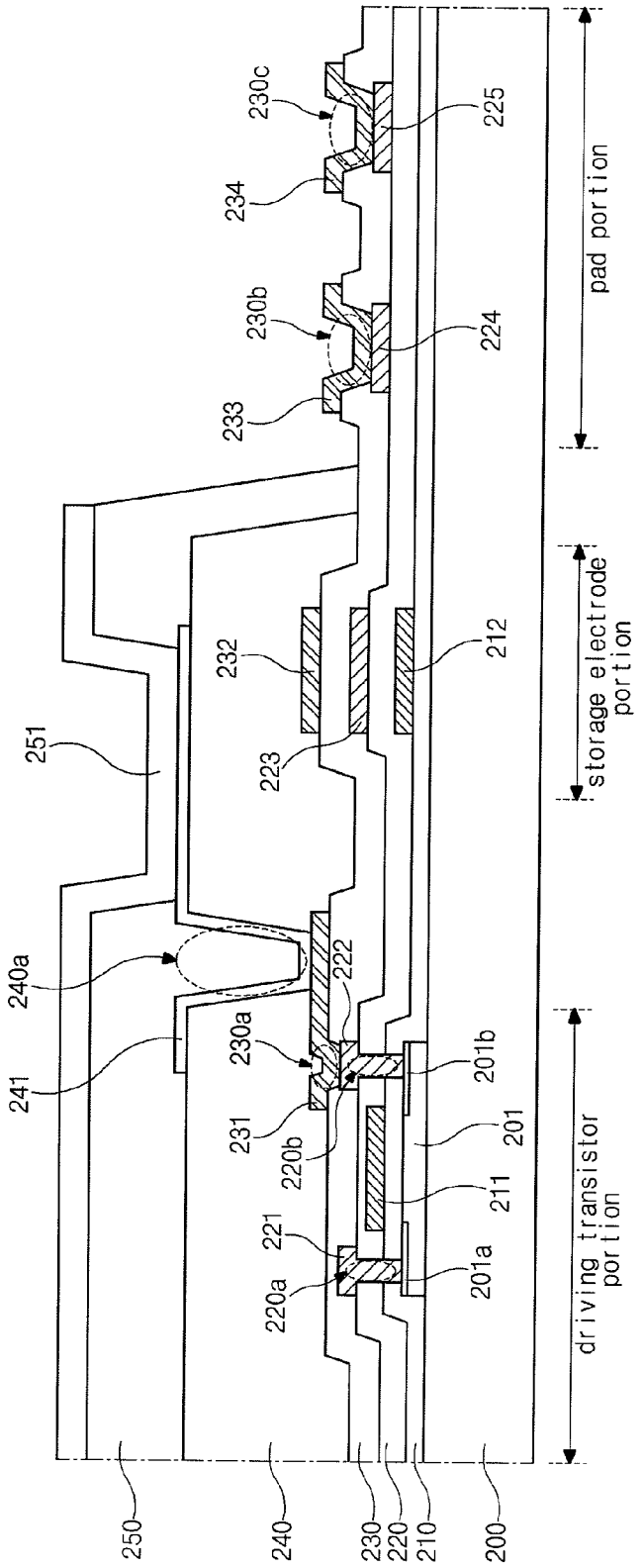

230c
225
234
230b
224
233
pad portion
232
212
251
223
storage electrode portion
240a
222
230a
201b
241
231
220b
201
211
221
220a
201a
driving transistor portion
250
240
230
220
210
200

FIG. 4A

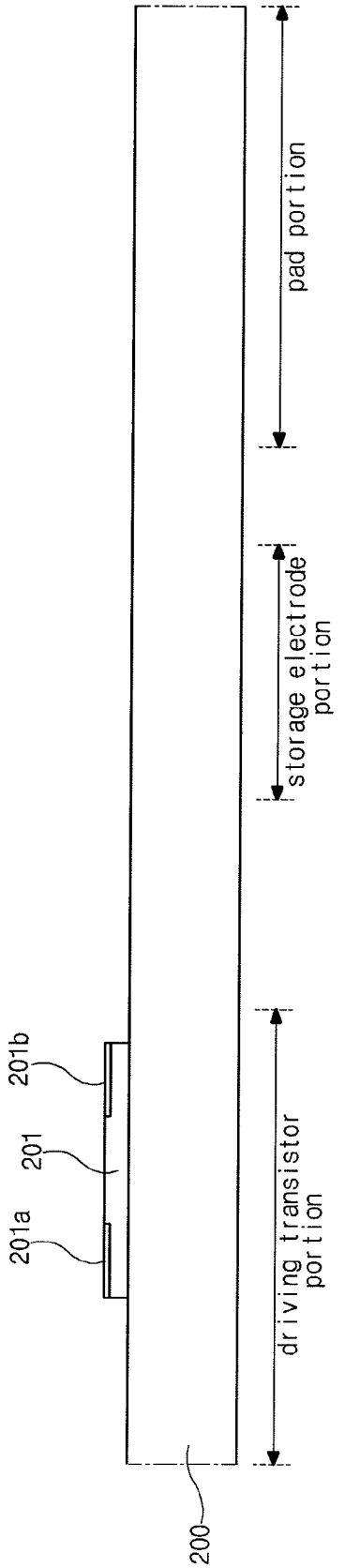

pad portion
storage electrode portion
driving transistor portion
201b
201
201a
200

FIG. 4B

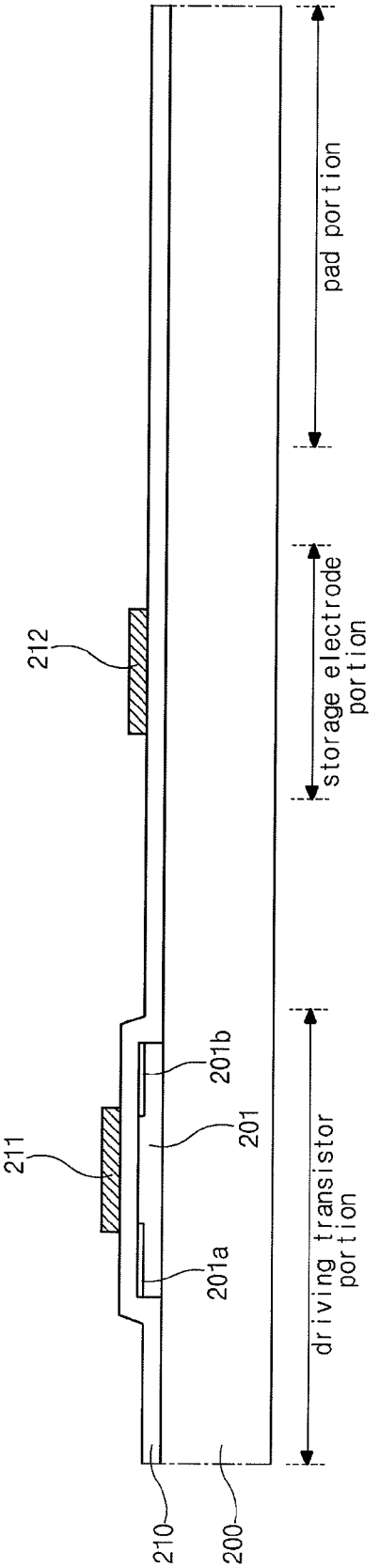

212
pad portion
storage electrode portion
211
201b
201
201a
driving transistor portion
210
200

FIG. 4C

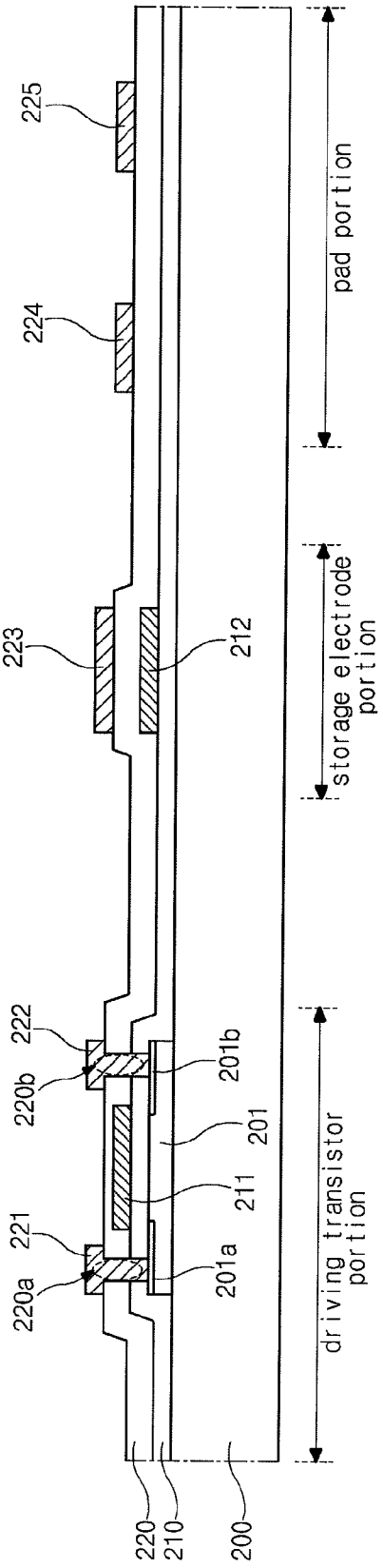

225
224
223
212
222
220b
201b
201
211
221
220a
201a
220
210
200
pad portion
storage electrode portion
driving transistor portion

FIG. 4D

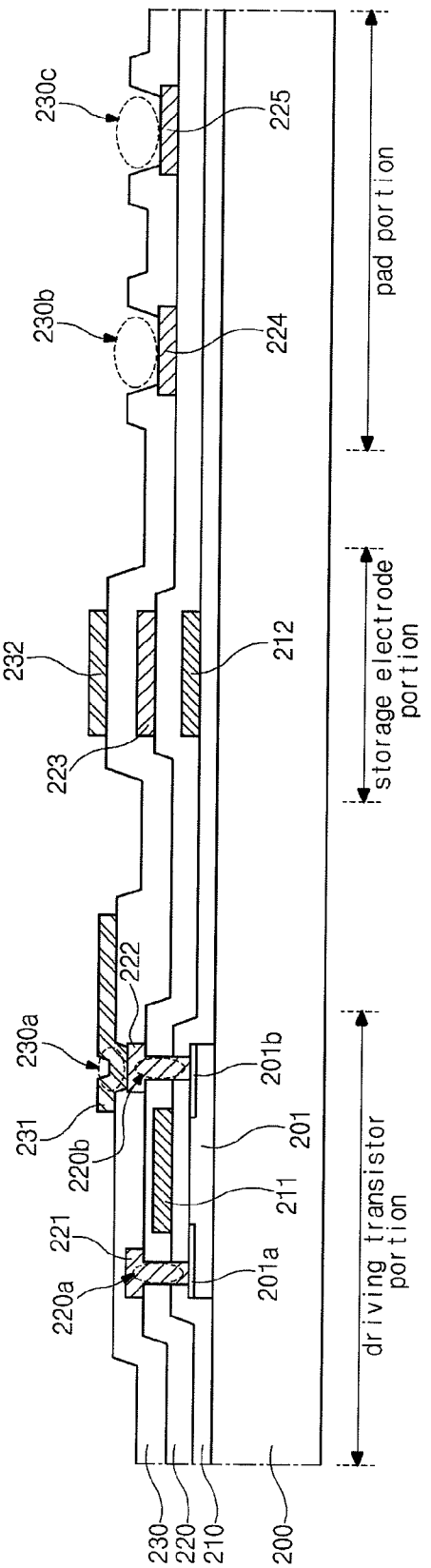

230c
225
230b
224
232
223
212
222
230a
231
220b
201b
201
211
221
220a
201a
230
220
210
200
pad portion
storage electrode portion
driving transistor portion

FIG. 5A

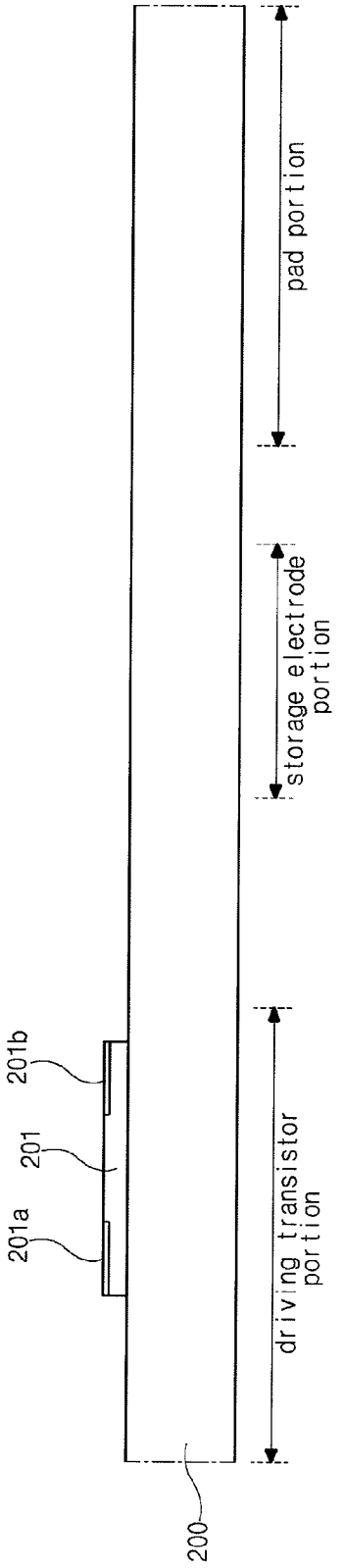

pad portion
storage electrode portion
driving transistor portion
201b
201
201a
200

FIG. 5B

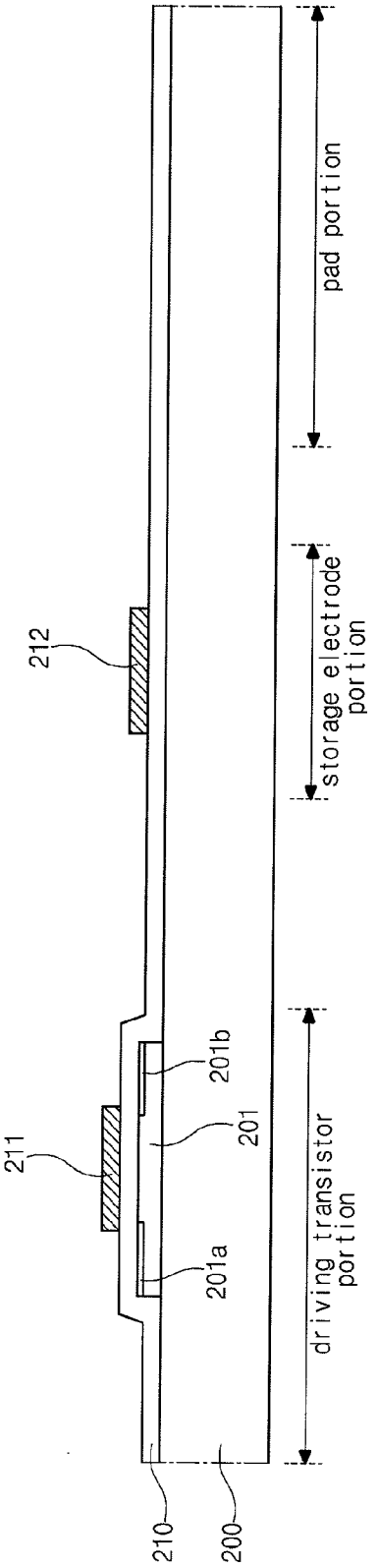

pad portion
storage electrode portion
driving transistor portion
212
211
201b
201
201a
210
200

FIG. 5C

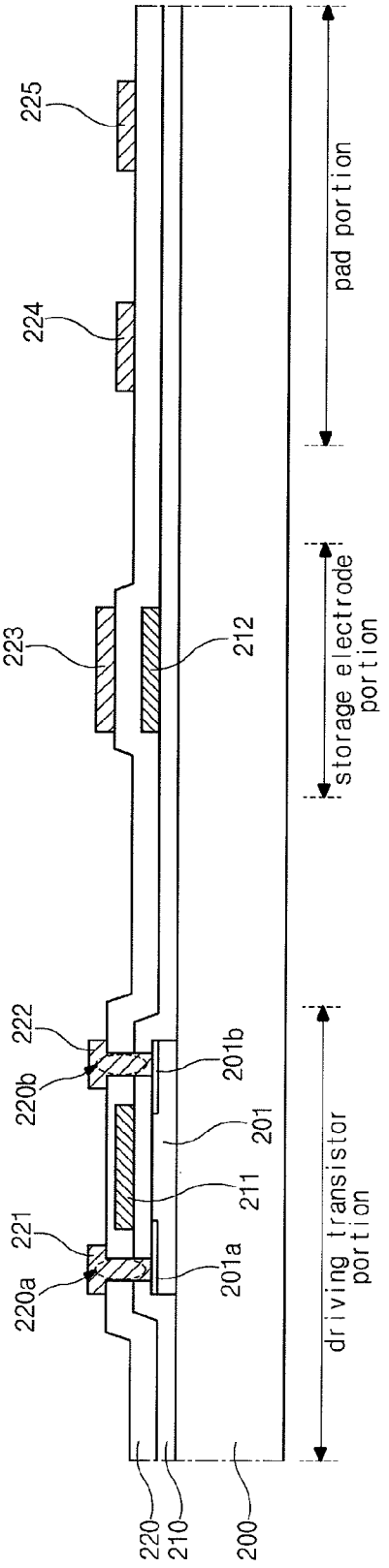
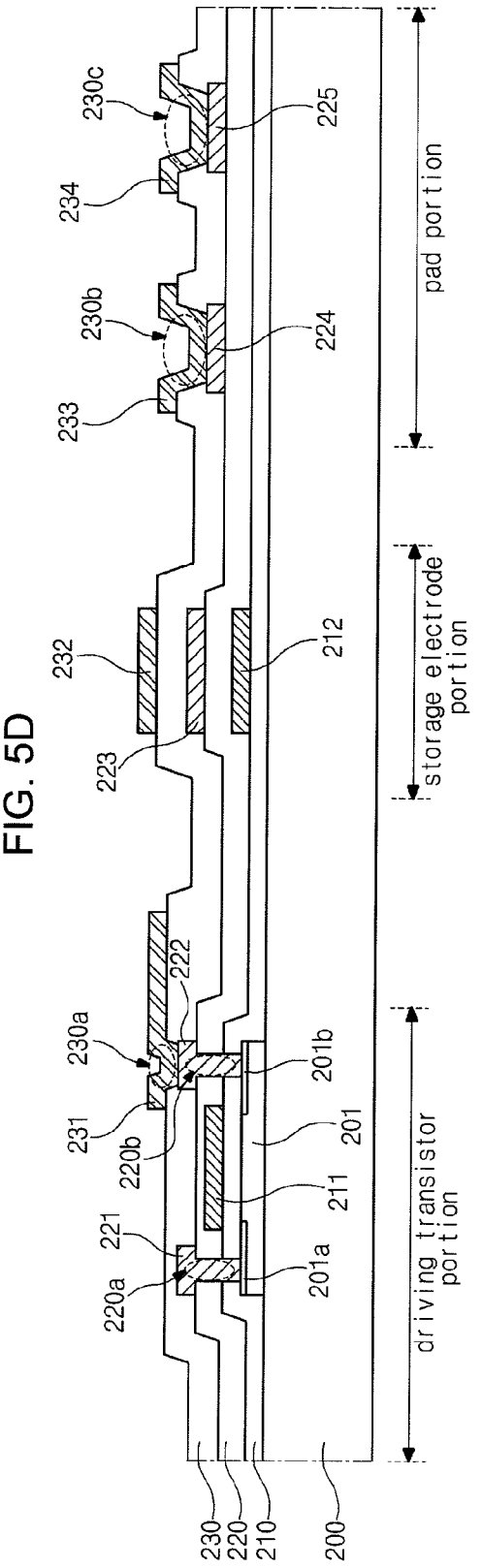

225
224
223
212
222
220b
201b
201
211
221
220a
201a
pad portion
storage electrode portion
driving transistor portion
220
210
200

FIG. 5D


230c
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222
230a
231
220b
201b
201
211
221
220a
201a
pad portion
storage electrode portion
driving transistor portion
230
220
210
200

ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2012-0018612, filed in Korea on Feb. 23, 2012, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] Embodiments of the invention relate to an organic light emitting diode display device and a method of manufacturing the same, and more particularly, to an organic light emitting diode display device and a method of manufacturing the same achieving high resolution in large size.

[0004] 2. Discussion of the Related Art

[0005] Recently, many efforts and studies have been being made to develop flat panel displays, such as liquid crystal display (LCD) devices and organic light emitting diode (OLED) display devices, as substitute for cathode-ray tubes (CRTs).

[0006] Of these flat panel displays, since the OLED display devices are self-luminescent without a need for a light source, have a thinner profile, are lighter weight, and have better color reproduction than the LCD devices, the OLED display devices have come into the spotlight as next-generation display devices.

[0007] The OLED display device is generally categorized into a passive type and an active type. Among these types, the active type OLED display device, which includes a thin film transistor in each pixel and has low power consumption and advantage in resolution, is widely used to realize a high-resolution and large-sized image display device.

[0008] FIG. **1** is a cross-sectional view illustrating an active type OLED display device according to a related art. Referring to FIG. **1**, in the related art OLED display device, a semiconductor layer **101** and a first storage electrode **102** are formed on a substrate **100**. On the semiconductor layer **101** and the second storage electrode **102**, a gate electrode **111**, a source electrode **121**, a drain electrode **122**, a second storage electrode **112** and a third storage electrode **123** are formed with a plurality of insulating layers **110**, **120**, **130** and **140** located thereamong.

[0009] A gate pad **124** connected with a gate electrode of a switching transistor and a data pad **125** connected with a source electrode of the switching transistor are formed below the third insulating layer **130**.

[0010] The source electrode **121** and the drain electrode **122** are formed on the second insulating layer **120**, and the drain electrode **122** is connected with an anode **141**. An organic light emitting layer **151** is formed on the anode **141** and a bank layer **150** formed on the fourth insulating layer **140**.

[0011] A second storage electrode **112** is formed on the first insulating layer **110** corresponding to the first storage electrode **102**. In a similar manner, a third storage electrode **123** is formed on the second insulating layer **120** corresponding to the second storage electrode **112**. The storage electrodes **102**, **112** and **123** function to produce a capacitance and maintain light emission of the organic light emitting layer **151** even when a gate signal is not applied. As the number of the storage electrodes **102**, **112** and **123** is increased a capacitance sufficient to operate the organic light emitting layer **151** is achieved. However, since a size of each pixel region is limited, circuit design reducing the occupied area of the storage electrodes is required in order to achieve high resolution with high integration in the space limited pixel region.

[0012] Regarding a large-sized panel, a voltage drop occurs as a pixel is farther from a power supply terminal. If the voltage drop is not compensated, disuniformity of brightness may occur. Since the pixel regions have the same limited area, as components for compensation circuits including the storage electrodes increase, degree of integration is reduced and high resolution is thus difficult to achieve.

[0013] Further, since a third contact hole **140***a* is formed by etching two layers, and in particular, a height of the fourth insulating layer **140** formed for planarization is great, a step of the third contact hole **140***a* formed in the fourth insulating layer **140** is greater than other contact holes. The anode **141** formed on the third contact hole **140** having the great step is uneven in thickness or partially cut, and this may cause problems in electric connection.

[0014] Further, the gate pad **124** and the data pad **125** are exposed after the fourth contact hole **140***b* and the fifth contact hole **140***c* are formed. When the pads **124** and **125** are exposed for a long time until a layer is formed thereon, the pads **124** and **125** may be oxidized and damaged. The damage of the pads **124** and **125** may cause an unstable electric connection.

[0015] Among the storage electrodes **102**, **112** and **123**, the second storage electrode **112** and the third storage electrode **123** are made of metal while the first storage electrode **102** is made of a silicon group material, which is the same one of the semiconductor layer **101**. Accordingly, to use the first storage electrode **102** as an electrode, an additional semiconductor process such as a doping process is required, and this reduces process efficiency.

SUMMARY OF THE INVENTION

[0016] Accordingly, embodiments of the invention are directed to an organic light emitting diode display device and a method of manufacturing the same that substantially obviates one or more of the problems due to limitations and disadvantages of the related art, and provide other advantages.

[0017] An advantage of the invention is to provide an organic light emitting diode display device and a method of manufacturing the same that can achieve high resolution, improve uniformity of brightness in large-size, increase stability in electric connection, and improve process efficiency.

[0018] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0019] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, an organic light emitting diode display device includes: a substrate; a semiconductor layer on the substrate and including source and drain regions; a first insulating layer on the semiconductor layer; a gate electrode and a first storage electrode on the first insulating layer; a

second insulating layer on the gate electrode and the first storage electrode; source and drain electrodes connected with the source and drain regions, respectively; a second storage electrode on the second insulating layer at a location corresponding to the first storage electrode; a third insulating layer on the source and drain electrodes and the second storage electrode; a first metal layer on the third insulating layer and connecting the drain electrode to an anode; and a second metal layer on the third insulating layer at a location corresponding to the second storage electrode.

[0020] In another aspect, a method of manufacturing an organic light emitting diode display device includes: sequentially forming a semiconductor layer and a first insulating layer on a substrate, the semiconductor layer including source and drain regions; forming a gate electrode and a first storage electrode on the first insulating layer; forming a second insulating layer on the gate electrode and the first storage electrode, and patterning the second insulating layer to form contact holes exposing the source and drain regions, respectively; forming source and drain electrodes at the contact holes, respectively, and a second storage electrode on the second insulating layer at a location corresponding to the first storage electrode; forming a third insulating layer on the source and drain electrodes and the second storage electrode; forming a first metal layer on the third insulating layer; and forming a second metal layer on the third insulating layer at a location corresponding to the second storage electrode.

[0021] It is to be understood that both the foregoing general description and the following detailed description are by way of example and explanatory, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0023] In the drawings:

[0024] FIG. **1** is a cross-sectional view illustrating an active type OLED display device according to a related art;

[0025] FIG. **2** is a cross-sectional view illustrating an OLED display device according to a first embodiment of the invention

[0026] FIG. **3** is a cross-sectional view illustrating an OLED display device according to a second embodiment of the invention;

[0027] FIGS. **4**A to **4**D are cross-sectional views illustrating a method of manufacturing the OLED display device according to the first embodiment of the invention; and

[0028] FIGS. **5**A to **5**D are cross-sectional views illustrating a method of manufacturing the OLED display device according to the second embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0029] Reference will now be made in detail to illustrated embodiments of the invention, which are illustrated in the accompanying drawings.

[0030] FIG. **2** is a cross-sectional view illustrating an OLED display device according to a first embodiment of the invention. Referring to FIG. **2**, the OLED display device of the first embodiment includes a substrate **200**, a semiconductor layer **201**, a plurality of insulating layers **210**, **220**, **230** and **240**, a plurality of contact holes **220***a*, **220***b*, **230***a*, **230***b*, **230***c* and **240***a*, a gate electrode **211**, a source electrode **221**, a drain electrode **222**, first and second storage electrodes **212** and **223**, first and second metal layers **231** and **232**, a bank layer **250** and an organic light emitting layer **251**.

[0031] The semiconductor layer **201** is formed on the substrate **200** and includes a source region **201***a* and a drain region **201***b*. The first insulating layer **210** is formed on the semiconductor layer **201**. The gate electrode **211** and the first storage electrode **212** are formed on the first insulating layer **210**. The gate electrode **211** is supplied with a gate signal and produces a channel in the semiconductor layer **201**.

[0032] The second insulating layer **220** is formed on the gate electrode **211** and the first storage electrode **212**. When the second insulating layer **220** is patterned, the first and second contact holes **220***a* and **220***b* exposing the source and drain regions **201***a* and **201***b*, respectively, are formed, and the source and drain electrodes **221** and **222** are formed thereat. Thus, the source and drain electrodes **221** and **222** are connected with the source and drain regions **201***a* and **201***b*, respectively. Accordingly, when a gate electrode **211** is supplied with a signal, a channel is formed and a data signal is transferred from the source electrode **221** to the drain electrode **222**.

[0033] The second storage electrode **223** is formed on the second insulating layer **220** at a location corresponding to (or overlapping) the first storage electrode **212**. The third insulating layer **230** is formed on the source electrode **221**, the drain electrode **222** and the second storage electrode **223**. The second storage electrode **223** and the first storage electrode **212** together form a capacitor.

[0034] When the source electrode **221**, the drain electrode **222** and the second storage electrode **223** are formed, a gate pad **224** connected with a gate electrode of a switching transistor and a data pad **225** connected with a source electrode of the switching transistor are formed. The gate pad **224** and the data pad **225** are formed on the second insulating layer **220**.

[0035] A data signal applied to the data pad **225** is periodically transferred from the source electrode of the switching transistor to a drain electrode of the switching transistor according to a gate signal supplied from the gate pad **224**, and is then transferred to the gate electrode **211** of a driving transistor portion connected with the drain electrode of the switching transistor. The data signal transferred to the gate electrode **211** forms a channel in the semiconductor layer **201**, and a power voltage at the source electrode is thus transferred to the drain electrode **222**. The power voltage is transferred to the organic light emitting layer **251** via the drain electrode **222** and operates the organic light emitting layer **251**.

[0036] The first metal layer **231** is formed on the third insulating layer **230** to connect the drain electrode **222** to the anode **241**. By patterning the third insulating layer **230**, the first metal layer **231** is formed at the third contact hole **230***a* exposing the drain electrode **222**. Further, when forming the third contact hole **230***a*, the fourth contact hole **230***b* and the fifth contact hole **230***c* exposing the gate pad **224** and the data pad **225**, respectively, may be formed.

[0037] The first metal layer **231** may be made of a metal including one of molybdenum (Mo), copper (Cu) and aluminum (Al). In particular, the first metal layer **231** may have a double-layered structure of (or a multiple layer structure of), for example, aluminum-neodymium (AlNd)/molybdenum

(Mo) or copper (Cu)/molybdenum-titanium (MoTi). An end of the first metal layer **231** is connected with the drain electrode **222**, and the other end of the first metal layer **231** is connected with the anode **241**, and to do this, the first metal layer **231** extends toward the anode **241**. Since the first metal layer **231** transfers the power voltage to the anode **241** to operate the organic light emitting diode **251**, the first metal layer **231** functions as a signal line in a pixel and also forms a mesh structure crossing a power voltage line. Through such a mesh structure of a signal line, a voltage transferred to a pixel farther from the power voltage terminal is compensated, and uniformity of brightness of a panel can thus be improved particularly for a large-sized OLED display device.

[0038] The second metal layer **232** is formed on the third insulating layer **230** corresponding to the second storage electrode **223**. Similar to the first metal layer **231**, the second metal layer **232** may be made of a metal including one of molybdenum (Mo), copper (Cu) and aluminum (Al). In particular, the second metal layer **232** may have a double-layered structure of (or a multiple layer structure of), for example, aluminum-neodymium (AlNd)/molybdenum (Mo) or copper (Cu)/molybdenum-titanium (MoTi). The second metal layer **232** and the second storage electrode **223** together form a capacitor. Accordingly, using two storage electrodes **212** and **223** and one metal layer **232**, a capacitance having an amount sufficient to maintain operation of the organic light emitting layer **251** can be formed. Accordingly, an additional doping process, as described with reference to FIG. **1** in the related art, is removed, and process efficiency can be thus improved.

[0039] The fourth insulating layer **240** is formed on the first and second metal layers **231** and **232**. The fourth insulating layer **240** is a layer for planarization, and may be made of an organic material such as poly acryl. By pattering the fourth insulating layer **240**, the sixth contact hole **240***a* is formed. The anode **241** is formed at the sixth contact hole **240***a* and directly contacts the first metal layer **231**. The first metal layer **231** is formed between the third insulating layer **230** and the fourth insulating layer **240**, and this makes a step of the sixth contact hole **240***a* be lower, and electric connection of the anode **241** can be thus stable.

[0040] The bank layer **250** is formed on the anode **241** and the fourth insulating layer **240**, and the organic light emitting layer **251** is formed on the bank layer **250** and the anode **241**. The organic light emitting layer **251** is supplied with the power voltage, which is applied to the drain electrode **222**, from the anode **241** via the first metal layer **231** and emits light.

[0041] FIG. **3** is a cross-sectional view illustrating an OLED display device according to a second embodiment of the invention. The OLED display device of the second embodiment is similar to that of the first embodiment. Accordingly, explanations of parts similar to parts of the first embodiment may be omitted for the purpose of explanations.

[0042] A third insulating layer **230** is formed on a source electrode **221**, a drain electrode **222**, a second storage electrode **223**, a gate pad **224** and a data pad **225** which are formed on a second insulting layer **220**.

[0043] By patterning the third insulating layer **230**, a third contact hole **230***a* exposing the drain electrode **222**, and fourth and firth contact holes **230***b* and **230***c* exposing the gate and data pads **224** and **225**, respectively, are formed. Third and fourth metal layers **233** and **234** are formed at the fourth and fifth contact holes **230***b* and **230***c*, respectively, and this prevents the gate and data pads **224** and **225** from being damaged in production processes.

[0044] Similar to first and second metal layers **231** and **232**, the third and fourth metal layers **233** and **234** may be made of a metal including one of molybdenum (Mo), copper (Cu) and aluminum (Al). In particular, the third and fourth metal layers **233** and **234** may have a double-layered structure of (or a multiple layer structure of), for example, aluminum-neodymium (AlNd)/molybdenum (Mo) or copper (Cu)/molybdenum-titanium (MoTi).

[0045] Further, since the first to fourth metal layers **231** to **234** are all on the third insulating layer **230**, the metal layers **231** to **234** can be simultaneously formed in one process. Since the metal layers **231** to **234** having various functions are simultaneously formed, burden in production process can be reduced despite employment of a new structure.

[0046] A method of manufacturing the OLED display device according to the first embodiment of the invention is explained with reference to FIGS. **4**A to **4**D. FIGS. **4**A to **4**D are cross-sectional views illustrating a method of manufacturing the OLED display device according to the first embodiment of the invention. Referring to FIG. **4**A, a semiconductor layer **201** including source and drain regions **201***a* and **201***b* is first formed on a substrate **200**. The source and drain regions **201***a* and **201***b* include P (positive) type or N (negative) type impurities, and the semiconductor layer **201** may be formed of amorphous silicon, polysilicon, or an oxide.

[0047] Then, referring to FIG. **4**B, a first insulating layer **210** is formed on the semiconductor layer **201**, and a gate electrode **211** and a first storage electrode **212** are formed on the first insulating layer **210**. The gate electrode **211** and the first storage electrode **212** may be formed by depositing a metal on the first insulating layer **210** using a sputtering process and then etching an unnecessary portion using a dry etching. Molybdenum (Mo) may be used as the metal. Other metals or materials maybe used.

[0048] Then, referring to FIG. **4**C, a second insulating layer **220** is formed on the gate electrode **211** and the first storage electrode **212** and is then patterned to form first and second contact holes **220***a* and **220***b* exposing the source and drain regions **201***a* and **201***b*, respectively. In more detail, a photoresist is coated on the second insulating layer **220**, and light exposure and developing are then conducted to form a photoresist pattern. The photoresist pattern is formed such that the photoresist remains on the second insulating layer **220** except for regions where the first and second contact holes **220***a* and **220***b* are formed. Then, the second insulating layer **220** and the first insulating layer **210** are etched in the regions, where the photoresist is removed, using wet etching, and the source and drain regions **201***a* and **201***b* are exposed.

[0049] Then, source and drain electrodes **221** and **222** are formed using a metal including one of molybdenum (Mo) and aluminum-neodymium (AlNd) and directly connected with the source and drain regions **201***a* and **201***b*, respectively. The source and drain electrodes **221** and **222** are formed using a sputtering process and may be formed to have a single metallic layer or multiple metallic layers of a thickness of hundreds of angstroms to thousands of angstroms. Further, a second storage electrode **223** is formed on the second insulating layer **220** corresponding to the first storage electrode **212**. The second storage electrode **223** may be formed in the same process of forming the source and drain electrodes **221** and **222**.

[0050] Then, referring to FIG. **4**D, a third insulating layer **230** is formed on the source and drain electrodes **221** and **222** and the second storage electrode **223**. The third insulating layer **230** may be made of an insulating material, for example, silicon nitride (SiNx) or silicon oxide (SiO_2), using plasma-enhanced chemical vapor deposition (PECVD). Then, in a similar manner to formation of the first and second contact holes **220***a* and **220***b*, a third contact hole **230***a* exposing the drain electrode **222** is formed, and a first metal layer **231** is formed at the third contact hole **230***a*. The first metal layer **231** is formed to have a predetermined length such that an end of the first metal layer **231** is connected with the drain electrode **222**, and the other end of the first metal layer **231** is connected with an anode **241** to be formed later.

[0051] Further, a second metal layer **232** is formed on the third insulating layer **230** corresponding to the second storage electrode **223**. The second metal layer **232** and the second storage electrode **223** together form a capacitor, and a capacitance of an amount sufficient to maintain operation of the organic light emitting layer **251** can be thus formed. Further, since the second metal layer **232** is formed using a simple process, an additional doping process can be omitted, and process efficiency can be thus improved.

[0052] A method of manufacturing the OLED display device according to the second embodiment of the invention is explained with reference to FIGS. **5**A to **5**D. FIGS. **5**A to **5**D are cross-sectional views illustrating a method of manufacturing the OLED display device according to the second embodiment of the invention. Processes of FIGS. **5**A to **5**C are substantially the same as those of FIGS. **4**A to **4**C, and explanations thereof may be omitted.

[0053] Referring to FIG. **5**D, a third insulating layer **230** is formed on a source electrode **221**, a drain electrode **222**, a second storage electrode **223**, a gate pad **224** and a data pad **225** and patterned to form a third contact hole **230***a*, a fourth contact hole **230***b* and a fifth contact hole **230***c*. The fourth and fifth contact holes **230***b* and **230***c* can be formed along with the third contact hole **230***a* by etching the third insulating layer **230** using a photolithography process. Then, first to fourth metal layers **231** to **234** are formed at the third contact hole **230***a*, on the third insulating layer **230** corresponding to the second storage electrode **223**, at the fourth contact hole **230***b*, and at the fifth contact hole **230***c*, respectively.

[0054] Further, by forming new metal layers **231**, **232**, **233** and **234** instead of reducing the number of electrodes in a storage electrode portion, design of a pixel driving portion can be easier in a limited area, and high integration and high resolution can be achieved. In particular, when the first metal layer **231** connected with the anode **241** crosses a power voltage line to form a mesh structure, voltage of a power source portion is compensated and uniformity of brightness can be thus improved. Therefore, high resolution can be achieved even for a large-sized OLED display device, and also, uniformity of brightness can be improved.

[0055] As described above, according to the embodiments of the invention, since a storage electrode are replaced with a new metal layer, degree of freedom of circuit design is obtained. Accordingly, through high integration, there is advantage in realization of high resolution.

[0056] Further, according to the embodiments of the invention, a new metal layer and a power portion connected with an anode are configured in a mesh structure. Accordingly, uniformity of brightness can be improved for a large-sized panel as well as a small-sized panel.

[0057] Further, according to the embodiments of the invention, a step of a contact portion of an anode is reduced due to a new metal layer. Accordingly, stability of electric connection can increase.

[0058] Further, according to the embodiments of the invention, a storage electrode formed using an additional doping process is replaced with a new metal layer. Accordingly, process efficiency can be improved.

[0059] It will be apparent to those skilled in the art that various modifications and variations can be made in the invention without departing from the spirit or scope of the invention. Thus, it is intended that the invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An organic light emitting diode display device, comprising:
- a substrate;
- a semiconductor layer on the substrate and including source and drain regions;
- a first insulating layer on the semiconductor layer;
- a gate electrode and a first storage electrode on the first insulating layer;
- a second insulating layer on the gate electrode and the first storage electrode;
- source and drain electrodes connected with the source and drain regions, respectively;
- a second storage electrode on the second insulating layer at a location corresponding to the first storage electrode;
- a third insulating layer on the source and drain electrodes and the second storage electrode;
- a first metal layer on the third insulating layer and connecting the drain electrode to an anode; and
- a second metal layer on the third insulating layer at a location corresponding to the second storage electrode.

2. The device according to claim **1**, further comprising gate and data pads on the second insulating layer; and
- third and fourth metal layers on the gate and data pads, respectively, that are exposed by the third insulating layer.

3. The device according to claim **2**, wherein the first to fourth metal layers are made of the same material.

4. The device according to claim **2**, wherein the first to fourth metal layers each have a single layer or multiple layers.

5. The device according to claim **2**, wherein the first to fourth metal layers are each made of a metal including at least one of molybdenum (Mo), copper (Cu), aluminum (Al), neodymium (Nd) and titanium (Ti).

6. The device according to claim **4**, wherein the multiple layers include aluminum-neodymium (AlNd) and molybdenum (Mo) layers or copper (Cu) and molybdenum-titanium (MoTi) layers.

7. A method of manufacturing an organic light emitting diode display device, the method comprising:
- sequentially forming a semiconductor layer and a first insulating layer on a substrate, the semiconductor layer including source and drain regions;
- forming a gate electrode and a first storage electrode on the first insulating layer;
- forming a second insulating layer on the gate electrode and the first storage electrode, and patterning the second insulating layer to form contact holes exposing the source and drain regions, respectively;

forming source and drain electrodes at the contact holes, respectively, and a second storage electrode on the second insulating layer at a location corresponding to the first storage electrode;

forming a third insulating layer on the source and drain electrodes and the second storage electrode;

forming a first metal layer on the third insulating layer; and

forming a second metal layer on the third insulating layer at a location corresponding to the second storage electrode.

8. The method according to claim **7**, further comprising forming gate and data pads on the second insulating layer; and

forming third and fourth metal layers on the gate and data pads, respectively, that are exposed by the third insulating layer.

9. The method according to claim **8**, wherein the first to fourth metal layers are simultaneously formed.

10. The method according to claim **8**, wherein the first to fourth metal layers each have a single layer or multiple layers.

11. The method according to claim **8**, wherein the first to fourth metal layers are each made of a metal including at least one of molybdenum (Mo), copper (Cu), aluminum (Al), neodymium (Nd) and titanium (Ti).

12. The method according to claim **10**, wherein the multiple layers include aluminum-neodymium (AlNd) and molybdenum (Mo) layers or copper (Cu) and molybdenum-titanium (MoTi) layers.

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