(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 March 2005 (17.03.2005)

PCT

(10) International Publication Number
WO 2005/024948 A2

(51) International Patent Classification[7]: H01L 27/00

(21) International Application Number: PCT/US2004/028325

(22) International Filing Date: 1 September 2004 (01.09.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/654,313 3 September 2003 (03.09.2003) US

(71) Applicant (*for all designated States except US*): **EASTMAN KODAK COMPANY** [US/US]; 343 State Street, Rochester, New York 14650-2201 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): **GUIDASH, Robert Michael** [US/US]; 460 Antlers Drive, Rochester, New York 14618 (US).

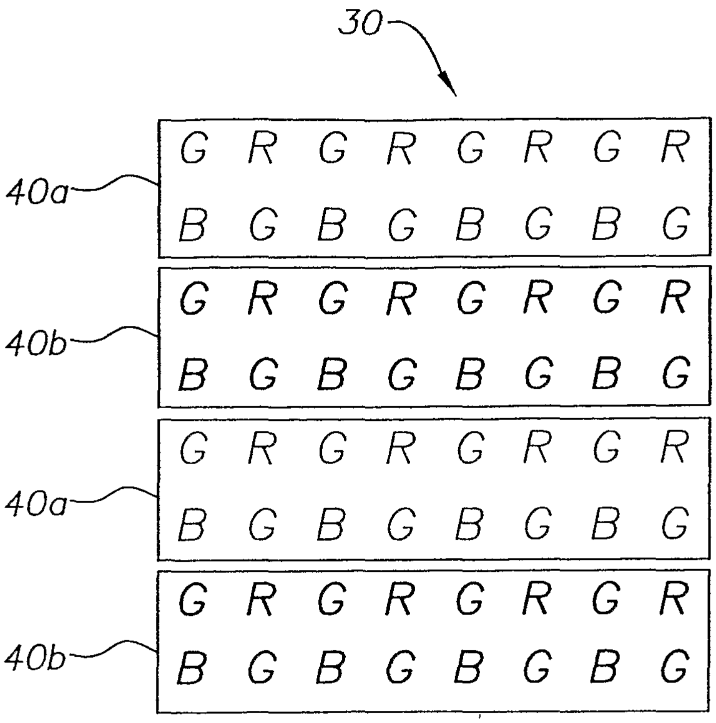
(74) Common Representative: **EASTMAN KODAK COMPANY**; 343 State Street, Rochester, New York 14650-2201 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: IMAGE SENSOR WITH EXTENDED DYNAMIC RANGE



(57) Abstract: An image sensor includes a plurality of pixels; a color filter pattern spanning at least a portion of the pixels, wherein the color filter pattern forms a color filter kernel having colors in a predetermined arrangement; and a mechanism for controlling integration time of the pixels, wherein the integration time of the plurality of pixels is spatially variant in a pattern that is correlated with the color filter array kernel.

WO 2005/024948 A2

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

IMAGE SENSOR WITH EXTENDED DYNAMIC RANGE

FIELD OF THE INVENTION

The present invention pertains to semiconductor-based image sensors with increased dynamic range.

BACKGROUND OF THE INVENTION

Solid state image sensors are now used extensively in many types of image capture applications. The two primary image sensor technologies utilized are Charge Coupled Devices CCD and CMOS x-y addressable devices. Currently, there exists many different specific embodiments of both technologies, including Active Pixel Sensors (APS) and Passive Pixel Sensors (PPS) for CMOS x-y addressable devices. All are basically comprised of a set or array of photodetectors that convert incident light into an electrical signal that can be readout and used to construct an image correlated to the incident light pattern. The exposure or integration time for the array of photodetectors can be controlled by well known mechanisms. The signal represents the amount of light incident upon a pixel photosite. The dynamic range (DR) of an imaging sensing device is defined as the ratio of the effective maximum detectable signal level, typically referred to as the saturation signal, (V_{sat}), with respect to the rms. noise level of the sensor, (σ_{noise}). This is shown in Equation 1.

Equation 1: $$\text{Dynamic Range} = V_{sat} / \sigma_{noise}$$

Image sensor devices such as charge coupled devices (CCD) that integrate charge created by incident photons have dynamic range limited by the amount of charge that can be collected and held in a given photosite, (V_{sat}). For example, for any given CCD, the amount of charge that can be collected and detected in a pixel is proportional to the pixel area. Thus for a commercial device used in a megapixel digital still camera (DSC), the number of electrons representing Vsat is on the order of 13,000 to 20,000 electrons. If the incident light is very bright and creates more electrons that can be held in the pixel or photodetector, these excess electrons are extracted by the anti-blooming mechanism in the pixel and do not contribute to an increased saturation signal. Hence, the maximum detectable signal level is limited to the amount of charge that can be held in the photodetector or pixel. The DR is also limited by the sensor noise level, σ_{noise}. Due to the limitations on Vsat, much work has been done in CCD's to decrease σ_{noise} to very low levels. Typically, commercial megapixel DSC devices have a DR of 1000:1 or less.

The same limitations on DR also exist for APS and PPS devices. The V_{sat} is limited by the amount of charge that can be held and isolated in the photodetector. Excess charge is lost. This can become even more problematic with APS and PPS compared to CCD due to the active and passive components within the pixel, limiting the area available for the photodetector, and due to the low voltage supply and clocks used in CMOS devices. In addition, since APS devices have been used to provide image sensor systems on a chip, the digital and analog circuits used on APS devices such as timing and control and analog to digital conversion, that are not present on CCD's, provide a much higher noise floor on APS devices compared to CCD. This is due to higher temporal noise as well as possibly quantization noise from the on-chip analog to digital converter.

In commonly assigned U.S. Patents 6,069,377 Guidash discloses the prior art approaches to extending dynamic range of APS devices, and discloses a new invention to extend dynamic range. This method has the disadvantage of requiring more than four transistors per pixel and limits the size of the pixel that can be made. In U.S. Patents 6,307,195 and 6,486,504 Guidash discloses extending dynamic range by collection of the charge that blooms from the photodetector, and by co-integratoin of the photodetector and floating diffusion within a single pixel. These approaches have the potential disadvantage of spatial variation of the photodetector saturation level contributing to fixed pattern noise in the sensor, and does not increase the sensitivity of the sensor.

Prior art APS devices also suffer from poor sensitivity to light due to the limited fill factor induced by integration of active components in the pixel, and by loss of transmission of incident light through the color filter layer placed above the pixel.

From the foregoing discussion it should be apparent that there remains a need within the prior art for a device that retains extended dynamic range while retaining low fixed pattern noise, small pixel, and high sensitivity.

SUMMARY OF THE INVENTION

The present invention provides a means to control the integration separately for any given spatial pattern on the image sensor, and more specifically for a pattern that is compatible with one or two dimensions of the kernel in the CFA pattern. This is done by providing separate TG or RG busses for pixels in a given row or set of rows, or by providing any means to control integration time separately for a given pattern of pixels in the image sensor array. By doing so, valid data is always available for the dark and bright regions of an image simultaneously.

Advantageous Effect Of The Invention

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1a is a prior art pixel array;

Fig. 1b is another prior art pixel array;

Fig. 2a is a pixel array of the present invention;

Fig. 2b is an alternative embodiment of the present invention;

Fig. 3 is graph graphically illustrating the implementation of Figs. 2a and 2b;

Fig. 4a is an illustration of two integration control lines per row;

Fig. 4b is an illustration of one integration time signal line per row; and

Fig. 5 is a camera for implementing the pixel array of Figs. 2a and 2b into a preferred commercial embodiment.

DETAILED DESCRIPTION OF THE INVENTION

Typical prior art image sensor pixel arrays are shown in Figs. 1a and 1b. The image sensor in Fig 1a can be of any technology type such as CCD or CMOS APS. The pixel array 10 in Fig. 1a comprises a set of photodetectors. The integration time is constant for each pixel, represented by the pixels in region 10a all having the same integration time. The drawback of this approach is that if the integration time is long, pixels in the bright areas of an image will become saturated and the image details in the bright region will be lost. If the integration time is chosen to be short, the image quality in dark regions of the image will be poor due to low signal and high noise. The image sensor in Fig 1b was disclosed in U.S. Patent Application Serial No. 08/960,418, filed July 17, 2002, entitled ACTIVE PIXEL SENSOR WITH PROGRAMMABLE COLOR BALANCE, by Guidash, in which each color of the pixel array 20 associated with the CFA pattern has a separate integration time to achieve charge domain white balance. This is represented in Fig 1b by regions indicated as 20a, green pixels in the green-red rows, region 20b, red pixels in the green-red rows, region 20c, blue pixels in the green-blue rows, and region 20d, green pixels in the green-blue rows. This has the same drawbacks as those cited for the image sensor pixel array in Fig 1a.

Referring to Fig. 2a, the image sensor pixel array 30 of the present invention includes an array that facilitates different programmable integration times, but in a different spatial pattern than that shown in Fig 1b. For an x-y addressable CMOS image sensor this can be accomplished with separate transfer gates or reset gates. For a CCD image sensor this can be accomplished by having separate transfer gates. The image sensor pixel array 30 in Fig 2a is constructed to have pixels with two different integration times for mated pairs of rows 40a and40b that are correlated with the color filter array pattern pitch or kernel. Pixels with long integration times are referred to as fast pixels. Pixels with short integration times are referred to as slow pixels. In the case of the Bayer CFA pattern, this is a two-row pitch. By having separate integration times in this pattern, the effective dynamic range of the image sensor is extended as shown in Fig. 3. In region 1, low light level region, both the slow and fast pixels of the sensor have not saturated. The fast pixels will have signal levels that are well above the noise floor. The slow pixels will have signal levels that are within a predetermined ratio compared to the sensor noise floor. In region 2, both the slow and fast pixels have not saturated, and both have adequate signal-to-noise ratio. In region 3, high light level regions, the fast pixels have saturated or clipped and do not contain valid signal level information. The slow pixels have not saturated and do contain valid signal level information with adequate signal to noise ratio. Since the valid information is correlated with the CFA pattern, the missing information from the fast pixels can be determined by interpolation of the slow pixels. With the separate integration time architecture shown in Fig 3, a single frame capture is taken, and spatially adaptive image processing performed. In region 2, standard prior art color image processing methods are employed to render an image. For an area of pixels in the image capture that fall into region 3, interpolation of the slow pixels is used to determined the missing signal information in the fast pixels. This results in a loss of true MTF in the extremely bright areas of the image, but leads to an effectively higher saturation illumination level, Isat. This effectively extends the intra-scene dynamic range of the image sensor. Although true spatial resolution is degraded in the extreme bright regions, the image content that would otherwise be lost in the image capture is preserved.

The sensor architecture of Fig. 2a is designed to provide an integration time pattern with two rows of a first integration time, and the two adjacent rows with a second integration time. This can be accomplished with any type of image sensor by having multiple or separate controls for integration time in this pattern. For CMOS and other x-y addressable image sensors this can be accomplished simply by having the image sensor timing arranged with twoseparate sets of integration pointers that are applied to the pairs of alternating rows signal lines that control integration time. This could be transfer gate lines in each row, or reset gates lines in each row, or any other per row signal that is used to control integration time for that row. In the case of CCD image sensors, this requires that the transfer gate interconnects are constructed so that there are separate and isolated connections to the transfer gate lines for at least alternating pairs of rows.

A second embodiment of the present invention is shown in the array in Fig. 2b. In this embodiment, the sensor array 50 is constructed to have two separate and programmable integration times in a 2 by 2 pixel pattern 60a and 60b. In the case of an x-y addressable image sensor technology, this is achieved by having multiple signal lines per row that are used to control integration time, such as transfer gate or reset gate. These multiple signal lines per row are connected to alternating pairs of pixels to produce the integration time pattern shown in Fig, 2b.

Referring to Fig. 4a, the routing of the multiple signal lines 70 that control integration time is shown. One disadvantage with routing multiple signal lines 70 to control integration time for each row is reduction of fill factor or a larger pixel size in order to fit the extra signal lines into the pixel pitch. This is overcome by the signal line routing architecture shown in Figure 4b. In this case a single integration time control line 80 is used per row, but it is actually routed to pixels in two adjacent rows. The signal line 80 in the adjacent row is routed in a similar manner to create the integration time pattern shown in Fig. 2b. With this approach, although a single row of data is readout from the sensor at one time, the pixels contained within the data stream are from physically adjacent rows in the array. In order to properly reconstruct the image, the interlaced data must be corrected in the camera image memory. This is also a feature of the present invention. Since either on-chip or in-camera memory can be set up to write data into two or more row locations, there is no need to have the sensor read out all pixels from a physical row at the same time.

As previously discussed, this provides an image sensor and image capture system with wide intra-scene dynamic range and wide exposure latitude.

A single image capture can render a full range of image information with optimization of the integration time for low light levels without clipping signal information in the high light regions of an image. This can greatly simplify the exposure control system and algorithms in an imaging system since choice of exposure or integration time does not need to be as precise.

It should also be noted that an image capture system using such a sensor can be used to measure or determine the dynamic range of a scene to set the two integration times appropriately. During the metering phase of a camera system, two widely separated integration times can be used to determine the maximum and minimum light levels in the scene. The two integration times can then be adjusted to cover the range of illumination in the scene. For example, if the dynamic range of the scene to be captured is within the inherent dynamic range of the image sensor, then the two integration times can be set to the same value. If the scene contains a dynamic range that is wider than the true dynamic range of the sensor, then the two integration times can be set to match or optimally cover the dynamic range of the scene.

Referring to Fig. 5, there is shown a camera 90 for implementing the image sensor of the present invention is one of many consumer-oriented commercial embodiments.

The invention has been described with reference to a preferred embodiment. However, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention.

PARTS LIST

10	pixel array
20	pixel array
20a	green pixels, in the green-red rows
20b	red pixels, in the green-red rows
20c	blue pixels, in the green-blue rows
20d	green pixels, in the green-blue rows
30	pixel array
40a	mated pair of rows
40b	mated pair of rows
50	sensor array
60a	2 by 2 pixel pattern
60b	2 by 2 pixel pattern
70	multiple signal line
80	single integration time control line
90	camera

CLAIMS:

1. An image sensor comprising:

(a) a plurality of pixels;

(b) a color filter pattern spanning at least a portion of the pixels, wherein the color filter pattern forms a color filter kernel having colors in a predetermined arrangement; and

(c) a mechanism for controlling integration time of the pixels, wherein the integration time of the plurality of pixels is spatially variant in a pattern that is correlated with the color filter array kernel.

2. The image sensor as in claim 1, wherein the color filter pattern is a Bayer color filter pattern.

3. The image sensor as in claim 1, wherein the color filter pattern is a 2x2 kernel.

4. The image sensor as in claim 3, wherein the integration time pattern is an alternating pattern of two lines at one integration time and adjacent two lines at a second integration time.

5. The image sensor as in claim 3, wherein the integration time for a first set of 2x2 pixels associated with a first kernel is at a first integration time, and the integration time of adjacent 2x2 kernels in the same set of two lines at a second integration time.

6. The image sensor as in claim 5, wherein the integration time pattern of adjacent two lines groups is offset by two pixels.

7. The image sensor of claim 1 wherein the integration time pattern is a multiple of the color filter kernel.

8. An image sensor comprising:

(a) a plurality of pixels arranged in an array of rows and columns; and

(b) a readout mechanism that provides a series of output signal values associated with a row sync signal with a number of data signal values corresponding to a number of pixels in a row or desired portion of a row; wherein the output signal values have signals that are generated from pixels within at least two physically separate rows within the array.

9. A camera comprising:

(a) an image sensor comprising:

(a1) a plurality of pixels;

(a2) a color filter pattern spanning at least a portion of the pixels, wherein the color filter pattern forms a color filter kernel having colors in a predetermined arrangement; and

(a3) a mechanism for controlling integration time of the pixels, wherein the integration time of the plurality of pixels is spatially variant in a pattern that is correlated with the color filter array kernel.

10. The camera as in claim 9, wherein the color filter pattern is a Bayer color filter pattern.

11. The camera as in claim 9, wherein the color filter pattern is a 2x2 kernel.

12. The camera as in claim 11, wherein the integration time pattern is an alternating pattern of two lines at one integration time and adjacent two lines at a second integration time.

13. The camera as in claim 11, wherein the integration time for a first set of 2x2 pixels associated with a first kernel is at a first integration time, and

the integration time of adjacent 2x2 kernels in the same set of two lines at a second integration time.

14. The camera as in claim 13, wherein the integration time pattern of adjacent two lines groups is offset by two pixels.

15. The camera as in claim 1, wherein the integration time pattern is a multiple of the color filter kernel.

16. The camera as in claim 9 further comprising a mechanism that reads out at least a subset of the plurality of pixels and uses the signal values obtained from the readout to determine the integration times of the plurality of pixels.

17. A camera comprising:

(a) an image sensor comprising:

(b) a plurality of pixels arranged in an array of rows and columns; and

(c) a readout mechanism that provides a series of output signal values associated with a row sync signal with a number of data signal values corresponding to a number of pixels in a row or desired portion of a row; wherein the output signal values have signals that are generated from pixels within at least two physically separate rows within the array.

18. The camera as in claim 17, wherein the data values are reconstructed in the camera memory.

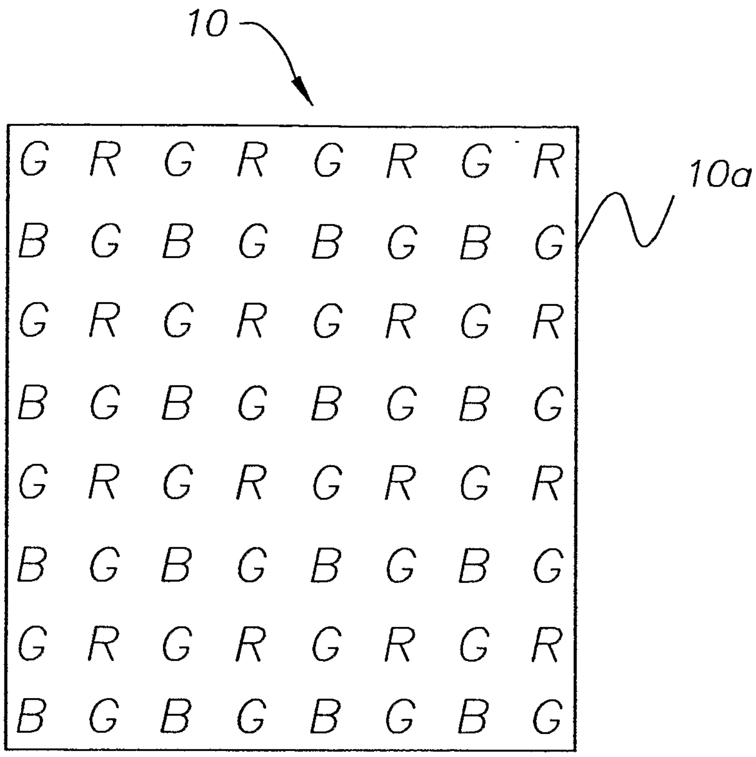


FIG. 1a
(Prior Art)

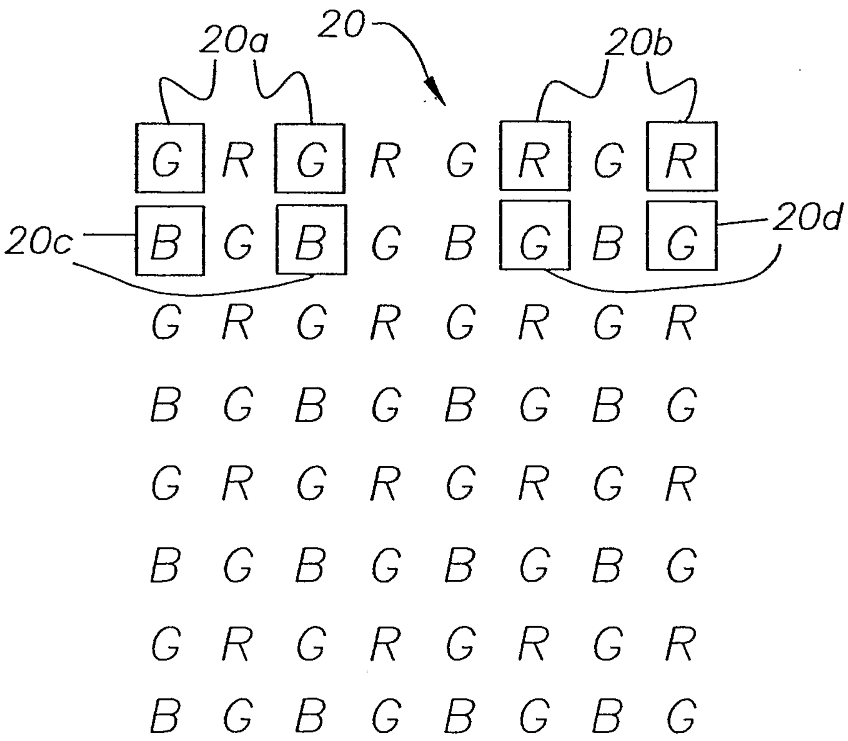


FIG. 1b
(Prior Art)

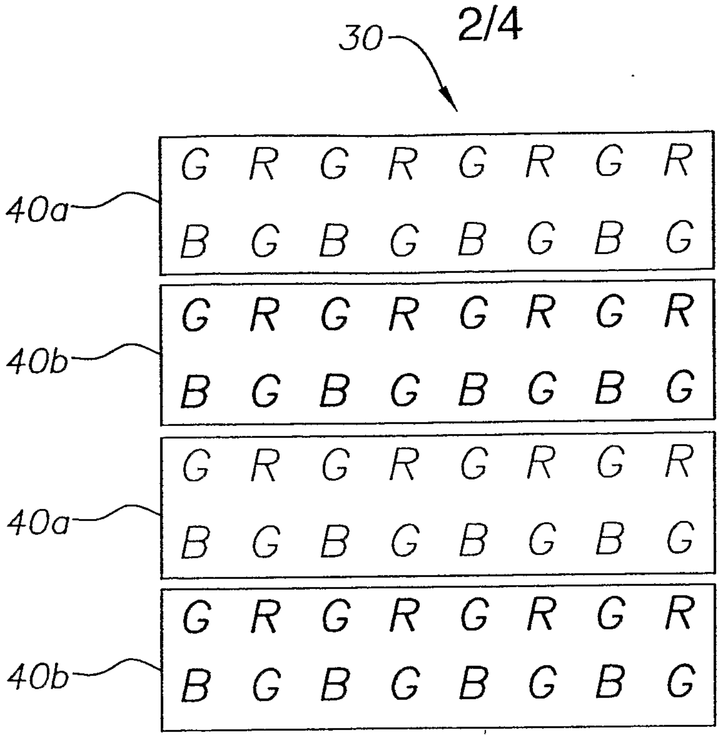

30
40a
40b
40a
40b
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 2a

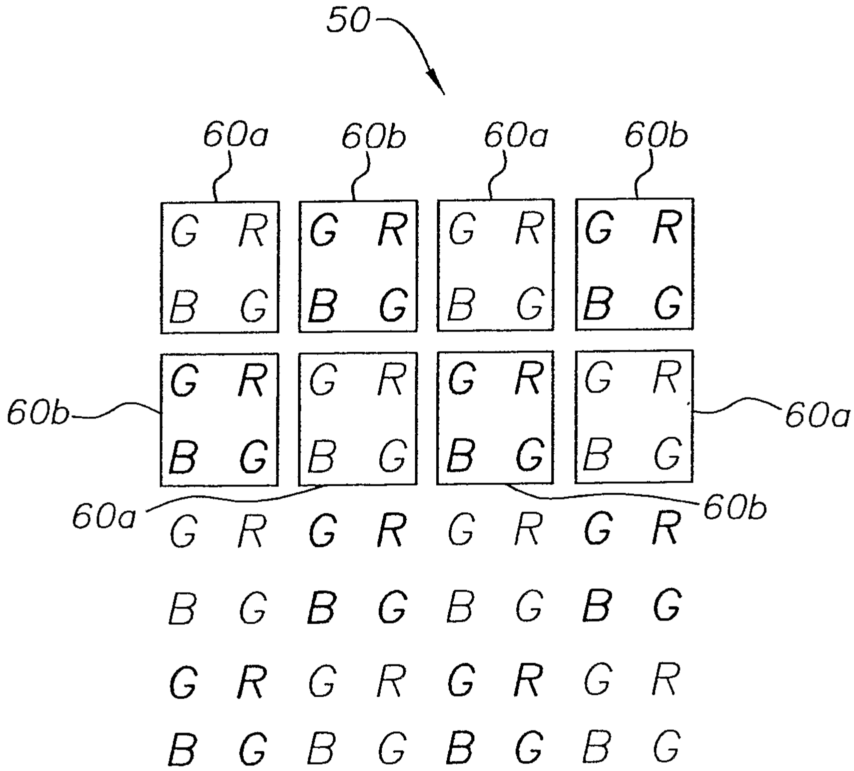

50
60a
60b
60a
60b
60b
60a
60a
60b
G R
B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 2b

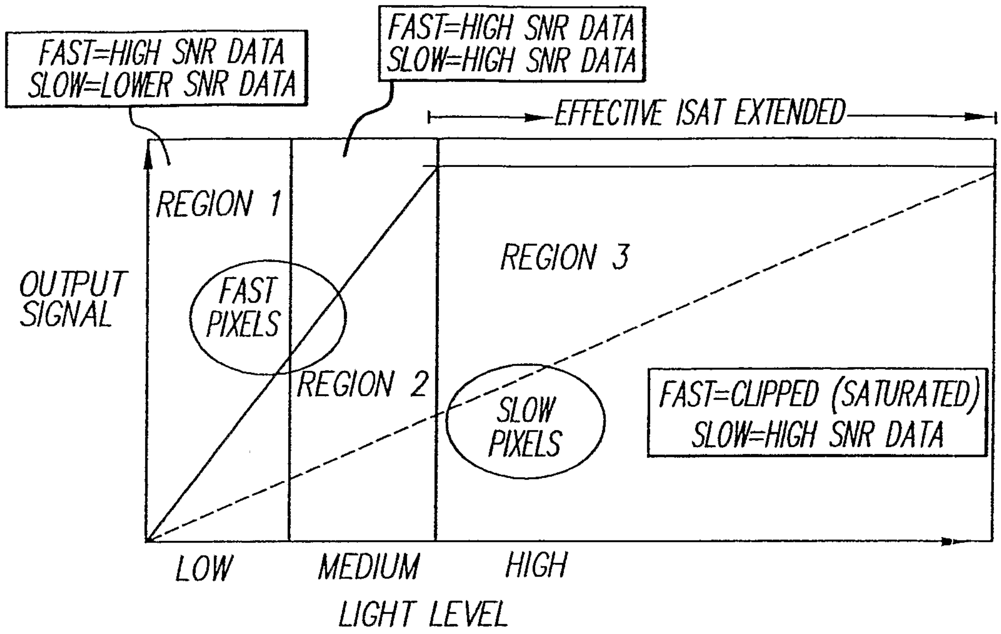

FAST=HIGH SNR DATA
SLOW=LOWER SNR DATA
FAST=HIGH SNR DATA
SLOW=HIGH SNR DATA
EFFECTIVE ISAT EXTENDED
REGION 1
OUTPUT SIGNAL
FAST PIXELS
REGION 3
REGION 2
SLOW PIXELS
FAST=CLIPPED (SATURATED)
SLOW=HIGH SNR DATA
LOW
MEDIUM
HIGH
LIGHT LEVEL

FIG. 3

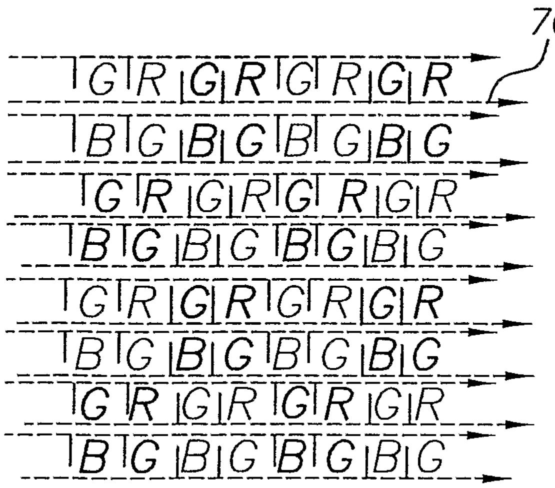

70
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 4a

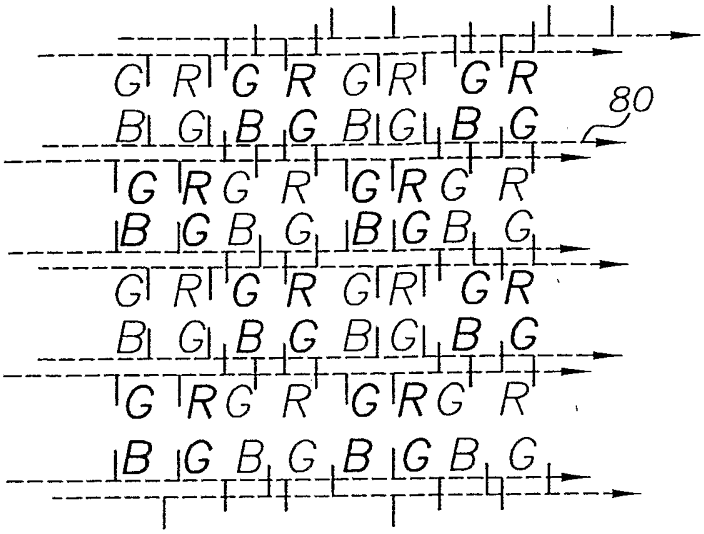

G R G R G R G R
B G B G B G B G
80
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G
G R G R G R G R
B G B G B G B G

FIG. 4b

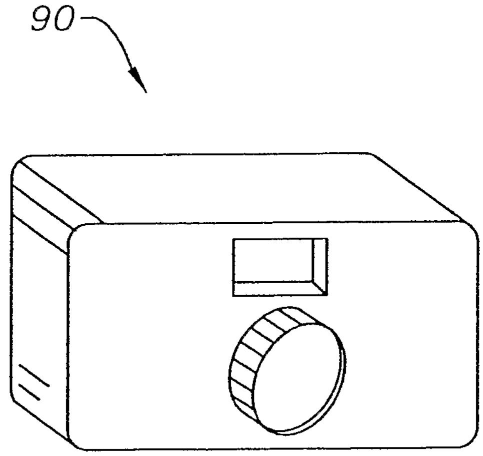

90

FIG. 5