(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 January 2015 (29.01.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/012958 A1

(51) International Patent Classification:
G06F 13/40 (2006.01) *H01P 3/02* (2006.01)
H01P 3/08 (2006.01)

(21) International Application Number:
PCT/US2014/040608

(22) International Filing Date:
3 June 2014 (03.06.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/947,328 22 July 2013 (22.07.2013) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: DIFFERENTIAL-TO-SINGLE-ENDED TRANSMISSION LINE INTERFACE

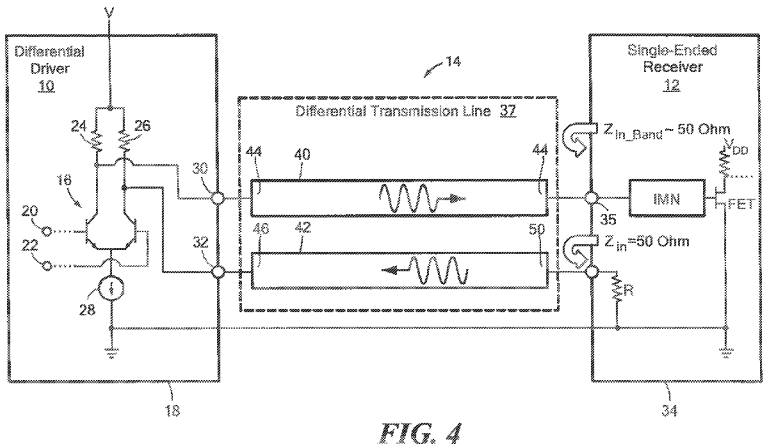

FIG. 4

(57) Abstract: An interface for connecting a differential signal circuit having a differential signal output and a reference potential terminal to an input of a single ended signal circuit and a reference potential terminal. The interface includes a differential transmission line having a pair of electromagnetically coupled microwave transmission lines having first ends connected to the differential signal output and second ends, one of the second ends being connected to the single ended circuit input and the other one of the second ends being coupled to the reference potential terminals of the differential signal circuit and the single ended signal circuit.

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Differential–to–Single-Ended Transmission Line Interface

TECHNICAL FIELD

[0001] This disclosure relates generally to differential –to-single ended transmission lines interfaces.

BACKGROUND

[0002] As is known in the art, single-ended data transmission uses only one signal line, with its voltage potential referred to ground. While the signal line provides the forward path for signal currents, ground provides the return current path. Single-ended interfaces benefit from their simplicity and their low implementation cost, but have three main drawbacks:

1) They are highly sensitive to noise pick-up, because noise induced into the signal or ground paths adds directly to the receiver input, thus causing false receiver triggering.

2) Another concern is crosstalk, which is the capacitive and inductive coupling between adjacent signal and control lines, particularly at higher frequencies. Further, due to the physical differences between the signal trace and the ground plane, the transversal electromagnetic waves (TEM) generated in single-ended systems can radiate into the circuit environment, thus representing a significant source of electromagnetic interference (EMI) to adjacent circuits.

[0003] As is known in the art, differential signaling uses a signal pair consisting of two conductors- one for the forward, the other for the return current to flow. Each signal conductor possesses a common-mode voltage, VCM, superimposed with SO percent of the differential-driver output VOD, but of opposite polarity to one another. When the conductors of a differential pair are close to each other, electrically coupled external noise induced into both conductors equally appears as common-mode noise at the receiver input. Receivers with differential inputs are sensitive to signal differences only, but immune to common-mode signals. The receiver, therefore, rejects common-mode noise and signal integrity is maintained. Close electric coupling provides another benefit. The currents in the two conductors, being of equal amplitude but opposite polarity, create magnetic fields that cancel each other. The TEM waves of the two conductors, now being robbed of their magnetic fields, cannot radiate into the environment. Only the far smaller

fringing fields outside the conductor loop can radiate, thus yielding significantly lower EMI.

[0004] As is also known in the art, it is sometimes necessary to connect differential signal circuit (such as a driver fabricated using, for example, a silicon-based technology) to single-ended circuit (a receiver such fabricated using III-V-based technology). Proper interface between the differential signal circuit and the single-ended circuit is critical to system performance, even more so in multi-chip modules with large distances between the chips.

[0005] One technique used to connect differential circuitry, such as a driver, to single ended circuitry, such as a receiver, is shown on FIG. 1. Here, a differential driver includes a pair of bipolar transistors formed on a silicon chip having collector electrodes providing a differential signal and emitter electrodes connected together and then to a reference potential, here ground, through a current source, as shown. One of the collector outputs is connected to one end of a single ended transmission line (TL) and the other collector is connected to the reference potential through a resistor, as shown. The other end of the single ended transmission line is connected to the input of a receiver. The receiver includes a Field Effect Transistor FET formed on a column III-V semiconductor chip. The FET has a gate electrode connected to the single ended transmission line through an input impedance matching network (IMN), as shown, an a source electrode connected to the reference potential, as shown. The disadvantages are: Cross-talk between adjacent TLs; Driver sensitivity to noise in bias lines ("ground bounce"); Additional TL loss due to radiation; and one-half of the signal is lost in the termination within the driver

[0006] Another interface uses a balun (passive balanced-to-unbalanced transformer) as shown in FIG. 2. Depending on where the balun is located (it could be on either of the two chips or as a separate component), the driver and receiver are connected through either a single-ended transmission line (TL) or a differential TL (Diff TL) or combination of the two. Disadvantages in using a balun are: There is some cross-talk between adjacent TL and radiation loss if single ended transmission line (S-E TL) is used; Balun loss and bandwidth limit; and Balun complexity and size (especially at low frequencies.

[0007] Yet, another interface uses an active converter, as shown in FIG. 3. Depending where the active converter is located (it could be on either of the two chips or as a separate component), the driver and receiver are connected through either a single-ended TL or a differential TL or combination of the two. Disadvantages: Some cross-talk between adjacent TL and radiation loss if single ended TL is used; The active converter's bandwidth limit and its DC power consumption of the DC voltage source.

SUMMARY

[0008] In accordance with the present disclosure, an interface is provided for connecting a differential signal circuit having a differential signal output and a reference potential terminal to an input of a single ended signal circuit and a reference potential terminal. The interface includes a differential transmission line comprising a pair of electromagnetically coupled microwave transmission lines having first ends connected to the differential signal output and second ends, one of the second ends being connected to the single ended circuit input and the other one of the second ends being coupled to the reference potential terminals.

[0009] In one embodiment, the differential transmission line comprises a pair of electromagnetically coupled microstrip transmission lines having a pair of strip conductors disposed over a common ground plane conductor.

[0010] In one embodiment, the differential transmission line comprises stripline structures having a pair of electromagnetically coupled strip conductors disposed between a pair of common ground plane conductors to form a pair of stripline transmission lines.

[0011] In one embodiment, the differential transmission line has a predetermined odd mode characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined odd mode characteristic impedance of the differential transmission line.

[0012] In one embodiment, an interface structure is provided for connecting a plurality differential signal circuits, each one having a differential signal output and a reference

potential terminal, to a plurality of single ended signal circuits, each one having an input and a reference potential terminal. The interface structure includes: a plurality of stacked differential transmission lines, each one of the differential transmission lines having a pair of electromagnetically coupled microwave stripline structures, each one of the strip line structures having a pair of strip conductors disposed in a plane between a pair of ground plane conductors to form a pair of stripline circuits for each one of the plurality of stacked stripline structures. The pair of strip conductors of each one of the stripline structures have first ends connected to the differential signal output of a corresponding one of the plurality of differential signal circuits and one of the second ends connected to the input of a corresponding one of the plurality of single ended circuits and the other one of the second ends coupled to the reference potential terminals of the plurality of differential signal circuits and the plurality of single ended signal circuits.

[0013] In one embodiment, portions of the pair of strip conductors of one of the stripline structures overlay portions of the pair of strip conductors of another one of the stripline structures.

[0014] The details of one or more embodiments of the disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the disclosure will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0015] FIG. 1 is a schematic circuit diagram of a differential signal circuit having a differential signal output connected to an input of a single ended signal circuit according to the PRIOR ART;

[0016] FIG. 2 is a schematic circuit diagram of a differential signal circuit having a differential signal output connected to an input of a single ended signal circuit according to the PRIOR ART;

[0017] FIG. 3 is a schematic circuit diagram of a differential signal circuit having a differential signal output connected to an input of a single ended signal circuit according to the PRIOR ART;

[0018] FIG. 4 is a schematic circuit diagram of a differential signal circuit having a differential signal output connected to an input of a single ended signal circuit according to the disclosure;

[0019] FIG. 5 is a diagrammatical sketch of the schematic circuit diagram of FIG. 4.

[0020] FIG. 5A is a diagrammatic sketch of a differential transmission line used in the circuit of FIG. 5;

[0021] FIG. 6 is a diagrammatical sketch of a schematic circuit diagram showing a plurality of differential signal circuits interconnected to a plurality single ended signal circuits according to the disclosure; and

[0022] FIG. 6A is a diagrammatic sketch of an exemplary one of a stack of a differential transmission lines used in the circuit of FIG. 6;

[0023] FIG. 7 is a cross sectional sketch of a portion of the diagrammatical sketch of FIG, 6 taken along line 7-7 in FIG. 6 according to another embodiment of the disclosure.

[0024] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0025] Referring now to FIG. 4, a differential signal circuit transmitter 10 is shown connected to a single ended signal circuit receiver 12 through an interface 14. More particular, the transmitter 10 includes a differential driver 16, here a differential amplifier having a pair of bipolar transistors T1, T2 formed on a silicon substrate 18. The transistors T1, T2 have an input signal fed to the base electrodes thereof via input terminals 20, 22. The collectors are connected to a voltage source V through resistors 24, 26, as shown. The emitter electrodes are connected together and then to a reference potential, here ground,

through a current source 28, as shown. It is noted that each one of the collectors is connected to a corresponding one of a pair of output terminals 30, 32, as shown and thereby produce a differential signal output between the output terminals 30, 32.

[0026] The receiver 12 includes a field effect transistor FET having a gate electrode connected to the interface 14 through an impedance matching network (IMN), as shown. Here the FET and is formed on a column III-V substrate 34, as shown. The drain electrode is coupled to a voltage source VDD and the source electrode is connected to a reference potential, here ground as shown. The receiver 12 is a single ended signal circuit having a single input 35.

[0027] The interface 14 includes a differential transmission line 37 having a pair of electromagnetically coupled strip conductors 40, 42 having first ends 44, 46 connected to the differential signal output (output terminal 30, 32) and second ends 48, 50, one of the second ends 48 being connected to the single ended circuit input 35 and the other one of the second ends 50 being connected to the reference potential terminals of the differential signal circuit and the single ended signal circuit, here ground; it being noted that the second end 50 is coupled to ground though a resistor R also formed on the column III-V substrate 34, as shown.

[0028] More particularly, referring also to FIG. 5, the pair of strip conductors 40, 42 is disposed over a common ground plane conductor 64. Still more particularly, the strip conductors 40, 42 are disposed on one surface of a dielectric substrate 66 and the ground plane conductor 64 is deposed on the opposite surface of the dielectric substrate 66.

[0029] It is noted that the differential transmission line 37 has a predetermined odd mode characteristic impedance. The odd mode characteristic impedance is the characteristic impedance of a single transmission line when the two strip conductors 40, 42 in the differential transmission line are driven differentially (with signals of the same amplitude and opposite polarity). Thus, referring also to FIG. 5A, the differential transmission line 37 is made up of two microstrip transmission lines, 60, 62. One of the two microstrip transmission lines includes strip conductor 40 and the portion of the ground plane conduction under the strip conductor 40. Thus, there is an electric field between the strip

conductor 40 and the portion of the ground plane conduction under the strip conductor 40 as indicated by the arrows in FIG. 5A. The other one of the two microstrip transmission lines includes strip conductor 42 and the portion of the ground plane conduction under the strip conductor 42. Thus, there is an electric field between the strip conductor 40 and the portion of the ground plane conduction under the strip conductor 40 as indicated by the arrows in FIG. 5A. It is noted that the two strip conductors 40, 40 are proximate each other such that an electric field exists between the two strip conductors 40, 42 as indicated by the arrows in FIG. 5A. Thus, the differential transmission line 37 comprises a pair of electromagnetically coupled microwave transmission lines 60, 62.

[0030] The impedance between the input terminal 30 and the input terminal 32, that is, the odd mode characteristic impedance of the differential transmission line 37, is here, for example, 50 ohms. Thus, the IMN is designed to provide an input impedance into the input terminal 35 matched to the predetermined odd mode characteristic impedance of the differential transmission line 37, here, for example, 50 ohms. Likewise, the resistor R is designed to provide an input impedance matched to the predetermined odd mode characteristic impedance of the differential transmission line 37, here, for example, 50 ohms.

[0031] Referring now to FIG. 6 an interface structure 70 is shown for connecting a plurality of, here for illustration three, differential signal circuit transmitters differential signal circuits, 10a-10c, each one having a differential signal output and a reference potential terminal, to a corresponding plurality of single ended signal circuits 12a-12c, each one having an input and a reference potential terminal.

[0032] The interface structure 70 includes: a plurality of, here three, stacked differential transmission lines, 37a, 37b and 37c (FIG. 7), each comprising a pair of electromagnetically coupled microwave transmission lines, here stripline structures 14a-14c, each one of the stripline structures 14a-14c having a pair of strip conductors 40a, 42a-40c, 42c, respectively, as shown, disposed in a plane between a pair of ground plane conductors 64a-64d to form a pair of stripline circuits for each one of the plurality of stacked stripline structures 14a-14c. The pair of strip conductors 40a, 42a of stripline structures 14a have first ends connected to the transmitters differential signal circuits 10a

and one of the second ends connected to the input of single ended signal circuit 12a and the other one of the second ends connected to the reference potential terminals of the plurality of differential signal circuits and the plurality of single ended signal circuits through a matching resistor Ra, as indicated. The pair of strip conductors 40b, 42b of stripline structures 14b have first ends connected to the transmitters differential signal circuits 10b and one of the second ends connected to the input of single ended signal circuit 12b and the other one of the second ends connected to the reference potential terminals of the plurality of differential signal circuits and the plurality of single ended signal circuits through a matching resistor Rb, as indicated. In like manner, The pair of strip conductors 40c, 42c of stripline structures 14c have first ends connected to the transmitters differential signal circuits 10c and one of the second ends connected to the input of single ended signal circuit 12a and the other one of the second ends connected to the reference potential terminals of the plurality of differential signal circuits and the plurality of single ended signal circuits through a matching resistor Rc, as indicated. It is noted that portions of the pair of strip conductors of one of the stripline structures overlay portions of the pair of strip conductors of another one of the stripline structures.

[0033] More particularly, and referring also to FIG. 7, the stripline structures 14a-14c each includes a pair of dielectric boards $74a_1$, $74a_2$ - $74c_1$, $74c_2$, as shown. Dielectric board $74a_1$ has a ground plane conductor 64a on its bottom surface and dielectric board $74a_2$ has a ground plane conductor 64b on its upper surface. Disposed between the upper surface of the dielectric board $74a_1$ and the lower surface of the dielectric board $74a_2$ are the pair of strip conductors 40c and 42c. Dielectric board $74b_1$ has the ground plane conductor 64b on its lower surface and dielectric board $74b_2$ has a ground plane conductor 64c on its upper surface. Disposed between the upper surface of the dielectric board $74b_1$ and the lower surface of the dielectric board $74b_2$ are the pair of strip conductors 40b and 42b.

[0034] In like manner, dielectric board $74c_1$ has a ground plane conductor 64c on its bottom surface and dielectric board $74c_2$ has a ground plane conductor 64d on its upper surface. Disposed between the upper surface of the dielectric board $74c_1$ and the lower surface of the dielectric board $74c_2$ are the pair of strip conductors 40a and 42a.

[0035] Thus, the ground plane conductors 64b and 64c provide electrical isolation between the, stacked differential transmission lines, 37a, 37b and 37c.

[0036] Here again, referring to FIGS. 6 and 7, each one of the stacked differential transmission lines 37a, 37b and 37c has a predetermined odd mode characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined odd-mode characteristic impedance of such one of the stacked differential transmission lines 37a, 37b and 37c. The impedance matching circuit includes a resistor Ra, Rb and Rc. Here, for example, the odd mode impedance of each one of the differential transmission lines is 50 ohms.

[0037] As shown in FIG. 6A for an exemplary of the stacked differential transmission lines, here differential transmission line 37a has a pair of transmission lines 60a, 62a with the strip conductors 40a, 42a having an electric field coupled between them as shown in FIG. 6A, and with an electric field coupled between the strip conductors 40a, 42a and the pair of ground plane conductors 64b, 64c, as shown by the arrows in FIG. 6A.

[0038] It is noted that the connections between the strip conductors 40a, 42a-40c, 42c and the differential signal circuit transmitter 10a-10c and single ended signal circuit receiver 12a-12c are made through vertically extending conductive vias 76 which pass through the dielectric boards and are electrically insulated by the dielectric boards $74a_1$, $74a_2$ - $74c_1$, $74c_2$, from the ground plane conductors 64a-64d.

[0039] It is also noted that the bottom surface of the differential signal circuit transmitters differential signal circuits, 10a-10c, and the bottom surface of the single ended signal circuits 12a-12c have ground plane conductors 64a-64d which are electrically connected to the ground plane conductors of the interface structure. Also, the ground of the circuits are all electrically interconnected.

[0040] It should now be appreciated an interface for connecting a differential signal circuit having a differential signal output and a reference potential terminal to an input of a single ended signal circuit and a reference potential terminal according to the disclosure includes

a differential transmission line comprising a pair of electromagnetically coupled microwave transmission lines having first ends connected to the differential signal output and second ends, one of the second ends being connected to the single ended circuit input and the other one of the second ends being coupled to the reference potential terminals. The interface can include one or more of the following features independently or in combination with another feature including: wherein the differential transmission line includes a pair of electromagnetically coupled microwave transmission lines comprises microstrip transmission lines having a pair of strip conductors disposed over a common ground plane conductor; wherein the pair of microwave transmission lines comprises the electromagnetically coupled pair of microwave transmission lines comprises stripline structures having a pair of strip conductors disposed between a pair of common ground plane conductors to form a pair of stripline circuits; wherein the differential transmission line has a predetermined odd mode characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined characteristic odd mode impedance of the differential transmission line; wherein the impedance matching circuit includes a resistor; wherein the differential transmission line has a predetermined odd mode characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined odd mode characteristic impedance of the differential transmission line.

[0041] It should now also be appreciated an interface structure for connecting a plurality differential signal circuits, each one having a differential signal output and a reference potential terminal, to a plurality of single ended signal circuits, each one having an input and a reference potential terminal according to the disclosure includes: a plurality of stacked differential transmission lines, each one of the differential transmission line comprising a microwave stripline structure, each stripline structure having a pair of electromagnetically coupled strip conductors disposed in a plane between a pair of ground plane conductors to form a pair of stripline circuits for each one of the plurality of stacked differential transmission lines; wherein the pair of strip conductors of each one of the stripline structures have first ends connected to the differential signal output of a corresponding one of the plurality of differential signal circuits and one of the second ends

connected to the input of a corresponding one of the plurality of single ended circuits and the other one of the second ends coupled to the reference potential terminals of the plurality of differential signal circuits and the plurality of single ended signal circuits. The interface structure can include one or more of the following features independently or in combination with another feature including: wherein portions of the pair of strip conductors of one of the stripline structures overlay portions of the pair of strip conductors of another one of the stripline structures; wherein each one of the differential transmission lines has an odd mode predetermined characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined odd mode characteristic impedance of such one of the differential transmission line; wherein the impedance matching circuit includes a resistor.

[0042] A number of embodiments of the disclosure have been described. For example, other types of differential transmission lines may be used such as coaxial transmission lines where the coaxial transmission line includes a pair of electromagnetically coupled conductors. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the disclosure. Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. An interface for connecting a differential signal circuit having a differential signal output and a reference potential terminal to an input of a single ended signal circuit and a reference potential terminal, comprising:

a differential transmission line comprising a pair of electromagnetically coupled microwave transmission lines having first ends connected to the differential signal output and second ends, one of the second ends being connected to the single ended circuit input and the other one of the second ends being coupled to the reference potential terminals.

2. The interface recited in claim 1 wherein the differential transmission line includes a pair of electromagnetically coupled microwave transmission lines comprises microstrip transmission lines having a pair of strip conductors disposed over a common ground plane conductor.

3. The interface recited in claim 1 wherein the pair of microwave transmission lines comprises the electromagnetically coupled pair of microwave transmission lines comprises stripline structures having a pair of strip conductors disposed between a pair of common ground plane conductors to form a pair of stripline circuits.

4. The interface recited in claim 1 the differential transmission line has a predetermined odd mode characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined characteristic odd mode impedance of the differential transmission line.

5. The interface recited in claim 4 wherein the impedance matching circuit includes a resistor.

6. The interface recited in claim 2 wherein the differential transmission line has a predetermined odd mode characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance

matching circuit having an impedance matched to the predetermined odd mode characteristic impedance of the differential transmission line.

7. The interface recited in claim 6 wherein the impedance matching circuit includes a resistor.

8. The interface recited in claim 3 wherein the differential transmission line has a predetermined odd mode characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined odd mode characteristic impedance of the differential transmission line.

9. The interface recited in claim 8 wherein the impedance matching circuit includes a resistor.

10. An interface structure for connecting a plurality differential signal circuits, each one having a differential signal output and a reference potential terminal, to a plurality of single ended signal circuits, each one having an input and a reference potential terminal, comprising:

a plurality of stacked differential transmission lines, each one of the differential transmission line comprising a microwave stripline structure, each stripline structure having a pair of electromagnetically coupled strip conductors disposed in a plane between a pair of ground plane conductors to form a pair of stripline circuits for each one of the plurality of stacked differential transmission lines;

wherein the pair of strip conductors of each one of the stripline structures have first ends connected to the differential signal output of a corresponding one of the plurality of differential signal circuits and one of the second ends connected to the input of a corresponding one of the plurality of single ended circuits and the other one of the second ends coupled to the reference potential terminals of the plurality of differential signal circuits and the plurality of single ended signal circuits.

11. The interface structure recited in claim 10 wherein portions of the pair of strip conductors of one of the stripline structures overlay portions of the pair of strip conductors of another one of the stripline structures.

12. The interface recited in claim 11 wherein each one of the differential transmission lines has an odd mode predetermined characteristic impedance and wherein said other one of the second ends is connected to the reference potential terminals through an impedance matching circuit having an impedance matched to the predetermined odd mode characteristic impedance of such one of the differential transmission line.

13. The interface recited in claim 12 wherein the impedance matching circuit includes a resistor.

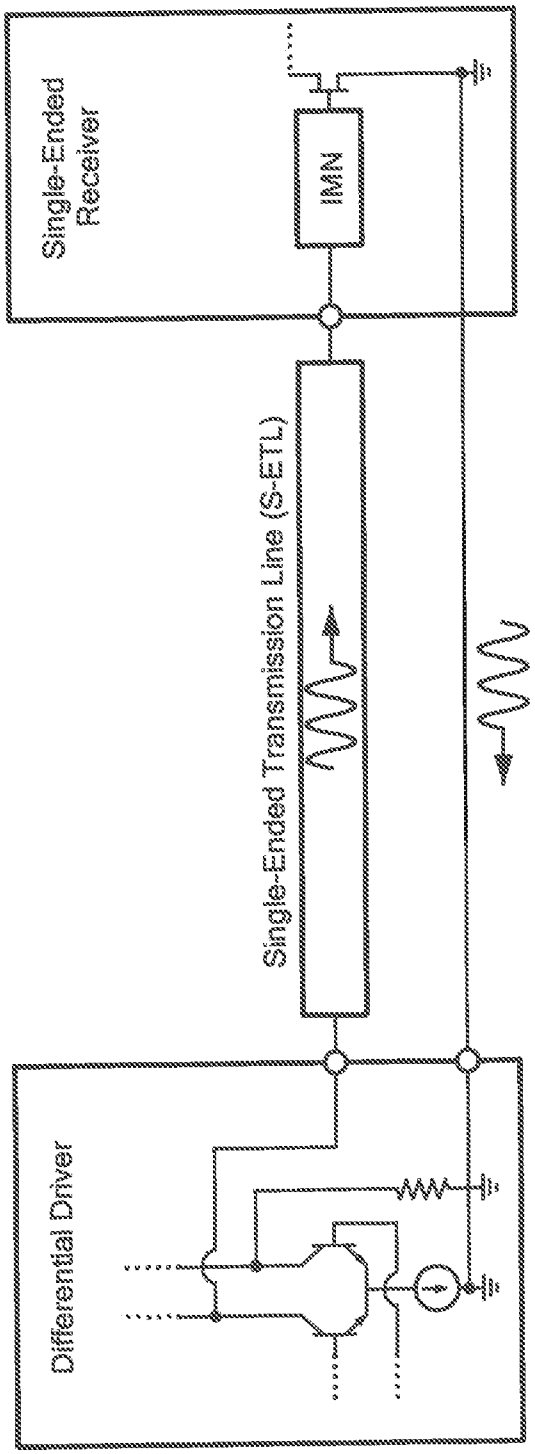

FIG. 1
PRIOR ART

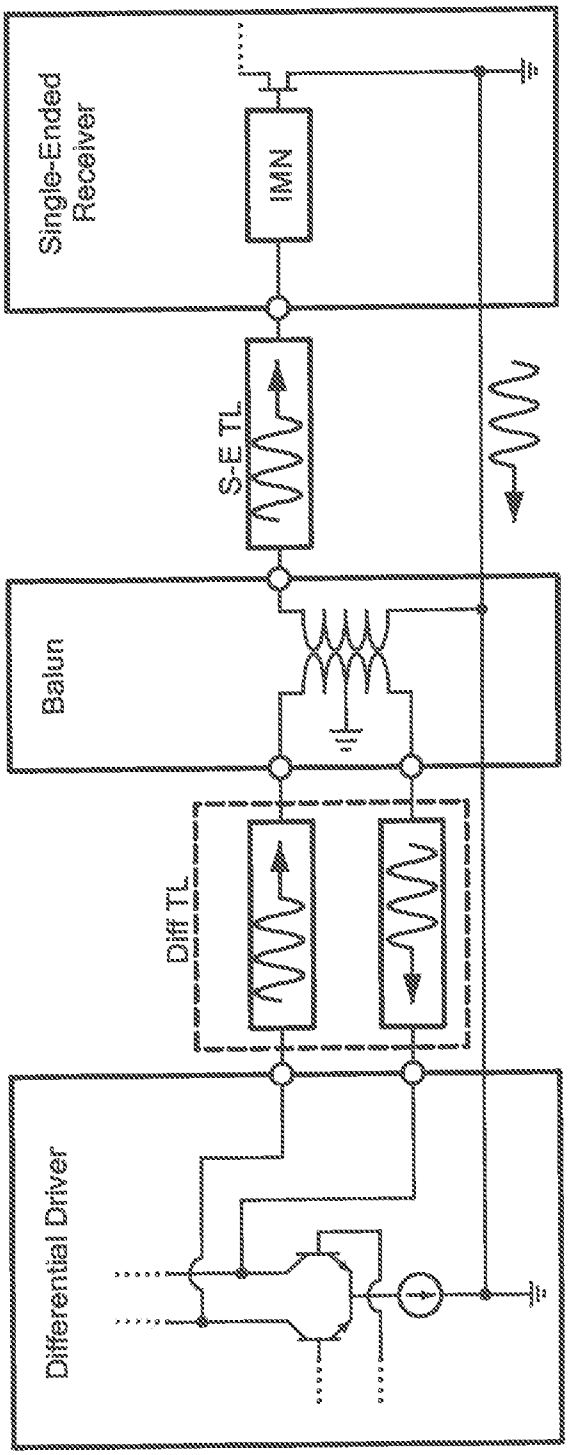

FIG. 2
PRIOR ART

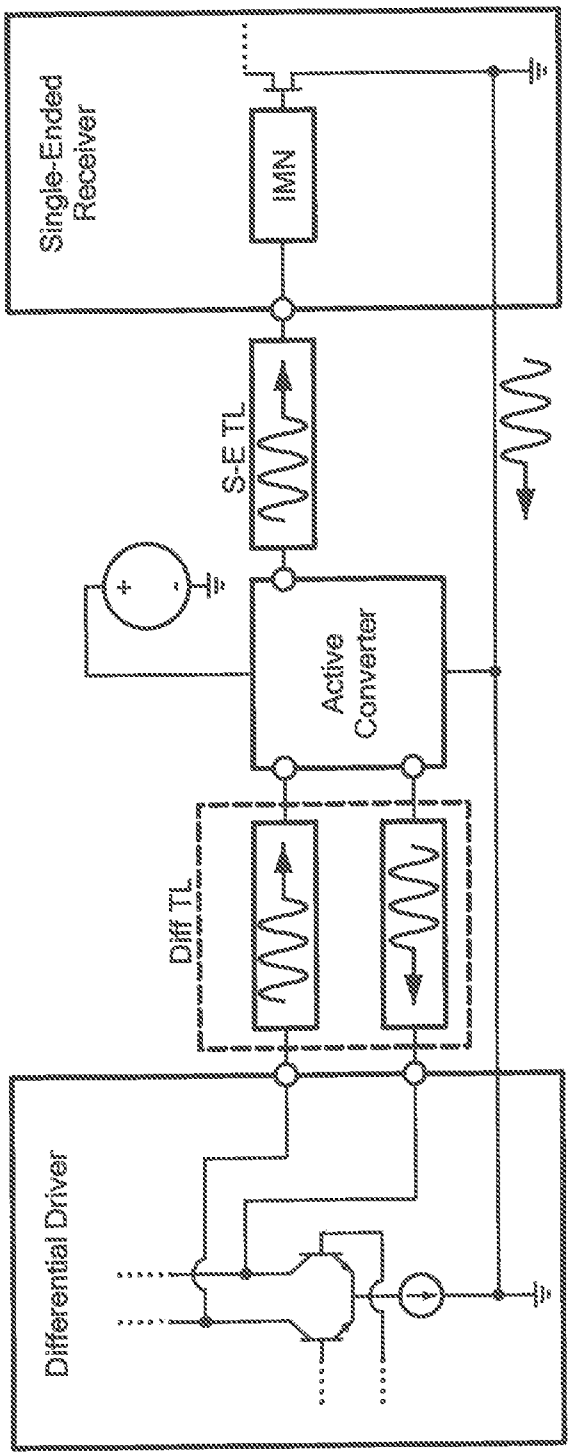

FIG. 3

PRIOR ART

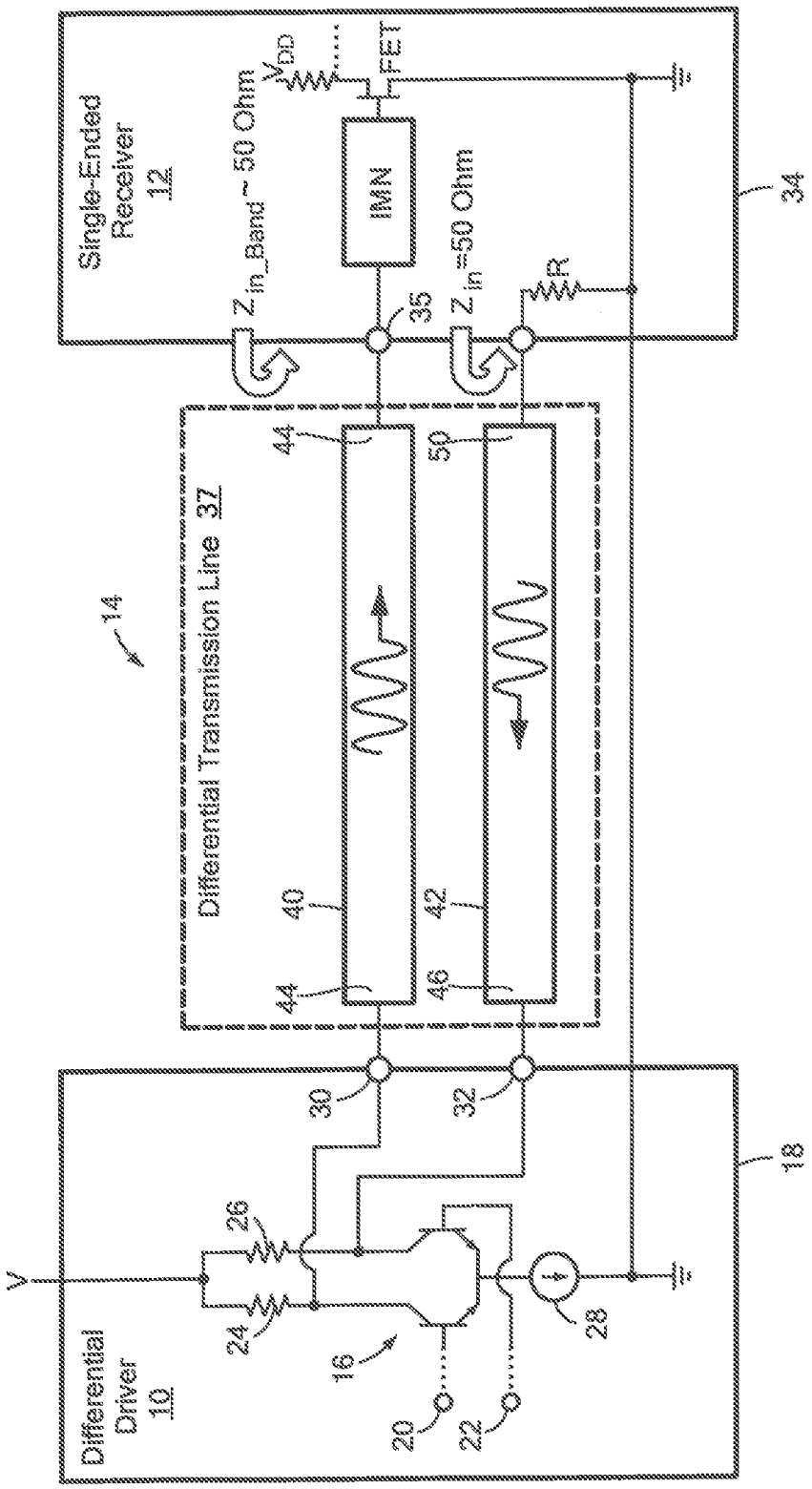
Single-Ended Receiver 12
V_{DD}
FET
IMN
Z_{in_Band} ~ 50 Ohm
Z_{in}=50 Ohm
R
35
34
14
Differential Transmission Line 37
44
50
40
42
44
46
30
32
18
26
24
16
20
22
28
V
Differential Driver 10

FIG. 4

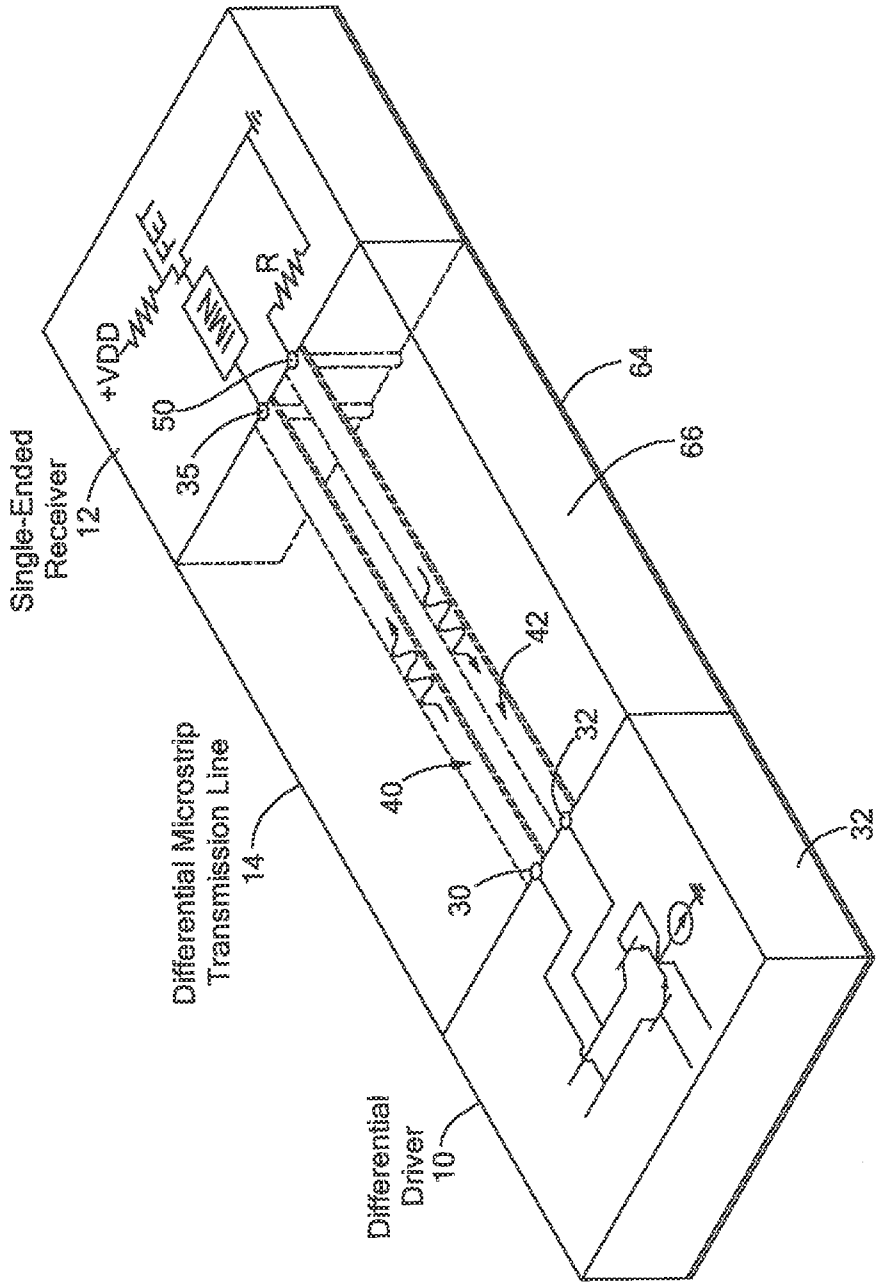
Single-Ended Receiver
12
Differential Microstrip Transmission Line
14
Differential Driver
10
+VDD
50
35
R
64
66
42
40
32
30
32

FIG. 5

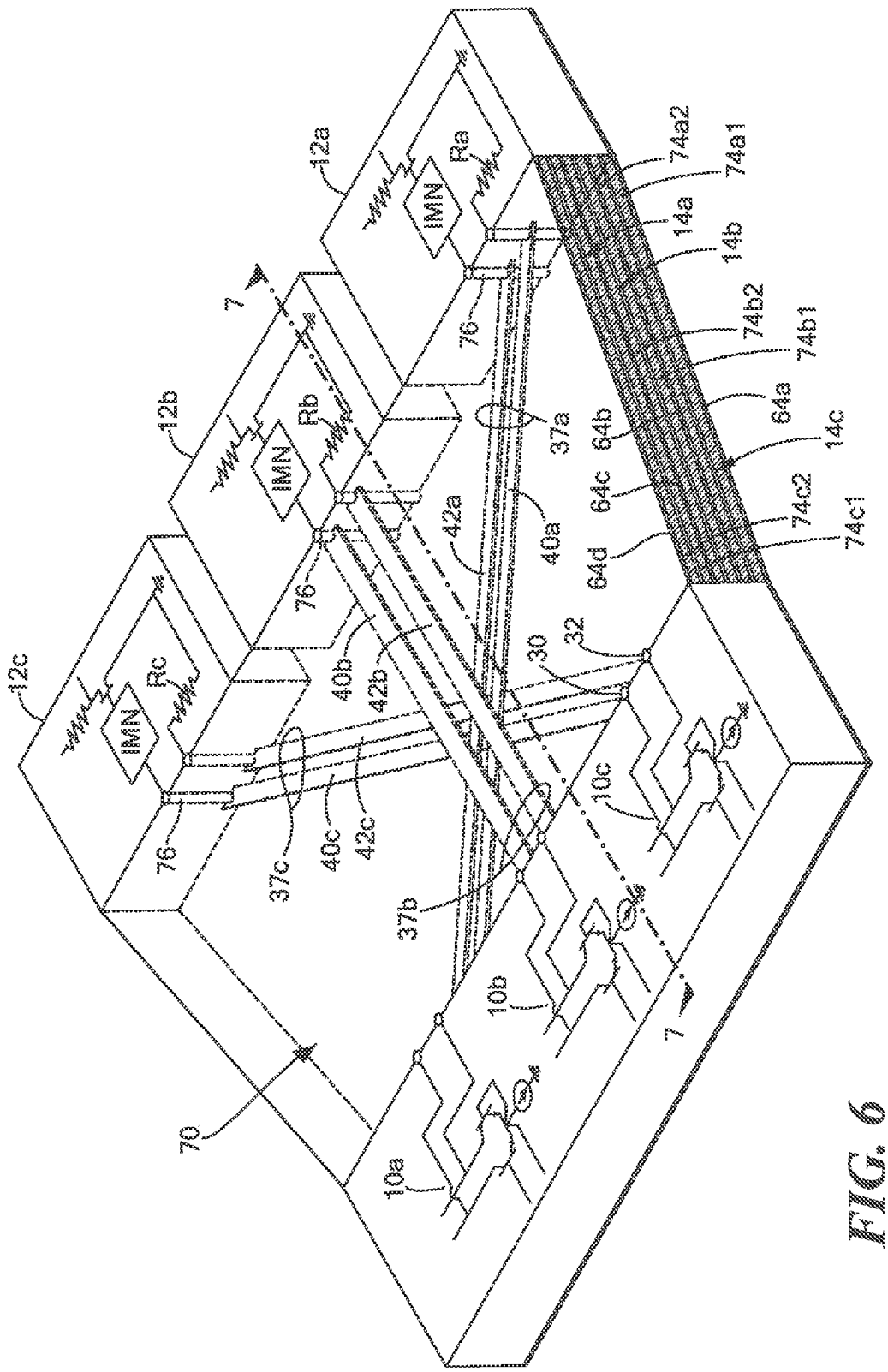
12a
12b
12c
IMN
Ra
Rb
Rc
7
76
74a2
74a1
14a
14b
74b2
74b1
64a
64b
14c
64c
64d
74c2
74c1
37a
40a
42a
40b
42b
30
32
37c
40c
42c
37b
10c
10b
10a
70

FIG. 6

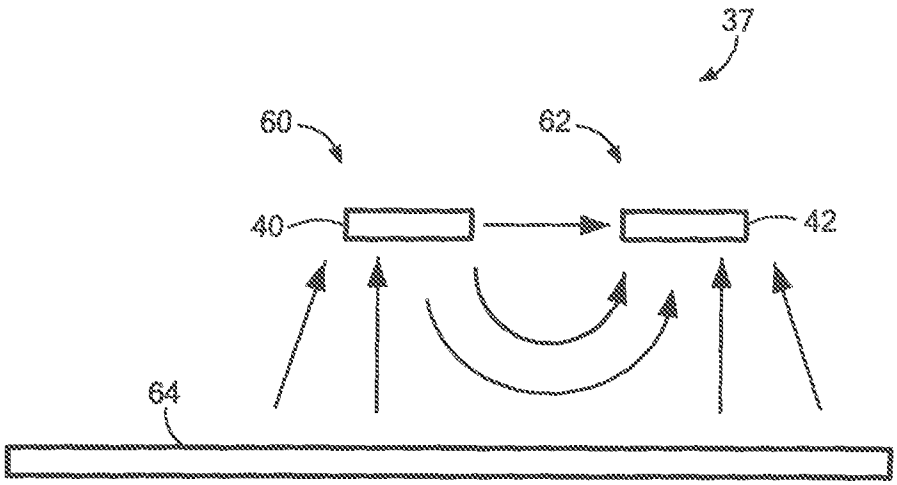

FIG. 5A

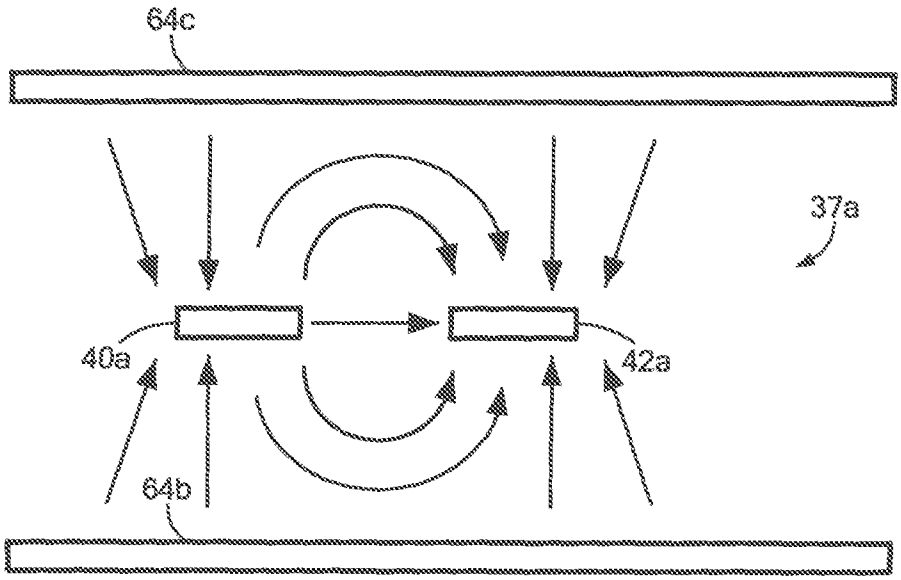

FIG. 6A

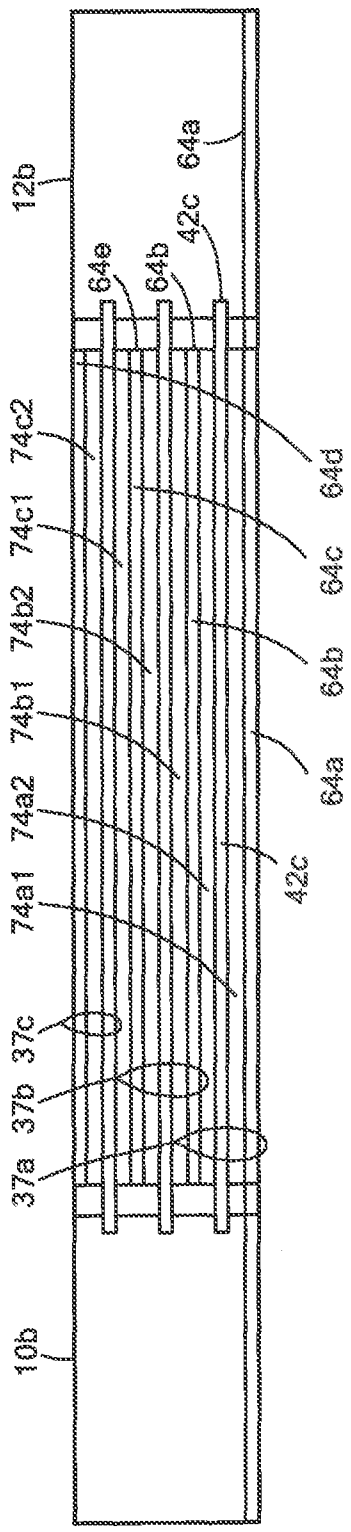
12b
64a
42c
64e
64b
74c2
64d
74c1
64c
74b2
64b
74b1
64a
74a2
42c
74a1
37c
37b
37a
10b

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/040608

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/40 H01P3/08 H01P3/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01P G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/259337 A1 (TABATABAI MOHAMMAD [US]) 14 October 2010 (2010-10-14) paragraphs [0018], [0023] - [0025]; figures 4,5	1-13
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A	US 2009/295481 A1 (LIN INN-FU [TW] ET AL) 3 December 2009 (2009-12-03) abstract	1-13

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 August 2014	25/08/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jünger, Bernhard

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/040608

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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