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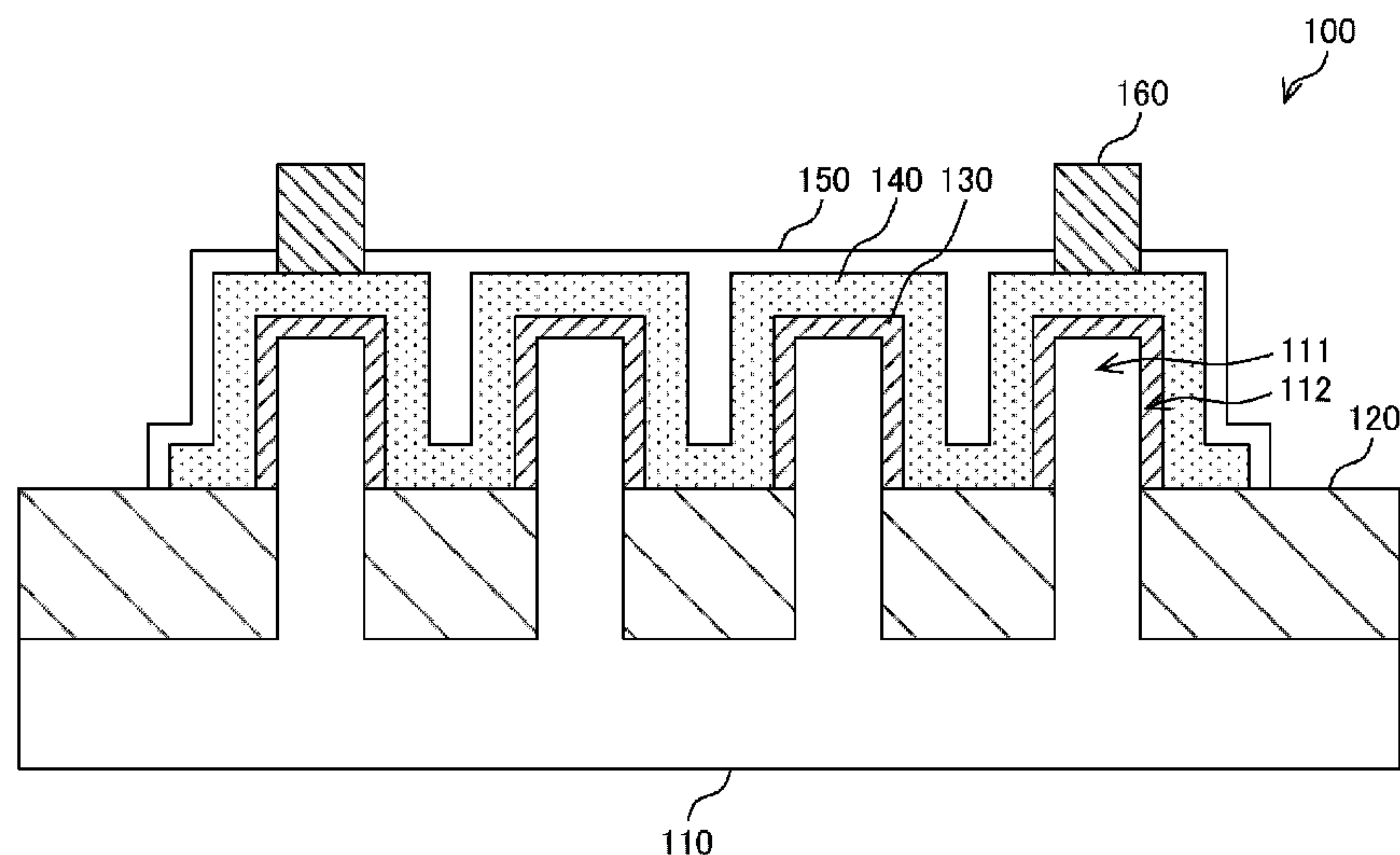
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(54) Title: RESISTANCE ELEMENT AND ELECTRONIC DEVICE



(57) Abstract: A resistance element includes a resistive film, in which the resistive film is adjacent to a protrusion formed on a surface of a semiconductor substrate, the protrusion including a step traversed by the resistive film.

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Description

Title of Invention: RESISTANCE ELEMENT AND ELECTRONIC DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

- [0001] This application claims the benefit of Japanese Priority Patent Application JP 2019-198096 filed on October 31, 2019, the entire contents of which are incorporated herein by reference.

Technical Field

- [0002] The present disclosure relates to a resistance element and an electronic device. Specifically, the present disclosure relates to a resistance element formed on a semiconductor substrate and an electronic device including the resistance element.

Background Art

- [0003] In the past, passive elements formed by processing a surface of a semiconductor substrate are employed. For example, a resistance element in which a polycrystalline silicon film included in a resistor is placed in a trench formed in a semiconductor substrate is employed (for example, see PTL 1). In this resistance element, an n-type first polycrystalline silicon film, a silicon oxide film, and a p-type second polycrystalline silicon film are laminated in this order inside the trench.

Citation List

Patent Literature

- [0004] PTL 1: JP 11-330375 A

Summary

Technical Problem

- [0005] The technique in the related art has a difficulty in manufacturing a resistance element with a high resistance value. Reduction of a resistor in volume is necessary to enable a high resistance value. In the structure described in the foregoing technique, a plurality of films is laminated inside the trench formed in the semiconductor substrate. Accordingly, there is a limit in reducing the volume of the resistor, which makes it difficult to manufacture a resistance element with a high resistance value. On the other hand, in a case where a resistor with a long resistance pattern is formed to yield a resistance element with a high resistance value, there is a problem that an area occupied by the resistance element increases.

Solution to Problem

- [0006] The present disclosure has been made to solve the problems. According to a first aspect of the present disclosure, there is provided a resistance element including a

resistive film, in which the resistive film is adjacent to a protrusion formed on a surface of a semiconductor substrate, the protrusion including a step traversed by the resistive film.

- [0007] In addition, in the first aspect, the resistance element may include a plurality of the resistive films connected in series.
- [0008] Furthermore, in the first aspect, the plurality of the resistive films traversing the step of each of a plurality of the protrusions on the semiconductor substrate may be connected in series.
- [0009] Still further, in the first aspect, the resistance element may further include a protective film placed between the plurality of resistive films connected in series between the plurality of protrusions.
- [0010] Still further, in the first aspect, two adjacent protrusions of the plurality of protrusions may be placed at an interval exceeding twice a thickness of the resistive film.
- [0011] Still further, in the first aspect, the resistive film may be adjacent to the protrusion via an insulating film.
- [0012] Still further, in the first aspect, the resistance element may further include an insulating layer placed on the surface of the semiconductor substrate adjacent to the protrusion, in which the resistive film traverses a step between the insulating layer and the protrusion.
- [0013] Still further, in the first aspect, the protrusion may have a height of about 400 nm or less from the insulating layer.
- [0014] Still further, in the first aspect, the resistive film may include polycrystalline silicon.
- [0015] Still further, in the first aspect, the protrusion may be formed by grinding a surface of the semiconductor substrate around the protrusion.
- [0016] Still further, in the first aspect, the protrusion may be formed simultaneously with a fin of a fin transistor placed on the semiconductor substrate.
- [0017] In addition, according to a second aspect of the present disclosure, there is provided an electronic device including: a resistance element including a resistive film adjacent to a protrusion formed on a surface of a semiconductor substrate, the protrusion including a step traversed by the resistive film; and a transistor placed on the semiconductor substrate and connected to the resistance element.
- [0018] According to the above aspects, a resistive film is adjacent to a side surface of a protrusion. Such a configuration makes it possible to elongate the resistive film.

Brief Description of Drawings

- [0019] [fig.1]Fig. 1 is a view of a configuration example of a resistance element according to a first embodiment of the present disclosure.
- [fig.2]Fig. 2 is a cross-sectional view of the configuration example of the resistance

element according to the first embodiment of the present disclosure.

[fig.3A]Fig. 3A shows an example of a method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.3B]Fig. 3B shows an example of a method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.3C]Fig. 3C shows an example of a method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.4D]Fig. 4D shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.4E]Fig. 4E shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.4F]Fig. 4F shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.4G]Fig. 4G shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.5H]Fig. 5H shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.5I]Fig. 5I shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.5J]Fig. 5J shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.6K]Fig. 6K shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.6L]Fig. 6L shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.6M]Fig. 6M shows the example of the method for manufacturing the resistance element according to the first embodiment of the present disclosure.

[fig.7A]Fig. 7A is a view of other configuration example of the resistance element according to the first embodiment of the present disclosure.

[fig.7B]Fig. 7B is a view of other configuration example of the resistance element according to the first embodiment of the present disclosure.

[fig.7C]Fig. 7C is a view of other configuration example of the resistance element according to the first embodiment of the present disclosure.

[fig.8]Fig. 8 is a cross-sectional view of a configuration example of a resistance element according to a second embodiment of the present disclosure.

[fig.9]Fig. 9 is a cross-sectional view of a configuration example of a resistance element according to a third embodiment of the present disclosure.

[fig.10]Fig. 10 is a cross-sectional view of a configuration example of a resistance

element according to a fourth embodiment of the present disclosure.

[fig.11]Fig. 11 is a view of a configuration example of an electronic device according to a fifth embodiment of the present disclosure.

[fig.12]Fig. 12 is a perspective view of the configuration example of the electronic device according to the fifth embodiment of the present disclosure.

[fig.13]Fig. 13 is a perspective view of another configuration example of the electronic device according to the fifth embodiment of the present disclosure.

Description of Embodiments

[0020] Next, an embodiment for implementing the present disclosure (hereinafter, referred to as “embodiment”) will be described with reference to the drawings. In the drawings, the same or similar parts are denoted by the same or similar reference numerals. Furthermore, an embodiment will be described in the following order.

1. First embodiment
2. Second embodiment
3. Third embodiment
4. Fourth embodiment
5. Fifth embodiment

[0021] <1. First Embodiment>

(Configuration of resistance element)

Fig. 1 is a view of a configuration example of a resistance element according to a first embodiment of the present disclosure. Fig. 1 is a plan view of a configuration example of a resistance element 100. The resistance element 100 is formed on a semiconductor substrate 110 (not shown) that has a surface provided with an insulating layer 120. The semiconductor substrate 110 includes protrusions 111, and a resistive film 140 is adjacent to the protrusions 111. In the example shown in Fig 1, the resistance element 100 is provided with four protrusions 111 traversed by the resistive film 140.

[0022] (Cross-sectional configuration of resistance element)

Fig. 2 is a cross-sectional view of the configuration example of the resistance element according to the first embodiment of the present disclosure. Fig. 2 is a cross-sectional view of the configuration example of the resistance element 100 taken along line a-a' in Fig. 1. The resistance element 100 shown in Fig. 2 is formed on the surface of the semiconductor substrate 110, including the resistive film 140, an insulating film 130, a protective film 150, an insulating layer 120, and a contact plug 160.

[0023] The semiconductor substrate 110 is provided with the resistance element 100. The semiconductor substrate 110 includes, for example, silicon (Si). The semiconductor substrate 110 has n-type or p-type conductivity. Furthermore, the semiconductor

substrate 110 may include a well region with a low impurity concentration. Still further, the semiconductor substrate 110 may include an intrinsic semiconductor.

- [0024] The resistive film 140 is a film-shaped resistor including a resistive material having predetermined resistivity. The resistive film 140 is adjacent to the protrusions 111 which are to be described. Each protrusion 111 has a step 112 traversed by the resistive film 140. The semiconductor substrate 110 in Fig. 2 is provided with a plurality of protrusions 111 having the steps 112 traversed by the resistive film 140. The resistive film 140 traversing the steps 112 increases an effective length of the resistive film 140 and increases a resistance of the resistive film 140. The resistive film 140 includes, for example, polycrystalline silicon and the like. When polycrystalline silicon is used in the resistive film 140, it is possible to adjust the resistivity by implantation of impurities such as boron (B) and phosphorus (P). Furthermore, a metal such as tantalum (Ta) and a compound such as titanium nitride (TiN) are also employable as the resistive film 140.
- [0025] Four protrusions 111 are shown in Fig. 2, but note that the number of protrusions 111 is not limited. The resistive film 140 in Fig. 2 is an example in which the resistive film placed on each of a plurality of steps 112 is connected in series.
- [0026] The protrusions 111 are regions having a protruding shape formed on the surface of the semiconductor substrate 110. Each protrusion 111 includes the same member as the semiconductor substrate 110. Each protrusion 111 is formed, for example, by grinding the surface of the semiconductor substrate 110 around a region where the protrusion 111 is to be placed.
- [0027] The insulating layer 120 is placed on the surface of the semiconductor substrate 110. This insulating layer 120 is placed on the surface of the semiconductor substrate 110 excluding the protrusions 111. The protrusions 111 protrude from the insulating layer 120. The insulating layer 120 may include an insulator such as silicon oxide (SiO₂) and silicon nitride (SiN). The insulating layer 120 separates the resistive film 140 from the surface of the semiconductor substrate 110 excluding the protrusions 111, which leads to reduction in parasitic capacitance of the resistance element 100.
- [0028] The insulating film 130 is placed on a surface of each protrusion 111. This insulating film 130 insulates the semiconductor substrate 110 including the protrusions 111 from the resistive film 140. The insulating film 130 includes, for example, SiO₂.
- [0029] The protective film 150 is a film that covers the resistive film 140 and protects the resistive film 140. This protective film 150 includes, for example, an insulator such as SiN. The protective film 150 fills a gap caused in the resistive film 140 between the adjacent protrusions 111, leading to prevention of voids.
- [0030] The contact plug 160 is adjacent to the resistive film 140 and connects the resistance element 100 and a wire. This contact plug 160 includes, for example, a metal such as

tungsten (W) or copper (Cu). In the example shown in Fig. 2, the contact plug 160 is placed on a surface of the resistive film 140 adjacent to the top of the protrusions 111. The contact plug 160 may also be placed on a surface of the resistive film 140 adjacent to the insulating layer 120.

[0031] The protrusions 111 are formed on the surface of the semiconductor substrate 110, and the resistive film 140 is formed to be adjacent to the protrusions 111 and across the steps 112 of the protrusions 111. Accordingly, the resistive film 140 is formed on side surfaces of the protrusions 111. Such a configuration increases an effective length of the resistive film 140 and increases a resistance of the resistive film 140. Such a configuration reduces an area occupied by the resistance element 100 on the surface of the semiconductor substrate 110.

[0032] (Method for manufacturing resistance element)

Figs. 3A to 6M show an example of a method for manufacturing the resistance element according to the first embodiment of the present disclosure. Figs. 3A to 6M show an example of a process for manufacturing the resistance element 100. First, the surface of the semiconductor substrate 110 is subjected to thermal oxidation to form a SiO₂ film (not shown). Next, a SiN film 301 is formed. The film formation is performed, for example, by chemical vapor deposition (CVD) (see Fig. 3A).

[0033] Next, a resist 302 is placed on a surface of the SiN film 301. An opening 303 is formed in a region of the resist 302 excluding a region where the protrusions 111 are to be formed (see Fig. 3B).

[0034] Next, the surfaces of the SiN film 301 and the semiconductor substrate 110 are ground using the resist 302 as a mask. The grinding is performed, for example, by anisotropic etching in which dry etching is employed. Due to this etching, the protrusions 111 are formed on the surface of the semiconductor substrate 110 (see Fig. 3C).

[0035] Next, a SiO₂ film 304 is placed on the surface of the semiconductor substrate 110. The film formation is performed, for example, by CVD (see Fig. 4D).

[0036] Next, the SiO₂ film 304 is ground. The grinding is performed, for example, by anisotropic etching in which dry etching is employed. Here, using the SiN film 301 as an etching stopper makes it possible to grind the SiO₂ film 304 while leaving the protrusions 111 untouched. Accordingly, the insulating layer 120 is formed (see Fig. 4E).

[0037] Next, the SiN film 301 is removed by wet etching and the like, and the insulating film 130 is placed on the surfaces of the protrusions 111 protruding from the insulating layer 120. This step is performed, for example, by thermally oxidizing the semiconductor substrate 110 including the protrusions 111 (see Fig. 4F).

[0038] Next, a resistive material film 305, which is a material of the resistive film 140, is placed. This step is performed, for example, by forming a polycrystalline silicon film

by CVD (see Fig. 4G). Note that, when a resistance value of the resistive film 140 is adjusted, impurities are implanted into the resistive material film 305. The implantation is performed by ion implantation using P, B and the like as impurities, for example.

[0039] Next, on a surface of the resistive material film 305, a resist 306 having a shape of the resistive film 140 is placed (see Fig. 5H).

[0040] Next, the resistive material film 305 is etched using the resist 306 as a mask. The etching is performed, for example, by dry etching. Accordingly, the resistive film 140 is formed (see Fig. 5I).

[0041] Next, the protective film 150 is placed. This step is performed, for example, by placing a film of an insulator such as SiN or SiO₂ and etching the resistive film 140 (see Fig. 5J).

[0042] Next, an interlayer film 306 (not shown in Fig. 2) is placed. This step is performed, for example, by forming a film of an insulator such as SiO₂ by CVD and the like (see Fig. 6K).

[0043] Next, a contact hole 307 is formed in a region of the interlayer film 306 where the contact plug 160 is to be placed. This step is performed by dry etching (see Fig. 6L). Note that a silicide film may be placed on a surface of the resistive film 140 where the contact plug 160 is to be placed.

[0044] Next, a metal serving as a material of the contact plug 160, for example, W is placed in the contact hole 307 to form the contact plug 160. This step is performed, for example, by forming a W film by CVD and removing W in portions other than the contact hole 307 (see Fig. 6M). In this manner, it is possible to manufacture the resistance element 100.

[0045] (Modification)

The resistance element 100 is provided with the protrusions 111 having a rectangular cross section. However, the protrusions 111 may have a different shape.

[0046] (Other configurations of resistance element)

Figs. 7A to 7C are views of other configuration examples of the resistance element according to the first embodiment of the present disclosure. In the example shown in Fig. 7A, each protrusion 111 has a tapered cross section. A resistive film 140 in Fig. 7A includes a trapezoidal cross-sectional valley 141 placed between adjacent protrusions 111.

[0047] A resistive film 140 shown in Fig. 7B is provided with protrusions 111 that has a tapered cross section, as similar to Fig. 7A, and with valleys 142 having a triangular cross section.

[0048] A resistive film 140 shown in Fig. 7C is an example, being adjacent to an insulating layer 120 having a curved surface. The resistive film 140 in Fig. 7C includes valleys

143 having a cross section curved according to the shape of a surface of the insulating layer 120.

[0049] Note that the configuration of the resistance element 100 is not limited to these examples. For example, the resistive film 140 may be placed on a protrusion 111 having a triangular or hemispherical cross section.

[0050] As described above, in the resistance element 100 according to the first embodiment of the present disclosure, the resistive film 140 is formed across the steps of the plurality of protrusions 111, which makes it possible to extend the resistive film 140 along the steps. Such a configuration increases a length of the resistive film 140 without increasing the size in the longitudinal direction. Such a configuration enables the resistive film 140 with a high resistance value and facilitates an increase in resistance of the resistance element 100.

[0051] <2. Second Embodiment>

In the resistance element 100 according to the first embodiment, the plurality of protrusions 111 is placed on the semiconductor substrate 110. In a second embodiment of the present disclosure, the size and the like of a protrusion 111 will be proposed.

[0052] (Cross-sectional configuration of resistance element)

Fig. 8 is a cross-sectional view of a configuration example of a resistance element according to the second embodiment of the present disclosure. Fig. 8 simply shows a configuration example of a resistance element 100. In Fig. 8, t_1 and t_2 represent a thickness of a resistive film 140 and a thickness of an insulating film 130, respectively. Furthermore, w represents an interval between adjacent protrusions 111. In a case where the insulating film 130 is placed as shown in Fig. 8, w represents an interval between insulating films 130 on surfaces of the protrusions 111. In addition, h represents a height of each protrusion 111 from a surface of an insulating layer 120.

[0053] The interval w between the protrusions 111 is preferably larger than twice the thickness t_1 of the resistive film 140. This is because such a configuration prevents the resistive film 140 on a side surface of a protrusion 111 between adjacent protrusions 111 from touching the resistive film 140 on the opposite side surface and prevents a decrease in resistance value.

[0054] Furthermore, the height h of the protrusion 111 from the surface of the insulating layer 120 is preferably about 400 nm or less. As described in Figs. 5H to 5J, the resistive film 140 is formed by dry etching the resistive material film 305 such as polycrystalline silicon adjacent to the insulating film 130 on the surfaces of the protrusions 111. In this dry etching, the top (upper surface) of each protrusion 111 is more likely to be overetched than a portion near the bottom, which easily causes damages to the insulating film 130 adjacent to the upper surface of each protrusion 111. In a case where the thickness t_2 of the insulating film 130 is 10 nm, the height h is adjusted to about

400 nm or less so as to reduce damages to the insulating film 130 during the dry etching.

[0055] Other configurations of the resistance element 100 are similar to those of the resistance element 100 according to the first embodiment of the present disclosure and will not be hereinafter described.

[0056] As described above, the resistance element 100 according to the second embodiment of the present disclosure prevents a change in resistance value by defining the size of the protrusions 111 and the like.

[0057] <3. Third Embodiment>

In the resistance element 100 according to the first embodiment, the insulating layer 120 is placed on the surface of the semiconductor substrate 110. A third embodiment of the present disclosure is different from the first embodiment in that the insulating layer 120 is omitted.

[0058] (Cross-sectional configuration of resistance element)

Fig. 9 is a cross-sectional view of a configuration example of a resistance element according to the third embodiment of the present disclosure. Similarly to Fig. 2, Fig. 9 shows a configuration example of a resistance element 100. Fig. 9 differs from the resistance element 100 in Fig. 2 in that the resistance element herein is provided with no insulating layer 120.

[0059] An insulating film 130 in Fig. 9 is placed on a surface of a semiconductor substrate 110 including protrusions 111 and is placed between the semiconductor substrate 110 and a resistive film 140. Accordingly, the semiconductor substrate 110 and the resistive film 140 are insulated.

[0060] Other configurations of the resistance element 100 are similar to those of the resistance element 100 according to the first embodiment of the present disclosure and will not be hereinafter described.

[0061] As described above, omission of the insulating layer 120 simplifies the configuration of the resistance element 100 according to the third embodiment of the present disclosure.

[0062] <4. Fourth Embodiment>

The resistance element 100 according to the first embodiment is provided with the plurality of protrusions 111. A fourth embodiment of the present disclosure is different from the first embodiment in that a resistance element is provided with one protrusion 111.

[0063] (Cross-sectional configuration of resistance element)

Fig. 10 is a cross-sectional view of a configuration example of a resistance element according to the fourth embodiment of the present disclosure. Similarly to Fig. 2, Fig. 10 shows a configuration example of a resistance element 100. The resistance element

herein differs from the resistance element 100 in Fig. 2 in that it includes a resistive film 144 that traverses a step of one protrusion 111.

[0064] The resistive film 144 in Fig. 10 traverses only one step 112 of the protrusion 111. This resistive film 144 is provided with contact plugs 160 and 161 with different heights. The contact plug 160 is adjacent to the resistive film 144 placed on the top of the protrusion 111. On the other hand, the contact plug 161 is adjacent to the resistive film 144 which is adjacent to an insulating layer 120. Since the contact plug 161 is placed near the bottom of the step 112 of the protrusion 111, the contact plug 161 is longer than the contact plug 160.

[0065] Note that the configuration of the resistance element 100 is not limited to this example. For example, both steps 112 of the protrusion 111 may be traversed by the resistive film 144. In this case, two contact plugs 161 are placed.

[0066] Other configurations of the resistance element 100 are similar to those of the resistance element 100 according to the first embodiment of the present disclosure and will not be hereinafter described.

[0067] As described above, the resistance element 100 according to the fourth embodiment of the present disclosure includes the resistive film 144 adjacent to one protrusion 111. Accordingly, it is possible to simplify the configuration of the resistance element 100.

[0068] <5. Fifth Embodiment>

The resistance element 100 according to the first embodiment includes the resistive film 140 that traverses the protrusions 111. In a fifth embodiment of the present disclosure, described is an electronic device that includes this resistance element 100.

[0069] (Circuit configuration of electronic device)

Fig. 11 is a view of a configuration example of an electronic device according to the fifth embodiment of the present disclosure. Fig. 11 is a circuit diagram showing a configuration example of an electronic device 10. The electronic device 10 in Fig. 11 includes a MOS transistor 200 and a resistance element 100. An example of the MOS transistor 200 includes an n-channel MOS transistor. The electronic device 10 in Fig. 11 corresponds to an amplifier circuit, being configured to amplify a signal input from an input signal line IN (signal line 11) and output the amplified signal to an output signal line OUT (signal line 12). Furthermore, a power wire Vdd for supplying power is wired to the electronic device 10 in Fig. 11.

[0070] The gate of the MOS transistor 200 is connected to the input signal line IN, and the drain is connected to the power wire Vdd. The source of the MOS transistor 200 is connected to one end of the resistance element 100 and to the output signal line OUT. The other end of the resistance element 100 is grounded.

[0071] The electronic device 10 in Fig. 11 is included in a source follower circuit. The resistance element 100 corresponds to the load resistance of the MOS transistor 200. As

described later, a Fin transistor is employable as the MOS transistor 200. The fin transistor is a MOS transistor including a fin formed on a semiconductor substrate. Here, the fin is a fin-shaped protrusion formed on a surface of the semiconductor substrate.

[0072] (Configuration of electronic device)

Fig. 12 is a perspective view of the configuration example of the electronic device according to the fifth embodiment of the present disclosure. Fig. 12 is a perspective view of the configuration example of the electronic device 10, showing outer shapes and arrangements of the MOS transistor 200 and the resistance element 100 formed on a surface of a semiconductor substrate.

[0073] The resistance element 100 in Fig. 12 includes a resistive film 145. The resistive film 145 is formed to traverse steps between two protrusions 111 and a protrusion 113. The protrusion 113 is longer than the protrusions 111 and is shared with the after-mentioned fin of the MOS transistor 200. In other words, the resistance element 100 is formed at one end of the protrusion 113, and the MOS transistor 200 is formed at the other end. Note that, in the resistance element 100 in Fig. 12, an insulating film 130, an insulating layer 120, a protective film 150, a contact plug 160, and the like are omitted.

[0074] The MOS transistor 200 is a fin transistor having one end of the protrusion 113 as a fin. This MOS transistor 200 includes a drain region 201, a gate 202, and a source region 203. The drain region 201 and the source region 203 are semiconductor regions formed in the protrusion 113 and have n-type conductivity. The gate 202 crosses over the protrusion 113 between the drain region 201 and the source region 203. A channel is formed near a surface of the protrusion 113 immediately below the gate 202. Note that Fig. 12 shows an outline of the MOS transistor 200, with a gate insulating film, a sidewall, and the like omitted. Note that in the MOS transistor 200, the protrusion 113 is formed to have predetermined conductivity by ion implantation and the like after formation of the protrusion 113. As described above, the protrusion (the protrusion 113) of the resistance element 100 is shared with the fin of the MOS transistor 200 and formed simultaneously on the surface of the semiconductor substrate 110.

[0075] Note that thick lines in Fig. 12 represent wires, and closed circles represent connections between the wires and the semiconductor regions or the resistive film 145. The drain region 201 of the MOS transistor 200 is connected to the power wire Vdd, and the gate 202 is connected to the input signal line IN. The source region 203 of the MOS transistor is connected to the output signal line OUT and to one end of the resistive film 145 adjacent to the protrusion 113. The other end of the resistive film 145 is grounded.

[0076] As shown in Fig. 12, when the resistance element 100 and the MOS transistor are placed on one semiconductor substrate, it is possible to simultaneously form

components such as an insulating film. For example, the insulating film 130 of the resistance element 100 may be formed simultaneously with a gate insulating film of the MOS transistor 200. Furthermore, the insulating layer 120 of the resistance element 100 may be formed simultaneously with the insulating layer provided below the gate 202 of the MOS transistor 200. Still further, the protective film 150 of the resistance element 100 may be formed simultaneously with a side wall insulating film (sidewall) of the gate 202 of the MOS transistor 200.

[0077] In this manner, since the protrusion 113 of the resistance element 100 is shared with the fin of the MOS transistor 200, it is possible to downsize the electronic device 10. Simultaneously forming the components of the resistance element 100 and the MOS transistor 200 simplifies a process for manufacturing the electronic device 10.

[0078] (Other configurations of electronic device)

Fig. 13 is a perspective view of another configuration example of the electronic device according to the fifth embodiment of the present disclosure. Similarly to Fig. 12, Fig. 13 is a perspective view of a configuration example of the electronic device 10, showing outer shapes and arrangements of the MOS transistor 200 and the resistance element 100 formed on a surface of a semiconductor substrate. The electronic device 10 in Fig. 13 differs from the electronic device 10 in Fig. 12 in that the protrusions 111 are omitted.

[0079] The resistance element 100 in Fig. 13 includes a resistive film 146. The resistive film 146 is formed to repeatedly traverse steps of a protrusion 113. As this resistive film 146 also traverses the steps, the resistive film 146 is extended along the steps, which enables the resistive film 146 with a high resistance value.

[0080] Other configurations of the electronic device 10 are similar to those of the electronic device 10 in Fig. 12 and will not be hereinafter described.

[0081] As described above, since the electronic device 10 according to the fifth embodiment of the present disclosure uses the resistance element 100 and the MOS transistor 200 included in a fin transistor, the protrusion 111 and the like are shared. Accordingly, it is possible to downsize the resistance element 100 and to simplify a process for manufacturing the resistance element 100.

[0082] Lastly, the embodiments are examples of the present disclosure, and the present disclosure is not limited to the embodiments. Therefore, within the technical idea of the present disclosure, it is possible to employ various modifications of the embodiments according to designs and the like.

[0083] Furthermore, the effects described herein are for purposes of illustration and not limitation. The present disclosure may produce other effects.

[0084] Still further, the drawings in the embodiments are schematic views, and dimensional ratios and the like of each part do not always match actual ones. In addition, it is a

matter of course that dimensional relations and ratios are different between drawings.

[0085] Note that the present technology also employs the following configurations.

- (1) A resistance element including a resistive film, in which the resistive film is adjacent to a protrusion formed on a surface of a semiconductor substrate, the protrusion including a step traversed by the resistive film.
- (2) The resistance element according to (1), further including a plurality of the resistive films connected in series.
- (3) The resistance element according to (2), in which the plurality of the resistive films traversing the step of each of a plurality of the protrusions on the semiconductor substrate is connected in series.
- (4) The resistance element according to (3), further including a protective film placed between the plurality of resistive films connected in series between the plurality of protrusions.
- (5) The resistance element according to (3) or (4), in which two adjacent protrusions of the plurality of protrusions are placed at an interval exceeding twice a thickness of the resistive film.
- (6) The resistance element according to any one of (1) to (5), in which the resistive film is adjacent to the protrusion via an insulating film.
- (7) The resistance element according to any one of (1) to (6), further including an insulating layer placed on the surface of the semiconductor substrate adjacent to the protrusion, in which the resistive film traverses a step between the insulating layer and the protrusion.
- (8) The resistance element according to (7), in which the protrusion has a height of about 400 nm or less from the insulating layer.
- (9) The resistance element according to any one of (1) to (8), in which the resistive film includes polycrystalline silicon.
- (10) The resistance element according to any one of (1) to (9), in which the protrusion is formed by grinding a surface of the semiconductor substrate around the protrusion.
- (11) The resistance element according to any one of (1) to (10), in which the protrusion is formed simultaneously with a fin of a fin transistor placed on the semiconductor substrate.
- (12) An electronic device including: a resistance element including a resistive film adjacent to a protrusion formed on a surface of a semiconductor substrate, the protrusion including a step traversed by the resistive film; and

a transistor placed on the semiconductor substrate and connected to the resistance element.

[0086] It should be understood by those skilled in the art that various modifications, combinations, sub-combinations and alterations may occur depending on design requirements and other factors insofar as they are within the scope of the appended claims or the equivalents thereof.

Reference Signs List

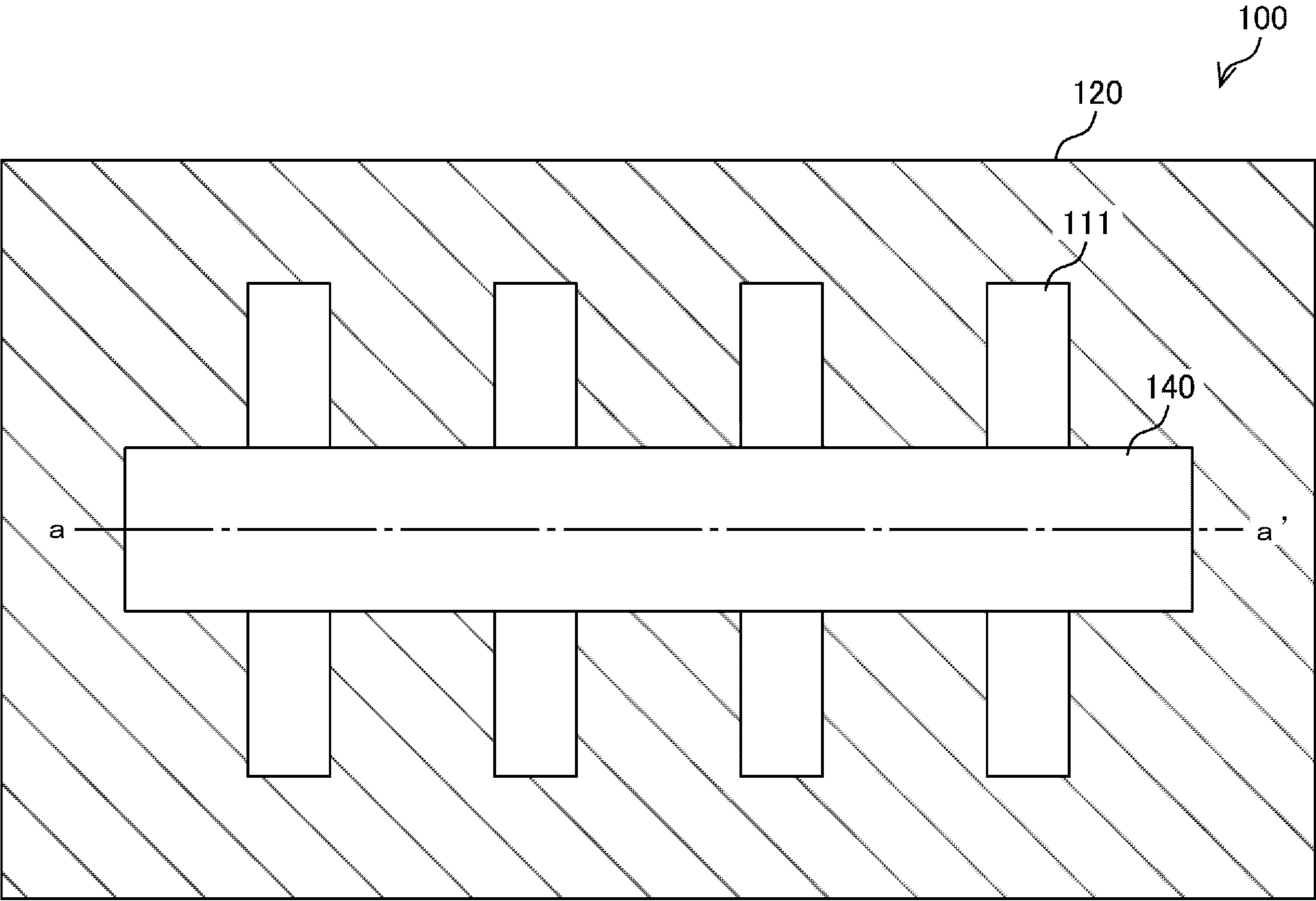
[0087] 10 Electronic device
100 Resistance element
110 Semiconductor substrate
111, 113 Protrusion
112 Step
120 Insulating layer
130 Insulating film
140, 144 to 146 Resistive film
150 Protective film
160, 161 Contact plug
200 MOS transistor

Claims

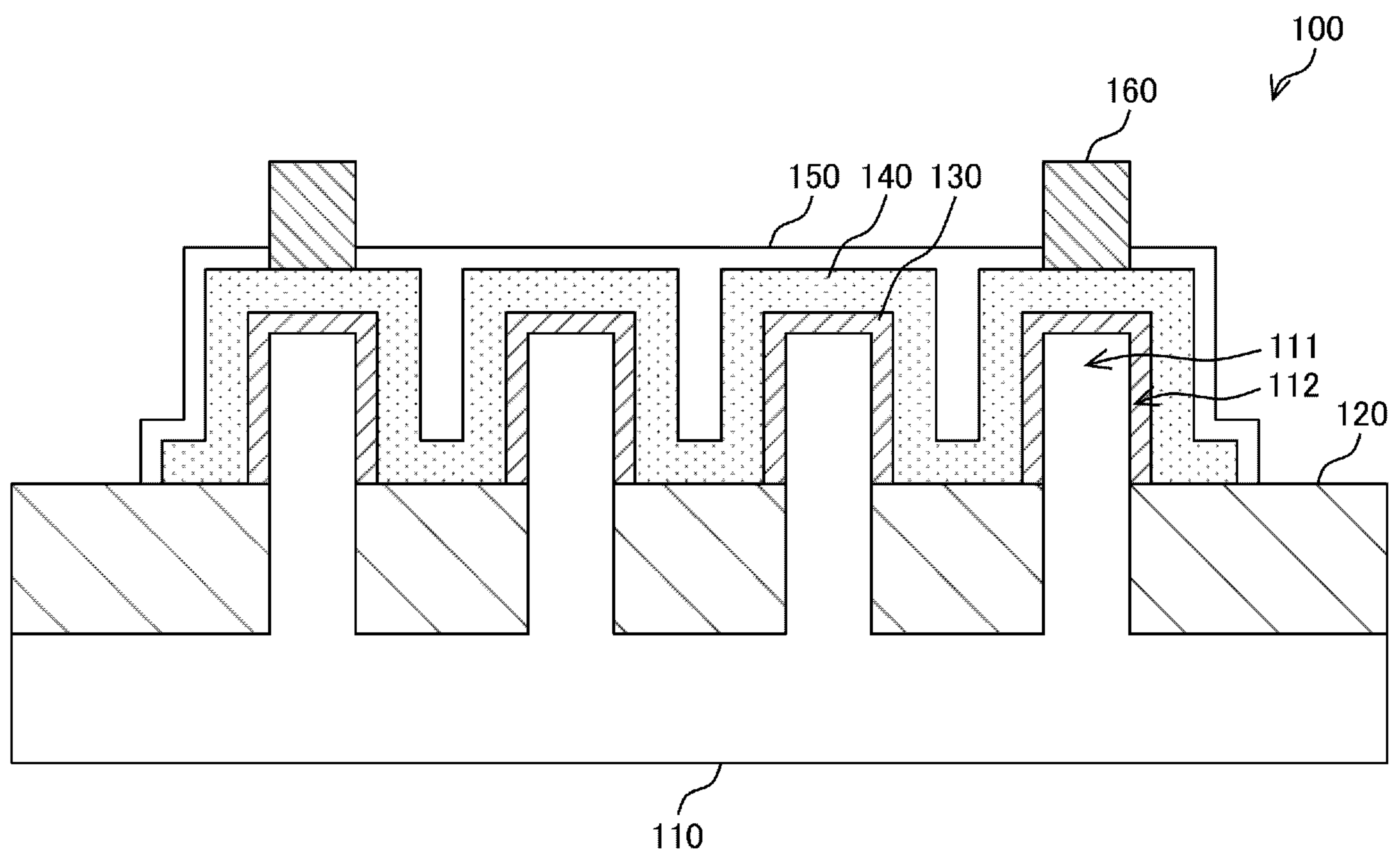
- [Claim 1] A resistance element comprising:
a resistive film,
wherein the resistive film is adjacent to a protrusion formed on a surface of a semiconductor substrate, the protrusion including a step traversed by the resistive film.
- [Claim 2] The resistance element according to claim 1, further comprising:
a plurality of the resistive films connected in series.
- [Claim 3] The resistance element according to claim 2, wherein the plurality of the resistive films traversing the step of each of a plurality of the protrusions on the semiconductor substrate is connected in series.
- [Claim 4] The resistance element according to claim 3, further comprising:
a protective film placed between the plurality of resistive films connected in series between the plurality of protrusions.
- [Claim 5] The resistance element according to claim 3, wherein two adjacent protrusions of the plurality of protrusions are placed at an interval exceeding twice a thickness of the resistive film.
- [Claim 6] The resistance element according to claim 1, wherein the resistive film is adjacent to the protrusion via an insulating film.
- [Claim 7] The resistance element according to claim 1, further comprising:
an insulating layer placed on the surface of the semiconductor substrate adjacent to the protrusion,
wherein the resistive film traverses a step between the insulating layer and the protrusion.
- [Claim 8] The resistance element according to claim 7, wherein the protrusion has a height of about 400 nm or less from the insulating layer.
- [Claim 9] The resistance element according to claim 1, wherein the resistive film includes polycrystalline silicon.
- [Claim 10] The resistance element according to claim 1, wherein the protrusion is formed by grinding a surface of the semiconductor substrate around the protrusion.
- [Claim 11] The resistance element according to claim 1, wherein the protrusion is formed simultaneously with a fin of a fin transistor placed on the semiconductor substrate.
- [Claim 12] An electronic device comprising:
a resistance element including a resistive film adjacent to a protrusion formed on a surface of a semiconductor substrate, the protrusion

including a step traversed by the resistive film; and
a transistor placed on the semiconductor substrate and connected to the
resistance element.

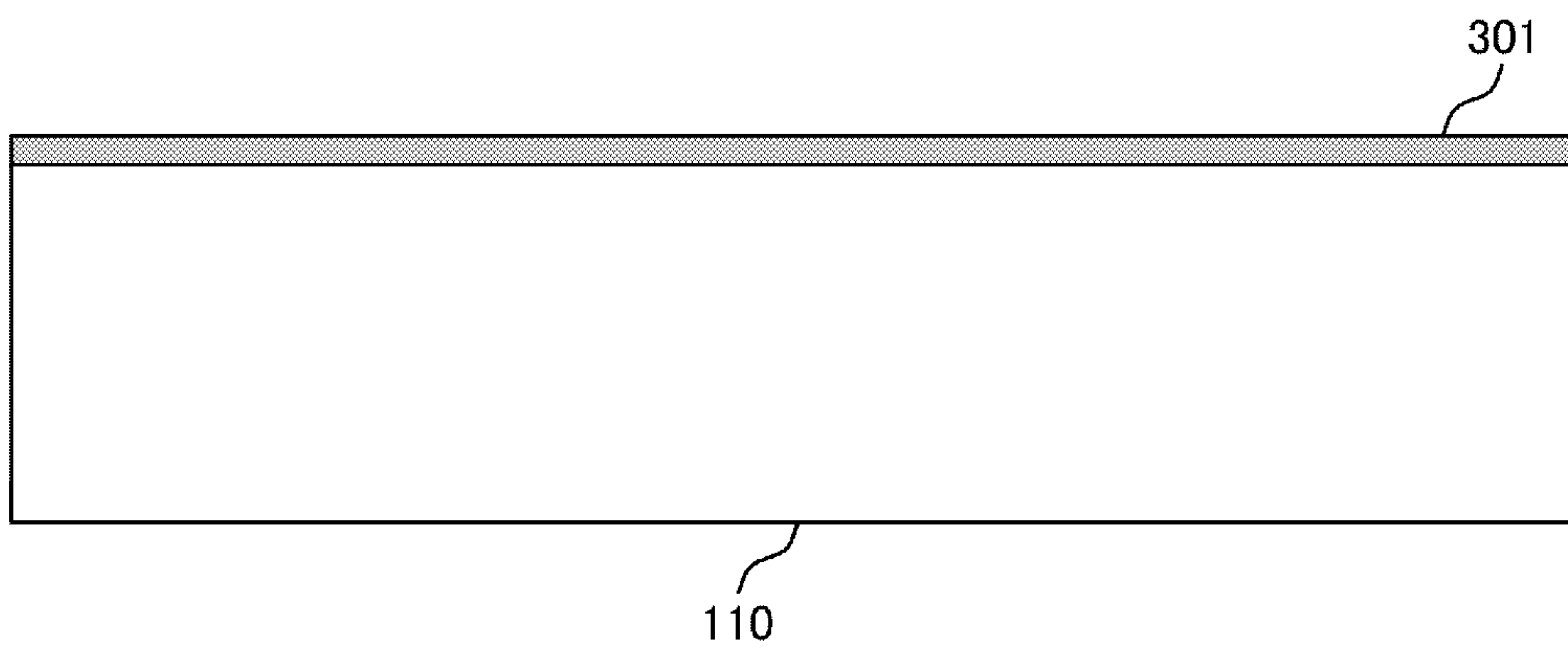
[Fig. 1]



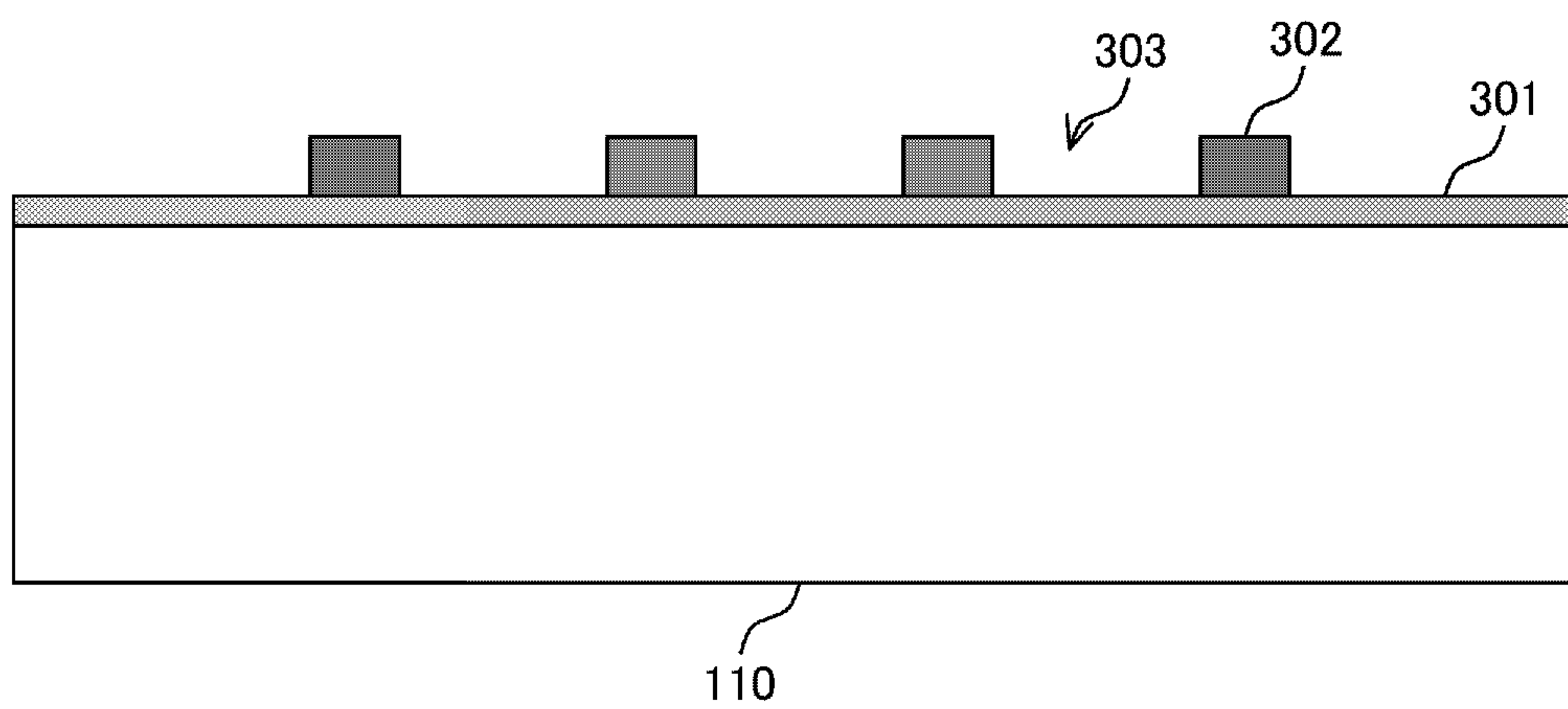
[Fig. 2]



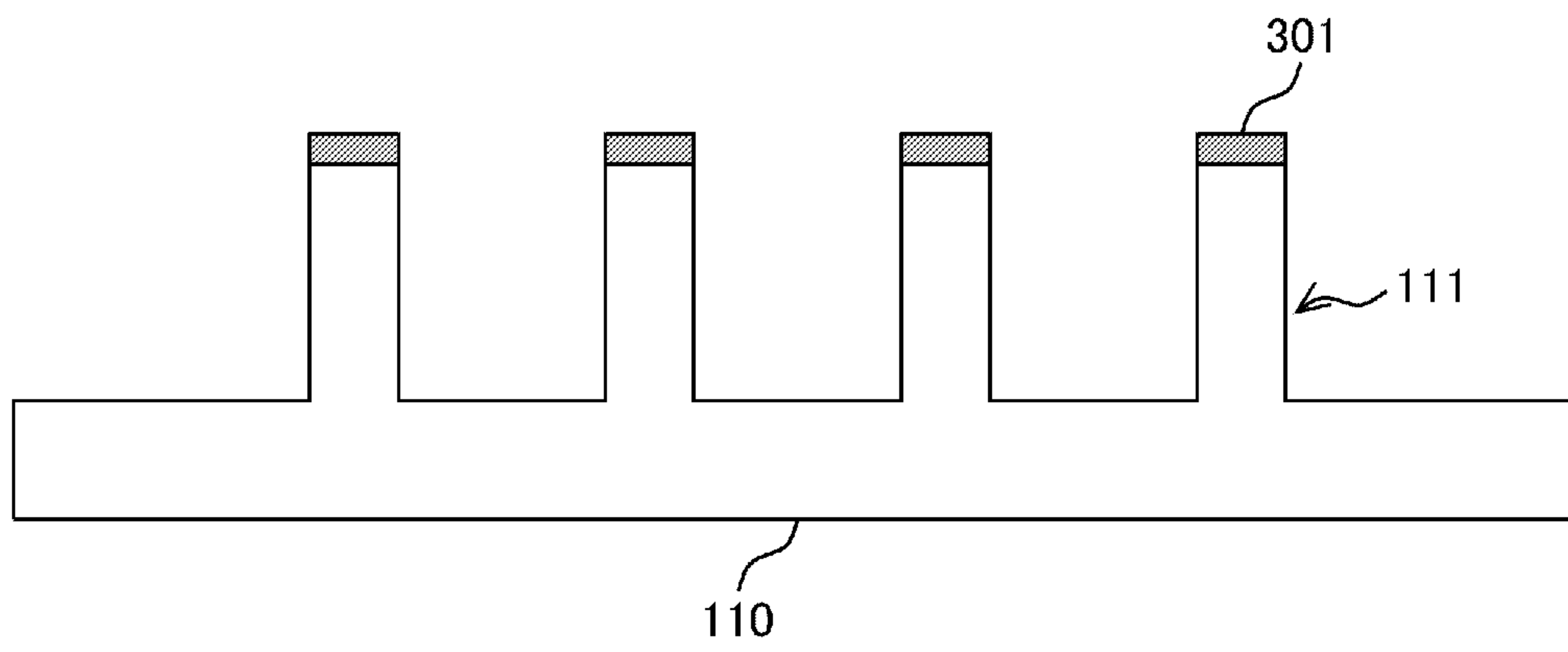
[Fig. 3A]



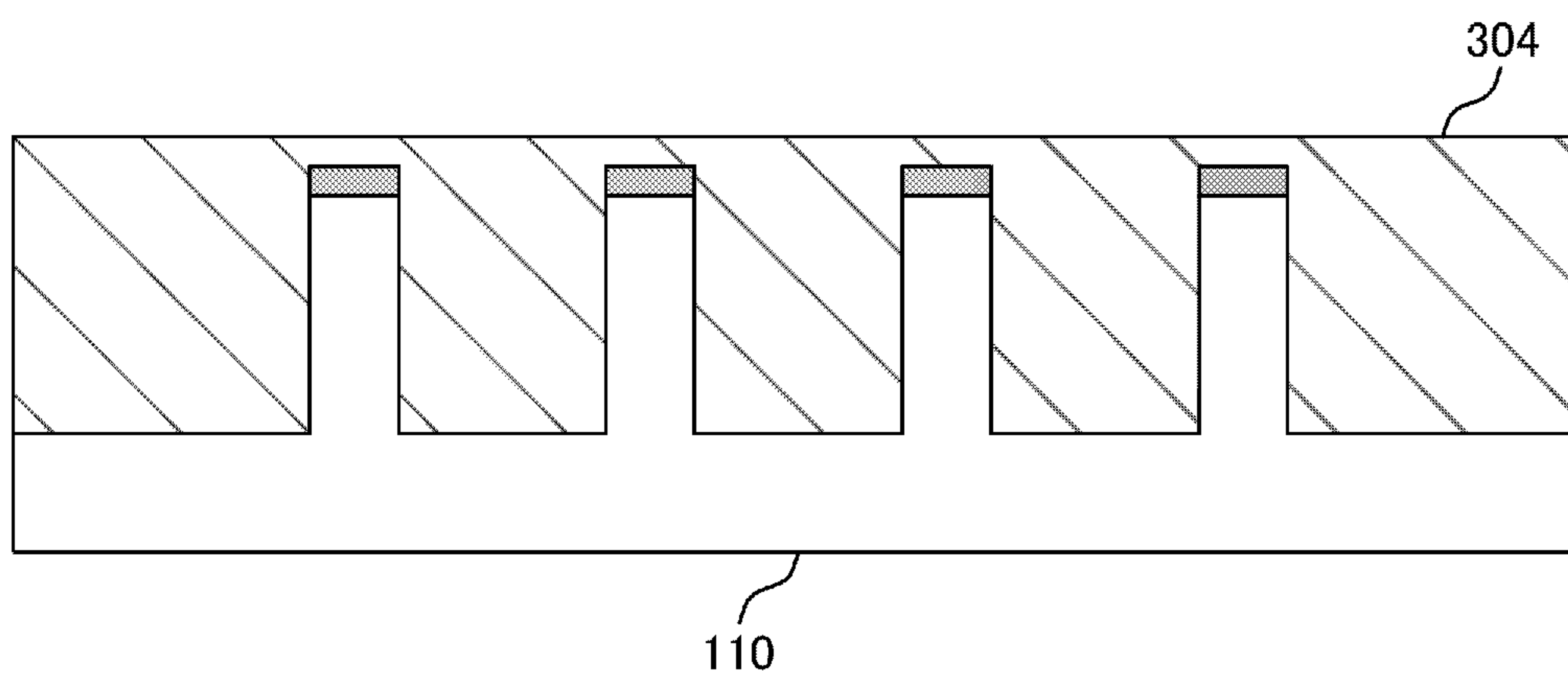
[Fig. 3B]



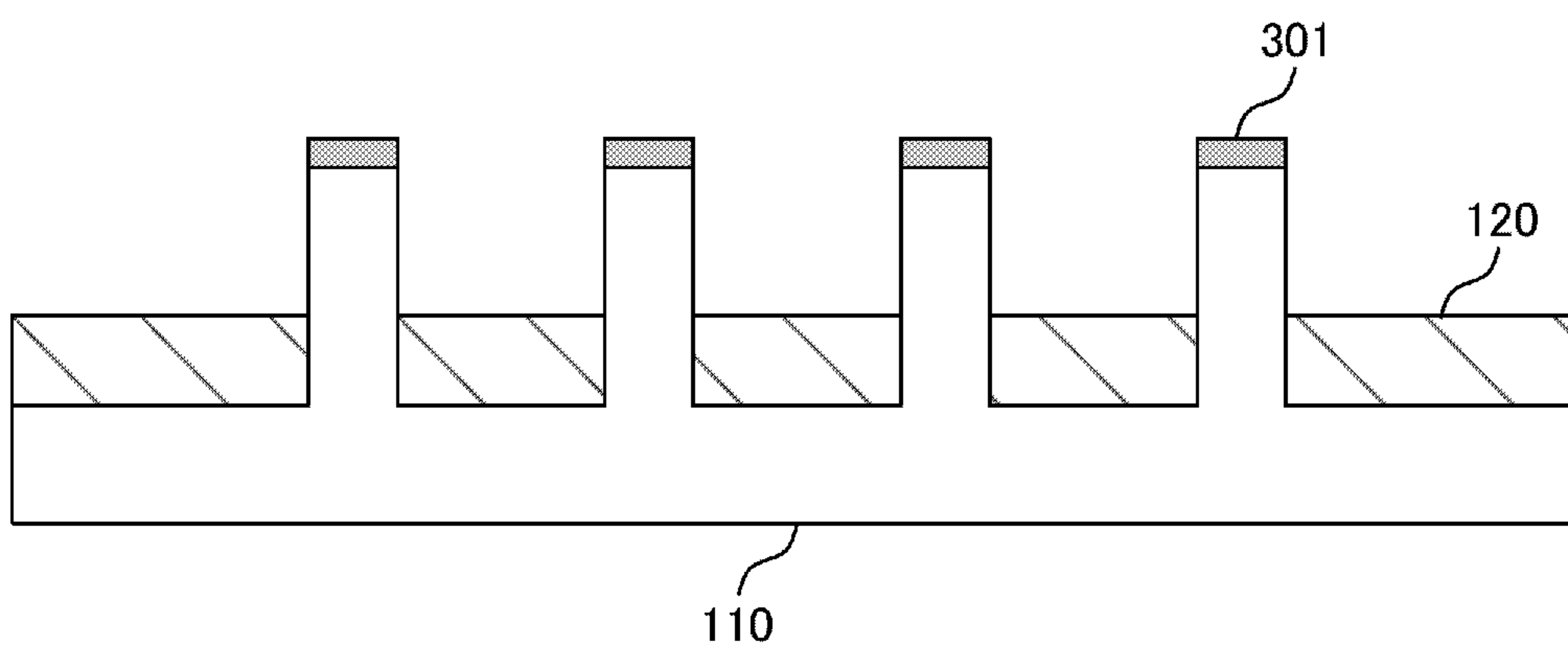
[Fig. 3C]



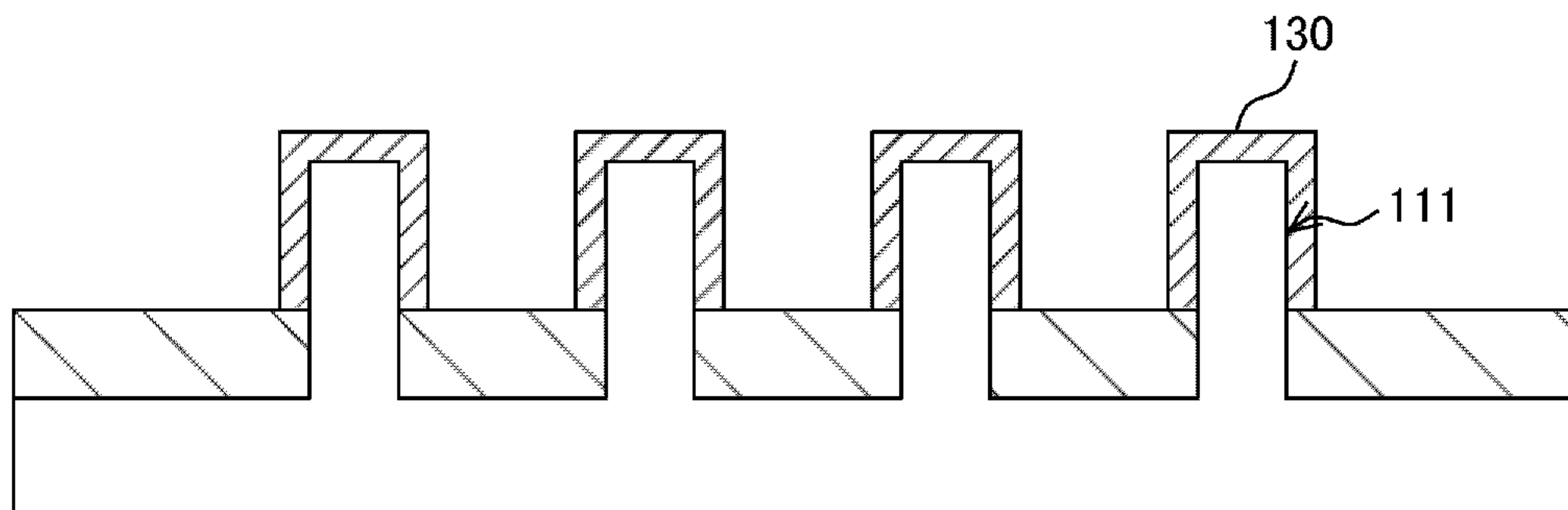
[Fig. 4D]



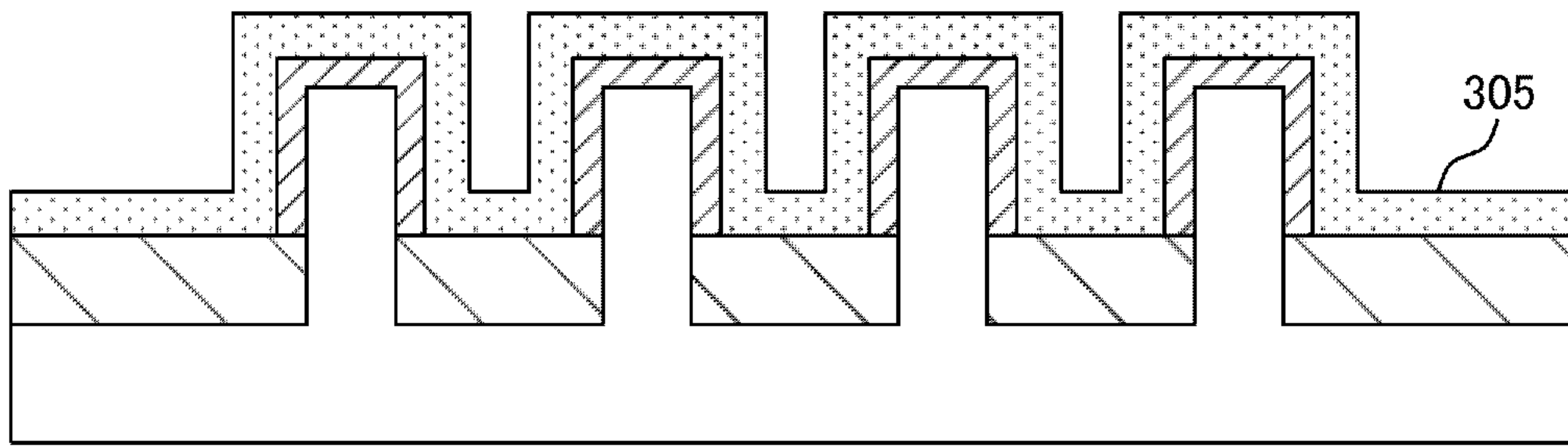
[Fig. 4E]



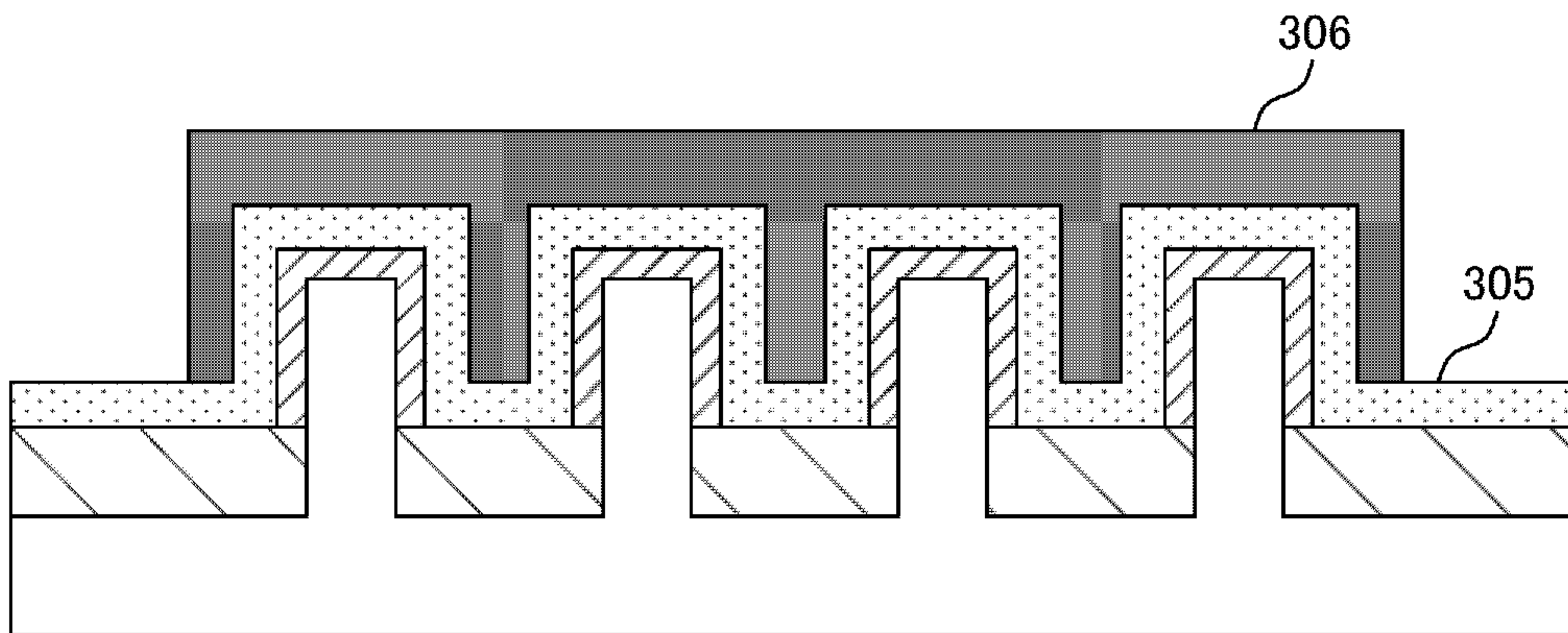
[Fig. 4F]



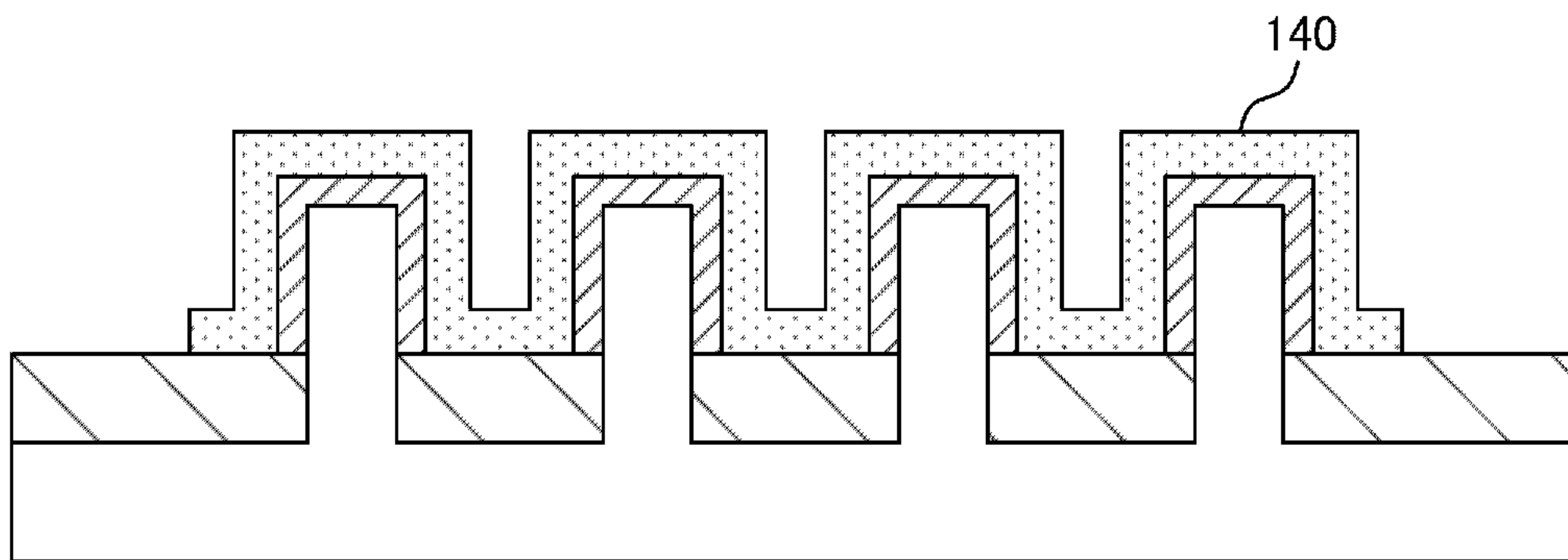
[Fig. 4G]



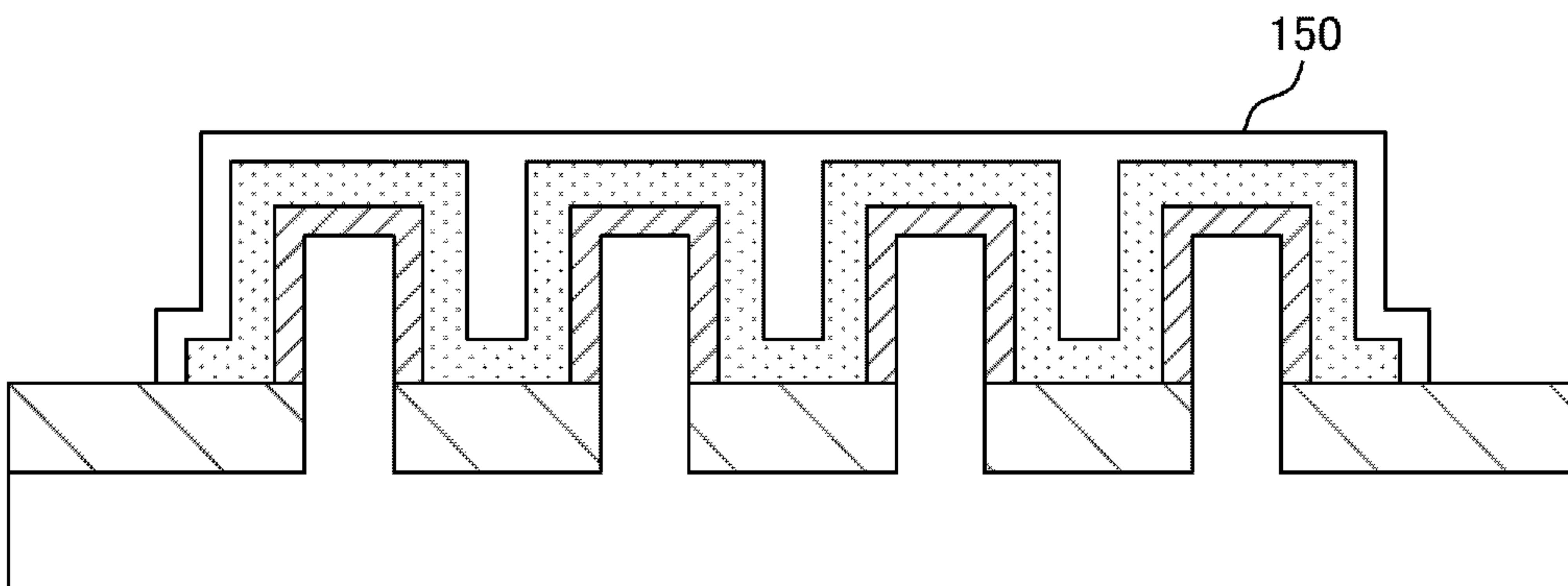
[Fig. 5H]



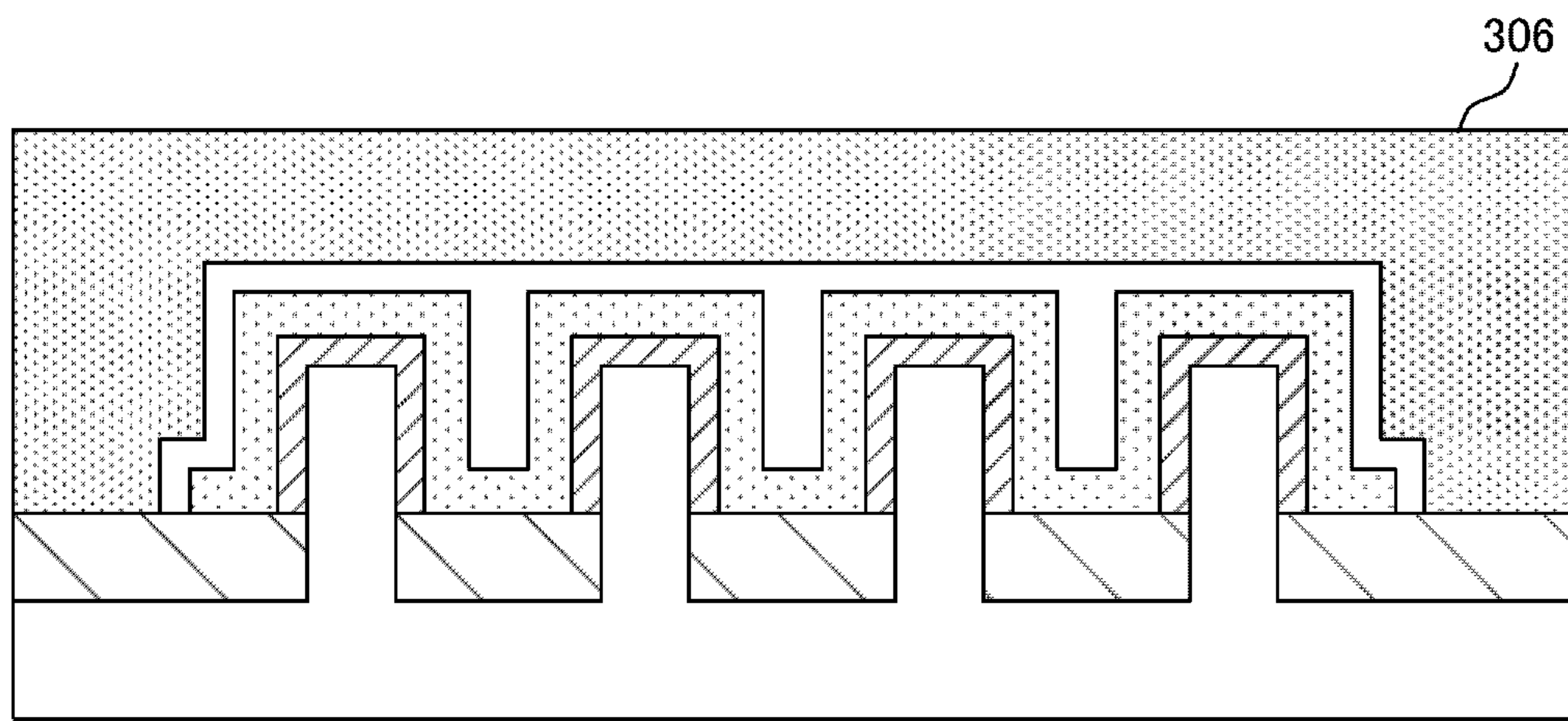
[Fig. 5I]



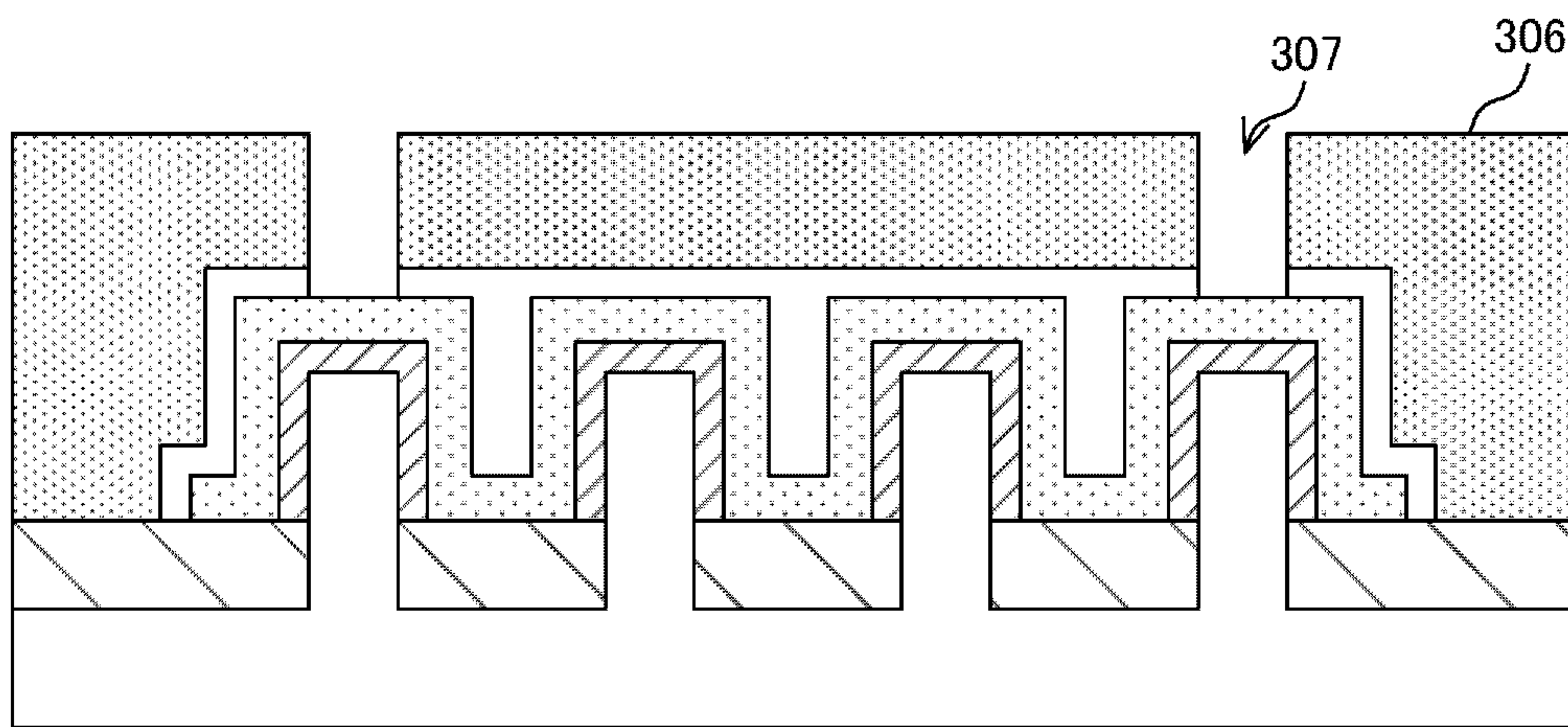
[Fig. 5J]



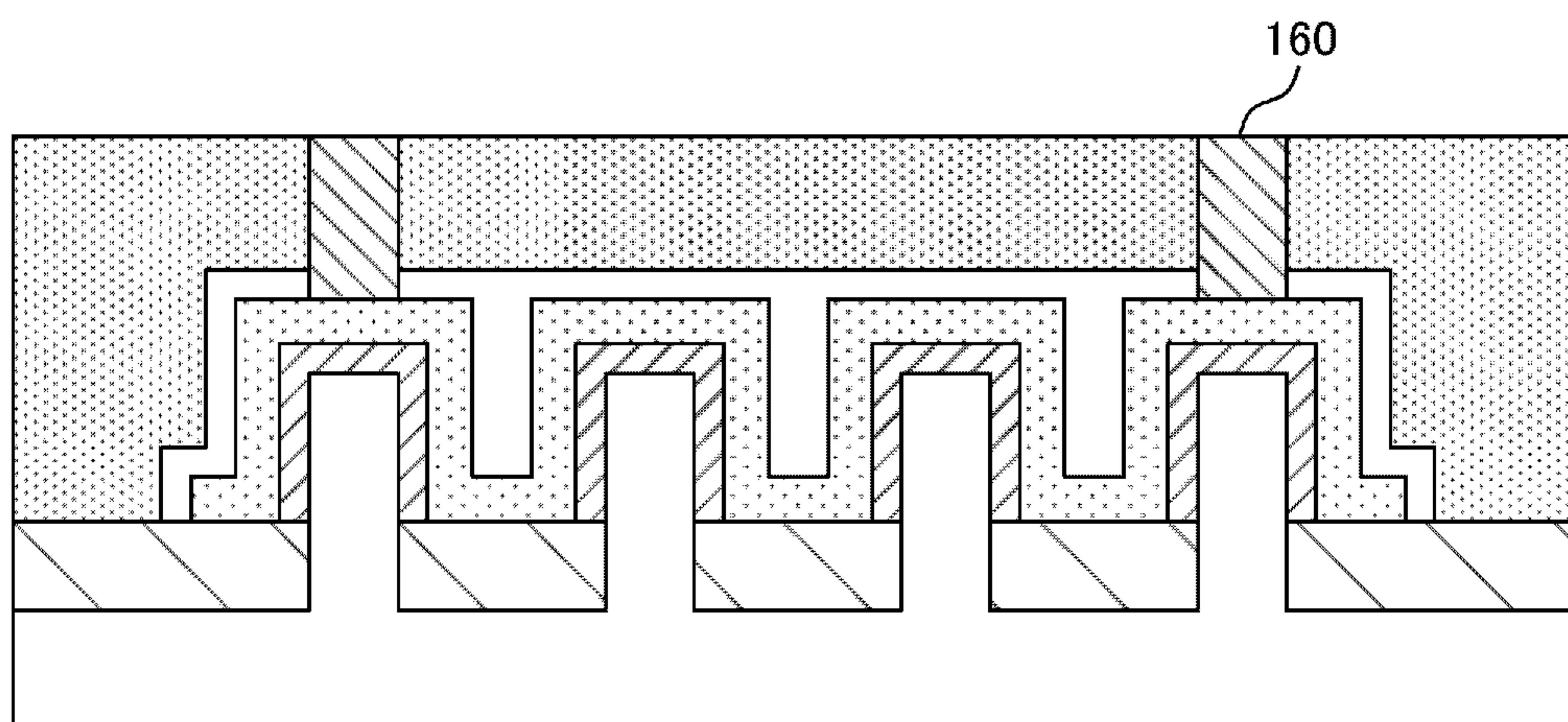
[Fig. 6K]



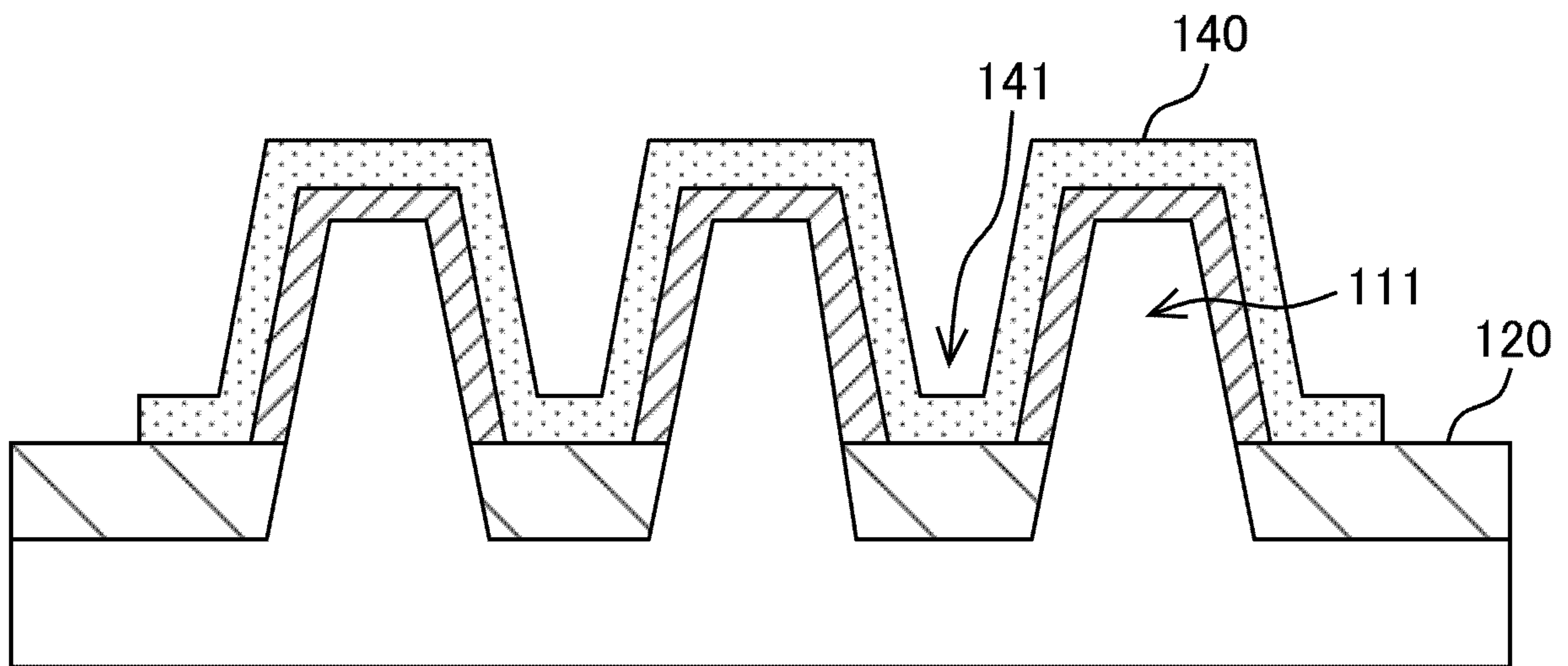
[Fig. 6L]



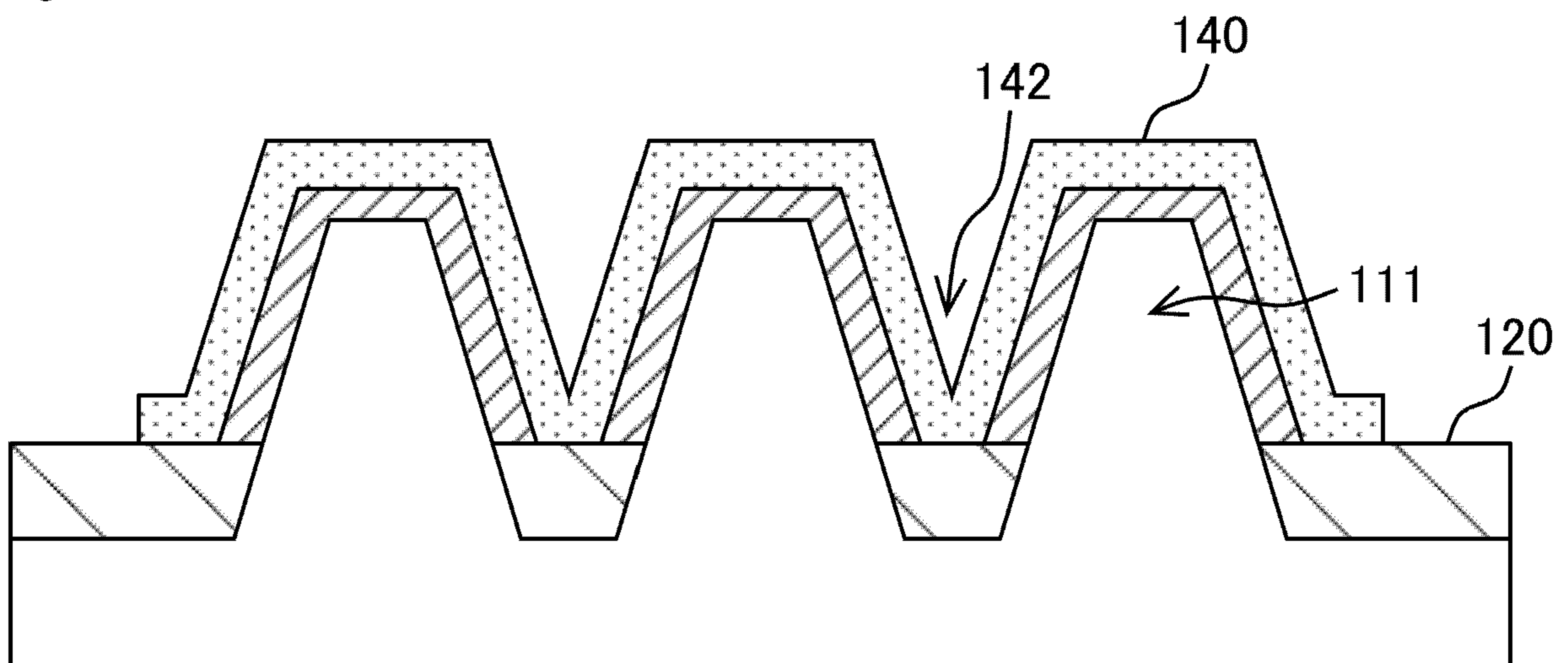
[Fig. 6M]



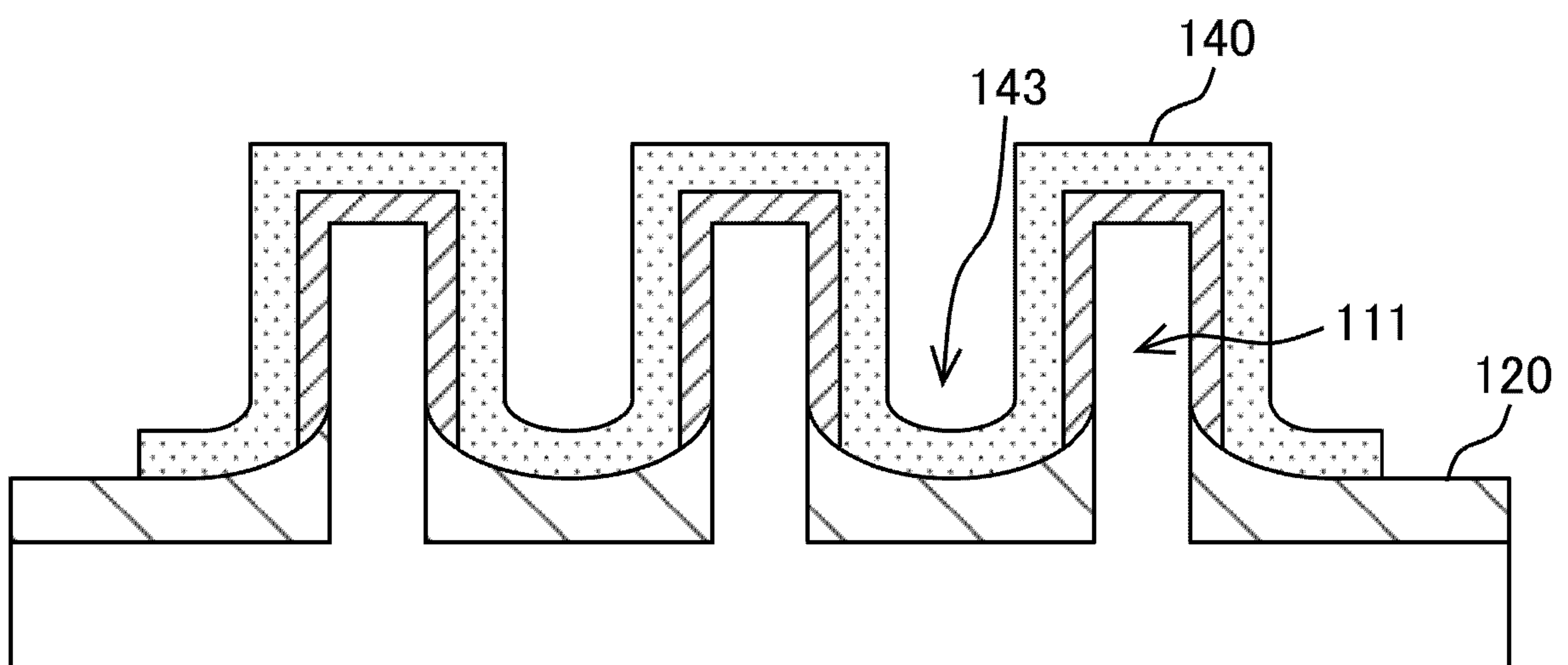
[Fig. 7A]



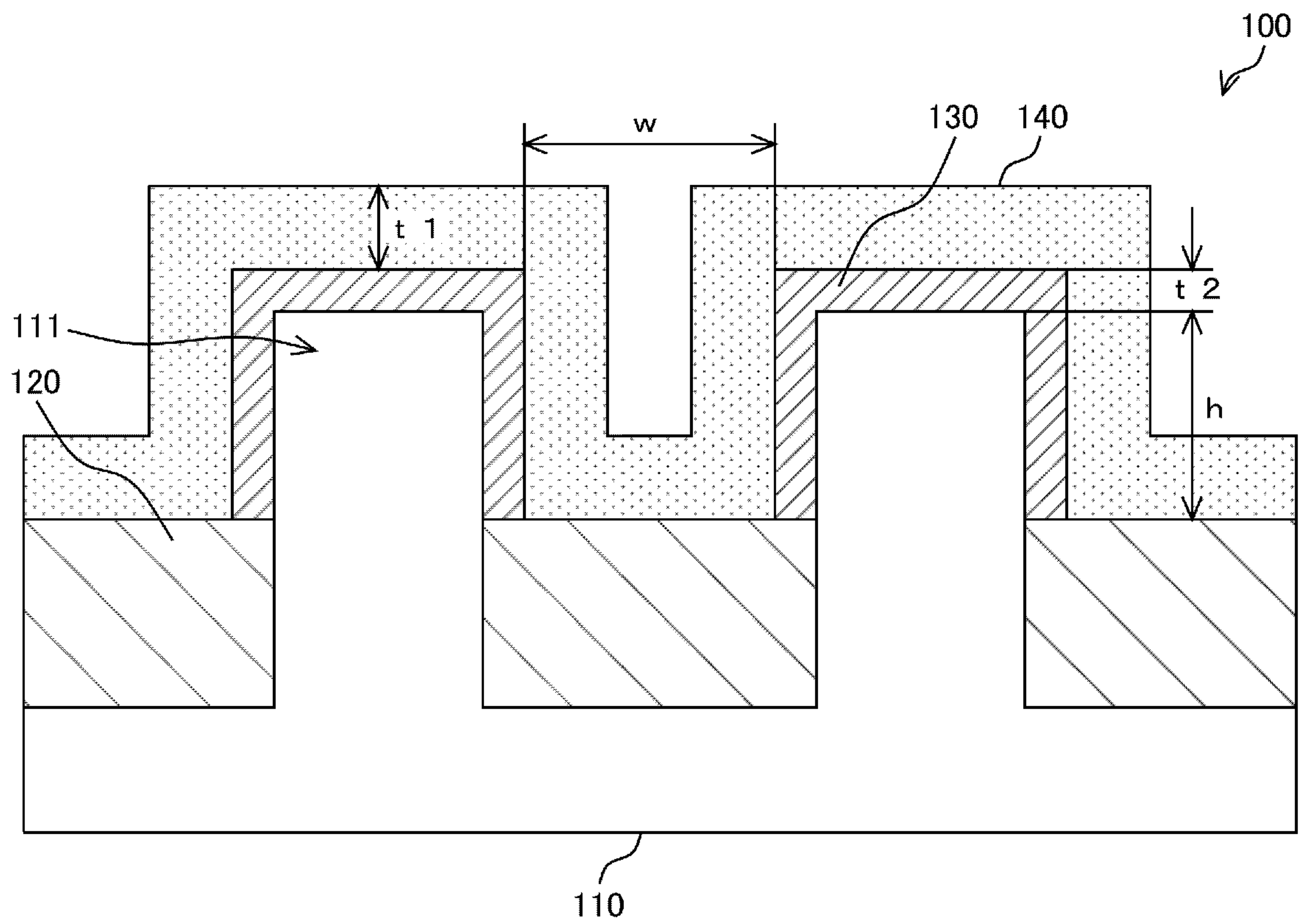
[Fig. 7B]



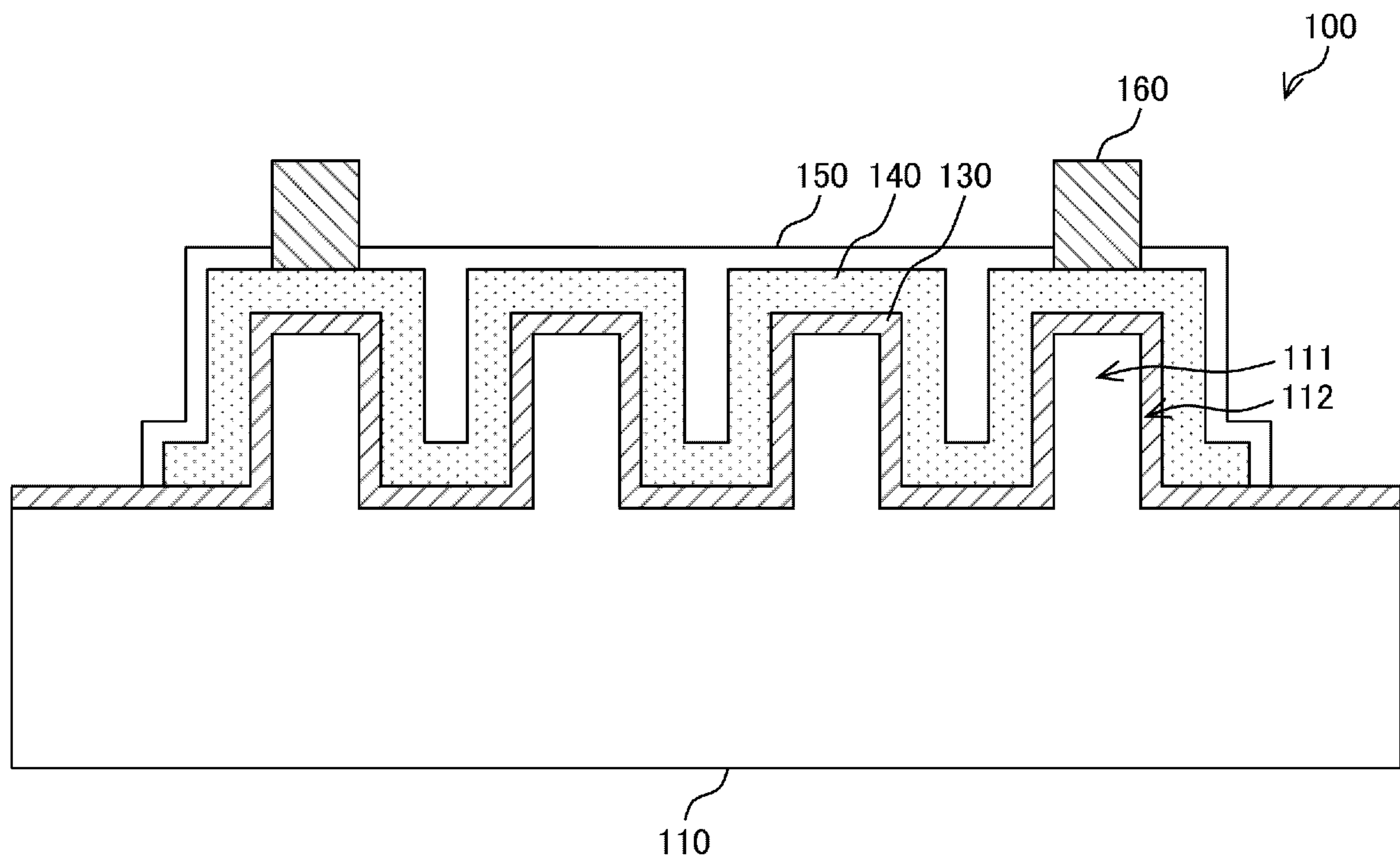
[Fig. 7C]



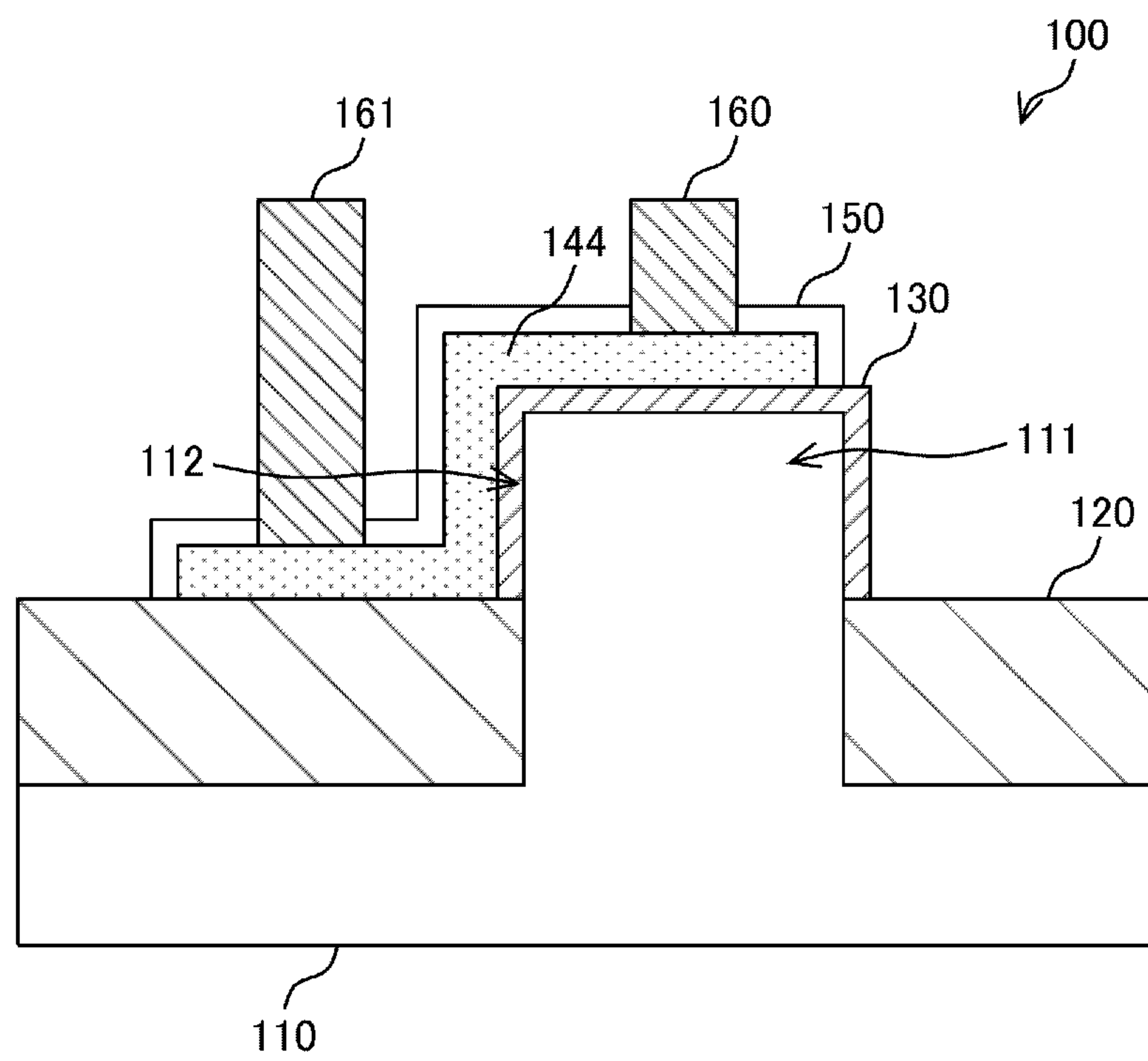
[Fig. 8]



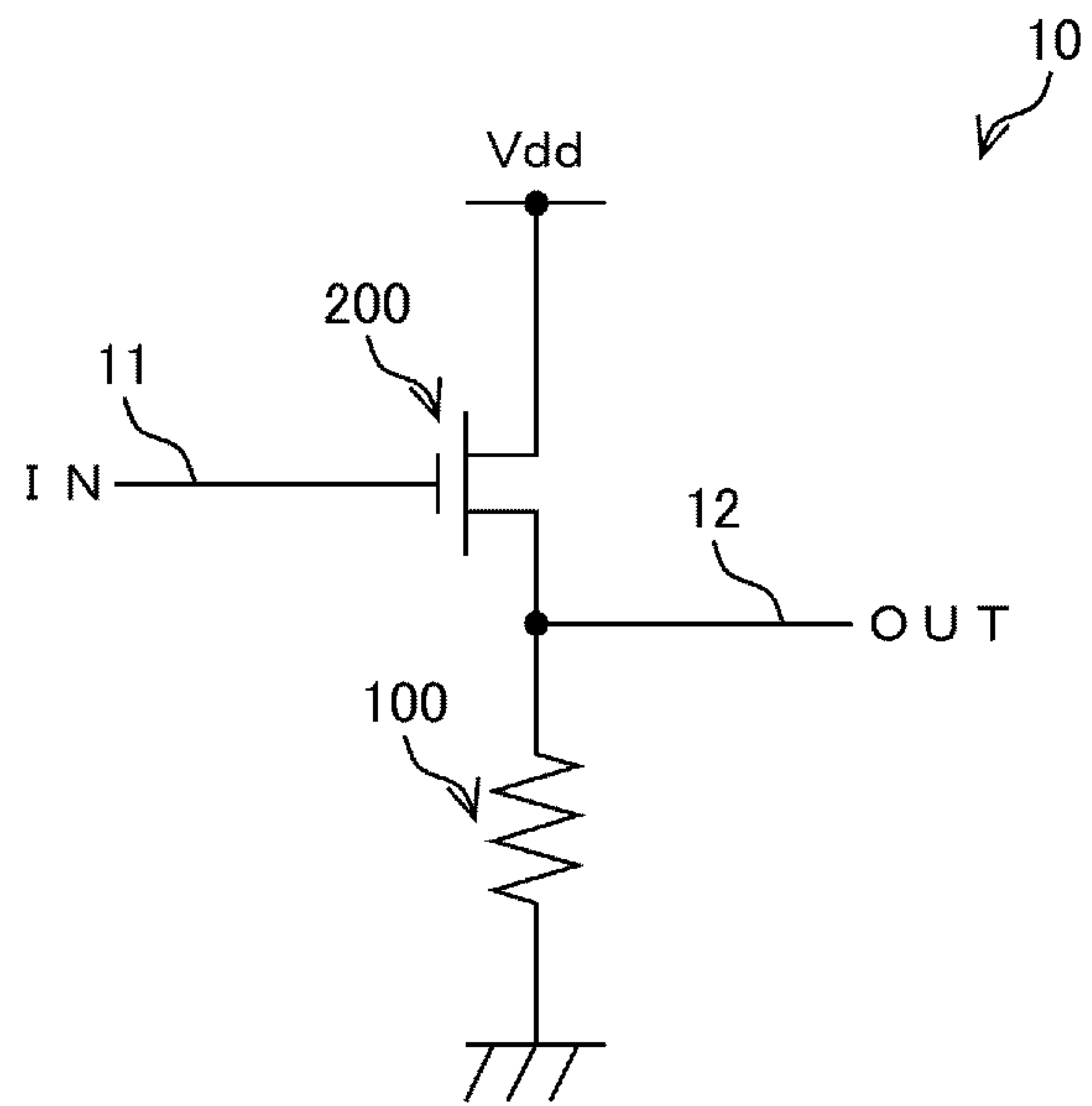
[Fig. 9]



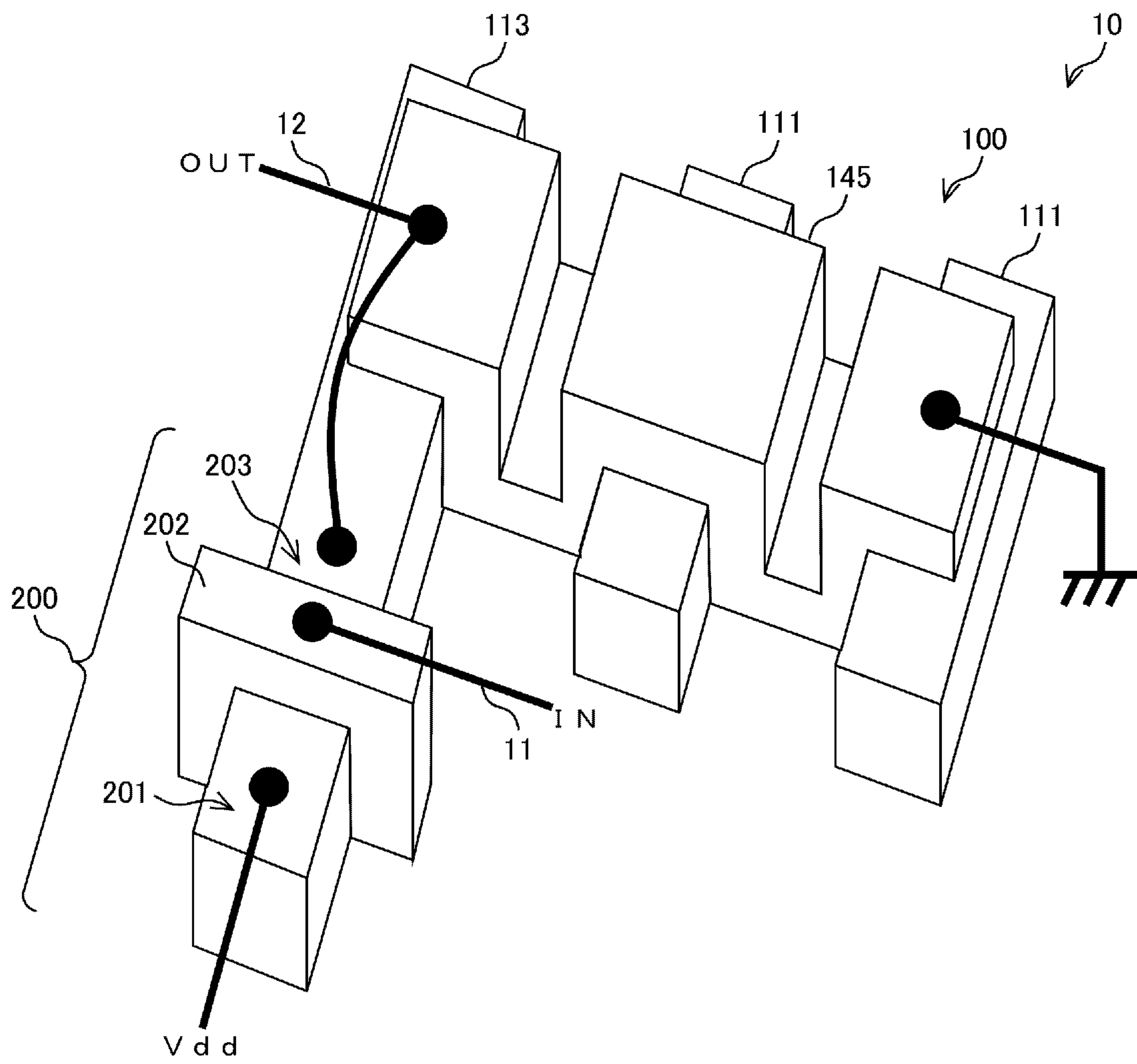
[Fig. 10]



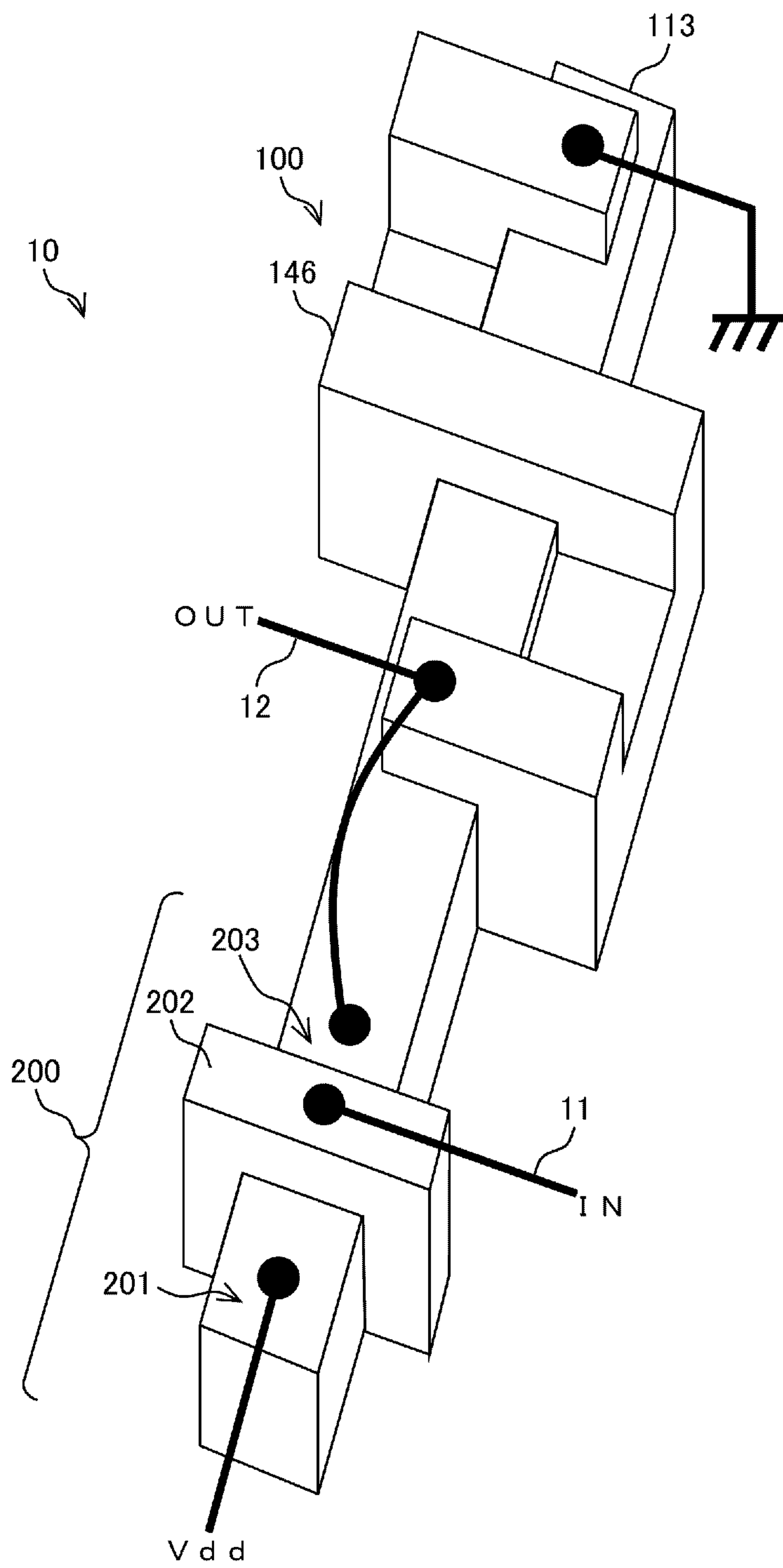
[Fig. 11]



[Fig. 12]



[Fig. 13]



INTERNATIONAL SEARCH REPORT

International application No

PCT/JP2020/030440

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H01L49/02 H01L27/06
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9 478 625 B1 (ZANG HUI [US] ET AL) 25 October 2016 (2016-10-25) column 6, line 56 - column 7, line 52; figures 20-22	1-7,11, 12
X	----- US 2014/084381 A1 (YEH JENG-YA D [US] ET AL) 27 March 2014 (2014-03-27) paragraphs [0032] - [0036]; figures 2A-2K	1,9
X	----- EP 2 590 221 A1 (BROADCOM CORP [US]) 8 May 2013 (2013-05-08) paragraphs [0034], [0042] - [0047]; figures 10A,10B	1,10
X	----- US 2015/333057 A1 (HOENTSCHEL JAN [DE] ET AL) 19 November 2015 (2015-11-19) paragraphs [0017], [0058] - [0081]; figures 4a-12b	1,7,8
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Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

9 October 2020

Date of mailing of the international search report

19/10/2020

Name and mailing address of the ISA/

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Bräckelmann, Gregor

INTERNATIONAL SEARCH REPORT

International application No

PCT/JP2020/030440

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 2015/061076 A1 (CHENG KANGGUO [US] ET AL) 5 March 2015 (2015-03-05) paragraphs [0038] - [0056]; figures 1-5 -----	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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