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(54) Title: NON-ETCH GAS COOLED EPITAXIAL STACK FOR GROUP IIIA-N DEVICES

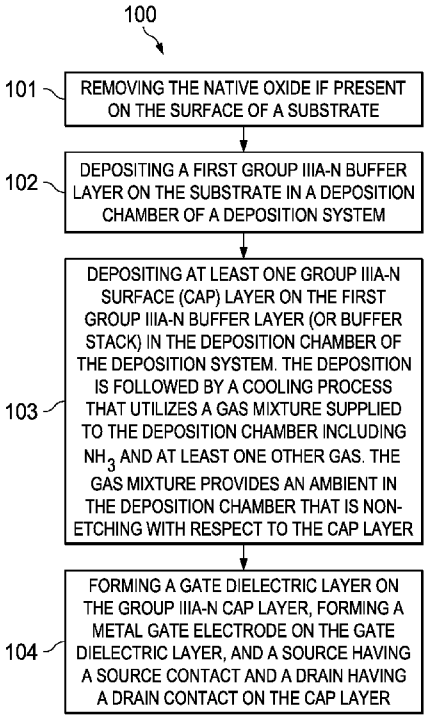

FIG. 1

(57) Abstract: In described examples, a method (100) of fabricating an epitaxial stack for Group IIIA-N transistors includes depositing (102) at least one Group IIIA-N buffer layer on a substrate in a deposition chamber of a deposition system. At least one Group IIIA-N cap layer is then deposited (103) on the first Group IIIA-N buffer layer. During a cool down from the deposition temperature for the cap layer deposition, the gas mixture supplied to the deposition chamber includes NH_3 and at least one other gas. The gas mixture provide an ambient in the deposition chamber that is non-etching with respect to the cap layer, so that at a surface of the cap layer: (a) a root mean square (rms) roughness is < 10 Å; and (b) a pit density for pits greater than (>) 2 nm deep is less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm.

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NON-ETCH GAS COOLED EPITAXIAL STACK FOR GROUP IIIA-N DEVICES

[0001] This relates to Group IIIA-N (e.g., GaN) field effect transistors (FETs), and more particularly to buffer layers for such FETs.

BACKGROUND

[0002] Gallium-nitride (GaN) is a commonly used Group IIIA-N material, where Group IIIA elements (such as Ga, boron, aluminum, indium, and thallium) are also sometimes referred to as Group 13 elements. GaN is a binary IIIA/V direct bandgap semiconductor that has a Wurtzite crystal structure. Its relatively wide band gap of 3.4 eV at room temperature (versus 1.1 eV for silicon) gives it special properties for a wide variety of applications in optoelectronics, high-power devices and high-frequency electronic devices.

[0003] Because GaN and silicon have significant thermal expansion coefficient mismatches, buffer layer(s) are commonly used between the silicon substrate and the GaN layer for strain management. This buffer technology forms the basis of most GaN-on-Si technology commonly used for high-electron-mobility transistor (HEMT), also known as heterostructure FET (HFET) or modulation-doped FET (MODFET) devices, which are field-effect transistors incorporating a junction between two materials with different band gaps (i.e. a heterojunction) as the channel instead of a doped region (as is generally the case for a MOSFET). Some buffer arrangements for such devices use either super lattice structures or a graded buffer structure.

[0004] A GaN cap layer deposition follows the deposition of at least one buffer layer. Conventional buffer layer and cap layer deposition processes use NH_3 and H_2 during the cool down from their respective deposition temperatures. The H_2 volume flow rate is generally several times the NH_3 volume flow rate.

SUMMARY

[0005] In described examples, a method of fabricating an epitaxial stack for Group IIIA-N transistors includes depositing at least one Group IIIA-N buffer layer on a substrate in a deposition chamber of a deposition system. At least one Group IIIA-N cap layer is then deposited on the first Group IIIA-N buffer layer. During a cool down from the deposition temperature for the cap layer deposition, the gas mixture supplied to the deposition chamber

includes NH_3 and at least one other gas. The gas mixture provide an ambient in the deposition chamber that is non-etching with respect to the cap layer, so that at a surface of the cap layer: (a) a root mean square (rms) roughness is < 10 Å; and (b) a pit density for pits greater than (>) 2 nm deep is less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a flow chart of steps in an example method of fabricating an epitaxial layer stack including at least one low defect density cap layer for a power group IIIA-N transistor, according to an example embodiment.

[0007] FIG. 2 is a cross sectional depiction of an example device stack that includes a Group IIIA-N buffer layer with a low defect density cap layer thereon, according to an example embodiment.

[0008] FIG. 3A is a cross sectional view of an example depletion-mode high-electron-mobility transistor (HEMT) with an epitaxial layer stack having a low defect density cap layer, according to an example embodiment.

[0009] FIG. 3B is a cross sectional view of an example enhancement-mode HEMT with a normally off gate with an epitaxial layer stack having a low defect density cap layer, according to an example embodiment.

[0010] FIG. 3C is a cross sectional view of an example IC including the depletion mode HEMT power device shown in FIG. 3A and the enhancement-mode HEMT shown in FIG. 3B both on the same low defect density cap layers on a buffer stack.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] The drawings are not necessarily drawn to scale. In the drawings, like reference numerals designate similar or equivalent elements. Some illustrated acts or events may occur in different order and/or concurrently with other acts or events. Furthermore, some illustrated acts or events may not be required to implement a methodology in accordance with this description.

[0012] Example embodiments recognize that the conventional NH3 and H2 gas mixture supplied to the deposition chamber during the cool down after epitaxial Group IIIA-N cap layer depositions for Group IIIA-N devices results in pits in the cap layer upon the cooling, which can be worsened after subsequent etching/cleaning where preferential etching can take place. H2 can attack Group IIIA-N cap layers (such as GaN or AlGaN) causing pits. Defects (such as pits) in the cap layer result in defects in the power transistor and, if they exist in a high enough density,

they can result in device failures.

[0013] In described examples, cap layer depositions follow the deposition of at least one buffer layer on a substrate with a cooling process that uses a supplied gas mixture including NH3 and at least one other gas, where the gas mixture provides an ambient in the deposition chamber that is non-etching with respect to the first Group IIIA-N layer. As used herein "non-etching" refers a resulting surface of the cap layer having: (a) a root mean square (rms) roughness of < 10 Å; and (b) a pit density for pits layer greater than (>) 2 nm deep less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm. One example uses a gas mixture during cooldown with only NH3 and N2.

[0014] FIG. 1 is a flow chart of steps in an example method 100 of fabricating an epitaxial layer stack including a low defect density cap layer for a Group IIIA-N power transistor, according to an example embodiment. All respective buffer and Group IIIA-N cap layers can be epitaxially deposited in a single run using a metal-organic chemical vapor deposition (MOCVD) system, molecular beam epitaxy (MBE) system, or hydride vapor phase epitaxy (HVPE) system.

[0015] Step 101 comprises removing the native oxide if present on the surface of the substrate (e.g., wafer). The substrate can comprise sapphire, silicon or silicon carbide (SiC).

[0016] Step 102 comprises depositing at least a first Group IIIA-N buffer layer on the substrate in a deposition chamber of a deposition system, using a deposition temperature generally from 1050 °C to 1300 °C. The buffer layer(s) can be 1 micron to 10 microns thick. The Group IIIA-N buffer layer(s) and cap layers described herein may be represented by the general formula AlxGayIn1-x-yN, where $0<x\leq 1$, $0\leq y\leq 1$, $0<x+y\leq 1$. For example, the Group IIIA-N layer can comprise at least one of AlN, AlGaN, AlInN, and AlInGaN. Other Group IIIA elements such as boron (B) may be included, and N may be partially replaced by phosphorus (P), arsenic (As), or antimony (Sb). Each of the Group IIIA nitride compound semiconductors may contain an optional dopant selected from Si, C, Ge, Se, O, Fe, Mn, Mg, Ca, Be, Cd, and Zn.

[0017] The buffer layer deposition(s) can optionally be followed by a cooling process cooling from the higher buffer layer deposition temperature (e.g., 1250 °C) to the lower deposition temperature of the cap layer deposition, such as 900 °C to 1050 °C, that uses a gas mixture supplied to the deposition chamber including NH3 and at least one other gas, where the gas mixture provides an ambient in the deposition chamber that is non-etching with respect to the first Group IIIA-N buffer layer. The ramp down rate during this cooling process is generally

5 °C/min to 40 °C/min. The other gas can be N2, Ar, He, Ne, Kr and or a combination of such gases. In one particular embodiment NH3 is supplied at 2 to 20 liters/min and N2 is supplied at 50 to 150 liters/min. Hydrogen (H2) may be provided up to about 40% by volume H2 provided the mixture remains non-etching.

[0018] Following step 102 the method can comprise optionally depositing at least a second Group IIIA-N buffer layer on the first Group IIIA-N buffer layer to form a buffer stack. The other buffer layer deposition step(s) can use the same process low defect density deposition process as step 102 described hereinabove including the described cooling process.

[0019] Step 103 comprises depositing at least one Group IIIA-N cap layer on the first Group IIIA-N buffer layer (or buffer stack). As described hereinabove, the cap layer deposition temperature is generally from 900 °C to 1050 °C.

[0020] The cap layer deposition is followed by a cooling process from the deposition temperature to a temperature generally from 300 °C to 550 °C that uses a gas mixture including NH3 and at least one other gas, where the gas mixture provides an ambient in the deposition chamber that is non-etching with respect to the cap layer. As described hereinabove, "non-etching" here refers to a resulting cap layer having: (a) a root mean square (rms) roughness of < 10 Å; and (b) a pit density for pits layer greater than (>) 2 nm deep less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm. Surface roughness may be measured by an atomic force microscopy (AFM) system, while the pit density may be measured by a defect analysis tool such as the KLA-Tencor CANDELA® 8620 Inspection System.

[0021] The other gas can be N2, Ar, He, Ne, Kr and or a combination of such gases. In one particular embodiment NH3 is supplied at 2 to 20 liters/min and N2 is supplied at 50 to 150 liters/min. Hydrogen (H2) may be provided up to about 40% by volume H2 provided the mixture remains non-etching. The ramp down rate during this cooling process is generally 5 °C/min to 40 °C/min, and as described hereinabove can cool down to a temperature of 300 °C to 550 °C, where the deposition chamber is vented to atmosphere and the boat of wafers is then generally removed from the deposition chamber.

[0022] Step 104 comprises forming a gate dielectric layer (e.g., SiN, SiON, Al2O3, AlN, silicon oxide or combination of any of these layers) on the cap layer, forming a metal gate electrode on the gate dielectric layer, and a source having a source contact and a drain having a drain contact on the cap layer. The gate electrode can comprise a TiW alloy in one embodiment.

The source and drain can be formed by sputtering a metal stack such as Ti/Al/TiN in one particular embodiment.

[0023] FIG. 2 is a cross sectional depiction of an example device stack 200 that includes a multi-layer buffer stack (buffer layer stack) 220 comprising a first Group IIIA-N buffer layer 220a and a second group IIIA-N buffer layer 220b both shown as AlN layers on a substrate (e.g., silicon) 210, according to an example embodiment. A Group IIIA-N cap layer 230 shown as a GaN layer is on the second Group IIIA-N buffer layer 220b, where the Group IIIA-N cap layer 230 has a low defect density formed using a cap layer cool down process using an ambient in the deposition chamber during cooling that is non-etching with respect to the cap layer. In another arrangement the first Group IIIA-N buffer layer 220a comprises AlN, the second group IIIA-N buffer layer 220b comprises GaN, and the Group IIIA-N cap layer 230 comprises AlGaN. Example thickness ranges for the Group IIIA-N cap layer 230 can be 5Å to 300Å which can be used as a HEMT layer, 50Å to 300Å for the second Group IIIA-N buffer layer 220b, and 0.1 μm to 5 μm for the first Group IIIA-N buffer layer 220a.

[0024] Advantages of example embodiments include the ability to deposit an essentially void and crack-free epitaxial GaN film stack including an essentially void and crack-free cap layer to enable obtaining higher transistor breakdown voltage, lower leakage current, and reduced substrate bow/warp. For example, power transistors can provide a breakdown voltage of at least of 100V at a leakage current density of 1 μamp per mm2.

[0025] Examples of power semiconductor devices that can use described epitaxial stacks include HEMT, double heterostructure field effect transistors (DHFETs), heterojunction bipolar transistors (HBTs) and bipolar junction transistors (BJTs). An HEMT, also known as heterostructure FET (HFET) or modulation-doped FET (MODFET), is a field-effect transistor incorporating a junction between two semiconductor materials with different band gaps (i.e. a heterojunction) as the two dimensional electron gas (2DEG) channel layer instead of a doped region (as is generally the case for a metal–oxide–semiconductor field-effect transistor (MOSFET)). The HEMT includes a compound semiconductor having a wide band gap such as GaN and AlGaN. Due to high electron saturation velocity in GaN and IIIA-N materials systems, the electron mobility in GaN HEMT is higher than that of other general transistors such as metal oxide semiconductor field effect transistors (MOSFETs).

[0026] FIG. 3A is a cross sectional view of an example depletion-mode HEMT power device

300 with a described epitaxial stack shown including a Group IIIA-N cap layer 230' on a buffer layer stack 220 on a substrate 210, according to an example embodiment. HEMT power device 300 is shown having a gate dielectric layer 235 such as comprising silicon nitride or silicon oxynitride. The Group IIIA-N cap layer 230' is a low defect density cap layer, with a surface of the Group IIIA-N cap layer 230' having: (a) a root mean square (rms) roughness of < 10 Å; and (b) a pit density for pits layer greater than (>) 2 nm deep less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm. In this embodiment, the Group IIIA-N cap layer 230' can comprise an AlGaN layer 230b sandwiched between a topmost (first) GaN layer 230c and bottommost (second) GaN layer 230a that is on the second Group IIIA-N buffer layer 220b. The topmost and bottommost GaN layers 230c, 230a generally each have a doping concentration between 1 x 1015 cm-3 and 1 x 1018 cm-3. The dopants can include carbon, magnesium, silicon, or zinc, or combination of such dopants.

[0027] HEMT power device 300 can be a discrete device, or one of many devices on an IC. More generally, the Group IIIA-N cap layer 230' may include one or more of GaN, InN, AlN, AlGaN, AlInN, InGaN, and AlInGaN. As described hereinabove, the Group IIIA-N layers can include other Group IIIA elements such as B, and N may be partially replaced by P, As, or Sb, and may also contain an optional dopant. In another specific example, the Group IIIA-N cap layer 230' can comprise a GaN layer on top of an AlxGayN layer or an InxAlyN layer. Yet another specific example is the Group IIIA-N cap layer 230' being a tri-layer stack can comprise GaN on InAlN on AlGaN.

[0028] HEMT power device 300 includes a source 241, a drain 242, and a gate electrode 240. Gate electrode 240 is positioned between the source 241 and drain 242, closer to the source 241 than the drain 242. The source 241, drain 242, and gate electrode 240 may be formed of metals and/or metal nitrides, but example embodiments are not limited thereto.

[0029] FIG. 3B is a cross sectional view of an example enhancement-mode HEMT power device 350 with a normally off gate with a Group IIIA-N cap layer 230' on a buffer layer shown as a buffer layer stack 220 on a substrate 210, according to an example embodiment. The Group IIIA-N cap layer 230' is a low defect density cap layer, with a surface of the Group IIIA-N cap layer 230' having: (a) a root mean square (rms) roughness of < 10 Å; and (b) a pit density for pits layer greater than (>) 2 nm deep less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm. In this embodiment, the gate electrode is a p-doped gate

electrode 245 (shown as a p-GATE ELECTRODE) that is in direct contact with the Group IIIA-N cap layer 230c (e.g., GaN layer). FIG. 3C is a cross sectional view of an example IC 380 including the depletion mode HEMT power device 300 shown in FIG. 3A and the enhancement-mode HEMT shown in FIG. 3B both using the same cap layers and buffer stack.

[0030] Example embodiments are further illustrated by the following examples.

[0031] AFM data was taken for a cap layer on a Si substrate formed using a NH3/N2 cap layer cooldown as compared to a known cap layer formed using a NH3/H2 gas mixture for the cap layer cooldown. In one example, the NH3/N2 flow ratios are 1:10 with flow ranging from 2 to 20 liters/min of NH3 and N2 in the range of 50 to150 liters/min. As deposited, the wafers processed with the described NH3/N2 cap layer cool down consistently showed no surface pits with data from wafers from several different runs. In contrast, the wafers processed with the known NH3/H2 cap layer cool down consistently showed surface pits 1 x 1010 per cm2 with sizes ranging from 10 nm to 200 nm with data taken from wafers from several different runs.

[0032] It was also found pits in the cap layer can be worsened after subsequent etching/cleaning where preferential etching at the defect sites was found to take place. Wafers with cap layers from a NH3/N2 cooled cap layer process and a known cap layer formed using a N2/H2 gas mixture for the cap layer cooldown were submitted for two sets of cleaning process. AFM analysis was performed on wafers for both cap layer processes. For wafers with a cap layer from a NH3/N2 cooled cap layer the depth of the pits as deposited were at about 0.7 nm to 1 nm, which remained at about 0.7 nm to 1 nm deep after the two sets of cleaning processes. For wafers with a cap layer from the known NH3/H2 cooled process the depth of the pits as deposited were at about 1 nm to 3 nm, which increased to 6 nm to 10 nm deep after the two sets of cleaning processes.

[0033] High-temperature-reverse-bias (HTRB) HEMT device data was obtained where the cap layer comprised GaN and the buffer layer comprised AlGaN formed using a N2/NH3 cap layer cooldown along with control GaN cap layer formed using a known NH3/H2 cap layer cooldown.

[0034] HTRB failures were associated with reliability fails due to GaN cap layer pits. HEMTs having a control GaN cap layer formed using a known N2/H2 cap layer cooldown had a burn-in failure rate of 5 % to 10%, while HEMTs having a GaN cap layer formed using a NH3/N2 cap layer cool down had a failure rate of < 2% HTRB fails.

[0035] Example embodiments are useful to form semiconductor die that may be integrated

into a variety of assembly flows to form a variety of different devices and related products. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, and conductive vias. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, insulated gate bipolar transistor (IGBT), CMOS, BiCMOS and MEMS.

[0036] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method of fabricating an epitaxial stack for Group IIIA-N transistors, the method comprising:

depositing at least a first Group IIIA-N buffer layer on a substrate in a deposition chamber of a deposition system, and

depositing at least one Group IIIA-N surface cap layer (cap layer) on the first Group IIIA-N buffer layer in the deposition chamber of the deposition system followed by a cooling process to $\leq$ 550 °C that uses a gas mixture supplied to the deposition chamber including NH_3 and at least one other gas, wherein the gas mixture provides an ambient in the deposition chamber that is non-etching with respect to the cap layer, so that at a surface of the cap layer: (a) a root mean square (rms) roughness is < 10 Å; and (b) a pit density for pits greater than (>) 2 nm deep is less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm.

2. The method of claim 1, wherein the depositing the first Group IIIA-N buffer layer is followed by the cooling process before the depositing the Group IIIA-N cap layer.

3. The method of claim 1, wherein the deposition system comprises a metal-organic chemical vapor deposition (MOCVD) system, molecular beam epitaxy (MBE) system, or a hydride vapor phase epitaxy (HVPE) system.

4. The method of claim 1, wherein a thickness of the Group IIIA-N cap layer is 3 nm to 50 nm.

5. The method of claim 1, wherein the first Group IIIA-N buffer layer and the cap layer both comprises GaN or AlGaN.

6. The method of claim 1, wherein the substrate comprises sapphire, silicon, or silicon carbide (SiC).

7. The method of claim 1, wherein the gas mixture consists of N_2 and NH_3.

8. The method of claim 1, further comprising:

forming a gate dielectric layer on the cap layer;

forming a metal gate electrode on the gate dielectric layer, and

forming a source having a source contact to the cap layer and a drain having a drain contact to the cap layer.

9. The method of claim 1, wherein the gas mixture is exclusive of H_2.

10. A power transistor device, comprising:

a substrate;

at least a first Group IIIA-N buffer layer on the substrate, and

at least one Group IIIA-N surface cap layer (cap layer) on the first Group IIIA-N buffer layer,

wherein a surface of the cap layer has: (a) a root mean square (rms) roughness of < 10 Å; and (b) a pit density for pits layer greater than (>) 2 nm deep less than (<) 10 pits per square μm with an average pit diameter less than (<) 0.05 μm;

a source having a source contact to the cap layer and a drain having a drain contact to the cap layer, and

a gate electrode on a gate dielectric on the cap layer.

11. The power transistor device of claim 10, wherein the substrate comprises sapphire, silicon, or silicon carbide (SiC).

12. The power transistor device of claim 10, wherein the first Group IIIA-N buffer layer and the cap layer both comprises GaN or AlGaN.

13. The power transistor device of claim 10, wherein the power transistor device comprises a High-electron-mobility transistor (HEMT).

14. The power transistor device of claim 10, wherein a thickness of the cap layer is 3 nm to 50 nm.

15. The power transistor device of claim 10, wherein the cap layer comprises depositing a Group IIIA-N tri-layer stack including a AlGaN layer sandwiched between a first GaN layer and a second GaN layer, wherein the first GaN layer and the second GaN layer both have a doping concentration between 1×10^{15} cm^{-3} and 1×10^{18} cm^{-3}.

16. The power transistor device of claim 10, wherein the first Group IIIA-N buffer layer comprises GaN on AlN, and wherein the cap layer comprises AlGaN.

17. The power transistor device of claim 10, wherein the power transistor device includes at least one enhancement-mode high-electron-mobility transistor (HEMT) and at least one depletion-mode HEMT both on the first Group IIIA-N buffer layer.

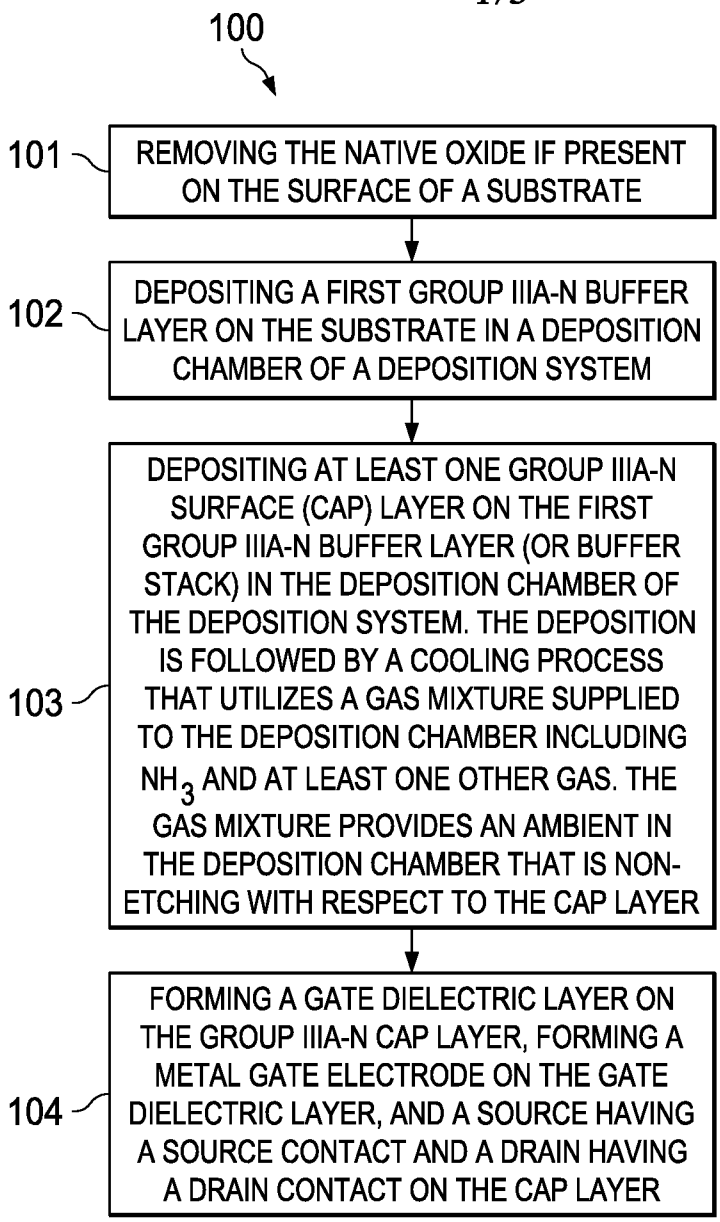
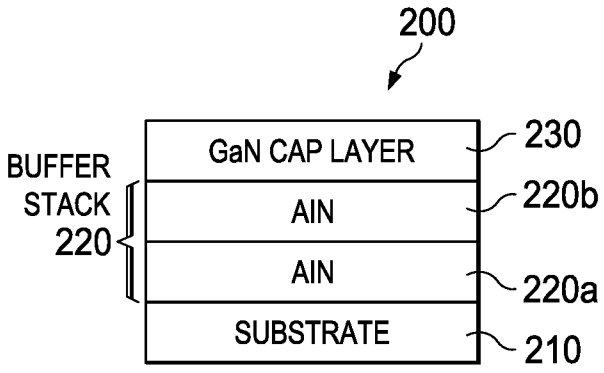

100
101
REMOVING THE NATIVE OXIDE IF PRESENT ON THE SURFACE OF A SUBSTRATE
102
DEPOSITING A FIRST GROUP IIIA-N BUFFER LAYER ON THE SUBSTRATE IN A DEPOSITION CHAMBER OF A DEPOSITION SYSTEM
103
DEPOSITING AT LEAST ONE GROUP IIIA-N SURFACE (CAP) LAYER ON THE FIRST GROUP IIIA-N BUFFER LAYER (OR BUFFER STACK) IN THE DEPOSITION CHAMBER OF THE DEPOSITION SYSTEM. THE DEPOSITION IS FOLLOWED BY A COOLING PROCESS THAT UTILIZES A GAS MIXTURE SUPPLIED TO THE DEPOSITION CHAMBER INCLUDING NH_3 AND AT LEAST ONE OTHER GAS. THE GAS MIXTURE PROVIDES AN AMBIENT IN THE DEPOSITION CHAMBER THAT IS NON-ETCHING WITH RESPECT TO THE CAP LAYER
104
FORMING A GATE DIELECTRIC LAYER ON THE GROUP IIIA-N CAP LAYER, FORMING A METAL GATE ELECTRODE ON THE GATE DIELECTRIC LAYER, AND A SOURCE HAVING A SOURCE CONTACT AND A DRAIN HAVING A DRAIN CONTACT ON THE CAP LAYER

FIG. 1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GaN CAP LAYER
230
BUFFER STACK 220
AlN
220b
AlN
220a
SUBSTRATE
210

FIG. 2

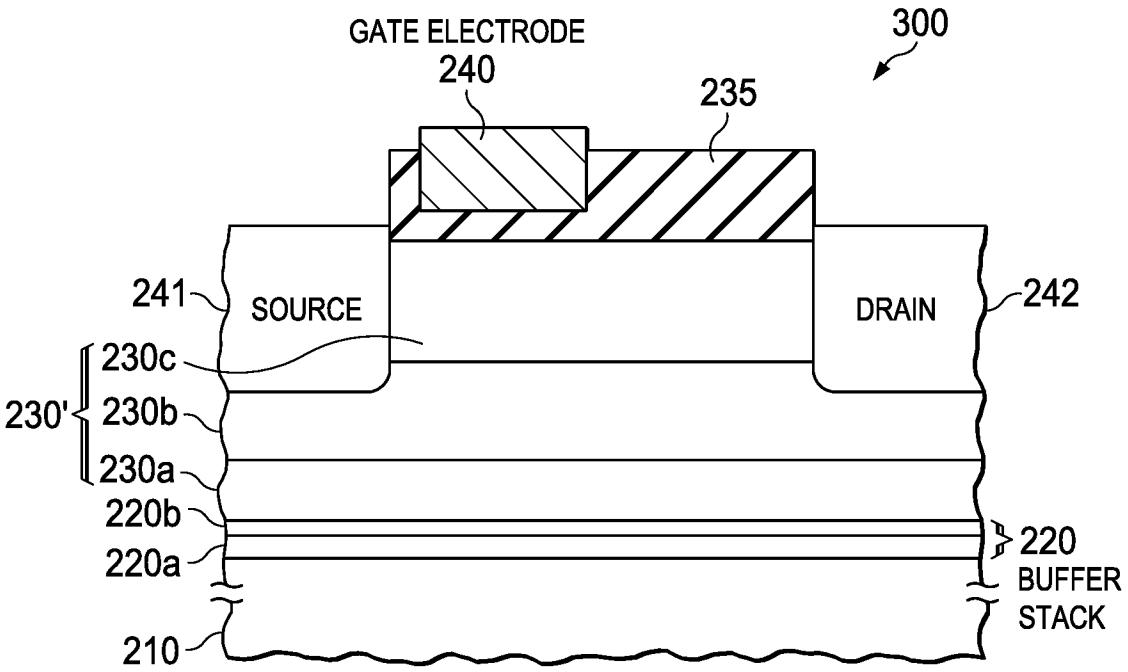
GATE ELECTRODE
240
300
235
241
SOURCE
DRAIN
242
230'
230c
230b
230a
220b
220a
220
BUFFER
STACK
210

FIG. 3A

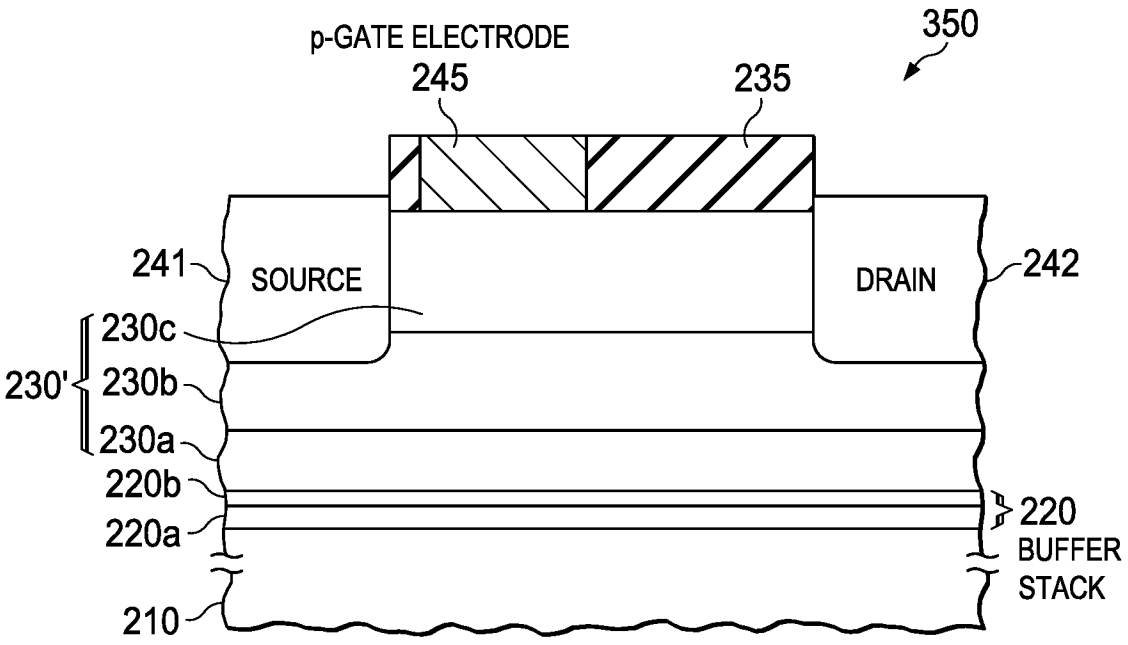
p-GATE ELECTRODE
245
350
235
241
SOURCE
DRAIN
242
230'
230c
230b
230a
220b
220a
220
BUFFER
STACK
210

FIG. 3B

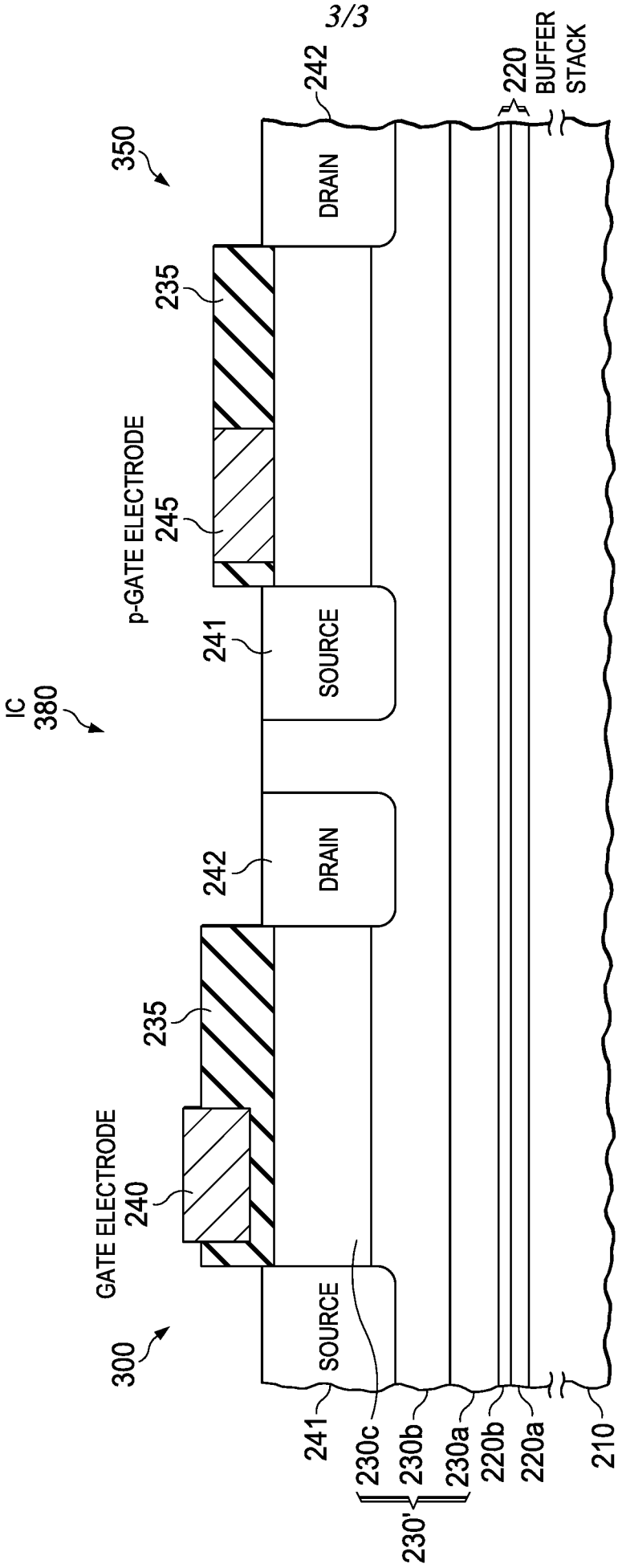
IC
380
350
300
242
DRAIN
220
BUFFER
STACK
235
p-GATE ELECTRODE
245
241
SOURCE
242
DRAIN
235
GATE ELECTRODE
240
SOURCE
241
230c
230b
230a
230'
220b
220a
210

FIG. 3C

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/069051

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/335 *(2006.01)*
H01L 21/20 *(2006.01)*
H01L 29/772 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00-21/335, 29/00-29/772

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/0108887 A1 (NITEK, INC.) 12.05.2011	1-17
A	US 2012/0223328 A1 (DOWA ELECTRONICS MATERIALS CO., LTD.) 06.09.2012	1-17
A	US 2015/0357419 A1 (AZURSPACE SOLAR POWER GMBH) 10.12.2015	1-17
A	US 2002/0175337 A1 (AXT, INC.) 28.11.2002	1-17
A	US 2014/0094223 A1 (SANSAPTAK DASGUPTA et al.) 03.04.2014	1-17

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 March 2017 (29.03.2017)	13 April 2017 (13.04.2017)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer I. Baginskaya Telephone No. (499) 240-25-91

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