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(54) MFOS MEMORY TRANSISTOR

(75) Inventors: **Sheng Teng Hsu**, Camas, WA (US); **Fengyan Zhang**, Vancouver, WA (US); **Tingkai Li**, Vancouver, WA (US)

Correspondence Address:
Matthew D. Rabdau
Patent Attorney
Sharp Laboratories of America, Inc.
5750 NW Pacific Rim Boulevard
Camas, WA 98607 (US)

(73) Assignee: **Sharp Laboratories of America, Inc.**

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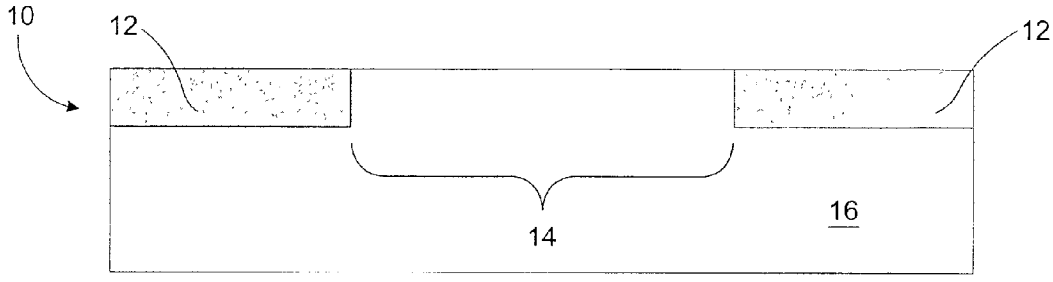
(57) **ABSTRACT**

A ferroelectric transistor gate structure with a ferroelectric gate and passivation sidewalls is provided. The passivation sidewalls serve as an insulator to reduce, or eliminate, the diffusion of oxygen or hydrogen into the ferroelectric gate. A method of forming the ferroelectric gate structure is also provided. The method comprises the steps of forming a sacrificial gate structure, removing the sacrificial gate structure, depositing passivation insulator material, etching the passivation insulator material using anisotropic plasma etching to form passivation sidewalls, depositing a ferroelectric material, polishing the ferroelectric material using CMP, and forming a top electrode overlying the ferroelectric material.



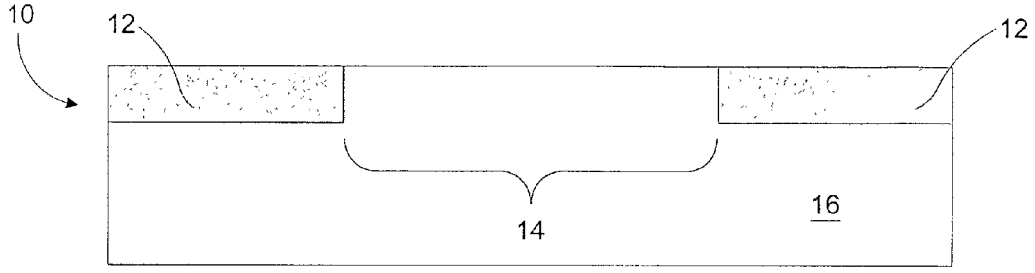


FIG. 1

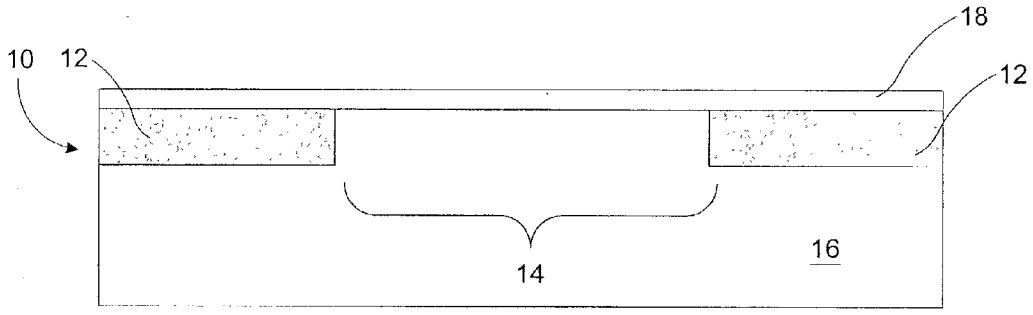


FIG. 2

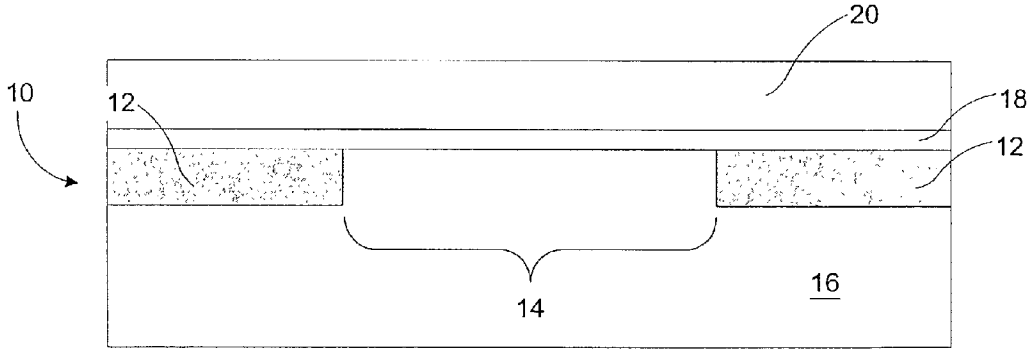


FIG. 3

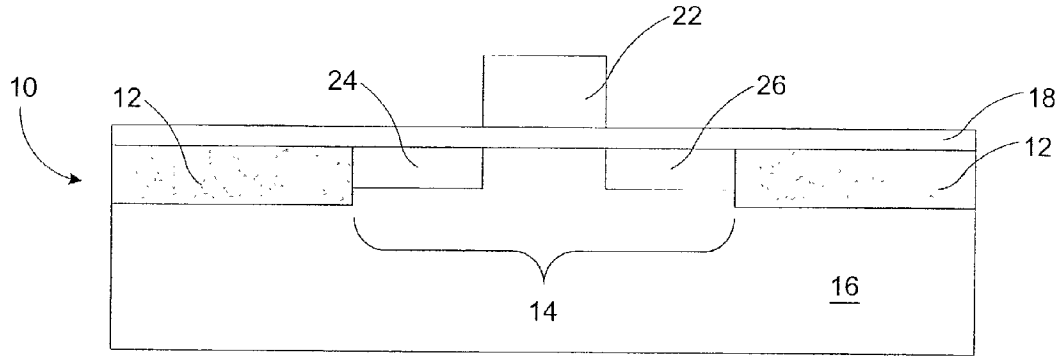


FIG. 4

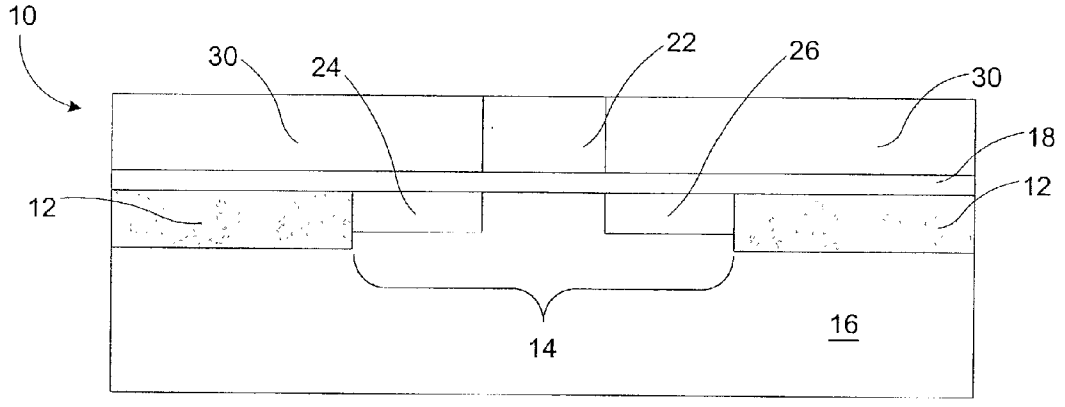


FIG. 5

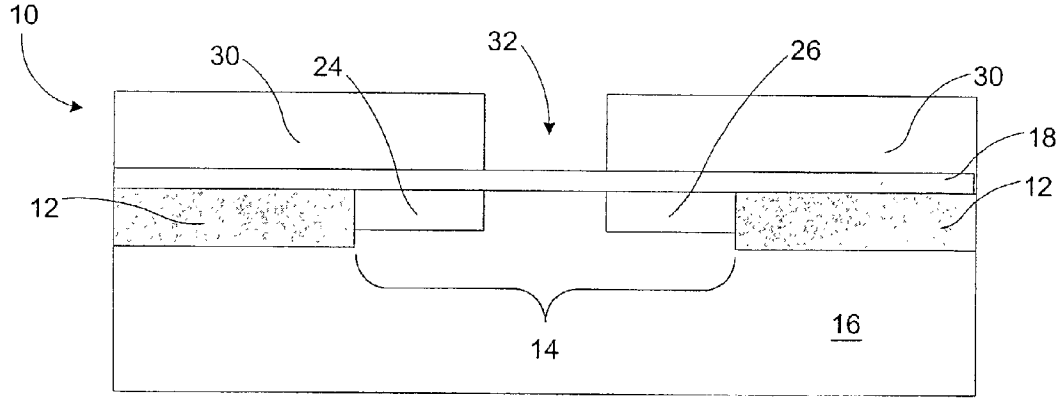


FIG. 6

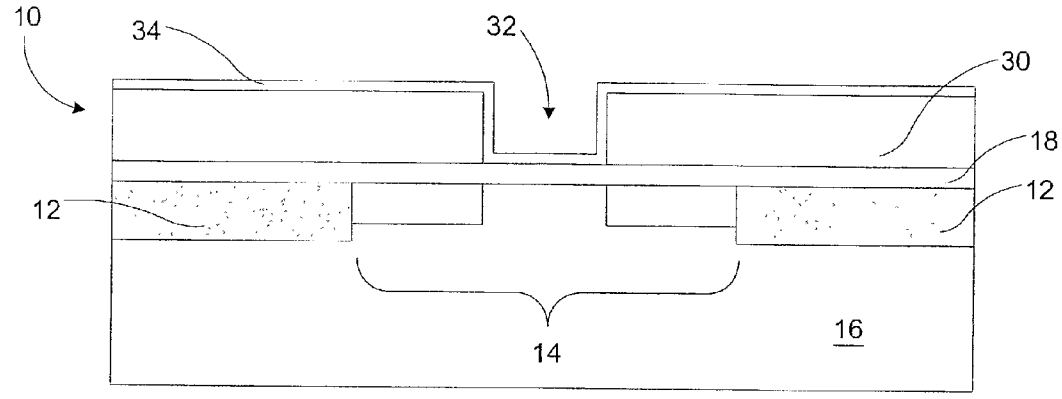


FIG. 7

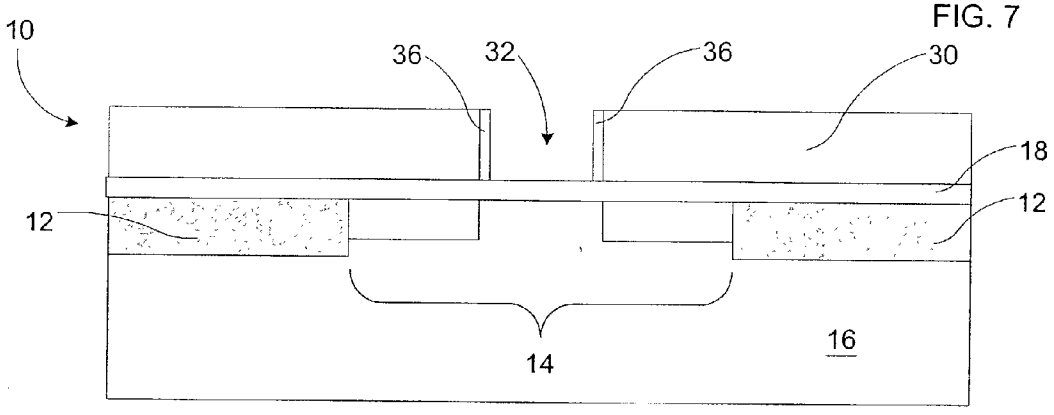


FIG. 8

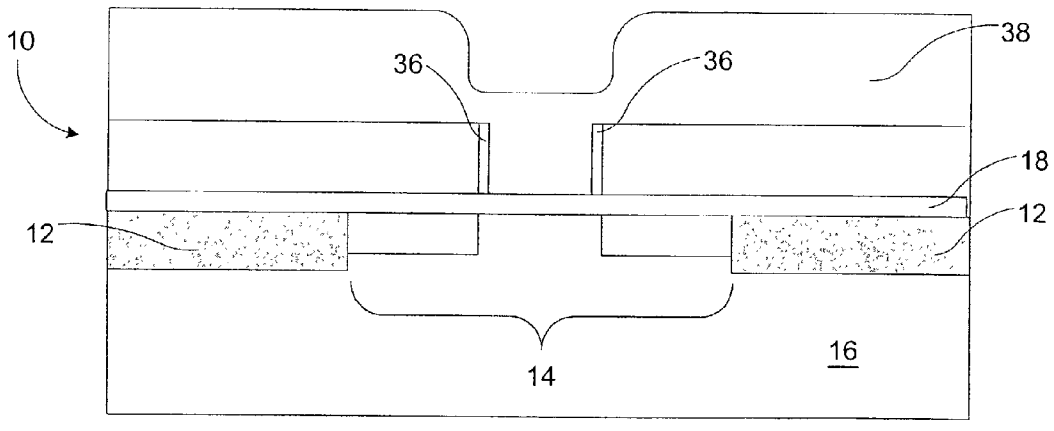


FIG. 9

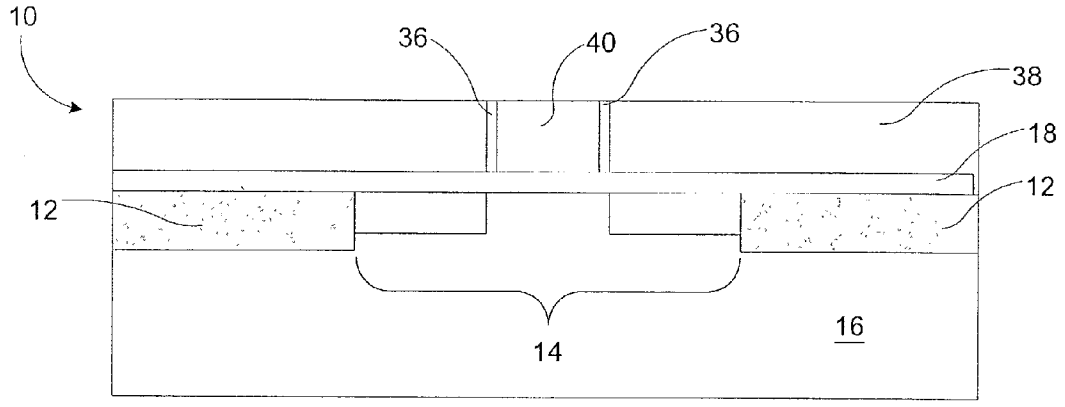


FIG. 10

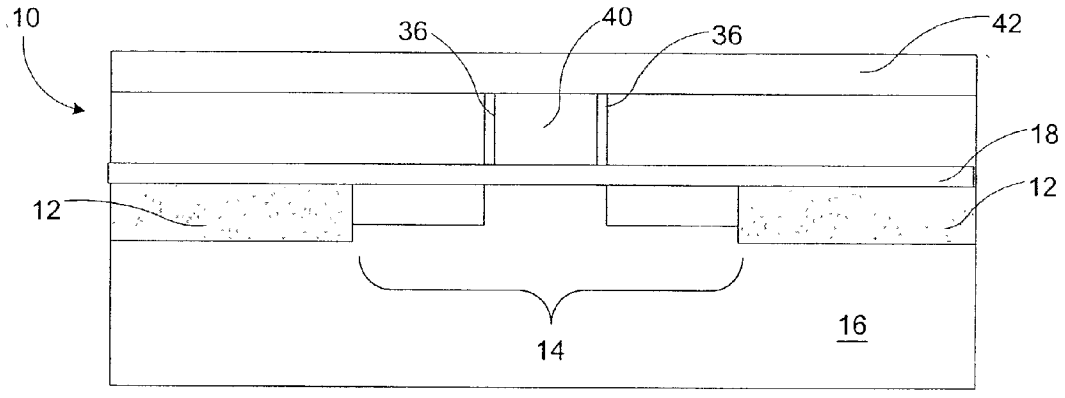


FIG. 11

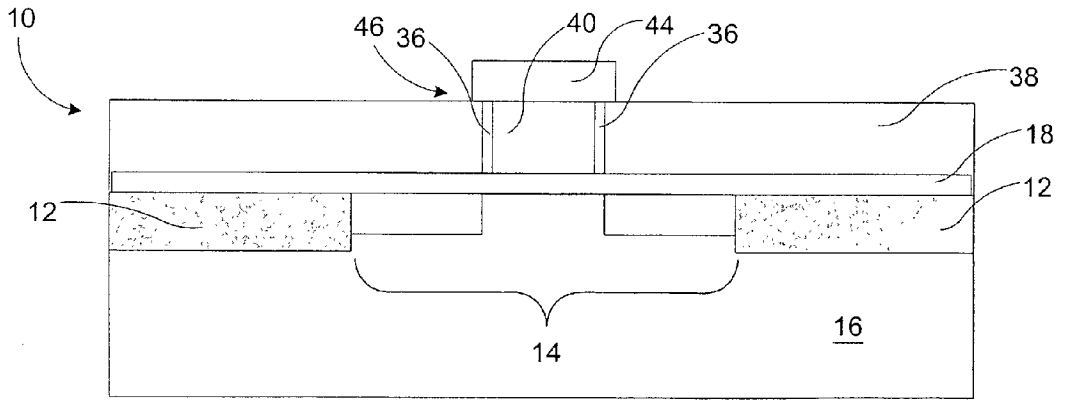


FIG. 12

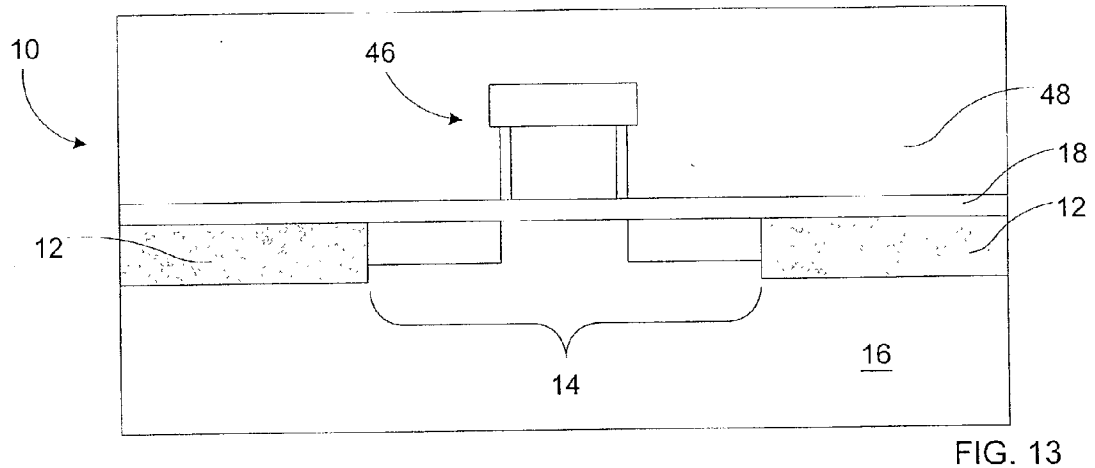


FIG. 13

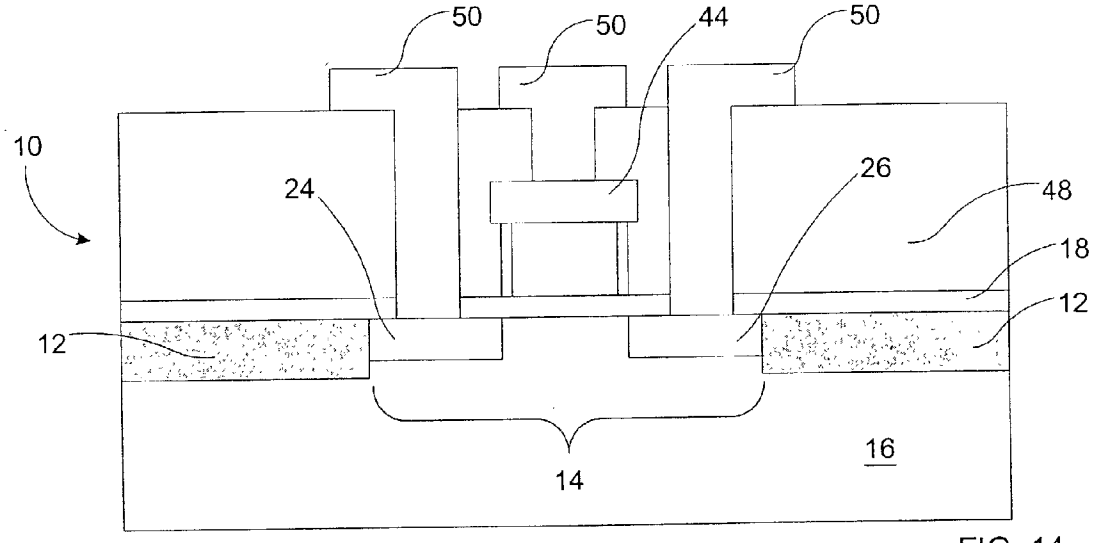


FIG. 14

MFOS MEMORY TRANSISTOR

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to semiconductor technology and more particularly to metal-ferroelectric-insulator semiconductor (MFIS) transistor structures, and methods of fabrication. An MFIS transistor is similar to an MFOS transistor, but is not limited to structures that use oxide as the insulator material.

[0002] Previously, single transistor ferroelectric memory transistors have utilized a ferroelectric electrode stack, comprising a ferroelectric gate with a top electrode. The device would be formed by depositing a ferroelectric material, followed by an overlying metal layer. The layers would then be plasma etched. Plasma etching degrades the ferroelectric properties of the ferroelectric gate, thereby reducing the reliability of the memory transistor. The ferroelectric material also needed to be passivated to prevent contamination from hydrogen. Passivation was also used to reduce unwanted interactions between the ferroelectric material and underlying oxide.

SUMMARY OF THE INVENTION

[0003] A ferroelectric transistor structure is provided comprising a ferroelectric gate overlying a semiconductor substrate. The ferroelectric gate has a bottom with a gate dielectric interposed between the bottom and the semiconductor substrate. The ferroelectric gate also has sides with adjacent passivation sidewalls, and a top covered with a top electrode. The top electrode, the passivation sidewalls and the gate dielectric serve to encapsulate the ferroelectric gate, thereby reducing, or eliminating, contamination due to oxygen, hydrogen or other contaminants.

[0004] A method of forming the ferroelectric gate structure of the present invention is also provided. A gate insulation material is formed over the substrate. A sacrificial gate structure is formed overlying the gate insulation material and removed to produce an open gate region. A passivation insulator is deposited over the substrate, including the open gate region. The passivation insulator is anisotropic plasma etched to form passivation sidewalls. A ferroelectric material is deposited over the substrate including the open gate region and then polished using CMP. A top electrode is then formed over the remaining ferroelectric material. The combination of the top electrode, the passivation sidewalls and the gate insulation serve to encapsulate and protected the ferroelectric material.

[0005] The gate insulator is preferably ZrO_2, zirconium silicate, Zr—Al—Si—O, HfO_2, hafnium silicate, Hf—Al—O, La—Al—O, lanthanum oxide Ta_2O_5, or other suitable high-k material. However, the gate insulator may also be silicon nitride, nitrogen implanted silicon dioxide, or silicon oxynitride.

[0006] The passivation sidewalls are preferably TiO_2, Al_2O_3, $TiAlO_x$, or Si_3N_4

[0007] The ferroelectric material is preferably PGO, PZT, SBT, SBO, SBTO, SBTN, STO, BTO, BLT, LNO, $YMnO_3$, or other suitable material.

[0008] The top electrode is preferably iridium, platinum, ruthenium, iridium oxide, platinum oxide, ruthenium oxide, or other suitable material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **FIG. 1** is a cross-sectional view of a semiconductor substrate ready for further processing.

[0010] **FIG. 2** is a cross-sectional view of the semiconductor substrate with a dielectric layer overlying the substrate.

[0011] **FIG. 3** is a cross-sectional view of the semiconductor substrate with a sacrificial layer overlying the dielectric layer.

[0012] **FIG. 4** is a cross-sectional view of the semiconductor substrate with a sacrificial gate structure overlying the dielectric layer.

[0013] **FIG. 5** is a cross-sectional view of the semiconductor substrate with the sacrificial gate structure surrounded by oxide.

[0014] **FIG. 6** is a cross-sectional view of the semiconductor substrate after the sacrificial gate is removed.

[0015] **FIG. 7** is a cross-sectional view of the semiconductor substrate following deposition of a passivation insulator layer.

[0016] **FIG. 8** is a cross-sectional view of the semiconductor substrate following anisotropic plasma etching of the passivation insulator layer.

[0017] **FIG. 9** is a cross-sectional view of the semiconductor substrate following deposition of a ferroelectric material layer.

[0018] **FIG. 10** is a cross-sectional view of the semiconductor substrate following chemical-mechanical polishing of the ferroelectric material layer.

[0019] **FIG. 11** is a cross-sectional view of the semiconductor substrate following deposition of a top electrode layer.

[0020] **FIG. 12** is a cross-sectional view of the semiconductor substrate showing a top electrode.

[0021] **FIG. 13** is a cross-sectional view of the semiconductor substrate with a passivation layer overlying device structures.

[0022] **FIG. 14** is a cross-sectional view of the semiconductor substrate showing metal contacts to the device structures.

DETAILED DESCRIPTION OF THE INVENTION

[0023] **FIG. 1** shows a semiconductor structure **10** that has been prepared using state of the art processes. Shallow trench isolation (STI) has been used to produce isolation regions **12**, and an active device region **14** on a substrate **16**. Although an STI structure is shown, it would also be possible to use LOCOS isolation instead of STI. The semiconductor substrate is preferably silicon or silicon on insulator (SOI).

[0024] **FIG. 2** shows the semiconductor structure **10** following formation of a gate insulation material **18**, which may also be referred to as the gate dielectric. The gate insulation material **18** is a metal oxide that does not react significantly with a ferroelectric material to be deposited in subsequent steps. Although, the gate insulation material may be silicon dioxide, nitrogen implanted silicon dioxide, silicon nitride or silicon oxynitride, the gate insulation material **18** is preferably a high-k material. Zirconium oxide (ZrO_2) is currently the preferred material. Although ZrO_2 is preferred, other suitable high-k materials including, zirconium silicate, Zr—Al—Si—O, HfO_2, hafnium silicate, Hf—Al—O, La—Al—O, lanthanum oxide and Ta_2O_5 may be used.

[0025] If the gate insulation material is a high-k material, the gate insulation material **18** is preferably deposited to an equivalent thermal oxide thickness of between 0.5 nm and 10 nm. The equivalent thermal oxide thickness may have an actual thickness greater than that of silicon dioxide due to higher dielectric constants associated with these materials. The gate insulation material is preferably deposited to a thickness of between approximately 1 nm and 100 nm.

[0026] A variety of methods are available for depositing the gate insulation material **18**. For silicon dioxide, the gate insulation material can be grown thermally and subsequently implanted as desired. In the case of other materials, which are deposited, the available deposition methods include chemical vapor deposition, including pulsed CVD, sputtering, or evaporation.

[0027] For example, ZrO_2 may be deposited using atomic layer deposition, also referred to as "pulsed CVD". Atomic layer deposition is used to deposit an extremely thin layer of material onto the substrate. Atomic layer deposition employs a chemical phenomenon known as chemisorption. In chemisorption, a material in a gas phase will adsorb to a surface saturating it, forming a monolayer. Most conventional deposition techniques employ physisorption processes, which produce multilayer deposition regions with a surface coverage that is purely statistical. By taking advantage of chemisorption, films can be grown that are extremely uniform in thickness and composition. For instance, ZrO_2 films have reportedly been grown this way on silicon by using zirconium chloride ($ZrCl_4$) to form the first monolayer, purging the system of $ZrCl_4$, and then exposing the surface to water vapor (H_2O). Other precursors for producing zirconium oxide layers include zirconium propoxide ($Zr(iOPr)_4$) and zirconium tetramethyl heptanedionato (Zr(t-mhd)4). Chemisorption occurs over a very limited range of temperature and pressures for a given gas-solid combination. For example, zirconium oxide has reportedly been deposited on silicon substrates at a temperature of 300 degrees Celsius using $ZrCl_4$ and H_2O. As the process produces a monolayer, thicker layers of zirconium oxide would be produced by adding additional monolayers.

[0028] ZrO_2 may also be deposited using the precursors identified above, as well as other precursors, in a more conventional CVD process.

[0029] An alternative deposition technique using conventional systems is to sputter targets to lay down a thin layer of high-k material. A sputtering target of high purity metal is used. A wafer is prepared and placed into a deposition chamber. The wafer is then heated to a temperature between room temperature and 500 degrees Celsius. A mixture of argon (Ar) and oxygen (O_2) is then introduced into the deposition chamber. A plasma with a sputtering power of between approximately 500 W and 5 kW is produced within the chamber. The zirconium shutter is opened to deposit zirconium over the wafer, and then closed. The presence of oxygen within the chamber will cause the target material to form ZrO_2 concurrently with the deposition on the wafer In another alternative embodiment of the deposition method of the present invention, evaporation of targets is used to deposit the thin layer. The basic process is substantially identical to the description provided above with regard to sputtering, except that instead of exposing the targets to a plasma, the targets are heated to a temperature of between approximately 1,000 and 2,000 degrees Celsius. As described above, shutters can be used to control the duration of the deposition.

[0030] **FIG. 3** shows a sacrificial layer **20** deposited overlying the gate insulation material **18**. The sacrificial layer is deposited to a thickness of between approximately 200 nm and 400 nm. The sacrificial layer is preferably silicon nitride or polysilicon. The sacrificial layer is preferably easy to remove by selective etching without affecting underlying or adjacent materials.

[0031] **FIG. 4** shows a sacrificial gate structure **22** formed by patterning the sacrificial layer using an overlying mask layer (not shown), and plasma etching the sacrificial layer. The plasma etch may stop at the gate insulation material. Alternatively, the plasma etch may partially, or completely, remove the gate insulation material from areas not covered by the mask pattern. A source region **24** and a drain region **26** are formed adjacent to the sacrificial gate structure **22**. The source region **24** and the drain region **26** may be formed by any state of the art process, but preferably by ion implantation.

[0032] **FIG. 5** shows the semiconductor structure **10** following deposition of an oxide layer **30**. The oxide layer **30** is deposited overlying the sacrificial gate structure and surrounding regions. The oxide layer **30** is deposited to a thickness at which the lowest portion of the oxide is at least as high as the sacrificial gate structure **22**. This thickness is preferably 1 to 2 times the height of the sacrificial gate structure **22** above the substrate **16**. Following deposition of the oxide layer it is polished using chemical-mechanical polishing (CMP) to expose the sacrificial gate structure **22**. The CMP process is preferably stopped at the top of the sacrificial gate structure **22**, without removing a significant portion of the sacrificial gate structure **22**.

[0033] **FIG. 6** shows the semiconductor structure **10** following removal of the sacrificial gate structure. The removal of the sacrificial gate structure leaves an open gate region **32**. The sacrificial gate structure is preferably removed using a wet etch process.

[0034] **FIG. 7** shows the semiconductor structure **10** following deposition of a passivation insulator **34**. The passivation insulator **34** is preferably selected from materials that will reduce, or eliminate, diffusion of oxygen or hydrogen through it. Preferred materials for forming the passivation insulator **34** are TiO_2, Al_2O_3, $TiAlO_x$, and Si_3N_4. The passivation insulator 34 may be deposited by sputtering or other suitable method known to one of ordinary skill in the art.

[0035] **FIG. 8** shows the semiconductor structure **10** following anisotropic plasma etching of the passivation insu-

lator **34**. The anisotropic etch removes the passivation insulator **34** from horizontal surfaces, leaving passivation sidewalls **36**.

[**0036**] **FIG. 9** shows the semiconductor structure **10** following deposition of a ferroelectric material **38**. The ferroelectric material fills the open gate region. Preferably, the ferroelectric material **38** is deposited to a thickness greater than the depth of the open gate region. The ferroelectric material **38** may be deposited by metal-organic chemical vapor deposition (MOCVD) or a chemical-solution deposition (CSD) process. The ferroelectric material is preferably selected from PGO, PZT, SBT, SBO, SBTO, SBTN, STO, BTO, BLT, LNO, and $YMnO_3$.

[**0037**] For example a PGO material, which may also be referred to as $Pb_5Ge_3O_{11}$, may be deposited using the following preferred method. The PGO material is deposited by metal organic vapor deposition (MOCVD) and RTP(Rapid Thermal Process) annealing techniques. The PGO material may be deposited at temperatures between 450 and 550° C.

[**0038**] An EMCORE oxide MOCVD reactor with liquid delivery system was used for the growth of PGO material. The precursors for the PGO material are listed in Table 1.

TABLE 1

The properties of precursors for PGO thin films

Precursors	Formula	Vapor Pressure (mm Hg)	Decomposition Temperature (° C.)
$Pb(TMHD)_2$	$Pb(C_{11}H_{19}O_2)_2$	180° C./0.05	325° C.
$Ge(ETO)_4$	$Ge(C_2H_5O)_4$	b.p. 185.5° C.	

[**0039**] Liquid precursors such as germanium alkoxides, germanium halides, lead alkyls, and lead halides use a bubbler with a controlled temperature to generate precursor vapors. Solid precursors, such as lead B-diketonates, are dissolved in a solvent and use a liquid delivery system coupled with a flash vaporizer to generate precursor vapors. Table 2 is a list of PGO precursors that may be used in some aspects of the present invention.

TABLE 2

The properties of precursors for PGO films

Precursor	Formula	Appearance at room temperature	Moisture stability	Vapor Pressure (mm Hg)	Decomp-osition Temp. (° C.)
$Ge(ETO)_4$	GeH_4 Ge_2H_6 Ge_3H_8 $Ge(OC_2H_5)_4$ $GeCl_4$ $(C_2H_5)_2GeCl_2$	colorless liquid	sensitive	185° C.	
Pb Tetraphenyl	$Pb(C6H5)4$	white powder		230° C/0.05	325° C.
$Pb(TMHD)_2$	$Pb(C_{11}H_{19}O_2)_2$ $Pb(C_2H_5)_4$	white powder		180° C/0.05	325° C.

[**0040**] Table 3 is a list of solvents that are alternately available for use in some aspects of the present invention.

TABLE 3

The properties of solvents for PGO films

Solvents	Formula	Boiling Temp. (° C.)
Tetrahydrofuran (THF)	C_4H_8O	65–67° C.
Iso-propanol	C_3H_7OH	97° C.
Tetraglyme	$C_{10}H_{22}O_5$	275° C.
Xylene	$C_6H_4(CH_3)_2$	137–144° C.
Toluene	$C_6H_5CH_3$	111° C.
Butyl ether	$[CH_3(CH_2)_3]_2O$	142–143° C.
Butyl acetate	$CH_3CO_2(CH_2)_3CH_3$	124–126° C.
2-Ethyl-1-hexanol	$CH_3(CH_2)_3CH(C_2H_6)CH_2OH$	183–186° C.

[**0041**] $[Pb(thd)_2]$ and $[Ge(ETO)_4]$ with a molar ratio of 5:3 were dissolved in a mixed solvent of tetrahydrofuran, isopropanol and tetraglyme in the molar ratio of 8:2:1. The precursor solutions have a concentration of 0.1 to 0.3 M/L of $Pb_5Ge_3O_{11}$. The solution was injected into a vaporizer (150° C.) by a pump at a rate of 0.1 ml/min to form precursor gases. The precursor gases were brought into the reactor using a preheated argon flow at 150-170° C. The deposition temperatures and pressure are 500° C. and 5-10 Torr separately. The shroud flow (Ar 4000 sccm) with oxygen (1000-2000 sccm) was led into the reactor. After deposition, the PGO material was cooled down to room temperature in an oxygen atmosphere. The PGO material may be annealed using RTP.

[**0042**] Alternatively, a CSD process may be used to deposit the ferroelectric material instead of MOCVD. One form of CSD process is a spin on method. For example, a PGO thin film may be deposited using the spin on method. The precursors are lead acetate and germanium iopropoxide in di (ethylene glycol) ethyl ether solution. The precursors are spun over the substrate and any overlying structures forming a film. The film is baked at 50 to 350 degrees Celsius for 1 to 10 minutes and pre-annealed after each spin coating at 400 to 500 degrees Celsius for 1 to 15 minutes to

evaporate the solvent and eliminate the organic components. Each spin coating layer has a thickness of between about 10 nm and 100 nm. After several repetitions, the PGO film can be produced with a desired thickness. The PGO film is crystallized at 500 to 600 degrees Celsius for 5 minutes to 3 hours in oxygen ambient. Optimization of the process can be achieved for a desired film thickness, without undue experimentation.

[0043] **FIG. 10** shows the semiconductor structure **10** following CMP of the ferroelectric material to produce a ferroelectric gate **40**. The CMP process preferably stops at the top of the passivation sidewalls **36**. Alternatively, the CMP process may extend slightly below the top of the passivation sidewalls **36**.

[0044] **FIG. 11** shows the semiconductor structure **10** following deposition of an electrode layer **42**. The electrode layer **42** comprises iridium, platinum, ruthenium, or their oxides. The electrode layer **42** is patterned and etched to form a top electrode **44**, as shown in **FIG. 12**. The electrode layer **42** may be patterned using photoresist or a hard mask material, such as TiN, TiO_2, $TiAlO_3$, SiO_2, SiN, or other suitable material. The electrode layer may be etched by plasma etching or other suitable etching process.

[0045] In an alternative embodiment, an inlaid, or damascene, method may be used to form the top electrode **44**. A trench would be formed using a method similar to that used in forming the ferroelectric gate, which was described in detail above. A metal, such as iridium, platinum, ruthenium, or their oxides, would then be deposited into the trench and polished using CMP to form the top electrode **44**.

[0046] **FIG. 12** shows the semiconductor structure **10** with a ferroelectric gate structure **46**. The ferroelectric gate structure **46** comprises the ferroelectric gate **40** protected by the gate insulation material **18** below, the passivation sidewalls **36** along the sides, and the top electrode **44** above. This will reduce, or eliminate, contamination of the ferroelectric gate **40** from oxygen or hydrogen diffusing into the ferroelectric gate **40**.

[0047] **FIG. 13** shows the semiconductor structure **10** with a passivation layer **48** deposited overlying the ferroelectric gate structure **46**.

[0048] **FIG. 14** shows the semiconductor structure **10** following final metallization using state of the art methods. Connections **50** to the source region **24**, the drain region **26**, and the top electrode **44** are shown as simplified structures. Any state of the art metallization scheme may be used, including copper metallization. The metallization may include barrier layers and other layers that are used in connection with various metallization schemes.

[0049] Although, metallization using deposition followed by etching is described above, it would also be possible to use a damascene metallization process instead. For example, use of the damascene metallization process is preferred for copper metallization.

What is claimed is:

1. A ferroelectric transistor structure comprising:

a) a ferroelectric gate having a bottom, sides and a top overlying a semiconductor substrate;

b) a gate insulator interposed between the ferroelectric gate and the semiconductor substrate; and

c) passivation sidewalls adjacent the sides.

2. The ferroelectric transistor structure of claim 1, wherein the semiconductor substrate is silicon or SOI.

3. The ferroelectric transistor structure of claim 1, wherein the ferroelectric gate is PGO, PZT, SBT, SBO, SBTO, SBTN, STO, BTO, BLT, LNO or $YMnO_3$.

4. The ferroelectric transistor structure of claim 1, wherein the gate insulator is silicon nitride, nitrogen implanted silicon oxide, or silicon oxynitride.

5. The ferroelectric transistor structure of claim 1, wherein the gate insulator is ZrO_2, zirconium silicate, Zr—Al—Si—O, HfO_2, hafnium silicate, Hf—Al—O, La—Al—O, lanthanum oxide or Ta_2O_5.

6. The ferroelectric transistor structure of claim 1, wherein the ferroelectric gate is deposited using a chemical-solution deposition (CSD) method.

7. The ferroelectric transistor structure of claim 1, wherein the passivation sidewalls comprise TiO_2, Al_2O_3, $TiAlO_x$, or Si_3N_4.

8. The ferroelectric transistor structure of claim 1, further comprising a top electrode overlying the ferroelectric gate.

9. The ferroelectric transistor structure of claim 8, wherein the top electrode comprises iridium, platinum, ruthenium, iridium oxide, platinum oxide, or ruthenium oxide.

10. A ferroelectric transistor structure comprising a ferroelectric gate having a bottom, sides and a top, overlying a semiconductor substrate, wherein the ferroelectric gate is encapsulated by the combination of a gate insulator on the bottom, passivation sidewalls on the sides, and a top electrode on the top.

11. The ferroelectric transistor structure of claim 10, wherein the semiconductor substrate is silicon or SOI.

12. The ferroelectric transistor structure of claim 10, wherein the ferroelectric gate is PGO, PZT, SBT, SBO, SBTO, SBTN, STO, BTO, BLT, LNO or $YMnO_3$.

13. The ferroelectric transistor structure of claim 10, wherein the gate insulator is ZrO_2, zirconium silicate, Zr—Al—Si—O, HfO_2, hafnium silicate, Hf—Al—O, La—Al—O, lanthanum oxide or Ta_2O_5

14. The ferroelectric transistor structure of claim 10, wherein the ferroelectric gate is deposited using a chemical-solution deposition (CSD) method.

15. The ferroelectric transistor structure of claim 10, wherein the top electrode comprises iridium, platinum, ruthenium, iridium oxide, platinum oxide, or ruthenium oxide.

16. The ferroelectric transistor structure of claim 10, wherein the passivation sidewalls comprise TiO_2, Al_2O_3, $TiAlO_x$, or Si_3N_4.

17. The ferroelectric transistor structure of claim 10, wherein the gate insulator is silicon nitride, nitrogen implanted silicon oxide, or silicon oxynitride.

18. A method of forming a ferroelectric transistor structure on a substrate comprising the steps of:

a) forming a gate insulator over the substrate;

b) producing a sacrificial gate structure overlying the substrate;

c) removing the sacrificial gate structure;

d) depositing a passivation insulator over the substrate;

e) etching the passivation insulator using anisotropic etching, whereby passivation sidewalls are formed;

f) depositing a ferroelectric material over the substrate;

g) polishing the ferroelectric material using chemical-mechanical polishing (CMP), whereby a ferroelectric gate is formed; and

h) forming a top electrode overlying the ferroelectric gate.

19. The method of claim 18, wherein the step of forming the sacrificial gate accomplished by the steps of:

a) depositing and patterning a layer of sacrificial gate material, whereby a sacrificial gate is formed;

b) forming an oxide overlying the sacrificial gate;

c) and polishing the oxide to expose the sacrificial gate.

20. The method of claim 19, wherein the layer of sacrificial gate material is silicon nitride or polysilicon.

21. The method of claim 19, wherein the step of polishing is accomplished using chemical-mechanical polishing (CMP).

22. The method of claim 18, wherein the step of depositing the gate insulator is accomplished by chemical vapor deposition (CVD), pulsed CVD, sputtering, or evaporation.

23. The method of claim 18, wherein the step of depositing the gate insulator deposits ZrO_2, zirconium silicate, Zr—Al—Si—O, HfO_2, hafnium silicate, Hf—Al—O, La—Al—O, lanthanum oxide or Ta_2O_5.

24. The method of claim 18, wherein the step of depositing the ferroelectric material is accomplished by metal-organic chemical vapor deposition (MOCVD), or chemical-solution deposition (CSD).

25. The method of claim 18, wherein the step of depositing the ferroelectric material deposits PGO, PZT, SBT, SBO, SBTO, SBTN, STO, BTO, BLT, LNO or $YMnO_3$.

26. The method of claim 18, wherein the top electrode is iridium, platinum, iridium oxide or platinum oxide.

27. The method of claim 18, wherein the step of forming the top electrode is accomplished by depositing and patterning a top electrode layer.

28. The method of claim 18, wherein the step of forming the top electrode is accomplished by using a damascene process.

29. The method of claim 18, wherein the step of depositing the passivation insulator deposits TiO_2, Al_2O_3, $TiAlO_x$, or Si_3N_4.

30. The method of claim 18, wherein the step of etching the passivation insulator is accomplished using anisotropic plasma etch.

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