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Marsh, Jr. et al.

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[54] CONTROL FOR CHAIN PRINTER

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[21] Appl. No.: **146,943**

Related U.S. Application Data

[62] Division of Ser. No. 877,354, Nov. 17, 1969, Pat. No. 3,629,861.

[52] **U.S. Cl.** ..... **101/93 C**, 101/111

[51] **Int. Cl.** **G06k 15/08**

[58] **Field of Search** 101/93, 111; 340/172.5

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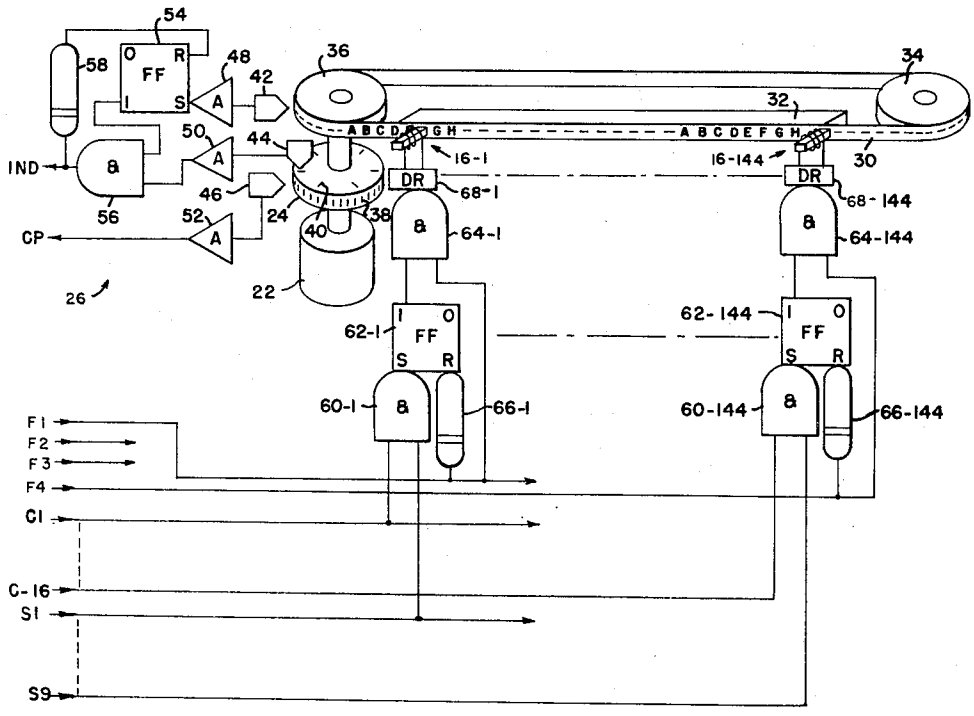
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[57] ABSTRACT

A control system for a horizontal type carrier, or "chain", printer wherein a recirculating shift register memory is employed to store the code representations of characters to be printed on the print line. A tracking or address counter is advanced in synchronism with the movement of data through the shift register and serves to identify each character stored therein with the particular print position in which it is to be printed. Generation of print command signals is accomplished by comparing, in sequence, each character stored in the memory with the output of a character generation counter which is advanced in synchronism with the movement of the type carrier to identify the order in which the types on the carrier move past the print positions. Actuation of the comparator and advancement of the character generation counter are controlled directly by the output of the tracking counter. Beginning-of-font sync pulses are generated by gating a primary index signal derived directly from the type carrier with a secondary index signal derived from a rotating code disc. A plurality of index marks are provided on the code disc in a manner to enable generation of properly timed beginning-of-font signals for any of a variety of different font length type carriers interchangeably employable in the printer.

3 Claims, 8 Drawing Figures



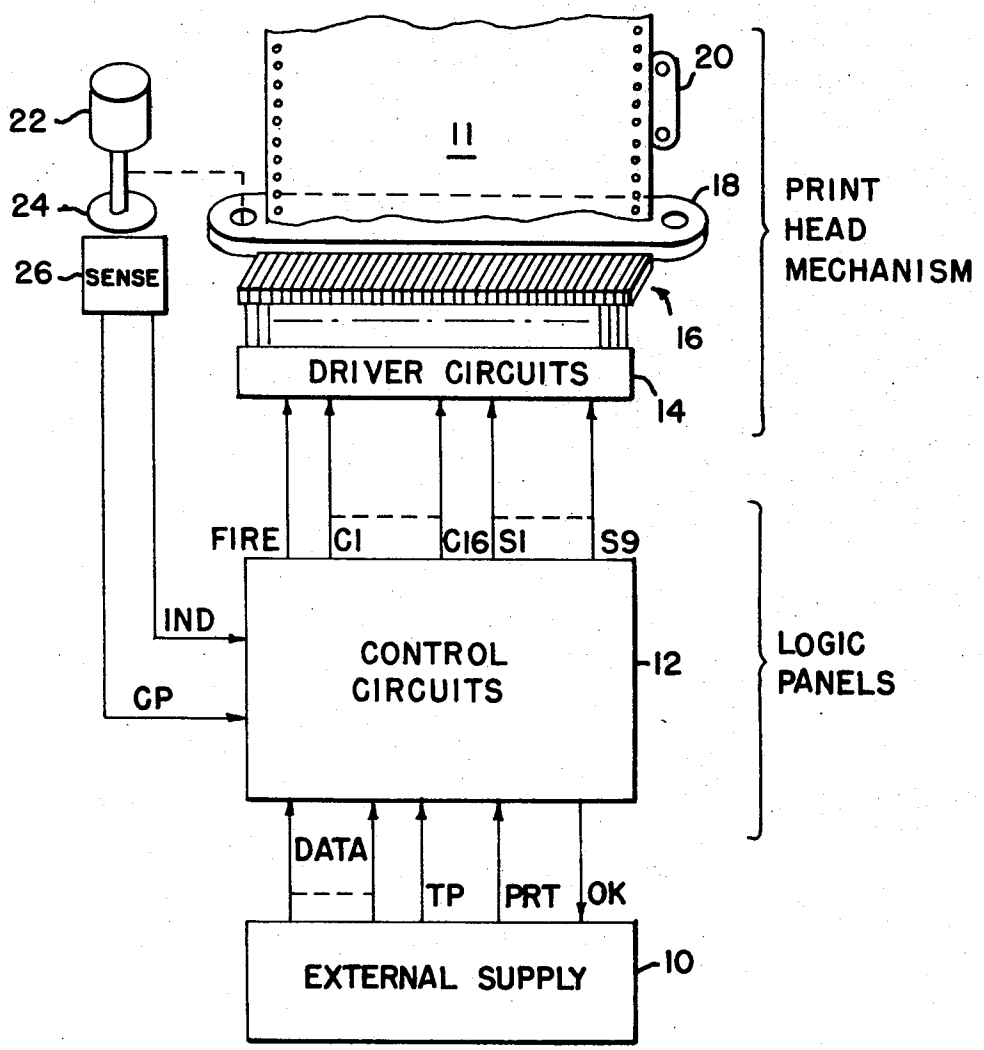


FIG. 1

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FIG. 2

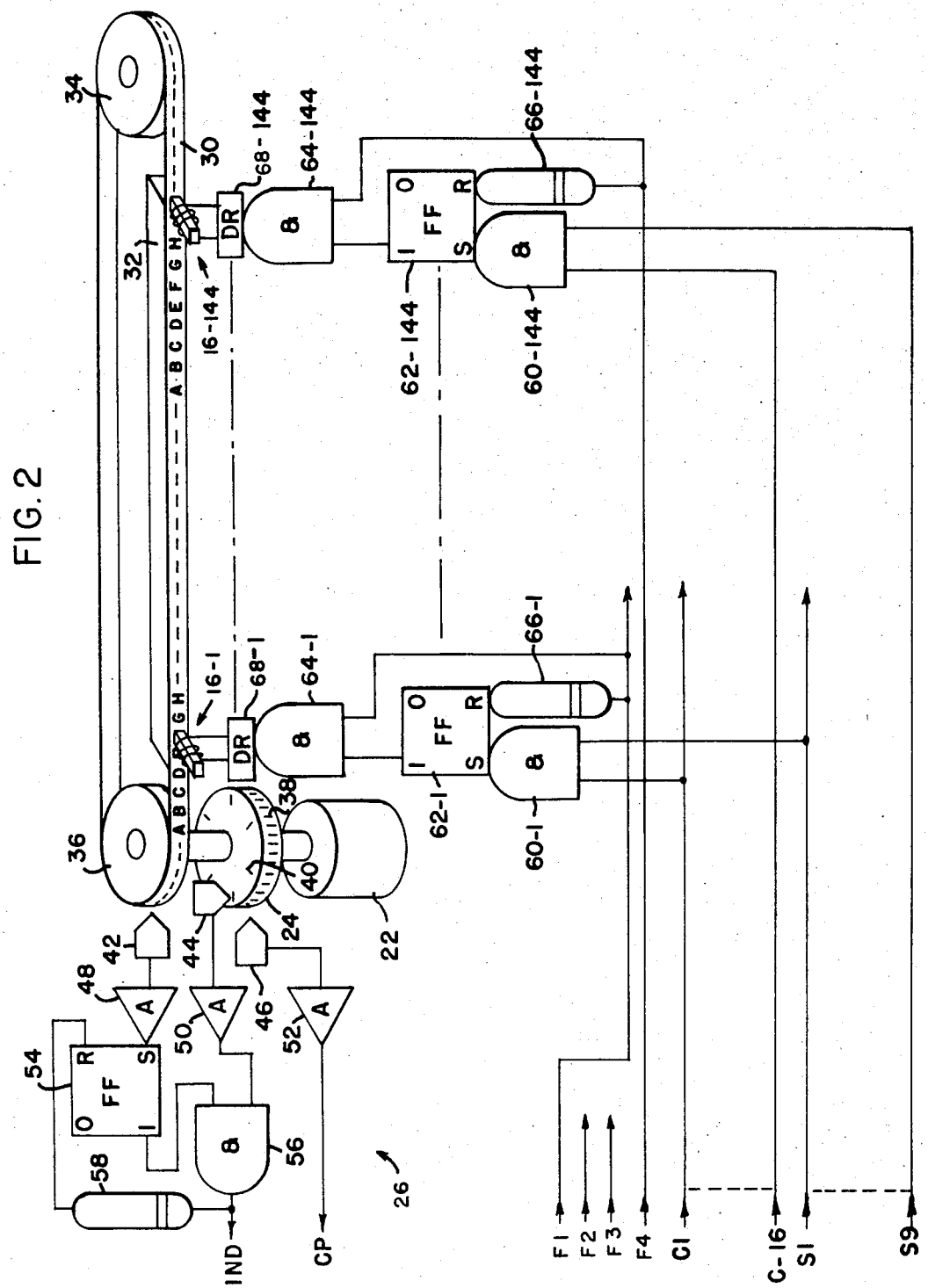
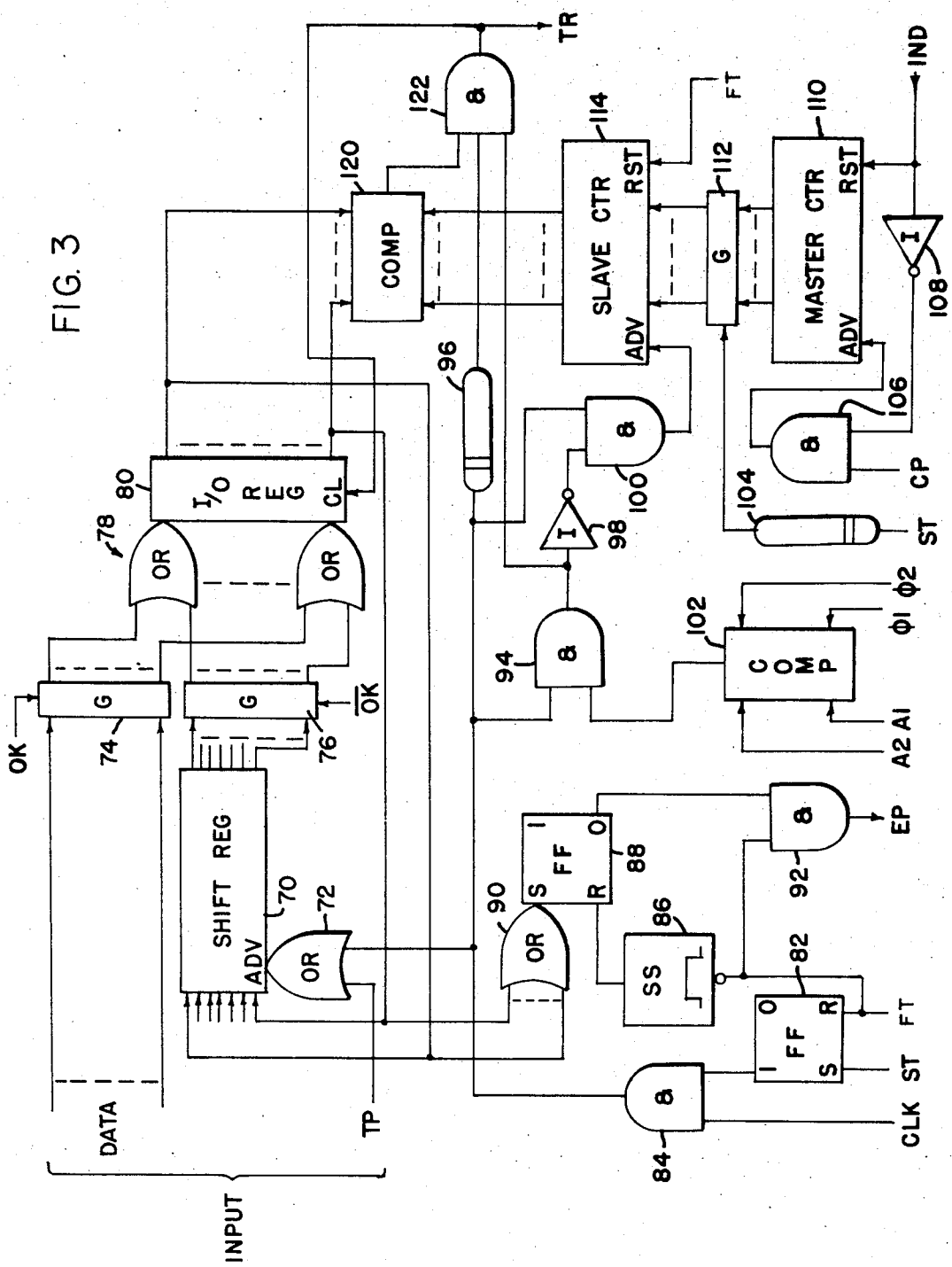

34
30
32
16-144
68-144
64-144
66-144
62-144
60-144
A B C D E F G H
DR
FF
16-1
68-1
64-1
66-1
62-1
60-1
36
38
40
22
24
42
44
46
48
50
52
54
56
58
26
IND
CP
F1
F2
F3
F4
C1
C-16
S1
S9

FIG. 3


TR
IND
FT
122
120
114
110
112
COMP
SLAVE CTR
RST
ADV
G
MASTER CTR
RST
ADV
I
108
96
106
80
I/O REG
CL
78
OR
OR
98
100
104
CP
ST
102
Φ2
Φ1
94
COMP
A2 A1
OK
74
G
G
76
OK
SHIFT REG
ADV
70
72
OR
90
FF
I
S
R
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R
I
S
FT
ST
CLK
84
DATA
TP
INPUT

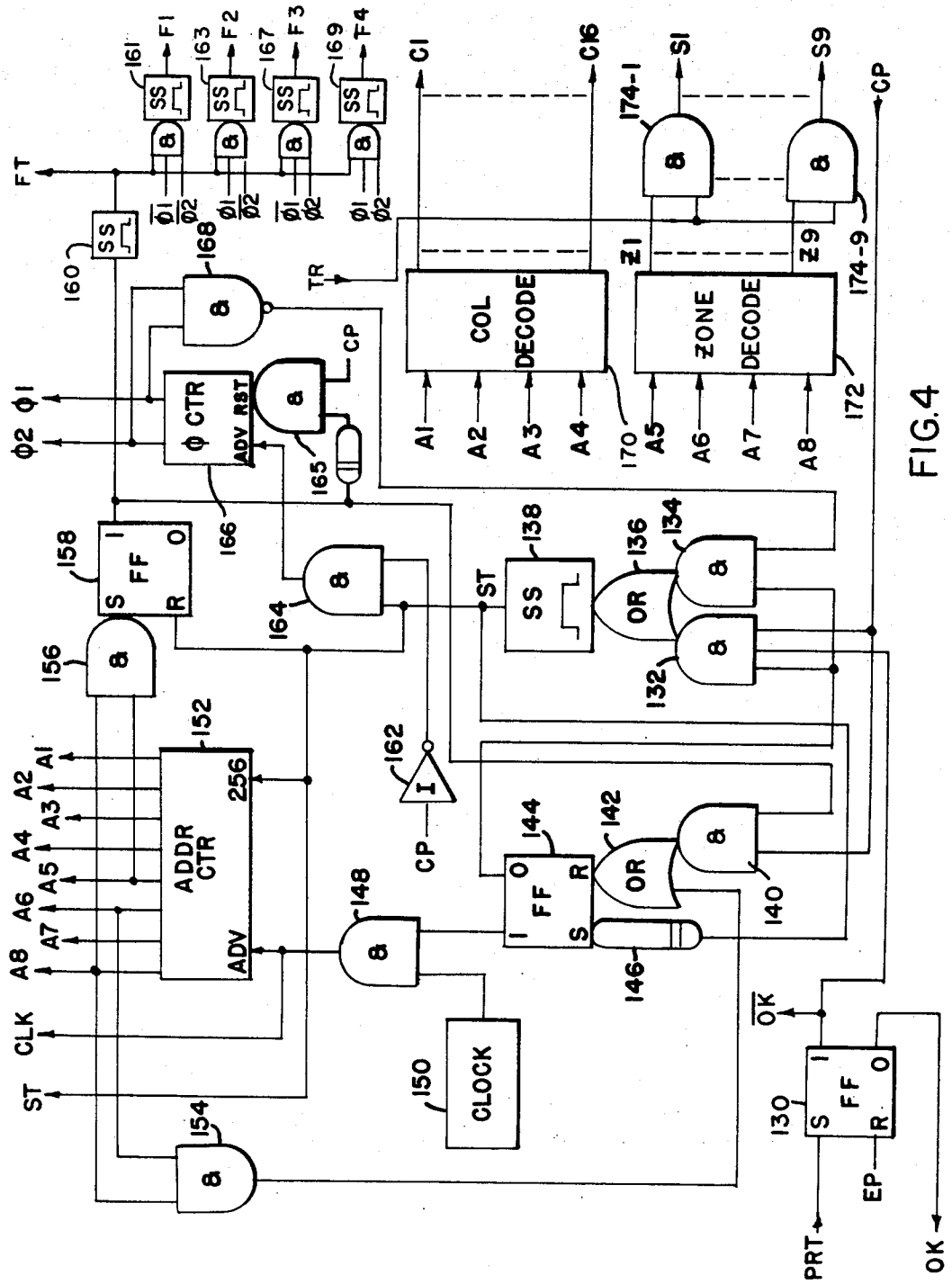

FT
SS
160
161
F1
163
F2
167
F3
169
F4
Φ1
Φ2
C1
C16
S1
S9
CP
174-1
174-9
Z1
Z9
TR
168
COL DECODE
ZONE DECODE
172
A1
A2
A3
A4
170
A5
A6
A7
A8
Φ CTR
ADV RST
165
166
158
FF
164
156
138
OR
136
134
132
ST
152
ADDR CTR
256
ADV
162
144
142
140
148
146
CLK
150
CLOCK
154
OK
130
EP
PRT

FIG.4

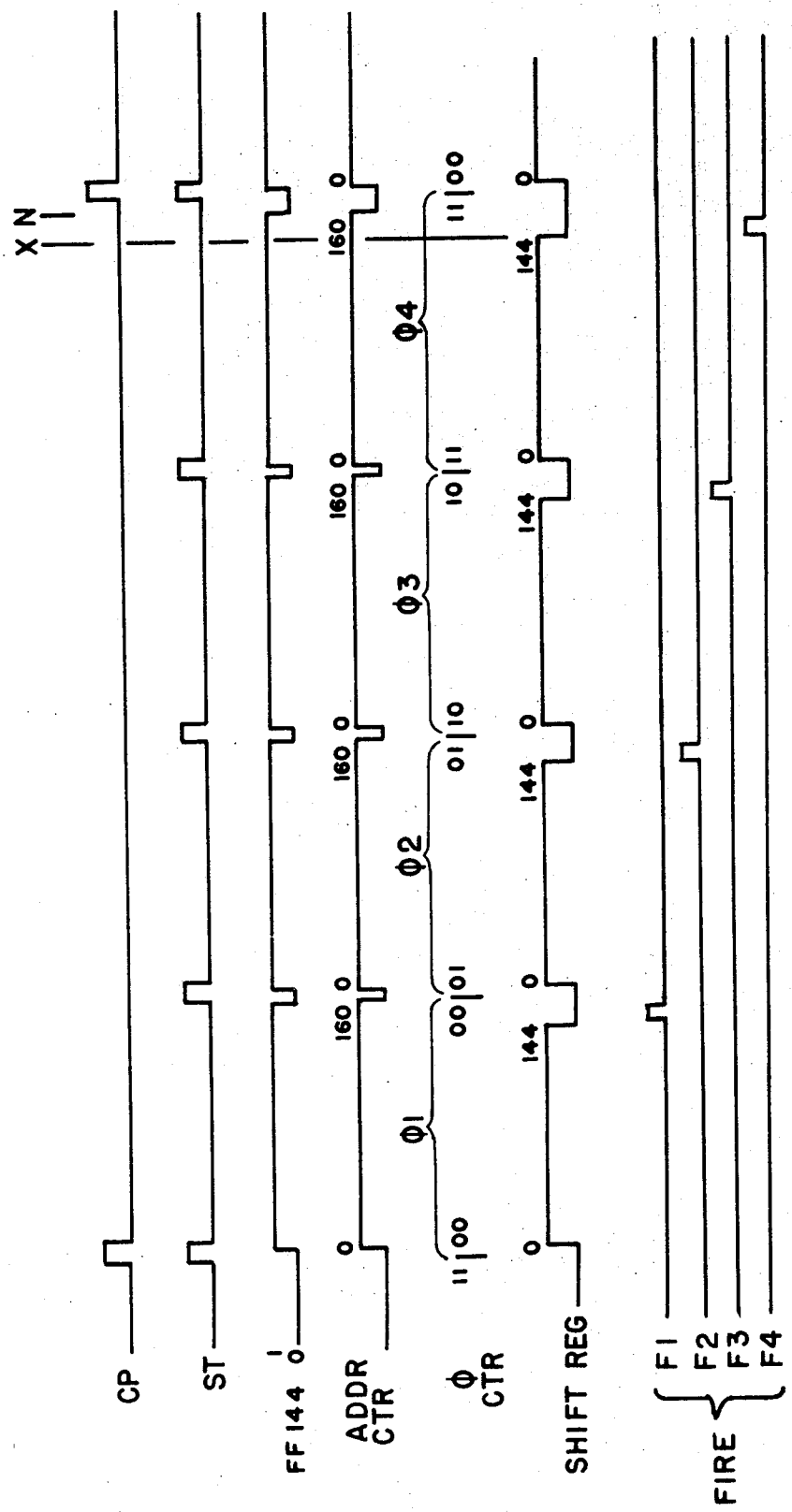

XN
CP
ST
FF 144
ADDR CTR
160
0
φ CTR
φ1
φ2
φ3
φ4
00
01
10
11
SHIFT REG
144
F1
F2
F3
F4
FIRE

FIG. 5

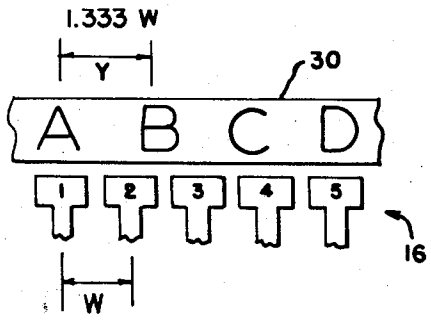


FIG. 6

PHASE	COLUMN PRINTED
ϕ 1	1 5 9 13 17 21 - - - - 141
ϕ 2	2 6 10 14 18 22 - - - - 142
ϕ 3	3 7 11 15 19 23 - - - - 143
ϕ 4	4 8 12 16 20 24 - - - - 144

FIG. 7

COLUMN DECODE

INPUT				OUTPUT
A4	A3	A2	A1	
0	0	0	0	C 1
0	0	0	1	C 2
0	0	1	0	C 3
0	0	1	1	C 4
0	1	0	0	C 5
0	1	0	1	C 6
0	1	1	0	C 7
0	1	1	1	C 8
1	0	0	0	C 9
1	0	0	1	C 10
1	0	1	0	C 11
1	0	1	1	C 12
1	1	0	0	C 13
1	1	0	1	C 14
1	1	1	0	C 15
1	1	1	1	C 16

FIG. 8

ZONE DECODE

INPUT				OUTPUT
A8	A7	A6	A5	
0	0	0	0	Z1
0	0	0	1	Z2
0	0	1	0	Z3
0	0	1	1	Z4
0	1	0	0	Z5
0	1	0	1	Z6
0	1	1	0	Z7
0	1	1	1	Z8
1	0	0	0	Z9

CONTROL FOR CHAIN PRINTER

This is a division of application Ser. No. 877,354 filed Nov. 17, 1969, and now Pat. No. 3,629,861.

BACKGROUND OF THE INVENTION

In the art of on-the-fly, high speed line printing two basic forms of print mechanisms are employed. The oldest form is the so-called drum print mechanism. This mechanism employs a bank of individually controllable print hammers, usually one for each of the possible print positions in the print line, in association with a constantly rotating type drum having engraved about its periphery the various characters of the type font arranged in rows and columns. The type characters of each column are aligned to cooperate with one of the hammers and the type characters of each row extending across the width of the drum are identical. The number of rows of type depends upon the number of different characters in the type font.

The second form of mechanism is the so-called "chain" print mechanism which also employs a bank of individually actuatable hammers but which, instead of a type drum, utilizes a constantly moving type chain or belt which moves the type characters past the print hammers in a direction parallel to the print line. The most frequently cited advantage of the chain mechanism over the drum mechanism is that horizontal registration of the printed characters (alignment of the characters with respect to a horizontal reference line) is much easier to control. That is, the unavoidable slight inaccuracies which occur in the timing of the print hammers cause the printed character images to be misplaced slightly in a horizontal direction rather than in a vertical direction, as is the case with the drum mechanism. The result is that the chain mechanism produces a much more even print line which has a more pleasing aesthetic appearance, is easier to read, and is more suitable for applications requiring a relatively high degree of print format control.

Additional advantages inherent in the chain mechanism include easy replaceability of individual types of type groupings on the carrier, lower cost of carrier manufacture, particularly when it is desired to produce carriers having different length type fonts or fonts with different character arrangements, and ease of removal and replacement of the carrier within the printer. Additionally, "ghosting" is more simply avoided with the chain mechanism as it is necessary merely to space the characters on the carrier slightly farther apart than the distance between print positions on the line.

The principal difficulty encountered in the implementation of a chain printing system lies in the area of control. The generation of properly timed print hammer actuation signals is more complicated because at any given instant each print hammer is confronted with a different character rather than with the same character as is the case with the drum printer. Thus, "character generation", which is the function of keeping track of which character is printable at each of the print hammers during each print subcycle, requires more than the simple code wheel or single counter used for character generation in the drum system. This complexity is further compounded when the type spacing on the carrier is greater than the print position spacing since all the hammers do not become actuatable for printing at the same instant.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is a principle object of the present invention to provide a simplified, low cost and reliable control system for a chain printer.

More specifically, objects of the invention are to provide an improved and simplified character generation system for a chain printer and to provide a control system operable, without major alteration, with a variety of different type carriers having different font lengths.

According to a first aspect of the invention, simplified character generation is accomplished for a system where type spacing is greater than print position spacing by tracking the scan of the memory (containing the characters to be printed in a line) with a single tracking or address counter and employing the output of this counter to control the character generation and comparison functions. A subsidiary "phase" counter is employed to arrest the advance of the character generator when predetermined counts are exhibited by the tracking counter whereupon the character generation sequence is maintained in proper synchronism. Correlative to this, the comparator is activated during the times that the character generator is arrested.

In accordance with a second aspect of the invention, proper generation of beginning-of-font or "index" sync pulses regardless of the length of the type font is accomplished by deriving a sequence of index pulses from a code disc and utilizing the moving carrier to gate the proper one of these index pulses to the control circuits in accordance with the length of the font provided on the carrier.

In accordance with a third aspect of the invention, reliability of the control circuits is enhanced and power requirements are reduced by locating the individual hammer driver circuits physically close to the hammers they control and by utilizing a coincident signal selection scheme for selecting hammers to be actuated whereby the number of control lines running from the logic circuits to the hammer mechanisms, located in a portion of the printer chassis remote from the logic circuits, is minimized.

These and other objects, features and advantages will be made apparent by the following detailed description of a preferred embodiment of the invention, the description being supplemented by drawings as follows:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the basic components and the intercomponent flow of data and control signals for the chain printing system of the invention.

FIG. 2 is a schematic diagram showing the mechanical and control circuit portions of the print head component of FIG. 1.

FIGS. 3 and 4 taken together constitute a schematic circuit diagram of the control circuit component of FIG. 1.

FIG. 5 is a waveform diagram showing the operation of the system of the invention during a single print cycle.

FIG. 6 is a diagram illustrating the relationship between the spacing of type characters on the type carrier and the spacing of print hammers (print positions) along the print line.

FIGS. 7 and 8 are truth tables showing the relationship between inputs and outputs of the column and zone decode circuits shown in FIG. 4.

GENERAL DESCRIPTION OF EMBODIMENT

Referring to FIG. 1, the line printing system of the invention comprises two basic components, the print head mechanism and the logic circuits. The print head includes a print chain cartridge **18**, a motor **22** and associated mechanical components for driving the print chain at a constant velocity, and a bank of print hammers **16** which are individually operable under control of a set of driver circuits **14**. The print head further comprises means including a pair of paper feed tractors **20** for feeding a print form **11** in a step-by-step fashion between the hammers **16** and chain **18** and a code disk **24** and set of sensing circuits **26** for generating basic control signals for synchronizing the operation of the control circuits with the movement of the type chain. Also, an ink ribbon (not shown) is provided between the hammers and the paper **11** in a conventional manner.

The control circuits **12**, which may be contained on a set of logic or circuit panels in a section of the system remote from the print head, receive and store coded signals transmitted from an external information supply device **10** representing the characters to be printed in a print line. Supply **10** also provides timing signals TP which are used by the control circuits to supervise the entrance into storage of the data characters. When a full line of characters has been entered, supply **10** transmits a print commanded signal PRT to the printer whereupon the printer launches into a print cycle to print the stored data. When the print line is completed the control circuits transmit a signal OK back to supply **10** indicating that the print system is prepared to receive the next line of data. OK is terminated by PRT and remains inactive throughout the print cycle to inhibit supply **10** from transmitting any new data before the termination of the print cycle.

To enable proper synchronization of the operation of the control circuits **12** with the movement of the type chain a sequence of character sync signals CP and index sync signals IND are generated by the code disk **24** and sensing circuits **26** and are transmitted to the control circuits. The CP pulses occur at a repetition rate identical to the rate at which the type characters on the type chain pass a fixed reference point. The index signals IND occur at a repetion rate equal to the repetition rate at which a predetermined character in each type font on the chain passes the stationary reference point. The type characters in each font are arranged in identical order. The index pulse is a "- beginning of font " pulse. Since both CP and IND are generated by sensing marks inscribed on the code disk **24** which is connected to the type chain drive mechanism, the unavoidable variations in the velocity of the type chain correspondingly alter the rep rate of CP and IND, enabling the control circuits to operate in proper synchronism with the type chain in a manner described subsequently.

During the print cycle, the control circuits transmit to the print head combinations of print hammer selection signals on lines C1 through C16 and S1 through S9. These signals operate, as described subsequently, in accordance with coincident selection principals to "- prime" or "cock" the driver circuits **14** associated with selected ones of the print hammers **16**. After this priming operation of FIRE signal is transmitted to the print head to actuate all of the primed driver circuits whereupon the print hammers associated therewith are driven against the ink ribbon to force paper **11** against the chain to print the desired characters. This alternating prime and fire sequence continues until all the characters stored in the memory have been printed whereupon OK is initiated to begin a new data loading sequence and the paper feed mechanism **20** is operated to step the paper to the next print line position.

DETAILED DESCRIPTION OF EMBODIMENT

Definition of Circuit Symbols

Before proceeding with a detailed description of the preferred embodiment of the invention the meaning of the logic circuit symbols used in FIGS. 2, 3 and 4 is given. It is to be understood that the logic schematics shown operate, as is conventional, on a binary voltage level basis wherein the inputs to the circuits and the outputs therefrom always exist at either of two discreet voltage levels, the upper voltage level (H) of the system or the lower voltage level (L) of the system.

An AND circuit is represented by a D-shaped block containing an & symbol. The input lines are always connected to the straight side of the block and the output line is always connected to the curved side of the block. The function of this circuit is to provide an H output voltage only when all input lines exist at the H level. When a small circle appears at the point where the output line joins the block then the function of the circuit is to provide an L level output only when all inputs are at the H level.

An OR circuit is represented by an arrow-shaped block containing the symbol OR. Input lines are always connected to the concave side of the block and the output line is always connected to the point. The function of this circuit is to provide an H level output only when any one or more of the input lines is at the H level.

A flip-flop circuit is represented by a rectangular block containing the symbol FF. The inputs are labeled set (S) and reset (R) and the outputs are labeled **1** and **0**. This circuit is bistable in nature and its outputs are always at opposite voltage levels. When a L to H voltage level transition is presented at the S input the 1 output goes to H and the 0 output goes to L unless the outputs are already in such a state in which case the output levels do not change. When a L to H transition is presented to the R input the 0 output goes to H and the 1 output goes to L unless the outputs already exist in such a state in which case there is no change in the output levels.

A single-shot multivibrator is represted by a rectangular block containing the symbol SS. The input line to the circuit is always connected to the left or bottom edge of the block and the output line is always connected to the right or top edge of the block. The function of this circuit is to generate an L to H to L square-wave output pulse of fixed duration in response to a L to H transition occurring at the input. When a small circle appears at the point where the input line joins the block then the function of the circuit is to provide the

square-wave output pulse in response to an H to L transition at the input.

An inverter circuit is represented by a triangular block containing the symbol I and having a small circle at the point where the output line joins the block. The function of this circuit is to provide an output level which is always opposite to the input level.

A delay circuit is represented by an elongated oval-shaped block with a pair of transverse stripes nearest the input end. The function of this circuit is to generate an output level which follows the input level but which changes state at some fixed period of time after the input changes state.

A gate circuit is a rectangular block containing the symbol G. Inputs into the gate circuit are identified by an arrowhead. The function of this circuit is to transfer the voltage levels on a plurality of input lines to an equal plurality of output lines whenever the gate control input line is at the H level. The latter line is a single input connected to one of the ends of the gate block. A gate circuit is usually made up of a plurality of AND circuits, one for each input line other than the gate control input. Each input into the gate is connected to the input of a different one of the ANDs and each output from the gate is taken from the output of a different one of the AND circuits. The gate control input line is connected to an input of all the ANDs.

A binary counter is represented by a rectangular block containing the symbol CTR. Inputs are supplied at an advance (ADV) input and a reset (RST) input, a pulse at the former operating to advance the value of the binary count exhibited on the output lines by one and a pulse at the latter operating to force the outputs to the all-0 state (unless some other reset count is indicated in lieu of the RST legend).

Print Head Mechanism

The pertinent details of the print head mechanism are schematically illustrated in FIG. **2**. The type chain cartridge includes a type-carrying band or chain **30** which is entrained for rotation about a pair of pulleys **34** and **36**. The chain carries a plurality of complete type fonts having characters evenly spaced about the full periphery of the chain. An anvil plate **32** backs up the chain in the area of the print line. While not shown in FIG. **2**, it is usual to provide teeth on the pulleys to mate with teeth on the chain whereby a positive, non-slip drive is obtained. It is also a usual practice to make the chain cartridge assembly, i.e., the chain **30**, anvil **32** and pulleys **34** and **36**, readily removable as an integral unit from the print head mechanism.

The motor **11** drives the chain through connection with the pulley **36**. The end of the motor drive shaft is provided with splines or is keyed or made square to enable easy disengagement of the pulley **36** from the drive shaft while at the same time providing a positive driving connection.

The code wheel **24** is also positively connected to the motor drive shaft so that it rotates in synchronism with the pulley **36**. The code wheel has inscribed about its periphery a plurality of marks **38** and also is provided with a plurality with radial marks **40** on its upper surface. These marks may be, for example, transparent apertures in an opaque disk or they might be magnetically detectable marks on a ferrous disk. The marks **38** correspond to the type characters on the chain **30** and are sensed by a transducer **46** which generates an output pulse in response to each mark. The marks pass transducer **46** at the same rate that the characters on the chain pass a stationary point. Each such output pulse is amplified and shaped by amplifier **52** and transmitted thereby as a CP pulse. The marks **40** are sensed by a transducer **44** and the outputs generated therefrom are processed by amplifier **50** and transmitted to one of the inputs of an AND circuit **56**. In the embodiment herein described, there is one mark **40** for each eight marks **38**.

A transducer **42** is positioned to sense beginning-of-font marks inscribed on the chain **30**. There is one such mark inscribed at some predetermined location within each of the type fonts on the chain. For ease of manufacture this mark may be placed on a type slug which carries a character or characters common to all different font arrangements usable with the printer. For example, if each of the different fonts includes a set of alphabetic characters then a predetermined alphabetic type slug would be suitable for supporting the beginning-of-font mark. This procedure, of course, simplifies the manufacturing of the type slugs and the assembly of the chains.

Each output pulse generated by transducer **42** is conditioned by an amplifier **48** and is fed to the set input of a flip-flop **54**. The **1** output from the flip-flop is fed to the other input of AND **56** so that each beginning-of-font mark on the type chain sets the flip-flop and causes AND **56** to become partially conditioned. Concurrently with this or slightly afterwards, a mark **40** is sensed by transducer **44** whereupon AND **56** is activated and the output pulse IND is generated. Because the actual timing of the IND pulse is determined by the mark **40**, which is accurately oriented with respect to the marks **38** carried on the same member, the IND and CP pulses bear the precise timing relationship with one another which is necessary for correct operation of the logic circuits.

In the present embodiment, the 8 to 1 ratio between marks **38** and marks **40** insures correct generation of the IND pulse for any type font having a number of characters evenly divisible by 8. Thus, type chains bearing fonts of characters in any of the standard lengths, e.g., 48 characters, 64 characters, 96 characters, 128 characters, etc., may be used with the printer without alteration of the sensing circuits **26**. Of course, as explained subsequently in connection with the control circuits, a slight modification of the character generation circuits must be made to account for the particular number of characters employed in the type font in use.

The print hammers **16** may be of conventional design and are supported in alignment with each of the print positions along the print line. A standard arrangement is to place the hammers on 0.1 inch centers to enable the printing of 10 characters per inch. In the present embodiment, there are 144 print hammers **16-1** through **16-144**. Since each hammer and hammer drive assembly is identical, only the first and last are shown in FIG. **2**.

Each hammer is actuated for printing by a solenoid coil which is connected to receive a current pulse from a driver circuit **68**. Each such driver circuit is in turn

controlled by the output from an AND circuit **64** which has a pair of inputs connected respectively to the 1 output of a flip-flop **62** and to a line which supplies one of four fire pulses F1, F2, F3 and F4 from the control circuits. Each flip-flop **62** has an AND circuit **60** connected to its set input and a delay circuit **66** connected to its reset input. The latter is connected to a fire pulse input line while the former receives a pair of inputs from the hammer select control lines C1 through C16 and S1 through S9. Each AND **60** has one input line connected to one of the C control lines and its other input connected to one of the S lines.

ANDs **60-1** through **60-16** associated with the first 16 print hammers are each connected to a different one of the 16 control lines C1 through C16, AND **60-1** being connected to C1, AND **60-2** being connected to C2, etc. The second group of sixteen AND's **60-17** through **60-32** are connected in similar sequence to the lines C1 through C16. This pattern of input connections repeats for each of the remaining seven groups of 16 AND circuits **60**. The S control lines are connected to the ANDs 16 at a time. That is, line S1 is connected to the second input of each of the first 16 ANDs **60-1** through **60-16**, line S2 is connected to the second input of each of the ANDs **60-17** through **60-32**, line S3 is connected to the second input of each of the ANDs **60-33** through **60-48**, etc.

Thus, when the control circuits of the system determine that a character to be printed is coming into alignment with the proper print position, signals are simultaneously transmitted to the print head on the proper C line and the proper S line to select the AND circuit **60** associated with that print position. This sets the corresponding flip-flop **62**. Thereafter, at a time determined to be the precise instant in which to begin actuation of the hammer, a fire pulse (F1–F4) is transmitted to the print head to activate the AND **64** which is connected to the output of the set flip-flop **62**, whereupon the hammer is actuated to print. After the firing operation has been initiated the delay circuit **66** associated with the set flip-flop passes the fire pulse to the reset input of the flip-flop to restore it to its initial condition. The fire pulse lines F1–F4 are connected to the hammer drive circuits in an every-fourth-hammer alternating sequence, i.e., line F1 is connected to control hammers **16-1**, **16-5**, **16-9**, etc., line F2 to hammers **16-2**, **16-6**, etc., line F3 to hammers **16-3**, **16-7**, etc. and line F4 to hammers **16-4**, **16-8**, etc.

Since the print head mechanism of FIG. 2 is located in a portion of the printer chassis which is remote from the control circuits, the reliability of the system is enhanced by the fact that only 29 control lines, i.e., the four fire lines, the C lines and S lines, are coupled between the logic circuits and the print head to control the 144 print hammers. This, coupled with the fact that signals are transmitted on the S lines only when it is desired to select a hammer for actual firing, minimizes the number of signals transmitted over the relatively lengthy connecting cable and thus the amount of electrical noise radiated into the system by the cable is kept to a minimum.

Further, power consumption is reduced since the F1–F4, C and S control signals are all low level logic signals which can be transmitted over the long connecting cable without significant power loss. The circuits which dissipate the most power are the driver circuits **68** which must feed high current drive pulses to the hammer solenoid coils. In the present system, power losses and noise are minimized by physically mounting the driver circuits **68** as close as possible to their associated hammer coils. This technique is permitted by the use of compact integrated circuit drivers mounted on printed circuit cards placed directly on the print head frame immediately adjacent the hammer modules.

Control Circuits

The control circuits **12** are shown in FIGS. **3** and **4**. The basic components are a buffer memory including a shift register **70** and input-output register **80** which function to store the characterms to be printed, a master six-position binary counter **110** and a six-position binary slave counter **114** which perform the character generation function, a six-bit comparator **120** for generating hammer select signals, an eight-position binary address or tracking counter **152** which supervises the various control operations, a two-position binary phase counter **166** and two-bit comparator **102** for controlling character generation and print comparison, and a pair of decode circuits **170** and **172** which operate from the address counter outputs to control generation of the hammer select control signals C and S.

Before proceeding with a description of the control circuits, reference is made to FIG. **6** for explanation of one of the basic precepts upon which operation of the system is based. FIG. **6** shows the spatial interrelation between the type characters on the type chain and the print positions in the print line. As noted from FIG. **6** the center-to-center distance between print positions (print Hammers) is W while the center-to-center distance Y between the type characters on the chain is 4/3 W. The principal reason for making Y greater than W is to reduce "ghosting." This is a phenomonon which occurs when a print hammer, in pressing the paper against the chain character to be printed, also creates sufficient pressure to generate a slight impression of the edge of the chain character adjacent to the character being printed. Ghosting is a problem with drum printers since the lateral spacing of types on the drum must equal to the spacing of the print hammers.

By opening up the spacing of types on chain **30**, as shown in FIG. **6**, ghosting is reduced or eliminated completely. A subsidiary reason for making the distance Y greater than the distance W is to stagger the operation of the print hammers. As noted from FIG. **6**, during the time it takes the print chain to move the distance Y (which is defined as one print cycle) all print hammers come into exact registration with one chain character. However, as illustrated in the table of FIG. **6**, all of the column hammers do not come into registration with a type character at the same instant. Hammer registrations occur in four groupings or phases, $\Phi 1$, $\Phi 2$, $\Phi 3$ and $\Phi 4$. This number of phases is dictated by the ratio of Y to W which in the case of the present embodiment is 4/3 (the distance spanned by four print columns equals the distance spanned by three character spaces on the chain).

Thus, during phase **1** of the print cycle, hammers **1**, **5**, **9**, **13**, etc., through **141** are the only hammers in re-

gistration with characters on the chain. During phase 2, hammers 2, 6, 10, 14, etc., through 142 come into registration with chain characters while during phase 3, hammers 3, 7, etc., through 143 are in registration and during phase 4, hammers 4, 8, 12, etc., through 144 are in registration. This means that even if one desires to print all the letters of the alphabet arranged in sequence across the print line, which will require all hammers to fire during the same print cycle, all the hammers do not fire simultaneously but instead the firings are staggered in four groupings of 36 hammers each.

It can be realized that if such a pattern was printed with a chain having type characters spaced at the distance W, every hammer would be required to fire at the same instant, which causes an excessive drain on the power supply and an unduly high force of impact is imposed on the type chain, ink ribbon and paper with potentially disasterous results. While it is true that the use of a chain having Y equal to W results in slightly faster completion of the print line, the small sacrifice in printing speed where Y is made greater than W is certainly justified.

It is noted that the number of phases X in any given system is equal to the ratio of Y to Y minus W. In the present embodiment X equals 4. In a system where Y equals 1.5 W, for example, X would equal 3 and in a system where Y equals 2.0 W, X would equal 2.

Referring back to FIGS. 3 and 4, data is loaded into the buffer memory shift register 70 during the data loading cycle by the alternating presentation of TP timing signals and data signals from the external input device. Each TP pulse operates through an OR circuit 72 to advance the data characters stored in shift register 70 one position to the right. An input data character is gated through a gate 74 and a set of OR circuits 78 into the I/O register 80. Thereafter, a TP pulse appears to shift the character from register 80 to the first storage position of the register 70. Thus, after 144 data characters representing the characters of one print line have been received from the input, character number 144 resides in register 80 while characters 1 through 143 reside in register 70, with character number 1 through 143 reside in register 70, with character number 1 residing in the storage position at the right-hand end of the register 70 and character 143 residing in the left-hand end position.

Following the loading operation, PRT is transmitted by the input device to set a print mode control flip-flop 130 whereupon OK terminates (shifts negative) and $\overline{OK}$ is initiated (shifts positive). The existence of OK in the low state inhibits the generation of any further TP or data signals by the input device.

The generation of $\overline{OK}$ initiates the beginning of print cycles by opening gate 76 to permit the circulation and recirculation of the data characters through the buffer memory. $\overline{OK}$ also provides a conditioning input to an AND circuit 132 whereupon the next CP pulse to occur activates AND 132, causing it to transmit an output through an OR 136 to trigger a single-shot 138. The output ST generated by single-shot 138 is fed to reset flip-flop 158, to reset the address counter 152 to the "256"state wherein all eight output lines A1 through A8 are forced to the 1 (high voltage) state, and is further transmitted to set a flip-flop 82 which conditions AND gate 84. ST is also fed to an input of AND 164 but since on this first print cycle ST is generated concurrently with CP, an inverter circuit 162 deconditions AND 164, preventing ST from being gated through to the advance input of the phase counter 166.

ST is also transmitted through a delay circuit 146 to the set input of a phase control flip-flop 144. When the flip-flop sets, it conditions an AND gate 148 to begin transmitting the regularly occurring outputs from a clock circuit 150 as the signal CLK to the advance inputs of address counter 152 and shift register 70, the latter being fed CLK through AND 84 and OR 72. The pulse train CLK is also presented through AND 84 to the inputs of a pair of AND circuits 94 and 100 and to the input of a delay circuit 96.

The first pulse of the CLK signal causes address register 152 to "turn over" from an all-1 output condition to the all-zero output condition (all eight output lines shifting to the 0 or low level state). It also causes the data in the buffer memory to shift one position to the right whereupon character number 1 of the print line is moved to register 80 and character number 144 is shifted to the first storage position in register 70.

The CP pulse which triggered the above sequence of operations is also fed through an AND 165 to reset the phase counter 166 to its 00 output state.

As the print cycle continues, the CLK pulses fed from AND 148 simultaneously advance the address counter 152 and the shift register 70. At the beginning of the 145th count of counter 152 the A5 and A6 output lines thereof simultaneously shift positive, activating AND 156 whereupon flip-flop 158 sets. The resulting positive shift at the 1 output of the flip-flop triggers a single-shot 160 to produce a "fire time" pulse FT. The latter triggers one of the four single-shots 161, 163, 167 or 169 to generate a fire pulse and is also fed to the reset input of flip-flop 82 which causes AND 84 to be deconditioned, terminating the supply of CLK pulses to the shift register 70. This halts the advance of the shift register and since it has been shifted 144 times prior to the halt of CLK pulses, the position of the data stored in the shift register and I/O register is the same as it was at the beginning of the count sequence i.e., character 144 is stored in register 80 and characters 1 through 143 are queued from right to left in register 70.

Address counter 152 continues advancing in response to the CLK pulses gated by AND 148 until the beginning of the 161st count. At that time the A6 and A8 outputs from the counter simultaneously shift positive, causing AND 154 to generate an output through OR 142 to reset phase control flip-flop 144. This shifts the 1 output of the flip-flop negative whereupon AND 148 is deconditioned and the supply of CLK pulses to the address counter terminates. The resetting of flip-flop 144 switches the 0 output thereof positive whereupon AND 134 is activated to retrigger single-shot 138 through OR 136. This action produces another ST pulse from single-shot 138 and initiates a second phase cycle which is executed in exactly the same manner as that just described. It is noted that this second ST pulse, since it does not accompany the generation of a CP pulse, is gated through AND 164 and advances the phase counter to its 01 output state.

At the end of the second phase cycle AND 154 again produces its output which resets flip-flop 144 and

generates a third ST pulse. The third ST pulse advances phase counter **166** to its 10 state.

At the end of the third phase cycle AND **154** again generates an output which results in the production of a fourth ST pulse which initiates a fourth phase cycle and advances the phase counter to its 11 output state. At this point it is noted that since the output state of the phase counter is **11** during the fourth phase cycle, the output of AND circuit **168** is at a low level whereupon AND **134** is deconditioned. Thus at the end of the fourth phase cycle the resetting of flip-flop **144** cannot trigger single-shot **138** to produce ST. This means that the control circuits will then cease operation until the next CP pulse occurs to activate AND **132** to initiate the next print cycle.

The character generation circuits comprise a pair of six stage binary counters **110** and **114**. Counter **110** is termed the master counter since it loads a new count through a gate **112** into counter **114**, termed the slave counter, at the beginning of each print cycle. Master counter **110** is advanced through an AND **106** one count by each CP pulse and thus keeps track of the instantaneous position of the type chain in respect to a fixed reference point. As the beginning of each character font on the chain passes the reference point IND is received from the print head mechanism and resets the master counter **110** to the count representative of the first character of the font. IND also acts through an inverter circuit **108** to decondition AND **106** whereupon the CP pulse occurring concurrently with the IND pulse does not advance the counter. With this arrangement it can be seen that it is important that CP and IND be exactly coincident. This is obtained by deriving both from the single code disk **24**.

An instant following the generation of ST at the beginning of each phase cycle, delay circuit **104** opens gate **112** to load the output count from the master counter into the slave counter **114**. Thereafter, as each phase cycle proceeds, AND **100** gates CLK pulses to advance the slave counter in accordance with the output of an inverter circuit **98**. The latter is connected to the output of an AND circuit **94** which acts in response to each CLK pulse to sample the output of the phase comparator **102**. Comparator **102** compares the outputs 1 and 2 of the phase counter with the two lowest order outputs A1 and A2 of the address counter. Whenever the value of these two-digit binary numbers is the same, comparator **102** generates an output which conditions AND (4 which in turn deconditions AND **100**. This prevents that particular CLK pulse from advancing the slave counter and the output count thereof does not change. When FT is generated on completion of each memory scan, the slave counter **114** is reset to an all-0 output state.

Hammer selection pulses are generated by the six-bit comparator circuit **120** which compares the code character appearing at any given instant at the output of register **80** with the code character represented at the output of the slave counter. If the outputs match, comparator **120** generates a positive pulse which is fed to an input of an AND circuit **122**. The latter will be activated by the CLK pulse appearing at the output of delay circuit **96** if AND **94** is producing a 1 output indicative of a match between the phase counter output and the A1-A2 output from the address counter **152**. The output generated by AND **122** is a true signal TR which is fed to the inputs of a set of nine AND circuits **174-1** through **174-9** and which is also fed back to clear the I/O register **80**. The latter action in effect erases the particular character from the memory and replaces it with an all-0 character. This, as described subsequently, indicates that that particular character has been printed.

The conversion of the TR pulses generated by AND **122** into print hammer control signals is effected by the column decode circuit **170** and the zone decode circuit **172**. The former of these circuits receives the A1 through A4 outputs from address counter **152** and converts them into an output signal on one of the **16** decode output lines C1 through **C16** in accordance with the truth table shown in FIGS. **7**. Looking at that table, it can be seen that, for example, when all four inputs to circuit **170** are in the 0 state an output signal is generated on line C1. All of the other C output lines are at that time inactive.

Zone decode circuit **172** receives at its inputs the high order outputs A5 through A8 of address counter **152** and provides in response thereto a signal on one of nine output lines Z1 through Z9 in accordance with the truth table shown in FIG. **8**. It can be seen by comparison of FIGS. **7** and **8** that the zone decode circuit **172** is identical to the column decode circuit **170** except that the final seven output lines are not employed for zone decoding.

The nine outputs Z1 through Z9 are fed to the inputs of the corresponding nine AND circuits **174-1** through **174-9**. The output signals generated by these AND circuits are the nine hammer select control signals S1 through S9. It can thus be seen that for each different count of address counter **152** the column and zone decode circuits generate a unique pair of output signals, one signal being from the C group and the other being from the Z group. The number of possible different combinations of C an Z signal combinations is equal to **144**, one for each different print hammer (print position) at the print head. If for any of these signal combinations a TR pulse is generated by AND **122**, the appropriate AND circuit **174** is activated to produce an S selection signal which combines with the active C selection signal to prime the corresponding hammer driver circuit at the print head by setting its flip-flop **62** (FIG. **2**).

A circuit including single-shot **86** (FIG. **3**), flip-flop **88**, OR **90** and AND **92** is provided to generate an end-of-print signal EP upon completion of the print line. When FT shifts negative, single-shot **86** produces an output pulse which resets flip-flop **88**. If during the following complete memory scan any valid data character is detected in the memory (only characters containing one or more 1 bits are valid characters) the resulting output signal from OR **90** operates to set flip-flop **88**. The resulting negative shift at the zero output thereof deconditions AND **92** so that when FT goes positive upon completion of the scan EP cannot be generated. If nothing but all-0 data characters are circulated during a memory scan, flip-flop **88** is not set and when FT goes positive at the end of the scan EP is generated. EP is fed to reset the print control flip-flop **130** (FIG. **4**) whereupon $\overline{OK}$ shifts negative and OK shifts positive to signal the external data supply device **10** that the printer is ready to receive the next line of print data.

Each of the four fire pulse single-shots **161, 163, 167** and **169** is gated by a phase-decoding AND circuit at its input whereupon each responds to FT during a different phase of the print cycle to produce its respective fire pulse. Thus, the AND which triggers single-shot **161** to produce F1 during phase **1** is fed by FT, $\overline{\Phi 1}$ and $\overline{\Phi 2}$ ($\overline{\Phi 1}$ and $\overline{\Phi 2}$ are the inverted forms of $\Phi 1$ and $\Phi 2$, respectively). Similarly, single-shot **163** is triggered to produce F2 during phase **2** on $FT \cdot \Phi 1 \cdot \overline{\Phi 2}$, single-shot **167** produces F3 during phase **3** on $FT \cdot \overline{\Phi 1} \cdot \Phi 2$ and single-shot **169** produces F4 during phase **4** on $FT \cdot \Phi 1 \cdot \Phi 2$.

Operation

With reference now to the waveform diagram of FIG. **5** and to the apparatus diagrams of FIGS. **2, 3** and **4**, a description is hereinafter given of the operation of the system through one complete print cycle.

Assuming that the data loading operation has just terminated, the first CP pulse shown in FIG. **5** is the first such pulse to occur after print control flip-flop **130** has been set by the PRT command. CP thus activates AND **132** to generate ST. CP also resets phase counter **166** to switch it from its 11 output state to its 00 output state which is indicative of phase **1**. An instant following the rise of CP and ST, at a time determined by the delay of delay circuit **146**, the phase control flip-flop **144** switches from its 0 to its 1 output state whereupon the shift register **70** and the address counter **152** begin advancing. The first advance of the former presents to the input of comparator **120** a code representation of the data character to be printed by hammer number **1** at print position **1**. At the same time, the advance of address counter **152** causes it to assume its all-0 output state whereupon since the phase counter is also in its all-0 output state comparator **102** activates AND **94** to cause AND **122** to sample the output of comparator **120**. If at that time the output of slave counter **114** represents the same character then residing in I/O register **80**, AND **122** generates TR. The latter signal activates AND **174-1** to produce S1 which, in combination with C1 which is then present at the output of column decode circuit **170**, activates AND **60-1** (FIG. **2**) which sets flip-flop **62-1**. This prepares hammer **1** to be fired when F1 is generated later in the phase.

On the next advance of the address counter and shift register, the character to be printed by hammer number **2** is presented to comparator **120** and the address counter is switched to an output of 00000001. since the lowest order pair of digits of this number (01) **does not match the** 00 output from the phase counter **166**, comparator **102** does not activate AND **94** and consequently the latter circuit does not provide a conditioning input to AND **122**. This inhibits the comparison operation. At the same time, however, AND **100** is activated to advance slave counter **114** one count.

The same procedure ensues for the next two advances of the address counter and shift register since the respective A1-A2 outputs of the address counter for each of those steps (**10** and **11**) do not match the 00 output of the phase counter.

However, on the fifth advance of the shift register and address counter the A1-A2 outputs of the latter again assume the 00 state and comparator **102** again inhibits advance of the slave counter and conditions AND **122** to sample the result of the comparison of the slave counter output with the data character to be printed by hammer number **5**.

This sequence repeats throughout the first phase of the print cycle whereupon every fourth data character presented by register **80** is compared with the output of the slave counter while the latter is advanced three counts for every four counts of the address counter. When F1 comes up, all hammers selected during the memory scan are fired.

At the beginning of the second phase ST advances the phase counter to an output state of 01 whereupon the output of comparator **120** is sampled on the second, sixth, 10th, 14th, etc., advances of the address counter while the slave counter is advanced only during the first, third, fourth, fifth, seventh, eighth, ninth, 11th, etc., advances of the address counter.

During the execution of the third phase of the print cycle, the output state of the phase counter is 10 so that AND **122** is conditioned to sample the comparison results on the third, seventh, 11th, etc. advances of the address counter while the slave counter is advanced on the first, second, fourth, fifth, sixth, eighth, etc. advances of the address counter.

It can thus be seen that during each phase of the print cycle the comparator **102** operates in response to the output counts from the address counter **152** and the phase counter **166** to control both the performance of the print comparisons and the advance of the slave counter. The comparisons effected during each given phase through this control conform to the table of FIG. **6** while the advance of the slave counter conforms with the character presentation sequence dictated by the Y to W spacing ratio also shown in FIG. **6**.

Referring again to FIG. **5**, it can be seen that at the end of the first print cycle the next CP pulse should be received at the time N if the type chain has not departed from its nominal velocity. However, as shown in FIG. **5**, the next CP pulse occurs slightly later than it should, indicating that the velocity of the type chain decreased slightly. However, due to the inhibiting effect of the output of AND **168** (FIG. **4**) during phase **4**, the resetting of flip-flop **144** does not trigger ST to begin the next print cycle. Instead, the system waits until CP is received whereupon the next print cycle is initiated and the operation of the control circuits is thus resynchronized with the movement of the type chain.

On the other hand, if the next CP pulse has occurred early (to the left of N in FIG. **5**) AND **140** (FIG. **4**) is activated to prematurely reset flip-flop **144** at a time before the address counter has reached its full phase count of **160** and the next print cycle is begun slightly ahead of the time it would have begun under nominal conditions. This again, resynchronizes the operation of the control circuits to the movement of the type chain.

It can be seen from FIG. **5** that if the velocity of the chain increases sufficiently to cause CP to be initiated prior to the time indicated by X, the address counter **152** would not be allowed to reach the **144** count necessary to set flip-flop **158** and trigger the fire pulse F4. This would cause a printing error since the print hammers which had been primed during the preceding phase four would not be fried at the end of phase **4** as they should be and instead would be fired upon the next generation of a fire pulse during some subsequent phase cycle. To prevent such errors the 1 output from

flip-flop **158** is used to condition AND **140** so that if CP occurs before the flip-flop has been set, the CP pulse does not have its usual effect and the control circuits are allowed to complete the phase **4** operation. After normal completion of phase **4** the circuits wait for the next CP pulse to trigger the next print cycle. For the same reason, AND **165** is provided to gate CP to the reset input of the phase counter **166** only after flip-flop **158** has been set. If AND **165** was not present there would be a possibility that an excessively early occurrence of CP, in switching the phase counter to the 00 output condition prior to completion of the full fourth phase memory scan, could prevent the performance of the proper comparisons required during the final portion of the memory scan and cause erroneous comparisons to be made.

The basic print cycle illustrated in FIG. **5** and just described is repeated by the system until all data in the buffer memory has been printed, as indicated by the generation of EP. When this occurs, the print control flip-flop **130** is reset and further operation of the control circuits is inhibited until a new line of data has been received and PRT begins a new series of print cycles. Of Course, CP and IND continue to advance and reset counter **110** so that synchronism with the chain is not lost.

The character generation counters **110** and **114** repetitively cycle through count sequences having a number of counts F equal to the number of characters in the type font. The slave counter runs through N/F cycles four times for each single count advance of the master counter, where N equals the number of print positions in the print line. If, as previously mentioned, the type chain is replaced by one carrying a different length font, some provision must be made to allow a corresponding alteration in the basic count cycle (F) of the counters. This may be done at the field maintenance level by a wiring change in the counter circuits or a simple switching network may be provided to permit a supervisory operator to make the appropriate circuit alterations.

It will be appreciated that various changes in the form and details of the above described preferred embodiment may be effected by persons of ordinary skill without departing from the true spirit and scope of the invention.

We claim:

1. In a system for generating sync signals in a printer having interchangeable type carriers, each of which employs a different length type font, combination comprising:

a first transducer positioned adjacent the type carrier for sensing a beginning-of-font mark thereon;

a bistable circuit connected to said first transducer and settable in response to detection of said beginning-of-font mark;

a coincidence circuit having a first input connected to the set output of said bistable circuit;

a timing disk rotatable in sync with the movement of said carrier and having character and index marks inscribed thereon, said character marks being spaced so as to pass a stationary reference point at the same repetition rate as the types on said carrier and said index marks being spaced so as to pass said reference point at $(1/n)$th said repetition rate, n being a submultiple of the number of characters in each different length type font usable with said printer;

a second transducer for sensing said character marks and generating character sync signals in response thereto; and

a third transducer for sensing said index marks and for transmitting to the second input of said coincidence circuit signals in response thereto, the outputs from said coincidence circuit being index sync pulses.

2. The system set forth in claim **1** further comprising:

a delay circuit for feeding each said index sync pulse to reset said bistable circuit at a time after said index mark has passed said third transducer.

3. The system set forth in claim **1** wherein said beginning-of-font mark is inscribed on said carrier adjacent a character type which is common to all different type fonts usable with said printer.

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