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[Continued on next page]

(54) Title: HANDLING SLOWER SCAN OUTPUTS AT OPTIMAL FREQUENCY

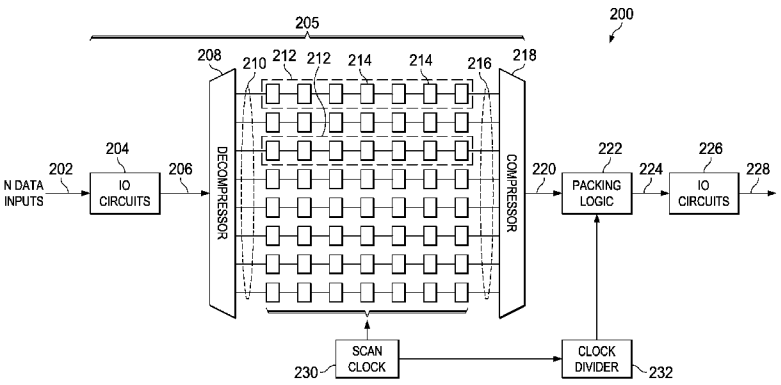

FIG. 2

(57) Abstract: In described examples of a circuit (200) for testing an integrated circuit, the circuit (200) includes a scan compression architecture (205) driven by a scan clock (230) and generates M scan outputs (220), where M is an integer. A clock divider (232) is configured to divide the scan clock (230) by k to generate k number of phase-shifted scan clocks, where k is an integer. A packing logic (222) is coupled to the scan compression architecture (205) and generates kM slow scan outputs (224) in response to the M scan outputs (220) and the k phase shifted scan clocks. The packing logic (222) further includes M number of packing elements, and each of the M packing elements receives a respective one of the M scan outputs (220). Each packing element includes k number of flip-flops, and each of the k flip-flops in a packing element receives a respective one of the M scan outputs (220). Each flip-flop receives a respective one of the k phase-shifted scan clocks, such that each flip-flop generates a respective one of the kM slow scan outputs in response to the scan output and the phase-shifted scan clock.

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HANDLING SLOWER SCAN OUTPUTS AT OPTIMAL FREQUENCY

BACKGROUND

[0001] This relates in general to scan testing, and in particular to scan testing of semiconductor devices such as integrated circuits (ICs).

[0002] Scan based techniques offer an efficient alternative to achieve high fault coverage compared to the functional pattern based testing. As the design size increases and multi-core SoCs (system-on-chip) becomes essential to drive high speed applications, test data volume and test application time grow unwieldy even in the highly efficient and balanced scan based designs. Scan compression technique is, so far, the best technique for test data volume and test time reduction during pattern execution of scan inserted designs. Few compression techniques that are implemented in SoCs include broadcast or Illinois architecture, muxed and XOR architecture or MISR (multiple input shift register) based compression architecture. A problem in today's power consuming devices is to handle the leakage power. Efforts are made to use ultra-low leakage library (ULL) cells. A ULL cell library based input/output (IO) receives a scan input on an input terminal and generates a scan output on an output terminal. The ULL cell library based IOs have relatively high inertial delay on clock and data path at the output terminal that can reach as high as the order of 30ns. The input terminal of these IOs is not affected by this timing issue because the inertial delay between clock and data path is relatively low. Under such conditions, it is not possible to drive scan operation at higher frequency, such as 30MHz or higher. Even though a very low cost tester (VLCT) can support data to be driven at higher clock frequency, slower scan output is a bottle neck to the operation. Accordingly, scan operation is not executed at optimal frequency resulting in higher test time.

SUMMARY

[0003] In described examples of a circuit for testing an integrated circuit, the circuit includes a scan compression architecture driven by a scan clock and generates M scan outputs, where M is an integer. A clock divider is configured to divide the scan clock by k to generate k number of phase-shifted scan clocks, where k is an integer. A packing logic is coupled to the scan compression architecture and generates kM slow scan outputs in response to the M scan outputs and the k number of phase shifted scan clocks. The packing logic further includes M number of packing elements, and each packing element of the M number of packing elements receives a scan output of the M scan outputs. Each packing element includes k number of flip-flops, and

each flip-flop of the k number of flip-flops in a packing element receives a scan output of the M scan outputs. Each flip-flop receives a phase-shifted scan clock of the k number of phase-shifted scan clocks, such that each flip-flop generates a slow scan output of the kM slow scan outputs in response to the scan output and the phase-shifted scan clock.

[0004] Another embodiment provides a method of testing, in which k number of phase-shifted scan clocks is generated from a scan clock, where k is an integer. A packing logic generates kM slow scan outputs from M scan outputs. The packing logic includes M number of packing elements, where M is an integer. Each packing element of the M number of packing elements generates k slow scan output in response to a scan output of the M scan outputs and the k number of phase-shifted scan clocks.

[0005] Additionally, an embodiment provides a computing device that includes a processing unit, multiple logic circuits coupled to the processing unit and a testing circuit. The testing circuit is coupled to at least one logic circuit of the multiple logic circuits. The testing circuit includes a scan compression architecture driven by a scan clock and generates M scan outputs, where M is an integer. A clock divider is configured to divide the scan clock by k to generate k number of phase-shifted scan clocks, where k is an integer. A packing logic is coupled to the scan compression architecture and generates kM slow scan outputs in response to the M scan outputs and the k number of phase shifted scan clocks. The packing logic further includes M number of packing elements, and each packing element of the M number of packing elements receives a scan output of the M scan outputs. Each packing element includes k number of flip-flops, and each flip-flop of the k number of flip-flops in a packing element receives a scan output of the M scan outputs. Each flip-flop receives a phase-shifted scan clock of the k number of phase-shifted scan clocks, such that each flip-flop generates a slow scan output of the kM slow scan outputs in response to the scan output and the phase-shifted scan clock.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a schematic of a circuit for testing an integrated circuit (IC).

[0007] FIG. 2 is a schematic of a circuit for testing an integrated circuit (IC), according to an embodiment.

[0008] FIG. 3 is a schematic of a packing logic, according to an embodiment.

[0009] FIG. 4A is a timing diagram of a clock divider, according to an embodiment.

[0010] FIG. 4B is a schematic of a packing logic, according to an embodiment.

[0011] FIG. 5 is a timing diagram of a packing logic, according to an embodiment.

[0012] FIG. 6 is a block diagram of a computing device according to an embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0013] FIG. 1 is a schematic of a circuit 100 for testing an integrated circuit (IC). The circuit 100 includes IO (input/output) circuits 104, a decompressor 108, scan chains 112, a scan clock 128, a compressor 118, an internal comparator 122 and a status register 126. The IO circuits 104 receive N data inputs 102 from a tester (not shown in FIG. 1), where N is an integer. Examples of testers include very low cost testers (VLCT) and high-end testers. The IO circuits 104 are coupled to the decompressor 108. The decompressor 108 is coupled to the scan chains 112. Each scan chain of the scan chains 112 includes scan cells, such as scan cells 114 of FIG. 1. The scan chains 112 are driven by the scan clock 128. The compressor 118 is coupled to the scan chains 112. The IO circuits 104, the decompressor 108, the scan chains 112 and the compressor 118 together form a scan compression architecture 105. The compressor 118 is coupled to the internal comparator 122. The internal comparator 122 receives an expected scan response input 124 from the tester. The status register 126 is coupled to the internal comparator 122.

[0014] In operation of the circuit 100, the IO circuits 104 receive N data inputs 102 from the tester and generate N scan inputs 106. The decompressor 108 receives the N scan inputs 106 and generates core scan inputs 110 in response to the N scan inputs 106. The core scan inputs 110 are provided to the scan chains 112. Each scan cell 114 of the scan cells shifts a core scan input of the core scan inputs 110 at a frequency of the scan clock 128. The scan chains 112 generate core scan outputs 116, in response to the core scan inputs 110 received by the scan chains 112. The compressor 118 receives the core scan outputs 116 and generates M scan outputs 120 in response to the core scan outputs 116, where M is an integer. The internal comparator 122 receives the M scan outputs 120 from the compressor 118. The internal comparator 122 also receives the expected scan response input 124 from the tester. The internal comparator 122 is configured to compare the M scan outputs 120 and the expected scan response input 124 to generate a test result 125. The test result 125 is stored in the status register 126. The status register 126 is capable of storing the test results in the form of one or more bits. In at least one example, the status register 126 includes one or more flip-flops (such as a D flip-flop) or latches. In each testing cycle, the tester generates a set of bits, which are provided as N data inputs 102 to the scan compression architecture 105, and multiple testing cycles constitute a testing pattern. The

test result 125 generated in each testing cycle is stored in the status register 126 and analyzed at the end of each testing pattern.

[0015] In some situations, the internal comparator 122 also receives unknown values (either "0" or "1"), which are termed as masked bits. In those situations, when values in M scan outputs 120 include masked bits, it is excluded from comparison with the expected scan response input 124 by the internal comparator 122. The internal comparator 122 continues to compare the normal logic "1" bits and logic "0" bits for comparison to ascertain the nature (faulty/fault-free) of the integrated circuit that is being tested. However, the use of internal comparator 122 inhibits analysis of test results at the end of each testing cycle, and the test results in circuit 100 are analyzed at the end of the testing pattern. Also, the unknown values are needed to be masked in M scan outputs 120, which add an additional overhead per scan output.

[0016] FIG. 2 is a schematic of a circuit 200 for testing an integrated circuit (IC), according to an embodiment. The circuit 200 includes first IO circuits 204, a decompressor 208, scan chains 212, a compressor 218, a packing logic 222, second IO circuits 226, a scan clock 230 and a clock divider 232. The IO circuits 204 receive N data inputs 202 from a tester (not shown in FIG. 2), where N is an integer. Examples of testers include very low cost testers (VLCT) and high-end testers. The IO circuits 204 are coupled to the decompressor 208. The decompressor 208 is coupled to the scan chains 212. Each scan chain of the scan chains 212 includes scan cells, such as scan cells 214. The scan chains 212 are driven by the scan clock 230. The compressor 218 is coupled to the scan chains 212. The IO circuits 204, the decompressor 208, the scan chains 212 and the compressor 218 together form a scan compression architecture 205. The compressor 218 is coupled to the packing logic 222. The packing logic 222 receives a signal from the clock divider 232. The packing logic 222 is coupled to the IO circuits 226.

[0017] In operation of the circuit 200, the IO circuits 204 receive N data inputs 202 from the tester and generate N scan inputs 206. The decompressor 208 receives the N scan inputs 206 and generates core scan inputs 210 in response to the N scan inputs 206. The core scan inputs 210 are provided to the scan chains 212. The scan chains 212 are driven by the scan clock 230. Each scan cell 214 of the scan cells shifts a core scan input of the core scan inputs 210 at a frequency of the scan clock 230. The scan chains 212 generate core scan outputs 216 in response to the core scan inputs 210 received by the scan chains 212. The compressor 218 receives the core scan outputs 216 and generates M scan outputs 220 in response to the core scan outputs 216, where M is an

integer. In one embodiment, M is equal to N. The clock divider 232 is configured to divide the scan clock 230 by k to generate k number of phase-shifted scan clocks, where k is an integer. For example, when frequency of scan clock 230 is 30 MHz, and k is equal to 3, the clock divider generates three phase-shifted scan clocks each of 10MHz. In one embodiment, the phase shift in the scan clocks is a function of k, such as 360^0 / k. In one embodiment, the phase shift in the scan clocks is 0 degrees, so the generated scan clocks are in same phase. The phase-shift in the clocks is predefined by a user and hardwired in the circuit 200. In at least one example, the clocks are phase shifted by 45, 90 or 180 degrees.

[0018] The packing logic 222 is coupled to the scan compression architecture 205 and generates kM slow scan outputs 224 in response to the M scan outputs 220 and k number of phase-shifted scan clocks. The features and operation of the packing logic 222 are further discussed in connection with FIG. 3. The packing logic 222 is coupled to the IO circuits 226. The IO circuits 226 are configured to generate kM data outputs 228 in response to the kM slow scan outputs 224. The N data inputs 202, the N scan inputs 206 and the M scan outputs 220 operate at a higher frequency, as compared to the kM slow scan outputs 224 and kM data outputs 228. Accordingly, the circuit 200 addresses the issue of handling kM slow scan outputs 224, even when the M scan outputs 220 are received at a faster rate, without loss of data and thereby saving time for testing the integrated circuit. In each testing cycle, the tester generates a set of bits, which are provided as N data inputs 202 to the scan compression architecture 205, and multiple testing cycles constitute a testing pattern. The packing logic 222 allows analysis of test results at the end of each testing cycle. Also, in situations when packing logic 222 receives unknown values (either “0” or “1”), which are termed as masked bits, these masked bits are treated as regular bits and do not add more overhead on the circuit 200.

[0019] FIG. 3 is a schematic of a packing logic 300, according to an embodiment. The packing logic 300 is similar in connection and operation to the packing logic 222 in the circuit 200. The packing logic 300 includes M number of packing elements (where M is an integer), such as packing elements 305A, 305B and 305M. The packing element 305M is the M^{th} packing element of the M number of packing elements. Each of the M packing elements is configured to receive a respective one of M scan outputs 320. For example, the packing element 305A receives a scan output 320A, the packing element 305B receives a scan output 320B, and the packing element 305M receives a scan output 320M. The scan output 320M is the M^{th} scan output of the M scan

outputs 320. Each packing element includes k number of flip-flops, where k is an integer. For example, the packing element 305A includes flip-flop 302a, 302b and 302k. The flip-flop 302k is the k^{th} flip-flop of the k number of flip-flops. Similarly, the packing element 305M includes flip-flops 306a, 306b and 306k. In one embodiment, the flip-flop is a latch, a combination of flip-flops, or a register. The packing logic 300 is configured to receive k number of phase shifted scan clocks from a clock divider (not shown in FIG. 3), similar to the clock divider 232 of FIG. 2. The packing logic 300 receives k phase shifted scan clocks, such as scan clock 1 (315a), scan clock 2 (315b) and scan clock k (315k). The scan clock k is the kth scan clock of the k phase shifted scan clocks. In one embodiment, the phase shift in the scan clocks is a function of k, such as 360^0 / k. In one embodiment, the phase shift in the scan clocks is 0 degrees, so the generated scan clocks are in same phase. The phase-shift in the clocks is predefined by a user and hardwired in the packing logic 300. In at least one example, the clocks are phase shifted by 45, 90 or 180 degrees. Each of the k flip-flops is configured to receive a respective one of the k phase-shifted scan clocks. For example, flip-flops 302a, 304a and 306a receive scan clock 1 (315a). Similarly, the flip-flops 302b, 304b and 306b receive scan clock 2 (315b), and flip-flops 306a, 306b and 306k receive scan clock k (315k). Each flip-flop is configured to generate a slow scan output in response to a scan output and a phase-shifted scan clock. Accordingly, each packing element generates k slow scan outputs in response to the scan output and the k number of phase-shifted scan clocks. For example, the packing element 305A generates slow scan outputs 324A1, 324A2 and 324Ak, where 324Ak is the k^{th} slow scan output. Similarly, the packing element 305B generates slow scan outputs 324B1, 324B2 and 324Bk, where 324 Bk is the k^{th} slow scan output. The packing logic 300 generates kM slow scan outputs 324 in response to the M scan outputs 320. In an embodiment, the packing logic 300 receives two scan outputs and includes two packing element, each with two flip-flops. Accordingly, the packing logic generates four slow scan outputs. The operation of packing logic is further discussed in connection with FIG. 4A and FIG. 4B.

[0020] FIG. 4A is a timing diagram of a clock divider, according to an embodiment. FIG. 4A shows the timing diagram when a clock divider, such as clock divider 232 (shown in FIG. 2), receives a scan clock (such as scan clock 230) and generates k number of phase-shifted scan clocks, where k is an integer. In at least one example, FIG. 4A shows the phase-shifted scan clocks from the clock divider 232, when k is equal to 3. The clock divider is configured to divide

the scan clock by k to generate k number of phase-shifted scan clocks. For example, if the frequency of the scan clock is 30MHz, then the clock divider would generate three phase-shifted scan clocks of 10MHz each. The scan clock 430 is received by the clock divider 232. The clock divider generates phase-shifted scan clock 1 (415a), scan clock 2 (415b) and scan clock 3 (415c). Each scan clock is phase-shifted by 120 degrees. For example, scan clock 2 (415b) is phase-shifted 120 degrees with respect to the scan clock 1(415a) and similarly, scan clock 3 (415c) is phase shifted 120 degrees with respect to the scan clock 2 (415b). In one embodiment, the phase shift in the scan clocks is a function of k, such as 360^0 / k. In one embodiment, the phase shift in the scan clocks is 0 degrees, so the generated scan clocks are in same phase. The phase-shift in the clocks is predefined by a user and hardwired in the clock divider 232. In at least one example, the clocks are phase shifted by 45, 90 or 180 degrees.

[0021] FIG. 4B is a schematic of a packing logic 400, according to an embodiment. The packing logic 400 is similar in connection and operation to the packing logic 300. The function of packing logic of FIG. 4B is when k is equal to 3 and M is equal to 4. The packing logic 400 includes four packing elements 405A, 405B, 405C and 405D. The packing logic 400 receives four scan outputs 420A, 420B, 420C and 420D. Each of the four packing elements is configured to receive a respective one of the four scan outputs 420. For example, the packing element 405A receives a scan output 420A, the packing element 405B receives a scan output 420B, and the packing element 405D receives a scan output 420D. Each packing element includes three flip-flops. For example, the packing element 405A includes flip-flop 402a, 402b and 402c. Similarly, the packing element 405C includes flip-flop 406a, 406b and 406c. In one embodiment, the flip-flop is a latch, a combination of flip-flops or a register. The packing logic 400 is configured to receive three phase shifted scan clocks from a clock divider (not shown in FIG. 4B), similar to clock divider 232 of FIG. 2. The packing logic 400 receives phase shifted scan clock 1 (415a), scan clock 2 (415b) and scan clock 3 (415c) of FIG. 4A. In one embodiment, the phase shift in the scan clocks is a function of k, such as 360^0 / k. In one embodiment, the phase shift in the scan clocks is 0 degrees, so the generated scan clocks are in same phase. The phase-shift in the clocks is predefined by a user and hardwired in the packing logic 400. In at least one example, the clocks are phase shifted by 45, 90 or 180 degrees. Each flip-flop is configured to receive a phase-shifted scan clock. For example, flip-flops 402a, 404a, 406a and 408a receive scan clock 1 (415a). Similarly, the flip-flops 402b, 404b, 406b and 408b receive

scan clock 2 (415b), and flip-flops 402c, 404c, 406c and 408c receive scan clock 3 (415c). Each flip-flop is configured to generate a slow scan output in response to a scan output and a phase-shifted scan clock. Accordingly, each packing element generates three slow scan outputs in response to the scan output and the phase-shifted scan clocks. For example, the packing element 405A generates slow scan outputs 424A1, 424A2 and 424A3. Similarly, the packing element 405B generates slow scan outputs 424B1, 424B2 and 424B3. The packing logic 400 generates 12 (4*3) slow scan outputs 424 in response to the four scan outputs 420.

[0022] FIG. 5 is a timing diagram 500 of a packing logic, according to an embodiment. The timing diagram 500 is explained with reference to FIG. 4A, FIG. 4B and packing logic 400. FIG. 5 shows the phase-shifted scan clocks and the slow scan outputs, when k is equal to 3 and M is equal to 4. FIG. 5 shows the timing diagram 500 when a clock divider, such as clock divider 232 (shown in FIG. 2), receives a scan clock 430 and generates phase-shifted scan clock 1 (415a), scan clock 2 (415b) and scan clock 3 (415c). The generation of scan clocks is discussed hereinabove in connection with FIG. 4A. The packing element 405A receives the scan output 420A. The timing diagram 500 shows three slow scan outputs, which are being generated by a packing element, such as packing element 405A in the packing logic 400 (shown in FIG. 4B). The flip-flop 402a receives the scan clock 1(415a) and the scan output 420A and generates a slow scan output 1 (424A1). Similarly, the flip-flop 402b generates a slow scan output 2 (424A2) in response to the scan clock 2(415b) and the scan output 420A. Also, the flip-flop 402c generates a slow scan output (424A3) in response to the scan clock 3(415c) and the scan output 420A. The timing diagram 500 further shows that for one scan output, the packing element generates three slow scan outputs. The scan output 420A is received by the packing logic 400 at the frequency of the scan clock 430, but the slow scan outputs (424A1-424A3) are generated at a frequency that is one-third of the frequency of the scan clock 430. Accordingly, each slow scan output is available as an output of the packing logic 400 for three pulses of the scan clock 430, so the packing logic 400 allows analysis of test results at the end of each pulse of clock cycle. The test results at the end of each pulse of clock cycle enable diagnosis of failing scan chain. Accordingly, the packing logic 400 addresses the issue of handling 12 slow scan outputs, even when the four scan outputs are received at a faster rate, without loss of data and thereby saving time for testing the integrated circuit.

[0023] FIG. 6 shows a computing device 600 of an embodiment. The computing device 600 is,

or is an integrated circuit incorporated into, a server farm, a computing device with hard-drive, a video recorder, a bluetooth device, a remote control, a keyboard, a mobile communication device (such as a mobile phone or a personal digital assistant), a personal computer, or any other type of electronic system.

[0024] In some examples, the computing device 600 can be a microcontroller, microprocessor or a system-on-chip (SoC), which includes a processing unit 612 such as a central processing unit (CPU). For example, the processing unit 612 can be a CISC-type (complex instruction set computer) CPU, RISC-type (reduced instruction set computer) CPU, or a digital signal processor (DSP). A tester 610 is coupled to the computing device 600. The tester 610 includes logic that supports testing and debugging of the computing device 600 executing the software applications 630. For example, the tester 610 is useful to emulate a defective or unavailable component(s) of the computing device 600. This allows verification of how the component(s), were it (they) actually present on the computing device 600, would perform in various situations (such as how the component(s) would interact with the software applications 630). In this way, the software applications 630 can be debugged in an environment that resembles post-production operation.

[0025] In at least one example, the processing unit 612 includes cache-memory and logic, which store and use information frequently accessed from the tester 610, so the processing unit 612 is responsible for directing complete functionality of the computing device 600. The computing device 600 includes logic circuits 615. At least one of the logic circuits 615 is coupled to a testing circuit 620. The testing circuit 620 is analogous to the circuit 200 in connection and operation. The testing circuit operates in conjunction with the tester 610. The testing circuit 620 addresses the issue of handling kM slow scan outputs, even when the M scan outputs are received at a faster rate, without loss of data and thereby saving time for testing the integrated circuit, where k, M and N are integers. In each testing cycle, the tester 610 generates a set of bits, which are provided as N data inputs to the testing circuit 620, and multiple testing cycles constitute a testing pattern. The testing circuit 620 allows analysis of test results at the end of each testing cycle. Also, in situations when testing circuit 620 receives unknown values (either “0” or “1”), which are termed as masked bits, the testing circuit 620 treats them as regular bits and does not add more overhead on the computing device 600.

[0026] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit comprising:

a scan compression architecture driven by a scan clock and configured to generate M scan outputs, wherein M is an integer;

a clock divider configured to divide the scan clock by k to generate k number of phase-shifted scan clocks, wherein k is an integer; and

a packing logic coupled to the scan compression architecture and configured to generate kM slow scan outputs in response to the M scan outputs and the k number of phase shifted scan clocks;

wherein the packing logic includes: M number of packing elements, each packing element of the M number of packing elements configured to receive a scan output of the M scan outputs; and k number of flip-flops in each packing element, each flip-flop of the k number of flip-flops in a packing element configured to receive a scan output of the M scan outputs and configured to receive a phase-shifted scan clock of the k number of phase-shifted scan clocks, such that each flip-flop generates a slow scan output of the kM slow scan outputs in response to the scan output and the phase-shifted scan clock.

2. The circuit of claim 1, wherein each packing element generates k slow scan outputs in response to the scan output and the k number of phase-shifted scan clocks.

3. The circuit of claim 1, wherein the scan compression architecture further includes:

a first plurality of input/output (IO) circuits configured to receive N data inputs and configured to generate N scan inputs, wherein N is an integer;

a decompressor coupled to the first plurality of IO circuits and configured to receive the N scan inputs;

a compressor coupled to the decompressor and configured to generate the M scan outputs; and

a plurality of scan chains coupled between the decompressor and the compressor, wherein each scan chain of the plurality of scan chains includes a plurality of scan cells.

4. The circuit of claim 1, further comprising a second plurality of IO circuits coupled to the packing logic and configured to generate kM data outputs in response to the kM slow scan outputs from the packing logic.

5. The circuit of claim 1, wherein the plurality of scan chains is driven by the scan clock.

6. The circuit of claim 1, wherein the decompressor is configured to generate a plurality of core scan inputs in response to the N scan inputs.

7. The circuit of claim 1, wherein the plurality of scan chains is configured to receive the plurality of core scan inputs, wherein each scan cell of the plurality of scan cells is configured to shift a core scan input of the plurality of core scan inputs at a frequency of the scan clock.

8. The circuit of claim 1, wherein the plurality of scan chains is configured to generate a plurality of core scan outputs in response to the plurality of core scan inputs.

9. The circuit of claim 1, wherein the compressor is configured to generate the M scan outputs in response to the plurality of core scan outputs.

10. A method of testing comprising:

generating k number of phase-shifted scan clocks from a scan clock, wherein k is an integer;

configuring a packing logic to generate kM slow scan outputs from M scan outputs, wherein the packing logic includes M number of packing elements, wherein M is an integer; and

configuring each packing element of the M number of packing elements to generate k slow scan output in response to a scan output of the M scan outputs and the k number of phase-shifted scan clocks.

11. The method of claim 10, further comprising:

generating N scan inputs in response to N data inputs;

generating a plurality of core scan inputs in response to the N scan inputs;

generating a plurality of core scan outputs in response to the plurality of core scan inputs; and

generating the M scan outputs in response to the plurality of core scan outputs.

12. The method of claim 10, wherein each packing element includes k number of flip-flops.

13. The method of claim 10, further comprising configuring each flip-flop of the k number of flip-flops in a packing element to generate a slow scan output in response to the scan output received at the packing element and to a phase-shifted scan clock of the k number of phase-shifted scan clocks.

14. The method of claim 10, further comprising a plurality of scan chains configured to generate a plurality of core scan outputs in response to the plurality of core scan inputs, each

scan chain of the plurality of scan chains includes a plurality of scan cells.

15. The method of claim 10, wherein each scan cell of the plurality of scan cells is configured to shift a core scan input of the plurality of core scan inputs at a frequency of the scan clock.

16. The method of claim 10, further comprising generating kM data outputs in response to the kM slow scan outputs.

17. A computing device comprising:

a processing unit;

a plurality of logic circuits coupled to the processing unit; and

a testing circuit coupled to at least one logic circuit of the plurality of logic circuits, the testing circuit including: a scan compression architecture driven by a scan clock and configured to generate M scan outputs, wherein M is an integer; a clock divider configured to divide the scan clock by k to generate k number of phase-shifted scan clocks, wherein k is an integer; and a packing logic coupled to the scan compression architecture and configured to generate kM slow scan outputs in response to the M scan outputs and the k number of phase shifted scan clocks;

wherein the packing logic includes: M number of packing elements, each packing element of the M number of packing elements configured to receive a scan output of the M scan outputs; and k number of flip-flops in each packing element, each flip-flop of the k number of flip-flops in a packing element configured to receive a scan output of the M scan outputs and configured to receive a phase-shifted scan clock of the k number of phase-shifted scan clocks, such that each flip-flop generates a slow scan output of the kM slow scan outputs in response to the scan output and the phase-shifted scan clock.

18. The computing device of claim 17, wherein the scan compression architecture further includes:

a first plurality of input/output (IO) circuits configured to receive N data inputs and configured to generate N scan inputs, wherein N is an integer;

a decompressor coupled to the first plurality of IO circuits and configured to receive the N scan inputs;

a compressor coupled to the decompressor and configured to generate the M scan outputs; and

a plurality of scan chains coupled between the decompressor and the compressor, wherein

each scan chain of the plurality of scan chains includes a plurality of scan cells.

19. The computing device of claim 17, further comprising a second plurality of IO circuits coupled to the packing logic and configured to generate kM data outputs in response to the kM slow scan outputs from the packing logic.

20. The computing device of claim 17, wherein the plurality of scan chains is configured to receive the plurality of core scan inputs, wherein each scan cell of the plurality of scan cells is configured to shift a core scan input of the plurality of core scan inputs at a frequency of the scan clock.

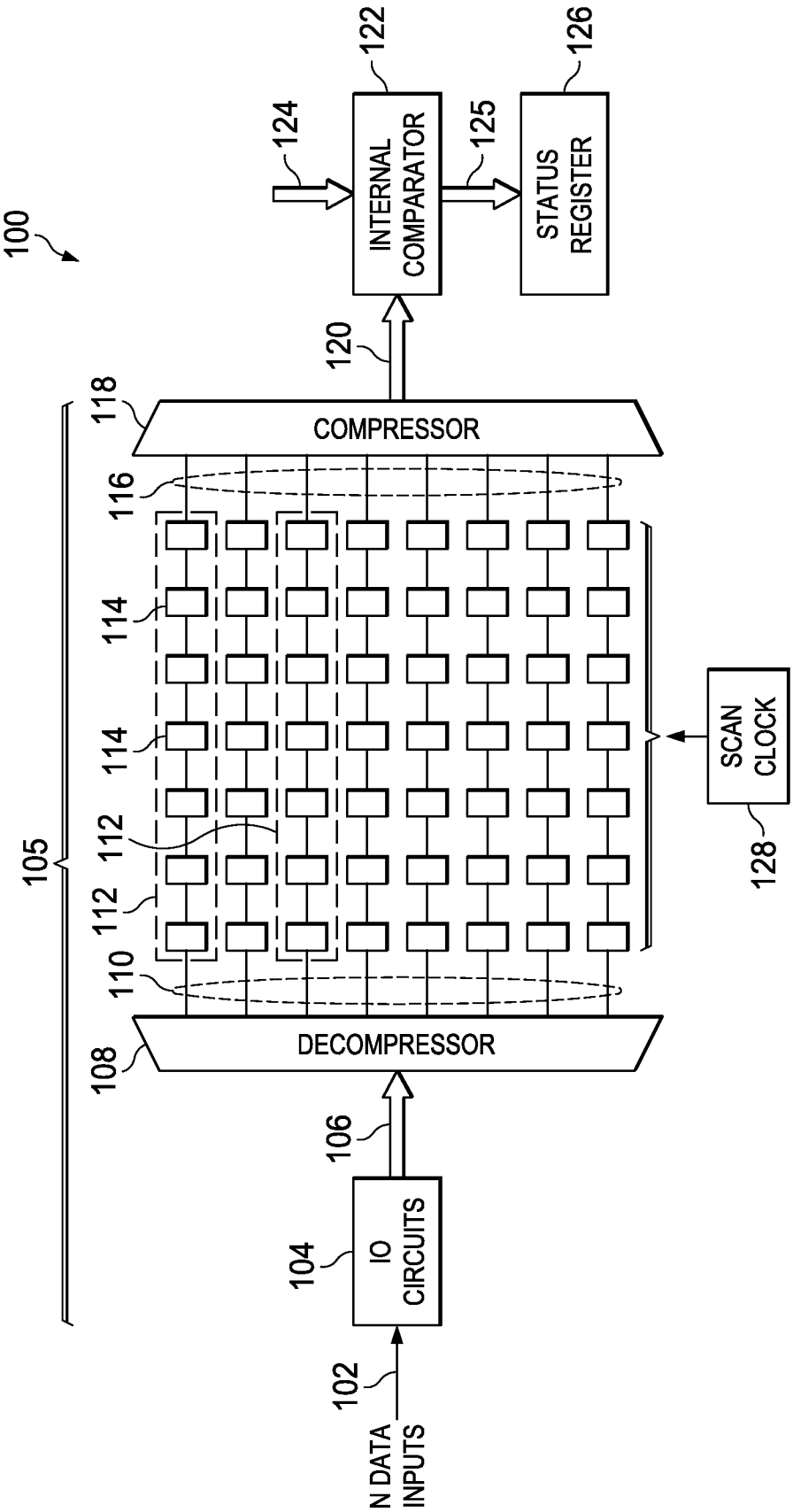
100
122
126
124
INTERNAL COMPARATOR
125
STATUS REGISTER
120
118
COMPRESSOR
116
114
114
112
112
105
110
SCAN CLOCK
128
DECOMPRESSOR
108
106
104
IO CIRCUITS
102
N DATA INPUTS

FIG. 1

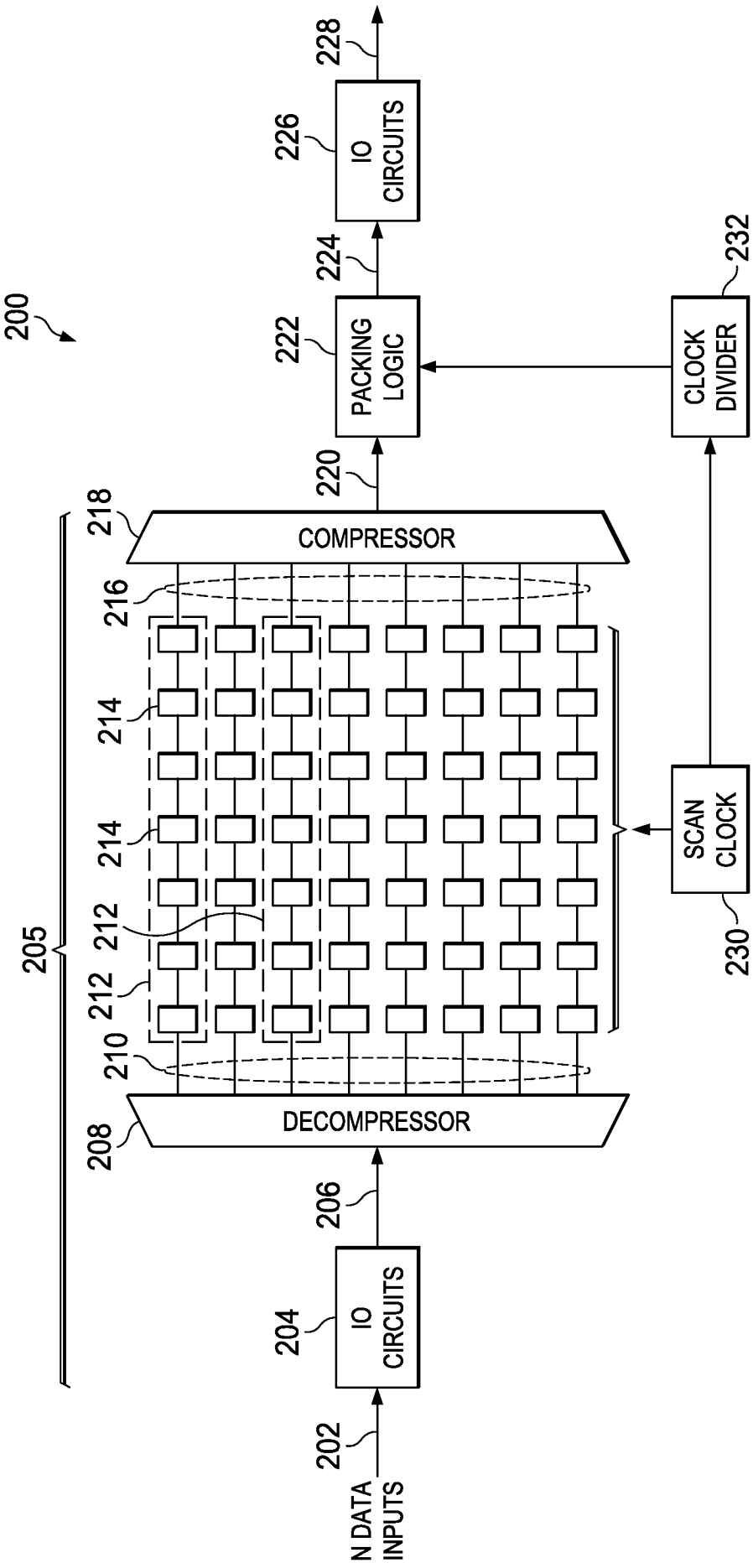
200
N DATA INPUTS
202
IO CIRCUITS
204
206
DECOMPRESSOR
208
210
212
212
214
214
216
COMPRESSOR
218
220
PACKING LOGIC
222
224
IO CIRCUITS
226
228
205
SCAN CLOCK
230
CLOCK DIVIDER
232

FIG. 2

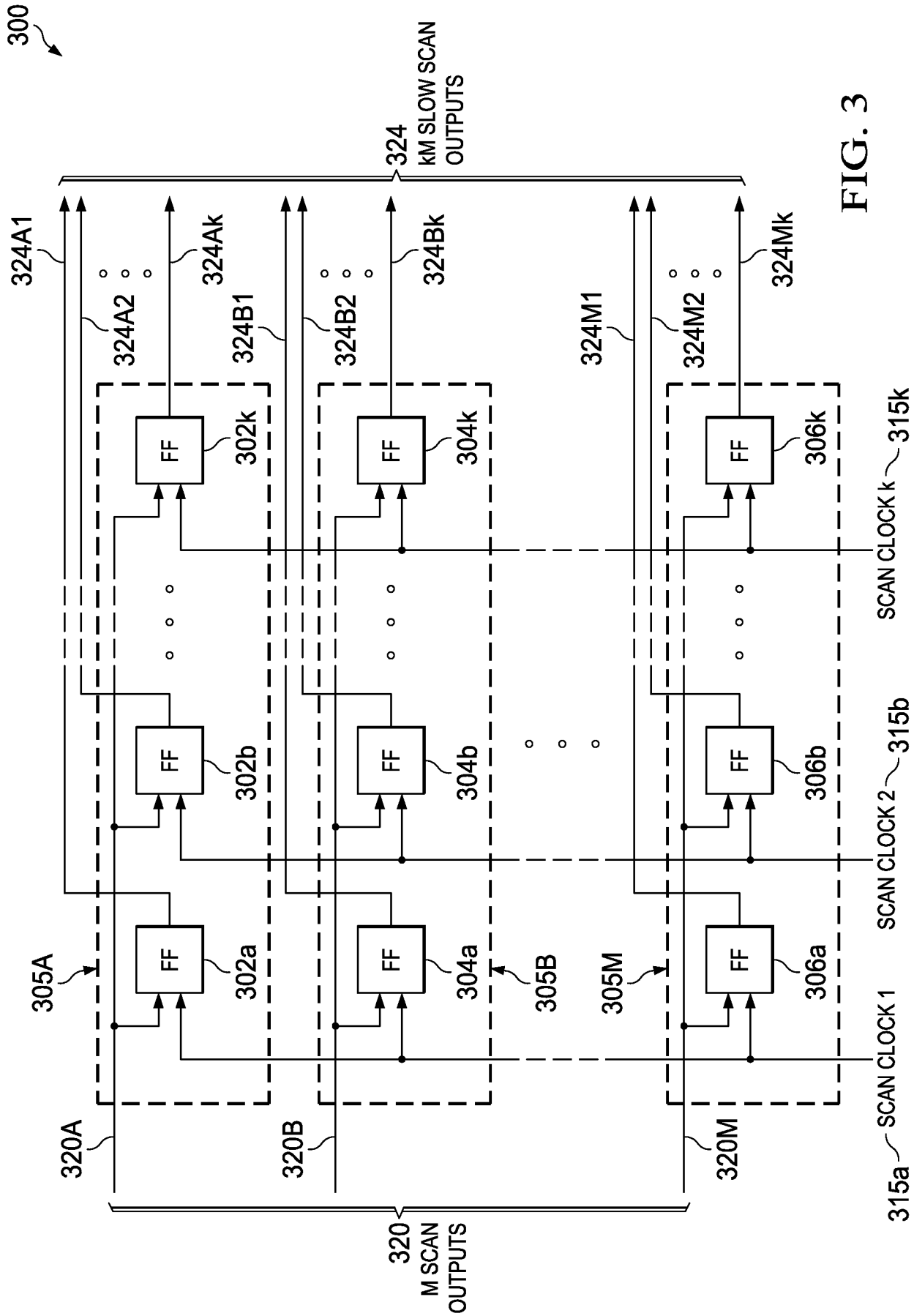
300
324
kM SLOW SCAN
OUTPUTS
324A1
324A2
324Ak
324B1
324B2
324Bk
324M1
324M2
324Mk
FF
302k
304k
306k
302b
304b
306b
302a
304a
306a
305A
305B
305M
315k
SCAN CLOCK k
315b
SCAN CLOCK 2
SCAN CLOCK 1
315a
320A
320B
320M
320
M SCAN
OUTPUTS

FIG. 3

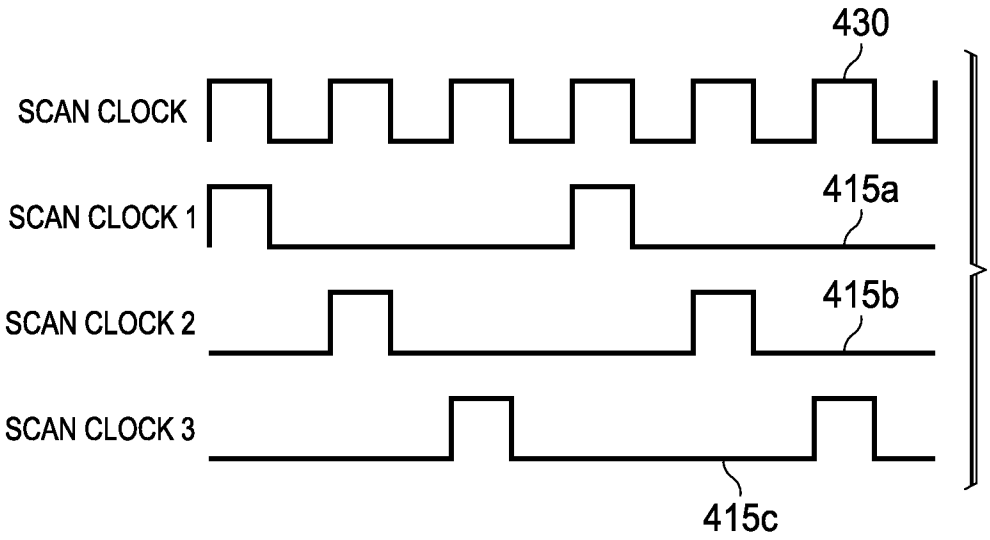
430
SCAN CLOCK
SCAN CLOCK 1
415a
SCAN CLOCK 2
415b
SCAN CLOCK 3
415c

FIG. 4A

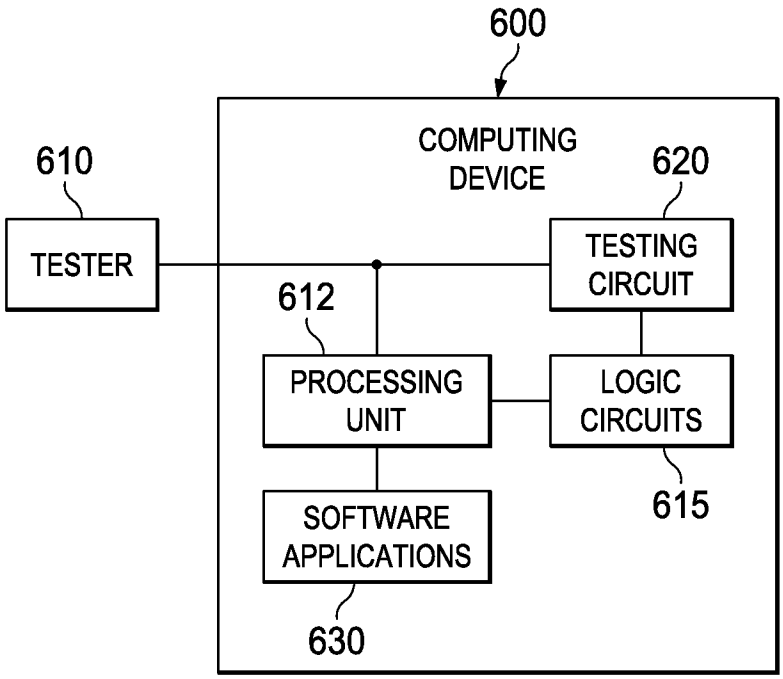
600
COMPUTING DEVICE
610
TESTER
620
TESTING CIRCUIT
612
PROCESSING UNIT
LOGIC CIRCUITS
615
SOFTWARE APPLICATIONS
630

FIG. 6

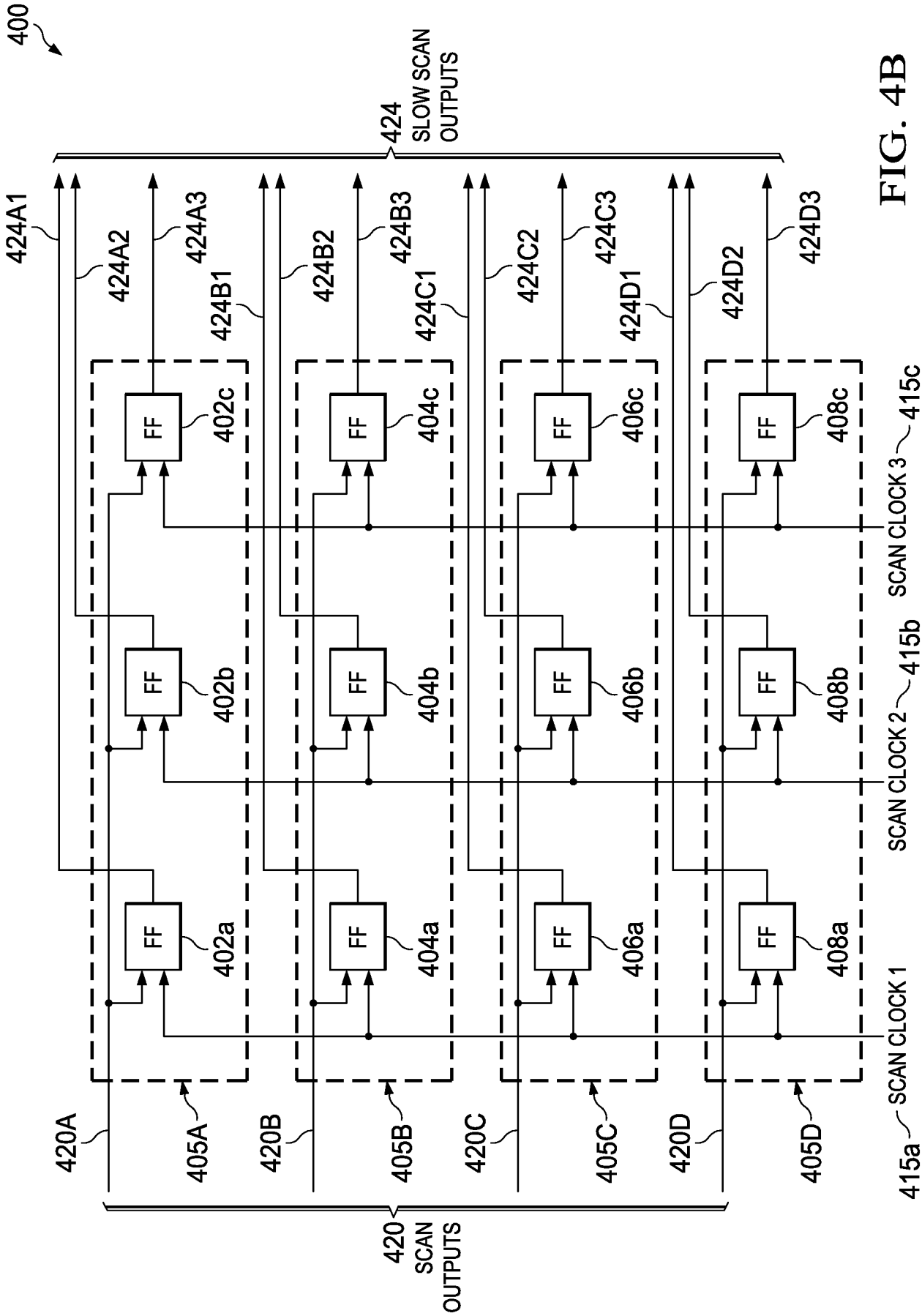
400
424
SLOW SCAN
OUTPUTS
424A1
424A2
424A3
424B1
424B2
424B3
424C1
424C2
424C3
424D1
424D2
424D3
FF
402c
404c
406c
408c
402b
404b
406b
408b
402a
404a
406a
408a
415c
SCAN CLOCK 3
415b
SCAN CLOCK 2
SCAN CLOCK 1
415a
420A
420B
420C
420D
405A
405B
405C
405D
420
SCAN
OUTPUTS

FIG. 4B

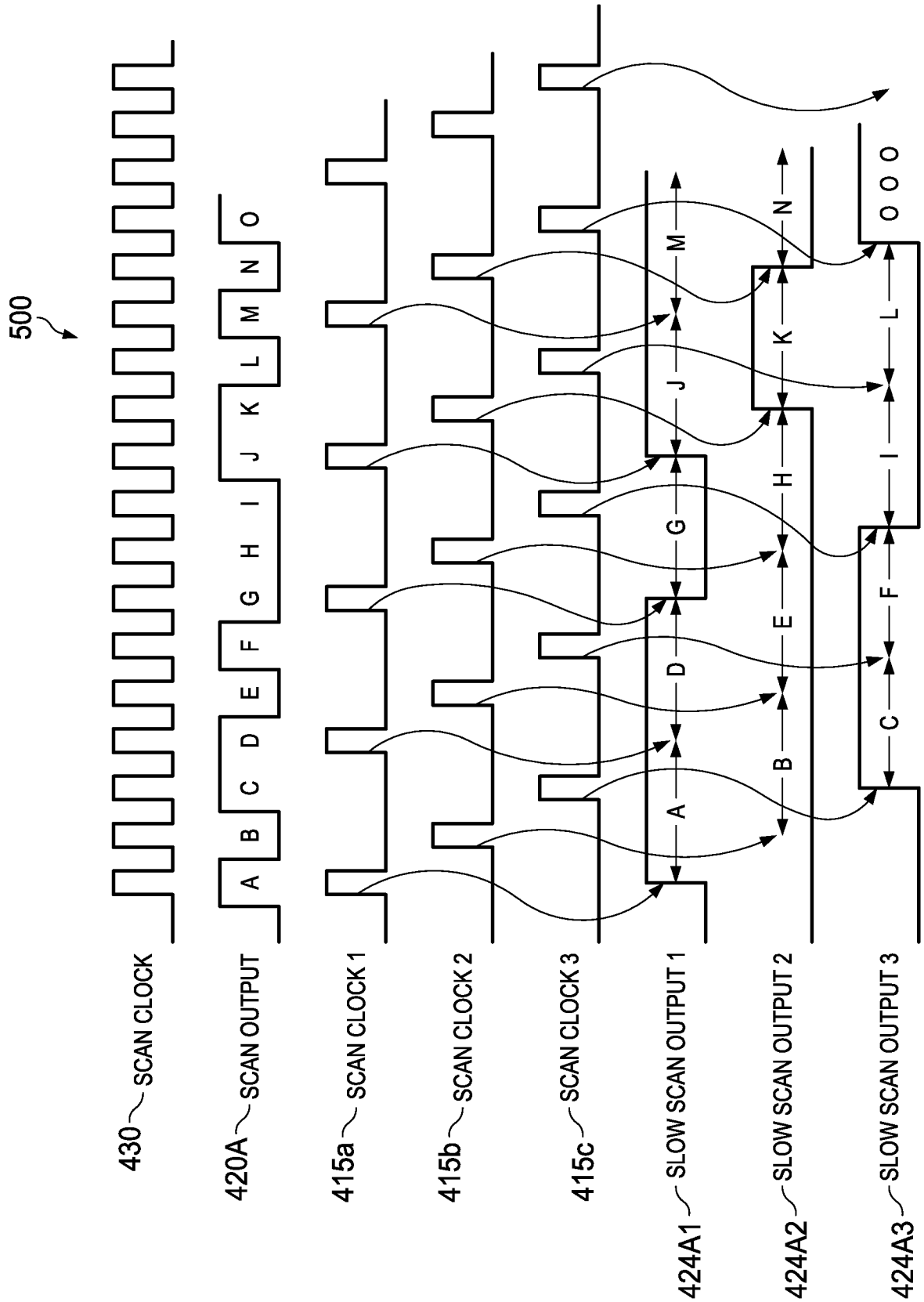
500
430 SCAN CLOCK
420A SCAN OUTPUT
A B C D E F G H I J K L M N O
415a SCAN CLOCK 1
415b SCAN CLOCK 2
415c SCAN CLOCK 3
424A1 SLOW SCAN OUTPUT 1
424A2 SLOW SCAN OUTPUT 2
424A3 SLOW SCAN OUTPUT 3
A B C D E F G H I J K L M N O O O

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/073090

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/28 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R 31/28, 19/00, G06F 11/16-11/25

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/0307750 A1 (TEXAS INSTRUMENTS INCORPORATED) 15.12.2011	1-20
A	US 2012/0331362 A1 (RAMESH C.TEKUMALLA) 27.12.2012	1-20
A	US 2013/0159800 A1 (TEXAS INSTRUMENTS INCORPORATED) 20.01.2013	1-20
A	US 2011/0167310 A1 (FREESCALE SEMICONDUCTOR, INC.) 07.07.2011	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 April 2015 (02.04.2015)	09 April 2015 (09.04.2015)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer N. Shutov Telephone No. (499) 240-25-91

Form PCT/ISA/210 (second sheet) (January 2015)