

(51) International Patent Classification:
G06F 3/06 (2006.01)(21) International Application Number:
PCT/US2015/030873(22) International Filing Date:
14 May 2015 (14.05.2015)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **HEWLETT PACKARD ENTERPRISE DEVELOPMENT LP** [US/US]; 11445 Compaq Center Drive West, Houston, TX 77070 (US).(72) Inventor: **MARTINEZ, Boris N.**; 11311 Chinden Blvd, Boise, Idaho 83714 (US).(74) Agent: **SU, Benjamin**; Hewlett Packard Enterprise, 3404 E. Harmony Road, Mail Stop 79, Fort Collins, CO 80528 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,

HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

- with international search report (Art. 21(3))

(54) Title: DATA TRANSFERS BASED ON STATE TRANSITION DETECTIONS

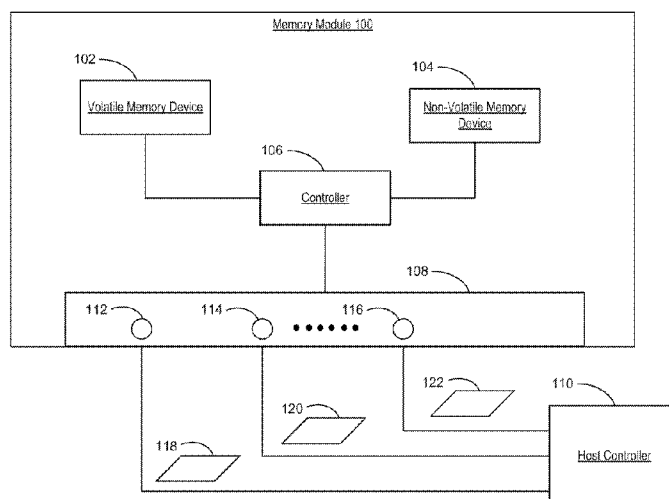


FIG. 1

(57) Abstract: An example memory module includes a data communication interface, a volatile memory device, a non-volatile memory device, and a controller coupled to the data communication interface, the volatile memory device, and the non-volatile memory device. The controller is to store data to the volatile memory device. The data is received via the data communication interface from a host controller. The controller is also to detect a first state transition of a first signal and a second state transition of a second signal via the data communication interface. The controller is further to determine whether to transfer the data from the volatile memory device to the non-volatile memory device based on a timing of the second state transition relative to the first state transition.

DATA TRANSFERS BASED ON STATE TRANSITION DETECTIONS

BACKGROUND

[0001] A computing device, such as a desktop computer, may include a plurality of electronic components. For example, an electronic component may be a power supply. As another example, an electronic component may be a storage device controller.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Some examples of the present application are described with respect to the following figures:

[0003] FIG. 1 is a block diagram of a memory module to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to an example;

[0004] FIG. 2 is a block diagram of an electronic device including a memory module to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to an example;

[0005] FIG. 3 is a timing diagram of state transitions of a clock enable signal and a reset signal, according to an example;

[0006] FIG. 4 is a block diagram of a memory module to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to another example; and

[0007] FIG. 5 is a flowchart illustrating a method of operation at a memory module to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to an example.

DETAILED DESCRIPTION

[0008] An example storage device controller may be a redundant array of independent disks (RAID) controller. The RAID controller may include on-board memory modules to store data associated with the RAID, such as RAID configuration, write requests, etc. In some examples, a RAID controller may include a memory module, such as a non-volatile dual in-line memory module (NVDIMM), to store the data as non-volatile data so that the data can be retrieved for subsequent use. A host controller of the RAID controller may store the data to the NVDIMM. In the event of a hot removal of the RAID controller from a computing device (i.e., the computing device is powered on and in operation when the RAID controller is removed), the hot removal of the RAID controller may trigger the NVDIMM to store data received from the host controller as non-volatile data. However, the NVDIMM may store the data as non-volatile data before all the data is transferred/flushed to the NVDIMM from the host controller. Thus, a likelihood of data corruption may be increased.

[0009] Examples described herein provide a memory module to save data as non-volatile data based on detections of state transitions of a clock enable signal and a reset signal. For example, a memory module may include a data communication interface, a volatile memory device, a non-volatile memory device, and a controller. The controller may be coupled to the data communication interface, the volatile memory device, and the non-volatile memory device. The controller is to store data to the volatile memory device. The data is received via the data communication interface from a host controller. The controller is to detect a first state transition of a first signal and a second state transition of a second signal via the data communication interface. The controller is further to determine whether to transfer the data from the volatile memory device to the non-volatile memory device based on a timing of the second state transition relative to the first state transition. In this manner, examples described herein may reduce a likelihood of data corruption.

[0010] Referring now to the figures, FIG. 1 is a block diagram of a memory module 100 to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to an example. Memory module 100 may be, an NVDIMM or any other memory device that retains data even after power is lost. Memory module 100 may include a volatile memory device 102, a non-volatile memory device 104, a controller 106, and a data communication interface 108.

[0011] Volatile memory device 102 may be a data storage device or circuit that loses stored data when power supplied to the data storage device or circuit is removed/lost. As an example, volatile memory device 102 may be implemented using dynamic random-access memory. Non-volatile memory device 104 may be a data storage device or circuit that retains stored data even when power supplied to the data storage device or circuit is removed/lost. As an example, non-volatile memory device 104 may be implemented using flash memory.

[0012] Controller 106 may be, for example, a semiconductor-based microprocessor, a field-programmable gate array (FPGA), an application specific integrated circuit (ASIC), and/or other hardware devices suitable for retrieval and execution of instructions stored in a computer-readable storage medium. Data communication interface 108 may be an electrical connector to enable memory module 100 to communicate with other electronic devices, such as a host controller 110.

[0013] Data communication interface 108 may include a plurality of electrical connectors or pins to sense signals from host controller 110, detect state transitions of the signals, receive data from host controller 110, and transmit data to host controller 110. For example, data communication interface 108 may include a first electrical contact 112, a second electrical contact 114, and a third electrical contact 116. As used herein, a state transition is a change in logic value of a signal.

[0014] Host controller 110 may be a device or circuit that connects a host electronic device to an electronic device, such as memory module 100, that is a part of the host electronic device. The host electronic device may control the electronic device via the host controller. As described in more detail in FIG. 2, memory module 100 and host controller 110 may be located in the same electronic device.

[0015] During operation, controller 106 may sense signals, such as a first signal asserted by host controller 110 via data communication interface 108. For example, controller 106 may sense a clock enable signal 118 and detect a state transition of clock enable signal 118 via first electrical contact 112. Controller 106 may also sense a reset signal 120 and detect a state transition of reset signal 120 via second electrical contact 114. Controller 106 may receive data 122 from host controller 110 via third electrical contact 116. As described in more detail in FIGs. 2-6, controller 106 may store data 122 in volatile memory device 102 as volatile data. Based on a timing of a state transition of 118 reset signal relative to a state transition of clock enable signal 118, controller 106 may determine whether to transfer data 122 from volatile memory device 102 to non-volatile memory device 104 via copying.

[0016] FIG. 2 is a block diagram of an electronic device 200 including a memory module to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to an example. Electronic device 200, for example, may be a RAID controller or other storage system controller.

[0017] Electronic device 200 may include memory module 100 of FIG. 1, host controller 110, a power storage device 202, and a power supply detection circuit 204. Power storage device 202 may be any device that stores power (e.g., electricity) and provides the stored power to an electronic device. As an example, power storage device 202 may be implemented using a nickel-metal hydride battery or a lithium ion battery. Power supply detection circuit 204 may be a circuit that detects whether power, in the form of alternating current (AC), is

being provided to a power supply 210. Power supply 210 may provide power to electronic device 200 in the form of direct current (DC). Power supply detection circuit 204 may assert a save signal 206 to memory module 100 via a fourth electrical contact 208 of data communication interface 108. Power supply detection circuit 204 may also assert save signal 206 to host controller 110. The state transition of save signal 206 may indicate the presence of AC provided power supply 210.

[0018] During operation, electronic device 200 may be plugged into or connected to a computing device 214 via a data connector of computing device 214, such as a peripheral component interconnect express (PCIe) slot. Computing device 214 may be, for example, a web-based server, a local area network server, a cloud-based server, a desktop computer, an all-in-one system, or any other electronic device suitable for receiving an electronic device, such as electronic device 200, in a data connector.

[0019] Electronic device 200 may experience a power loss. The power loss may be triggered by a power down event at computing device 214 (e.g., power supply 210 malfunctioning, computing device 214 powering off, etc.). Electronic device 200 may still be physically connected to computing device 214 during a power down event. The power loss may also be triggered by a hot removal of electronic device 200 from computing device 214.

[0020] When the power loss is triggered by a power down event, controller 106 may store data received from host controller 110, such as data 122, to non-volatile memory device 104 so that the data may be restored for subsequent use. When the power loss is triggered by a hot removal of electronic device 200, controller 106 may maintain the data in volatile memory device 102 and may not transfer the data to non-volatile memory device 104 as the data may be incomplete or corrupted. Thus, when memory module 100 is powered off, the data stored in volatile memory device 102 is lost.

[0021] Operation of electronic device 200 is now described with reference to a power down event. During a power down event, the AC power supplied to

power supply 210 is lost. Power supply detection circuit 204 may detect the loss of the AC power. Power supply detection circuit 204 may trigger a state transition of save signal 206 to indicate the loss of the AC power. In response to detecting the state transition of save signal 206, for example, from a logic high to a logic low, host controller 110 may initiate a data flushing operation by flushing or transmitting data 122 from a buffer 212 of host controller 110 to memory module 100 via third electrical contact 116. In response to detecting the state transition of save signal, controller 106 may store data 122 to volatile memory device 102 as volatile data.

[0022] Power supply 210 may continue to provide power to electronic device 200 for a brief period of time so that the data flushing operation may be completed. For example, power supply 210 may continue to provide power to electronic device 200 for 6 milliseconds during a power down event.

[0023] When host controller 110 has completed flushing all of data 122 to memory module 100, host controller 110 may trigger a state transition of clock enable signal 118, such as from a logic high to a logic low. In response to detecting the state transition of clock enable signal 118, controller 106 may place memory module 100 into a self-refresh mode. During the self-refresh mode, memory module 100 may not receive any data from host controller 110.

[0024] When power supply 210 no longer provides power to electronic device 200, components of electronic device 200, such as host controller 110, may be powered off except memory module 100 and power storage device 202. Power storage device 202 may provide power to memory module 100 for a period of time after power is no longer supplied to electronic device 200. For example, the period of time may be 10 milliseconds. The loss of power from power supply 210 may trigger a state transition of reset signal 120, for example, from a logic high to logic low as host controller 110 is powered off.

[0025] Operation of electronic device 200 is now described with reference to a hot removal of electronic device 200 from computing device 214. When electronic device 200 is physically hot removed from computing device 214,

power supplied to electronic device 200 may be lost. The loss of power may trigger a state transition of save signal 206, a state transition of clock enable signal 118, and a state transition of reset signal 120 as power supply detection circuit 204 and host controller 110 are powered off. Thus, the state transition of reset signal 120 may be triggered prior to all of data 122 is transmitted to memory module 100.

[0026] To distinguish between a power down event and a hot removal of electronic device 200, controller 106 may compare a timing of the state transition of reset signal 120 relative to the state transition of clock enable signal 118. Based on the comparison, controller 106 may determine whether to transfer data 122 from volatile memory device 102 to non-volatile memory device 104. For example, when the state transition of reset signal 120 is detected after the state transition of clock enable signal 118 and after the expiration of a waiting period that begins at the state transition of clock enable signal 118, the timing of the state transition of reset signal 120 may indicate a power down event. Thus, controller 106 may transfer data 122 stored in volatile memory device 102 to non-volatile memory device 104. The waiting period is described in more detail in FIG. 3.

[0027] When the state transition of reset signal 120 is detected prior to the expiration of a waiting period, the timing of the state transition of reset signal 120 may indicate a hot removal of electronic device 200. Thus, controller 106 may skip transferring data 122 to non-volatile device 104 by maintaining data 122 in volatile device 102.

[0028] FIG. 3 is a timing diagram 300 of state transitions of clock enable signal 118 and reset signal 120, according to an example. Timing diagram 300 is described with reference to memory module 100 of FIGs. 1-2.

[0029] At time T0, controller 106 may detect a state transition of reset signal 120 from a logic high to a logic low. At time T1 that is subsequent to time T0, controller 106 may detect a state transition of clock enable signal 118 from a logic high to a logic low. In response to detecting the state transition of reset

signal 120 prior to the state transition of clock enable signal 118, controller 106 may determine that a hot removal of electronic device 200 has occurred. Thus, controller 106 may not transfer data 122 from volatile memory device 102 to non-volatile memory device 104.

[0030] In some examples, during a hot removal of electronic device 200, controller 106 may detect the state transition of reset signal 120 after the state transition of clock enable signal 118 even though the state transition of reset signal 120 is triggered before or substantially at the same time as the state transition of clock enable signal 118 is triggered. The delay in detecting the state transition of reset signal 120 may be caused by routing delay of reset signal 120. To reduce the likelihood of transferring incomplete or corrupted data 122 to non-volatile memory device 104, controller 106 may initiate a waiting period 302 that begins at the state transition of clock enable signal 118, such as at time T1. Waiting period 302 may be set for a period of time to account for delays associated with routing reset signal 120 from host controller 110 to data communication interface 108. Thus, waiting period 302 may expire after time T1. For example, waiting period 302 may begin at time T1 and expire at time T3.

[0031] Controller 106 may compare the timing of state transition of reset signal 120 to waiting period 302. Based on the comparison, controller 106 may determine whether to transfer data 122 from volatile memory device 102 to non-volatile memory device 104. For example, when controller 106 detects a state transition of reset signal 120 prior to the expiration of waiting period 302, controller 106 may determine that a hot removal of electronic device 200 has occurred. For example, a state transition of reset signal 120 may be detected at time T2 that is prior to the expiration of waiting period 302 but after the state transition of clock enable signal 118 at time T1. Thus, controller 106 may not transfer data 122 from volatile memory device 102 to non-volatile memory device 104.

[0032] When controller 106 detects a state transition of reset signal 120 after the expiration of waiting period 302, controller 106 may determine that a power

down event at computing device has occurred. For example, controller 106 may detect a state transition of reset signal 120 at time T4 that is after the expiration of waiting period 302 at time T3. Thus, controller 106 may transfer data 122 from volatile memory device 102 to non-volatile memory device 104.

[0033] FIG. 4 is a block diagram of a memory module 400 to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to another example. Memory module 400 may implement memory module 100 of FIGs. 1-2. Memory module 400 may include a controller 402 and a computer-readable storage medium 404.

[0034] Controller 402 may be similar to controller 106. Controller 402 may fetch, decode, and execute instructions 406-412 to control a process of transferring data from a volatile memory device to a non-volatile memory device. As an alternative or in addition to retrieving and executing instructions, controller 402 may include at least one electronic circuit that includes electronic components for performing the functionality of instructions 406, 408, 410, 412 or a combination thereof.

[0035] Computer-readable storage medium 404 may be any electronic, magnetic, optical, or other physical storage device that contains or stores executable instructions. Thus, computer-readable storage medium 404 may be, for example, Random Access Memory (RAM), an Electrically Erasable Programmable Read-Only Memory (EEPROM), etc. In some examples, computer-readable storage medium 404 may be a non-transitory storage medium, where the term "non-transitory" does not encompass transitory propagating signals. As described in detail below, computer-readable storage medium 404 may be encoded with a series of processor executable instructions 406-412 for detecting a state transition of a clock enable signal, detecting a state transition of a reset signal, comparing a timing of the state transition of the reset signal to a waiting period that begins at the state transition of the clock enable signal, and determining whether to transfer data from a volatile memory device to a non-volatile memory device based on the comparison.

[0036] Clock enable signal state transition detection instructions 406 may detect a state transition of a clock enable signal. For example, referring to FIG. 1, controller 106 may sense clock enable signal 118 and detect a state transition of clock enable signal 118 via first electrical contact 112. Reset signal state transition detection instructions 408 may detect a state transition of a reset signal. For example, controller 106 may also sense reset signal 120 and detect a state transition of reset signal 120 via second electrical contact 114.

[0037] State transition timing comparison instructions 410 may compare a timing of a state transition of a reset signal to a waiting period that begins at a state transition of the clock enable signal. For example, referring to FIG. 3, controller 106 may compare the timing of state transition of reset signal 120 to waiting period 302. Data transfer determination instructions 412 may determine whether to transfer data from a volatile memory device to a non-volatile memory device based on the comparison. For example, referring to FIG. 3, based on the comparison, controller 106 may determine whether to transfer data 122 from volatile memory device 102 to non-volatile memory device 104.

[0038] FIG. 5 is a flowchart illustrating a method 500 of operation at a memory module to transfer data from a volatile memory device to a non-volatile memory device based on state transition detections of a clock enable signal and a reset signal, according to an example. Method 500 may be implemented by memory module 100 of FIGs. 1-2 and/or memory module 400 of FIG. 4.

[0039] Method 500 includes sensing, via a data communication interface of a memory module, a plurality of signals including a save signal, a clock enable signal, and a reset signal, at 502. For example, referring to FIG. 1, data communication interface 108 may include a plurality of electrical connectors or pins to sense signals from host controller 110, detect state transitions of the signals, receive data from host controller 110, and transmit data to host controller 110. Method 500 also includes in response to detecting a state transition of the save signal, storing data received from a host controller to a volatile memory device of the memory module, at 504. For example, referring to FIG. 2, in

response to detecting the state transition of save signal, controller 106 may store data 122 to volatile memory device 102 as volatile data.

[0040] Method 500 further includes in response to detecting a state transition of the reset signal prior to an expiration of a waiting period associated with a state transition of the clock enable signal, maintaining the data in the volatile memory device, at 506. For example, referring to FIG. 2, when the state transition of reset signal 120 is detected prior to the expiration of a waiting period, the timing of the state transition of reset signal 120 may indicate a hot removal of electronic device 200. Thus, controller 106 may skip transferring data 122 to non-volatile device 104 by maintaining data 122 in volatile device 102. Method 500 further includes in response to detecting the state transition of the reset signal after the expiration of the waiting period, transferring the data from the volatile memory device to a non-volatile memory device of the memory module, at 508. For example, referring to FIG. 3, when controller 106 detects a state transition of reset signal 120 after the expiration of waiting period 302, controller 106 may determine that a power down event at computing device has occurred. For example, controller 106 may detect a state transition of reset signal 120 at time T4 that is after the expiration of waiting period 302 at time T3. Thus, controller 106 may transfer data 122 from volatile memory device 102 to non-volatile memory device 104.

[0041] The use of "comprising", "including" or "having" are synonymous and variations thereof herein are meant to be inclusive or open-ended and do not exclude additional unrecited elements or method steps.

Claims

What is claimed is:

1. A memory module comprising:
a data communication interface;
a volatile memory device;
a non-volatile memory device; and
a controller coupled to the data communication interface, the volatile memory device, and the non-volatile memory device, the controller to:
store data to the volatile memory device, wherein the data is received via the data communication interface from a host controller;
detect a state transition of a clock enable signal and a state transition of a reset signal via the data communication interface; and
determine whether to transfer the data from the volatile memory device to the non-volatile memory device based on a timing of the state transition of the reset signal relative to the state transition of the clock enable signal.
2. The memory module of claim 1, wherein the clock enable signal and the reset signal are asserted by the host controller.
3. The memory module of claim 1, wherein the controller is to:
transfer the data to the non-volatile memory device when the state transition of the reset signal is detected after the state transition of the clock enable signal; and

maintain the data in the volatile memory device when the state transition of the reset signal is detected prior to the state transition of the clock enable signal.

4. The memory module of claim 1, wherein the memory module is coupled to a power storage device.

5. The memory module of claim 1, wherein the memory module is a non-volatile dual in-line memory module (NVDIMM).

6. The memory module of claim 1, wherein the memory module and the host controller are located in the same electronic device.

7. A method comprising:

sensing, via a data communication interface of a memory module, a plurality of signals including a save signal, a clock enable signal, and a reset signal;

in response to detecting a state transition of the save signal, storing data received from a host controller to a volatile memory device of the memory module;

in response to detecting a state transition of the reset signal prior to an expiration of a waiting period associated with a state transition of the clock enable signal, maintaining the data in the volatile memory device; and

in response to detecting the state transition of the reset signal after the expiration of the waiting period, transferring the data from the volatile memory device to a non-volatile memory device of the memory module.

8. The method of claim 7, wherein the waiting period begins at the state transition of the clock enable signal.

9. The method of claim 7, wherein the waiting period expires after the state transition of the clock enable signal.

10. The method of claim 7, wherein the save signal is asserted by a power supply detection circuit.

11. The method of claim 7, wherein the clock enable signal and the reset signal are asserted by the host controller.

12. A non-transitory computer-readable storage medium comprising instructions that when executed cause a controller of a memory module to:

- detect, via a data communication interface of the memory module, a state transition of a clock enable signal;
- detect a state transition of a reset signal;
- compare a timing of the state transition of the reset enable signal to a waiting period that begins at the state transition of the clock enable signal; and
- determine whether to transfer data from a volatile memory device of the memory module to a non-volatile memory device of the memory module based on the comparison.

13. The non-transitory computer-readable storage medium of claim 12, wherein the instructions when executed cause the controller to:

- transfer the to the non-volatile memory device when the state transition of the reset signal is detected after an expiration of the waiting period;
- and
- maintain the data in the volatile memory device when the state transition of the reset signal is detected prior to the expiration of the waiting period.

14. The non-transitory computer-readable storage medium of claim 12, wherein the clock enable signal and the reset signal are asserted by a host controller.

15. The non-transitory computer-readable storage medium of claim 12, wherein the state transition of the clock enable signal is indicative of a completion of a data flushing operation.

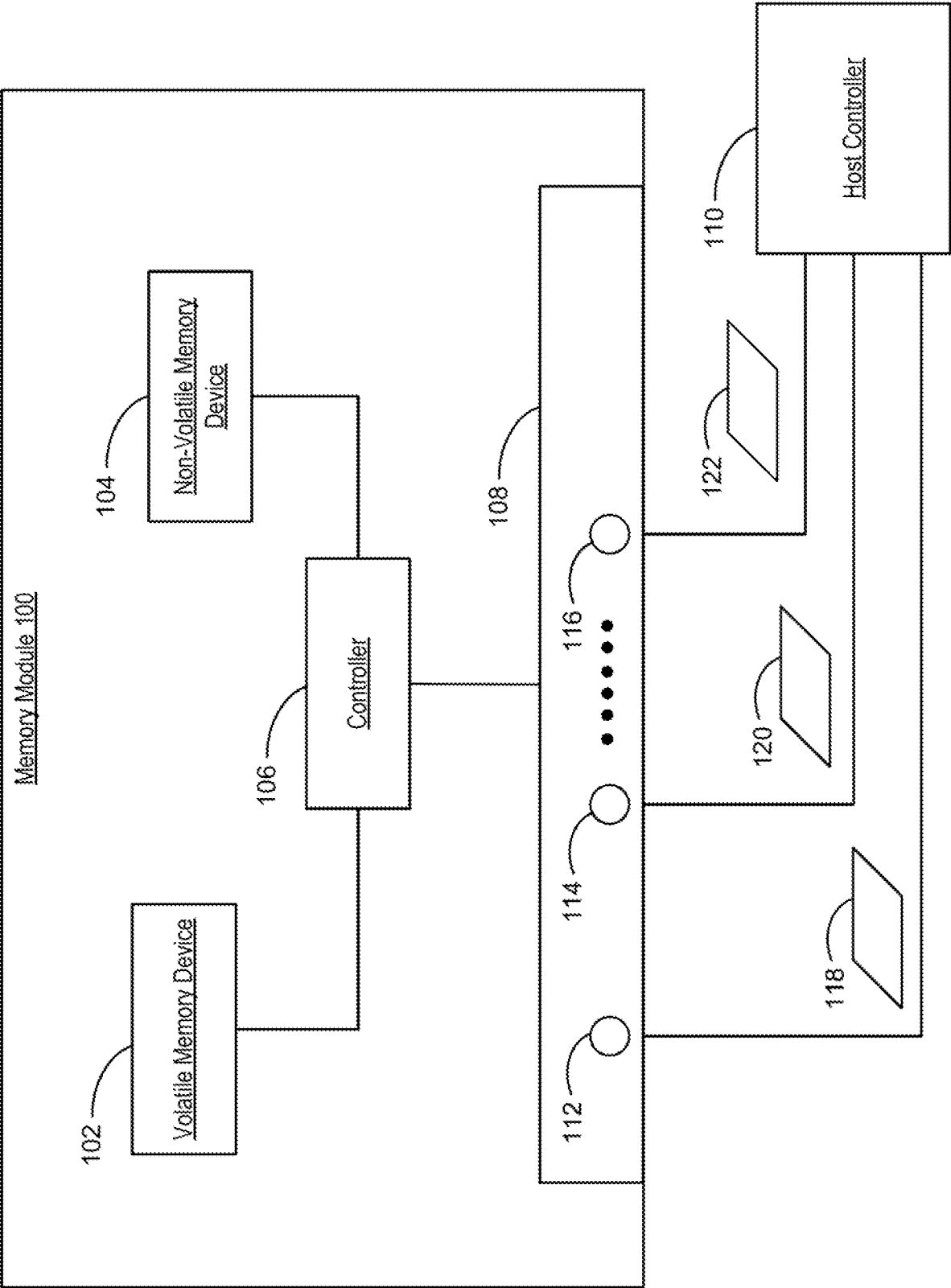


FIG. 1

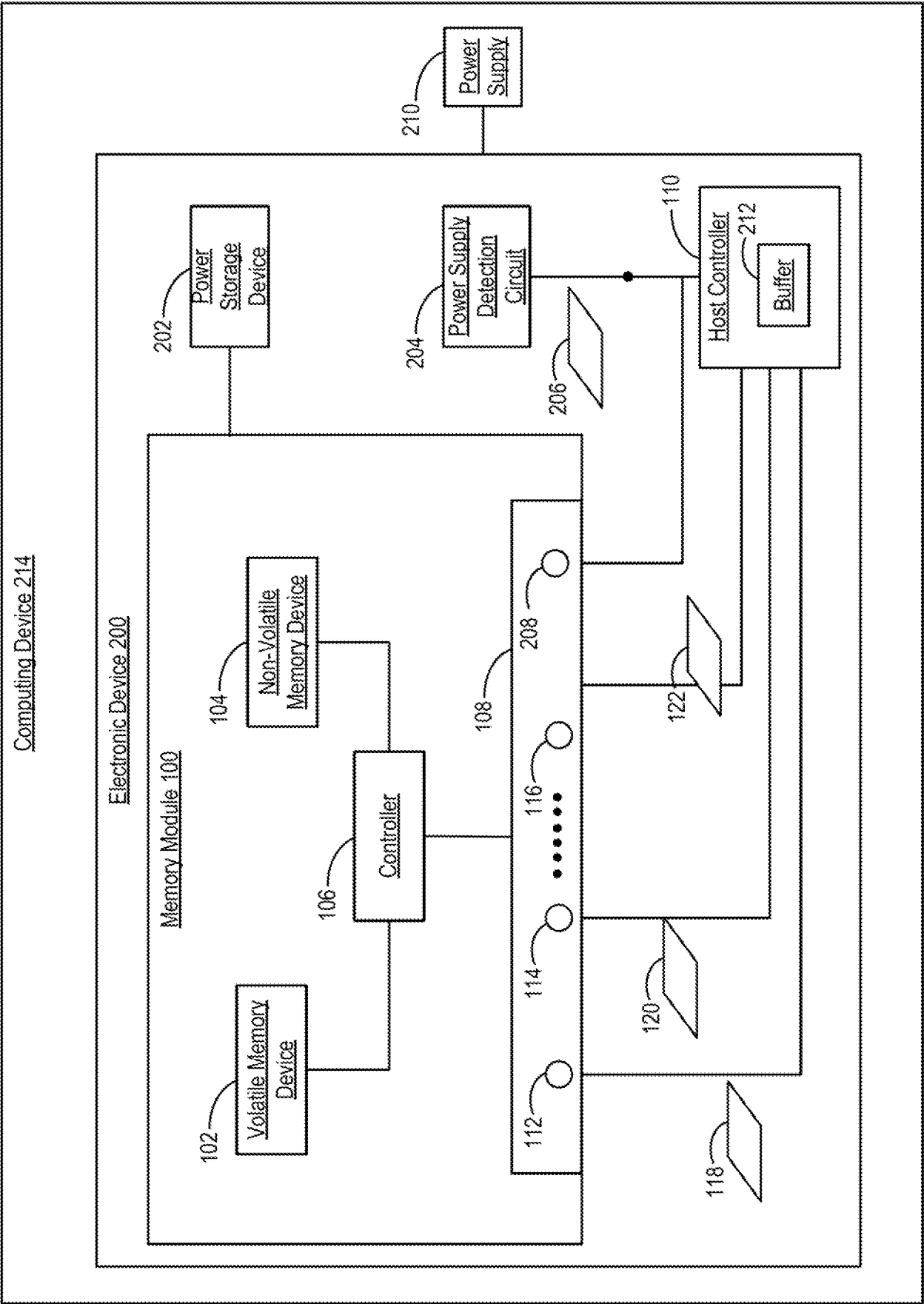


FIG. 2

300

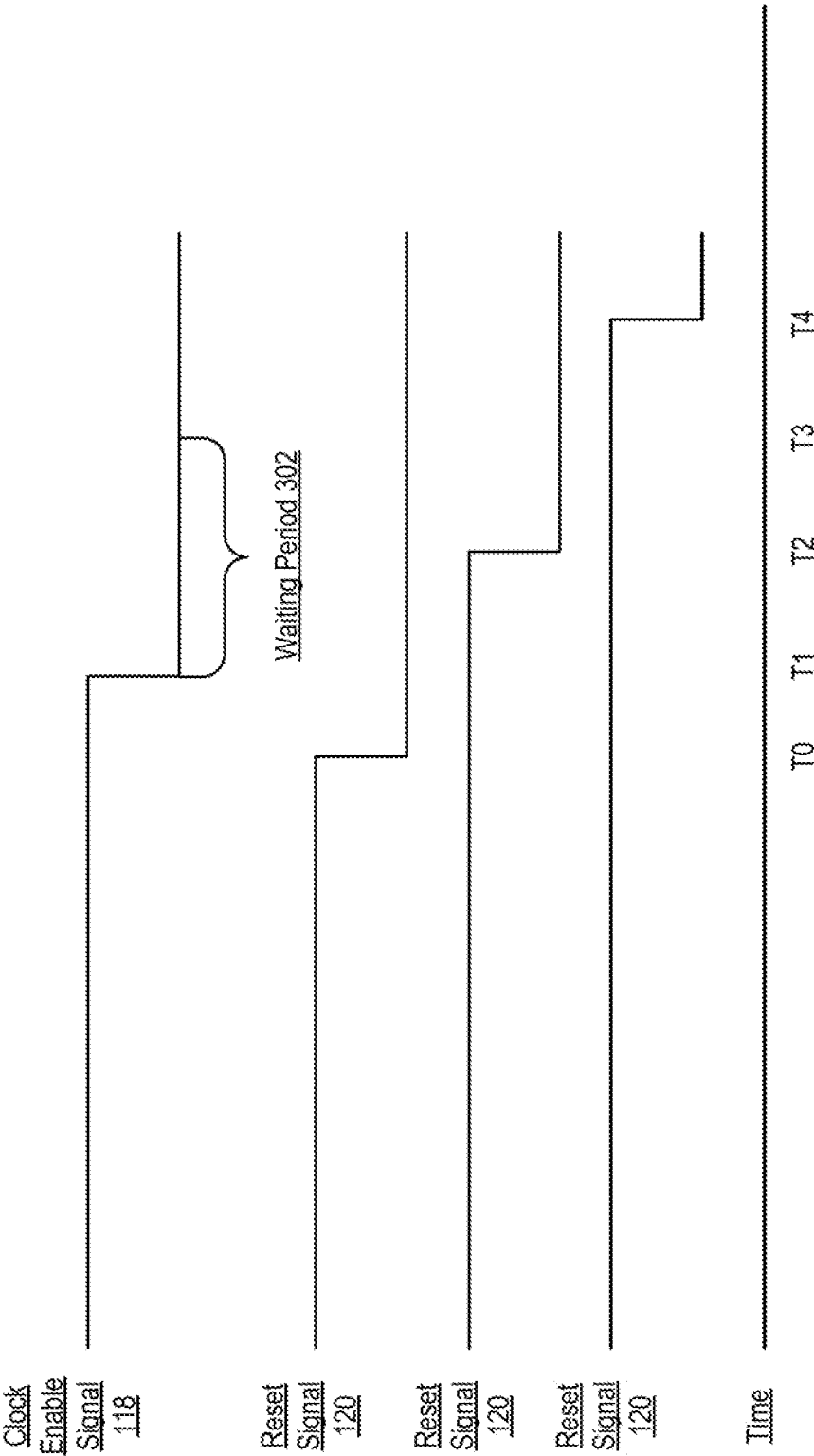


FIG. 3

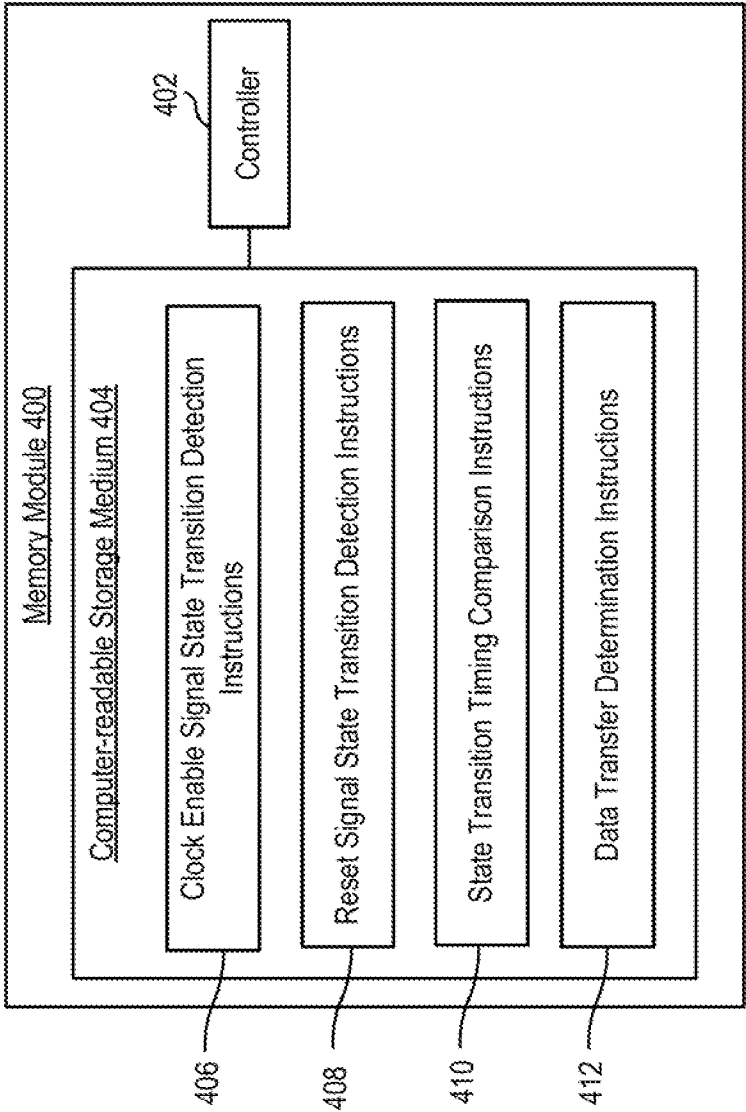


FIG. 4

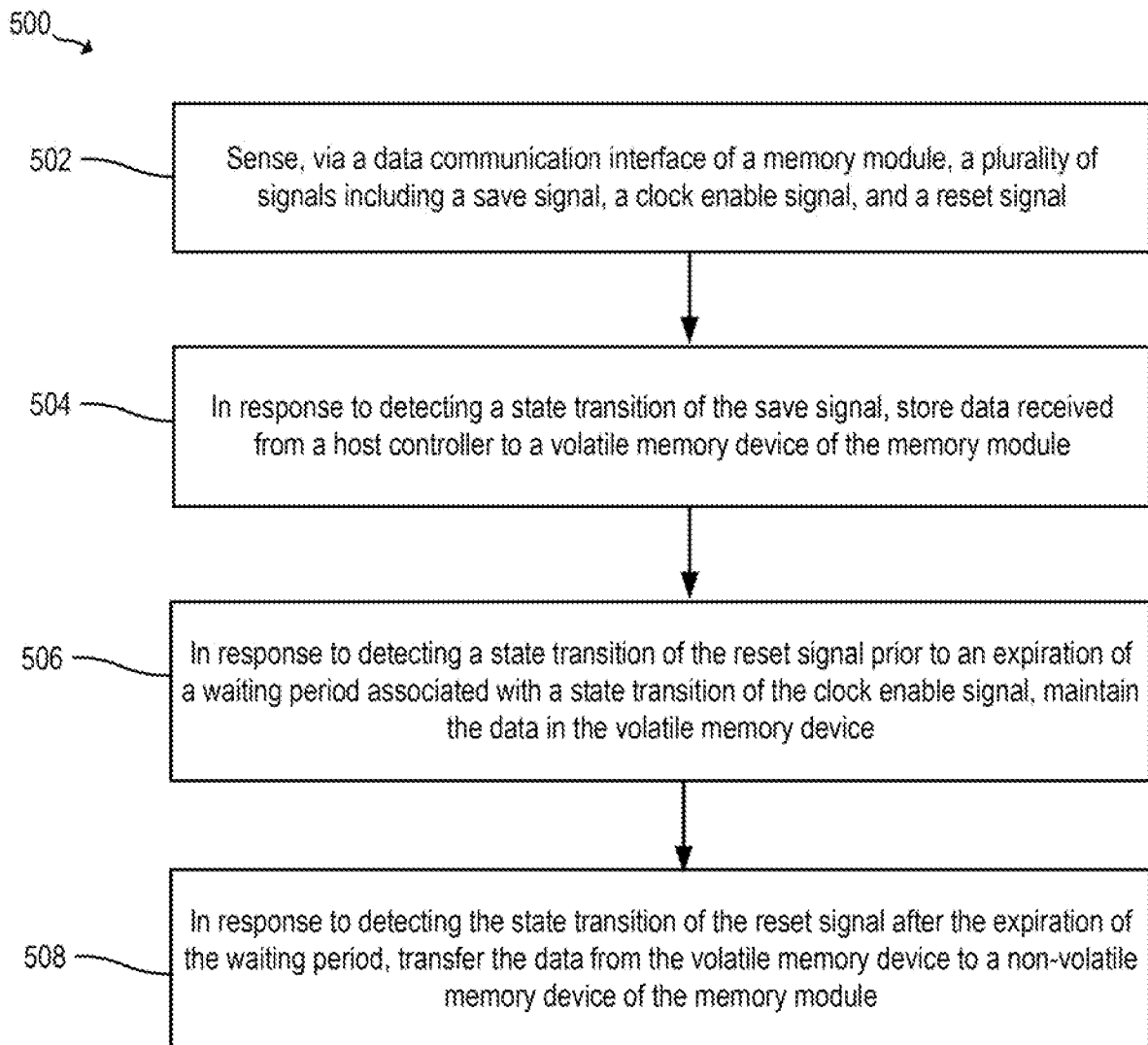


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/030873**A. CLASSIFICATION OF SUBJECT MATTER****G06F 3/06(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
G06F 3/06; G06F 12/02; G06F 12/06; G06F 11/30; G06F 13/14; G06F 9/00; G06F 11/00Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: state, transition, memory, module, volatile, non-volatile, data, transfer, detect, signal, period**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0271990 A1 (CHI-SHE CEHN et al.) 25 October 2012 See paragraphs [0007], [0026], [0028], [0030], [0043]; claims 1, 19; and figure 1.	1-15
Y	US 2005-0268157 A1 (FABRIZIO CAMPANALE) 01 December 2005 See paragraphs [0025]-[0027], [0117]-[0118]; claims 3-5; and figure 5b.	1-15
A	US 2012-0203962 A1 (AKIHITO MOCHIZUKI) 09 August 2012 See paragraphs [0023], [0027]; and figures 1-2.	1-15
A	US 2005-0216723 A1 (KENICHI IMAMIYA) 29 September 2005 See paragraphs [0025]-[0026], [0034]; and figure 1.	1-15
A	WO 2015-041698 A1 (INTEL CORPORATION) 26 March 2015 See paragraphs [0026]-[0027]; and figure 1.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

21 April 2016 (21.04.2016)

Date of mailing of the international search report

21 April 2016 (21.04.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

BYUN, Sung Cheal

Telephone No. +82-42-481-8262



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/030873

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