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(54) **Title**: MULTI-STAGE AMPLIFIER WITH CASCODE STAGE AND DC BIAS REGULATOR

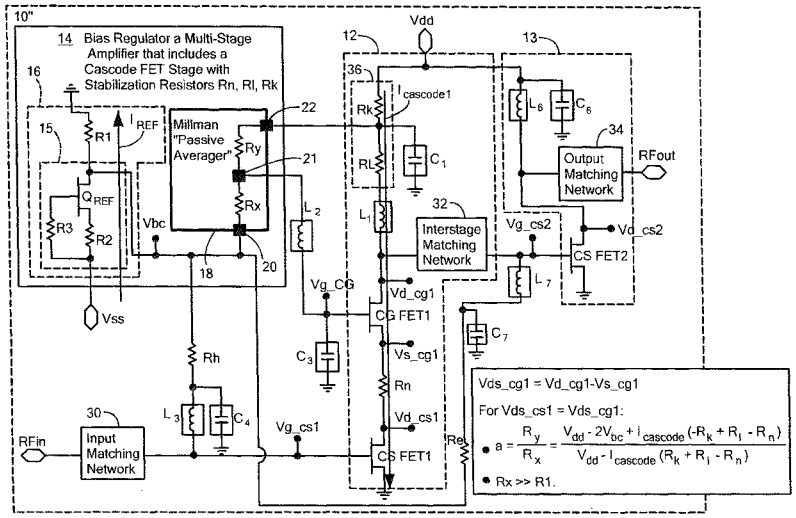

FIG. 6

(57) **Abstract**: A multi-stage amplifier (10") having a first amplifier stage (12) comprising: a pair of transistors arranged in a cascode amplifier arrangement; and an isolation circuit; and a second amplifier stage (13) coupled to an output of the first amplifier stage (12); and bias regulator (14) having a reference transistor. The cascode amplifier stage includes a pair of transistors arranged in a cascode amplifier arrangement. The bias regulator (14) produces a reference current through the reference transistor and DC bias voltages for the control electrodes of each of the pair of transistors in the cascode amplifier arrangement and for the second stage's transistor as a function of the reference current through the reference transistor.

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Multi-stage Amplifier with Cascode Stage and DC Bias Regulator

TECHNICAL FIELD

This disclosure relates generally to cascode amplifiers and more particularly to multi-stage amplifiers having a cascode stage and a DC bias regulator.

BACKGROUND

As is known in the art, a cascode amplifier may be formed with either Field Effect Transistors (FETs) or Bipolar Junction Transistors (BJTs). In the case of a FET a gate is used as a control electrode for controlling a flow of carriers between a source electrode and a drain electrode and in the case of a BJT a base electrode is used as a control electrode to control a flow of carriers between a collector electrode and a drain electrode. Thus, it should be noted that while a FET cascode amplifier is described, the material can be equivalently applied to a BJT. Thus, the gate electrode of a FET is equivalent to a base electrode of a BJT; either being referred to herein as a control electrode for the transistor. In like manner the terms drain and source may be interchanged for a FET as well as the terms emitter and collector for a BJT.

Thus, considering a Field Effect Transistor (FET) cascode amplifier, such FET cascode amplifier includes a common source (CS) connected FET serially connected to a common gate (CG) connected FET with the drain of the CS FET being coupled to the source of the CG FET; the drain of the common gate (CG) FET being coupled to a Vdd voltage supply. In a typical cascode arrangement, the sizes of the CS and CG FETs are equal (i.e. the total gate widths for the two transistors are the same Wg_cs=Wg_cg).

In general, DC biasing circuit or regulators, in order to operate effectively, must provide DC bias regulation (i.e. produce gate DC bias voltages for the CS and CG FETs or base DC bias voltages for BJTs) in such a way that the cascode amplifier performance (measured by DC drain/collector current, RF gain, noise figure, output power, linearity) is insensitive to variation in manufacturing process, temperature and external DC bias voltage. The first two variations typically manifest themselves as variations in transistor pinch off, Vp, or threshold voltage.

An additional requirement, specific to a cascode amplifier, is a controlled division of Vdd (or Vcc for a bipolar cascade amplifier) between the drain to source voltage (V_{ds}) of the common gate FET (Vds_cg) drain-source junction and the drain to source voltage of

the common source FET (Vds_cs) drain-source junction in order to ensure that both FETs are always in the saturation regime (Vds > Vknee), (where Vknee is the voltage at the knee of the saturation curve) so that the drain to source current (Ids) is nearly independent of Vds for both transistors in the cascode). For example, if Vdd=2V and Vknee=0.5V, one would like to avoid situations when Vds_cg = 0.4V and Vds_cs= 1.6V or Vds_cg = 1.6V and Vds_cs= 0.4V. Also, as is known in the art, the equal division results in the maximum output power and linearity of a cascode amplifier. Thus, a DC bias regulator for a cascode amplifier should be capable of enforcing a condition wherein the drain-source voltages for the common-source and common-gate (common-emitter and common-base) transistors are equal by design and remain equal in presence of variation in manufacturing process, temperature and external DC bias voltage.

One DC bias regulator for a cascode transistor amplifier is described in U. S. Patent No. 5,032,799 inventor Milberger, et al., entitled "Multistage cascode radio frequency amplifier" issued July 16, 1991. However, such DC bias regulator is a passive DC bias regulator circuit and therefore does not provide compensation for variations in manufacturing process, temperature and external DC bias voltage. Two active DC bias regulators are described in U. S. Patent No. 5,506,544, inventor Staudinger et al., entitled "Bias Circuit for Depletion Mode Field Effect Transistors", issued April 9, 1996 and in U. S. Patent No. 7,961,049, Busking et al., entitled "Amplifier with compensated gate bias", issued June 14, 2011; while these two DC bias regulators do compensate for process condition variations, they are specific for a common source FET and are used to maintain constant drain current through that single FET and not applicable for a cascode amplifier having a pair of FETs.

As is also known in the art, it is sometimes required that resistors used in an integrated circuit have a precise predetermined relationship in the value of their resistances for the circuit to operate properly. It is also known in the art that it is easier to fabricate resistor of equal resistance as compared fabricating resistors requiring a predetermined difference in resistance for proper operation of a circuit.

As is also known in the art, one circuit shown in FIG. 1, used to combine a pair of input voltages in a so-called Millman "Passive Averager", is described in an article entitled "A Useful Network Theorem" by Jacob Millman, published in the Proceedings of the IRE, September 1940, pages 413-471. As described therein, in a specific case an output voltage Vout is produced from a pair of input voltages Vx and Vy:

$$V_{out} = \frac{\frac{V_x}{R_x} + \frac{V_y}{R_y}}{\frac{1}{R_x} + \frac{1}{R_y}} = \frac{V_x R_y + V_y R_x}{R_x + R_y}$$

and in the specific case where $R_x = R_y$;

$$V_{out} = \frac{V_x + V_y}{2}$$

As is also known in the art, multi-stage amplifier may include a cascode amplifier as one of the stage therein. Thus, proper isolation between stages is required as well as proper DC biasing of the cascode stage. Thus, here again, a DC bias regulator for a cascode amplifier should be capable of enforcing a condition wherein the drain-source voltages for the common-source and common-gate (common-emitter and common-base) transistors are equal by design and remain equal in presence of variation in manufacturing process, temperature and external DC bias voltage.

SUMMARY

In accordance with the present disclosure, a multi-stage amplifier is provided having a first amplifier stage comprising: a pair of transistors arranged in a cascode amplifier arrangement; and an isolation circuit; and a second amplifier stage coupled to an output of the first amplifier stage. The cascode amplifier arrangement includes a pair of transistors arranged in a cascode amplifier arrangement and bias regulator having a reference transistor. The DC bias regulator produces a reference current through the reference transistor and DC bias voltages for the control electrodes of each of the pair of transistors in the cascode arrangement as a function of the reference current through the reference transistor.

The inventor has recognized that while U.S. Patent No. 5,506,544 and U. S. patent No. 7,961,049 describe DC bias circuits for the gate electrode of a single common-source FET amplifier, the Applicant has devised a circuit that generates two DC bias voltages for

gate electrodes of a cascode amplifier and a common-source amplifier (one for the gate electrode of a cascode amplifier's common-source FET and the second stage's common-source FET, and the other for the gate electrode of a cascode amplifier's common-gate FET) in a such a way that:

a) The DC current flowing through the drain-source junctions of the two transistors is insensitive to variations in the transistors' pinch-off voltage whereby both voltages (one for the gate electrode of a cascode amplifier's common-source FET and the other for the gate electrode of a cascode amplifier's common-gate FET) track the pinch-off voltage;

b) The requisite controlled division of an external DC bias voltage between the drain-source junctions of the two cascode amplifier's transistors is enforced at the nominal condition as well as in the presence of variations in the transistors' pinch-off voltage and/or variations in the external voltage source Vdd.

With such an arrangement, active, process and temperature invariant, DC bias is provided for both transistor in the cascode arrangement. More particularly, the bias regulator reduces multi-stage amplifier performance sensitivity to variations in the manufacturing process, temperature and external DC power sources; and enforces predetermined division of DC bias voltage between drain-source junctions of the cascode stage's common-gate and common-source transistors at a nominal operating condition as well as in the presence of variations in the operating conditions.

In one embodiment, an amplifier is provided having: a first amplifier stage, comprising: a pair of transistors arranged in a cascode amplifier arrangement; and an isolation circuit; and a second amplifier stage coupled to an output of the first amplifier stage. A voltage source is coupled to the first amplifier stage and the second amplifier stage, the isolation circuit being coupled between the a pair of transistors arranged in a cascode amplifier arrangement, the voltage source producing a current serially through the isolation circuit and the pair of transistor in the cascode amplifier arrangement. A DC bias regulator is provided having: a DC bias circuit for producing: a voltage related to a reference current produced by the DC bias circuit, such voltage being coupled to a control electrode of a first one of the pair of transistors; and a combiner having a pair of inputs coupled to: the voltage produced by the DC bias circuit and a voltage produced by the isolation circuit, respectively, to produce a DC bias voltage at a control electrode of a

second one of the pair of transistors related to a combination of the voltage produced by the DC bias circuit and the voltage produced by the combiner.

In one embodiment, a resistor is connected between the pair of pair of transistor in the cascode amplifier arrangement.

In one embodiment, the DC bias regulator comprises: a reference transistor. The DC bias regulator produces the reference current through the reference transistor. The DC bias regulator produces the DC bias voltages for each of the pair of transistors in the cascode amplifier arrangement as a function of the reference current produced through the reference transistor.

In one embodiment, the isolation circuit comprises a pair of serially connected resistors, the resistors being connected to a common junction, wherein the combiner includes a pair or resistors each one connected to a corresponding one of the pair of inputs of the combiner and to a combiner output, the combiner output being coupled to the control of the second one of the pair of transistors, one of the pair of inputs being connected to the junction.

In one embodiment, the combiner circuit produces the DC bias voltage as a function of the sum of the output voltage produced by the reference voltage and the isolation circuit.

In one embodiment, the combiner circuit produces the DC bias voltage as a function of the average of the output voltage produced by the reference voltage and the voltage produced by the isolation circuit.

In one embodiment, the current through the reference transistor is a saturation current for the reference transistor and current from the voltage supply to the pair of transistors in the cascode amplifier arrangement is a saturation current for both the pair of transistors in the cascode amplifier arrangement.

In one embodiment, the control electrode of a first one of the pair of transistors controls a flow of carriers between a first and second electrode of the first one of the pair of transistors in the cascode amplifier arrangement, and the control electrode of the second one of the pair of transistors in the cascode amplifier arrangement controls a flow of carriers between a first and second electrode of the second one of the pair of transistors in the cascode amplifier arrangement; and wherein the DC bias voltages produced at the control electrodes of the first one of the pair transistors in the cascode amplifier arrangement and the second one of the pair of transistor in the cascode amplifier

arrangement produces a voltage across the first and second electrodes of the first one of the pair of transistors in the cascode amplifier arrangement equal to the voltage across the first and second electrodes of the second one of the pair of transistors in the cascode amplifier arrangement.

In one embodiment, the resistances of the pair of resistors in the combiner are a function of the resistances of the pair of resistors in the isolation circuit and the resistance of the resistor between the pair of transistors in the cascode amplifier arrangement.

In one embodiment, the combiner is a Millman passive combiner.

In one embodiment, the second amplifier stage includes a second stage transistor having a control electrode for controlling a flow of carriers between a first electrode and a second electrode and wherein the control electrode of the second stage transistor is coupled to the output of the first amplifier stage and wherein the first electrode of the second stage transistor is connected to the voltage source and the second electrode is connected to a reference potential.

The details of one or more embodiments of the disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the disclosure will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic diagram of a Millman "Passive Averager" with two inputs according to the PRIOR ART;

FIG. 2 is a schematic diagram of a common-source FET amplifier with bias regulator according to the PRIOR ART;

FIG. 3 is a schematic diagram of a cascode amplifier according to the disclosure;

FIG. 4A and 4B are computer simulation results of the cascode amplifier of FIG. 3 using circuit models of GaAs FETs to represent transistors; FIG. 3A showing percent change in DC drain current, $I_{CASCODE}$, as a function of change in pinch off voltage for: (A) an cascode amplifier without any DC bias regulator; (B) a cascode amplifier with regulator to control DC bias of the gate electrode of only the common source FET; (C) a cascode amplifier according to the disclosure; FIG. 4 B shows Vds_cg/Vds_cs ratio as a function of change in pinch off voltage for : (A) an cascode amplifier without any DC bias

regulator; (B) a cascode amplifier with regulator to control DC bias of the gate electrode of only the common source FET; and (C) a cascode amplifier according to the disclosure;

FIG. 5 is a schematic diagram of a cascode amplifier having a stabilization resistor coupled between the pair of cascode arranged transistors according to the disclosure;

FIG. 6 is a schematic diagram of a two-stage cascaded amplifier having a first cascode amplifier stage feeding a second common-source amplifier stage according to the disclosure.

Fig.7A is a schematic of a Millman "Passive Averager" with two inputs and with variable resistors Rx and Ry.

Fig.7B is a schematic of a Millman "Passive Averager" with two inputs and with voltage-variable resistors implemented as transistors Qx and Qy.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Referring now to FIG. 3, an amplifier 10 is shown having: a pair of transistors, here FETs, CS FET and CG FET of equal total gate widths, Wg_cs=Wg_cg, arranged as a cascode amplifier 12, as shown, and a DC bias regulator 14. The pair of transistors CS FET and CG FET, of the cascode amplifier 10 is serially connected between a first voltage source, Vdd and ground potential, as shown. An input RF signal is fed to the gate of CS FET, as shown, for amplification by the amplifier 10 to produce an output RF signal at the drain of CG_FET, as indicated.

In order for the voltage Vds_cs between the source (S) and drain (D) electrodes of the CG FET to be equal to the voltage Vds_cg between the source (S) and drain (D) electrodes of the CS FET, Vd_cs needs to be equal to Vdd/2 (assuming that Vdd = Vd_cg, i.e., the RF choke L1 separating Vdd and Vd_cg has zero DC resistance). Note that in this commonly used notation, (A) Vds_cs = Vd_cs – Vs_cs = Vd_cs since Vs_cs =0 and (B) Vds_cg = Vd_cg – Vs_cg= Vdd-Vd_cs.

In order for Vds_cs to be equal to Vds_cg, Vgs_cg needs to be equal to Vgs_cs because they share the same current $I_{CASCODE}$ and their sizes are equal Wg_cs=Wg_cg. It is noted that both the CG FET and the CS FET operate with a saturation current $I_{CASCODE}$ and the cascode arrangement is a current-sharing arrangement. Therefore, Vgs_cg = Vg_cg – Vs_cg = Vg_cg – Vd_cs = Vg_cg – Vdd/2; or Vg_cg = Vdd/2 + Vgs_cg. Since

we want Vgs_cg to be equal to Vgs_cs, we want Vg_cg = Vdd/2 +Vgs_cs. Thus, Vg_cg must equal [Vdd+2Vgs_cs]/2 in order for Vds_cs = Vds_cg.

It should be noted that Qref, CS FET and CG FET are all formed in near proximity on the same integrated circuit, so that both the semiconductor material properties and environmental conditions are the same for the three transistors. Thus, the reference transistor Q_{REF}, produces a reference current I_{REF}, here for example, the saturation current, through the source electrode S and drain electrode D of the reference transistor Q_{REF}, and through the serially connected resistors R1a and R1b. The DC bias regulator 14 produces bias voltages Vg_cs and Vg_cg for the gate electrodes of the CS FET and CG FET, respectively, as a function of the reference current I_{REF} through the reference transistor Q_{REF} and the serially connected resistors R1a and R1b.

More particularly, the DC bias regulator 14 includes a bias circuit 16 and a voltage combiner circuit 18, here a Millman averaging circuit, FIG. 1. The bias circuit 16 includes a reference transistor Q_{REF}, connected as a current source 15, serially connected between a voltage Vss and ground through a voltage divider 17, having serially connected resistors R1a and R1b, as shown. The voltage divider 17 of the bias circuit 16 produces: a first output voltage V1b related to the reference current I_{REF} and the sum of resistors R1a and R2b (i.e., $V1b = I_{REF}(R1a+R1b)$ and a second voltage, $Vg\_cs = I_{REF} R1a/(R1a + R1b)$. Thus, Vg_cs is a predetermined fraction R1a/ (R1a+R1b) of the output voltage V1b, the second voltage Vg_cs being coupled to the control electrode, here the gate electrode G of a first one of the pair of transistors, here CS FET.

The combiner circuit 18 has a pair of inputs 20, 22 coupled to: the first output voltage Vg_cs produced by the voltage divider 17 and the first voltage source, Vdd, respectively, to produce a DC bias voltage Vg_cg at the control electrode, here the gate electrode G of the second transistor CG FET related to a combination of the first output voltage Vg_cs and the first voltage source Vdd. More particularly, here R1a= R1b so that Vg_cs = V1b/2 and therefore with Rx and Ry of the combiner 18 being equal and being much greater than R1a, so that the combiner circuit 18 produces the DC bias voltage Vg_cg as a function of the sum of the voltage V1b and the first voltage source Vdd; here [V1b + Vdd]/2. Since, V1b = 2Vg_cs, Vg_cg = [2Vg_cs + Vdd]/2 and therefore as described above, the voltage Vds_cg across the source and drain electrode S, D of the CG FET will be equal to the voltage Vds_cs across the source drain electrode S, D of the CS FET. It should be noted that in this arrangement, Vg_cg does not have direct dependence

on $I_{CASCODE}$, only through Vg_cs. It should also be noted that Vg_cg traces Vg_cs, i.e. if the pinch-off voltage for CS, CG and Qref FETs changes due to manufacturing and/or temperature, both Vg_cs and Vg_cg get adjusted automatically by the bias regulator arrangement to keep the $I_{CASCODE}$ constant and Vds_cs = Vds_cg.

Finally it is noted that because R1a= R1b (as noted above, fabrication of resistors or equal resistances is very precise), the voltage divider 17 produces a voltage Vg_cs which is precisely one half of the output voltage fed to input 20 of the combiner 18 (that is, from the equations described above, Vdd will split between Vds_cs and Vds_cg independent of the actual voltage Vdd). Therefore, the voltage Vds_cg across the source and drain electrodes S, D of the CG FET will be equal to the voltage Vds_cs across the source drain electrodes S, D of the CS FET independent of the actual voltage of Vdd resulting in a circuit independent of variations in Vdd and is, as described in below, independent of variations in pinch off voltage, Vp.

Referring to FIG. 3, according to the Millman Theorem described above:

$$V_{g\_cg} = \frac{\frac{V_{dd}}{R_y} + \frac{V_{1b}}{R_x}}{\frac{1}{R_y} + \frac{1}{R_x}} \quad (1)$$

If we select $R_y = R_x$ and assume that L2 has zero DC resistance, then:

$$V_{g\_cg} = \frac{V_{dd} + V_{1b}}{2} \quad (2)$$

We need to ensure that (it is assumed that L1 has zero DC resistance):

$$V_{ds\_cg} = V_{ds\_cs} \Leftrightarrow V_{d\_cs} = \frac{V_{dd}}{2} \quad (3)$$

For this to be true, the following must be enforced (assuming that L3 has zero DC resistance, the voltage drop across Rh is negligible, and CS FET and CG FET have the ame total gate width Wg_cs=Wg_cg)

$$V_{gs\_cg} = V_{gs\_cs} \Leftrightarrow V_{g\_cg} - V_{s\_cg} = V_{gs\_cs} \Leftrightarrow V_{g\_cg} = \frac{V_{dd}}{2} + V_{gs\_cs} \quad (4)$$

$$V_{g\_cg} = \frac{V_{dd} + 2V_{g\_cs}}{2} \quad (5)$$

If R1a=R1b (assuming that Rx >> R1a), the equal voltage division Vds_cg=Vds_cs in (3) is enforced from (2) and (5) by ensuring that V1b=2Vg_cs.

Thus, in summary, and referring to FIG. 3:

For the voltage across the source-drain of the CS FET (Vds_cs) to be equal to the voltage across the source-drain of the CG FET (Vds_cg):

- Vg_cg should be equal to (Vdd+2Vg_cs) / 2;
- R1a = R1b so that the voltage V1b at the first input 20 of the Millman "Passive Averager" 18 is equal to 2Vg_cs;
- Rx = Ry >> R1a so that:
  - the voltage Vg_cg at the output 21 of the Millman "Passive Averager" is equal to the average of the voltages at the Millman "Passive Averager" inputs 20 and 22 thus satisfying the condition of Vg_cg = (Vdd+2Vg_cs) / 2 to enforce Vds_cs=Vds_cg;
  - the current through resistor Rx of the Millman "Passive Averager" is much smaller than the reference current Iref through the reference transistor Qref .

To complete the circuit 10, the RF input signal is fed to the gate electrode G of the CS FET through a conventional DC blocking capacitor C5, drain of the CG FET is coupled to the RF output through a DC blocking capacitor C2.C1, C3 and C4 DC are bypass capacitors that along with RF blocking inductors L1-L3 allow for DC connection between the bias regulator and Vdd on one side and transistors CS_FET and CG_FET on the other while preventing an RF connection. Resistor Rh provides additional low-frequency (where L3 and C4 are no longer effective in blocking the AC signal) isolation between the bias regulator and the gate electrode G of the CS FET.

Referring now to FIGS. 4A and 4B, FIGS. 4A and 4B show computer simulation results of the cascode amplifier of FIG. 3; FIG. 4A showing percent change in DC drain current, $I_{CASCODE}$, as a function of change in pinch off voltage for: (A) an cascode

amplifier without any DC bias regulator; (B) a cascode amplifier with regulator to control DC bias of the gate electrode of only the common-source FET; (C) a cascode amplifier according to the disclosure and FIG. 3B shows Vds_cg/Vds_cs ratio as a function of change in pinch off voltage for (A) an cascode amplifier without any DC bias regulator; (B) a cascode amplifier with regulator to control DC bias of the gate electrode of only the common-source FET; (C) a cascode amplifier according to the disclosure. The curves demonstrate that the Cascode DC Bias Regulator demonstrates the required functionality:

1. reduced sensitivity to pinch-off voltage, Vp, variation;
2. enforced equality of drain-source voltages across the FET CS and FET CG

Referring now to FIG. 5, a cascode amplifier 10' is shown. Here, a stabilization resistor Rn is connected between the source of the CG FET and the drain of the CS FET, as shown. The function of the resistor Rn is to improve circuit's stability at the expense of lowering its gain> Because of the inclusion of the resistor Rn, the resistance values for resistors Rx and Ry now need to satisfy the following ratio a to ensure Vds_cs=Vds_cg:

Referring to FIG. 5, according to the Millman Theorem (assuming that L2 has zero DC resistance):

$$V_{g\_cg} = \frac{\frac{V_{dd}}{R_y} + \frac{V_{bc}}{R_x}}{\frac{1}{R_y} + \frac{1}{R_x}} \tag{6}$$

If $R_y = aR_x$ and Rx >> R1, then:

$$V_{g\_cg} = \frac{V_{dd} + aV_{bc}}{a+1} \tag{7}$$

We need to ensure that:

$$V_{ds\_cg} = V_{ds\_cs} \Leftrightarrow V_{d\_cg} - V_{s\_cg} = V_{d\_cs} \tag{8}$$

For this to be true, the following must be enforced (assuming that Vg_cs1=Vbc, in other words, L3 has zero DC resistance and the voltage drop across Rh is negligible, and also making CS FET and CG FET have the same total gate width Wg_cs=Wg_cg)

$$V_{gs\_cg} = V_{gs\_cs} \Leftrightarrow V_{gs\_cg} = V_{bc} \Leftrightarrow V_{g\_cg} = V_{s\_cg} + V_{bc} \tag{9}$$

Now, we need to express V_{s_cg} in terms of R_k, R_l, R_n, V_{dd} and $I_{cascode}$ (assuming L1 has zero DC resistance)

$$V_{d\_cg} = V_{dd} \tag{10}$$

$$V_{ds\_cg} + V_{d\_cs} = V_{dd} - I_{cascode}R_n \tag{11}$$

Since $V_{ds\_cg}=V_{d\_cs}$

$$V_{d\_cs} = \frac{V_{dd}-I_{cascode}R_n}{2} \tag{12}$$

$$V_{s\_cg} = V_{d\_cs} + I_{cascode}R_n = \frac{V_{dd}+I_{cascode}R_n}{2} \tag{13}$$

From (9) and (13)

$$V_{g\_cg} = V_{s\_cg} + V_{bc} = \frac{V_{dd}+I_{cascode}R_n}{2} + V_{bc} \tag{14}$$

Combining (7) and (14)

$$\frac{V_{dd}+aV_{bc}}{a+1} = \frac{V_{dd}+I_{cascode}R_n}{2} + V_{bc} \tag{15}$$

Using (15), the ratio a=Ry/Rx, which enforces Vds_cs = Vds_cg, can be derived as:

$$a = \frac{R_y}{R_x} = \frac{V_{dd}-2V_{bc}-I_{cascode}R_n}{V_{dd}+I_{cascode}R_n} \tag{16}$$

Referring now to FIG. 6, a two-stage cascade amplifier 10" having a first cascode amplifier stage 12' feeding a second common-source amplifier stage 13' is shown. Further, it is noted that here, because of the cascade of the two amplifiers 14' and 13', input, interstage, and output matching networks 30, 32, and 34, respectively, are included as shown. Here, in order to improve stability of the amplifier 10', the cascode amplifier 12' also includes the resistor Rn connected serially between the source of CG FET1 and the drain of CS FET2, as shown. Also included is an isolation circuit 36, here resistors Rk and RL, serially connected between Vdd and the drain of CG FET1, as shown to improve low frequency (i.e., frequencies much lower than the frequency of the RF input signal) isolation between the cascode amplifier stage 12' and the common-source amplifier stage

13'; the impedance matching between the cascode amplifier stage 12 and the common-source amplifier stage 13' being provided by the interstage matching network 32. It is noted that also included are by-pass capacitors C1, C3, C4, C6 and C7 and RF chokes L2, L6 and L7, arranged as shown.

It is also noted that the bias circuit 16' includes only one resistor R1 serially connected to the current source 15. Here, the current source produces a reference current I_{REF}, as indicated. The reference current I_{REF} passes through R1 to produce an output voltage Vbc from the DC bias circuit 16', as indicated. The output voltage Vbc is fed to:

(A) the gate of CS FET1 to provide a DC bias voltage Vg_cs1 through RF choke L3 and resistor Rh, here used to enhance low frequency isolation between the bias regulator 14 and the transistor CS FET1;

(B) the gate of CS FET2 of the common-source stage 13' to provide a DC bias voltage Vg_cs2 through low-frequency isolating resistor Re and RF choke L7; and,

(C) the input 20 of the voltage combiner circuit 18, as shown.

The second input 22 of the combiner is fed a voltage at the junction between resistors Rk and RL, as shown. Thus, the voltage at input 22 is a fraction of the voltage Vdd, as to be described.

The values Rx and Ry for the resistors in the combiner 18 are calculated based on chosen Rk, RL, and Rn values to enforce equal drain-source voltage division for the CS and CG FETs within the cascode amplifier 12'; more particularly that Vds_cs of CS FET1 ($V_{ds\_CS\ FET1}$) be equal to Vds_cg of CG FET1 $V_{ds\_CG\ FET1}$). More particularly, to ensure that $V_{ds\_CS\ FET1} = V_{ds\_CG\ FET1}$, the relation (27), shown and derived below, must be satisfied:

Referring to FIG. 6, according to the Millman Theorem (assuming that L2 has zero DC resistance)

$$V_{g\_cg} = \frac{\frac{V_{dd} - I_{cascode1} R_k}{R_y} + \frac{V_{bc}}{R_x}}{\frac{1}{R_y} + \frac{1}{R_x}} \tag{17}$$

If $R_y = aR_x$ and Rx >> R1, then:

$$V_{g\_cg} = \frac{V_{dd} - I_{cascode1}R_k + aV_{bc}}{a+1} \tag{18}$$

We need to ensure that:

$$V_{ds\_cg1} = V_{ds\_cs1} \Leftrightarrow V_{d\_cg1} - V_{s\_cg1} = V_{d\_cs1} \tag{19}$$

For this to be true, the following must be enforced (assuming that Vg_cs1=Vbc, in other words, L3 has zero DC resistance and the voltage drop across Rh is negligible, and also making CS FET and CG FET have the same total gate width Wg_cs=Wg_cg)

$$V_{gs\_cg} = V_{gs\_cs} \Leftrightarrow V_{gs\_cg} = V_{bc} \Leftrightarrow V_{g\_cg} = V_{s\_cg1} + V_{bc} \tag{20}$$

Now, we need to express V_{g_cg1} in terms of R_k, R_l, R_n, V_{dd} and $I_{cascode}$.

Assuming L1 has zero DC resistance

$$V_{ds_{cg1}} + V_{d_{cs1}} = V_{d_{cg1}} - I_{cascode1}R_n \tag{21}$$

$$V_{d\_cg1} = V_{dd} - I_{cascode1}(R_k + R_l) \tag{22}$$

Since $V_{ds\_cg1}=V_{d\_cs1}$

$$V_{d\_cs1} = \frac{V_{d\_cg1} - I_{cascode1}R_n}{2} = \frac{V_{dd} - I_{cascode1}(R_k + R_l + R_n)}{2} \tag{23}$$

$$V_{s\_cg1} = V_{d\_cs1} + I_{cascode1}R_n = \frac{V_{dd} - I_{cascode1}(R_k + R_l - R_n)}{2} \tag{24}$$

From (20) and (24)

$$V_{g\_cg} = V_{s\_cg1} + V_{bc} = \frac{V_{dd} - I_{cascode1}(R_k + R_l - R_n)}{2} + V_{bc} \tag{25}$$

Combining (18) and (25)

$$\frac{V_{dd} - I_{cascode1}R_k + aV_{bc}}{a+1} = \frac{V_{dd} - I_{cascode1}(R_k + R_l - R_n)}{2} + V_{bc} \tag{26}$$

Using (26), the ratio a=Ry/Rx, which enforces Vds_cs1 = Vds_cg1, can be derived as:

$$a = \frac{R_y}{R_x} = \frac{V_{dd} - 2V_{bc} + I_{cascode1}(-R_k + R_l - R_n)}{V_{dd} - I_{cascode1}(R_k + R_l - R_n)} \tag{27}$$

Alternatively, Ry and Rx can be set to obtain an arbitrary relationship between V_{ds_CS1} and V_{ds_CG1}.

Rk and RL are typically set to small resistance values to have small associated voltage drops across them. At the same time their non-zero resistances help to reduce quality factors of potential resonances associated with electrical interconnections and the reactive circuit components L1, L6, C1 and C6. In turn, lower resonances' quality factors improve circuit's stability.

A number of embodiments of the disclosure have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the disclosure. For example, as noted above, the transistors may be BJTs. Further, the resistors Rx and Ry and R1a and R1b may be selected to produce a ratio of Vds_cs to Vds_cg other than 1. Note, that if R1a and R1b are kept constant, changing Rx and Ry can produce different Vds_cs/Vds_cg ratios without changing the current flowing through the cascode between Vdd and ground. Further, the resistors Rx and Ry may be implemented as variable resistors, shown in FIG.7A to dynamically change the Vds_cs / Vds_cg ratio. Further, the resistors Rx and Ry may be implemented as voltage-variable resistors in the form of field-effect transistors (FETs) Qx and Qy, shown in FIG.7B, where two external voltages Vx and Vy applied to the control (gate) electrodes of such FETs) set the drain-source resistances of the FETs Qx and Qy respectively. Thus, it should be noted that while one DC bias circuit 16 has been used to produce the reference current as described, other bias circuits may be used.

It should now be appreciated a multi-stage amplifier according to the disclosure includes: a first amplifier stage comprising: a pair of transistors arranged in a cascode amplifier arrangement and an isolation circuit; and a second amplifier stage coupled to an output of the first amplifier stage; and wherein the cascode amplifier arrangement includes: a pair of transistors arranged in a cascode amplifier arrangement and a bias regulator having a reference transistor; the bias regulator produces a reference current through the reference transistor and DC bias voltages for the control electrodes of each of the pair of transistors in the cascode arrangement as a function of the reference current through the reference transistor.

It should now be appreciated an amplifier according to the disclosure includes: a first amplifier stage comprising a pair of transistors arranged in a cascode amplifier arrangement and an isolation circuit; a second amplifier stage coupled to an output of the

first amplifier stage; a voltage source coupled to the first amplifier stage and the second amplifier stage, the isolation circuit being coupled between the a pair of transistors arranged in a cascode amplifier arrangement, the voltage source producing a current serially through the isolation circuit and the pair of transistor in the cascode amplifier arrangement; a DC bias regulator comprising: a DC bias circuit for producing: a voltage related to a reference current produced by the DC bias circuit, such voltage being coupled to a control electrode of a first one of the pair of transistors and a combiner having a pair of inputs coupled to: the voltage produced by the DC bias circuit and a voltage produced by the isolation circuit, respectively, to produce a DC bias voltage at a control electrode of a second one of the pair of transistors related to a combination of the voltage produced by the DC bias circuit and the voltage produced by the combiner. The amplifier may include one or more of the following features, independently or in combination with another feature, to include: a resistor connected between the pair of pair of transistor in the cascode amplifier arrangement; wherein the DC bias regulator, comprises: a reference transistor, wherein the DC bias regulator produce the reference current through the reference transistor and wherein the DC bias regulator produces the DC bias voltages for each of the pair of transistors in the cascode amplifier arrangement as a function of the reference current produced through the reference transistor; wherein the isolation circuit comprises a pair of serially connected resistors, the resistors being connected to a common junction, wherein the combiner includes a pair or resistors each one connected to a corresponding one of the pair of inputs of the combiner and to a combiner output, the combiner output being coupled to the control of the second one of the pair of transistors, one of the pair of inputs being connected to the junction; wherein the combiner circuit produces the DC bias voltage as a function of the sum of the output voltage produced by the reference voltage and the isolation circuit; wherein the combiner circuit produces the DC bias voltage as a function of the average of the output voltage produced by the reference voltage and the voltage produced by the isolation circuit; wherein the current through the reference transistor is a saturation current for the reference transistor and current from the voltage supply to the pair of transistors in the cascode amplifier arrangement is a saturation current for both the pair of transistors in the cascode amplifier arrangement; wherein the control electrode of a first one of the pair of transistors controls a flow of carriers between a first and second electrode of the first one of the pair of transistors in the cascode amplifier arrangement, and the control electrode of the second

one of the pair of transistors in the cascode amplifier arrangement controls a flow of carriers between a first and second electrode of the second one of the pair of transistors in the cascode amplifier arrangement; and wherein the DC bias voltages produced at the control electrodes of the first one of the pair transistors in the cascode amplifier arrangement and the second one of the pair of transistor in the cascode amplifier arrangement produces a voltage across the first and second electrodes of the first one of the pair of transistors in the cascode amplifier arrangement equal to the voltage across the first and second electrodes of the second one of the pair of transistors in the cascode amplifier arrangement; wherein the resistances of the pair of resistors in the combiner are a function of the resistances of the pair of resistors in the isolation circuit and the resistance of the resistor between the pair of transistors in the cascode amplifier arrangement; wherein the combiner is a Millman passive combiner; wherein the a second amplifier stage includes a second stage transistor having a control electrode for controlling a flow of carriers between a first electrode and a second electrode and wherein the control electrode of the second stage transistor is coupled to the output of the first amplifier stage and wherein the first electrode of the second stage transistor is connected to the voltage source and the second electrode is connected to a reference potential; wherein: a first one of the electrodes of the second one of the transistors in the cascode amplifier arrangement is coupled to the voltage source through the isolation circuit, the second one of the electrodes of the second one of the pair of transistors is coupled to the second one of the electrodes of the first one of the pair of transistors in the cascode amplifier arrangement through a third resistor, and the second electrode of the first one of the pair of transistors in the pair of transistor in the cascode amplifier arrangement is coupled to the reference potential; wherein the first electrode of the second transistor is coupled to the control electrode of the second stage transistor; wherein the DC bias regulator, comprises: a reference transistor, wherein the DC bias regulator produce the reference current through the reference transistor, and wherein the DC bias regulator produces the DC bias voltages for each of the pair of transistors in the cascode amplifier arrangement as a function of the reference current produced through the reference transistor; wherein the isolation circuit comprises a pair of serially connected resistors, the resistors being connected to a common junction, wherein the combiner includes a pair or resistors each one connected to a corresponding one of the pair of inputs of the combiner and to a combiner output, the combiner output being coupled to the control of the second one of the pair of transistors,

one of the pair of inputs being connected to the junction; wherein the combiner circuit produces the DC bias voltage as a function of the sum of the output voltage produced by the reference voltage and the isolation circuit; wherein the combiner circuit produces the DC bias voltage as a function of the average of the output voltage produced by the reference voltage and the voltage produced by the isolation circuit; wherein the current through the reference transistor is a saturation current for the reference transistor and current from the voltage supply to the pair of transistors in the cascode amplifier arrangement is a saturation current for both the pair of transistors in the cascode amplifier arrangement; wherein the control electrode of a first one of the pair of transistors controls a flow of carriers between a first and second electrode of the first one of the pair of transistors in the cascode amplifier arrangement, and the control electrode of the second one of the pair of transistors in the cascode amplifier arrangement controls a flow of carriers between a first and second electrode of the second one of the pair of transistors in the cascode amplifier arrangement, and wherein the DC bias voltages produced at the control electrodes of the first one of the pair transistors in the cascode amplifier arrangement and the second one of the pair of transistor in the cascode amplifier arrangement produces a voltage across the first and second electrodes of the first one of the pair of transistors in the cascode amplifier arrangement equal to the voltage across the first and second electrodes of the second one of the pair of transistors in the cascode amplifier arrangement; or wherein: a first one of the electrodes of the second one of the transistors in the cascode amplifier arrangement is coupled to the voltage source through the isolation circuit, the second one of the electrodes of the second one of the pair of transistors is coupled to the second one of the electrodes of the first one of the pair of transistors in the cascode amplifier arrangement through a third resistor, and the second electrode of the first one of the pair of transistors in the pair of transistor in the cascode amplifier arrangement is coupled to the reference potential.

Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A multi-stage amplifier, comprising:

a first amplifier stage comprising:

a pair of transistors arranged in a cascode amplifier arrangement; and

an isolation circuit; and

a second amplifier stage coupled to an output of the first amplifier stage; and

wherein the cascode amplifier arrangement includes:

a pair of transistors arranged in a cascode amplifier arrangement; and

a bias regulator having a reference transistor; the bias regulator produces a reference current through the reference transistor and DC bias voltages for the control electrodes of each of the pair of transistors in the cascode arrangement as a function of the reference current through the reference transistor.

2. An amplifier, comprising:

a first amplifier stage comprising:

a pair of transistors arranged in a cascode amplifier arrangement; and

an isolation circuit;

a second amplifier stage coupled to an output of the first amplifier stage;

a voltage source coupled to the first amplifier stage and the second amplifier stage, the isolation circuit being coupled between the a pair of transistors arranged in a cascode amplifier arrangement, the voltage source producing a current serially through the isolation circuit and the pair of transistor in the cascode amplifier arrangement;

a DC bias regulator comprising:

a DC bias circuit for producing: a voltage related to a reference current produced by the DC bias circuit, such voltage being coupled to a control electrode of a first one of the pair of transistors; and

a combiner having a pair of inputs coupled to: the voltage produced by the DC bias circuit and a voltage produced by the isolation circuit, respectively, to produce a DC bias voltage at a control electrode of a second one of the pair of transistors related to a combination of the voltage produced by the DC bias circuit and the voltage produced by the combiner.

3. The amplifier recited in claim 2 including a resistor connected between the pair of pair of transistor in the cascode amplifier arrangement.

4. The amplifier recited in claim 2 wherein the DC bias regulator, comprises:

a reference transistor;

wherein the DC bias regulator produce the reference current through the reference transistor; and

wherein the DC bias regulator produces the DC bias voltages for each of the pair of transistors in the cascode amplifier arrangement as a function of the reference current produced through the reference transistor.

5. The amplifier recited in claim 3 including a resistor connected between the pair of transistors in the cascode amplifier arrangement.

6. The amplifier recited in claim 2 wherein the isolation circuit comprises a pair of serially connected resistors, the resistors being connected to a common junction, wherein the combiner includes a pair or resistors each one connected to a corresponding one of the pair of inputs of the combiner and to a combiner output, the combiner output being coupled to the control of the second one of the pair of transistors, one of the pair of inputs being connected to the junction.

7. The amplifier recited in claim 6 wherein the combiner circuit produces the DC bias voltage as a function of the sum of the output voltage produced by the reference voltage and the isolation circuit.

8. The amplifier recited in claim 7 wherein the combiner circuit produces the DC bias voltage as a function of the average of the output voltage produced by the reference voltage and the voltage produced by the isolation circuit.

9. The amplifier recited in claim 8 wherein the current through the reference transistor is a saturation current for the reference transistor and current from the voltage supply to the pair of transistors in the cascode amplifier arrangement is a saturation current for both the pair of transistors in the cascode amplifier arrangement.

10. The amplifier recited in claim 8 wherein the control electrode of a first one of the pair of transistors controls a flow of carriers between a first and second electrode of the first one of the pair of transistors in the cascode amplifier arrangement, and the control electrode of the second one of the pair of transistors in the cascode amplifier arrangement controls a flow of carriers between a first and second electrode of the second one of the pair of transistors in the cascode amplifier arrangement; and wherein the DC bias voltages produced at the control electrodes of the first one of the pair transistors in the cascode amplifier arrangement and the second one of the pair of transistor in the cascode amplifier arrangement produces a voltage across the first and second electrodes of the first one of the pair of transistors in the cascode amplifier arrangement equal to the voltage across the first and second electrodes of the second one of the pair of transistors in the cascode amplifier arrangement.

11. The amplifier recited in claim 6 wherein the resistances of the pair of resistors in the combiner are a function of the resistances of the pair of resistors in the isolation circuit and the resistance of the resistor between the pair of transistors in the cascode amplifier arrangement.

12. The amplifier recited in claim 11 wherein the combiner is a Millman passive combiner.

13 The amplifier recited in claim 2 wherein the a second amplifier stage includes a second stage transistor having a control electrode for controlling a flow of carriers between a first electrode and a second electrode and wherein the control electrode of the

second stage transistor is coupled to the output of the first amplifier stage and wherein the first electrode of the second stage transistor is connected to the voltage source and the second electrode is connected to a reference potential.

14. The amplifier recited in claim 13 wherein: a first one of the electrodes of the second one of the transistors in the cascode amplifier arrangement is coupled to the voltage source through the isolation circuit; the second one of the electrodes of the second one of the pair of transistors is coupled to the second one of the electrodes of the first one of the pair of transistors in the cascode amplifier arrangement through a third resistor; and the second electrode of the first one of the pair of transistors in the pair of transistor in the cascode amplifier arrangement is coupled to the reference potential.

15. The amplifier recited in claim 14 wherein the first electrode of the second transistor is coupled to the control electrode of the second stage transistor.

16. The amplifier recited in claim 15 wherein the DC bias regulator, comprises:

a reference transistor;

wherein the DC bias regulator produce the reference current through the reference transistor; and

wherein the DC bias regulator produces the DC bias voltages for each of the pair of transistors in the cascode amplifier arrangement as a function of the reference current produced through the reference transistor.

17. The amplifier recited in claim 16 wherein the isolation circuit comprises a pair of serially connected resistors, the resistors being connected to a common junction, wherein the combiner includes a pair or resistors each one connected to a corresponding one of the pair of inputs of the combiner and to a combiner output, the combiner output being coupled to the control of the second one of the pair of transistors, one of the pair of inputs being connected to the junction.

18. The amplifier recited in claim 17 wherein the combiner circuit produces the DC bias voltage as a function of the sum of the output voltage produced by the reference voltage and the isolation circuit.

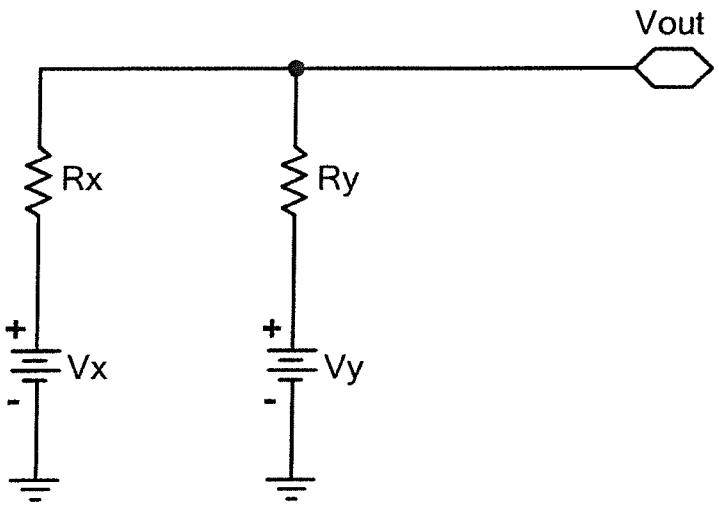
19. The amplifier recited in claim 18 wherein the combiner circuit produces the DC bias voltage as a function of the average of the output voltage produced by the reference voltage and the voltage produced by the isolation circuit.

20. The amplifier recited in claim 17 wherein the current through the reference transistor is a saturation current for the reference transistor and current from the voltage supply to the pair of transistors in the cascode amplifier arrangement is a saturation current for both the pair of transistors in the cascode amplifier arrangement.

21. The amplifier recited in claim 13 wherein the control electrode of a first one of the pair of transistors controls a flow of carriers between a first and second electrode of the first one of the pair of transistors in the cascode amplifier arrangement, and the control electrode of the second one of the pair of transistors in the cascode amplifier arrangement controls a flow of carriers between a first and second electrode of the second one of the pair of transistors in the cascode amplifier arrangement; and wherein the DC bias voltages produced at the control electrodes of the first one of the pair transistors in the cascode amplifier arrangement and the second one of the pair of transistor in the cascode amplifier arrangement produces a voltage across the first and second electrodes of the first one of the pair of transistors in the cascode amplifier arrangement equal to the voltage across the first and second electrodes of the second one of the pair of transistors in the cascode amplifier arrangement.

22. The amplifier recited in claim 21 wherein: a first one of the electrodes of the second one of the transistors in the cascode amplifier arrangement is coupled to the voltage source through the isolation circuit; the second one of the electrodes of the second one of the pair of transistors is coupled to the second one of the electrodes of the first one of the pair of transistors in the cascode amplifier arrangement through a third resistor; and the second electrode of the first one of the pair of transistors in the pair of transistor in the cascode amplifier arrangement is coupled to the reference potential.

23. The amplifier recited in claim 22 wherein the first electrode of the second transistor is coupled to the control electrode of the second stage transistor.



- In general case:

$$V_{out} = \frac{\frac{V_x}{R_x} + \frac{V_y}{R_y}}{\frac{1}{R_x} + \frac{1}{R_y}} = \frac{V_x R_y + V_y R_x}{R_x + R_y}$$

- In a specific case of $R_x = R_y$

$$V_{out} = \frac{V_x + V_y}{2}$$

FIG. 1

Prior Art

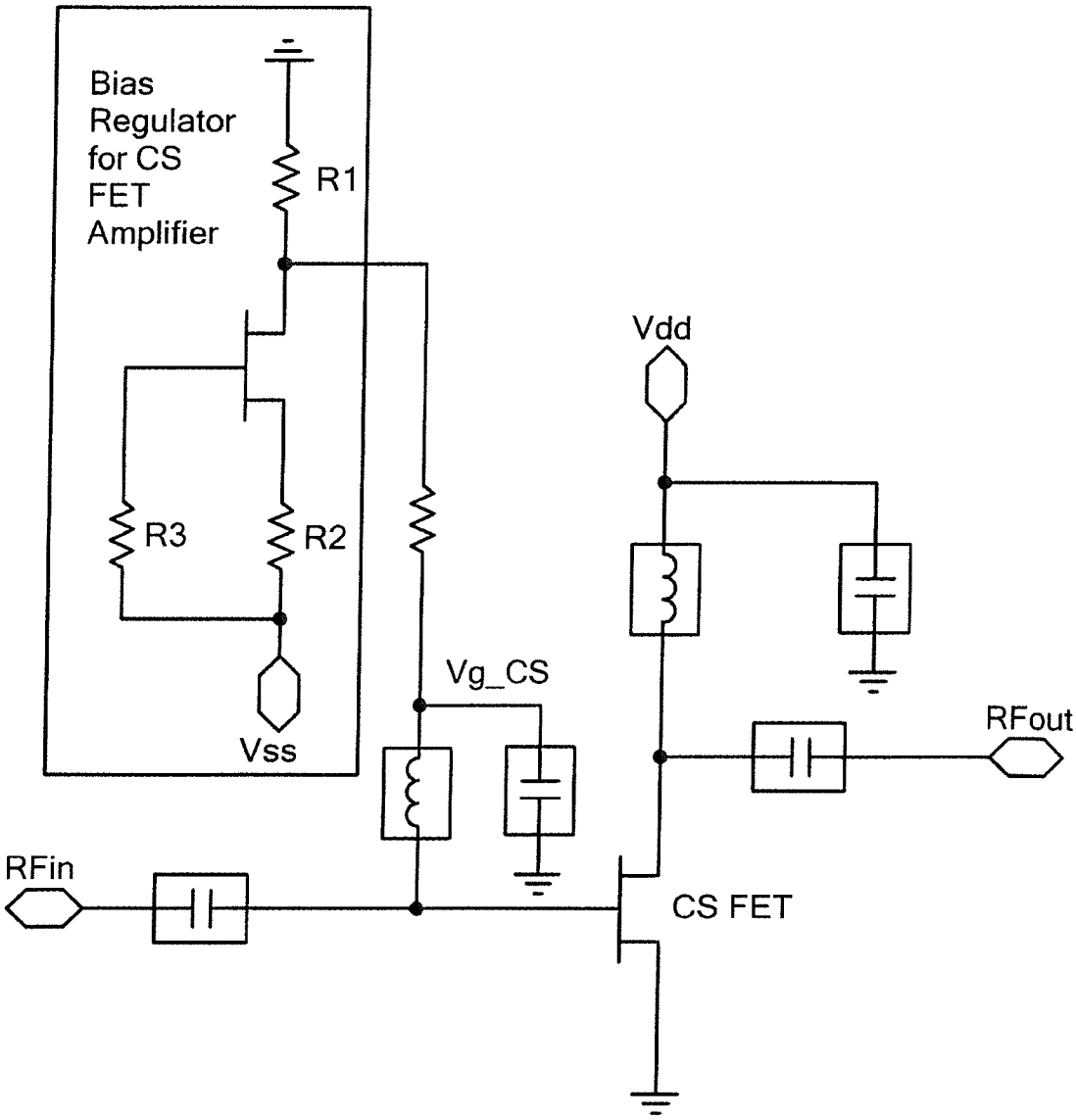


FIG. 2

Prior Art

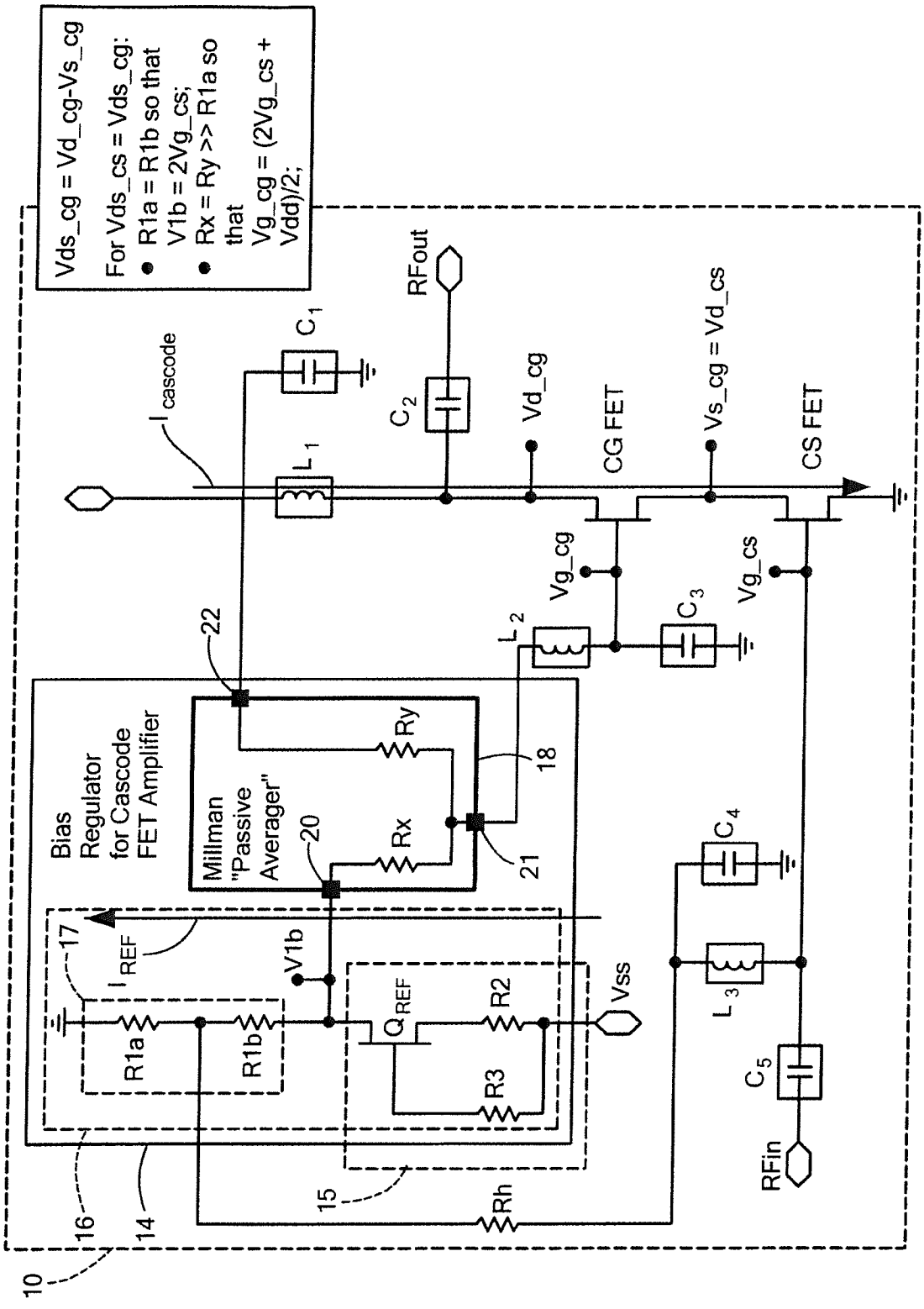

Vds_cg = Vd_cg-Vs_cg
For Vds_cs = Vds_cg:
R1a = R1b so that V1b = 2Vg_cs;
Rx = Ry >> R1a so that Vg_cg = (2Vg_cs + Vdd)/2;
RFout
C1
C2
Vd_cg
CG FET
Vs_cg = Vd_cs
CS FET
I cascode
L1
Vg_cg
Vg_cs
C3
L2
22
Bias Regulator for Cascode FET Amplifier
Millman "Passive Averager"
Ry
Rx
18
20
21
C4
17
I REF
V1b
R1a
R1b
QREF
R2
R3
Vss
L3
C5
RFin
Rh
16
14
15
10

FIG. 3

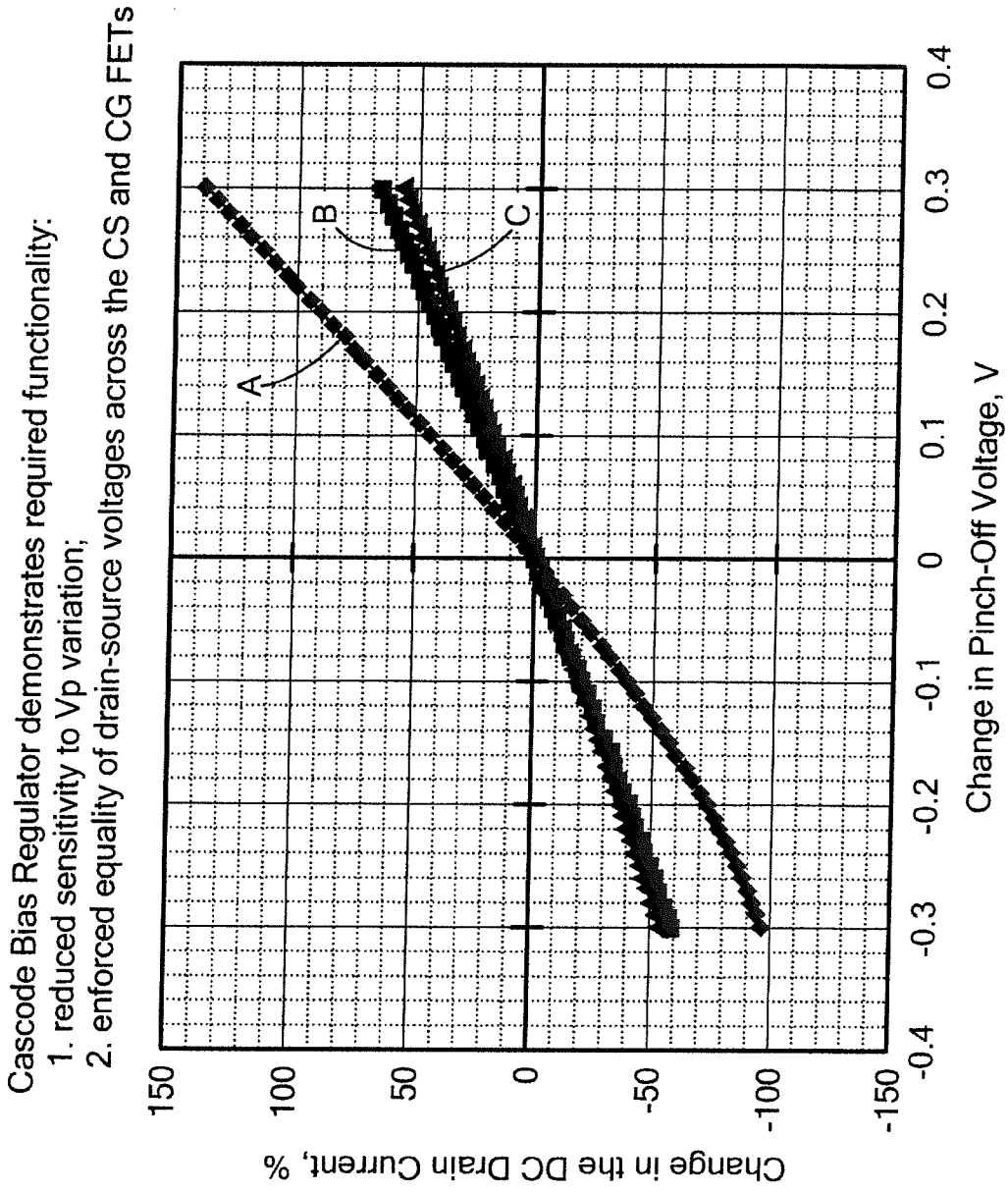

Cascode Bias Regulator demonstrates required functionality:
1. reduced sensitivity to Vp variation;
2. enforced equality of drain-source voltages across the CS and CG FETs
Change in the DC Drain Current, %
150
100
50
0
-50
-100
-150
-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
Change in Pinch-Off Voltage, V
A
B
C

FIG. 4A

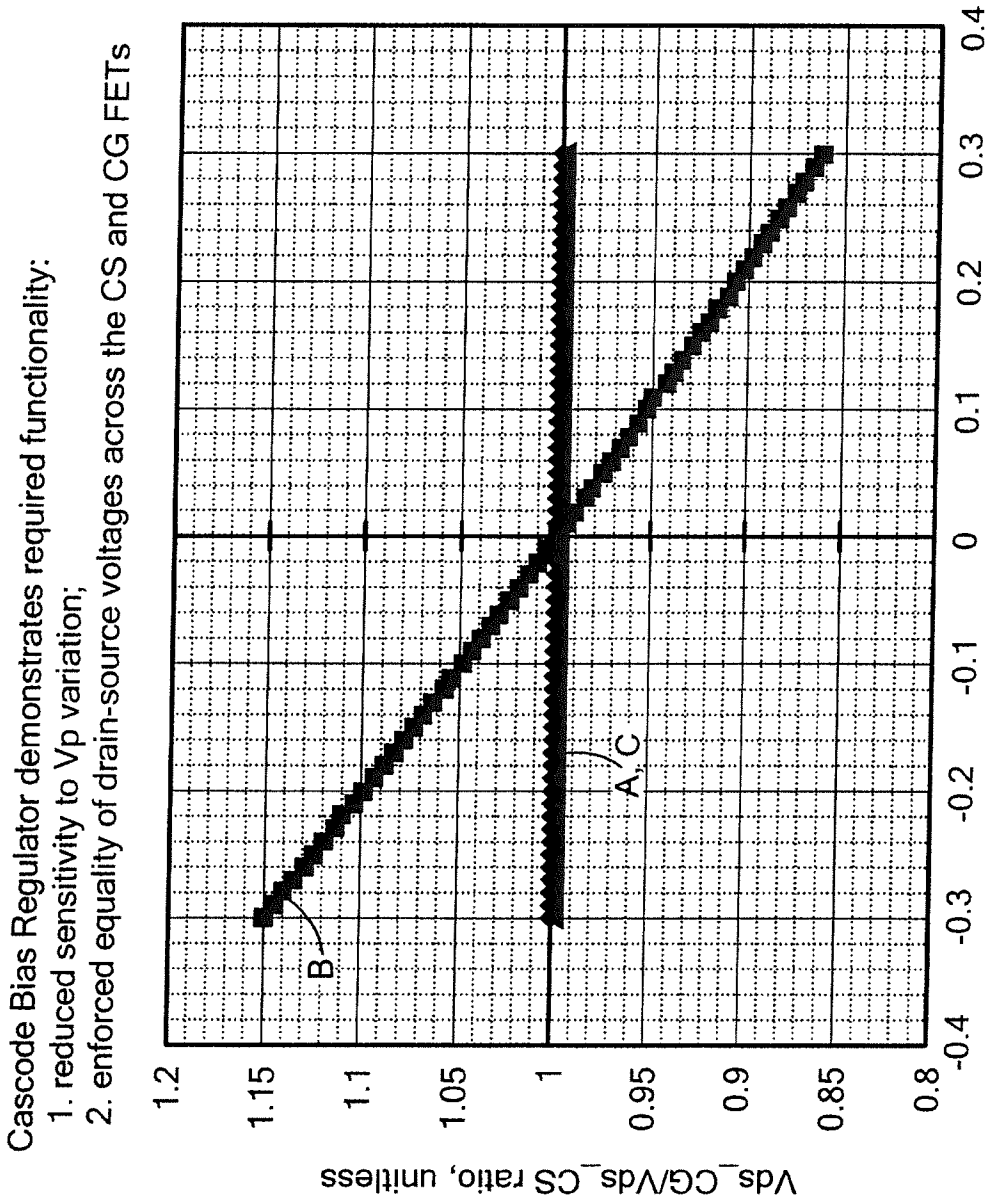
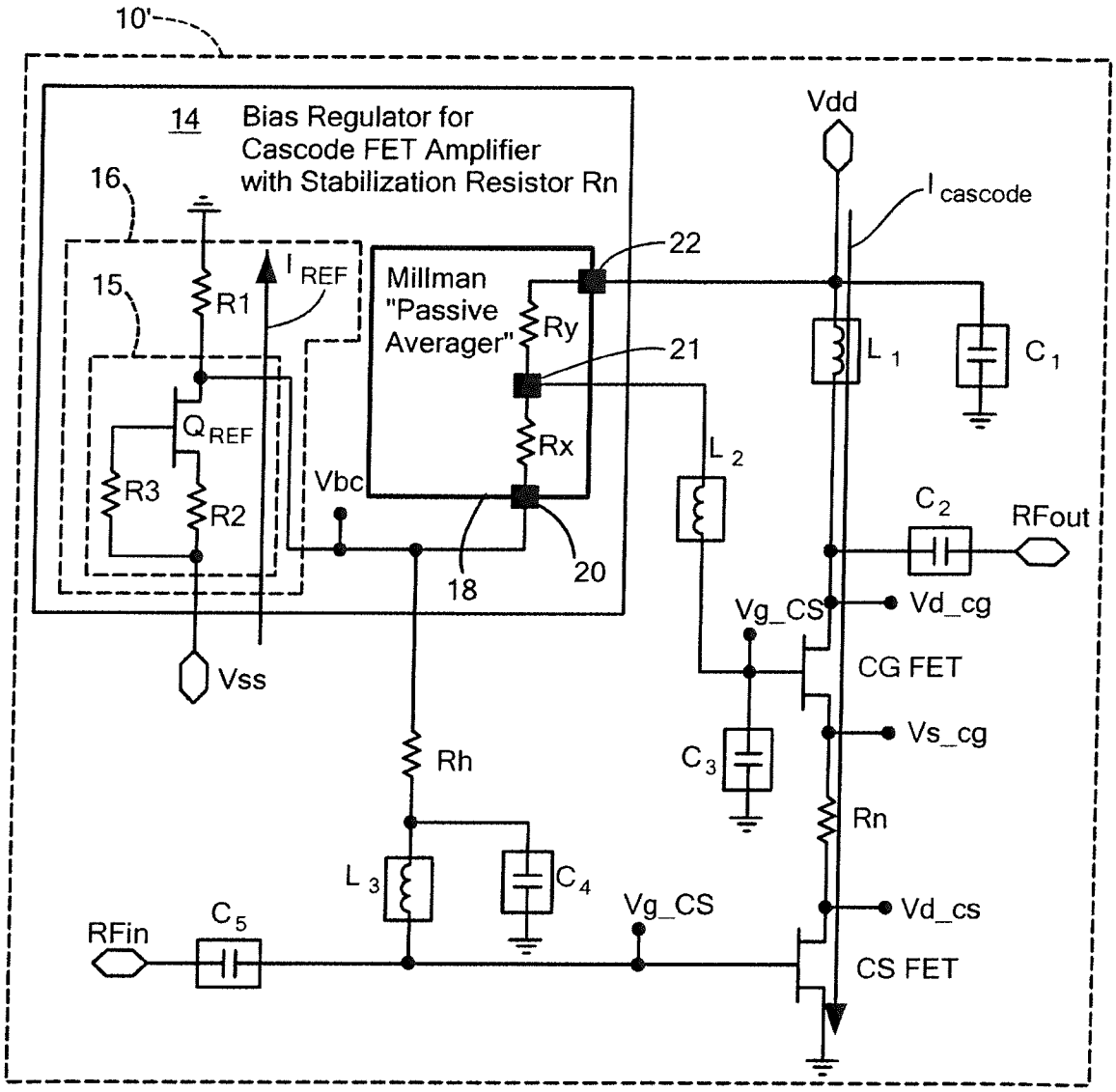

Cascode Bias Regulator demonstrates required functionality:
1. reduced sensitivity to Vp variation;
2. enforced equality of drain-source voltages across the CS and CG FETs
Vds_CG/Vds_CS ratio, unitless
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
B
A, C
-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
Change in Pinch-Off Voltage, V

FIG. 4B



Vds_cg = Vd_cg-Vs_cg

For Vds_cs = Vds_cg:

- $a = \frac{R_y}{R_x} = \frac{V_{dd} - 2V_{bc} - I_{cascode} R_n}{V_{dd} + I_{cascode} R_n}$
- Rx >> R1.

FIG. 5

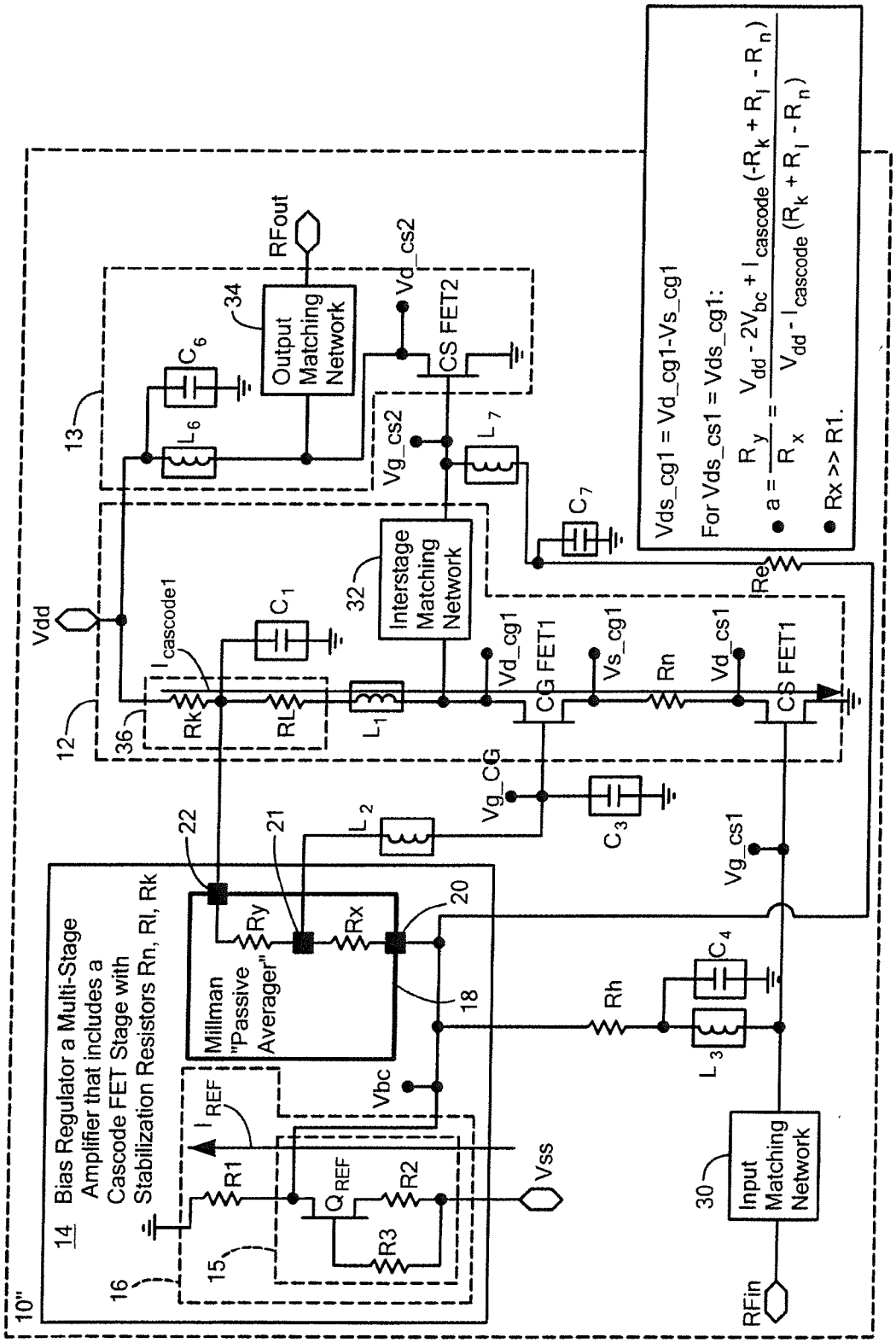

10"
14 Bias Regulator a Multi-Stage Amplifier that includes a Cascode FET Stage with Stabilization Resistors Rn, Rl, Rk
Millman "Passive Averager"
Ry
Rx
Rh
R1
R2
R3
Rk
RL
Rn
Re
Vdd
Vss
Vbc
Vg_CG
Vg_cs1
Vg_cs2
Vd_cg1
Vs_cg1
Vd_cs1
Vd_cs2
RFout
RFin
Output Matching Network
Interstage Matching Network
Input Matching Network
CG FET1
CS FET1
CS FET2
Vds_cg1 = Vd_cg1-Vs_cg1
For Vds_cs1 = Vds_cg1:
Rx >> R1.

FIG. 6

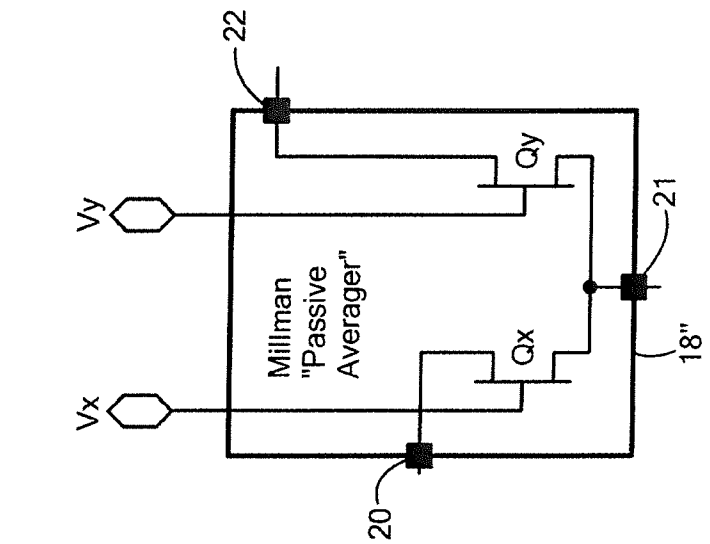

22
Qy
Vy
Millman
"Passive
Averager"
21
Qx
18"
Vx
20

FIG. 7B

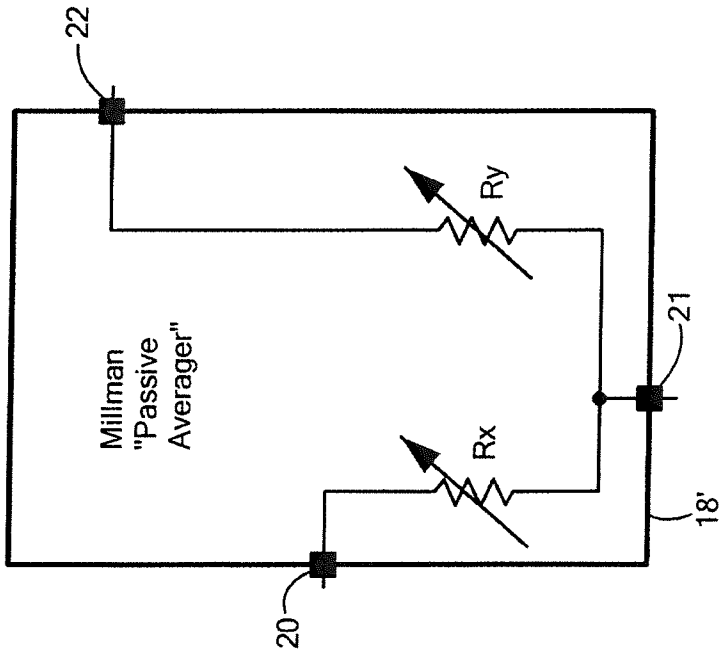

22
Ry
Millman
"Passive
Averager"
21
Rx
18'
20

FIG. 7A

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/045723

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/22 H03F1/30 H03F1/08 H03F3/193
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/127776 A1 (CHOW YUT HOONG [MY] ET AL) 27 May 2010 (2010-05-27) paragraphs [0020] - [0060]; figures 3,6	1-23
A	US 2009/085664 A1 (YANG PO-TANG [TW] ET AL) 2 April 2009 (2009-04-02) paragraphs [0004] - [0041]; figures 1-4	1-23
A	GB 2 075 298 A (GTE LABORATORIES INC) 11 November 1981 (1981-11-11) page 1, left-hand column, line 5 - page 3, right-hand column, line 92; figure 1	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2016	06/12/2016

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/045723

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