(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 December 2011 (15.12.2011)

PCT

(10) International Publication Number
WO 2011/153608 A1

(51) International Patent Classification:
G11C 11/4091 (2006.01) *G11C 11/4094* (2006.01)
G11C 11/406 (2006.01)

(21) International Application Number:
PCT/CA2011/000242

(22) International Filing Date:
4 March 2011 (04.03.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/353,437 10 June 2010 (10.06.2010) US

(71) Applicant *(for all designated States except US)*: **MOSAID TECHNOLOGIES INCORPORATED** [CA/CA]; 11Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **CHOI, Byoung, Jin** [KR/CA]; 104 Brady Avenue, Kanata, Ontario K2K 0B1 (CA).

(74) Agent: **SMART & BIGGAR**; 1000 de la Gauchetière Street West, Suite 3300, Montréal, Québec H3B 4W5 (CA).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: SEMICONDUCTOR MEMORY DEVICE WITH SENSE AMPLIFIER AND BITLINE ISOLATION

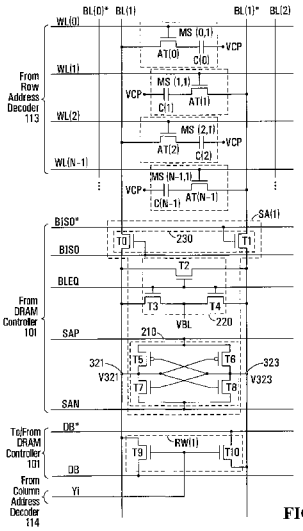


FIG. 2

(57) Abstract: A semiconductor memory device, including: a memory cell connected to a first bitline and associated with a second bitline; a sense amplifier, including a first input/output node and a second input/output node; and an isolator connected to the bitlines and to the input/output nodes, the isolator being configured to carry out bitline isolation during a refresh operation of the memory cell, where the bitline isolation includes electrically disconnecting the first bitline from the first input/output node and electrically disconnecting the second bitline from the second input/output node, followed by: electrically re-connecting the first bitline to the first input/output node while the second bitline remains electrically disconnected from the second input/output node.

WO 2011/153608 A1

SEMICONDUCTOR MEMORY DEVICE WITH SENSE AMPLIFIER AND BITLINE ISOLATION

TECHNICAL FIELD

[0001] The present invention relates generally to semiconductor memory devices and, more particularly, to a dynamic random access memory (DRAM) device with a sense amplifier and bitline isolation.

BACKGROUND

[0002] Today's mobile phones, laptops, tablet computers, game consoles, set-top boxes, GPS units and other electronics require random access memory. One form of random access memory is dynamic random access memory (DRAM), which is often used because of its high memory density (number of bits stored per unit area or volume).

[0003] Examples of background art that describe DRAM devices include U.S. Patent 5,148,399 granted to Cho et al. on September 15, 1992, entitled "Sense Amplifier Circuitry Selectively Separable From Bit Lines For Dynamic Random Access Memory", and U.S. Patent 7,505,343 granted to Kang on March 17, 2009, entitled "Sense Amplifier Circuit In Semiconductor Memory Device And Driving Method Thereof".

[0004] Cho et al. disclose an integrated circuit memory device that includes a sense amplifier circuit having a first transistor coupling section connected between a pair of bitlines and a pair of sense amplifier nodes. The sense amplifier circuit further includes a first sense amplifier connected between the sense amplifier nodes so as to selectively discharge one of the sense amplifier nodes and a second sense amplifier connected between the sense

amplifier nodes so as to selectively charge the other one of the sense amplifier nodes.

[0005] Kang discloses a sense amplifier circuit in a semiconductor memory device in which an under-drive is applied to a switching element of a pull-down side of a sense amplifier in order to compensate for poor driving capability in the case of performing a low voltage operation. The sense amplifier circuit includes: a sense amplifier which has a pull-down element composed of an NMOS transistor and a pull-up element composed of a PMOS transistor and is formed between bitlines to perform data exchange; and a drive controller which supplies a drive voltage for the use of pull-up and pull-down operations to the sense amplifier in order to perform the data exchange, and, during a specific time period included in a time for providing the drive voltage, performs an under-drive whereby the drive voltage for the use of the pull-down operation is used so that the sense amplifier is provided with a voltage that is lower than a voltage used in the pull-down operation in a normal state.

[0006] One feature of DRAM devices such as those of Cho et al. and Kang is that they must be refreshed in order to retain the data stored therein. Refreshing of the data occurs frequently and consumes power. This can be an issue for battery-operated units such as mobile phones and laptop/tablet computers. Therefore, it would be beneficial to devise power efficient methods and apparatus for refreshing the data stored in a DRAM device.

SUMMARY

[0007] According to a first broad aspect, embodiments of the present invention seek to provide a semiconductor memory device, including: a memory cell connected to a first bitline and associated with a second bitline; a sense amplifier, including a first input/output node and a second input/output node; and an isolator connected to the bitlines and to the input/output nodes, the isolator being controllable during a refresh operation of the memory cell to cause the first

bitline to be electrically connected to or disconnected from the first input/output node and, independently, to cause the second bitline to be electrically connected to or disconnected from the second input/output node.

[0008] According to a second broad aspect, embodiments of the present invention seek to provide a semiconductor memory device, including: a memory cell connected to a first bitline and associated with a second bitline; a sense amplifier, including a first input/output node and a second input/output node; and an isolator connected to the bitlines and to the input/output nodes, the isolator being configured to carry out bitline isolation during a refresh operation of the memory cell, where the bitline isolation includes electrically disconnecting the first bitline from the first input/output node and electrically disconnecting the second bitline from the second input/output node, followed by: electrically re-connecting the first bitline to the first input/output node while the second bitline remains electrically disconnected from the second input/output node.

[0009] According to a third broad aspect, embodiments of the present invention seek to provide a semiconductor memory device, including: a memory cell connected to a first bitline and associated with a second bitline; a sense amplifier, including a first input/output node and a second input/output node; and an isolator connected to the bitlines and to the input/output nodes, the isolator being configured to carry out bitline isolation during a refresh operation of the memory cell, wherein the bitline isolation includes electrically disconnecting the second bitline from the second input/output node while the first bitline remains electrically connected to the first input/output node.

[0010] According to a fourth broad aspect, embodiments of the present invention seek to provide a method of refreshing a memory cell connected to a first bitline and associated with a second bitline, the method including: connecting the first bitline to a first input/output node of a sense amplifier and connecting the second bitline to a second input/output node of the sense amplifier; triggering charge sharing between the memory cell and the first bitline; disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the second input/output node; activating the sense amplifier to initiate a

signal amplification process at the first and second input/output nodes; and re-connecting the first bitline to the first input/output node while the second bitline remains disconnected from the second input/output node.

[0011] According to a fifth broad aspect, embodiments of the present invention seek to provide a method of refreshing a memory cell connected to a first bitline and associated with a second bitline, the method including: connecting the first bitline to a first input/output node of a sense amplifier and connecting the second bitline to a second input/output node of the sense amplifier; triggering charge sharing between the memory cell and the first bitline; disconnecting the second bitline from the second input/output node while the first biltine remains connected to the first input/output node; and activating the sense amplifier to initiate a signal amplification process at the first and second input/output nodes.

[0012] Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Embodiments of the present invention will now be described, by way of example only, with reference to the attached drawings, wherein:

[0014] Fig. 1 is a block diagram illustrating an example of a dynamic random access memory (DRAM) device to which an embodiment of the present application is applicable;

[0015] Fig. 2 is a block diagram illustrating an example of a sense amplifier, according to an embodiment of the present invention;

[0016] Fig. 3A is a timing diagram showing operation of the sense amplifier of Fig. 2 when performing an "auto-refresh and read" operation;

[0017] Fig. 3B is a timing diagram showing operation of the sense amplifier of Fig. 2 when performing a "self-refresh" operation, according to an embodiment of the present invention;

[0018] Fig. 3C is a timing diagram showing operation of the sense amplifier of Fig. 2 when performing a "self-refresh" operation, according to another embodiment of the present invention;

[0019] Fig. 4 is a block diagram illustrating an example of a DRAM device to which another embodiment of the present application is applicable; and

[0020] Fig. 5 is a block diagram illustrating an example of a sense amplifier, according to an alternative embodiment of the present invention.

DETAILED DESCRIPTION

[0021] In the following detailed description, reference is made to the accompanying drawings, showing by way of illustration specific sample embodiments in which the present invention may be practiced. It is to be understood that other embodiments may be utilized and that logical, mechanical, electrical, and other changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, the scope of the present invention being defined by the appended claims.

[0022] Reference is made to Fig. 1, which shows a semiconductor memory device, in this case a dynamic random access memory (DRAM) device 100.

[0023] The DRAM device 100 includes a DRAM controller 101 and a memory array 102 comprising a set of memory cells arranged into N rows and M columns. Each memory cell can be used to store electrical charge representative of a data bit. A particular memory cell is denoted MS(x,y), where "x" (ranging from 0 to N-1) denotes the row and "y" (ranging from 0 to M-1) denotes the column in which the particular memory cell is located.

[0024] The DRAM device 100 also includes a row address decoder 113. The row address decoder 113 is connected to the DRAM controller 101, from which it receives the identity of a row in which is located a particular memory cell that is to be read from, written to or refreshed. The row address decoder 113 is connected to a plurality of wordlines WL(0), WL(1), ..., WL(N-1). The voltage on the wordlines WL(0), WL(1), ..., WL(N-1) can be made to vary between a first supply voltage VSS and a high positive voltage VPP. A suitable but non-limiting example value of the first supply voltage VSS is 0V, whereas a suitable but non-limiting example value of the high positive voltage VPP is 3.0V. By placing the high positive voltage VPP on a particular one of the wordlines WL(0), WL(1), ..., WL(N-1), a corresponding row of the memory array 102 is "enabled". The effect of enabling a row of the memory array 101 will become apparent from the description below.

[0025] The DRAM device 100 also includes a column address decoder 114. The column address decoder 114 is connected to the DRAM controller 101, from which it receives the identity of a column in which is located a particular memory cell that is to be read from or written to.

[0026] The DRAM device 100 also includes a plurality of read/write circuits RW(0), RW(1), ..., RW(M-1) and a plurality of sense amplifiers SA(0), SA(1), ..., SA(M-1), which will now be described in greater detail below.

[0027] Within the memory array 102, a pair of bitlines runs along each particular column, and each bitline in the particular column connects alternate cells in the particular column to a corresponding read/write circuit and to a corresponding sense amplifier for that column. For example, in column 0, a "left" bitline BL(0) connects memory cells MS(0,0), MS(2,0), MS(N-2,0) to read/write circuit RW(0) and to sense amplifier SA(0), whereas a "right" bitline BL(0)* connects memory cells MS(1,0), MS(3,0), MS(N-1,0) to the same read/write circuit RW(0) and to the same sense amplifier SA(0). In a similar fashion, a "left" bitline BL(1) and a "right" bitline BL(1)* connect alternating groups of cells in column 1 to read/write circuit RW(1) and to sense amplifier SA(1). A similar interconnectivity pattern with a "left" bitline and a "right" bitline applies to the other

columns of the memory array, i.e., from column 2 through column M-1. Of course, it should be understood that the terms "left" and "right" are used only for convenience and simplicity in reference to the pair of bitlines in a given column, and is not intended to confine the bitlines to a particular spatial location within an actual implementation. The "left" and "right" bitlines could indeed have been called "first" and "second" bitlines, "main" and "complementary" bitlines, "positive" and "negative" bitlines, etc.

[0028] Reference is now made to Fig. 2, which by way of non-limiting example illustrates a portion 200 of the DRAM device 100 in Fig. 1. Specifically, the portion 200 includes memory cells MS(0,1), MS(1,1), ..., MS(N-1,1) in column 1 of the memory array 102. (It is assumed that N is an even number, but this need not be the case in every embodiment.) Also forming part of portion 200 is read/write circuit RW(1) and sense amplifier SA(1) associated with column 1 of the memory array 102. It will be recalled that the pair of bitlines connected to read/write circuit RW(1) and sense amplifier SA(1) include left bitline BL(1) and right bitline BL(1)*. The following provides a more detailed description of the elements in portion 200.

[0029] Memory cell MS(0,1) includes an access transistor AT(0) with a drain connected to left bitline BL(1) and a source connected to a charge storage capacitor C(0). Another terminal of capacitor C(0) is connected to a cell plate voltage VCP (e.g., VDD/2). Transistor AT(0) also has a gate that is connected to wordline WL(0). Similarly, memory cell MS(2,1) includes an access transistor AT(2) with a drain connected to left bitline BL(1) and a source connected to a charge storage capacitor C(2). Another terminal of capacitor C(2) is connected to the cell plate voltage VCP. Transistor AT(2) also has a gate that is connected to wordline WL(2).

[0030] The same description applies to memory cell MS(1,1), except with respect to the right bitline BL(1)*. Specifically, memory cell MS(1,1) includes an access transistor AT(1) having a drain connected to right bitline BL(1)* and a source connected to a charge storage capacitor C(1). Another terminal of

capacitor C(1) is connected to the cell plate voltage VCP. Transistor AT(1) also has a gate that is connected to wordline WL(1).

[0031] Considering now operation of memory cell MS(0,1) in particular, when wordline WL(0) is enabled by the row address decoder 113, this turns on transistor AT(0), thereby electrically connecting capacitor C(0) to left bitline BL(1). In order to write a logic "1" to memory cell MS(0,1), a second supply voltage VDD is applied across capacitor C(0), whereas in order to write a logic "0" to memory cell MS(0,1), the aforementioned first supply voltage VSS is applied across capacitor C(0). A suitable but non-limiting example value of the second supply voltage VDD is 1.5V.

[0032] On the other hand, when wordline WL(0) is disabled, this turns off transistor AT(0), thereby electrically disconnecting left bitline BL(1) from capacitor C(0). This is done with the intent of keeping capacitor C(0) charged (or discharged, depending on the value of the data bit written to memory cell MS(0,1)). However, charge will dissipate from (or into) capacitor C(0) after a relatively short period of time and therefore the original charged or discharged state of capacitor C(0) needs to be periodically reapplied to capacitor C(0). This is the purpose of a "refresh" operation, which should regularly and frequently if one wishes the correct data bit to be accessible by reading memory cell MS(0,1) at some future time. The maximum amount of time allowable between refresh operations without risk of data error on a subsequent read operation is determined by the charge storage capabilities of capacitor C(0). In the industry, it is not unusual to specify the time between refresh operations (i.e., the "refresh period") to be on the order of 64 milliseconds.

[0033] Read/write circuit RW(1) includes NMOS transistors T9 and T10. Each of the transistors T9 and T10 has a gate, a source and a drain. The drain of transistor T9 is connected to left bitline BL(1) and the source of transistor T9 is connected to a first data line DB. The drain of transistor T10 is connected to a second data line DB* and the source of transistor T10 is connected to right bitline BL(1)*. The first data line DB and the second data line DB* are similarly connected through to the other sense amplifiers SA(0), SA(2), SA(3), ..., SA(M-

1). A column address line Yi, supplied by the column address decoder 114, is connected to the gates of transistors T9 and T10. The voltage on the column address line Yi can be made to vary between the first supply voltage VSS and the second supply voltage VDD.

[0034] Turning now to sense amplifier SA(1), this component includes a sense amplifier circuit 210, a bitline equalizer 220 and an isolator 230. Each of these components is now described.

[0035] In a non-limiting embodiment, the sense amplifier circuit 210 includes two P-channel transistors T5, T6 and two N-channel transistors T7, T8 that are cross-coupled. The cross-coupled transistors are connected to the DRAM controller 101 via a pair of sensing activation lines SAP, SAN. The sense amplifier circuit 210 has two input/output nodes 321 and 323 that connect to the cross-coupled transistors. Specifically, each of the transistors T5, T6, T7 and T8 has a gate, a source and a drain. The source of transistor T5 is connected to the drain of transistor T7, to the gate of transistor T6, to the gate of transistor T8 and to input/output node 321. In addition, the source of transistor T6 is connected to the drain of transistor T8, to the gate of transistor T5, to the gate of transistor T7 and to input/output node 323. Also, the drain of transistor T5 is connected to the drain of transistor T6 and to sensing activation line SAP. Finally, the source of transistor T7 is connected to the source of transistor T8 and to sensing activation line SAN. The voltage on sensing activation line SAP can be made to vary between a bitline pre-charge voltage VBL and the second supply voltage VDD, whereas the voltage on sensing activation line SAN can be made to vary between the first supply voltage VSS and the aforementioned bitline pre-charge voltage VBL.

[0036] In a non-limiting embodiment, the bitline equalizer 220 comprises three N-channel transistors T2, T3 and T4. Each of the transistors T2, T3, and T4 has a gate, a source and a drain. The drain of transistor T2 is connected between left bitline BL(1) and the source of transistor T2 is connected to right bitline BL(1)*. The drain of transistor T3 is connected to left bitline BL(1) and the source of transistor T4 is connected to right bitline BL(1)*. The bitline pre-charge

voltage VBL is fed to the junction where the source of transistor T3 meets the drain of transistor T4. In an embodiment, the bitline pre-charge voltage VBL is kept between the first supply voltage VSS and the second supply voltage VDD. In an embodiment, the bitline pre-charge voltage VBL is kept midway between VSS and VDD, i.e., VBL = ½(VDD + VSS).

[0037] The bitline equalizer 220 is connected to the DRAM controller 101 via a bitline equalization line BLEQ. Specifically, the bitline equalization line BLEQ leads to the gates of transistors T2, T3 and T4. The voltage on the bitline equalization line can be made to vary between the first supply voltage VSS and the second supply voltage VDD, which allows switching on and off of the gates of transistors T2, T3 and T4. Consequently, the electric potential between left bitline BL(1) and right bitline BL(1)* can be equalized under control of the DRAM controller 101.

[0038] In a non-limiting embodiment, the isolator 230 can include two bitline isolation transistors, namely N-channel transistors T0 and T1. Each of the transistors T0 and T1 has a gate, a source and a drain. Transistor T0 is connected between the sense amplifier circuit 210 and left bitline BL(1), whereas transistor T1 is connected between the sense amplifier circuit 210 and right bitline BL(1)*. More specifically, the source and the drain of transistor T0 are connected to the left bitline BL(1) and to input/output node 321, respectively. Similarly, the source and the drain of transistor T1 are connected to right bitline BL(1)* and to input/output node 323, respectively.

[0039] A first bitline isolation line BIS0 connects the gate of transistor T0 to the DRAM controller 101, whereas a second bitline isolation line BIS0* connects the gate of transistor T1 to the DRAM controller 101. The voltage on each of the bitline isolation lines BIS0, BIS0* can be made to vary between the first supply voltage VSS and the high positive voltage VPP. In this way, left bitline BL(1) can be electrically disconnected from and re-connected to input/output node 321 in a controllable fashion. Similarly, right bitline BL(1)* can be electrically disconnected from and re-connected to input/output node 323. In an embodiment, the bitline isolation lines BIS0, BIS0* are controlled independently

so that their respective voltages may change (i.e., rise or fall) at different times, although they can also be made to change together (simultaneously). This allows independent isolation of bitlines BL(1), BL(1)* from input/output nodes 321, 323, respectively.

[0040] The following will now describe operation of sense amplifier SA(1) under various circumstances.

[0041] Firstly, a pre-charge operation will be described. To begin with, it is assumed that wordline WL(0) is at the first supply voltage VSS and sensing activation lines SAP, SAN are at the biltine pre-charge voltage VBL. DRAM controller 101 then sets the voltage on bitline isolation line BLEQ to the second supply voltage VDD, thereby turning on transistors T2, T3 and T4. This has the effect of forcing the voltage on input/output nodes 321 and 323 to the bitline pre-charge voltage VBL. Meanwhile, the voltage on first bitline isolation line BIS0 and the voltage on second bitline isolation line BIS0* are kept at the high positive voltage VPP, thus keeping transistors T0 and T1 in a conductive state. This electrically connects left bitline BL(1) to input/output node 321 and also connects right bitline BL(1)* to input/output node 323, hence causing both the voltage on left bitline BL(1) and the voltage on right bitline BL(1)* to also be at VBL. It is recalled that in an embodiment, VBL may be midway between the first supply voltage VSS and the second supply voltage VDD. The DRAM controller 101 then sets the voltage on the bitline isolation line BLEQ to VSS, disconnecting left bitline BL(1) from right bitline BL(1)* but leaving them pre-charged.

[0042] Reference is now made to Fig. 3A, which is a timing diagram showing operation of the sense amplifier SA(1) of Fig. 2 during an "auto-refresh and read" operation, following the aforementioned bitline pre-charge operation. In this case, the voltage on first bitline isolation line BIS0 and the voltage on second bitline isolation line BIS0* are kept at the high positive voltage VPP, thus effectively placing transistors T0 and T1 in a conductive state and leaving them as such throughout the "auto-refresh and read" operation.

[0043] $\tau 0$: The row address decoder 113 activates wordline WL(0) (i.e., the voltage on wordline WL(0) transitions from the first

supply voltage VSS to the high positive voltage VPP). This turns on transistor AT(0) forming part of memory cell MS(0,1). As a result, charge sharing takes place between capacitor C(0) and left bitline BL(1). Meanwhile, the voltage on right bitline BL(1)* stays at the pre-charge voltage VBL. As can be seen from Fig. 3A, a small potential difference between left bitline BL(1) and right bitline BL(1)* will develop. The sign of this potential difference (i.e., positive or negative) depends on the data value of memory cell MS(0,1). Since transistors T0 and T1 remain conductive, a small potential difference will also develop between input/output node 321 and input/output node 323.

[0044] $\tau 1$: The DRAM controller 101 activates enables the sense amplifier circuit 210. Specifically, the voltage on sensing activation line SAP transitions to the second supply voltage VDD, while the voltage on sensing activation line SAN transitions to the first supply voltage VSS. This triggers operation of the sense amplifier circuit 210, by virtue of which a positive feedback mechanism is carried out by transistors T5, T6, T7 and T8. This results in amplification of the potential difference between input/output nodes 321 and 323, with the voltage at input/output node 321 rising and the voltage at input/output node 323 falling. Since transistors T0 and T1 remain conductive, the potential difference between left bitline BL(1) and right bitline BL(1)* increases as well, although with a slight lag due to the line capacitance.

[0045] After a certain amount of time, left bitline BL(1) and right bitline BL(1)* are fully developed, i.e., the voltage on left bitline BL(1) and right bitline BL(1)* has converged, in this case to VDD and VSS, respectively. This results in the second supply voltage VDD on left bitline BL(1) being

applied across capacitor C(0) via transistor AT(0) (which is conducting), thereby effecting restoration of charge to memory cell MS(0,1), i.e., memory cell MS(0,1) is "refreshed".

[0046] At this stage, reading from memory cell MS(0,1) is possible by connecting left bitline BL(1) to first data line DB and by connecting right bitline BL(1)* to second data line DB*. Specifically, this is achieved by the column address decoder 114 transitioning the voltage of the column address line Yi to the second supply voltage VDD for a certain amount of time, and then latching the value of the first and second data lines DB, DB* by returning the voltage of the column address line Yi back to the first supply voltage VSS.

[0047] $\tau 2$: The row address decoder 113 de-activates wordline WL(0) (i.e., the voltage on wordline WL(0) transitions from the high positive voltage VPP to the first supply voltage VSS). This turns off transistor AT(0) forming part of memory cell MS(0,1). It is now safe to adjust the voltages on left bitline BL(1) and complemenary bitline BL(1)* without fear of affecting the data content of memory cell MS(0,1).

[0048] $\tau 3$: The DRAM controller 101 de-activates sensing activation lines SAP, SAN. Specifically, the voltage on sensing activation lines SAP, SAN transitions to the bitline pre-charge voltage VBL. This quickly brings the voltage on input/output nodes 321 and 323 to VBL. Since transistors T0 and T1 remain conductive, the voltage on left bitline BL(1) and right bitline BL(1)* is similarly brought to VBL, although with a slight delay due to line capacitance. The sense amplifier SA(1) is now ready for another pre-charge operation as of $\tau 4$.

[0049] Reference will now be made to Figs. 3B and 3C, which show timing diagrams of the sense amplifier SA(1) of Fig. 2 during a "self-refresh" operation. The "self-refresh" operation can be performed while the memory device 100 is in a "self-refresh" mode of operation (a minimum mode of operation entered into when the system does not operate for a long time). The "self-refresh" operation can also be performed while the memory device 100 is in an "auto-refresh and read" mode for special applications, for example low performance and/or low power operation. A command received along a command line causes the memory device 100 to enter into the "self-refresh" mode (or the low-performance / low-power "auto-refresh and read" mode). As such, the command could be indicative of an instruction to enter the appropriate mode. The command could also quite simply be indicative of an instruction to perform a "self-refresh" operation, without regard to any specific mode of operation of the memory controller 100.

[0050] In accordance with two specific non-limiting embodiments of the present invention, there will be illustrated a method of refreshing memory cell MS(0,1) connected to left bitline BL(1) and associated with right bitline BL(1)*, that will include: connecting left bitline BL(1) to input/output node 321 of sense amplifier circuit 210 and connecting right bitline BL(1)* to input/output node 323 of sense amplifier circuit 210; triggering charge sharing between memory cell MS(0,1) and left bitline BL(1); disconnecting left bitline BL(1) from input/output node 321 and disconnecting right bitline BL(1)* from input/output node 323; activating sense amplifier circuit 210 to initiate a signal amplification process at input/output nodes 321 and 323; and re-connecting direct bitline B1* to input/output node 321 while complementary bitline B1* remains disconnected from input/output node 323.

[0051] Accordingly, specific reference is now made to Fig. 3B, which is a timing diagram showing operation of the sense amplifier SA(1) of Fig. 2 during a refresh operation, following the aforementioned bitline pre-charge operation, and in accordance with a specific non-limiting embodiment of the present invention. The description begins under the assumption that the voltage on first bitline

isolation line BIS0 and the voltage on second bitline isolation line BIS0* is at the high positive voltage VPP, thus initially placing transistors T0 and T1 in a conductive state.

[0052] τ0: The row address decoder 113 activates wordline WL(0) (i.e., the voltage on wordline WL(0) transitions from the first supply voltage VSS to the high positive voltage VPP). This turns on transistor AT(0) forming part of memory cell MS(0,1). As a result, charge sharing takes place between capacitor C(0) and left bitline BL(1). Meanwhile, the voltage on right bitline BL(1)* stays at the bitline pre-charge voltage VBL. As can be seen from Fig. 3B, a small potential difference between left bitline BL(1) and right bitline BL(1)* will develop. The sign of this potential difference (i.e., positive or negative) depends on the data value of memory cell MS(0,1). Since transistors T0 and T1 are in a conductive state, a small potential difference will also develop between input/output node 321 and input/output node 323.

[0053] τ1: The isolator 230 is caused to isolate left bitline BL(1) from input/output node 321 and to isolate right bitline BL(1)* from input/output node 323. This is achieved through control of the isolator 230 by the DRAM controller 101. Specifically, the voltage on first bitline isolation line BIS0 and the voltage on second bitline isolation line BIS0* are transitioned to the first supply voltage VSS, thus effectively turning off transistors T0 and T1. Transistors T0 and T1 may, but are not required to, be turned off simultaneously.

[0054] τ2: The DRAM controller 101 enables the sense amplifier circuit 210. Specifically, the voltage on sensing activation line SAP transitions to the second supply voltage VDD, while the voltage on sensing activation line SAN transitions to the first

supply voltage VSS. The voltage on sensing activation line SAP and the voltage on sensing activation line SAN may, but need not, be transitioned simultaneously. This triggers operation of the sense amplifier circuit 210, by virtue of which a positive feedback mechanism is carried out by transistors T5, T6, T7 and T8. As a result, there will be amplification of the potential difference between input/output nodes 321 and 323, with the voltage at input/output node 321 rising and the voltage at input/output node 323 falling. However, since transistors T0 and T1 have been turned off, the original (small) potential difference between left bitline BL(1) and right bitline BL(1)* does not change. After a certain amount of time, a considerable potential difference will develop between input/output nodes 321 and 323, whereas the potential difference between left bitline BL(1) and right bitline BL(1)* will still be at its original (small) value.

[0055] $\tau 3$: The isolator 230 is caused to re-connect left bitline BL(1) to input/output node 321, while right bitline BL(1)* remains isolated from input/output node 323. This is achieved through control of the isolator 230 by the DRAM controller 101. Specifically, the voltage on first bitline isolation line BIS0 is transitioned to the high positive voltage VPP, effectively turning on transistor T0. Meanwhile, the voltage on second bitline isolation line BIS0* remains at the first supply voltage VSS, thus keeping transistor T1 turned off. This leads to the following behavior:

[0056] - In the case of left bitline BL(1) and input/output node 321: the voltage at input/output node 321 will drop somewhat during a transient phase while the voltage on left bitline BL(1) will rise somewhat during this period. Eventually, due to continued action of positive

feedback in the sense amplifier circuit 210, the voltage at input/output node 321 will begin to increase again and tend towards the second supply voltage VDD, while the voltage on left bitline BL(1) will rise continually (although somewhat delayed relative to the voltage at input/output node 321) until it too converges to the second supply voltage VDD. This results in the second supply voltage VDD on left bitline BL(1) being applied across capacitor C(0) via transistor AT(0) (which is conducting), thereby effecting restoration of charge to memory cell MS(0,1), i.e., memory cell MS(0,1) is "refreshed".

[0057] - In the case of right bitline BL(1)* and input/output node 323: the voltage at input/output node 323 will, if it had not already fallen to the first supply voltage VSS, decrease until this voltage is reached. Thereafter, the voltage at input/output node 323 will stay at this level, namely the first supply voltage VSS. Meanwhile, the voltage on right bitline BL(1)* will remain what it was prior to isolation of right bitline BL(1)* from input/output node 323, namely the bitline pre-charge voltage VBL.

[0058] It will thus be observed that the potential difference $\Delta V1$ between input/output node 321 and input/output node 323 exceeds the potential difference $\Delta V2$ between left bitline BL(1) and right bitline BL(1)*. The fact that $\Delta V2$ is less than $\Delta V1$ implies that less power is consumed by the sense amplifier SA(1). If power consumption is squarely proportional to voltage, then in this example, the power consumption will be around a quarter (1/4) of that which

would be consumed if bitlines BL(1) and BL(1)* were allowed to fully develop.

[0059] $\tau 4$: The row address decoder 113 de-activates wordline WL(0) (i.e., the voltage on wordline WL(0) transitions from the high positive voltage VPP to the first supply voltage VSS). This turns off transistor AT(0) forming part of memory cell MS(0,1). It is now safe to adjust the voltages on left bitline BL(1) and complemenary bitline BL(1)* without fear of affecting the data content of memory cell MS(0,1).

[0060] $\tau 5$: The DRAM controller 101 de-activates sensing activation lines SAP, SAN. Specifically, the voltage on sensing activation lines SAP, SAN transitions to the bitline pre-charge voltage VBL. This quickly brings the voltage on input/output nodes 321 and 323 to VBL. Since transistor T0 remains conductive, the voltage on left bitline BL(1) is similarly brought to VBL, although with a slight delay due to line capacitance. Meanwhile, the voltage on right bitline BL(1)* does not change from its previous value, which is conveniently still VBL. Therefore, when the isolator 230 is caused to re-connect right bitline BL(1)* to input/output node 323 (which occurs at $\tau 6$), there will be no change to the voltage on complementary biltine BL(1)*. The sense amplifier 210 is now ready for another pre-charge operation.

[0061] Specific reference is now made to Fig. 3C, which is a timing diagram showing operation of the sense amplifier SA(1) of Fig. 2 during a refresh operation, following the aforementioned bitline pre-charge operation, and in accordance with another specific non-limiting embodiment of the present invention. The description begins under the assumption that the voltage on first bitline isolation line BIS0 and the voltage on second bitline isolation line BIS0* is at the high positive voltage VPP, thus initially placing transistors T0 and T1 in a conductive state.

[0062] $\tau 0$: The row address decoder 113 activates wordline WL(0) (i.e., the voltage on wordline WL(0) transitions from the first supply voltage VSS to the high positive voltage VPP). This turns on transistor AT(0) forming part of memory cell MS(0,1). As a result, charge sharing takes place between capacitor C(0) and left bitline BL(1). Meanwhile, the voltage on right bitline BL(1)* stays at the bitline pre-charge voltage VBL. As can be seen from Fig. 3C, a small potential difference between left bitline BL(1) and right bitline BL(1)* will develop. The sign of this potential difference (i.e., positive or negative) depends on the data value of memory cell MS(0,1). Since transistors T0 and T1 are in a conductive state, a small potential difference will also develop between input/output node 321 and input/output node 323.

[0063] $\tau 1$: The DRAM controller 101 activates sensing activation lines SAP, SAN. Specifically, the voltage on sensing activation line SAP transitions to the second supply voltage VDD, while the voltage on sensing activation line SAN transitions to the first supply voltage VSS. The voltage on sensing activation line SAP and the voltage on sensing activation line SAN may, but need not, be transitioned simultaneously. This triggers operation of the sense amplifier circuit 210, by virtue of which a positive feedback mechanism is carried out by transistors T5, T6, T7 and T8. The result will be amplification of the potential difference between input/output nodes 321 and 323, with the voltage at input/output node 321 rising and the voltage at input/output node 323 falling. Since transistors T0 and T1 remain conductive, the potential difference between left bitline BL(1) and right bitline BL(1)*

increases as well, although with a slight lag due to the line capacitance.

[0064] $\tau 2$: The isolator 230 is caused to isolate left bitline BL(1) from input/output node 321 and to isolate right bitline BL(1)* from input/output node 323. This is achieved through control of the isolator 230 by the DRAM controller 101. Specifically, the voltage on first bitline isolation line BIS0 and the voltage on second bitline isolation line BIS0* are transitioned to the first supply voltage VSS, thus effectively turning off transistors T0 and T1. Transistors T0 and T1 may, but are not required to, be turned off simultaneously.

[0065] It is noted that isolation of left bitline BL(1) from input/output node 321 and isolation of right bitline BL(1)* from input/output node 323 occurs before the potential difference between left bitline BL(1) and right bitline BL(1)* has had a chance to fully develop (i.e., converge to its final values). However, isolation does not affect the behavior of the sense amplifier circuit 210 with respect to input/output nodes 321 and 323, and therefore the potential difference between input/output nodes 321 and 323 continues to grow, possibly even until it has converged to its final value (whereby, in this case, the voltage at input/output node 321 will be the second supply voltage VDD and the voltage at input/output node 323 will be the first supply voltage VSS).

[0066] $\tau 3$: The isolator 230 is caused to re-connect left bitline BL(1) to input/output node 321, while right bitline BL(1)* remains isolated from input/output node 323. This is achieved through control of the isolator 230 by the DRAM controller 101. Specifically, the voltage on first bitline isolation line BIS0 is transitioned to the high positive voltage VPP, effectively turning on transistor T0. Meanwhile, the voltage

on second bitline isolation line BIS0* remains at the first supply voltage VSS, thus keeping transistor T1 turned off. This leads to the following behavior:

[0067] - In the case of left bitline BL(1) and input/output node 321: the voltage at input/output node 321 will drop somewhat during a transient phase while the voltage on left bitline BL(1) will rise somewhat during this period. Eventually, due to continued action of positive feedback in the sense amplifier circuit 210, the voltage at input/output node 321 will begin to increase again and tend towards the second supply voltage VDD, while the voltage on left bitline BL(1) will rise continually (although somewhat delayed relative to the voltage at input/output node 321) until it too converges to the second supply voltage VDD. This results in the second supply voltage VDD on left bitline BL(1) being applied across capacitor C(0) via transistor AT(0) (which is conducting), thereby effecting restoration of charge to memory cell MS(0,1), i.e., memory cell MS(0,1) is "refreshed".

[0068] - In the case of right bitline BL(1)* and input/output node 323: the voltage at input/output node 323 will, if it had not already fallen to the first supply voltage VSS, decrease until this voltage is reached. Thereafter, the voltage at input/output node 323 will stay at this level, namely the first supply voltage VSS. Meanwhile, the voltage on right bitline BL(1)* will remain what it was prior to isolation of right bitline BL(1)* from input/output node 323, namely an intermediate voltage between the bitline pre-charge voltage VBL and the first supply voltage VSS. In this

illustrated example embodiment, the voltage on right bitline BL(1)* remains at a level that is about 50% of the way between VBL and VSS. (If VBL is midway between VSS and VDD, then clearly this represents a level that is 75% of the way between VDD and VSS.) Of course, other intermediate values are possible as the voltage reached by right bitline BL(1)* when transistor T1 is turned off.

[0069] It will thus be observed that the potential difference $\Delta V1$ between input/output node 321 and input/output node 323 exceeds the potential difference $\Delta V3$ between left bitline BL(1) and right bitline BL(1)*. In this case, $\Delta V3$ is not as small as $\Delta V2$ that had been previously obtained (in Fig. 3B) by isolating bitlines BL(1), BL(1)* from input/output nodes 321 and 323, respectively, prior to activating the sense amplifier circuit 210. Nevertheless, the fact that $\Delta V3$ is still less than $\Delta V1$ implies that less power is consumed by the sense amplifier SA(1). If power consumption is squarely proportional to voltage, then in this example, the power consumption will be around nine sixteenths (9/16) of that which would be consumed if bitlines BL(1) and BL(1)* were allowed to fully develop.

[0070] $\tau 4$: The row address decoder 113 de-activates wordline WL(0) (i.e., the voltage on wordline WL(0) transitions from the high positive voltage VPP to the first supply voltage VSS). This turns off transistor AT(0) forming part of memory cell MS(0,1). It is now safe to adjust the voltages on left bitline BL(1) and complemenary bitline BL(1)* without fear of affecting the data content of memory cell MS(0,1).

[0071] $\tau 5$: The DRAM controller 101 de-activates sensing activation lines SAP, SAN. Specifically, the voltage on sensing

activation lines SAP, SAN transitions to the bitline pre-charge voltage VBL. This quickly brings the voltage on input/output nodes 321 and 323 to VBL. Since transistor T0 remains conductive, the voltage on left bitline BL(1) is similarly brought to VBL, although with a slight delay due to line capacitance. Meanwhile, the voltage on right bitline BL(1)* does not change from its previous value, which is between VBL and VSS. Therefore, when the isolator 230 is caused to re-connect right bitline BL(1)* to input/output node 323 (which occurs at $\tau 6$), the voltage on complementary biltine BL(1)* will rise and reach VBL. The sense amplifier 210 is now ready for another pre-charge operation.

[0072] In an alternative embodiment, transistor T0 in the isolator 230 can remain conductive throughout the entire refresh operation. That is, rather than switch off transistor T0 at time $\tau 1$ (in Fig. 3B) or $\tau 2$ (in Fig. 3C) and switch it back on at time $\tau 3$, transistor T0 can remain turned on all along. This will provide comparable power savings benefits and performance, provided that any capacitive transients during switching off of transistor T1 do not significantly affect the performance of sense amplifier circuit 210. Specifically, in the case where transistor T0 is not switched off during the refresh operation, the values of $\Delta V1$ as well as $\Delta V2$ (Fig. 3B) and $\Delta V3$ (Fig. 3C) will be the same as those in the case where transistor T0 was switched off, because these values are calculated when left bitline BL1 is in fact connected to input/output terminal 321.

[0073] Moreover, it is envisaged that transistor T0 may even be eliminated from the isolator 230. This is the case in Fig. 5, where sense amplifier 500 is seen to contain the same sense amplifier circuit 210 and bitline equalizer 220 as previously described with reference to sense amplifier SA(1). However, in this embodiment, an isolator 530 includes only transistor T1. A permanent electrical connection exists between left bitline BL(1) and input/output terminal 321. Consequently, the first bitline isolation line BIS0 can be dispensed with and only control of the second bitline isolation line BIS0* is required. The manner of

controlling the signals is the same as described above with reference to Figs. 3B and 3C, except that there is no first bitline isolation line BIS0 to manipulate. It will thus be appreciated that in such an embodiment, right bitline BL(1)* will be electrically disconnected from input/output terminal 323 while left bitline BL(1) remains electrically connected to input/output terminal 321.

[0074] In another embodiment, shown in Fig. 4, the memory array 102 is subdivided into a plurality of sub-arrays of rows and columns such that a particular memory cell in a given one of the memory sub-arrays is addressed by specifying its row and column within the given memory sub-array. By way of non-limiting example, reference numeral 410 shows a first memory sub-array, reference numeral 420 shows a second memory sub-array and reference numeral 430 shows a third memory sub-array. Of course, the total number of memory sub-arrays may be different (i.e., lesser or greater).

[0075] In the present non-limiting embodiment, memory sub-array 410, is addressed by a set of wordlines $WL_{410}(0)$, $WL_{410}(1)$, ... $WL_{410}(N-1)$, memory sub-array 420 is addressed by a set of wordlines $WL_{420}(0)$, $WL_{420}(1)$, ... $WL_{420}(N-1)$, and memory sub-array 430 is addressed by a set of wordlines $WL_{430}(0)$, $WL_{430}(1)$, ... $WL_{430}(N-1)$. In the present non-limiting embodiment, each of the memory sub-arrays 410, 420, 430 is assumed to have N rows and M columns of memory cells, but this need not be the case in all embodiments. For example, a given memory sub-array may have a greater or lesser number of rows, correspondingly requiring a greater or lesser number of wordlines.

[0076] In the specific embodiment of Fig. 4, the M sense amplifiers associated with a given memory sub-array can themselves be grouped into two (2) arrays of sense amplifiers. Considering memory sub-array 420 in particular, sense amplifiers SA(0), SA(2), ..., SA(M-2) form a lower sense amplifier array 450, while sense amplifiers SA(1), SA(3), ..., SA(M-1) form an upper sense amplifier array 440. Advantageously, the sense amplifiers in the upper sense amplifier array 450 can be re-used to connect to bitlines and memory cells in memory sub-array 410, while the sense amplifiers in the lower sense amplifier array 440 can be re-used to connect to bitlines and memory cells in memory sub-

array 430. Therefore, even though M sense amplifiers are needed for a given memory sub-array, each of these M sense amplifiers is shared with a neighboring (upper or lower) memory sub-array (where one exists), and thus the total number of sense amplifiers can be kept to (M+1)/2 times the number of memory sub-arrays. Meanwhile, the capacitive load handled by a given sense amplifier does not increase, as it handles the left and right bitlines for only one of its neighboring memory sub-arrays at any given time, while remaining isolated from the other one of its neighboring memory sub-arrays.

[0077] As can be appreciated, in the embodiments above, where a pair of bitlines is associated with a given sense amplifier responsible for refreshing a given memory cell, the periods of time during which each of the bitlines is connected to (or isolated from) the corresponding input/output node of the sense amplifier are different. That is to say, during the time when the sense amplifier is carrying out its sensing operation (and the potential difference at the input/output nodes begins to increase), the one bitline in the pair that is connected to the memory cell being refreshed will be allowed to track the voltage of the corresponding input/output node of the sense amplifier, allowing the memory cell to be restored with the correct charge. However, the other bitline will be isolated from the corresponding input/output node of the sense amplifier during at least part of the sensing operation, which reduces the current flowing on that other bitline during the refresh operation, thereby consuming less power than if it had been allowed to continuously track the corresponding input/output node of the sense amplifier. Those skilled the art will appreciate that in this way, it may be possible to achieve reduced power consumption irrespective of the size of the memory array, the operating temperature or the refresh period.

[0078] In the embodiments described above, the manner in which device elements and circuits are shown as connected to each other is done for the sake of simplicity. In practical applications of the present invention, elements, circuits, etc. may be either connected directly to one another, or they may be connected indirectly to one another through other elements, circuits, etc., necessary for operation of devices and apparatus. Thus, in an actual configuration, the circuit

elements and circuits described herein may be directly or indirectly coupled with or connected to one another.

[0079] It should also be appreciated that in some embodiments, all or part of the DRAM device can be manufactured based on a low-level hardware description obtained using a logic synthesis tool that is run on a computing device. The logic synthesis tool is configured to read source code containing a functional description of the DRAM device (e.g., in a language such as HDL, VHDL, Verilog) and to output a definition of the physical implementation of a circuit suitable for implementing corresponding functionality.

[0080] Additionally, although the above description has been provided in the context of a DRAM memory device, those skilled in the art may find that aspects of the invention apply to other memory types.

[0081] The above-described embodiments of the present invention are intended to be examples only. Alterations, modifications and variations may be effected to the particular embodiments by those of skill in the art without departing from the scope of the invention, which is defined solely by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A semiconductor memory device, including:
   - a memory cell connected to a first bitline and associated with a second bitline;
   - a sense amplifier, including a first input/output node and a second input/output node; and
   - an isolator connected to the bitlines and to the input/output nodes, the isolator being controllable during a refresh operation of the memory cell to cause the first bitline to be electrically connected to or disconnected from the first input/output node and, independently, to cause the second bitline to be electrically connected to or disconnected from the second input/output node.

2. A semiconductor memory device, including:
   - a memory cell connected to a first bitline and associated with a second bitline;
   - a sense amplifier, including a first input/output node and a second input/output node; and
   - an isolator connected to the bitlines and to the input/output nodes, the isolator being configured to carry out bitline isolation during a refresh operation of the memory cell, wherein the bitline isolation includes:
     - electrically disconnecting the first bitline from the first input/output node and electrically disconnecting the second bitline from the second input/output node, followed by:
     - electrically re-connecting the first bitline to the first input/output node while the second bitline remains electrically disconnected from the second input/output node.

3. The semiconductor memory device defined in claim 2, wherein said electrically disconnecting the first bitline from the first input/output node and

said electrically disconnecting the second bitline from the second input/output node occur substantially simultaneously.

4. The semiconductor memory device defined in claim 2, wherein said isolator is further configured to electrically re-connect the second bitline to the second input/output node after the refresh operation is complete.

5. The semiconductor memory device defined in claim 2, wherein the sense amplifier is responsive to receipt of at least one sensing activation signal from a controller to initiate a signal amplification process at the first and second input/output nodes.

6. The semiconductor memory device defined in claim 5, further comprising said controller.

7. The semiconductor memory device defined in claim 6, wherein said controller is operative to cause the isolator to carry out said bitline isolation in response to detection of a command to perform a refresh operation.

8. The semiconductor memory device defined in claim 5, wherein said electrically disconnecting the first bitline from the first input/output node and electrically disconnecting the second bitline from the second input/output node is carried out before said signal amplification process has been initiated.

9. The semiconductor memory device defined in claim 5, wherein the signal amplification process causes the first input/output node to tend towards a first final electric potential and the second input/output node to tend towards a second final electric potential different from the first final electric potential, wherein said electrically disconnecting the first bitline from the first input/output node and electrically disconnecting the second bitline from the second input/output node is carried out after said amplification process has

been initiated but before the second input/output node has reached the second final electric potential.

10. The semiconductor memory device defined in claim 5, wherein the signal amplification process causes the first input/output node to tend towards a first final electric potential and the second input/output node to tend towards a second final electric potential different from the first final electric potential, wherein said electrically disconnecting the first bitline from the first input/output node and electrically disconnecting the second bitline from the second input/output node is carried out after said amplification process has been initiated but before the second input/output node has reached an electrical potential that is three-quarters of the way between the first final electric potential and the second final electric potential.

11. The semiconductor memory device defined in claim 10, further including a pre-charge circuit configured to pre-charge the first and second input/output nodes to a bitline pre-charge voltage that is between the first final electric potential and the second final electric potential.

12. The semiconductor memory device defined in claim 11, wherein the bitline pre-charge voltage is midway between the first final electric potential and the second final electric potential.

13. The semiconductor memory device defined in claim 11, wherein the controller is configured to pre-charge the first and second input/output nodes before sending causing the sense amplifier to initiate the signal amplification process at the first and second input/output nodes.

14. The semiconductor memory device defined in claim 11, wherein the memory cell includes a transistor connected between the first bitline and a capacitor, the transistor having a gate connected to a wordline activatable by the

controller, the controller being configured to activate the wordline after pre-charging the first and second input/output nodes and before causing the sense amplifier to initiate the signal amplification process at the first and second input/output nodes, wherein activation of the wordline causes charge sharing between the capacitor and the first bitline.

15. The semiconductor memory device defined in claim 14, wherein at the time when the wordline is activated, the first bitline is electrically connected to the first input/output node and the second bitline is electrically connected to the second input/output node.

16. The semiconductor memory device defined in claim 15, wherein the controller is configured to pre-charge the first and second input/output nodes while the first bitline is electrically connected to the first input/output node and the second bitline is electrically connected to the second input/output node.

17. The semiconductor memory device defined in claim 11, wherein the at least one sensing activation signal is delivered from the controller to the sense amplifier over a first sensing activation line and a second sensing activation line, and wherein the controller is configured to set the first sensing activation line to the first final electric potential and to set the second sensing activation line to the second final electric potential in order to initiate the signal amplification process at the first and second input/output nodes.

18. The semiconductor memory device defined in claim 17, wherein the sense amplifier includes a first transistor, a second transistor, a third transistor and a fourth transistor, wherein each transistor has a gate, a source and a drain, wherein the source of the first transistor is connected to the drain of the second transistor, to the gates of the third and fourth transistors and to the first input/output node, wherein the source of the third transistor is connected to the drain of the fourth transistor, to the gates of the first and second

transistors and to the second input/output node, wherein the drain of the first transistor is connected to the drain of the third transistor and the first sensing activation line and wherein the source of the second transistor is connected to the source of the fourth transistor and the second sensing activation line.

19. The semiconductor memory device defined in claim 18, wherein said electrically disconnecting the first bitline from the first input/output node and electrically disconnecting the second bitline from the second input/output node is carried out after said amplification process has been initiated but before the second input/output node has reached an electrical potential that is midway between the bitline precharge voltage and the second final electric potential.

20. The semiconductor memory device defined in claim 2, wherein the isolator includes:
    - a first isolation element responsive to a first control signal to cause the first bitline to be electrically connected to or disconnected from the first input/output node; and
    - a second isolation element responsive to a second control signal independent of the first control signal to cause the second bitline to be electrically connected to or disconnected from the second input/output node.

21. The semiconductor memory device defined in claim 20, wherein the first isolation element includes a first transistor and wherein the second isolation element includes a second transistor.

22. The semiconductor memory device defined in claim 21, wherein the first transistor includes a gate that receives the first control signal and wherein the second transistor includes a gate that receives the second control signal.

23. A semiconductor memory device, including:
    - a memory cell connected to a first bitline and associated with a second bitline;
    - a sense amplifier, including a first input/output node and a second input/output node; and
    - an isolator connected to the bitlines and to the input/output nodes, the isolator being configured to carry out bitline isolation during a refresh operation of the memory cell, wherein the bitline isolation includes electrically disconnecting the second bitline from the second input/output node while the first bitline remains electrically connected to the first input/output node.

24. The semiconductor memory device defined in claim 23, the isolator being further configured to electrically re-connect the second bitline to the second input/output node after the refresh operation is complete.

25. The semiconductor memory device defined in claim 23, wherein the sense amplifier is responsive to receipt of at least one sensing activation signal from a controller to initiate a signal amplification process at the first and second input/output nodes.

26. The semiconductor memory device defined in claim 25, further comprising said controller.

27. The semiconductor memory device defined in claim 26, wherein said controller is operative to cause the isolator to carry out said bitline isolation in response to detection of a command to perform a refresh operation.

28. The semiconductor memory device defined in claim 25, wherein said electrically disconnecting the second bitline from the second input/output node is carried out before said signal amplification process has been initiated.

29. The semiconductor memory device defined in claim 25, wherein the signal amplification process causes the first input/output node to tend towards a first final electric potential and the second input/output node to tend towards a second final electric potential different from the first final electric potential, wherein said electrically disconnecting the second bitline from the second input/output node is carried out after said amplification process has been initiated but before the second input/output node has reached the second final electric potential.

30. The semiconductor memory device defined in claim 25, wherein the signal amplification process causes the first input/output node to tend towards a first final electric potential and the second input/output node to tend towards a second final electric potential different from the first final electric potential, wherein said electrically disconnecting the second bitline from the second input/output node is carried out after said amplification process has been initiated but before the second input/output node has reached an electrical potential that is three-quarters of the way between the first final electric potential and the second final electric potential.

31. The semiconductor memory device defined in claim 30, further including a pre-charge circuit configured to pre-charge the first and second input/output nodes to a bitline pre-charge voltage that is between the first final electric potential and the second final electric potential.

32. The semiconductor memory device defined in claim 31, wherein the bitline pre-charge voltage is midway between the first final electric potential and the second final electric potential.

33. The semiconductor memory device defined in claim 31, wherein the controller is configured to pre-charge the first and second input/output nodes before

sending causing the sense amplifier to initiate the signal amplification process at the first and second input/output nodes.

34. The semiconductor memory device defined in claim 31, wherein the memory cell includes a transistor connected between the first bitline and a capacitor, the transistor having a gate connected to a wordline activatable by the controller, the controller being configured to activate the wordline after pre-charging the first and second input/output nodes and before causing the sense amplifier to initiate the signal amplification process at the first and second input/output nodes, wherein activation of the wordline causes charge sharing between the capacitor and the first bitline.

35. The semiconductor memory device defined in claim 34, wherein at the time when the wordline is activated, the first bitline is electrically connected to the first input/output node and the second bitline is electrically connected to the second input/output node.

36. The semiconductor memory device defined in claim 35, wherein the controller is configured to pre-charge the first and second input/output nodes while the first bitline is electrically connected to the first input/output node and the second bitline is electrically connected to the second input/output node.

37. The semiconductor memory device defined in claim 31, wherein the at least one sensing activation signal is delivered from the controller to the sense amplifier over a first sensing activation line and a second sensing activation line, and wherein the controller is configured to set the first sensing activation line to the first final electric potential and to set the second sensing activation line to the second final electric potential in order to initiate the signal amplification process at the first and second input/output nodes.

38. The semiconductor memory device defined in claim 37, wherein the sense amplifier includes a first transistor, a second transistor, a third transistor and a fourth transistor, wherein each transistor has a gate, a source and a drain, wherein the source of the first transistor is connected to the drain of the second transistor, to the gates of the third and fourth transistors and to the first input/output node, wherein the source of the third transistor is connected to the drain of the fourth transistor, to the gates of the first and second transistors and to the second input/output node, wherein the drain of the first transistor is connected to the drain of the third transistor and the first sensing activation line and wherein the source of the second transistor is connected to the source of the fourth transistor and the second sensing activation line.

39. The semiconductor memory device defined in claim 38, wherein said electrically disconnecting the second bitline from the second input/output node is carried out after said amplification process has been initiated but before the second input/output node has reached an electrical potential that is midway between the bitline precharge voltage and the second final electric potential.

40. The semiconductor memory device defined in claim 23, wherein the isolator includes:
    - an isolation element responsive to a control signal to cause the second bitline to be electrically connected to or disconnected from the second input/output node.

41. The semiconductor memory device defined in claim 40, wherein the isolation element includes a transistor.

42. The semiconductor memory device defined in claim 41, wherein the transistor includes a gate that receives the control signal.

43. The semiconductor memory device defined in claim 40, wherein the first bitline is permanently electrically connected to the first input/output node.

44. A method of refreshing a memory cell connected to a first bitline and associated with a second bitline, the method including:
- connecting the first bitline to a first input/output node of a sense amplifier and connecting the second bitline to a second input/output node of the sense amplifier;
- triggering charge sharing between the memory cell and the first bitline;
- disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the second input/output node;
- activating the sense amplifier to initiate a signal amplification process at the first and second input/output nodes; and
- re-connecting the first bitline to the first input/output node while the second bitline remains disconnected from the second input/output node.

45. The method defined in claim 44, wherein said disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the second input/output node are performed before said activating the sense amplifier.

46. The method defined in claim 44, wherein said disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the second input/output node are performed after said activating the sense amplifier.

47. The method defined in claim 44, wherein said disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the second input/output node are performed substantially simultaneously.

48. The method defined in claim 44, wherein the charge sharing is triggered by activating a wordline associated with the memory cell.

49. The method defined in claim 44, wherein said triggering charge sharing includes connecting a capacitor of the memory cell to the first bitline.

50. The method defined in claim 44, wherein said triggering charge sharing causes development of a non-zero potential difference between the first and second bitlines.

51. The method defined in claim 50, further including:
- before said triggering charge sharing, connecting the first and second bitlines to one another so as to equalize the electric potential between the first and second bitlines.

52. The method defined in claim 51, wherein said activating the sense amplifier causes development of an amplified potential difference between the first and second input/output nodes.

53. The method defined in claim 52, wherein development of an amplified potential difference between the first and second input/output nodes tends towards a maximum value.

54. The method defined in claim 53, wherein said disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the second input/output node is performed before the amplified potential difference between the first and second input/output nodes has reached the maximum value.

55. The method defined in claim 53, wherein said disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the

second input/output node is performed before the amplified potential difference between the first and second input/output nodes has reached 75% of the maximum value.

56. The method defined in claim 53, wherein said disconnecting the first bitline from the first input/output node and disconnecting the second bitline from the second input/output node is performed before the amplified potential difference between the first and second input/output nodes has reached 50% of the maximum value.

57. The method defined in claim 44, wherein the connecting, triggering, disconnecting, activating and re-connecting are performed periodically for a plurality of memory cells.

58. The method defined in claim 44, further comprising receiving an indication of a command to perform a refresh operation and, responsive to said command, performing the connecting, triggering, disconnecting, activating and re-connecting.

59. A method of refreshing a memory cell connected to a first bitline and associated with a second bitline, the method including:
- connecting the first bitline to a first input/output node of a sense amplifier and connecting the second bitline to a second input/output node of the sense amplifier;
- triggering charge sharing between the memory cell and the first bitline;
- disconnecting the second bitline from the second input/output node while the first biltine remains connected to the first input/output node; and
- activating the sense amplifier to initiate a signal amplification process at the first and second input/output nodes.

60. The method defined in claim 59, wherein said disconnecting the second bitline from the second input/output node is performed before said activating the sense amplifier.

61. The method defined in claim 59, wherein said disconnecting the second bitline from the second input/output node is performed after said activating the sense amplifier.

62. The method defined in claim 59, wherein the charge sharing is triggered by activating a wordline associated with the memory cell.

63. The method defined in claim 59, wherein said triggering charge sharing includes connecting a capacitor of the memory cell to the first bitline.

64. The method defined in claim 59, wherein said triggering charge sharing causes development of a non-zero potential difference between the first and second bitlines.

65. The method defined in claim 64, further including:
- before said triggering charge sharing, connecting the first and second bitlines to one another so as to equalize the electric potential between the first and second bitlines.

66. The method defined in claim 65, wherein said activating the sense amplifier causes development of an amplified potential difference between the first and second input/output nodes.

67. The method defined in claim 66, wherein development of an amplified potential difference between the first and second input/output nodes tends towards a maximum value.

68. The method defined in claim 67, wherein said disconnecting the second bitline from the second input/output node is performed before the amplified potential difference between the first and second input/output nodes has reached the maximum value.

69. The method defined in claim 67, wherein said disconnecting the second bitline from the second input/output node is performed before the amplified potential difference between the first and second input/output nodes has reached 75% of the maximum value.

70. The method defined in claim 67, wherein said disconnecting the second bitline from the second input/output node is performed before the amplified potential difference between the first and second input/output nodes has reached 50% of the maximum value.

71. The method defined in claim 59, wherein the connecting, triggering, disconnecting and activating are performed periodically for a plurality of memory cells.

72. The method defined in claim 59, further comprising receiving an indication of a command to perform a refresh operation and, responsive to said command, performing the connecting, triggering, disconnecting and activating.

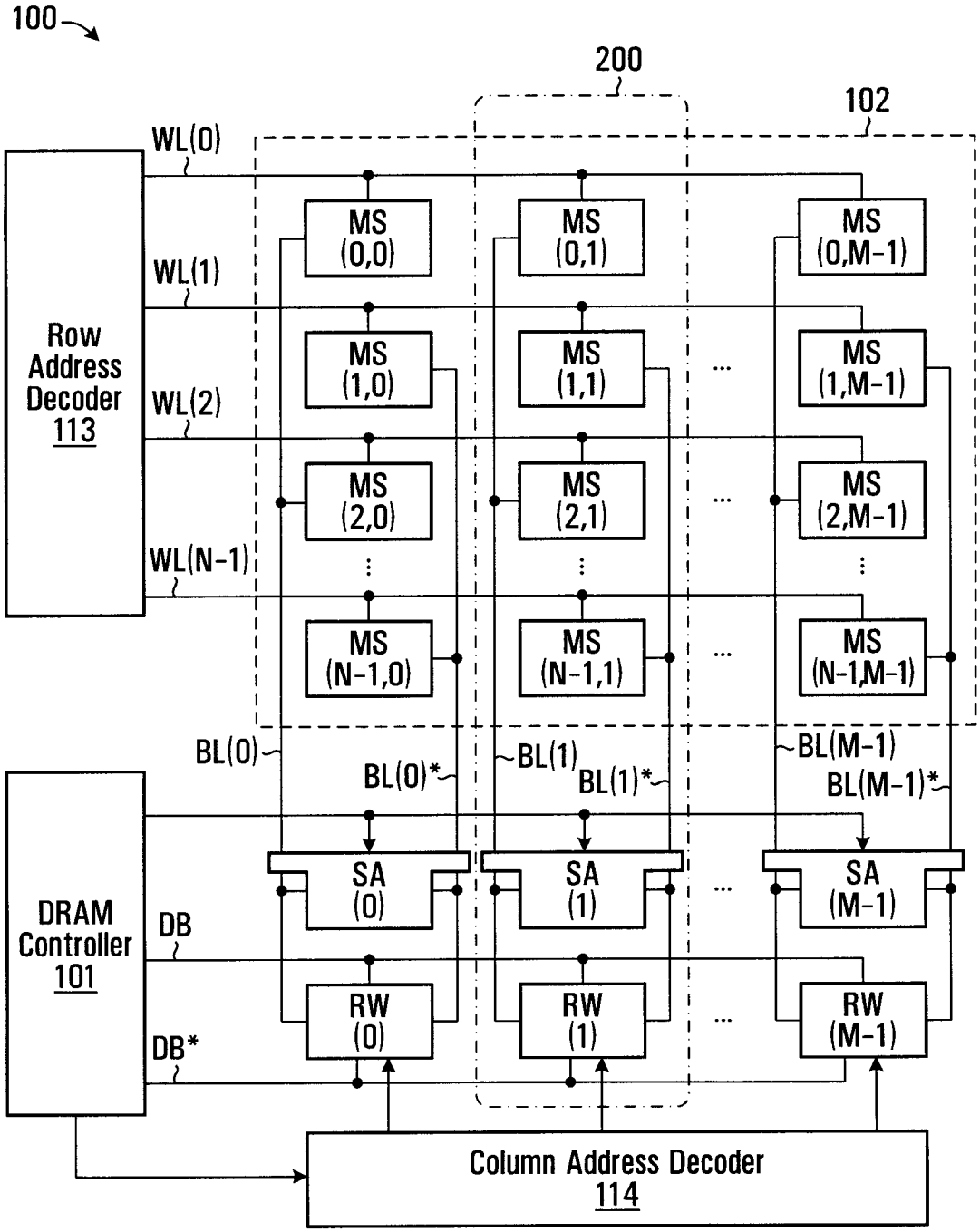

100
200
102
WL(0)
WL(1)
WL(2)
WL(N-1)
Row Address Decoder 113
MS (0,0)
MS (0,1)
MS (0,M-1)
MS (1,0)
MS (1,1)
MS (1,M-1)
MS (2,0)
MS (2,1)
MS (2,M-1)
MS (N-1,0)
MS (N-1,1)
MS (N-1,M-1)
BL(0)
BL(0)*
BL(1)
BL(1)*
BL(M-1)
BL(M-1)*
DRAM Controller 101
DB
DB*
SA (0)
SA (1)
SA (M-1)
RW (0)
RW (1)
RW (M-1)
Column Address Decoder 114

FIG. 1

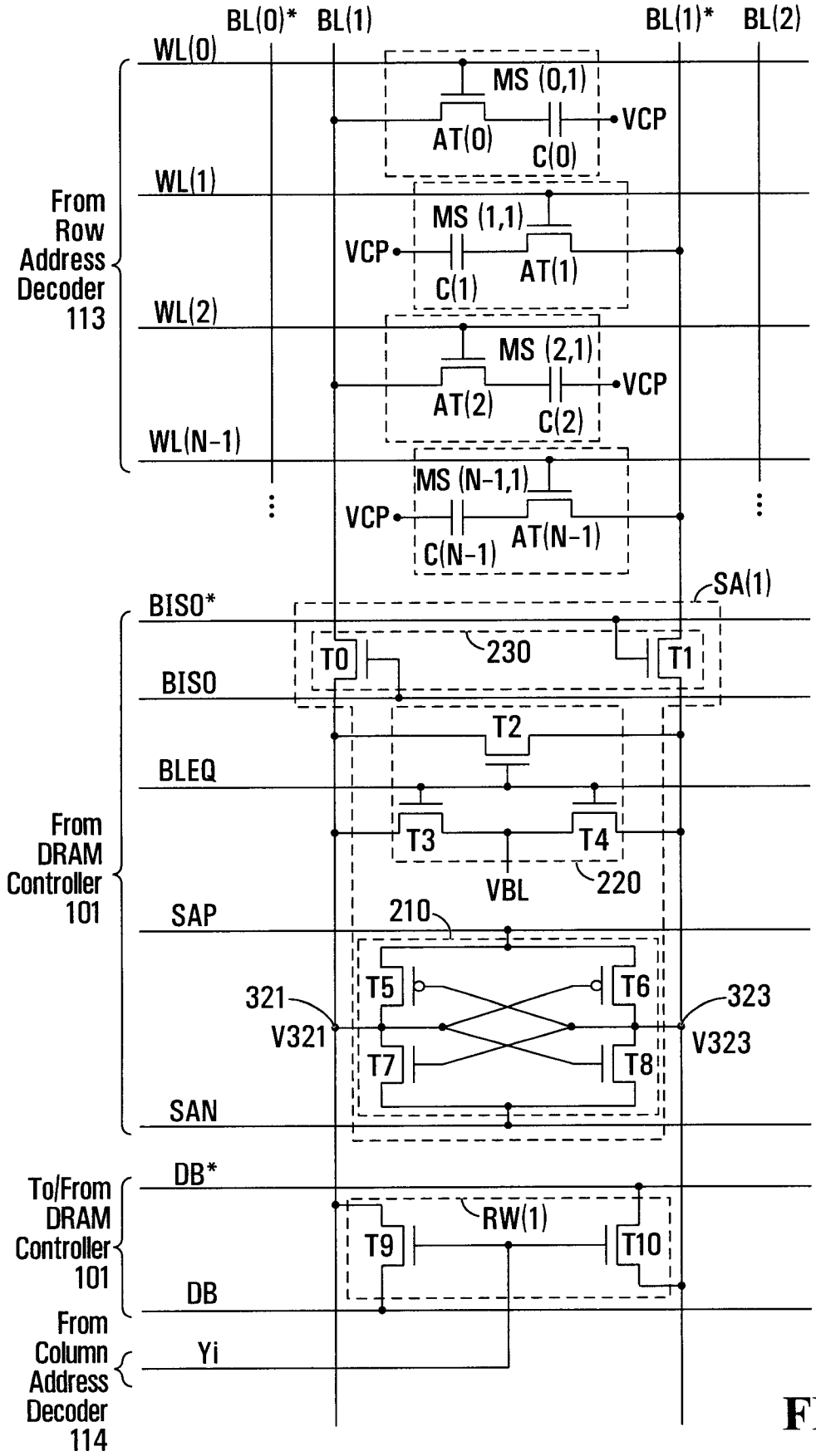

BL(0)*
BL(1)
BL(1)*
BL(2)
WL(0)
WL(1)
WL(2)
WL(N-1)
From Row Address Decoder 113
MS (0,1)
AT(0)
C(0)
VCP
MS (1,1)
C(1)
AT(1)
MS (2,1)
AT(2)
C(2)
MS (N-1,1)
C(N-1)
AT(N-1)
SA(1)
BISO*
BISO
BLEQ
SAP
SAN
From DRAM Controller 101
T0
T1
230
T2
T3
T4
VBL
220
210
T5
T6
T7
T8
321
V321
323
V323
To/From DRAM Controller 101
DB*
DB
RW(1)
T9
T10
From Column Address Decoder 114
Yi

FIG. 2

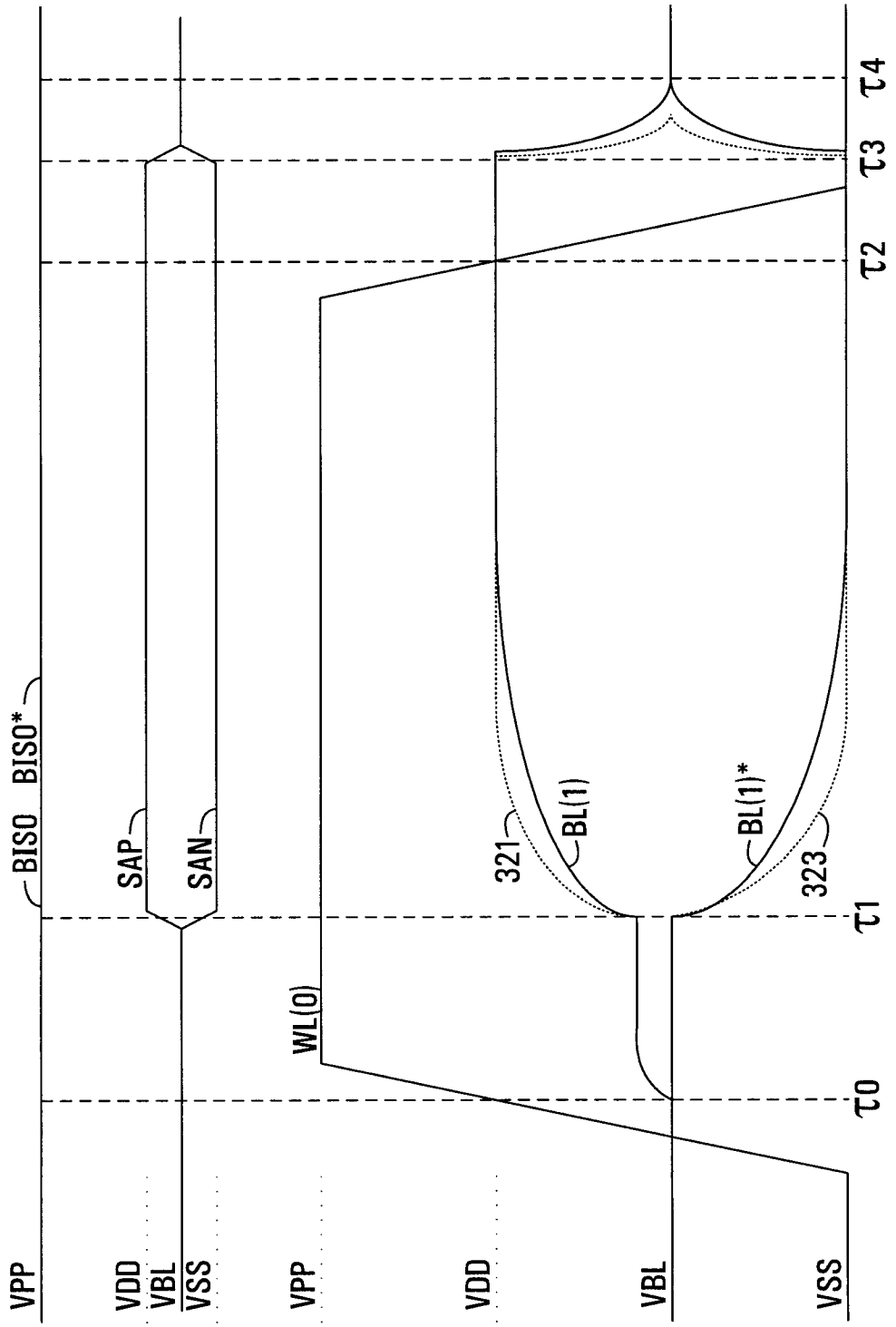

BISO
BISO*
SAP
SAN
WL(0)
321
BL(1)
BL(1)*
323
τ0
τ1
τ2
τ3
τ4
VPP
VDD
VBL
VSS
VPP
VDD
VBL
VSS

FIG. 3A

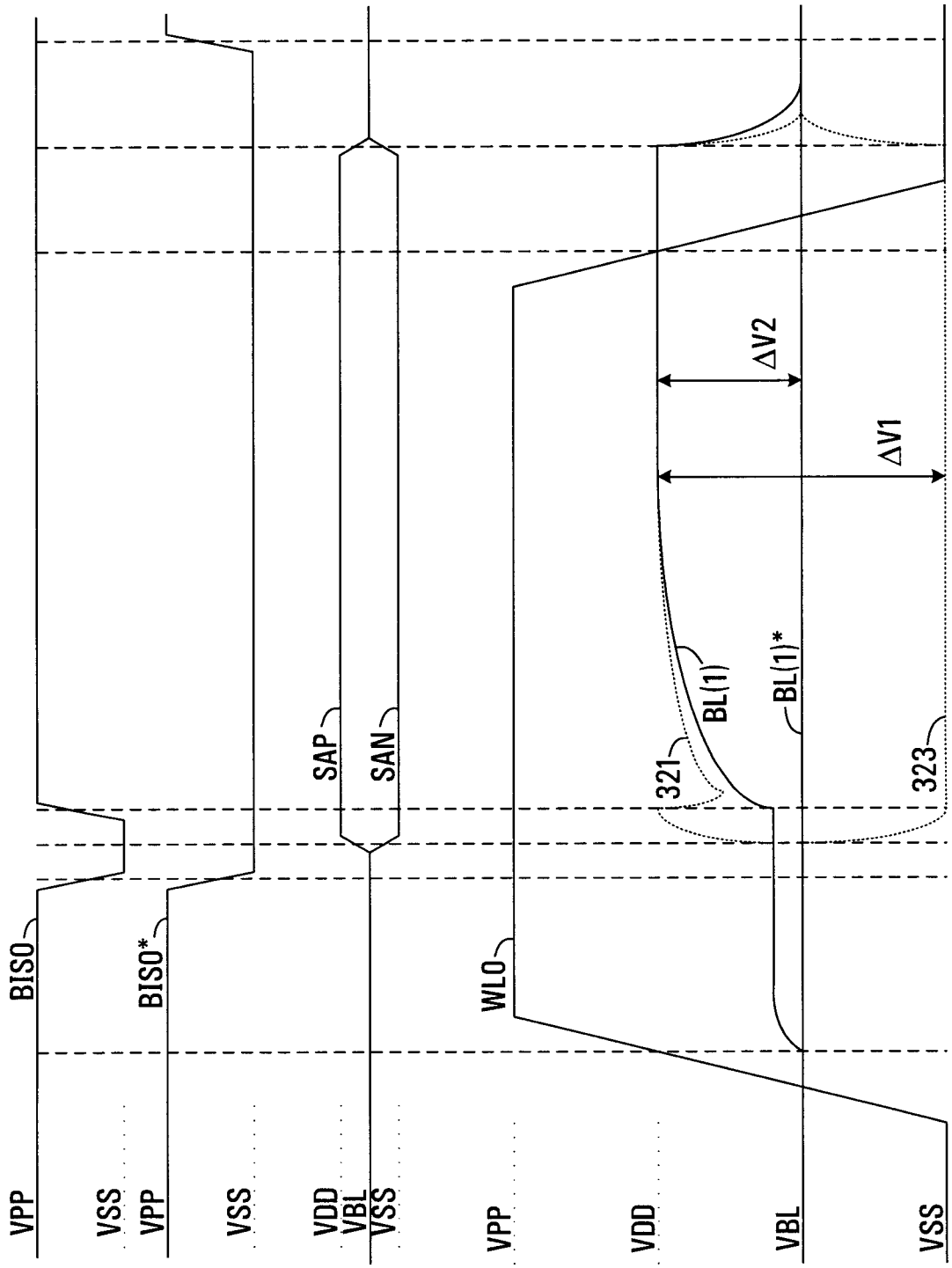

BISO
BISO*
WLO
SAP
SAN
VPP
VSS
VPP
VSS
VDD
VBL
VSS
VPP
VDD
VBL
VSS
τ0
τ1
τ2
τ3
τ4
τ5
τ6
ΔV2
ΔV1
BL(1)
BL(1)*
321
323

FIG. 3B

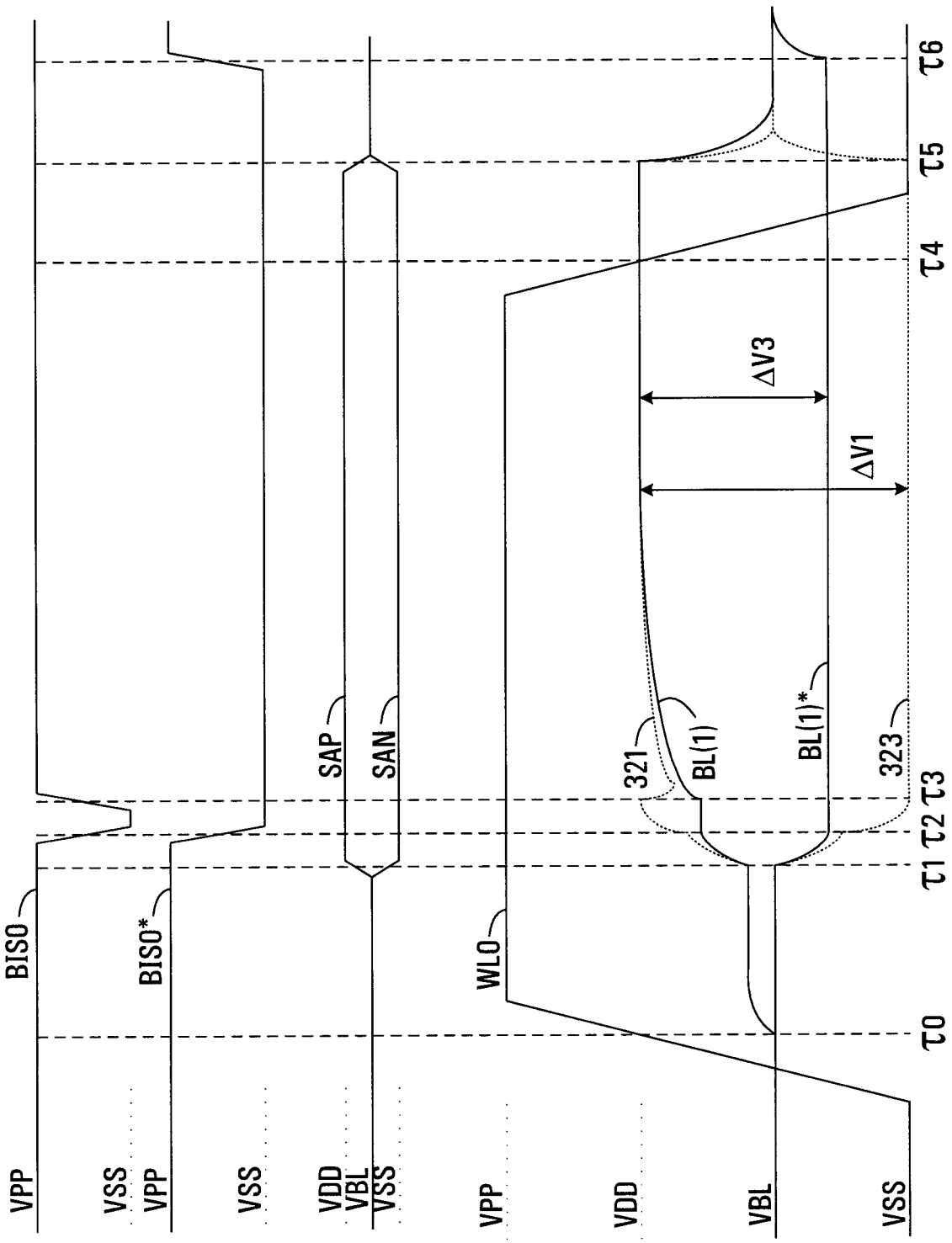

BISO
BISO*
SAP
SAN
WLO
321
BL(1)
BL(1)*
323
ΔV3
ΔV1
τ0
τ1
τ2
τ3
τ4
τ5
τ6
VPP
VSS
VPP
VSS
VDD
VBL
VSS
VPP
VDD
VBL
VSS

FIG. 3C

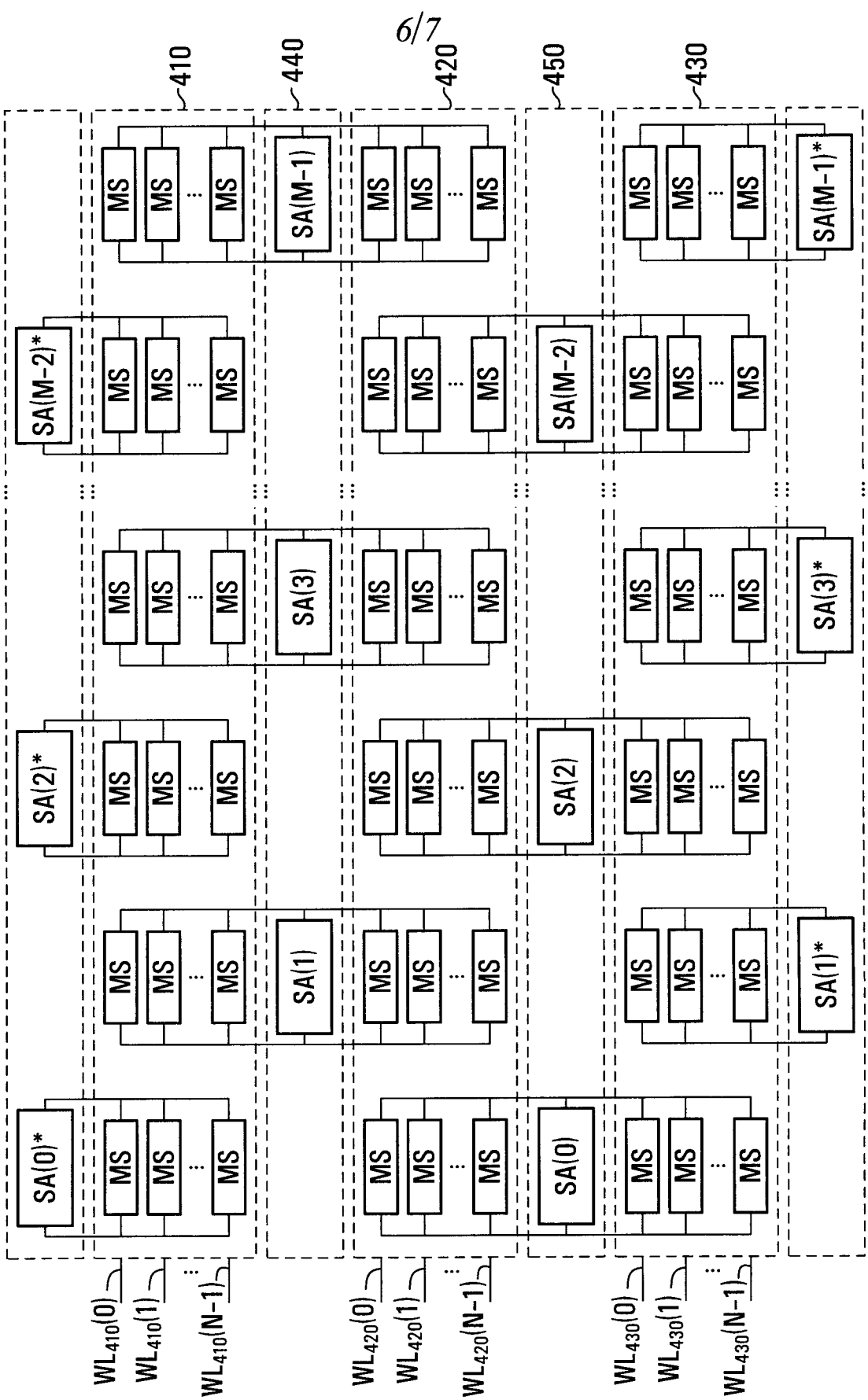

410
440
420
450
430
MS
SA(0)*
SA(1)
SA(2)*
SA(3)
SA(M-2)*
SA(M-1)
SA(0)
SA(1)*
SA(2)
SA(3)*
SA(M-2)
SA(M-1)*
WL410(0)
WL410(1)
WL410(N-1)
WL420(0)
WL420(1)
WL420(N-1)
WL430(0)
WL430(1)
WL430(N-1)

FIG. 4

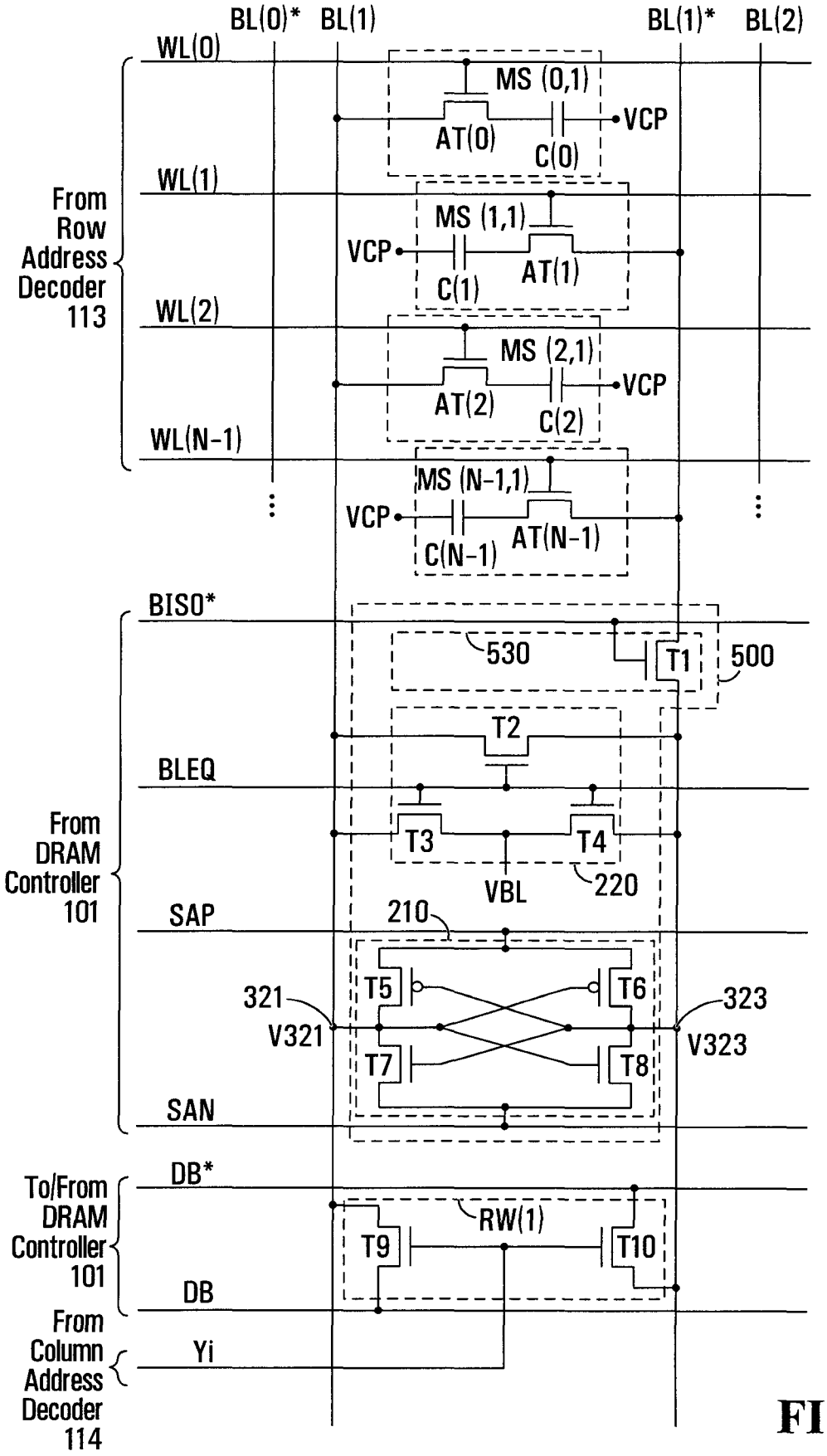

BL(0)*
BL(1)
BL(1)*
BL(2)
WL(0)
WL(1)
WL(2)
WL(N-1)
From Row Address Decoder 113
MS (0,1)
AT(0)
C(0)
VCP
MS (1,1)
AT(1)
C(1)
MS (2,1)
AT(2)
C(2)
MS (N-1,1)
AT(N-1)
C(N-1)
BISO*
530
T1
500
T2
BLEQ
T3
T4
VBL
220
From DRAM Controller 101
SAP
210
T5
T6
321
V321
323
V323
T7
T8
SAN
DB*
To/From DRAM Controller 101
RW(1)
T9
T10
DB
From Column Address Decoder 114
Yi

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2011/000242

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***G11C 11/4091*** (2006.01) , ***G11C 11/406*** (2006.01) , ***G11C 11/4094*** (2006.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (2006.01): G11C 11/4091, G11C 11/406, G11C 11/4094 in combination with keywords

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Database: Canadian Patent Database, TotalPatent
Keywords: memory cell, bitline, sense amplifier, node, isolator, connect, disconnect, refresh

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6667922 B1 (CAMACHO S. M. et al.) 23 December 2003 (23-12-2003) * Column 3, line 27 - Column 8, line 25; Figures 9-10 *	1, 23-43, 59-72
A	* Entire document *	2-22, 44-58
A	US 20020085428 A1 (KANG S.S. et al.) 4 July 2002 (4-7-2002) * Claim 1 - Claim 24 *	1-72
A	US20040223396 A1 (NAKAMURA Y. et al.) 11 November 2004 (11-11-2004) * Entire document *	1-72

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 April 2011 (13-04-2011)	9 May 2011 (09-05-2011)

Name and mailing address of the ISA/CA
Canadian Intellectual Property Office
Place du Portage I, C114 - 1st Floor, Box PCT
50 Victoria Street
Gatineau, Quebec K1A 0C9
Facsimile No.: 001-819-953-2476

Authorized officer
Andy Wong (819) 953-1562

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2011/000242

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US6667922B1	23 December 2003 (23-12-2003)	DE10337047A1	04 March 2004 (04-03-2004)
US2002085428A1	04 July 2002 (04-07-2002)	DE10154879A1	18 July 2002 (18-07-2002)
		DE10154879B4	11 October 2007 (11-10-2007)
		KR20020057356A	11 July 2002 (11-07-2002)
		US6438042B1	20 August 2002 (20-08-2002)
US2004223396A1	11 November 2004 (11-11-2004)	JP2004334961A	25 November 2004 (25-11-2004)
		JP4229230B2	25 February 2009 (25-02-2009)
		TWI273599B	11 February 2007 (11-02-2007)
		US6944076B2	13 September 2005 (13-09-2005)