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(54) Title: LARGE GAIN-BANDWIDTH AMPLIFIER, METHOD, AND SYSTEM

(57) Abstract: An amplifier includes multiple stages. Early stages of the multi-stage amplifier have low gain and preserve band-
width.



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LARGE GAIN-BANDWIDTH AMPLIFIER, METHOD, AND SYSTEM

Field

5 The present invention relates generally to amplifier circuits, and more specifically to amplifier circuits having a large gain-bandwidth product.

Background

10 Semiconductor materials such as silicon and gallium-arsenide are commonly used to manufacture integrated circuits for use in electronics. These integrated circuits typically have many transistors that are used as building blocks for larger circuits such as amplifiers. A commonly used performance measure for amplifiers is the “gain-bandwidth product.” The gain-bandwidth product describes an inverse relationship between gain and bandwidth above a certain operating frequency. In other words, amplifiers with a large
15 gain-bandwidth product can amplify signals at higher frequencies than amplifiers with a small gain-bandwidth product.

 The gain-bandwidth product of amplifiers is influenced by many factors, including the underlying semiconductor manufacturing process. For example, an amplifier circuit manufactured using one process may have a higher gain-bandwidth product than the same
20 amplifier circuit manufactured using a different process. This may be problematic in situations where an amplifier designed using a process that supports a high gain-bandwidth product is shared with designers that desire the same amplifier performance, but use a process that does not support such a high gain-bandwidth product.

 For the reasons stated above, and for other reasons stated below which will become
25 apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternate amplifiers.

Brief Description of the Drawings

 Figure 1 shows a diagram of a receiver;
30 Figure 2 shows a circuit schematic of an amplifier input stage;
 Figure 3 shows a circuit schematic of an amplifier stage with active devices and current summing points;
 Figure 4 shows a circuit schematic of a non-linear amplifier stage;

Figure 5 shows a diagram of a receiver;

Figure 6 shows a circuit schematic of an amplifier input stage;

Figure 7 shows a diagram of a receiver;

Figure 8 shows a simultaneous bidirectional port circuit;

5 Figures 9 and 10 show system diagrams in accordance with various embodiments of the present invention; and

Figure 11 shows a flowchart in accordance with various embodiments of the present invention.

10

Description of Embodiments

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that the various
15 embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein in connection with one embodiment may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may
20 be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

25 Figure 1 shows a diagram of a receiver. Receiver 100 includes a multi-stage amplifier followed by inverters 140 and 150. The multi-stage amplifier includes first stage 110, second stage 120, and third stage 130. Receiver 100 receives a DATA signal and a REF signal on differential input nodes, and produces an output signal at standard logic levels.

30 The topology of receiver 100 provides for a higher overall gain-bandwidth product that cannot be achieved with a single stage amplifier having a comparable output amplitude. First stage 110 is a low gain differential input stage. First stage 110 can operate at higher frequencies than a single stage amplifier with the same gain-bandwidth

product, because the gain of first stage 110 is lower than the gain of a single stage amplifier.

Second stage 120 receives four output signals from first stage 110 and sums currents at low impedance points, and also has low gain. Second stage 120, like first stage 110, preserves high bandwidth operation by having low gain. Third stage 130 is a high gain stage that operates as a level converter to increase the signal level. Inverters 140 and 150 are included to provide standard logic output levels and signal transition times, but are not necessary. For example, in some embodiments, inverters 140 and 150 provide complementary metal oxide semiconductor (CMOS) output signal. Various embodiments of first stage 110, second stage 120, and third stage 130 are described with reference to the figures that follow.

Figure 2 shows a circuit schematic of an amplifier input stage. Input stage 110 includes complementary differential input amplifiers 210 and 220. Amplifier 210 includes current source 202 and transistors 212, 214, 216, and 218. Transistors 212 and 214 form a first differential input pair of transistors that receive input signals from the differential input on nodes 204 and 206.

The transistors shown in Figure 2 are shown as isolated gate transistors, and specifically as metal oxide semiconductor field effect transistors (MOSFETs). For example, transistors 212 and 214 are shown as P-type MOSFETs, and transistors 216 and 218 are shown as N-type MOSFETs. Other types of switching or amplifying elements may be utilized for the various transistors of input stage 110 without departing from the scope of the present invention. For example, the transistors of amplifier 210 may be junction field effect transistors (JFETs), bipolar junction transistors (BJTs), or any device capable of performing as described herein.

Transistors 216 and 218 are "diode-connected" transistors that provide "diode loads" to the differential input transistor pair formed by transistors 212 and 214. The term "diode-connected," as used herein, refers to a transistor that has a gate and a drain coupled together, as do transistors 216 and 218. The diode loads represent relatively low impedance loads that keep the gain of amplifier 210 low. In some embodiments, other load devices are used in input stage 110. For example, in some embodiments, resistors are used in place of transistors 216 and 218, and in other embodiments, diodes are used in place of transistors 216 and 218.

Output signals R_{OUTN} and D_{OUTN} are produced by amplifier 210 on nodes 240 and

242, respectively. The voltage difference between output signal R_{OUTN} and lower power supply node 262 represents the gate-to-source voltage (V_{GS}) on transistor 216. The voltage difference between output signal D_{OUTN} and lower power supply node 262 represents the gate-to-source voltage (V_{GS}) on transistor 218. R_{OUTN} and D_{OUTN} vary as
5 current is switched between the two load devices based on the action of the differential input pair formed by transistors 212 and 214.

Amplifier 220 includes current source 221 and transistors 222, 224, 226, and 228. Transistors 222 and 224 form a second differential input pair of transistors that receive input signals from the differential input on nodes 204 and 206.

10 Transistors 226 and 228 are diode-connected transistors that provide diode loads to the differential input transistor pair formed by transistors 222 and 224. The diode loads represent relatively low impedance loads that keep the gain of amplifier 220 low.

Output signals R_{OUTP} and D_{OUTP} are produced by amplifier 220 on nodes 250 and 252, respectively. The voltage difference between reference node 260 and output signals
15 R_{OUTP} and D_{OUTP} represent the source-to-gate voltages (V_{SG}) on the corresponding load devices, as current is switched between the two load devices based on the action of the differential input pair formed by transistors 222 and 224.

Amplifier 210 utilizes P-type transistors for the differential input pair of transistors, and amplifier 220 utilizes N-type transistors for the differential input pair.
20 Accordingly, amplifiers 210 and 220 are referred to as “complementary.”

The complementary amplifiers of input stage 110 provide a wide common mode input voltage range. When the input common mode voltage approaches the voltage value of the upper power supply node 260, amplifier 210 may cease to operate, in part because current source 202 may stop sourcing current to the rest of amplifier 210. As amplifier
25 210 shuts off, amplifier 220 continues to operate. The opposite is true when the input common mode voltage approaches the voltage value of the lower power supply node 262. As the input common mode voltage drops, amplifier 220 may cease to operate, but amplifier 210 will continue to operate.

Figure 3 shows a circuit schematic of an amplifier stage with active devices and
30 current summing points. Amplifier stage 120 includes current mirror transistors 302, 304, 306, and 308. Amplifier stage 120 also includes diode-connected transistors 312, 314, 316, and 318. Transistors 312 and 316 are coupled between upper power supply node 260 and lower power supply node 262 to form low impedance node 320, and transistors 314

and 318 are coupled between upper power supply node 260 and lower power supply node 262 to form low impedance node 322.

Transistors 302, 304, 306, and 308 are active devices that source current to low impedance nodes 320 and 322. The currents sourced by transistors 302 and 306 are summed at low impedance node 322, and the currents sourced by transistors 304 and 308 are summed at low impedance node 320. As such, low impedance nodes 320 and 322 are current summing points within a low gain amplifier stage.

Currents sourced by transistors 302, 304, 306, and 308 are influenced by the voltages on the corresponding gate nodes. For example, the signal R_{OUTN} on node 240 influences the amount of current sourced by transistor 308. Referring now back to Figure 2, R_{OUTN} represents the gate-to-source voltage (V_{GS}) of diode-connected transistor 218. Because the same V_{GS} is applied across transistors 216 (Figure 2) and 308 (Figure 3), transistor 308 operates as a current mirror and mirrors the current that flows drain-to-source in transistor 216. Transistors 302, 304, and 306 operate as current mirrors in a similar fashion.

The gain of amplifier stage 120 is low, due in part to the low impedance current summing nodes at 320 and 322. The active devices at the input to amplifier stage 120, and the low impedance current summing points combine to form an amplifier that preserves high bandwidth operation with low gain. Signals A and B form a differential output signal from amplifier stage 120 on nodes 322 and 320.

The operation of amplifier stage 120 preserves the wide common mode input range described above with reference to Figure 2. If one of the complementary differential amplifiers in input stage 110 (Figure 2) begins to shut off, the corresponding active devices in amplifier stage 120 will also begin to shut off, but the remaining active devices will still operate. For example, as the input common mode voltage approaches the upper rail, amplifier 210 (Figure 2) will begin to shut off, and R_{OUTN} and D_{OUTN} will drop below the threshold voltage of the diode connected transistors 216 and 218, and transistors 306 and 308 will shut off. During this time, however, transistors 302 and 304 will continue to operate. The opposite is also true. As transistors 302 and 304 shut off, transistors 306 and 308 still operate. This preserves the wide common mode input range of receiver 100 (Figure 1).

Figure 4 shows a circuit schematic of a non-linear amplifier stage. Amplifier stage 130 includes complementary non-linear amplifiers 420 and 430. Amplifiers 420 and 430

include differential input pairs, a diode load and a load transistor coupled as a positive feedback device. For example, amplifier 420 includes differential pair of transistors 402 and 404, diode-connected transistor 406, and load transistor 408 coupled as a positive feedback device. Also for example, amplifier 430 includes differential pair of transistors 412 and 414, diode-connected transistor 416, and load transistor 418 coupled as a positive feedback device.

Each of amplifiers 420 and 430 detect a voltage differential on input nodes 460 and 462, and produce an output voltage near either upper power supply node 260 or lower power supply node 262. Outputs from both amplifier stages 420 and 430 are combined to form the output signal "OUT" on node 450. Amplifier stage 130 operates as a level converter to convert the signal levels received to nearly the level of the power supply nodes 260 and 262. The voltages at the power supply nodes are also referred to as the "supply rails."

Amplifier stage 130 operates with high gain and high bandwidth, in part because it is non-linear. An output signal near the supply rails can be produced at the frequency of operation of the earlier amplifier stages 110 and 120. Other non-linear amplifier stages can be utilized for amplifier stage 130 without departing from the scope of the present invention.

Amplifier stage 120 (Figure 3) is shown having two low impedance nodes (320, 322), and two output signals (A, B). In some embodiments, amplifier stage 120 includes four low impedance nodes, and four output signals, one from each low impedance node. For example, transistor 304 may be coupled to diode-connected transistor 316 to form a first low impedance node, transistor 308 may be coupled to diode-connected transistor 312 to form a second low impedance node, transistor 302 may be coupled to diode-connected transistor 318 to form a third low impedance node, and transistor 306 may be coupled to diode-connected transistor 314 to form a fourth low impedance node. In these embodiments, amplifier stage 120 includes four output nodes, one corresponding to each of the low impedance nodes.

Amplifier stage 130 (Figure 4) is shown having two input nodes coupled in parallel between amplifiers 420 and 430. In some embodiments, amplifier stage 130 receives four input signals on four separate nodes, with one node connected to one transistor of each differential input transistor pair. For example, in embodiments described in the previous paragraph, amplifier stage 120 provides four output signals from low impedance nodes,

and these output signals may be provided separately to the gates of transistors 402, 404, 412, and 414.

Figure 5 shows a diagram of a receiver. Receiver 500 includes a multi-stage amplifier and inverters 140 and 150. The multi-stage amplifier of receiver 500 includes input stage 510, second stage 120, and third stage 130. Amplifier stages 120 and 130, and inverters 140 and 150 are described above with reference to previous figures. Input stage 510 is similar to input stage 110 (Figures 1, 2), but it includes circuitry to select a reference voltage as half of the differential input signal. Input stage 510 is described below with reference to Figure 6.

Figure 6 shows a circuit schematic of an amplifier input stage. Input stage 510 includes complementary differential input amplifiers 610 and 620. Amplifier 610 includes current source 602 and transistors 632, 634, 636, 638, 640, 642 and 644.

Transistors 632 and 636 are pass transistors that select either transistor 634 or transistor 638 to be electrically included in the circuit based on the logic level of signal "REFERENCE SELECT." When REFERENCE SELECT is high, transistor 632 is off, transistor 636 is on, and transistor 638 is in the circuit. In this case, transistors 642 and 638 form a first differential input pair of transistors that receive an input signal ("DATA") on node 641, and a reference voltage ("REF_{LO}") on node 637. When REFERENCE SELECT is low, transistor 636 is off, transistor 632 is on, and transistor 634 is in the circuit. In this case, transistors 642 and 634 form the first differential input pair of transistors that receive the input signal on node 641, and a reference voltage ("REF_{HI}") on node 639.

The transistors shown in Figure 6 are shown as isolated gate transistors, and specifically as metal oxide semiconductor field effect transistors (MOSFETs). For example, transistor 642 is shown as a P-type MOSFET, and transistor 644 is shown as an N-type MOSFET. Other types of switching or amplifying elements may be utilized for the various transistors of input stage 510 without departing from the scope of the present invention. For example, the transistors of amplifier 610 may be junction field effect transistors (JFETs), bipolar junction transistors (BJTs), or any device capable of performing as described herein.

Transistors 640 and 644 are "diode-connected" transistors that provide diode loads to the first differential input transistor pair. The diode loads represent relatively low impedance loads that keep the gain of amplifier 610 low. In some embodiments, other

load devices are used in input stage 510. For example, in some embodiments, resistors are used in place of transistors 640 and 644, and in other embodiments, diodes are used in place of transistors 640 and 644.

Output signals D_{OUTN} and R_{OUTN} are produced by amplifier 510 on nodes 670 and 672, respectively. The voltage difference between output signal R_{OUTN} and lower power supply node 262 represents the gate-to-source voltage (V_{GS}) on transistor 640. The voltage difference between output signal D_{OUTN} and lower power supply node 262 represents the gate-to-source voltage (V_{GS}) on transistor 644. R_{OUTN} and D_{OUTN} vary as current is switched between the two load devices based on the action of the first differential input pair.

Amplifier 620 includes current source 601 and transistors 652, 654, 656, 658, 660, 662 and 664. Transistors 652 and 656 are pass transistors that select either transistor 654 or transistor 658 to be electrically included in the circuit based on the logic level of the REFERENCE SELECT signal. When REFERENCE SELECT is high, transistor 652 is off, transistor 656 is on, and transistor 658 is in the circuit. In this case, transistors 662 and 658 form a second differential input pair of transistors that receive the input signal on node 641 and the reference voltage REF_{LO} on node 637. When REFERENCE SELECT is low, transistor 656 is off, transistor 652 is on, and transistor 654 is in the circuit. In this case, transistors 662 and 654 form the second differential input pair of transistors that receive the input signal on node 641 and the reference voltage REF_{HI} on node 639.

Input stage 510 is shown having a mechanism to select between two reference voltage values. In some embodiments, the reference voltage to be used can be selected from more than two possibilities. For example, more pass transistor and input transistor combinations can be in parallel with transistors 652, 654, 656, and 658. Any number of these circuits can be included in parallel, thereby allowing any number of reference voltages to be selectable.

Output signals R_{OUTP} and D_{OUTP} are produced by amplifier 620 on nodes 680 and 682, respectively. The voltage difference between upper power supply node 260 and output signals R_{OUTP} and D_{OUTP} represent the source-to-gate voltages (V_{SG}) on the corresponding load device, as current is switched between the two load devices based on the action of the second differential input pair.

Amplifier 610 utilizes P-type transistors for the differential input pair of transistors, and amplifier 620 utilizes N-type transistors for the differential input pair.

Accordingly, amplifiers 610 and 620 are referred to as “complementary.”

The complementary amplifiers of input stage 510 provide a wide common mode input voltage range. When the input common mode voltage approaches the voltage value of the upper power supply node 260, amplifier 610 may cease to operate, in part because
5 current source 602 may stop sourcing current to the rest of amplifier 610. As amplifier 610 shuts off, amplifier 620 continues to operate. The opposite is true when the input common mode voltage approaches the voltage value of the lower power supply node 262. As the input common mode voltage drops, amplifier 620 may cease to operate, but amplifier 610 will continue to operate.

10 Figure 7 shows a diagram of a receiver. Receiver 700 includes parallel input stages 510A-510D, second stage 120, third stage 130, and inverters 140 and 150. Second stage 120, third stage 130, and inverters 140 and 150 are described above with reference to previous figures.

Input stages 510A-510D are each separate input stages with selectable reference
15 voltages such as input stage 510 (Figure 6). Input stages 510A-510D are coupled in parallel with respect to the input signals $DATA$, REF_{HI} , and REF_{LO} , and the output signals that drive second stage 120. Each of input stages 510A-510D receives a separate REFERENCE SELECT signal. This allows each of the parallel input stages to separately select between REF_{HI} and REF_{LO} for comparison against the $DATA$ signal.

20 Figure 8 shows a simultaneous bidirectional port circuit. Simultaneous bidirectional port circuit 800 includes output driver 810, control circuit 820, and receiver 830. Output driver 810 drives data onto conductor 812, and receiver 830 receives data from conductor 812. Another simultaneous bidirectional port circuit can be coupled to drive data on conductor 812 in same manner as bidirectional port circuit 800.

25 Conductor 812 is a simultaneous bidirectional signal node. When two simultaneous bidirectional port circuits are configured to drive data on conductor 812, the voltage on the conductor is the sum of the voltages representing data from both simultaneous bidirectional data ports. Receiver 830 receives the data transmitted by the other simultaneous bidirectional port circuit (not shown) by subtracting the effects of the
30 voltage driven by output driver 810.

Receiver 830 can be implemented using a receiver with a selectable reference, such as receiver 500 (Figure 5) or receiver 700 (Figure 7). The selected reference corresponds to the data that is being driven on conductor 812 by driver 810. By utilizing the outbound

data to select a reference in receiver 830, the effects of the voltage driven by output driver 810 can be “subtracted” out from the voltage on the simultaneous bidirectional signal node, and receiver 830 can receive the data driven onto conductor 812 by the other port circuit (not shown).

5 Control circuit 820 receives the data to be driven by driver 810, and provides the REFERENCE SELECT signal to receiver 830. In some embodiments, control circuit 820 includes a buffer or inverter. In these embodiments, the outgoing data effectively serves as the REFERENCE SELECT signal. For example, when receiver 830 includes receiver 500 (Figure 5), a single REFERENCE SELECT signal is provided to select between
10 REF_{HI} and REF_{LO} in input stage 510. In other embodiments, control circuit 820 includes more circuitry than a buffer or inverter. For example, when receiver 830 includes receiver 700 (Figure 7), control circuit 820 may provide multiple REFERENCE SELECT signals.

 In some embodiments, multiple REFERENCE SELECT signals are provided by control circuit 820. This may be useful when output driver 810 includes a controlled slew
15 rate feature. For example, output driver 810 may drive outgoing data onto conductor 812 at a controlled slew rate to reduce the rise time or fall time of the signal. To “subtract” the effects of the outgoing signal as it transitions with a controlled slew rate, control circuit 820 may assert the multiple REFERENCE SELECT signals in sequence. In these
embodiments, control circuit 820 may also provide control signals to output driver 810 to
20 control the outgoing slew rate.

 By utilizing receiver 500 (Figure 5) or receiver 700 (Figure 7) for receiver 830, the effective gain-bandwidth product of receiver 830 can be increased. This can be useful to allow simultaneous bidirectional port circuits manufactured in a slower process to
communicate with simultaneous bidirectional port circuits manufactured in a faster
25 process. The simultaneous bidirectional port circuits in the faster process can have a single stage amplifier for a receiver, whereas the simultaneous bidirectional port circuit in the slower process can have one of the multi-stage amplifiers described herein as the receiver.

 Multi-stage amplifiers, receivers, simultaneous bidirectional port circuits and other
30 embodiments of the present invention can be implemented in many ways. In some embodiments, they are implemented in integrated circuits as part of data busses. In some embodiments, design descriptions of the various embodiments of the present invention are included in libraries that enable designers to include them in custom or semi-custom

designs. For example, any of the disclosed embodiments can be implemented in a synthesizable hardware design language, such as VHDL or Verilog, and distributed to designers for inclusion in standard cell designs, gate arrays, or the like. Likewise, any embodiment of the present invention can also be represented as a hard macro targeted to a specific manufacturing process. For example, receiver circuit 700 (Figure 7) can be represented as polygons assigned to layers of an integrated circuit.

Figures 9 and 10 show system diagrams in accordance with various embodiments of the present invention. Figure 9 shows system 900 including integrated circuits 910 and 920. Integrated circuit 910 includes simultaneous bidirectional (SBD) port circuit 912, and integrated circuit 920 includes SBD port circuit 922. As shown in Figure 9, both SBD port circuits drive data onto, and receive data from, conductor 902. Conductor 902 serves as a simultaneous bidirectional signal node. One or more of SBD port circuits 912 and 922 can be implemented with SBD port circuit 800 (Figure 8) that includes one of the multi-stage, high gain-bandwidth amplifiers described herein.

Integrated circuits 910 and 920 can be any type of integrated circuit capable of including one or more SBD port circuits as shown. For example, either integrated circuit 910 or 920 can be a processor such as a microprocessor, a digital signal processor, a microcontroller, or the like. Either integrated circuit can also be an integrated circuit other than a processor such as an application-specific integrated circuit (ASIC), a communications device, a memory controller, or a memory such as a dynamic random access memory (DRAM). For ease of illustration, portions of integrated circuits 910 and 920 are not shown. The integrated circuits may include much more circuitry than illustrated in Figure 9 without departing from the scope of the present invention.

In some embodiments, integrated circuit 910 includes a processor, SBD port circuit 912 does not include a multi-stage amplifier, integrated circuit 920 includes a memory device, and SBD port circuit 922 does include a multi-stage amplifier of the type described herein. In these embodiments, the use of one of the multi-stage amplifiers in integrated circuit 920 may allow a memory device manufactured in a slower process to communicate with a processor manufactured in a faster process. In other embodiments, SBD port circuits in both integrated circuits include multi-stage amplifiers, regardless of whether processors or memory devices are included.

Integrated circuits 910 and 920 are shown in Figure 9 having a single SBD port circuit each. In some embodiments, each integrated circuit may have many more SBD

port circuits. For example, in some embodiments, entire data busses are driven by banks of SBD port circuits. In other embodiments, nodes for control signals or groups of nodes for control signals are driven by SBD port circuits.

Figure 10 shows electronic system 1000 including processor 1010 and memories
5 1020 and 1030. Processor 1010 includes SBD port circuits 1012 and 1014, memory 1020 includes SBD port circuits 1022 and 1024, and memory 1030 includes SBD port circuits 1032 and 1034. One or more of the SBD port circuits shown in Figure 9 may include a receiver with a multi-stage amplifier, such as receiver 500 (Figure 5) or receiver 700 (Figure 7).

10 Processor 1010, memory 1020, and memory 1030 are configured in a ring such that each device communicates with two others using at least one SBD port circuit coupled to a simultaneous bidirectional signal node. For example, processor 1010 communicates with memory 1020 using SBD port circuit 1014 coupled to simultaneous bidirectional signal node 1002, and also communicates with memory 1030 using SBD port circuit 1012
15 coupled to simultaneous bidirectional signal node 1006. Also for example, memory device 1020 communicates with memory device 1030 using SBD port circuit 1024 coupled to simultaneous bidirectional signal node 1004.

Processor 1010 and memory devices 1020 and 1030 are shown in Figure 10 having two SBD port circuits each. In some embodiments, each device may have many more
20 SBD port circuits. For example, in some embodiments, entire data busses are driven by banks of SBD port circuits. In other embodiments, nodes for control signals or groups of nodes for control signals are driven by SBD port circuits.

In some embodiments, processor 1010 is part of one integrated circuit die, memory device 1020 is part of a second integrated circuit die, and memory device 1030 is part of a
25 third integrated circuit die. In these embodiments, each of the integrated circuit dice may be separately packaged and mounted on a common circuit board. Each of the integrated circuits may also be separately packaged and mounted on separate circuit boards interconnected by the simultaneous bidirectional signal nodes. In other embodiments, processor 1010 and memory devices 1020 and 1030 are separate integrated circuit dice
30 packaged together, such as in a multi-chip module.

Figure 10 shows one processor and two memory devices. In some embodiments, many more memory devices are included. Further, any number of processors can be included. In other embodiments, circuit types other than processors and memory devices

are included in system 1000.

Systems represented by the various foregoing figures can be of any type. Examples of represented systems include computers (e.g., desktops, laptops, handhelds, servers, tablets, web appliances, routers, etc.), wireless communications devices (e.g.,
5 cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games, watches, etc.), and the like.

10 Figure 11 shows a flowchart in accordance with various embodiments of the present invention. In some embodiments, method 1100, or portions thereof, is performed by a multi-stage amplifier, embodiments of which are shown in previous figures. In other embodiments, method 1100 is performed by a simultaneous bidirectional port circuit, an integrated circuit, or an electronic system. Method 1100 is not limited by the particular
15 type of apparatus performing the method. The various actions in method 1100 may be performed in the order presented, or may be performed in a different order. Further, in some embodiments, some actions listed in Figure 11 are omitted from method 1100.

Method 1100 is shown beginning with block 1110 in which a simultaneous bidirectional data signal is received, and in block 1120, the simultaneous bidirectional data
20 signal is compared against a reference voltage with a low gain input stage. The actions in these blocks correspond to the operation of input stage 110 (Figures 1, 2) or input stage 510 (Figures 5, 6). These actions may also correspond to a parallel combination of input stages such as those shown in Figure 7. In some embodiments, the comparing action includes selecting a reference voltage from a plurality of reference voltages. For example,
25 a reference voltage may be selected using input stage 510 (Figure 6).

In block 1130, at least one current mirror is driven with an output of the low gain stage, and in block 1140, currents from the at least one current mirror are summed at a diode load. The actions of blocks 1130 and 1140 correspond to the operation of second
stage 120 (Figure 3). In block 1150, a signal at the diode load is amplified with a non-
30 linear gain stage, such as third stage 130 (Figure 4).

Although the present invention has been described in conjunction with certain embodiments, it is to be understood that modifications and variations may be resorted to without departing from the spirit and scope of the invention as those skilled in the art

readily understand. Such modifications and variations are considered to be within the scope of the invention and the appended claims.

What is claimed is:

1. An amplifier circuit comprising:
an input stage having a low impedance load; and
5 a second stage including an active device coupled to the low impedance load of the input stage, and including a diode load coupled to the active device.
2. The amplifier circuit of claim 1 wherein the low-impedance load of the input stage comprises a diode-connected transistor.
3. The amplifier circuit of claim 2 wherein the active device comprises a current
10 mirror transistor to mirror current in the diode-connected transistor.
4. The amplifier circuit of claim 1 wherein:
the input stage includes first and second input transistors configured as a differential input pair; and
the second stage includes first and second current mirror transistors coupled to the
15 first and second input transistors.
5. The amplifier circuit of claim 4 further comprising first and second diode-connected transistors coupled as load devices to the first and second input transistors.
6. The amplifier circuit of claim 1 further comprising a non-linear third stage coupled to the diode load of the second stage.
- 20 7. The amplifier circuit of claim 1 wherein the input stage includes complementary differential input circuits having input nodes coupled in parallel.
8. The amplifier circuit of claim 1 wherein the input stage includes a differential input stage having a selectable reference.

9. The amplifier circuit of claim 1 wherein the input stage includes a plurality of differential input stages coupled in parallel, wherein each of the plurality of differential input stages is configured to independently select a reference.

10. A simultaneous bidirectional port circuit comprising:

5 an output driver; and

a receiver having a low gain first stage coupled to the output driver, and a second stage having current mirrors responsive to the low gain first stage to supply currents to low impedance summing points.

11. The simultaneous bidirectional port circuit of claim 10 wherein the low gain first stage comprises:

10 a first input node coupled to receive an input signal from the output driver, a second input node coupled to receive a first reference voltage, and a third input node coupled to receive a second reference voltage; and

a selection mechanism configured to select the first reference voltage or the second reference voltage to compare against the input signal.

12. The simultaneous bidirectional port circuit of claim 10 wherein the low impedance summing points comprise a first circuit node coupled between power supply nodes by a first pair of diodes, and a second circuit node coupled between the power supply nodes by a second pair of diodes.

20 13. The simultaneous bidirectional port circuit of claim 12 further comprising a high gain stage coupled to receive a differential input signal from the first and second circuit nodes.

14. The simultaneous bidirectional port circuit of claim 10 further comprising a high gain stage to amplify a signal at the low impedance summing points.

25 15. A memory device comprising:

a receiver circuit to extract incoming data from a node configured to have a simultaneous bidirectional data signal, the receiver circuit including:

a low gain first stage to preserve bandwidth;
a low gain second stage having current mirrors driving a diode load; and
a high gain third stage.

16. The memory device of claim 15 wherein the low gain first stage comprises a
5 plurality of input stages in parallel, wherein each input stage is configured to
independently select a reference signal to compare against the simultaneous bidirectional
data signal.

17. The memory device of claim 16 wherein each of the plurality of input stages
includes complementary differential input transistor pairs.

10 18. The memory device of claim 17 wherein each of the plurality of input stages
includes at least one diode load.

19. The memory device of claim 15 further comprising an inverter following the high
gain third stage.

15 20. The memory device of claim 15 wherein the low gain first stage comprises a
differential pair of transistors coupled to low impedance load devices.

21. The memory device of claim 20 wherein the low impedance load devices comprise
diode-connected transistors.

22. An electronic system comprising:
a microprocessor configured to send and receive data on a simultaneous
20 bidirectional signal node; and
a memory device having a receiver circuit to extract an incoming data stream from
the simultaneous bidirectional signal node, the receiver circuit including:
a low gain first stage to preserve bandwidth;
a low gain second stage having current mirrors driving a diode load; and
25 a high gain third stage.

23. The electronic system of claim 22 wherein the low gain first stage comprises a differential pair of transistors coupled to low impedance load devices.

24. The electronic system of claim 23 wherein the low impedance load devices comprise diode-connected transistors.

5 25. A method comprising:
receiving a simultaneous bidirectional data signal;
comparing the simultaneous bidirectional data signal against a reference voltage
with a low gain input stage;
driving at least one current mirror with an output of the low gain stage; and
10 summing currents from the at least one current mirror at a diode load.

26. The method of claim 25 wherein comparing comprises selecting the reference voltage from a plurality of reference voltages.

27. The method of claim 25 further comprising amplifying a signal at the diode load with a non-linear gain stage.

15 28. The method of claim 25 wherein comparing comprises:
comparing with a low gain input stage that includes complementary differential input transistor pairs with parallel input nodes and multiple output nodes.

29. The method of claim 28 wherein driving at least one current mirror comprises driving a separate current mirror for each of the multiple output nodes.

20 30. The method of claim 29 wherein summing comprises summing currents from the separate current mirrors to form a differential output node.

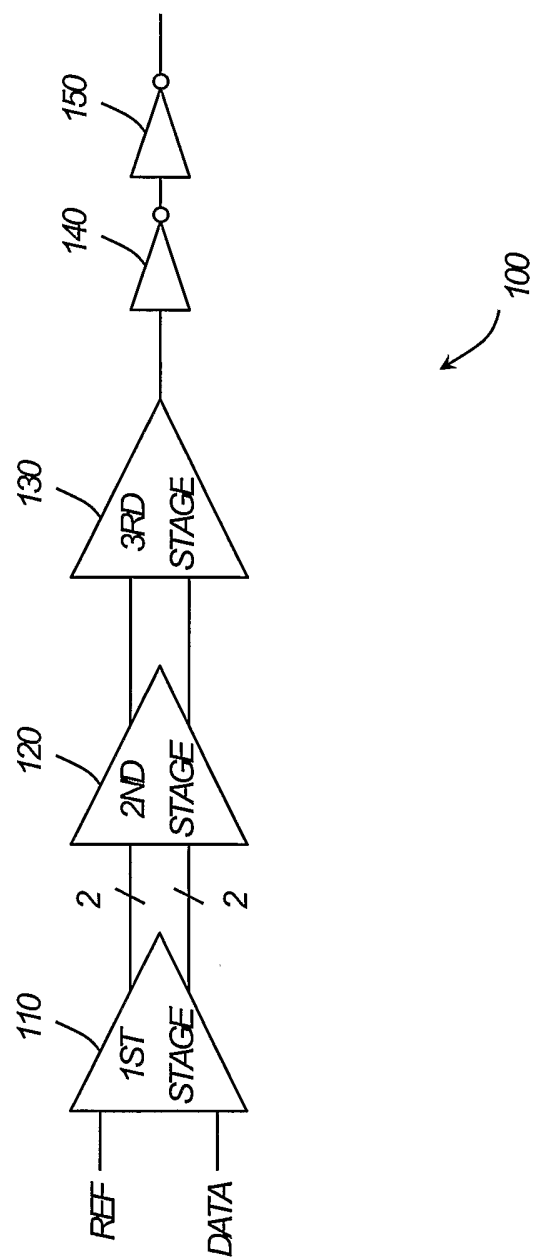


FIG. 1

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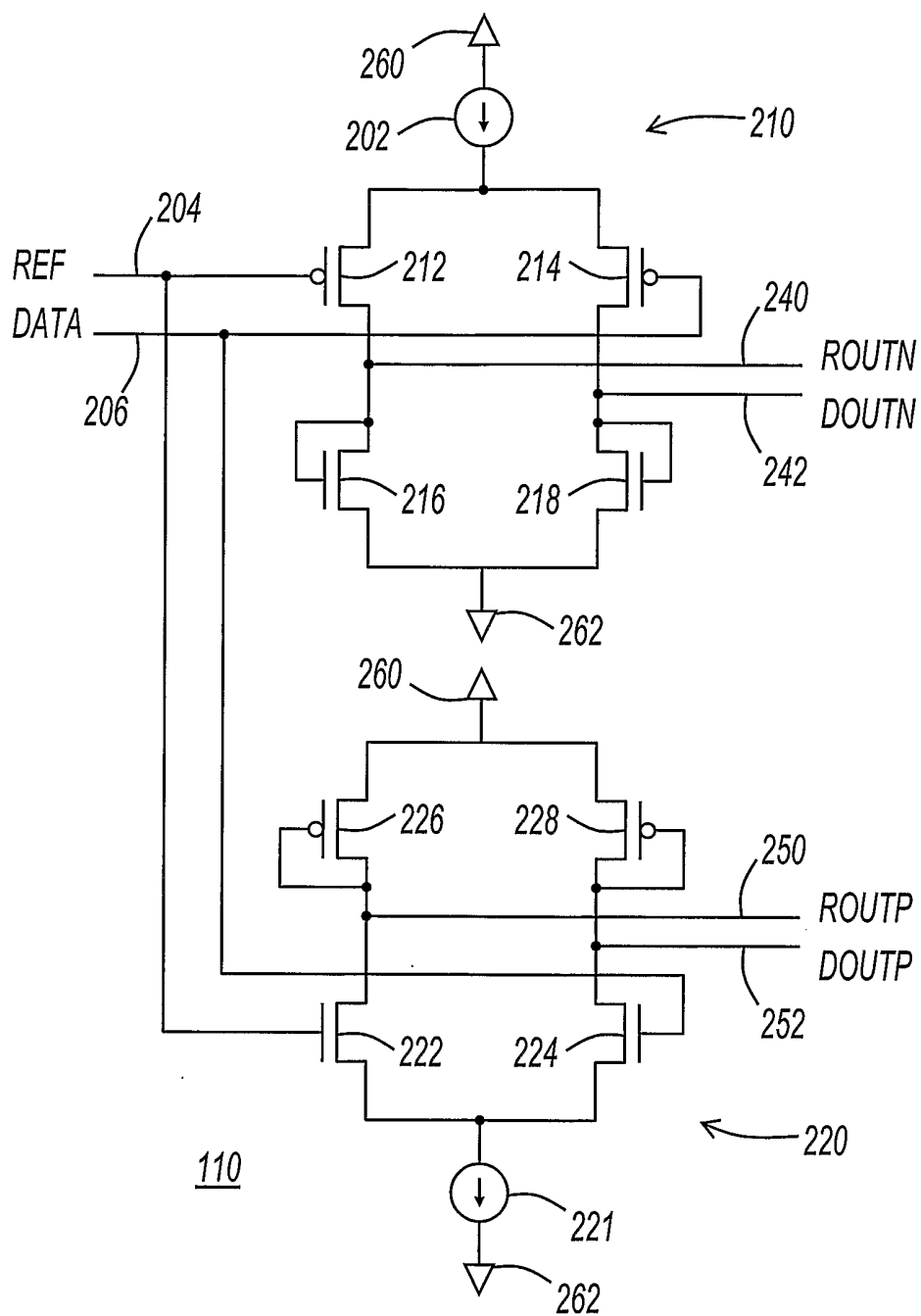


FIG. 2

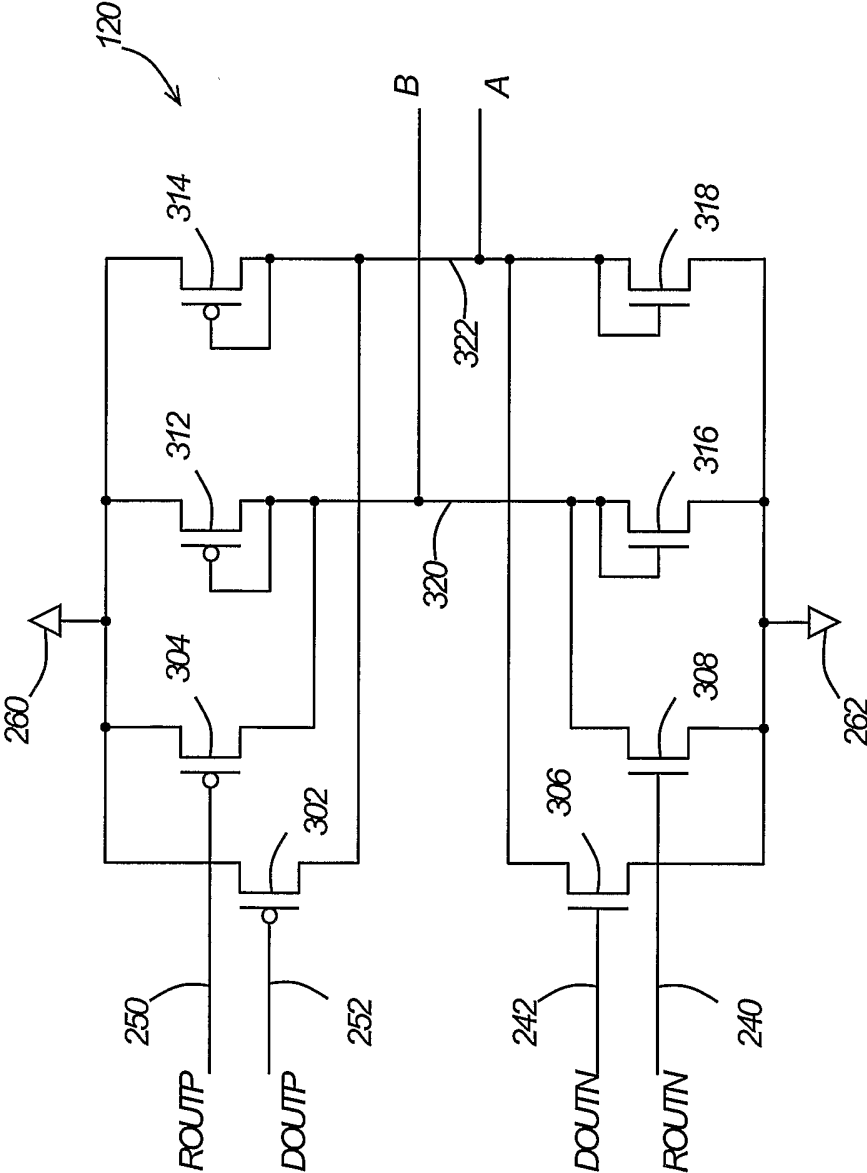


FIG. 3

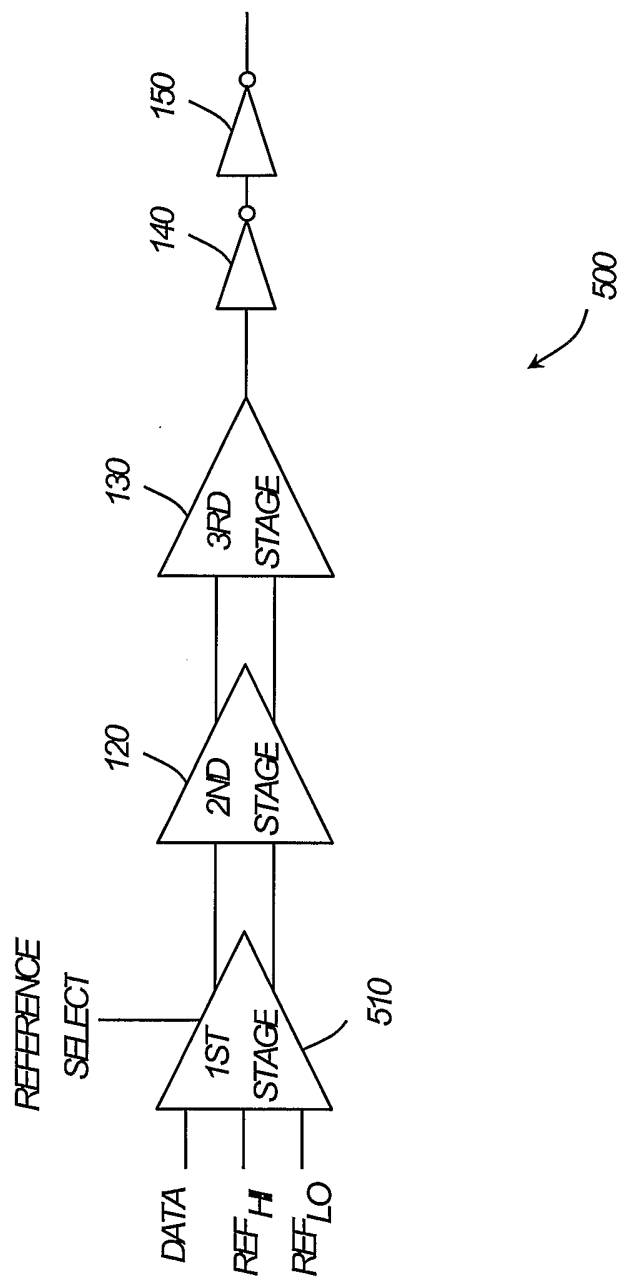


FIG. 5

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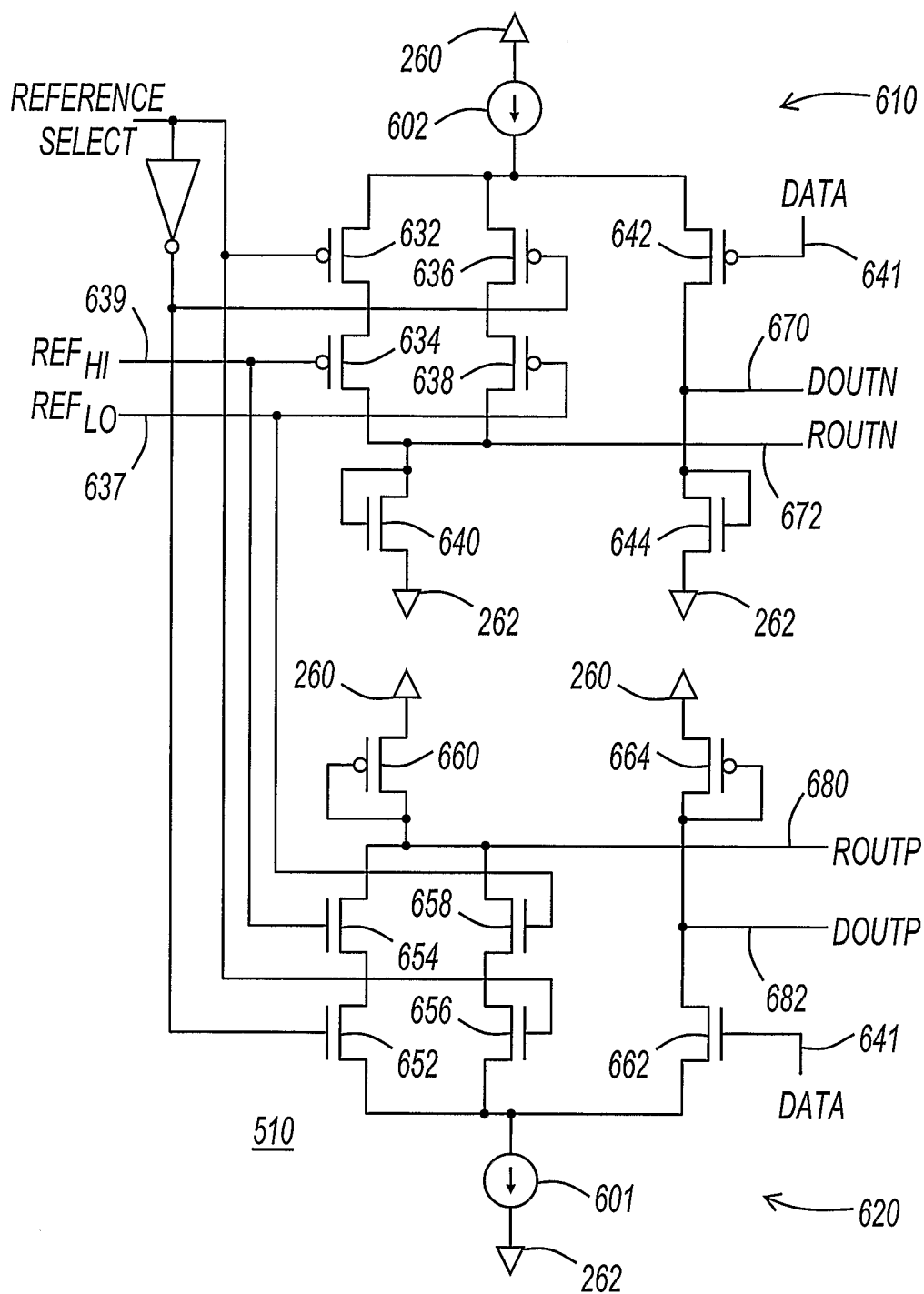


FIG. 6

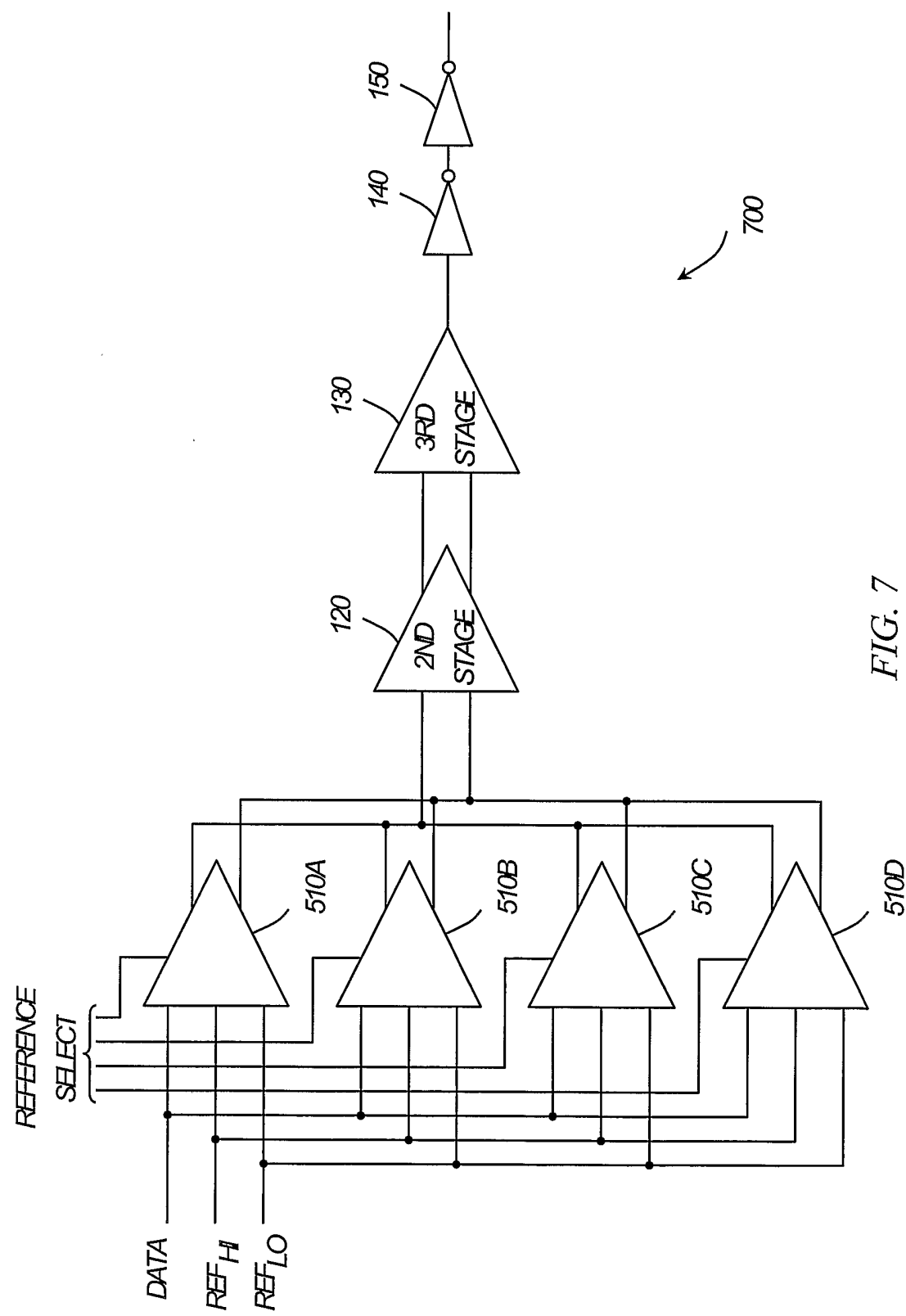


FIG. 7

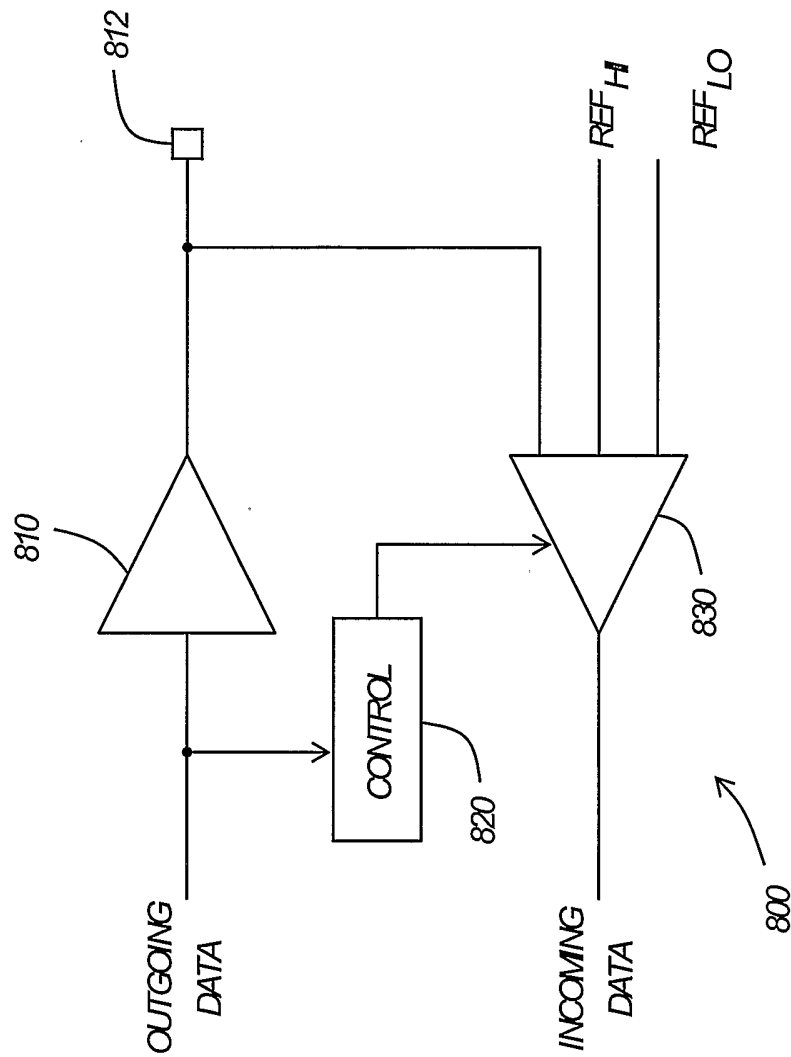


FIG. 8

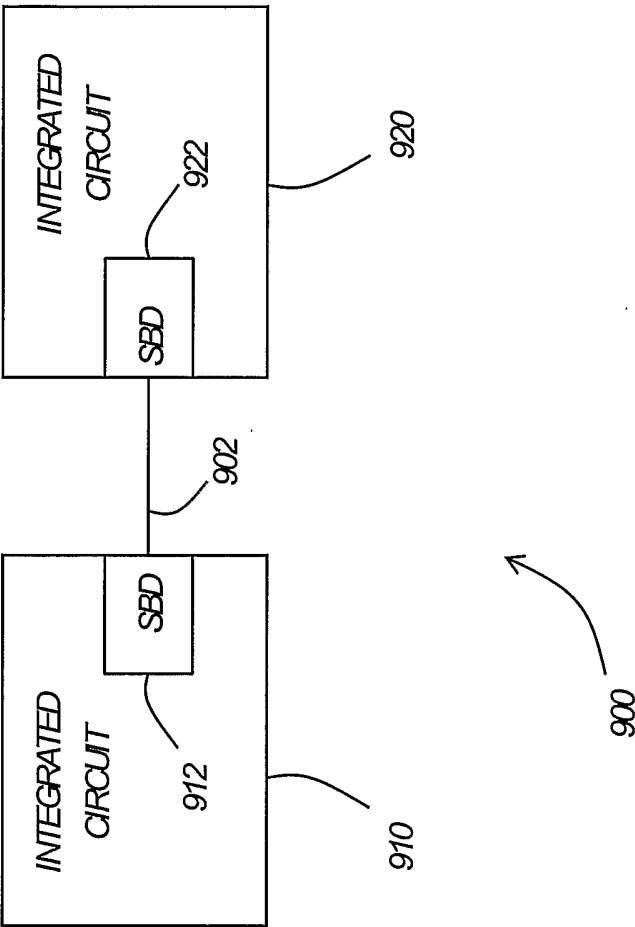


FIG. 9

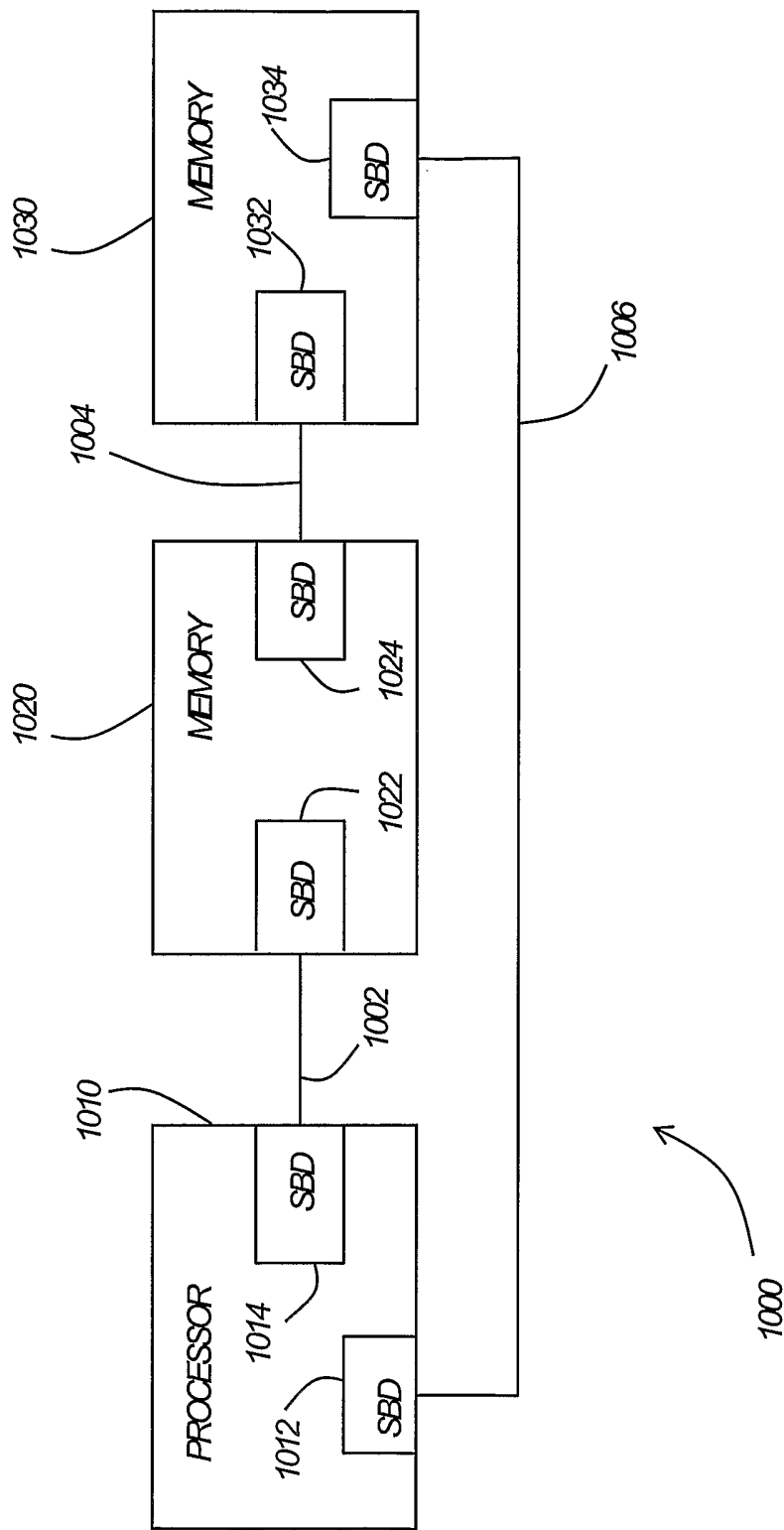


FIG. 10

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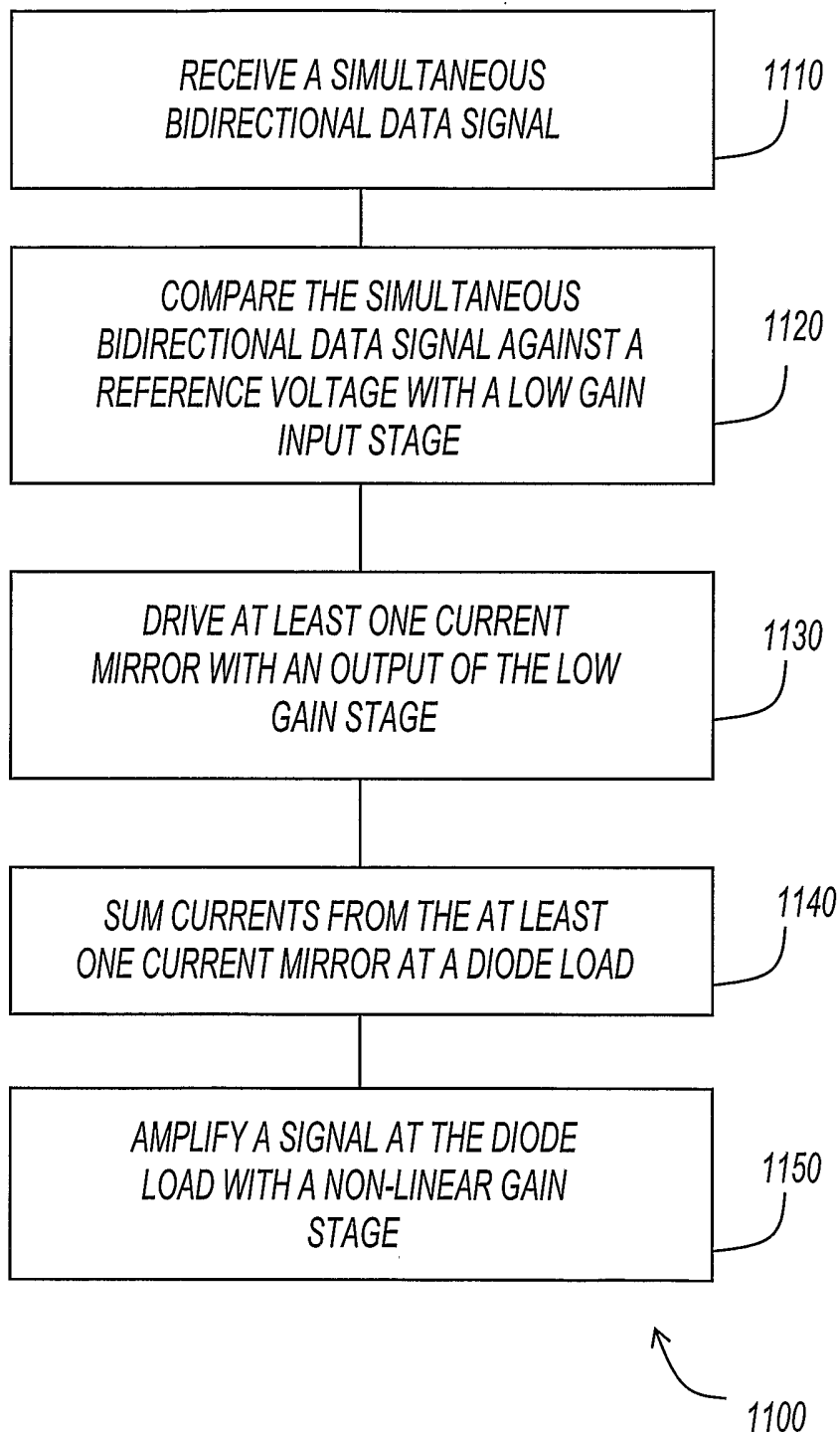


FIG. 11