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Serially Fed Flash Type Analog to Digital Converter

Technical Field

This invention relates to the field of Analog to Digital Converter (ADC), an electronic circuit, more specifically, the Flash ADC. In the Conventional Flash ADC, analog input voltage is fed to all the comparators in the Comparator Array simultaneously, which leads to large input capacitance. Whereas, in the 'Serially Fed Flash ADC', the analog input voltage signal is fed to a single node of a 'Resistor ladder' reducing the input capacitance, apart from many more other advantages.

Background Art

Analog to Digital Converter is an important interface block in most of the modern electronic circuits. There are many ADC architectures proposed for different purposes. Among them, the "Flash ADC" architecture is the fastest, because of its parallel nature. In a Conventional Flash ADC, analog to digital conversion starts with comparing simultaneously the analog input voltage V_{in} with a L number of fixed voltage levels through L comparators, ($L = 2^n$) simultaneously, which gives what is known as 'Thermometer-Code', combination of series-of-zeros and series-of-ones, e.g., 000...0011...111. Thermometer Code is then converted into One-Out-Of-N-Code and then to Binary Code. Since the analog input voltage signal is fed to all the comparators simultaneously, it leads to large input capacitance which is a major drawback of a Conventional Flash ADC along with the large silicon area. The high input capacitance, in turn, demands for pre power amplifiers to boost analog input signal power before being fed to the Comparators Array. Further, the Conventional Flash ADC contains 'analog comparators' made out of operational amplifiers. To maintain a healthy Signal to Noise Ratio(SNR), the size of operational amplifiers and in turn the MOSFETs should be made as large as possible, demanding large silicon area, which is an opposite trend to the constantly improving VLSI technologies. Thus, all the advantages of the best available VLSI

technology at a time cannot be used for fabrication of analog components. In addition, system integration is a major challenge when analog components have to be integrated into a single silicon chip along with digital components. Also, the accuracy of the Conventional Flash ADC is very much dependent on the precision of the reference DC voltage, which has to be carefully designed. In addition, in a Conventional Flash ADC, there are three conversion stages, the one, Analog to Thermometer Code, the second, Thermometer Code to One-Out-of-N-Code, and the third, One-Out-of-N-Code to Binary Code. Out of these, in the first stage, Thermometer Code is prone to be affected by bubbles due to the meta-stability errors in the comparators demanding for costly bubble error and sparkle error corrector schemes.

In this disclosure, we propose a radically different kind of Flash ADC which alleviates most of the problems of the Conventional Flash ADC. This new topology is theoretically simple, sound and instead of working around the problems of the Conventional Flash ADC, a paradigm shift in the design approach has been taken. It can be tested for preliminary functioning using simulation software like Multisim 2001 textbook version from Interactive Image Technologies Ltd.

Disclosure of the Invention

This disclosure is about a type of flash ADC, called 'Serially Fed Flash ADC', where the analog input voltage signal V_{in} is fed to a single node of a 'Resistor Ladder' consisting of L ($= 2^n$) voltage taps. Two possible Embodiments of this invention are disclosed here.

Embodiment1

In the Embodiment1, voltages tapped in the Resistor Ladder are fed to an XOR Device Array (XDA), which contains $L + 1$ XOR2 devices ($L = 2^n$). The output of the XDA is a One-Out-Of-N-Code which can be easily encoded to Binary Code.

The central working principle of the Embodiment1 of this ADC is in the 'Thresh-hold behavior' of an XOR2 device, with a 'Thresh-hold voltage', V_{th} and all the XOR2 devices in

the XDA are of the same V_{th} . If V_a and V_b are two analog inputs to an XOR2 device, then, for (i). $V_a > V_{th}$ and $V_b < V_{th}$, Similarly, for (ii). $V_a < V_{th}$ and $V_b > V_{th}$, the outputs of the XOR2 is HIGH(or 1), This is called as 'Thresh-hold behavior'. The Resistor Ladder, containing $L + 1$ resistors, is designed such that, for a step change in V_{in} by $\pm ?$, the voltage level equal to Thresh-hold voltage V_{th} of the XOR2 device climbs up or down inside the Resistor Ladder by one resistor step.

Moreover, the connection of the XOR2 devices in the XDA is also such that, at a time, only one XOR2 device shall have the voltage level equal to Thresh-hold voltage, V_{th} lying in between two of its inputs. For any other XOR2 device in the XDA, either both inputs are greater than V_{th} or both inputs are lesser than V_{th} . Thus, only one XOR2 device is at output state 1 (or HIGH) out of $L + 1$ XOR2 devices in the XDA.

This generates One-Out-Of-N-Code directly from the analog input without resorting to Thermometer Code in between, leading to faster conversion to Binary Code than in the Conventional Flash ADC.

In addition, the Resistor Ladder, XDA, and One-Out-Of-N-Code to Binary Code Converter are all digital circuits making this ADC, totally an 'All Digital ADC', which is a huge advantage for system integration into a single silicon chip, along with the digital components.

To improve the input reception and rejection capacity of the XOR2 devices in the XDA, an additional 'Buffer Array' can be inserted between the Resistor Ladder and XDA. A Buffer is nothing but two inverters cascaded together with sharper transfer characteristics and the ones used here are of Thresh-hold voltages same as the XOR2 devices in the XDA. Depending on the requirement, inside the Buffer Array, many stages of buffers can be used in cascade, forming a 'Buffer Stack'. Since, Buffer Array has the capacity to condition the voltages tapped from the Resistor Ladder into 'logically better acceptable levels' to the XOR2 devices, effectively, Buffer Array produces Thermometer Code.

Similarly, to generate Thermometer Code from the voltages tapped from the Resistor Ladder, 'AND gate Array' can also be used in the place of Buffer Array.

Main attraction of this ADC is that all the Buffers and XOR2 devices are identical in every respect, thus, increasing the 'Regularity' of the VLSI silicon chip design. There is also no demand as to what should be the Thresh-hold voltage V_{th} by this topology, rather, whatever V_{th} the best available VLSI technology at the time produces is taken. This, Thresh-hold voltage V_{th} is taken into consideration during the Resistor Ladder design.

Embodiment2

In the Embodiment2, The Resistor Ladder is same as in the Embodiment1, but, the voltages tapped in the Resistor Ladder are fed to a Comparator Array (CA), which contains L (where, $L = 2^n$) Comparators. The output of the CA is a Thermometer-Code which can be encoded to One-Out-Of-N-Code and then to Binary Code.

The central working principle of the Embodiment2 of this ADC is the Comparator Array with all the comparators connected to a single 'Thresh-hold voltage' (or 'Reference voltage'), V_{th} . As in the case of the Embodiment1, the Resistor Ladder, containing $L + 1$ resistors, is designed such that, for a step change in V_{in} by $\pm?$, the voltage level equal to Thresh-hold voltage V_{th} of the Comparator Array climbs up or down inside the resistor ladder by one resistor step.

The connection of the Comparator Array to the Resistor Ladder is also such that, as the voltage levels in successive tapping points in the ladder, $V_0, V_1, \dots, V_{(L-1)}$, raise, Thermometer Code is generated at the output of the Comparator Array. This Thermometer Code is converted into One-Out-Of-N-Code and, then to Binary Code through proper or suitable logic circuits already known to the 'skilled persons' in the 'Art'.

Resistor Ladder Design

In both the Embodiments, specification for an ADC is provided as follows, FIG 2B,

(a). n , the Resolution of the ADC in positive integers

(b). $V_{in(max)}$, in Volts, maximum analog input voltage signal

(c). V_{th} , in Volts, the Thresh-hold voltage of the XOR2 devices in the XDA (for Embodiment1) or the Comparator Array (for Embodiment2).

Then, $\Delta = \frac{V_{in(max)}}{L}$, a step change in the input voltage signal V_{in} 200 is calculated, where $L = 2^n$. Thus, the input voltage signal, V_{in} 200 is restricted to be in the range of values, $[0 \leq V_{in} \leq V_{in(max)}]$. Given, $R = [R_0 + R_1 + R_2 + \dots + R_{(L-1)} + R_{ovf}]$, the total resistance of the ladder, the resistors, $R_0, R_1, R_2, \dots, R_{(L-1)}$, and R_{ovf} , FIG 2A, the successive resistors in the ladder are calculated using the following routine, FIG 2B :

(i). Select a suitable value for R.

(ii). For $k = 0, 1, 2, 3, \dots, (L-1)$, calculate, iteratively,

$$R_k = [Z_k - Z_{(k-1)}]$$

$$\text{Where, } Z_k = \frac{(k+1)\Delta R}{(k+1)\Delta + V_{th}}, \text{ with } Z_{-1} = 0$$

(iii). $R_{ovf} = R - Z_{(L-1)}$

Brief Description of the Drawing

FIG 1, is about an n-bit Conventional Flash ADC, Prior Art

FIG 2, The Resistor Ladder in FIG 2A and the Resistor Ladder Design Calculation routine in FIG 2B

FIG 3, is about an n-bit version of Embodiment1 of the Serially Fed Flash ADC

FIG 4, is about the 3-bit version of Embodiment1 of the Serially Fed Flash ADC

FIG 5, is about an n-bit version of Embodiment2 of the Serially Fed Flash ADC

FIG 6, is about the 3-bit version of Embodiment2 of the Serially Fed Flash ADC

FIG 7, is about an n-bit version of Embodiment1 of the Serially Fed Flash ADC with additional 'Buffer Array' (BA) to improve the input reception of the 'XOR Device Array' (XDA), FIG 8, is about the 3-bit version of FIG 7

FIG 9, is about an n-bit version of Embodiment1 of the Serially Fed Flash ADC, where Full XOR2 devices of the XDA is replaced by Half XOR2 devices, FIG 10, is about the 3-bit version of FIG 9.

FIG 11, Shows the 'Thresh-hold behavior' of the XOR2 device. FIG 11a, when $V_a < V_{th}$ and V_b is varied from 0V to a final HIGH value and FIG 11b when $V_a > V_{th}$ and V_b is varied from 0V to a final HIGH value.

FIG 12, is about an n-bit version of Embodiment1 of the Serially Fed Flash ADC with additional 'AND gate Array' to improve the input reception of the 'XOR Device Array' (XDA), FIG 13, is about the 3-bit version of FIG 12

FIG 14, is about tables containing voltage tapped in the Resistor Ladder. FIG 14A,

Best mode to perform the Invention

Embodiment 1

The best mode to perform the Embodiment1 of this ADC is explained with a 3-bit case as the example, FIG 4. FIG 3 shows the n-bit version of the Embodiment1.

Consider (i). $n = 3$, the resolution of the ADC (ii). $V_{in(max)} = 10V$, maximum analog input voltage signal, V_{in} 400 (iii). $\Delta = \frac{V_{in(max)}}{L} = \frac{10}{8} = 1.25V$, a step change in the input voltage signal, V_{in} 400 (iv). $V_{th} = 2.5V$, the Thresh-hold voltage of the XOR2 devices 430-0 to 430-8 in the XDA 430, selected for illustration. These specifications work for the XOR2 gates of IC 7486 in Multisim. Thus, the input voltage signal, V_{in} 400 is restricted to be in the range of values, $[0 \leq V_{in} \leq V_{in(max)}]$. It should be understood that this restriction is only for the explanation and as such invention is applicable to any n greater than 1 and any $V_{in(max)}$ greater

than 0V and V_{th} greater than 0V. V_{th} 420, the DC voltage kept in series with V_{in} 400 in the FIG 4, is equal to the Thresh-hold voltage of the XOR2 devices 430-0 to 430-8 in the XDA 430, always.

For this specification, the values of the resistors in the Resistor Ladder 410 calculated using the routine in FIG 2B, are as follows: $R_0 = 0.3333R$, $R_1 = 0.1667R$, $R_2 = 0.1000R$, $R_3 = 0.0667R$, $R_4 = 0.0476R$, $R_5 = 0.0357R$, $R_6 = 0.0278R$, $R_7 = 0.0222R$, $R_{ovf} = 0.2000R$, where R is the total sum of all the resistors in the ladder. When V_{in} 400 takes the values in integral multiples of Δ , the voltages at different taps in the Resistor Ladder 410, $V_0, V_1, \dots, V_7$, and V_{ovf} are given in the FIG 14A. The FIG 14B shows the voltage information $V_0, V_1, \dots, V_7$, and V_{ovf} , where every voltage is compared with V_{th} 420. FIG 14C shows the levels of voltage

10 tappings in the Resistor Ladder 410 with reference to V_{th} 420 when V_{in} 400 lies in the interval $[k\Delta < V_{in} \leq (k+1)\Delta]$, for $k = 0, 1, 2, \dots, 8$ and for $V_{in} > 9\Delta$.

(1). When $V_{in} = 0V$, $V_0 = V_{th}$ 420 and all the other voltages, V_1 through V_7 , are less than V_{th} 420. But, when $0 < V_{in} \leq \Delta$, $V_0 > V_{th}$ 420 and all the other voltages, V_1 through V_7 , are less than V_{th} 420. Thus, for the XOR2 device 430-0, the V_{th} lies between its two inputs, V_0 and V_1 . For all other XOR2 devices, 430-1 through 430-7 both inputs are less than V_{th} 420. Therefore, $Y_0 = 1$, $Y_1 = 0$, $Y_2 = 0$, $Y_3 = 0$, $Y_4 = 0$, $Y_5 = 0$, $Y_6 = 0$ and $Y_7 = 0$, i.e, $Y = [1\ 0\ 0\ 0\ 0\ 0\ 0\ 0]$ 440 and $[B_0 = 0, B_1 = 0, B_2 = 0]$ 480.

(2). When $V_{in} = \Delta = 1.25V$, $V_0 > V_{th}$ 420, $V_1 = V_{th}$ 420, and all the other voltages, V_2 through V_7 , are less than V_{th} 420. But, when $\Delta < V_{in} \leq 2\Delta$, both V_0 and V_1 are greater than V_{th} 420, and all the other voltages, V_2 through V_7 , are less than V_{th} 420. Thus, for the XOR2 device 430-0 both the inputs are greater than V_{th} 420, for the XOR2 device 430-1 the V_{th} 420 lies between two of its inputs, V_1 and V_2 . For all other XOR2 devices, 430-2 through 430-7 both inputs are less than V_{th} 420. Therefore, $Y_0 = 0$, $Y_1 = 1$, $Y_2 = 0$, $Y_3 = 0$, $Y_4 = 0$, $Y_5 = 0$, $Y_6 = 0$ and $Y_7 = 0$, i.e, $Y = [0\ 1\ 0\ 0\ 0\ 0\ 0\ 0]$ 440 and $[B_0 = 0, B_1 = 0, B_2 = 1]$ 480.

(3). When $V_{in} = 2\Delta = 2.5V$, both V_0 and V_1 are greater V_{th} , $V_2 = V_{th}$ 420, and all the other voltages, V_3 through V_7 , are less than V_{th} 420. But, when $2\Delta < V_{in} \leq 3\Delta$, all the voltages V_0 through V_2 are greater than V_{th} 420, and all the other voltages, V_3 through V_7 , are less than

$V_{th} 420$. Thus, for the XOR devices 430-0 and 430-1, both the inputs are greater than $V_{th} 420$, for the XOR2 device 430-2 the $V_{th} 420$ lies between two of its inputs, V_2 and V_3 . For all other XOR2 devices, 430-3 through 430-7 both inputs are less than $V_{th} 420$. Therefore, $Y0 = 0$, $Y1 = 0$, $Y2 = 1$, $Y3 = 0$, $Y4 = 0$, $Y5 = 0$, $Y6 = 0$ and $Y7 = 0$, i.e., $Y = [0\ 0\ 1\ 0\ 0\ 0\ 0\ 0]$ 440 and [$B_0 = 0$, $B_1 = 1$, $B_2 = 0$] 480.

(4). When $V_{in} = 3? = 3.75V$, all the voltages V_0 through V_2 are greater V_{th} , $V_3 = V_{th} 420$, and all the other voltages, V_4 through V_7 , are less than $V_{th} 420$. But, when $3? < V_{in} <= 4?$, all the voltages V_0 through V_3 are greater than $V_{th} 420$, and all the other voltages, V_4 through V_7 , are less than $V_{th} 420$. Thus, for the XOR2 devices 430-0 through 430-2, both the inputs are greater than $V_{th} 420$, for the XOR2 device 430-3 the $V_{th} 420$ lies between two of its inputs, V_3 and V_4 . For all other XOR2 devices, 430-4 through 430-7 both inputs are less than $V_{th} 420$. Therefore, $Y0 = 0$, $Y1 = 0$, $Y2 = 0$, $Y3 = 1$, $Y4 = 0$, $Y5 = 0$, $Y6 = 0$ and $Y7 = 0$, i.e., $Y = [0\ 0\ 0\ 1\ 0\ 0\ 0\ 0]$ 440 and [$B_0 = 0$, $B_1 = 1$, $B_2 = 1$] 480.

(5). When $V_{in} = 4? = 5V$, all the voltages V_0 through V_3 are greater $V_{th} 420$, $V_4 = V_{th} 420$, and all the other voltages, V_5 through V_7 , are less than $V_{th} 420$. But, when $4? < V_{in} <= 5?$, all the voltages V_0 through V_4 are greater than $V_{th} 420$, and all the other voltages, V_5 through V_7 , are less than $V_{th} 420$. Thus, for the XOR2 devices 430-0 through 430-3, both the inputs are greater than $V_{th} 420$, for the XOR2 device 430-4 the $V_{th} 420$ lies between two of its inputs, V_4 and V_5 . For all other XOR2 devices, 430-5 through 430-7 both inputs are less than $V_{th} 420$. Therefore, $Y0 = 0$, $Y1 = 0$, $Y2 = 0$, $Y3 = 0$, $Y4 = 1$, $Y5 = 0$, $Y6 = 0$ and $Y7 = 0$, i.e., $Y = [0\ 0\ 0\ 0\ 1\ 0\ 0\ 0]$ 440 and [$B_0 = 1$, $B_1 = 0$, $B_2 = 0$] 480.

(6). When $V_{in} = 5? = 6.25V$, all the voltages V_0 through V_4 are greater $V_{th} 420$, $V_5 = V_{th} 420$, and both V_6 and V_7 are less than $V_{th} 420$. But, when $5? < V_{in} <= 6?$, all the voltages V_0 through V_5 are greater than $V_{th} 420$, and all the other voltages, V_6 through V_7 , are less than $V_{th} 420$. Thus, for the XOR2 devices 430-0 through 430-4, both the inputs are greater than $V_{th} 420$, for the XOR2 device 430-5 the $V_{th} 420$ lies between two of its inputs, V_5 and V_6 . For all other XOR2 devices, 430-6 through 430-7 both the inputs are less than $V_{th} 420$. Therefore, $Y0 = 0$, $Y1 = 0$, $Y2 = 0$, $Y3 = 0$, $Y4 = 0$, $Y5 = 1$, $Y6 = 0$ and $Y7 = 0$, i.e., $Y = [0\ 0\ 0\ 0\ 0\ 1\ 0\ 0]$ 440 and [$B_0 = 1$, $B_1 = 0$, $B_2 = 1$] 480.

(7). When $V_{in} = 6? = 7.5V$, all the voltages V_0 through V_5 are greater $V_{th} 420$, $V_6 = V_{th} 420$, and V_7 is less than $V_{th} 420$. But, when $6? < V_{in} \leq 7?$, all the voltages V_0 through V_6 are greater than $V_{th} 420$, and V_7 is less than $V_{th} 420$. Thus, for the XOR2 devices 430-0 through 430-5, both the inputs are greater than $V_{th} 420$, for the XOR2 device 430-6 the $V_{th} 420$ lies
 5 between two of its inputs, V_6 and V_7 . For the XOR2 device 430-7 both inputs are less than $V_{th} 420$. Therefore, $Y_0 = 0$, $Y_1 = 0$, $Y_2 = 0$, $Y_3 = 0$, $Y_4 = 0$, $Y_5 = 0$, $Y_6 = 1$ and $Y_7 = 0$, i.e, $Y = [0\ 0\ 0\ 0\ 0\ 0\ 1\ 0]$ 440 and $[B_0 = 1, B_1 = 1, B_2 = 0]$ 480.

(8). When $V_{in} = 7? = 8.75V$, all the voltages V_0 through V_6 are greater $V_{th} 420$, $V_7 = V_{th} 420$. But, when $7? < V_{in} \leq 8?$, all the voltages V_0 through V_7 are greater than $V_{th} 420$. Thus, for
 10 the XOR2 devices 430-0 through 430-6, both the inputs are greater than $V_{th} 420$, for the XOR2 device 430-7 the $V_{th} 420$ lies between two of its inputs, V_7 and $0V$ (GND). Therefore, $Y_0 = 0$, $Y_1 = 0$, $Y_2 = 0$, $Y_3 = 0$, $Y_4 = 0$, $Y_5 = 0$, $Y_6 = 0$ and $Y_7 = 1$, i.e, $Y = [0\ 0\ 0\ 0\ 0\ 0\ 0\ 1]$ 440 and $[B_0 = 1, B_1 = 1, B_2 = 1]$ 480.

(9). when $V_{in} > 8? = V_{in(max)} = 10V$, V_0 through V_7 are greater than $V_{th} 420$ and $V_{ovf} > V_{th} 420$. Now for XOR2 device 430-8, $V_{th} 420$ lies between V_{ovf} and $0V$ (GND). Therefore, $B_{ovf} = 1$, which indicate the overflow of the analog input voltage. Also, for the XOR2 device 430-7, $V_{th} 420$ lies between two of its inputs V_7 and $0V$ (GND), therefore, $Y_7 = 1$, producing the maximum possible One-Out-Of-N-Code, i.e, $Y = [0\ 0\ 0\ 0\ 0\ 0\ 0\ 1]$ and $[B_0 = 1, B_1 = 1, B_2 = 1]$.
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(10). In general, when $V_{in} 400$ is lesser than $8? = V_{in(max)} = 10V$, both the inputs of XOR2 device 430-8 are less than $V_{th} 420$, therefore, $B_{ovf} = 0$, indicating that $V_{in} 400$ is within the maximum allowed level.

The output of the XDA 430, i.e, Y 440, which is a One-Out-Of-N-Code, can be encoded to Binary Code using many possible methods already known to skilled persons in the art, one of
 25 them being, Binary ROM Encoder 450.

The internal architecture of the ROM Encoder 450 is such that to the line corresponding to Y_0 , memory cells producing the Binary Code $[B_0 = 0, B_1 = 0, B_2 = 0]$ is kept, the line corresponding to Y_1 , memory cells producing the Binary Code $[B_0 = 0, B_1 = 0, B_2 = 1]$ is

kept, to the line corresponding to Y2, memory cells producing the Binary Code [$B_0 = 0, B_1 = 1, B_2 = 0$] is kept, to the line corresponding to Y3, memory cells producing the Binary Code [$B_0 = 0, B_1 = 1, B_2 = 1$] is kept, to the line corresponding to Y4, memory cells producing the Binary Code [$B_0 = 1, B_1 = 0, B_2 = 0$] is kept, to the line corresponding to Y5, memory cells producing the Binary Code [$B_0 = 1, B_1 = 0, B_2 = 1$] is kept, to the line corresponding to Y6, memory cells producing the Binary Code [$B_0 = 1, B_1 = 1, B_2 = 0$] is kept and to the line corresponding to Y7, memory cells producing the Binary Code [$B_0 = 1, B_1 = 1, B_2 = 1$] is kept.

Very importantly, the XDA 430 need not contain full XOR2 devices, implementing $Y = \bar{a}b + a\bar{b}$, instead, Half XOR2 devices of the same V_{th} are sufficient, i.e, to implement, $Y = a\bar{b}$, as shown in the FIG 9 and FIG 10, with the working same as in FIG 3 and FIG 4 circuits. Half XOR2 devices in the place of Full XOR2 devices is sufficient for this circuit since (0,0), (1,0) and (1,1) are the only three input combinations appearing and (0,1) is never an input combination from the Resistor Ladder.

Embodiment2

In the Embodiment1, XDA can be replaced by a Comparator Array (CA) which is used in the conventional flash ADC. With this and other minor modifications, we explain the working of the best way to implement Embodiment2, with a specific example of 3-bit ADC, FIG 6. FIG 5 shows the n-bit version of the Embodiment2.

Consider (i). $n = 3$, the resolution of the ADC (ii). $V_{in(max)} = 10V$, maximum analog input voltage signal (iii). $? = V_{in(max)} / L = 10 / 8 = 1.25V$, a step change in the input voltage signal, V_{in} (iv). $V_{th} = 2.5V$, the reference voltage for the Comparator Array (selected). Thus, the input voltage signal, V_{in} is restricted to be in the range of values, [$0 \leq V_{in} \leq V_{in(max)}$]. It should be understood that this restriction is only for the explanation and as such invention is applicable to any n greater than 1 and any $V_{in(max)}$ greater than 0V and V_{th} greater than 0V.

For this specification, the resistors calculated in the Resistor Ladder 610 will be exactly same as those in the Resistor Ladder 410. It should be understood that different specifications will lead to different resistor values, but for the uniformity of this document same specification is

maintained for both the Embodiments. With this, FIGs 14A, 14B and 14C show the values of the voltage tappings as in the case of Embodiment 1.

(1). When $V_{in} = 0$, all the voltages V_0 through V_7 , are less than V_{th} . Therefore, all the Comparators 140-0 through 140-7 produce output 0. Thus, [$T0 = 1, T1 = 0, T2 = 0, T3 = 0,$
 5 $T4 = 0, T5 = 0, T6 = 0, T7 = 0$], [$O0 = 1, O1 = 0, O2 = 0, O3 = 0, O4 = 0, O5 = 0, O6 = 0,$
 $O7 = 0$] and [$B_0 = 0, B_1 = 0, B_2 = 0$]. This remains the Binary output as long as the V_{in} is less than or equal to $?$, i.e, $0 < V_{in} \leq ?$.

(2). When $V_{in} = ? = V_{th}$, $V_0 = V_{th}$, and all the other voltages, V_1 through V_7 , are less than V_{th} . But, when $? < V_{in} \leq 2?$, $V_0 > V_{th}$, and all the other voltages, V_1 through V_7 , are less than
 10 V_{th} . Therefore, Comparator 140-0 produces output 1 and all the Comparators 140-1 through 140-7 produce output 0. Thus, [$T0 = 1, T1 = 1, T2 = 0, T3 = 0, T4 = 0, T5 = 0, T6 = 0, T7 = 0$], [$O0 = 0, O1 = 1, O2 = 0, O3 = 0, O4 = 0, O5 = 0, O6 = 0, O7 = 0$] and [$B_0 = 0, B_1 = 0, B_2 = 1$].

(3). When $V_{in} = 2?$, V_0 is greater than V_{th} , $V_1 = V_{th}$, and all the other voltages, V_2 through V_7 ,
 15 are less than V_{th} . But, when $2? < V_{in} \leq 3?$, $V_1 > V_{th}$, and all the other voltages, V_2 through V_7 , are less than V_{th} . Therefore, Comparators 140-0 and 140-1 produce output 1 and all the Comparators 140-2 through 140-7 produce output 0. Thus, [$T0 = 1, T1 = 1, T2 = 1, T3 = 0,$
 $T4 = 0, T5 = 0, T6 = 0, T7 = 0$], [$O0 = 0, O1 = 0, O2 = 1, O3 = 0, O4 = 0, O5 = 0, O6 = 0,$
 $O7 = 0$] and [$B_0 = 0, B_1 = 1, B_2 = 0$].

(4). When $V_{in} = 3?$, V_0 and V_1 are greater than V_{th} , $V_2 = V_{th}$, and all the other voltages, V_3
 20 through V_7 , are less than V_{th} . But, when $3? < V_{in} \leq 4?$, $V_2 > V_{th}$, and all the other voltages, V_3 through V_7 , are less than V_{th} . Therefore, Comparators 140-0 through 140-2 produce output 1 and all the Comparators 140-3 through 140-7 produce output 0. Thus, [$T0 = 1, T1 = 1, T2 = 1, T3 = 1, T4 = 0, T5 = 0, T6 = 0, T7 = 0$], [$O0 = 0, O1 = 0, O2 = 0, O3 = 1, O4 = 0, O5 = 0, O6 = 0, O7 = 0$] and [$B_0 = 0, B_1 = 1, B_2 = 1$].

(5). When $V_{in} = 4?$, V_0 through V_2 are greater than V_{th} , $V_3 = V_{th}$, and all the other voltages, V_4 through V_7 , are less than V_{th} . But, when $4? < V_{in} \leq 5?$, $V_3 > V_{th}$, and all the other voltages, V_4 through V_7 , are less than V_{th} . Therefore, Comparators 140-0 through 140-3

produce output 1 and all the Comparators 140-4 through 140-7 produce output 0. Thus, [$T_0 = 1, T_1 = 1, T_2 = 1, T_3 = 1, T_4 = 1, T_5 = 0, T_6 = 0, T_7 = 0$], [$O_0 = 0, O_1 = 0, O_2 = 0, O_3 = 0, O_4 = 1, O_5 = 0, O_6 = 0, O_7 = 0$] and [$B_0 = 1, B_1 = 0, B_2 = 0$].

5 (6). When $V_{in} = 5?$, V_0 through V_3 are greater than V_{th} , $V_4 = V_{th}$, and all the other voltages V_5 through V_7 , are less than V_{th} . But, when $5? < V_{in} \leq 6?$, $V_4 > V_{th}$, and all the other voltages, V_5 through V_7 , are less than V_{th} . Therefore, Comparators 140-0 through 140-4 produce output 1 and all the Comparators 140-5 through 140-7 produce output 0. Thus, [$T_0 = 1, T_1 = 1, T_2 = 1, T_3 = 1, T_4 = 1, T_5 = 1, T_6 = 0, T_7 = 0$], [$O_0 = 0, O_1 = 0, O_2 = 0, O_3 = 0, O_4 = 0, O_5 = 1, O_6 = 0, O_7 = 0$] and [$B_0 = 1, B_1 = 0, B_2 = 1$].

10 (7). When $V_{in} = 6?$, V_0 through V_4 are greater than V_{th} , $V_5 = V_{th}$, V_6 and V_7 are less than V_{th} . But, when $6? < V_{in} \leq 7?$, $V_5 > V_{th}$, and V_6 and V_7 are less than V_{th} . Therefore, Comparators 140-0 through 140-5 produce output 1 and the Comparators 140-6 and 140-7 produce the output 0. Thus, [$T_0 = 1, T_1 = 1, T_2 = 1, T_3 = 1, T_4 = 1, T_5 = 1, T_6 = 1, T_7 = 0$], [$O_0 = 0, O_1 = 0, O_2 = 0, O_3 = 0, O_4 = 0, O_5 = 0, O_6 = 1, O_7 = 0$] and [$B_0 = 1, B_1 = 1, B_2 = 0$].

(8). When $V_{in} = 7?$, V_0 through V_5 are greater than V_{th} , $V_6 = V_{th}$, V_7 is less than V_{th} . But, when $7? < V_{in} \leq 8?$, $V_6 > V_{th}$. Therefore, Comparators 140-0 through 140-6 produce output 1 and comparator 140-7 produces 0. Thus, [$T_0 = 1, T_1 = 1, T_2 = 1, T_3 = 1, T_4 = 1, T_5 = 1, T_6 = 1, T_7 = 1$], [$O_0 = 0, O_1 = 0, O_2 = 0, O_3 = 0, O_4 = 0, O_5 = 0, O_6 = 0, O_7 = 1$] and [$B_0 = 1, B_1 = 1, B_2 = 1$].

(9). When $V_{in} > 8?$, Comparators 140-0 through 140-6 produce output 1. Thus, [$T_0 = 1, T_1 = 1, T_2 = 1, T_3 = 1, T_4 = 1, T_5 = 1, T_6 = 1, T_7 = 1$], [$O_0 = 0, O_1 = 0, O_2 = 0, O_3 = 0, O_4 = 0, O_5 = 0, O_6 = 0, O_7 = 1$] and [$B_0 = 1, B_1 = 1, B_2 = 1$]. In addition, $V_{ovf} > V_{th}$, therefore, comparator 140-7 produces output 1, thus $B_{ovf} = 1$, indicating the overflow of the V_{in} above the allowable maximum input voltage.

(10). In general, when $V_{in} \leq 8?$, $V_{ovf} \leq V_{th}$, therefore, $B_{ovf} = 0$, indicating that V_{in} is within the allowable maximum range.

Claims

We claim,

1. A Resistor Ladder, which is connected to a varying input voltage Signal V_{in} in series with a DC voltage V_{th} , Completing an 'Electrical Loop' containing (i) V_{th} , (ii) V_{in} and (iii) The Resistor Ladder in that sequence,

With $L+1$ series resistors (for $L > 1$) $R_0, R_1, \dots, R_{(L-1)}, R_{ovf}$, with consecutive $L+1$ voltage tappings $V_0, V_1, \dots, V_{(L-1)}, V_{ovf}$, with ' V_0 at the junction of V_{in} and the resistor R_0 ', with every, ' V_k at the junction of resistors $R_{(k-1)}$ and R_k for $k = 1, 2, 3, \dots, (L-1)$ ' and with, ' V_{ovf} at the junction of $R_{(L-1)}$ and R_{ovf} ',

10 The values of the resistors $R_0, R_1, \dots, R_{(L-1)}, R_{ovf}$, calculated such that for a selected resistor $R = R_0 + R_1 + R_2 + \dots + R_{(L-1)} + R_{ovf}$, the k^{th} resistor $R_k = [Z_k - Z_{(k-1)}]$, where $Z_k = \frac{(k+1)\Delta R}{(k+1)\Delta + V_{th}}$, with $Z_{-1} = 0$, for $k = 0, 1, 2, 3, \dots, (L-1)$, and the input step size $\Delta = \frac{V_{in(max)}}{L}$, where $V_{in(max)}$ is the maximum value of V_{in} and $R_{ovf} = [R - Z_{(L-1)}]$,

Wherein, the resistors $R_0, R_1, \dots, R_{(L-1)}, R_{ovf}$ calculated are such that for a change in V_{in} by $\pm?$, the voltage level equal to V_{th} climbs up or down inside the Resistor Ladder by one resistor step,

And, V_{th} can be an algebraic sum of many DC voltages, i.e kept or connected in series, and V_{in} can be an algebraic sum of many varying input voltage signals, i.e kept or connected in series.

20 2. An n -bit ($n > 0$) Analog to Digital Converter comprising of a Resistor Ladder and the Electrical Loop of Claim1, with L replaced by 2^n , and An Array of $L+1$ XOR2 devices (XDA), the inputs of k^{th} XOR2 device connected to voltage tappings V_k and $V_{(k+1)}$, for $k = 0, 1, \dots, (L-2)$ and the inputs of $(L-1)^{th}$ XOR2 device are connected to the voltage tapping $V_{(L-1)}$ and GND(0V), the inputs of L^{th} XOR2 device are connected to the voltage tapping V_{ovf} and GND, where the output of the XDA is an One-Out-Of-N-Code which can be encoded to

Binary Code, the output of the L^{th} XOR2 device giving B_{ovf} , the overflow indication of V_{in} over $V_{\text{in(max)}}$.

3. An Analog to Digital Converter of Claim2, where a 'Buffer Array' with $L+1$ 'Buffer stacks' is included between Resistor Ladder and the XDA, the input of every k^{th} Buffer Stack connected to voltage tapping V_k for $k = 0, 1, 2, \dots, (L-1)$ and the input of L^{th} Buffer Stack connected to V_{ovf} , and the outputs of every k^{th} and $(k+1)^{\text{th}}$ Buffer Stacks connected to the inputs of k^{th} XOR2 device in the XDA, for $k = 0, 1, 2, \dots, (L-2)$ and the inputs of $(L-1)^{\text{th}}$ XOR2 device connected to the output of $(L-1)^{\text{th}}$ Buffer Stack and GND, the inputs of L^{th} XOR2 device connected to the output of L^{th} Buffer Stack and GND.
4. An Analog to Digital Converter of Claim2, where an 'AND Gate Array' with $L+1$ two-input AND gates (AND2) is included between the Resistor Ladder and the XDA, the two inputs of every k^{th} AND2 is connected to the voltage tapping pairs $[V_k, V_{(k+1)}]$, for $k = 0, 1, 2, \dots, (L-2)$, the two inputs of the $(L-1)^{\text{th}}$ AND2 is connected to the voltage tapping $V_{(L-1)}$ and logic 1 (or HIGH), the two inputs of the L^{th} AND2 is connected to the voltage tapping V_{ovf} and logic 1 (or HIGH), The XOR devices in the XDA are connected to the outputs of the AND Gate Array as, with, the two inputs of the 0^{th} XOR2 is connected to the logic 1 (or HIGH) and the output of 0^{th} AND2, the two inputs of every k^{th} XOR2 connected to the outputs of the $(k-1)^{\text{th}}$ and k^{th} AND2 gates for $k = 1, 2, 3, \dots, L$, The output of the L^{th} XOR2 giving the output B_{ovf} , indicating the overflow of V_{in} over $V_{\text{in(max)}}$.
5. Analog to Digital Converter of Claim2 or Claim3 or Claim4, where in XOR2 device in XDA is replaced by the 'Half XOR2 Devices' implementing only the one min-term corresponding to the input combination $(1, 0)$ out of four input possibilities $(0, 0)$, $(0, 1)$, $(1, 0)$ and $(1, 1)$, i.e, $Y = a\bar{b}$
6. An n -bit ($n > 0$) Analog to Digital Converter comprising of a Resistor Ladder and the Electrical Loop of Claim1, with L replaced by 2^n , and a Comparator Array (CA) - An Array of L number of Analog Comparators, which are generally two input devices with an inverting and a non-inverting input, with inverting inputs of all the Comparators in the Array are connected to a single DC reference or Thresh-hold voltage V_{th} , and non-inverting inputs of

every k^{th} Comparator connected to the $(k+1)^{\text{th}}$ voltage tapings $V_{(k+1)}$, for $k = 0, 1, 2, \dots, (L-2)$, and the non-inverting input of $(L-1)^{\text{th}}$ Comparator connected to the voltage tapping V_{ovf} , as a whole the output of the array is taken, The output of the CA producing what are known in most of the scientific and Engineering literatures as 'Thermometer Code', which
5 can be further converted into Binary Code through proper electronic circuits and the output of the $(L-1)^{\text{th}}$ Comparator giving the overflow indication of V_{in} over $V_{\text{in(max)}}$.

PRIOR ART

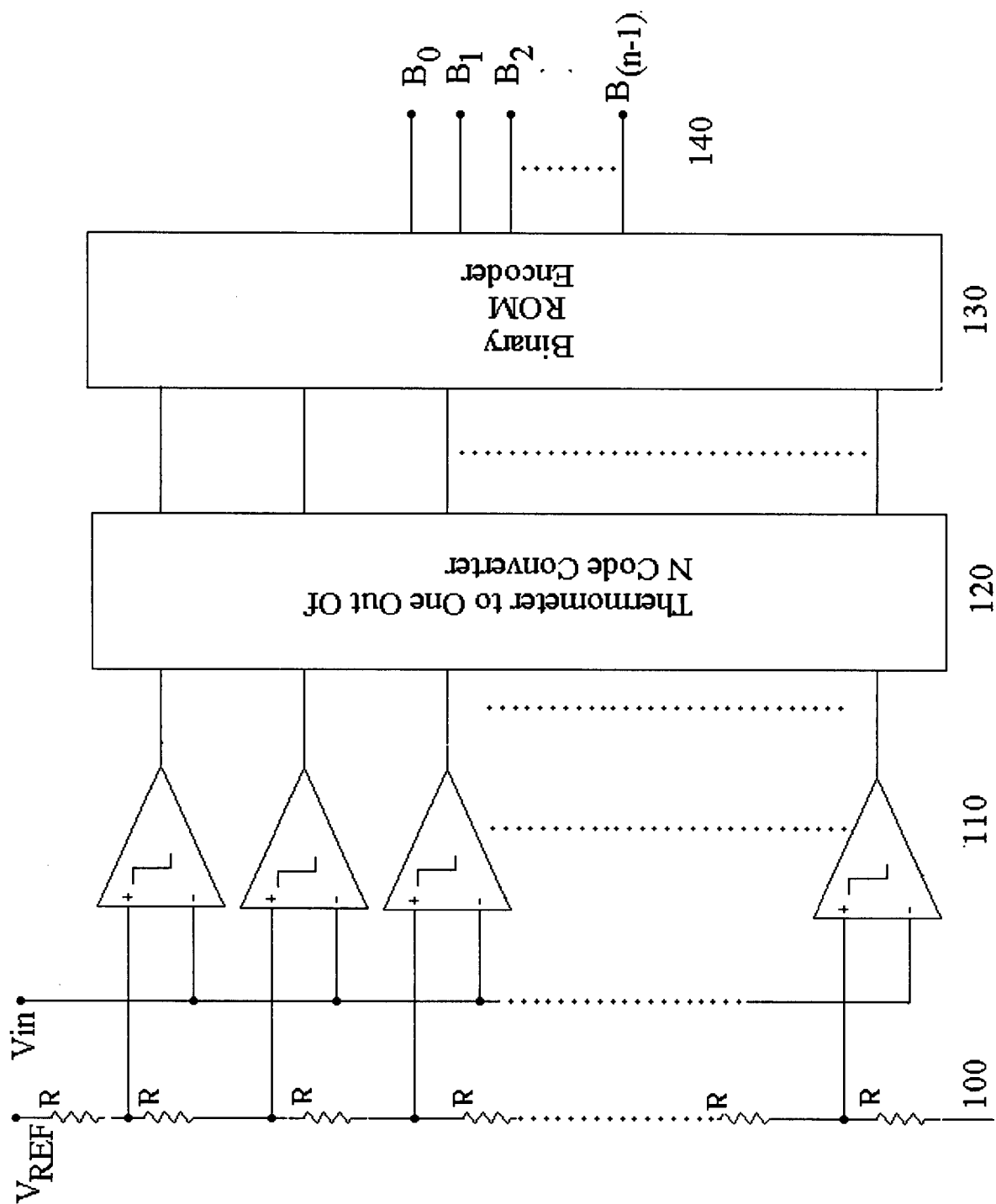


FIG 1

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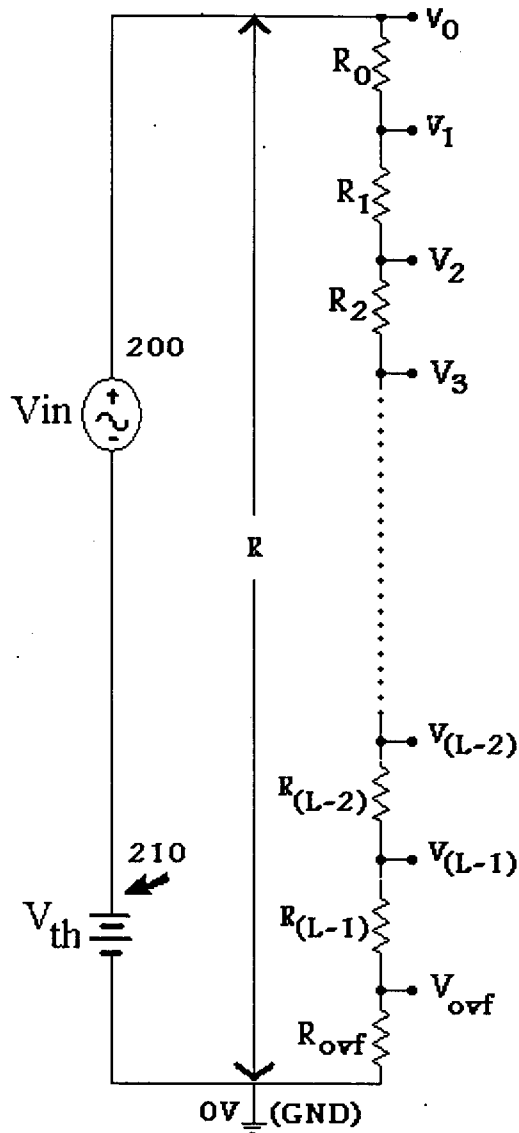


FIG 2A

Given, (a) n , The Resolution of the ADC

(b) $V_{in(max)}$, in Volts

(c) V_{th} , in Volts

(i) $\Delta = \frac{V_{in(max)}}{L}$, Where $L = 2^n$

(ii) Select a suitable value for R

(iii) For $k=0, 1, 2, 3, \dots, (L-1)$

$$R_k = [Z_k - Z_{k-1}]$$

Where

$$Z_k = \frac{[(k+1)\Delta R]}{[(k+1)\Delta + V_{th}]} \text{ with } Z_{-1} = 0$$

(iv) $R_{ovf} = R - Z_{L-1}$

FIG 2B

FIG 2

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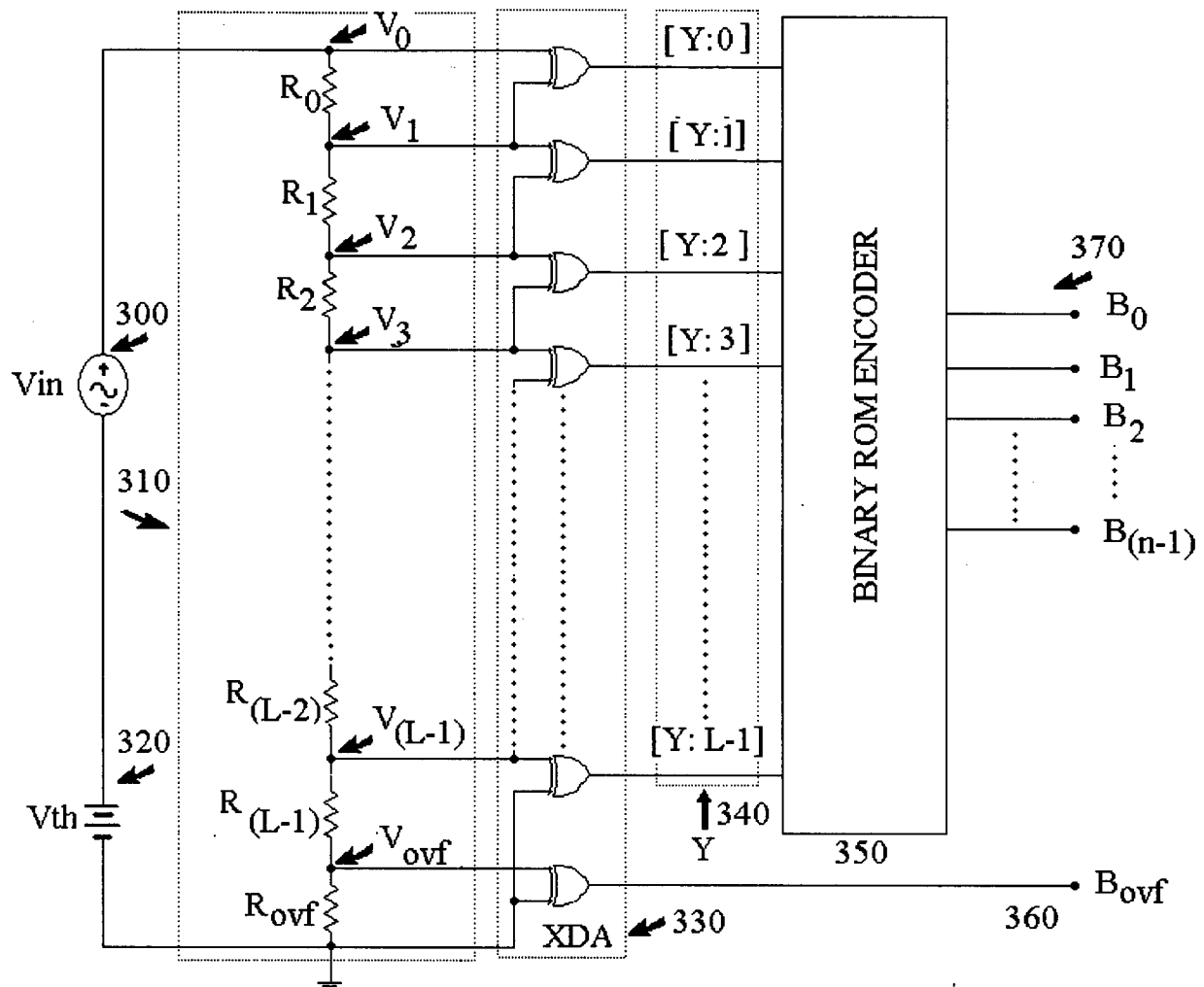


FIG 3

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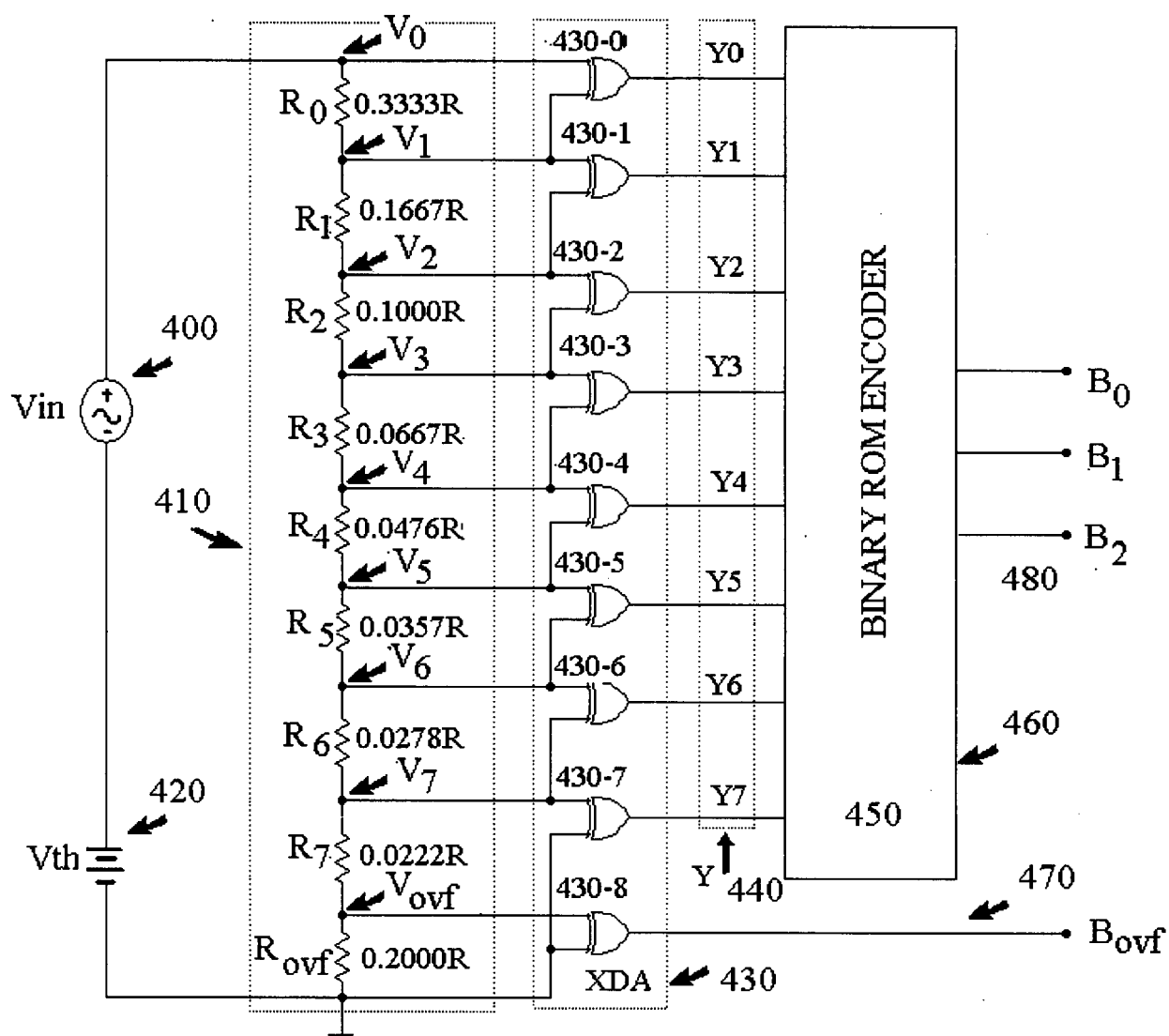


FIG 4

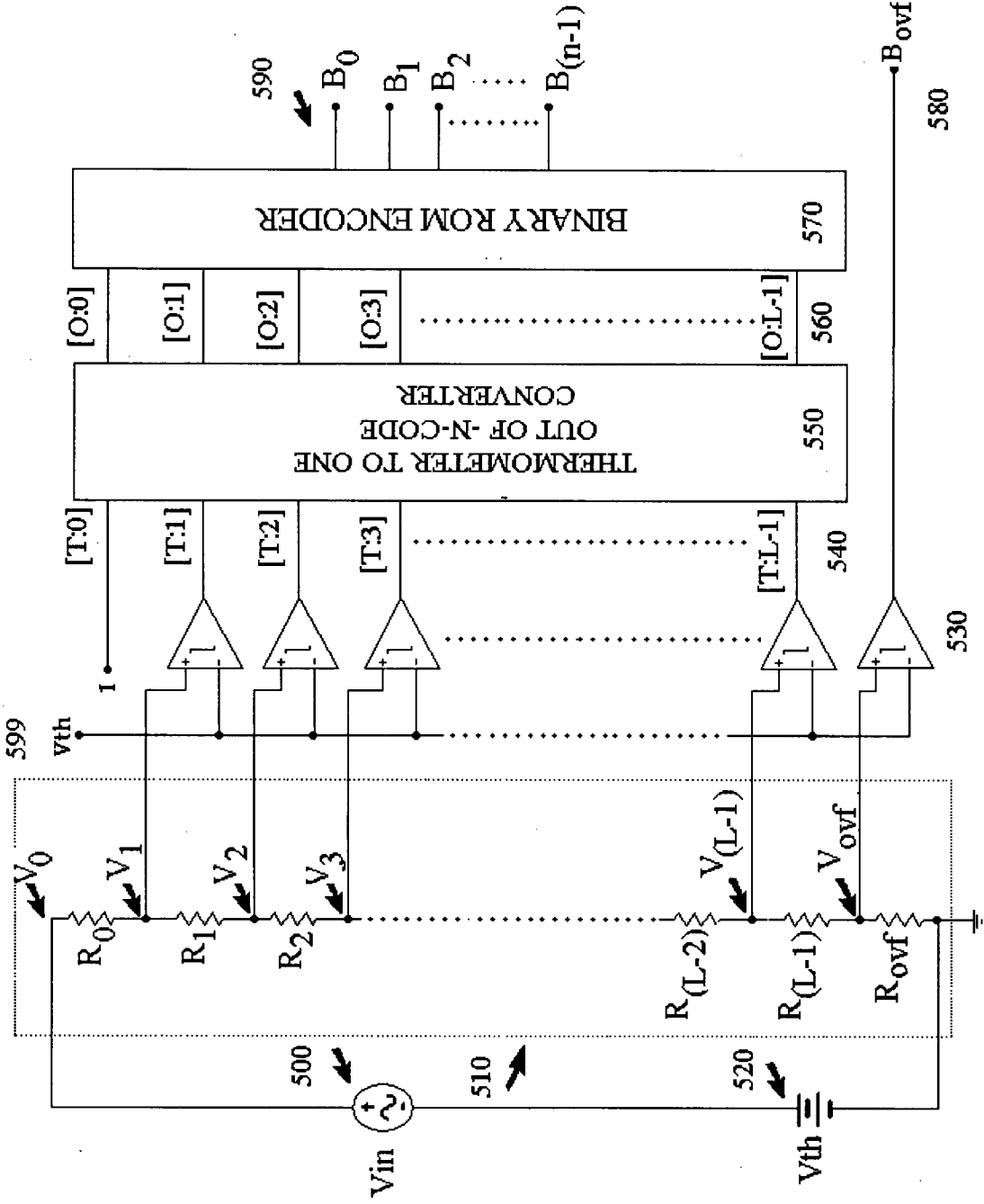


FIG 5

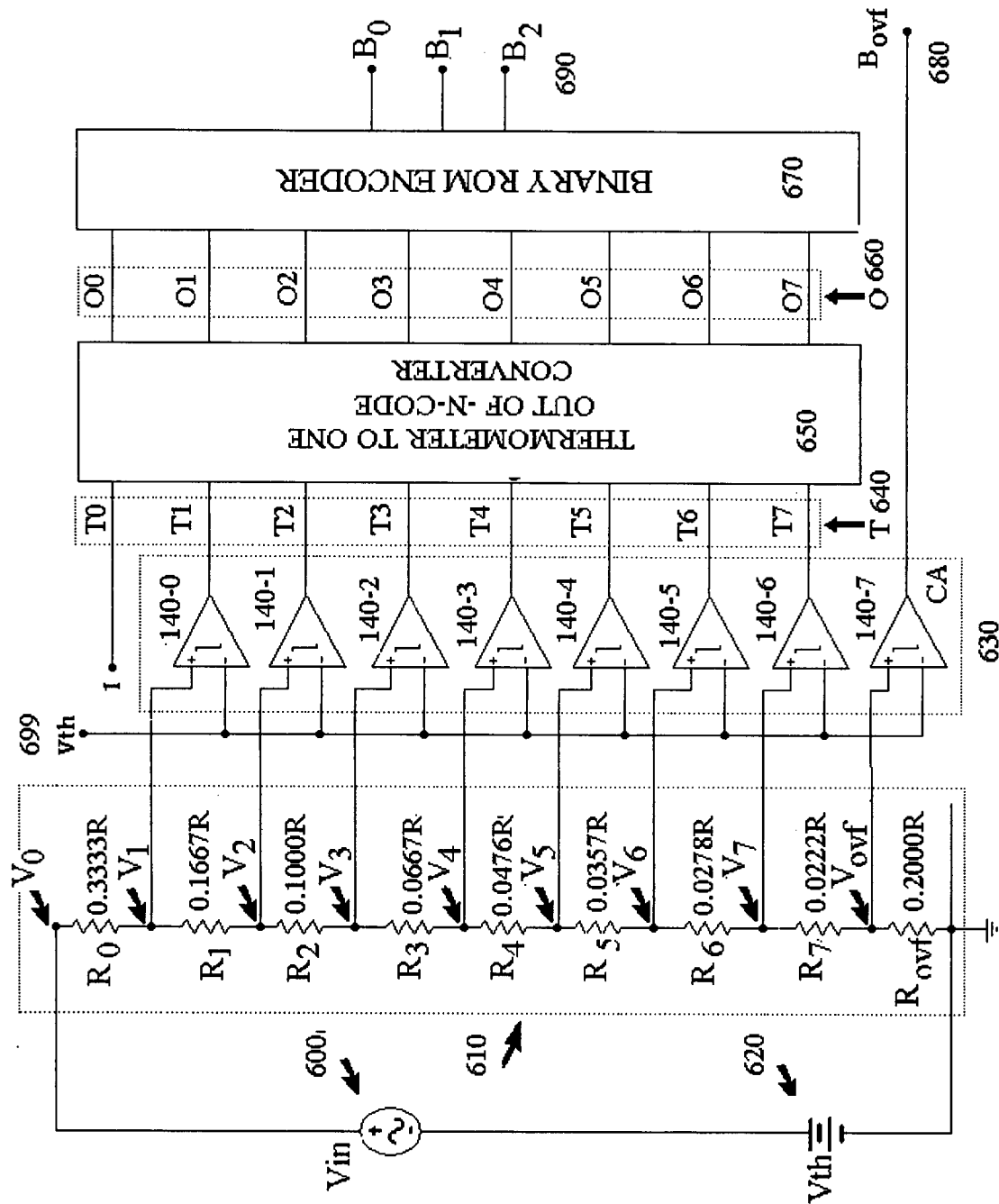


FIG 6

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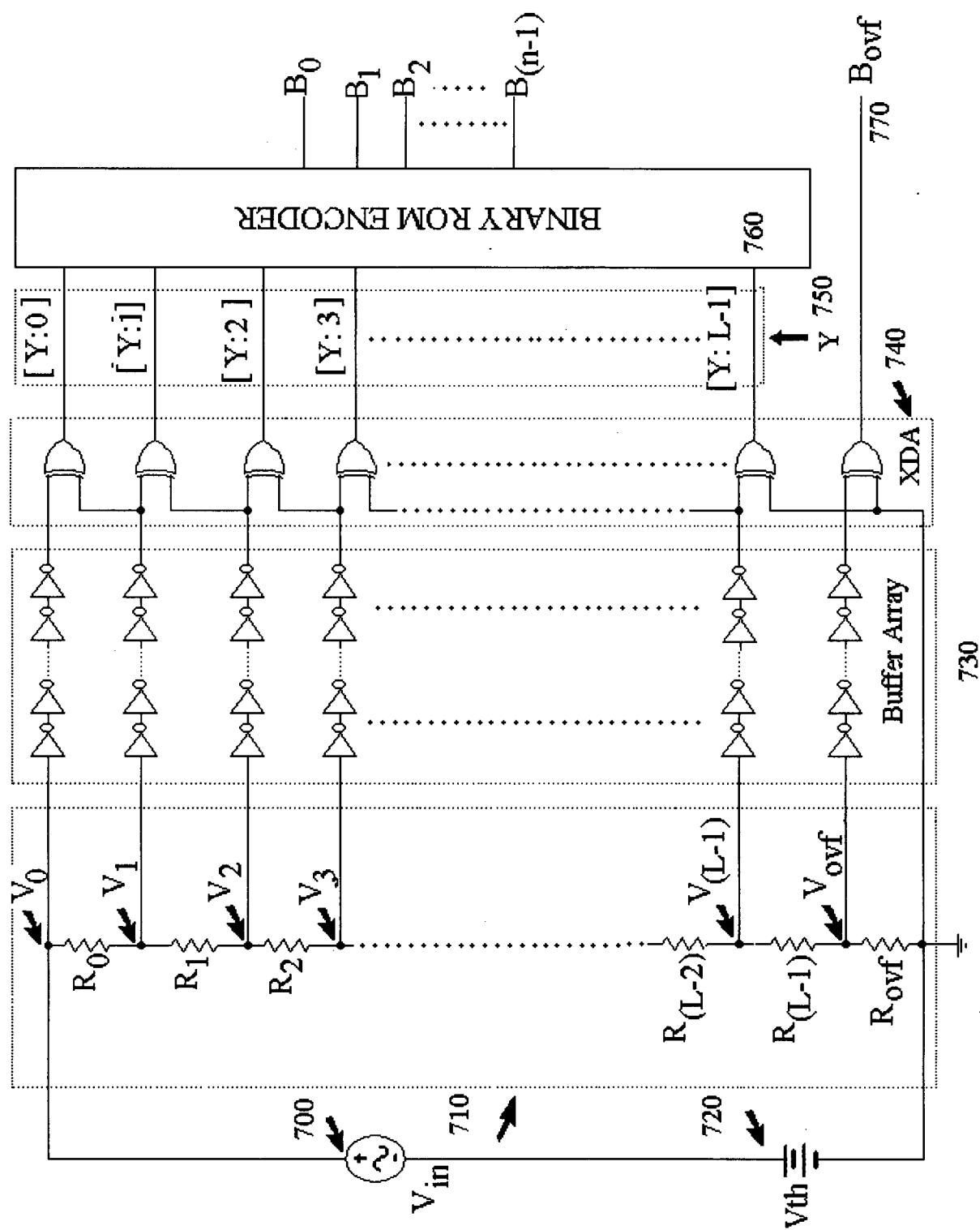


FIG 7

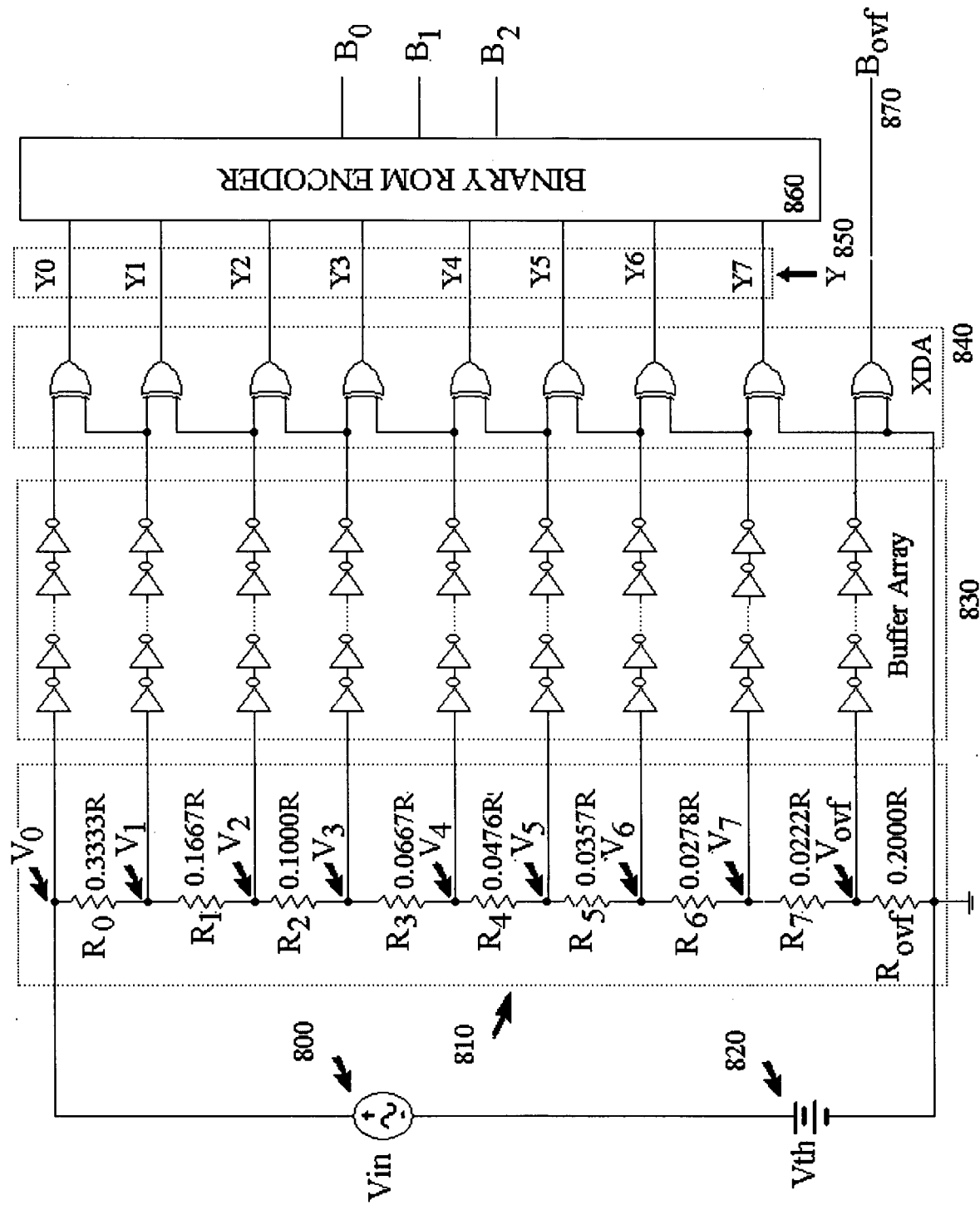


FIG 8

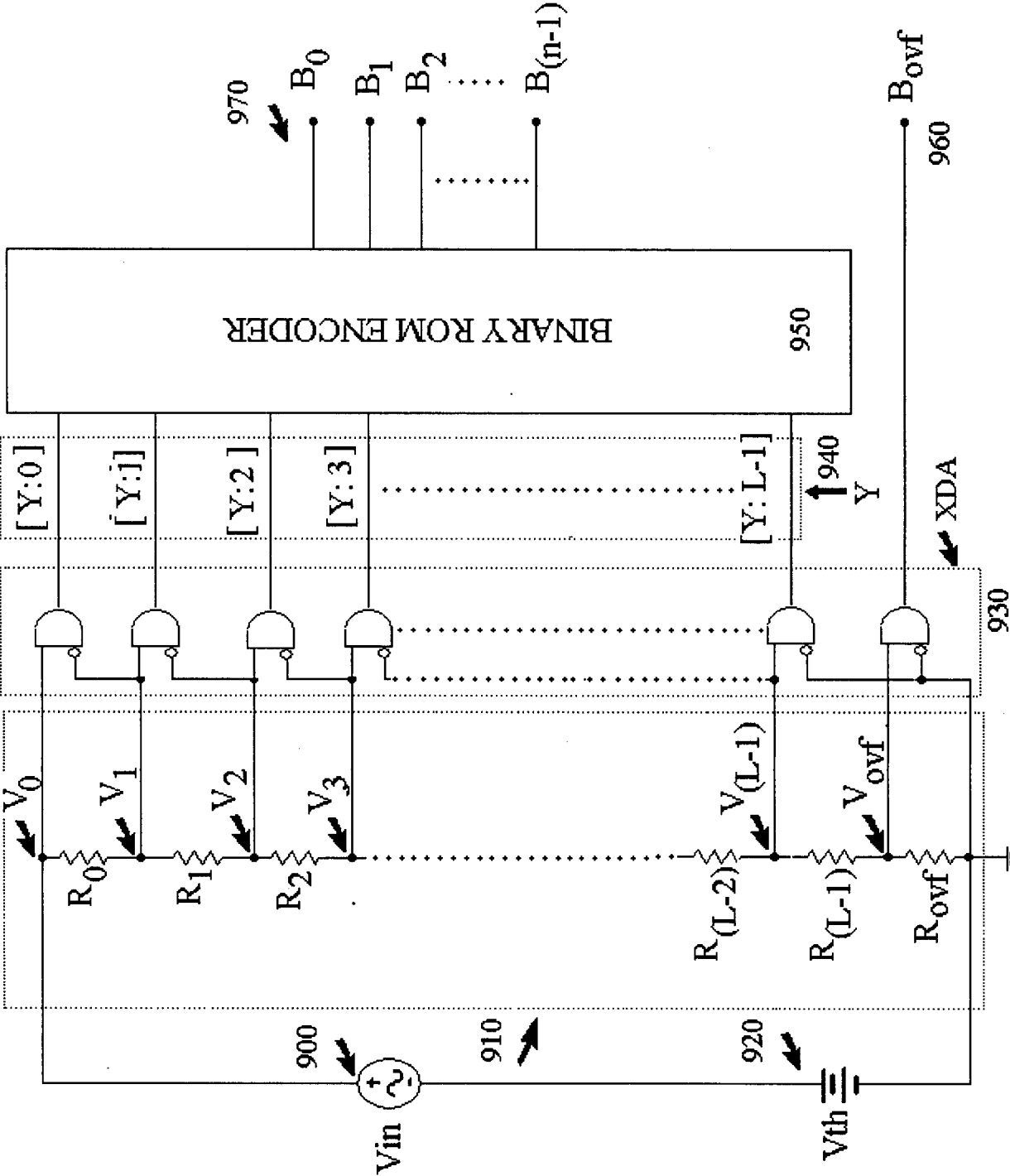


FIG 9

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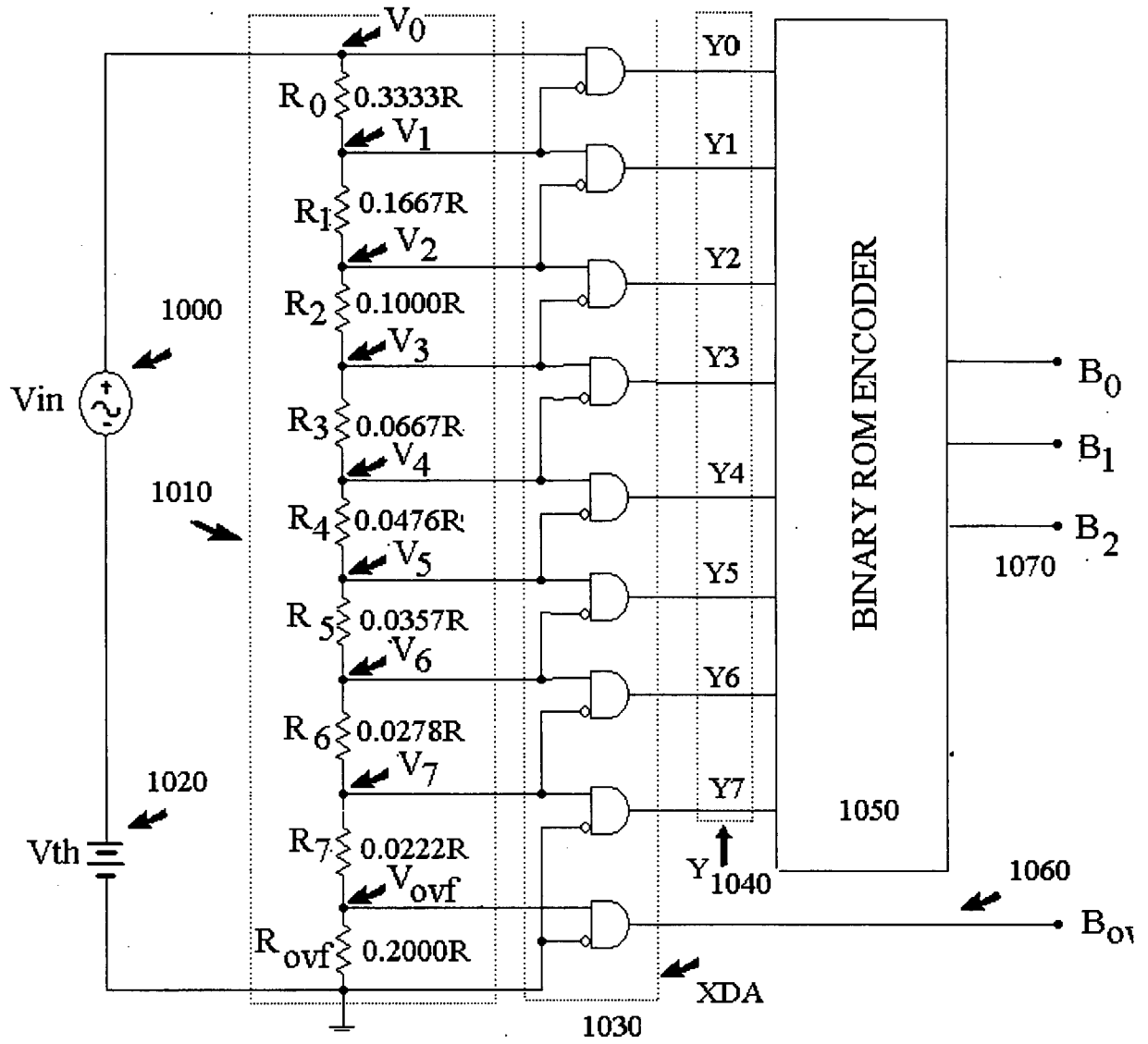


FIG 10

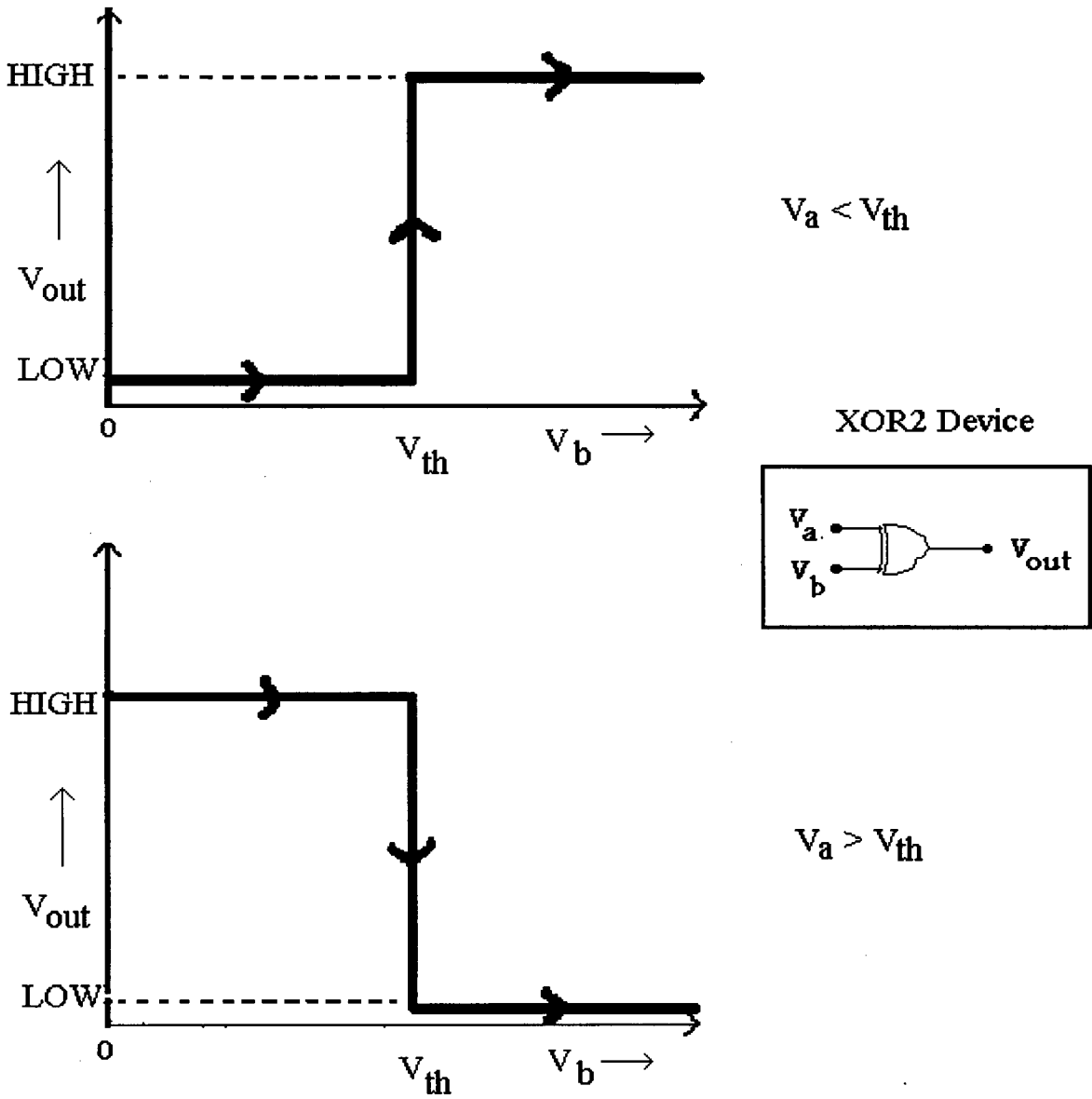


FIG 11

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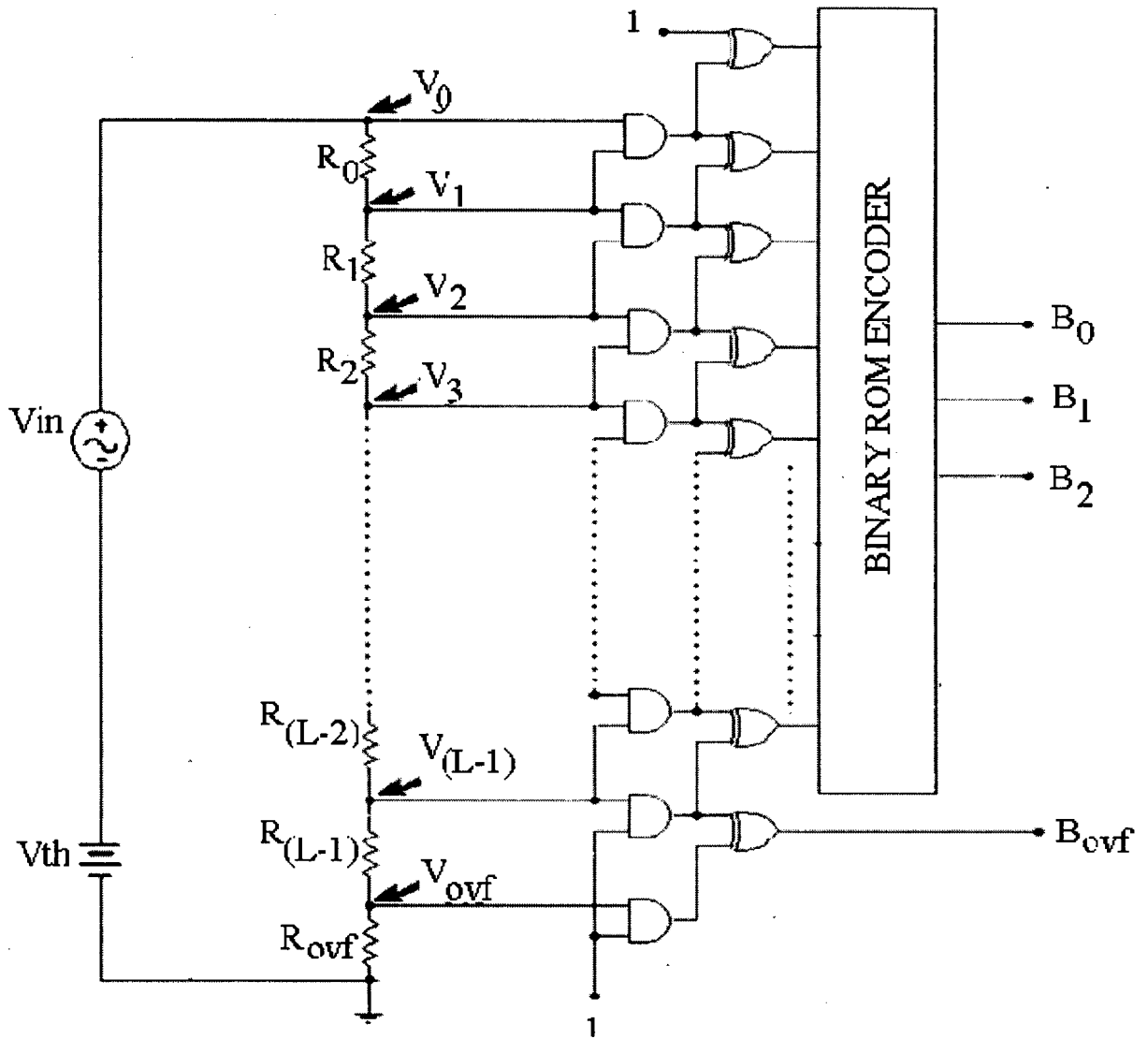


FIG 12

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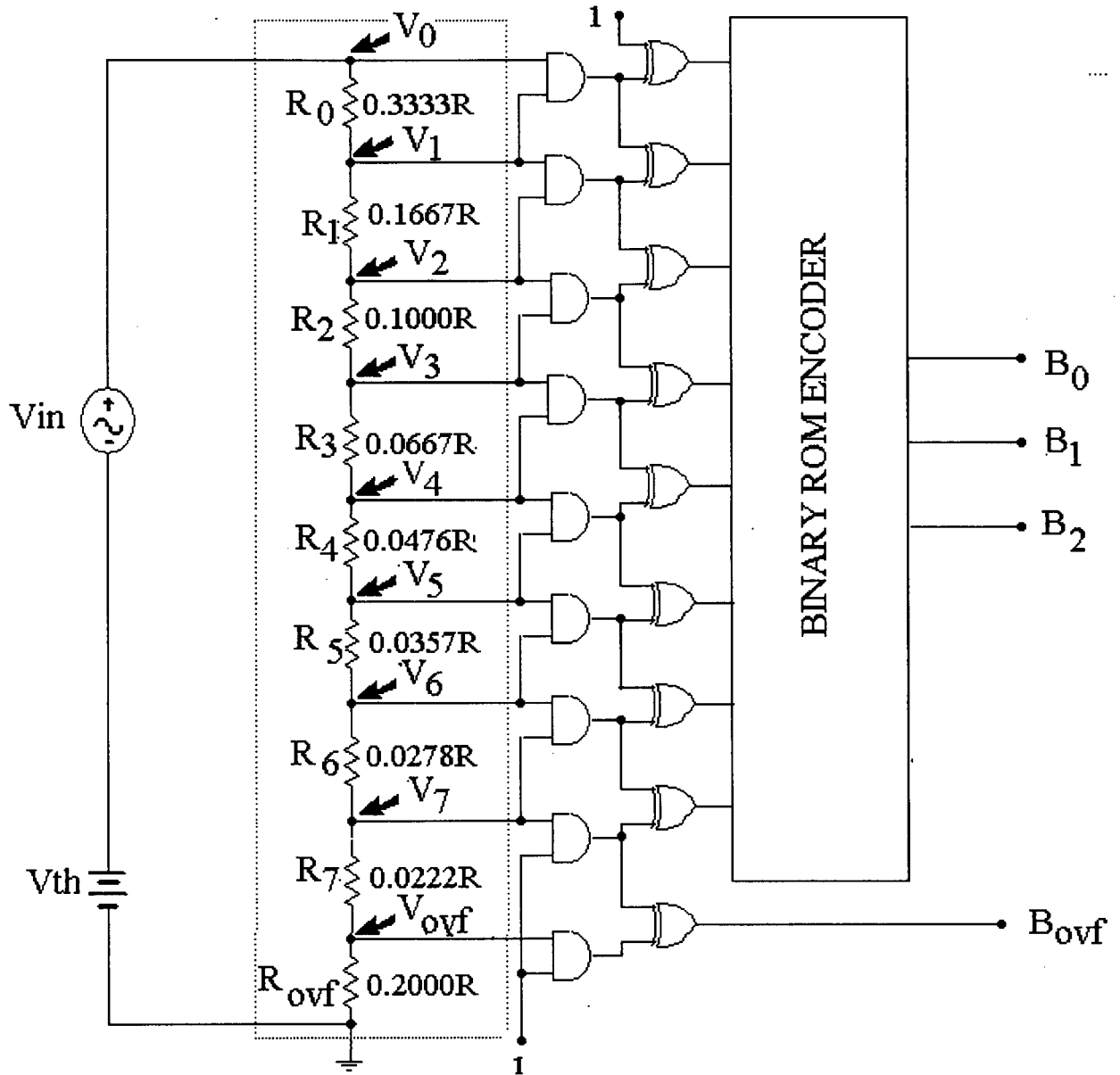


FIG 13

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V_{in}	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_{out}
0.00	2.5000	1.6667	1.2500	1.0000	0.8333	0.7143	0.6250	0.5556	0.5000
1.25	3.7500	2.5000	1.8750	1.5000	1.2500	1.0714	0.9375	0.8333	0.7500
2.50	5.000	3.3333	2.5000	2.0000	1.6667	1.4286	1.2500	1.1111	1.0000
3.75	6.2500	4.1667	3.1250	2.5000	2.0833	1.7857	1.5625	1.3889	1.2500
5.00	7.5000	5.0000	3.7500	3.0000	2.5000	2.1429	1.8750	1.6667	1.5000
6.25	8.7500	5.8333	4.3750	3.5000	2.9167	2.5000	2.1875	1.9444	1.7500
7.50	10.0000	6.6667	5.0000	4.0000	3.3333	2.8571	2.5000	2.2222	2.0000
8.75	11.2501	7.5000	5.6250	4.5000	3.7500	3.2143	2.8125	2.5000	2.2500
10.0	12.2500	8.3333	6.2500	5.0000	4.1667	3.5714	3.1250	2.7778	2.5000

FIG 14 A

V_{in}	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_{out}
0	V_{th}	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
Δ	$>V_{th}$	V_{th}	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
2Δ	$>V_{th}$	$>V_{th}$	V_{th}	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
3Δ	$>V_{th}$	$>V_{th}$	$>V_{th}$	V_{th}	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
4Δ	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	V_{th}	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
5Δ	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	V_{th}	$<V_{th}$	$<V_{th}$	$<V_{th}$
6Δ	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	V_{th}	$<V_{th}$	$<V_{th}$
7Δ	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	V_{th}	$<V_{th}$
8Δ	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	V_{th}

FIG 14 B

V_{in}	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_{out}
$0 < V_{in} \leq \Delta$	$>V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
$\Delta < V_{in} \leq 2\Delta$	$>V_{th}$	$>V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
$2\Delta < V_{in} \leq 3\Delta$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
$3\Delta < V_{in} \leq 4\Delta$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
$4\Delta < V_{in} \leq 5\Delta$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
$5\Delta < V_{in} \leq 6\Delta$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$<V_{th}$	$<V_{th}$	$<V_{th}$
$6\Delta < V_{in} \leq 7\Delta$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$<V_{th}$	$<V_{th}$
$8\Delta < V_{in} \leq 9\Delta$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$<V_{th}$
$V_{in} > 9\Delta$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$	$>V_{th}$

FIG 14 C

FIG 14

INTERNATIONAL SEARCH REPORT

International application No

PCT/IN2011/000415

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03M1/36

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M G06F H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC

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Y	the whole document	2,3,5
X	----- EP 1 780 894 A2 (IND TECHNOLOGY RES [TW]) 2 May 2007 (2007-05-02) abstract; figures 3A-3E page 3, paragraph 1 page 3, paragraph 3 - page 4, paragraph 11 page 5, paragraph 16 - page 6, paragraph 21	1,6
X	----- US 5 231 399 A (GORMAN GARY M [US] ET AL) 27 July 1993 (1993-07-27) abstract; figure 2 ----- -/-	1,6



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

3 May 2012

Date of mailing of the international search report

14/05/2012

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Brosa, Anna-Maria

INTERNATIONAL SEARCH REPORT

International application No

PCT/IN2011/000415

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