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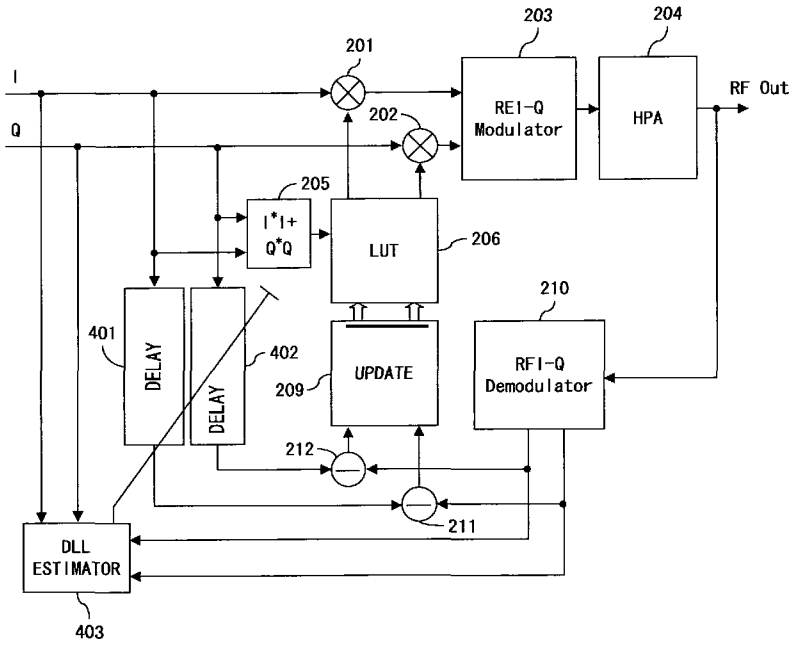
**(54) Title:** AMPLIFIER DEVICE WITH NONLINEAR-DISTORTION COMPENSATION




**(57) Abstract:** An input signal is amplified by an amplifier unit to obtain an amplified signal and delayed by a delay amount to obtain a delayed signal. A nonlinear distortion in the amplified signal is compensated for based on the amplified signal and the delayed signal. A signal delay according to the amplifier unit is estimated and the delay amount for the input signal is controlled based on an estimated signal delay.

WO 2009/011071 A1

# DESCRIPTION

## AMPLIFIER DEVICE WITH NONLINEAR-DISTORTION COMPENSATION

### Technical Field

The present invention relates to an amplifier device for adaptively compensating for a nonlinear distortion in the amplified signal.

### Background Art

High power amplifiers (HPAs) for third-generation (3G) wireless communication systems and wireless local area network (WLAN) like IEEE811.X or IEEE816.X need high linearity at the HPA output, to achieve a high adjacent channel leakage ratio (ACLR) and low error vector magnitude (EVM). In addition, high efficiency is desirable. However, when operating with high efficiency, HPAs are the most non-linear. Digital predistortion (DPD) is an efficient cost-effective means of compensating for HPA nonlinearity and retaining high efficiency.

The DPD reference design (see non-patent document 1) implements an adaptive lookup table (LUT) and applies correction values from the LUT to the incoming stream of samples. It also compares the measured output with the input, and uses this measurement to update the LUT, making the system adaptive.

For 3G and WLAN systems the DPD reference design can operate on up to four universal mobile telecommunication systems (UMTS) channels and correct 3rd and 5th order intermodulation products.

DPD is commonly used to linearize HPAs. Ideal HPAs are perfectly linear. Denoting input and output amplitude and a coefficient by $V_{IN}$, $V_{OUT}$ and $k$, respectively, their response can be described with the following equation (see line 101 in Fig. 1).

$$V_{0OT} = k\text{-}ViH \qquad (1)$$

However, real HPAs as used in wireless system exhibit some nonlinearities and eventually reach saturation. This nonlinearity can be expressed as follows by adding the term $f_{NL}$ into the equation (1), where $f_{NL}$ is used to describe the nonlinearity (see curve 102 in Fig. 1).

$$V_{OUT} = f_{NL} \cdot k \cdot V_{IN} \qquad (2)$$

The nonlinearity adversely affects the overall performance of a wireless system. It causes in-band distortion, which degrades the performance of the receiver, and out-of-band distortion, which degrades the performance of receivers in adjacent channels.

The task of the predistorter is to add predistortion before the power amplifier, which is exactly the inverse of the distortion caused by the power amplifier i.e. equals $f_{ui,}^{-1}$. When combining the predistorter with the power amplifier, the terms $f_{NL}$ and $f_{NL}^{-1}$ cancel out, and the overall system can be described by the ideal HPA equation (1).

The nonlinearity of the HPA is affected by ageing and changes in the operating environment, in particular the temperature. For this reason, the nonlinearity changes over time, and the solution should be made adaptive such that the predistorter tracks the changes in behavior of HPA.

Fig. 2 describes the basic algorithm implemented in the reference design. The incoming complex samples, in in-phase (I) and quadrature (Q) signals, have correction factors applied from LUT 206 at mixers 201 and 202 and then sent to the radio frequency (RF) I-Q modulator 203. The addresses for the LUT 206 are derived from the input power by address calculator 205. The LUT 206 must contain two values for each location - the I and Q correction factors.

In the RF I-Q modulator 203, samples are up-converted and sent to HPA 204. The HPA output is down-converted in RF I-Q

Demodulator 210, which allows us to measure the error, i.e., the difference between the input phase and magnitude, and the measured phase and magnitude at the HPA output. Obviously, delay units 207 and 208 ensure that the input is compared to the correct output value by subtractors 211 and 212. The error signals output from the subtractors 211 and 212 are used by update unit 209 to update the values currently stored in the LUT 206.

The input data signals are fed into the address calculator 205, which determines the address of the LUT values. This LUT values modify the input data signals. In the design shown in Fig. 2, only power indexing is used.

The delay units 207 and 208 delay the input I and Q signals and output the delayed signals to the subtractors 211 and 212. This delay compensates for the delay of the predistorted signal traveling to the HPA 204 and then the HPA output making its way back to the feedback processing at the subtractors 211 and 212. To synchronize the feedback HPA output with the delayed input, an elaborate delay matching scheme is reguired.

In a synchronization scheme with discrete multitone transmission described in non-patent document 2, a receiver estimates a delay and splits the delay into an integer part $J\text{-}T_{SAMPL}$ and its fractional part $\Delta$ where J and $T_{SAMPL}$ represent an integer and a sample period, respectively. The first delay $J \cdot T_{SAMPL}$ can be estimated with coarse synchronization technigue based on the periodic cyclic prefix property. Thus generally-speaking, the synchronization is performed as follows: a timing unit adjusts the sampling clock phase over $\Delta$. In addition, input data signals are delayed by J sampling clocks. Therefore there is a problem how to estimate the integer part $J\text{-}T_{SAMPL}$ -

The simplest approach for coarse integer part of delay estimation is implementation of correlator based on the cyclic prefix properties. Thus the integer part estimation with a non-data-aided maximum likelihood (ML) -based evaluation can be implemented. Because of the cyclic prefix properties this algorithm correlates the received sample sequence with a

shifted version over 2N samples of that sequence, where N represents the size of a fast Fourier transform.

Fig. 3 shows an integer part ML estimator according to such an approach. The grey area in each symbol corresponds to a cyclic prefix. This non-coherent estimator includes multipliers 301 and 302 and integrator 303, and computes correlation values between the received sample sequence and the shifted sequence for different values of J as estimation result 304. The value of J which produces the maximum correlation value results in an estimation of J.

The most problem with such an estimator is that an autocorrelation function of an orthogonal frequency division multiplexing (OFDM) signal is relatively flat. This problem becomes more serious for the oversampled OFDM signal, where the flat region of the autocorrelation function is extended over oversampled symbols. Another problem with an autocorrelation is the significant level of sidelobe because of a high peak-to-average power ratio. The significant level of sidelobe can cause a "false locking" during estimations.

Patent Document 1 relates to a delay circuit for adjusting a time difference between an input signal and an output signal of an electronic device. In the delay circuit, either one of the signal of a real number value and the signal of an imaginary number value of a coefficient corresponding to the output signal and the input signal is selected, whether to invert the sign of the selected signal and output it or to output it with the sign as is is selected, and the signal of the average value of the selected value is outputted as the time difference signal.

Patent Document 1: Japanese Patent Application Publication No. 2004-172913

Non-patent Document 1: "Digital Predistortion Reference Design," [online], [Searched June 11, 2007], Internet <URL: http://www.altera.com/literature/an/an314.pdf >

Non-patent Document 2: T. Pollet and M. Peeters,

"Synchronization with DMT Modulation," IEEE Communications Magazine, pp. 80-86, April 1999.

**Disclosure of Invention**

An object of the present invention is to synchronize a feedback signal from an amplifier output with a delayed input signal and compensate for a nonlinear distortion in the amplifier output precisely based on the feedback signal and the delayed input signal in an adaptive manner.

An amplifier device according to the present invention comprises an amplifier unit, a variable delay unit, a compensator and an estimator. The amplifier unit amplifies an input signal and outputs an amplified signal. The variable delay unit delays the input signal by a delay amount and outputs a delayed signal. The compensator compensates for a nonlinear distortion in the amplified signal based on the amplified signal and the delayed signal. The estimator estimates a signal delay according to the amplifier unit and controls the delay amount of the variable delay unit based on an estimated signal delay.

The amplifier unit, the variable delay unit and the compensator provides a modified DPD scheme with an adjustable delay amount, which is controlled by the estimator based on the estimated signal delay. According to such an amplifier device, the amplified signal which is fed back from the amplifier unit can be synchronized more precisely with the delayed signal delayed by the delay unit. Therefore, a superior compensation in the DPD reference design is performed for the nonlinear distortion.

**Brief Description of Drawings**

Fig. lisa graph showing a typical HPA AM-AM performances;

Fig. 2 is a configuration diagram showing a DPD reference design;

Fig. 3 is a circuit diagram showing a non-coherent integer part estimator;

Fig. 4 is a configuration diagram showing a HPA device according to an embodiment of the present invention;

Fig. 5 is a block diagram showing a part of a DLL estimator;

Fig. 6 is a configuration diagram showing a correlator;

Fig. 7 is a circuit diagram showing a phase removing circuit;

Fig. 8 is a configuration diagram showing an all-positive to bipolar converter; and

Fig. 9 is a graph showing simulation results of delay estimation for an OFDM signal.

**Best Mode of Carrying Out the Invention**

A best mode for carrying out the present invention is hereinafter described in detail with reference to the drawings.

Fig. 4 shows a configuration of a HPA device according to an embodiment of the present invention. This HPA device has a configuration where delay units 207 and 208 are replaced with variable delay units 401 and 402 in the configuration shown in Fig. 2 and a Delay-Locked Loop (DLL) estimator 403 is added. The HPA device is used as an OFDM transmitter in a wireless communication system and receives a reference complex signal including OFDM symbols. However, the application target of the HPA device is not limited to OFDM signal and includes signals modulated by other types of modulation method.

The DLL estimator 403 estimates a delay of the predistorted signals traveling from the mixers 201 and 202 to the HPA 204 and the HPA output signals traveling to the subtractors 211 and 212. More specifically, the DLL estimator 403 splits the delay into an integer part $J\text{-}T_{SAMPL}$ and its fractional part $\Delta$, adjusts the sampling clock phase over $\Delta$ and estimates the integer J to control the delay amount of the variable delay units 401 and 402 based on the estimated value of J.

A non-coherent integer part estimator provided in the DLL estimator 403 is realized by such a configuration shown in Fig.

5. Variable delay unit 503 delays i-th OFDM symbol in the reference complex signal by i clocks and controller 502 changes the delay amount by one clock from one OFDM symbol to the next OFDM symbol until i reaches the maximum value M (i = 0, ..., M). In this case, the maximum possible integer delay of the delay unit 503 is represented by $M\text{-}T_{SAMPL}$.

Correlator 501 calculates the mutual correlation between the delayed signal with a delay amount of i clocks and a HPA output signal for each input reference signal, and outputs the obtained correlation value Corr (i) to the controller 502. Thus, after all M+1 measurements, correlation values Corr (0) through Corr (M) are available at the controller 502. According to ML approach, the controller 502 determines a value of i corresponding to the maximum value of Corr(i) as the most reliable estimation result for J.

$$MAXO_{VERALL}\, i\,(Corr\ (i)\ , i\ ) \equiv i \approx J \qquad (3)$$

The controller 502 outputs a control signal which sets the delay amount of the delay units 401 and 402 to the estimated value.

Fig. 6 shows a configuration example of the correlator 501. This correlator includes phase removing circuits 601 and 607, subtracters 602 and 608, constant generators 603 and 609, comparators 604 and 610, multiplier 605 and integrator 606. The main idea behind this embodiment is to make the delay estimation less complex i.e. to exclude from the calculation all resource-consuming operations like multiplication and square root calculations. Therefore, such a circuit as shown in Fig. 7 is proposed for phase removing circuits 601 and 607.

This phase removing circuit comprises modulus operation circuits 701 and 702 and adder 703. In this example, the possible approximation $A = (X^2+Y^2)^{1/2} \approx |X| + |Y|$ has been employed for removing the phase dependence from the OFDM signals, where X and Y represents in-phase and quadrature signals, respectively.

The modulus operation circuits 701 and 702 output modulus |X| and |Y|, respectively and the adder 703 outputs a sum of |X| and IY I.

The subtractor 602 subtracts from the output of the phase removing circuit 601 a constant generated by the constant generator 603. The comparator 604 compares the subtraction result with zero and generates a signal indicating a sign of the subtraction result. This comparison operation is realized by a sign extraction circuit 801 as shown in Fig. 8. The sign extraction circuit 801 extracts the sign bit from a bipolar signal output from the subtractor 602 and output it to the multiplier 605.

The subtraction of the constant with the following sign extraction operation has two purposes:

(1) Making from the all-positive signal after the modulus operation a bipolar signal at the sign extraction circuit input; and

(2) Removing the amplitude modulation.

Thus, after the sign extraction operation, the new bipolar signal has a constant amplitude. Extracting the signal's sign bit make it possible to replace the multiplier 605 with a simpler logical AND circuit.

Let' s see more details about these purposes and the effect of the correlator. The amplitude of OFDM signal is an all-positive random variable with a non-zero average .According to the configuration shown in Fig. 6, in order to obtain the delay estimation result the input signal amplitude (all-positive value) has to be multiplied by the amplitude (all-positive value) of the reference signal delayed by i clocks . Multiplication itself is a very computing resource consuming operation, thus it is desirable to replace it with an alternative less complex operation, for example a logical AND. The logical AND can not operate with all-positive values, meanwhile it works well with bipolar values. Therefore, a circuit that produces a bipolar signal from the all-positive

signal is necessary.

The implementation of the circuit shown in Fig. 6 makes it possible to replace multiplication with a logical AND operation. The circuit shown in Fig. 8 represents such an "All-positive to Bipolar" converter which is a part of the circuit shown in Fig. 6.

By selecting the constant equal to the OFDM signal average amplitude, the subtractor 602 can convert the all-positive amplitude of the original OFDM signal into the bipolar signal with the zero average. The following sign extraction circuit 801 converts input all-positive input signal into the bipolar pseudo-noise like signal with constant amplitude and a sharp autocorrelation function. In fact, the sharp autocorrelation function provides the better estimation abilities. Note that after the average removing from the original signal, amplitude of the newly obtained signal is still a random variable.

The operations of the phase removing circuit 607, the subtractor 608, the constant generator 609 and the comparator 610 is same as those of the phase removing circuit 601, the subtractor 602, the constant generator 603 and the comparator 604. The multiplier 605 computes 1-bit quantization value as a logical AND between signs of the bipolar signals output from the comparators 604 and 610. The integrator 606 computes a correlation value Corr(i) by summing the logical AND values output from the multiplier 605 for a sample sequence of the i-th OFDM symbol.

As mentioned above, the sign extraction operation produces the bipolar zero-average constant amplitude signal from the original signal. This bipolar signal is very close to the pseudo-noise signal of M-sequence that amplitude has only +1 or -1 value. Because this signal is very similar to the M-sequence, such pseudo-noise like signal has a very sharp autocorrelation function. Therefore, a good integer part estimation performance is possible even without amplitude information.

Additionally, removing the amplitude modulation from the input signal significantly reduces the autocorrelation function sidelobe levels. The Non-coherent estimator based on a cyclic prefix correlation, shown in Fig. 3, is suffering from false locking. This is because the cyclic prefix is typically less than 25% of a symbol and the only cyclic prefix (small input signal portion) is used for the correlation operation in this estimator. In contrast, in the proposed estimator the whole energy of input signal can be used for the correlation operation. Therefore, the probability of the "false locking" decreases gradually.

Fig. 9 shows simulation results of delay estimation for an OFDM signal with 1024 subcarriers. horizontal and vertical axes represent the actual and estimated delay values, respectively and 12 represents an oversampling ratio (12 = 1, 2, 4). According to the simulation results, the proposed low-complexity integer part delay estimator has linear discrimination characteristic which is linear in a wide range of input integer delays. Additionally, there is no false locking that can distort the estimator's discrimination characteristic.

# CLAIMS

1. An amplifier device, comprising:

an amplifier unit operable to amplify an input signal and output an amplified signal;

a variable delay unit operable to delay the input signal by a delay amount and output a delayed signal;

a compensator operable to compensate for a nonlinear distortion in the amplified signal based on the amplified signal and the delayed signal; and

an estimator operable to estimate a signal delay according to the amplifier unit and control the delay amount of the variable delay unit based on an estimated signal delay.

2. The amplifier device according to claim 1, wherein

the compensator applies predistortion according to the input signal to the input signal before input to the amplifier unit and updates a value of the predistortion based on the amplified signal and the delayed signal, and the estimator estimates the signal delay of the input signal traveling from the compensator to the amplifier unit and coming back to the compensator as the amplified signal.

3. The amplifier device according to claim 1 or 2, wherein

the estimator removes phase dependence in the input signal and the amplified signal by a modulus operation and computes a correlation between the input signal and the amplified signal after the modulus operation to estimate the signal delay.

4. The amplifier device according to claim 3, wherein

the estimator computes a first sum of modulus of an in-phase signal and a quadrature signal included in the input signal and a second sum of modulus of an in-phase signal and a quadrature signal included in the amplified signal and

computes the correlation using the first and second sums.

5. The amplifier device according to claim 4, wherein the estimator subtracts a constant from each of the first and second sums to generate first and second subtraction results, respectively, extracts a sign from each of the first and second subtraction results to generate first and second sign information, respectively and computes the correlation using the first and second sign information.

6. The amplifier device according to claim 5, wherein the estimator computes a logical AND value between the first and second sign information and obtains the correlation by summing logical AND values for a sample sequence included in the input signal.

7. The amplifier device according to claim 5 or 6, wherein the estimator uses an average of amplitude of the input signal as the constant.

8. The amplifier device according to claim 1 or 2, wherein the estimator removes amplitude modulation from the input signal and the amplified signal and computes a correlation between the input signal and the amplified signal where the amplitude modulation is removed to estimate the signal delay.

9. A method of compensating for a nonlinear distortion in an output signal of an amplifier unit, comprising:

amplifying an input signal by the amplifier unit to obtain an amplified signal;

delaying the input signal by a delay amount to obtain a delayed signal;

compensating for a nonlinear distortion in the amplified signal based on the amplified signal and the delayed signal;

estimating a signal delay according to the amplifier

unit; and

controlling the delay amount based on an estimated signal delay.

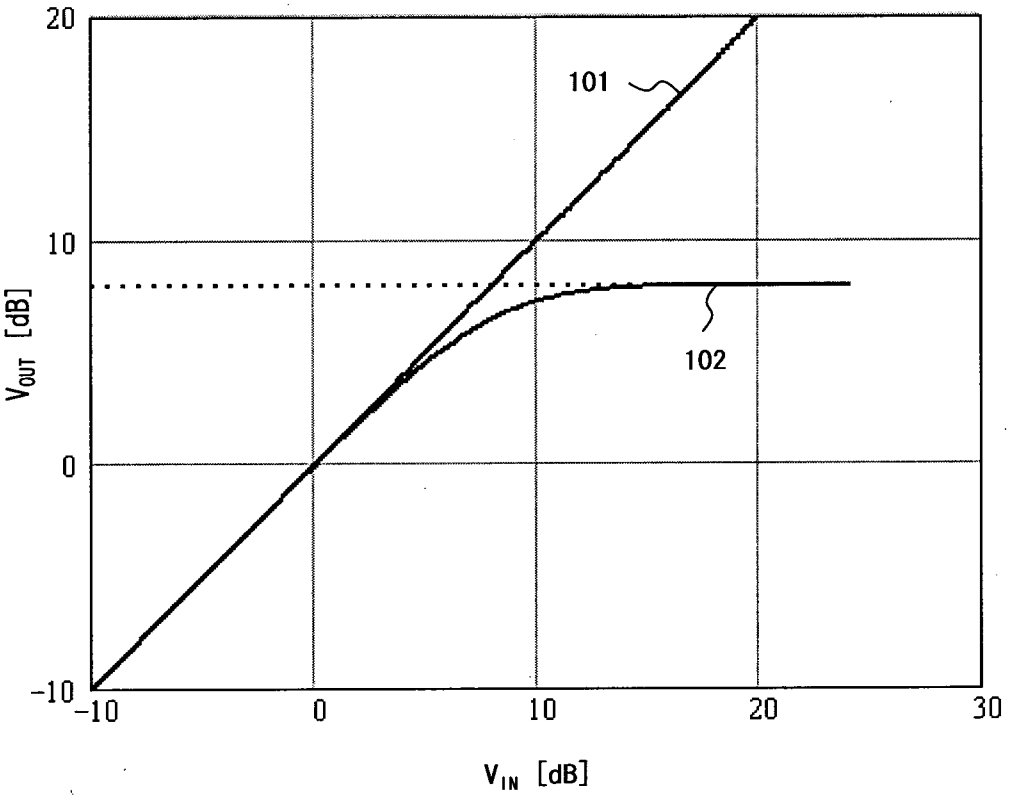



FIG. 1

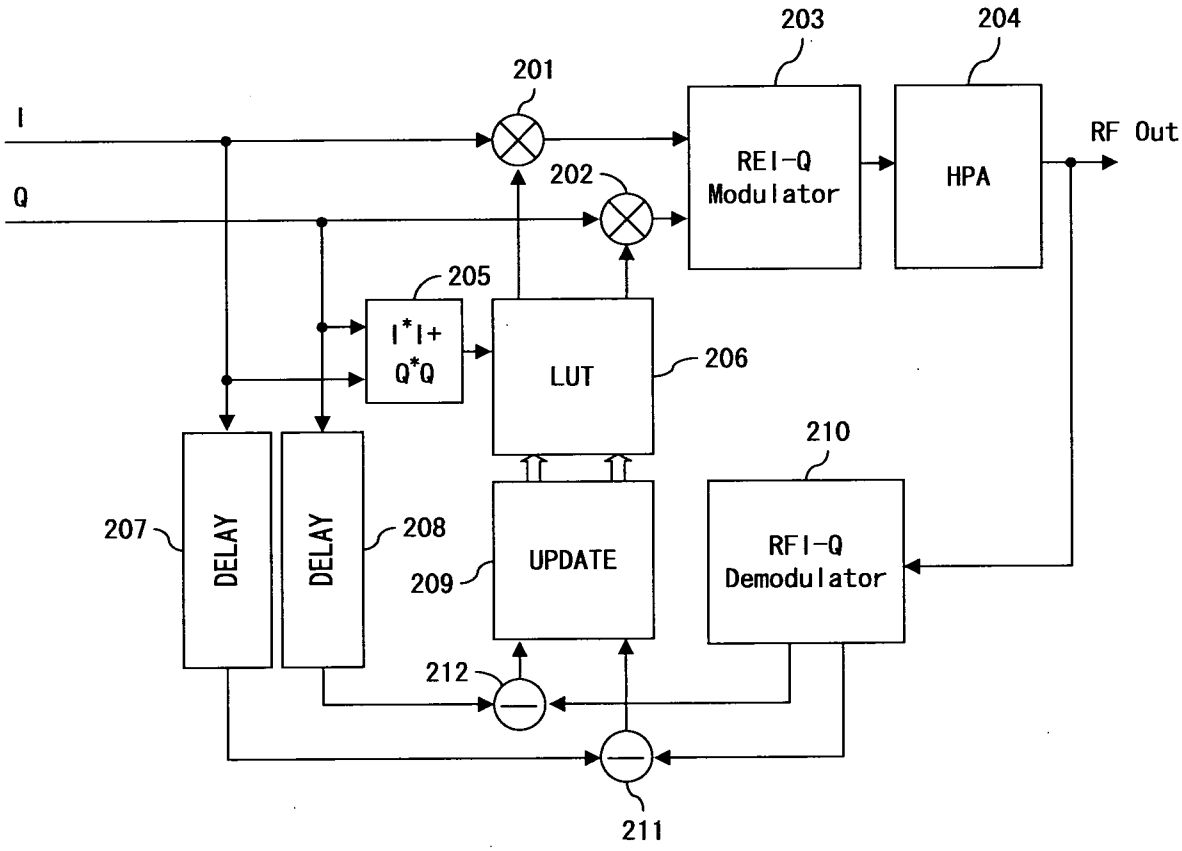

I
Q
201
202
203
204
REI-Q Modulator
HPA
RF Out
205
I*I+ Q*Q
LUT
206
210
207
DELAY
DELAY
208
209
UPDATE
RFI-Q Demodulator
212
211

FIG. 2

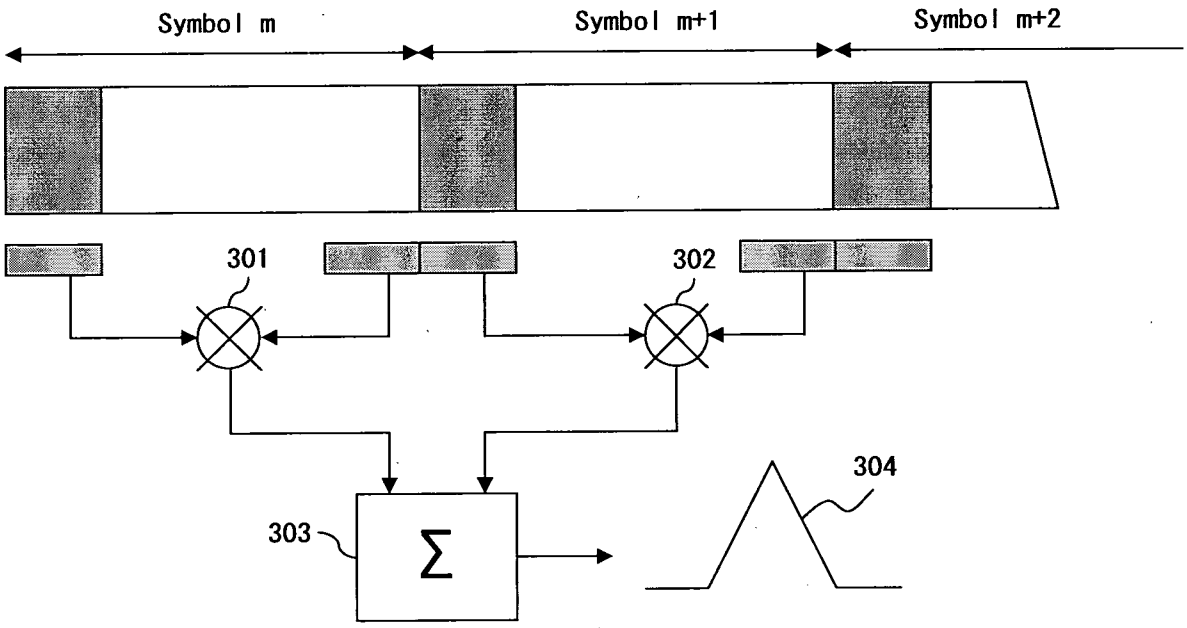



FIG. 3

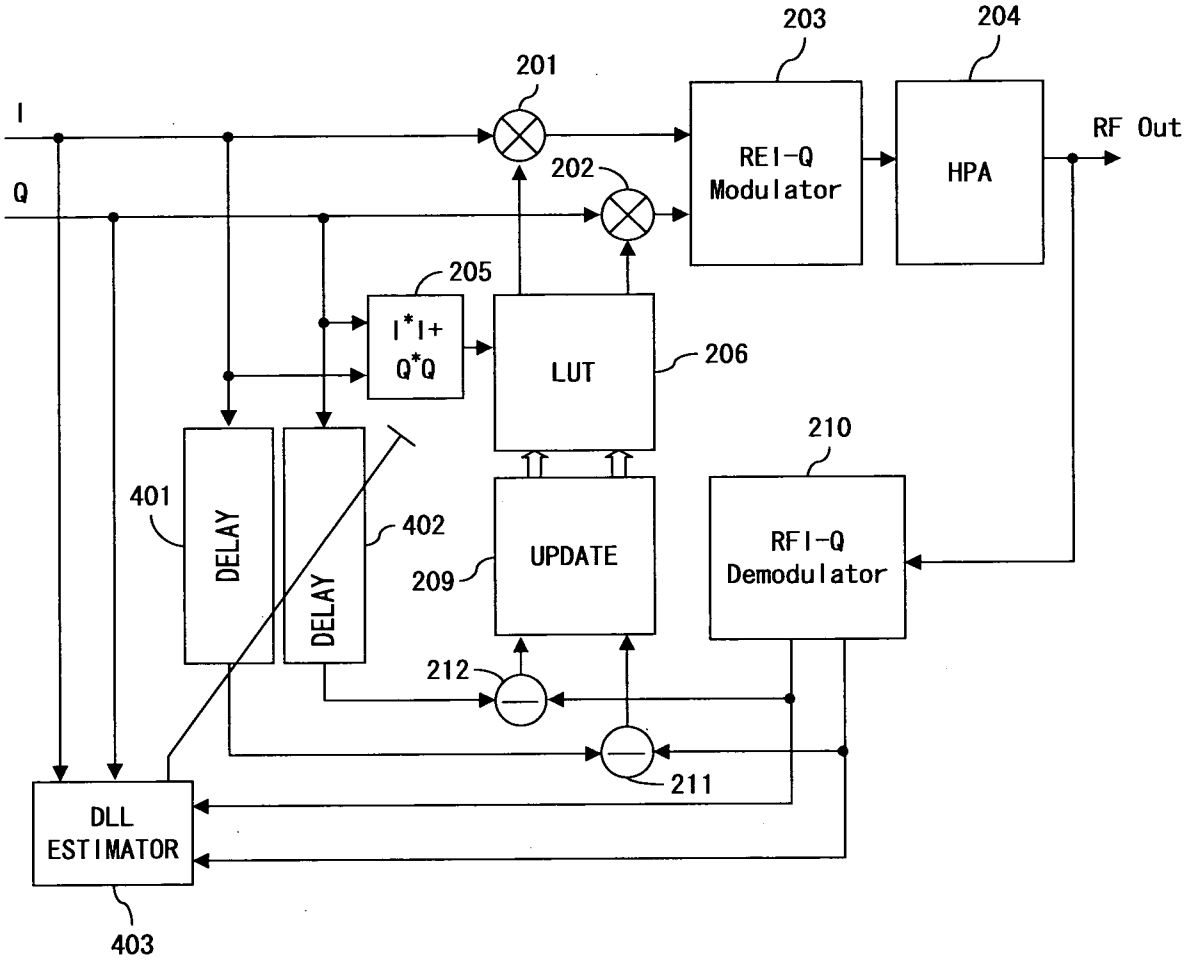

I
Q
201
202
203
REI-Q Modulator
204
HPA
RF Out
205
I*I+ Q*Q
LUT
206
210
401
DELAY
DELAY
402
UPDATE
209
RFI-Q Demodulator
212
211
DLL ESTIMATOR
403

FIG. 4

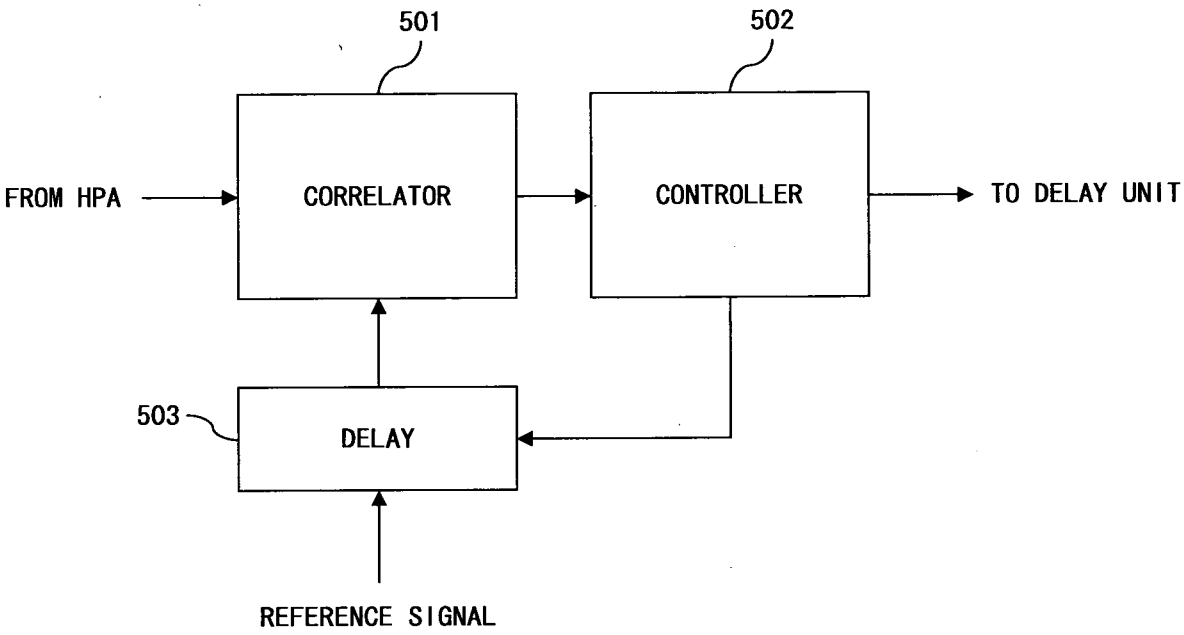

501
502
FROM HPA
CORRELATOR
CONTROLLER
TO DELAY UNIT
503
DELAY
REFERENCE SIGNAL

FIG. 5

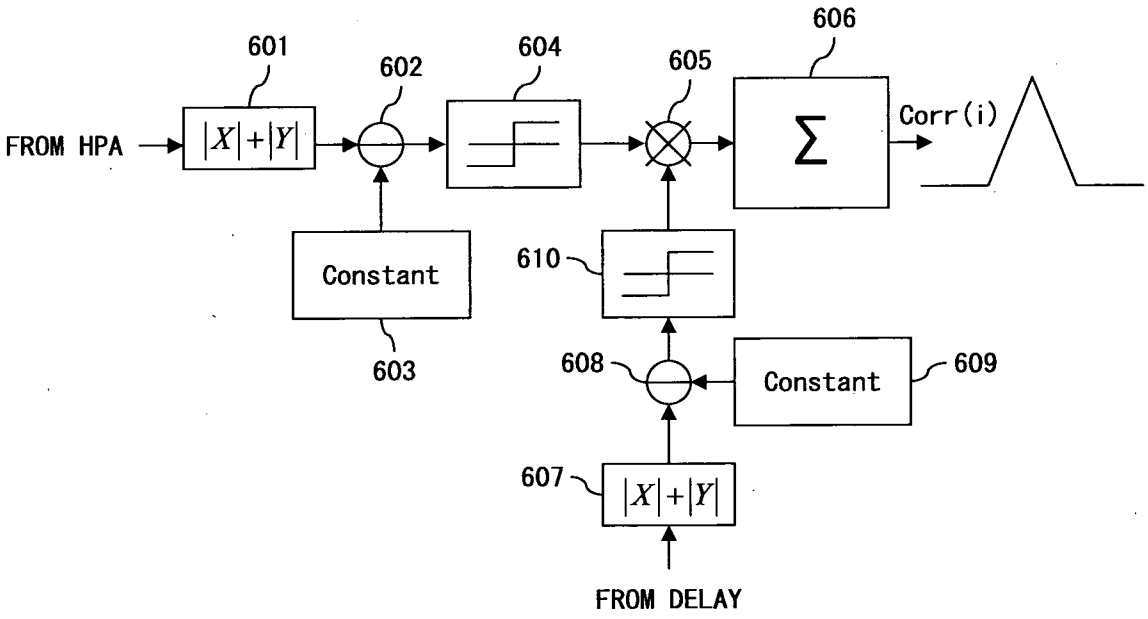

601
602
604
605
606
FROM HPA
|X|+|Y|
Σ
Corr(i)
Constant
603
610
608
Constant
609
607
|X|+|Y|
FROM DELAY

FIG. 6

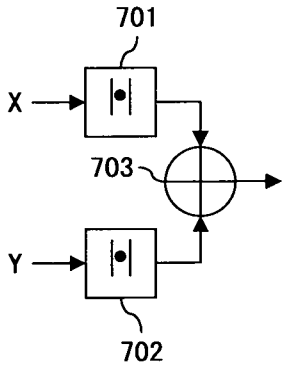



FIG. 7

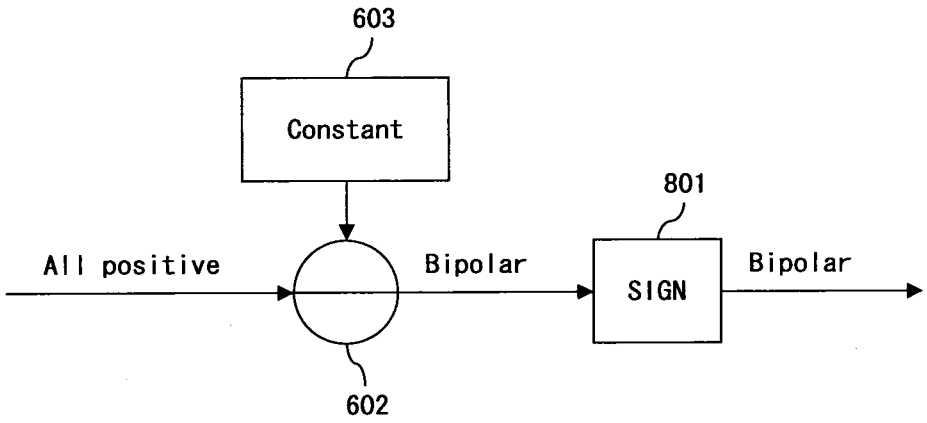



FIG. 8

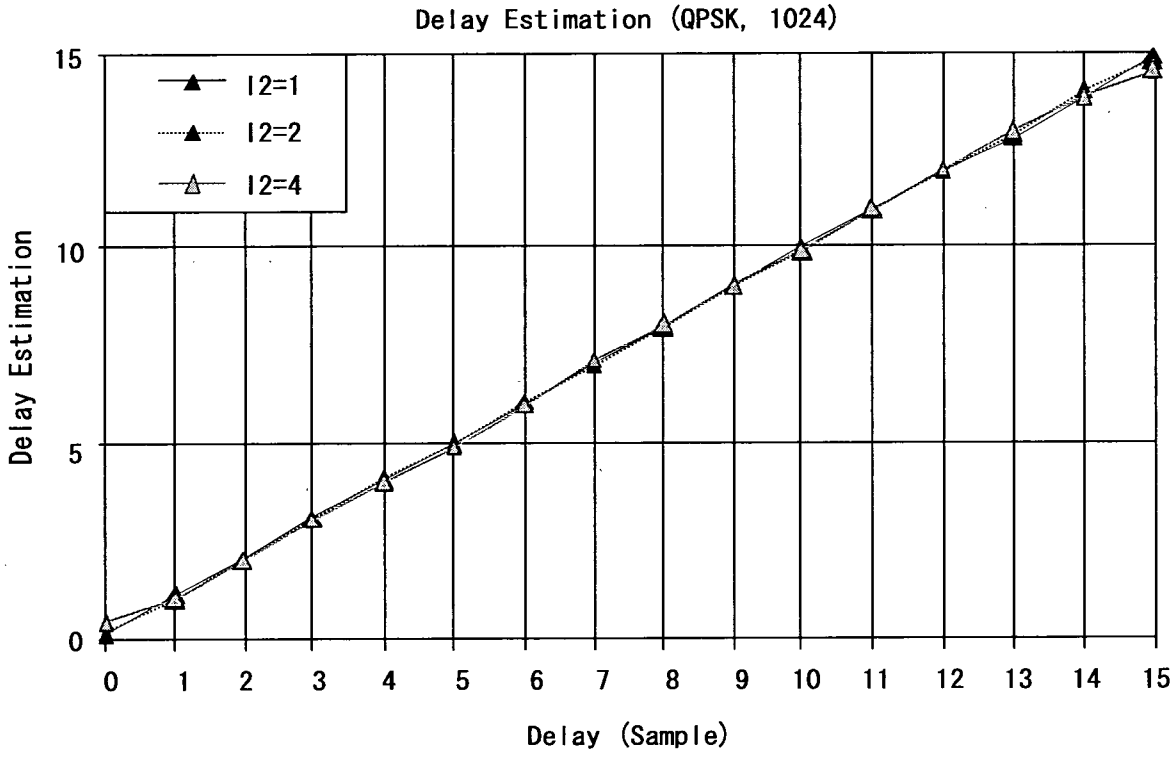

Delay Estimation (QPSK, 1024)
I2=1
I2=2
I2=4
Delay Estimation
Delay (Sample)
0
5
10
15
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

FIG. 9

# INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2007/064624

**A. CLASSIFICATION OF SUBJECT MATTER**
INV . H03F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. **FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal , WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | EP 1 511 181 A (FUJITSU LTD [JP]) 2 March 2005 (2005-03-02) paragraph [0002] - paragraph [0010]; figure 1 paragraph [0042] - paragraph [0043]; figure 7 | 1,2,9 |
| X | EP 1 089 428 A (TOKYO SHIBAURA ELECTRIC CO [JP]) 4 April 2001 (2001-04-04) paragraph [0012] - paragraph [0021]; figure 2 | 1,2,9 |
| X | US 2005/184803 Al (HIROSE NOBUO [JP] ET AL) 25 August 2005 (2005-08-25) paragraph [0095] - paragraph [0101]; figure 1 | 1,2,9 |

-/-

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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O " document referring to an oral disclosure, use, exhibition or other means

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"&' document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the International search report |
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| 27 May 2008 | 03/06/2008 |
| Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patβntlaan 2 NL - 22BO HV RiJSWiJk Tel. (+31-70) 340-2040, Tx. 31 651 epo πl, Fax: (+31-70) 340-3016 | Authorized officer Lorenzo, Carl os |

Form POT/ISA/210 (second sheet) (April 2005)

# INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2007/064624

**C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
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