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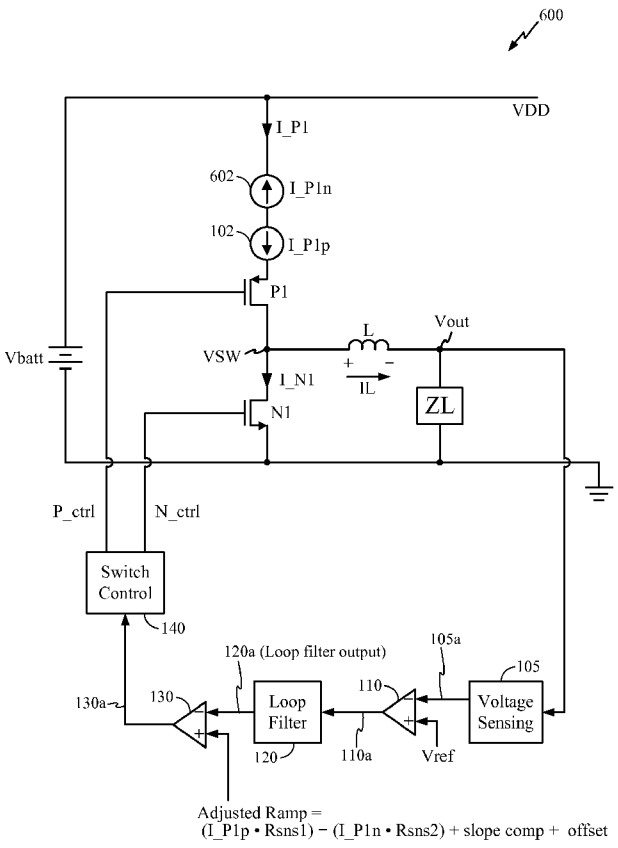
(54) Title: NEGATIVE CURRENT SENSE FEEDBACK FOR REVERSE BOOST MODE



(57) Abstract: Techniques for providing negative current information to a control loop for a buck converter in reverse boost mode. In an aspect, negative as well as positive current through an inductor is sensed and provided to adjust a ramp voltage in the control loop for the buck converter. The techniques may prevent current through the inductor during reverse boost mode from becoming increasingly negative without bound; the techniques thereby reduce settling times when the target output voltage is reduced from a first level to a second level. In an aspect, the negative current sensing may be provided by sensing negative current through a charging, or PMOS, switch of the buck converter. The sensed negative current may be subtracted from a current used to generate the ramp voltage.

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NEGATIVE CURRENT SENSE FEEDBACK FOR REVERSE BOOST MODE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This international application claims the benefit of U.S. Non-Provisional Application Serial No. 13/752,197 entitled "NEGATIVE CURRENT SENSE FEEDBACK FOR REVERSE BOOST MODE" and filed on January 28, 2013, which is expressly incorporated by reference herein in its entirety.

BACKGROUND

Field

[0002] The disclosure relates to techniques for utilizing negative current sense feedback in a buck converter.

Background

[0003] Buck converters are commonly used in electrical devices to step down a voltage from a first level (e.g., from a battery source) to a lower second level. In typical applications, buck converters source current to a load, and are not usually configured to sink current from a load. In these applications, when it is desired to decrease the target output voltage level of the buck converter, the buck converter will reduce the current sourced to the load, or stop providing current to the load, thus relying on the load to eventually discharge the output voltage to the desired value. If the load resistance is small, then it could take a long time for the output voltage to be discharged to the lower target level.

[0004] In one prior art implementation of a current mode buck converter (e.g., one that forces a continuous condition mode, or CCM), the inductor current is allowed to go negative during a "reverse boost mode." In reverse boost mode, the inductor can draw current away from the load, thereby allowing the buck converter to discharge the load more quickly. In such prior art implementations, however, the inductor current can grow increasingly negative without bound. Furthermore, when the output voltage reaches the lower target level, the negative inductor current would still need to be brought back to a positive level to drive the load. This undesirably causes undershoot, and prolongs the settling time of the system.

[0005] It would be desirable to provide techniques for configuring a buck converter in reverse boost mode to reduce output voltage undershoot and settling time during target level transitions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG 1 illustrates a prior art implementation of a buck converter.

[0007] FIG 2 illustrates exemplary signal waveforms present in the buck converter when Vfb ≈ Vref, e.g., during steady-state operation of the buck converter.

[0008] FIG 3 illustrates an exemplary implementation of the buck converter shown in FIG 1.

[0009] FIG 4 illustrates exemplary signal waveforms present in the buck converter during a transient period associated with a scenario wherein it is desired to quickly reduce Vout from a first level V1 to a second level V2 less than V1.

[0010] FIG 5 illustrates exemplary voltage and current waveforms present in the buck converter, during a transition in which the target value of Vout is brought from a first level V1 down to a second level V2 considerably less than V1.

[0011] FIG 6 illustrates an exemplary embodiment of the present disclosure, wherein negative current flow through the PMOS switch P1 is sensed and fed back to the control loop of the buck converter.

[0012] FIG 7 illustrates exemplary signal waveforms present in the buck converter during a period when Vout transitions from V1 to V2, wherein negative current through P1 is provided as feedback to the control loop described hereinabove.

[0013] FIG 8 illustrates exemplary voltage and current waveforms present in the buck converter during a transition in Vout from V1 to V2, wherein negative current through P1 is used to adjust the control loop according to the present disclosure.

[0014] FIG 9 illustrates an exemplary implementation of the buck converter in FIG 6.

[0015] FIG 10 illustrates an exemplary embodiment of a method according to the present disclosure.

DETAILED DESCRIPTION

[0016] Various aspects of the disclosure are described more fully hereinafter with reference to the accompanying drawings. This disclosure may, however, be embodied in many different forms and should not be construed as limited to any specific structure or function presented throughout this disclosure. Rather, these aspects are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art. Based on the teachings herein one skilled in the art should

appreciate that the scope of the disclosure is intended to cover any aspect of the disclosure disclosed herein, whether implemented independently of or combined with any other aspect of the disclosure. For example, an apparatus may be implemented or a method may be practiced using any number of the aspects set forth herein. In addition, the scope of the disclosure is intended to cover such an apparatus or method which is practiced using other structure, functionality, or structure and functionality in addition to or other than the various aspects of the disclosure set forth herein. It should be understood that any aspect of the disclosure disclosed herein may be embodied by one or more elements of a claim.

[0017] The detailed description set forth below in connection with the appended drawings is intended as a description of exemplary aspects of the invention and is not intended to represent the only exemplary aspects in which the invention can be practiced. The term "exemplary" used throughout this description means "serving as an example, instance, or illustration," and should not necessarily be construed as preferred or advantageous over other exemplary aspects. The detailed description includes specific details for the purpose of providing a thorough understanding of the exemplary aspects of the invention. It will be apparent to those skilled in the art that the exemplary aspects of the invention may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the novelty of the exemplary aspects presented herein. In this specification and in the claims, the terms "module" and "block" may be used interchangeably to denote an entity configured to perform the operations described.

[0018] FIG 1 illustrates a prior art implementation of a buck converter 100. Note FIG 1 is shown for illustrative purposes only, and is not meant to limit the scope of the present disclosure. For example, it will be appreciated that the techniques of the present disclosure may readily be applied to other buck converter implementations (not shown) incorporating e.g., alternative types of switches, circuit topologies, feedback configurations, etc. Such alternative exemplary embodiments are contemplated to be within the scope of the present disclosure.

[0019] In FIG 1, the buck converter 100 includes an input, e.g., a battery generating a voltage level Vbatt, and switching transistors P1 and N1 configured by a switch control block 140 to alternately charge and discharge an inductor L. The inductor is coupled to a load ZL, and current from the inductor L supports an output voltage Vout at the load. The current through P1 is labeled I_P1, and the current through N1 is labeled I_N1. A positive

current sensor 102 is further provided for sensing a positive component I_P1p of I_P1, wherein "positive" I_P1 is defined herein as flowing in the direction from P1's source to P1's drain, as labeled in FIG 1. The node coupling the drains of P1 and N1 supports a switching voltage VSW. The switch control block 140 controls the switches N1, P1 based on an input signal 130a derived from Vout, e.g., according to a control loop mechanism as further described hereinbelow.

[0020] In particular, a voltage sensing block 105 senses the output voltage Vout and generates a signal 105a (or "Vfb"). An amplifier 110 subtracts Vfb from a reference voltage Vref to generate an amplified output error signal 110a (or "Verr"). Verr is filtered by a loop filter 120 to generate signal 120a (or "Loop filter output"). Loop filter output is compared to a term "Ramp" by a PWM comparator 130. When P1 is on, Ramp may be computed as follows (Equation 1):

$$\text{Ramp} = (\text{I\_P1p} \cdot \text{Rsns1}) + \text{Slope comp} + \text{Offset};$$

wherein I_P1p is the sensed positive current through P1, Rsns1 is a resistance (not shown in FIG 1), Slope comp is a slope compensation term, and Offset is a ramp offset term.

[0021] Note during every cycle, when P1 is off, the control block 140 may reset the value of Ramp back to Offset. In particular, when P1 is off, I_P1p automatically goes to zero, while the Slope comp term may be manually reset by the control block 140. The output signal 130a of comparator 130 may be a pulse-width modulated (PWM) output voltage, or V_PWM. V_PWM is provided to the switch control block 140, which generates gate control voltages P_ctrl and N_ctrl for P1 and N1, respectively, to turn the transistor switches on and off.

[0022] It will be appreciated that the buck converter output voltage Vout may be configured to approach a target voltage level by, e.g., appropriately setting the reference voltage Vref or by adjusting the divide ratio in block 105. Note as Ramp is generated in part based on the sensed P1 current I_P1 (e.g., through the positive component I_P1p of I_P1 shown in Equation 1), the control of the buck converter 100 may also be referred to as a type of "current-mode control."

[0023] FIG 2 illustrates exemplary signal waveforms present in the buck converter 100 when Vfb $\approx$ Vref, e.g., during steady-state operation of the buck converter 100. Note FIG 2 is only meant to illustrate buck converter operation during one possible time interval and corresponding to one possible regime of operation, and is not meant to suggest any type of fixed or general relationships between the signals shown.

[0024] In FIG 2, the buck converter 100 is synchronized to a clock signal CLK, and P1 is enabled at the beginning t1 of a first cycle. From time t1 to t2, P1 is on and N1 is off. This time interval has a duration of TON, and is also denoted a "charging phase," as during this time a positive voltage drop of (Vbatt – Vout) is expected across L to charge the inductor with a positive current IL. During the charging phase, the signal Ramp is seen to increase from a level Offset at t1 up to the Loop filter output at t2, due to the increasing inductor current and also the ramping characteristics of Slope comp. Referring to FIG 1, it can be seen that at time t2, when Ramp is no longer less than Loop filter output, V_PWM will toggle from low to high.

[0025] Responsive to this toggling in V_PWM, the switch control block 140 will re-configure switches P1, N1 so that N1 is on and P1 is off, starting at t2. The interval from time t2 to t3 has a duration of TOFF, and corresponds to a "discharging phase," wherein the current IL through L decreases, i.e., IL is discharged through ground via N1. Note the interval from time t2 to t3 may correspond to an interval wherein Ramp is reset back to Offset. At t3, a new cycle of CLK begins, and the discharging phase transitions back to the charging phase.

[0026] FIG 3 illustrates an exemplary implementation 100.1 of the buck converter 100 shown in FIG 1. Note FIG 3 is shown for illustrative purpose only, and is not meant to restrict the scope of the present disclosure to any particular implementation of a buck converter or positive current sensing block shown.

[0027] In FIG 3, a positive current sensor 102.1 is provided for sensing the positive current I_P1p through P1. In particular, sensor 102.1 includes a feed-through PMOS transistor PE1 coupling the positive supply voltage (Vbatt) to a negative (-) input of an amplifier 301 when P1 is turned on. The positive (+) input of amplifier 301 is coupled to the drain voltage (VSW) of P1. In this manner, amplifier 301 generates a voltage proportional to (VSW – Vbatt) at the gate of PMOS transistor P2. A positive source-to-drain voltage drop across P1 (e.g., due to series on-resistance of P1) will thus be amplified by 301 and coupled to the gate of P2, which will generate a drain current I(I_P1p) that is a function of the positive current I_P1p through P1.

[0028] From the sensor 102.1, the generated current I(I_P1p) combines with the current Offset to generate a voltage V1 across R1 and R2. V1 is coupled to a first plate of a capacitor C1. At the same time, a current source Slope comp generates a voltage V2 at a second plate of C1. The voltage V2 between the second plate of C1 and ground, also

labeled "Ramp" in FIG 3, corresponds to the voltage Ramp that may be provided to PWM comparator 130. Note a reset switch S1 is provided to periodically reset the voltage across C1, e.g., S1 may be held in reset until the beginning of every cycle based on a control signal (not shown) generated by block 140.

[0029] It will be appreciated that by setting the reference voltage Vref at amplifier 110, or by adjusting the voltage sensing divide ratio in block 105, the duration of TON relative to TOFF may be adjusted such that Vout is configured to approach a desired target level. In particular, when it is desired to decrease Vout, TON may be decreased (and TOFF increased), thereby reducing the current IL delivered to the load each cycle. Conversely, when it is desired to increase Vout, TON may be increased (and TOFF decreased), thereby increasing the current IL delivered to the load each cycle.

[0030] To rapidly reduce Vout, N1 is enabled to discharge Vout. In certain cases, there may then be a large negative voltage applied across the inductor, causing the inductor current to quickly ramp down. If N1 is enabled for a long enough duration, then the inductor current flow may eventually become net negative. In certain implementations of buck converters, to prevent negative current flow through the inductor L, N1 is automatically disabled once the current IL becomes negative, at which point P1 and N1 are both turned off. In this event, if it is desired to further reduce the output voltage Vout, then the load ZL is relied upon to discharge the output voltage Vout, as there is no other significant current discharge path available. Note if the load impedance ZL is small, then it may take a long time for Vout to reach the final target value.

[0031] In certain implementations, to increase the rate at which Vout may be reduced, the inductor current IL may be allowed to become negative, i.e., the inductor L may sink current IL from the load ZL through ground. This mode of operation is also known as a "forced continuous condition mode (CCM)" or "reverse boost mode" of the buck converter. Note that during reverse boost mode, IL may flow from ZL through N1 through ground when N1 is on. Furthermore, IL may flow from Vout through P1 through Vbatt when P1 is on. In effect, when N1 is on and P1 is off, and the inductor current is negative, then energy is transferred from the load into the inductor. Subsequently, when N1 is off and P1 is on, the energy stored in the inductor is returned to the input, e.g., the battery.

[0032] FIG 4 illustrates exemplary signal waveforms present in the buck converter 100 during a transient period associated with a scenario wherein Vout is reduced from a first level V1 to a second level V2 less than V1. In particular, Vref may be set to a value less

than the sampled voltage Vfb, causing Loop filter output to be less than Ramp. In this case, the charging phase will only last for a minimum duration TON' from t1' to t2', during which time P1 will be turned on and N1 will be turned off. Note in the instance shown, TON' is a non-zero minimum time interval for which P1 is always on during each cycle, regardless of the relationship between Ramp and Loop filter output.

[0033] At t2', the discharging phase commences and lasts for a duration TOFF' to t3'. Note P1 is turned on during TON' even though Loop filter output is less than Ramp, as the buck converter implementation 100 shown in FIG 4 imposes a minimum on-time TON' for all cycles. Note while the minimum on-time TON' in FIG 4 is shown as being a non-zero time interval, in alternative exemplary embodiments, the minimum duration TON' may be zero, in which case P1 may be turned off the entire time when Loop filter output is less than Ramp. Further note the waveforms in FIG 4 are drawn according to scale, and further are not meant to imply any specific relationships between the minimum on-time TON' and the cycle duration.

[0034] FIG 5 illustrates exemplary voltage and current waveforms present in the buck converter 100, during a transition in which the target value of Vout is brought from a first level V1 down to a second level V2 considerably less than V1. Note the waveforms in FIG 5 are shown for illustrative purposes only, and are not meant to suggest that signal waveforms will necessarily have the profiles shown.

[0035] In FIG 5, prior to time T1, the current IL initially has a positive value I1, and the corresponding output voltage Vout has a first value V1. At T1, IL begins to decrease, e.g., in response to a setpoint of Vout being decreased from V1 to a lower level V2. As IL decreases, it eventually becomes negative, crossing zero current at time T2. Vout correspondingly starts to decrease at T2, when IL becomes negative (assuming the load current is zero). Following T2, once the corresponding Vout becomes less than V2, then IL will eventually start to increase (after decreasing to as low as I3), and once again become positive. In conjunction, Vout will also start to increase, and eventually settle close to its target level around time T3. Thereafter, IL and Vout will settle to their steady-state levels (e.g., IL at I2 and Vout at V2), until a next change in the target value of Vout.

[0036] It will be appreciated from the above description that there are at least two problems associated with using reverse boost mode to rapidly reduce Vout. First, during reverse boost mode, the current IL through N1 may become increasingly negative without bound, which may have adverse consequences due to the limited power handling capability of the

system. Second, it may take a considerable additional amount of time to bring Vout to the target level due to undershoot characteristics of the system as further described hereinbelow.

[0037] In particular, in FIG 5, it can be seen that following T1, the level of Vout crosses the target value of V2 twice: once at time T2.1, and once again at T3. In the time duration between T2.1 and T3, Vout may be characterized as being in a state of "undershoot," wherein the transient value of Vout temporarily is less than the target value of V2, and later increases back to V2. For example, between T2.1 and T3, Vout may decrease to as low as V3, before starting to increase again. It will be seen that this undershoot is due at least in part to the large negative current IL established after T2. A significant amount of time is required to discharge the negative current from the inductor L and to re-charge L back to a positive, steady-state current to sustain the target output voltage V2. It will be appreciated that the aforementioned scenario is an obstacle to achieving fast settling times for current mode buck converters in reverse boost mode.

[0038] It would be desirable to provide techniques to feed information regarding the inductor current IL back into the control loop, and, in particular, to back off the amount of negative current through IL as Vout approaches the target voltage to reduce undershoot and settling time.

[0039] FIG 6 illustrates an exemplary embodiment of the present disclosure, wherein negative current flow through the PMOS switch P1 is sensed and fed back to the control loop of the buck converter 600. Note similarly labeled elements in FIGs 1 and 6 may correspond to elements having similar functionality, unless otherwise noted. In FIG 6, a negative current sensor 602 is provided to sense the magnitude of negative current I_P1n through P1. (Note according to the conventions adopted herein, a negative measured value for I_P1 will correspond to a positive I_P1n.) In the exemplary embodiment shown, the output I_P1n of the negative current sensor 602 is used to generate an "Adjusted ramp" signal for the comparator 130, wherein Adjusted ramp is defined as follows, when P1 is on (Equation 2):

$$\text{Adjusted ramp} = (I\_P1p \cdot Rsns1) - (I\_P1n \cdot Rsns2) + \text{Slope comp} + \text{Offset};$$

wherein I_P1n is the sensed negative current through P1, and Rsns2 is a resistance (not shown in FIG 6). From comparing Equation 2 with Equation 1, it will be appreciated that, when inductor current IL is positive, Adjusted ramp is equal to Ramp; however, when IL is negative, Adjusted ramp will be less than Ramp, due to the term (I_P1n · Rsns2).

Furthermore, Adjusted ramp will be increasingly less than Ramp as IL becomes more negative.

[0040] From FIG 6, it will accordingly be appreciated that the lower value of Adjusted ramp at the positive (+) input terminal of comparator 130 will generate a PWM output voltage 130a with a longer TON / shorter TOFF than a corresponding value of Ramp. In other words, using Adjusted ramp per Equation 2, the PMOS on-time will be progressively increased as the inductor current IL becomes increasingly negative, which will in turn prevent IL from further becoming increasingly negative without bound.

[0041] FIG 7 illustrates exemplary signal waveforms present in the buck converter 600 during a period when Vout transitions from V1 to V2, wherein negative current through P1 is provided as feedback to the control loop described hereinabove. Note FIG 7 is shown for illustrative purposes only, and is not meant to limit the scope of the present disclosure to any exemplary signal waveforms shown.

[0042] In FIG 7, Adjusted ramp is shown as a dashed line. The time interval shown (e.g., from before t1* to after t6*) corresponds to a period of time during which Vout is transitioning from V1 to V2, and, in particular, wherein negative current IL flows through the inductor L. During these times, when P1 is on, I_P1n will have positive magnitude (due to negative IL being detected), and thus Adjusted ramp will be correspondingly reduced as according to Equation 2. For example, in FIG 7, for a duration TON* between times t1* and t2*, P1 is on, and Adjusted ramp is seen to decrease from a level Offset greater than Loop filter output prior to t1* to a level less than Loop filter output at t1*. Following t2*, for a duration TOFF* between t2* and t3*, P1 is off and N1 is on. At t3*, the cycle is repeated.

[0043] FIG 8 illustrates exemplary voltage and current waveforms present in the buck converter 600 during a transition in Vout from V1 to V2, wherein negative current through P1 is used to adjust the control loop according to the present disclosure. Note the waveforms in FIG 8 are shown for illustrative purposes only, and are not meant to suggest that signal waveforms will necessarily have the profiles shown. Note similarly labeled variables in FIGs 5 and 8 may have similar values unless otherwise noted; for example, the exemplary levels of V1 and V2 in FIG 8 may correspond to the same levels described with reference to FIG 5.

[0044] In FIG 8, similar to FIG 5, the current IL initially has a positive value I1 at T1, and the corresponding output voltage Vout has a first value V1. At T1, IL begins to decrease,

e.g., in response to a setpoint of Vout being decreased from V1 to a lower level V2. As IL decreases, it eventually becomes negative, crossing zero at time T2. When IL becomes negative, then I_P1n as sensed by sensor 602 will be positive. As earlier described hereinabove, a positive I_P1n decreases Adjusted ramp relative to Ramp, thereby increasing the P1 turn-on time TON* relative to the implementation profiled in FIG 5. IL decreases to as low as I3* before increasing again to I2.

[0045] Due to the presence of the term I_P1n in Adjusted ramp, it will be appreciated that I3* is considerably greater (i.e., less negative) than the negative current I3 shown in FIG 5. Correspondingly, Vout is seen to settle to the target value of V2 at time T3*, which is significantly earlier than the time T3 corresponding to the implementation profiled in FIG 5. It will thus be appreciated from the above description that the time needed to transition from V1 to V2 will be significantly less for the buck converter 600 than for the buck converter 100.

[0046] It will be appreciated that an advantage of the techniques described herein is that, by incorporating the negative P1 current I_P1n to generate Adjusted ramp per Equation 2 in the manner described, the same control logic incorporated by, e.g., the switch control block 140, can be re-used with minimal modifications, thereby introducing minimal additional complexity to the control system. In particular, linear and continuous control techniques may be adopted for the buck converter 100. Furthermore, the control system advantageously does not need to accommodate switching between separate "forward buck" and "reverse boost" states, thereby improving system stability.

[0047] FIG 9 illustrates an exemplary implementation 600.1 of the buck converter 600. Note FIG 9 is shown for illustrative purposes only, and is not meant to limit the scope of the present disclosure to only the exemplary embodiment of the buck converter 600 shown in FIG 6.

[0048] In FIG 9, the sensor 602 of FIG 6 is implemented using circuitry 602.1 including a feed-through PMOS transistor PE2 coupling VSW to the positive (+) input of an amplifier 910. The negative (-) input of amplifier 910 is coupled to Vbatt. In this manner, amplifier 910 generates a voltage proportional to (VSW minus Vbatt) at the gate of NMOS transistor N2, whose drain is coupled to the drain of PE2. The gate voltage of N2 is further provided to an NMOS transistor N3, also denoted a "negative-current" transistor, whose drain is coupled to a node 699. Node 699 is in turn coupled to V3' via R2, wherein V3' is also

coupled to the output of the positive current sensor 102.1. Node 699 is further coupled to V1' via R3, wherein V1' is coupled to the Offset current source, C1, and switch S1.

[0049] In particular, during reverse boost mode, VSW is expected to be larger than Vbatt when P1 is on, and thus N3 is expected to be turned on, generating a drain current I(I_P1n) that is a linear function of negative P1 current, with the polarity indicated. It will be seen that I(I_P1n) is subtracted from the currents Offset and I(I_P1p) that would otherwise flow through resistors R1 and R2, and thus the voltage V1' at a first plate of capacitor C1 is expected to be correspondingly less as a result of I(I_P1n).

[0050] FIG 10 illustrates an exemplary embodiment of a method 1000 according to the present disclosure. Note the method 1000 is shown for illustrative purposes only, and is not meant to restrict the scope of the present disclosure.

[0051] At block 1010, a first node of an inductor is selectively coupled to a supply voltage.

[0052] At block 1020, the first node of the inductor is selectively coupled to ground.

[0053] At block 1030, the selective coupling is configured to set an output voltage at a load coupled to a second node of the inductor. The configuring may comprise comparing a filtered error voltage to an adjusted ramp voltage.

[0054] At block 1040, negative current is sensed through the inductor, wherein the adjusted ramp voltage comprises an additive term that reduces the adjusted ramp voltage in response to negative current being sensed.

[0055] Note while exemplary embodiments have been described hereinabove wherein a PMOS transistor is used as the charging switch (e.g., in the exemplary embodiment 600 of FIG 6) coupling the inductor L to Vbatt, the techniques described may readily be utilized in alternative exemplary embodiments employing elements other than a PMOS transistor for the charging switch. For example, in an alternative exemplary embodiment (not shown), an NMOS switch may also be utilized, and the negative current through the NMOS (charging) switch may be sensed and utilized per the techniques described herein. Such alternative exemplary embodiments are contemplated to be within the scope of the present disclosure.

[0056] It will be appreciated that any types of applications incorporating buck converters may utilize the techniques of the present disclosure. For example, in certain exemplary embodiments, a buck converter incorporating the techniques described herein may be applied to average power tracking (APT) schemes, switched-mode battery chargers (SMBC's), and fast transient supply (FTS) schemes known in the art. Such exemplary embodiments are contemplated to be within the scope of the present disclosure.

[0057] In this specification and in the claims, it will be understood that when an element is referred to as being "connected to" or "coupled to" another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected to" or "directly coupled to" another element, there are no intervening elements present. Furthermore, when an element is referred to as being "electrically coupled" to another element, it denotes that a path of low resistance is present between such elements, while when an element is referred to as being simply "coupled" to another element, there may or may not be a path of low resistance between such elements.

[0058] Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0059] Those of skill in the art would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the exemplary aspects disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the exemplary aspects of the invention.

[0060] The various illustrative logical blocks, modules, and circuits described in connection with the exemplary aspects disclosed herein may be implemented or performed with a general purpose processor, a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any

conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0061] The steps of a method or algorithm described in connection with the exemplary aspects disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

[0062] In one or more exemplary aspects, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc

(DVD), floppy disk and Blu-Ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0063] The previous description of the disclosed exemplary aspects is provided to enable any person skilled in the art to make or use the invention. Various modifications to these exemplary aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other exemplary aspects without departing from the spirit or scope of the invention. Thus, the present disclosure is not intended to be limited to the exemplary aspects shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

1. An apparatus comprising:

a charging switch configured to selectively couple a first node of an inductor to a supply voltage;

a discharging switch configured to selectively couple the first node of the inductor to ground;

a control block configured to control the charging and discharging switches to set an output voltage at a load coupled to a second node of the inductor, the control loop comprising a comparator comparing a filtered error voltage to an adjusted ramp voltage;

a negative current sense block configured to sense negative current through the inductor, wherein the adjusted ramp voltage comprises an additive term that reduces the adjusted ramp voltage in response to negative current being sensed.

2. The apparatus of claim 1, further comprising a positive current sense block to sense positive current through the inductor, wherein the adjusted ramp voltage further comprises an additive term that increases the adjusted ramp voltage in response to positive current being sensed.

3. The apparatus of claim 1, wherein the charging switch comprises a PMOS transistor, and the discharging switch comprises an NMOS transistor.

4. The apparatus of claim 1, the negative current sense block configured to sense negative current through the charging switch.

5. The apparatus of claim 4, the negative current sense block comprising an amplifier configured to sense a voltage drop across the charging switch corresponding to negative inductor current.

6. The apparatus of claim 5, the negative current sense block further comprising:

a feed-through transistor coupled to a control voltage of the charging switch, wherein the amplifier has an input terminal coupled to the feed-through transistor;

the output of the amplifier coupled to a negative-current transistor, wherein the negative-current transistor has a drain coupled to circuitry for generating current proportional to the adjusted ramp voltage.

7. The apparatus of claim 6, the circuitry for generating current proportional to the adjusted ramp voltage comprising an offset current source, a capacitor C1, and a slope compensation current source.

8. The apparatus of claim 1, wherein the charging switch comprises an NMOS transistor.

9. The apparatus of claim 1, the control block configured to implement a linear and continuous control loop system to set the output voltage.

10. The apparatus of claim 1, wherein the switches, control block, and negative current sensing block are incorporated in a buck converter, and the buck converter is used in an average power tracking scheme, a switched-mode battery charger, or as a fast transient supply buck converter.

11. A method comprising:

selectively coupling a first node of an inductor to a supply voltage;

selectively coupling the first node of the inductor to ground;

configuring the selective coupling to set an output voltage at a load coupled to a second node of the inductor, the configuring comprising comparing a filtered error voltage to an adjusted ramp voltage; and

sensing negative current through the inductor, wherein the adjusted ramp voltage is reduced in response to negative current being sensed.

12. The method of claim 11, further comprising:

sensing positive current through the inductor, wherein the adjusted ramp voltage is increased in response to positive current being sensed.

13. The method of claim 11, the sensing the negative current through the inductor comprising sensing negative current through a charging switch for selectively coupling the first node of the inductor to the supply voltage.

14. The method of claim 13, the sensing the negative current comprising sensing a voltage drop across the charging switch.

15. The method of claim 13, wherein the charging switch comprises a PMOS transistor.

16. The method of claim 13, the sensing the negative current through charging switch being performed during a time interval when the charging switch is enabled to couple the first node of the inductor to the supply voltage.

17. An apparatus comprising:

means for selectively coupling a first node of an inductor to a supply voltage;

means for selectively coupling the first node of the inductor to ground;

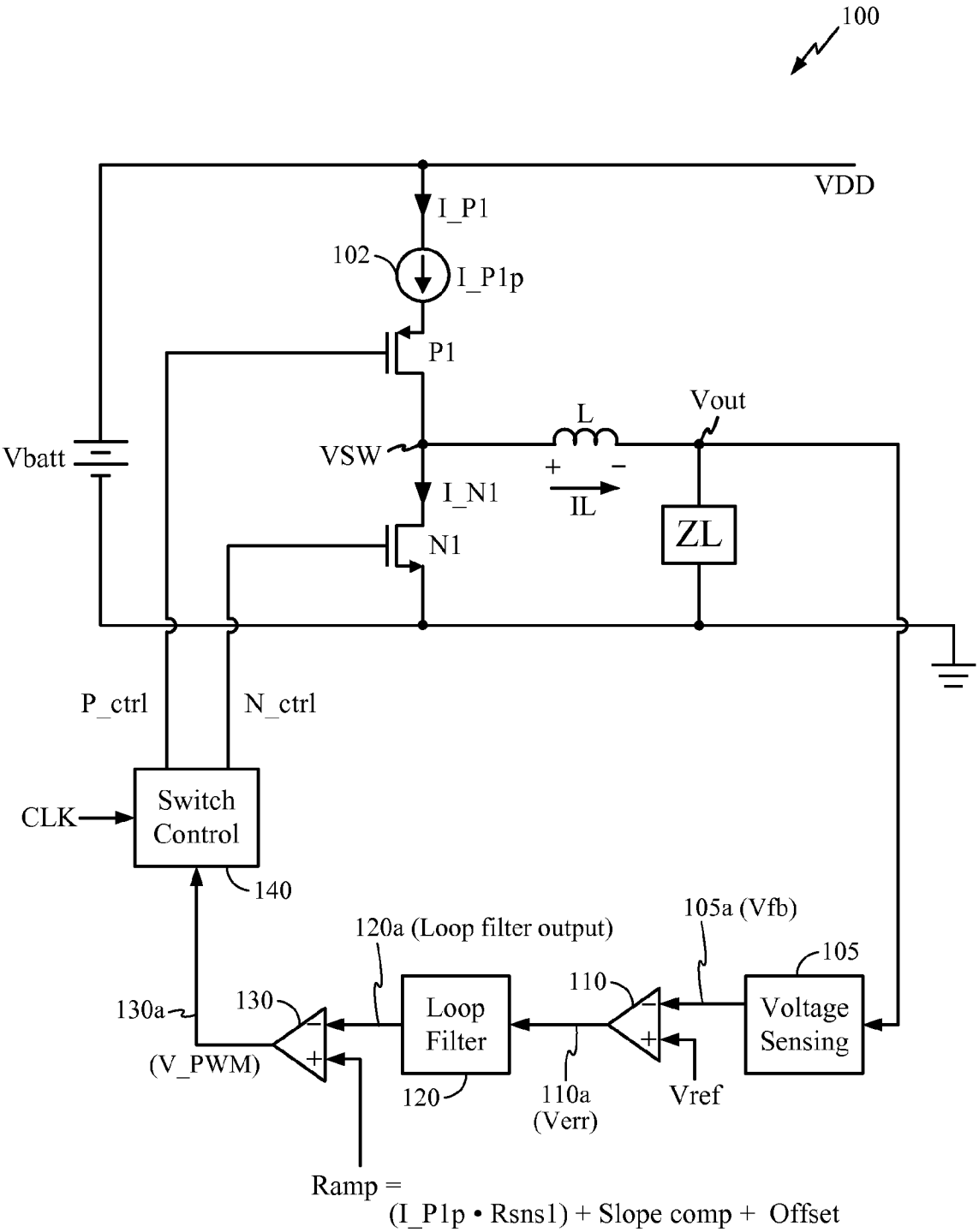
means for configuring the selective coupling to set an output voltage at a load coupled to a second node of the inductor, the configuring comprising comparing a filtered error voltage to an adjusted ramp voltage; and

means for sensing negative current through the inductor.

18. The apparatus of claim 17, further comprising means for sensing positive current through the inductor.

19. The apparatus of claim 17, the means for sensing negative current through the inductor further comprising means for sensing negative current through the charging switch.

20. The apparatus of claim 19, the means for sensing negative current through the charging switch comprising means for sensing a voltage drop across the charging switch.



(PRIOR ART)

FIG 1

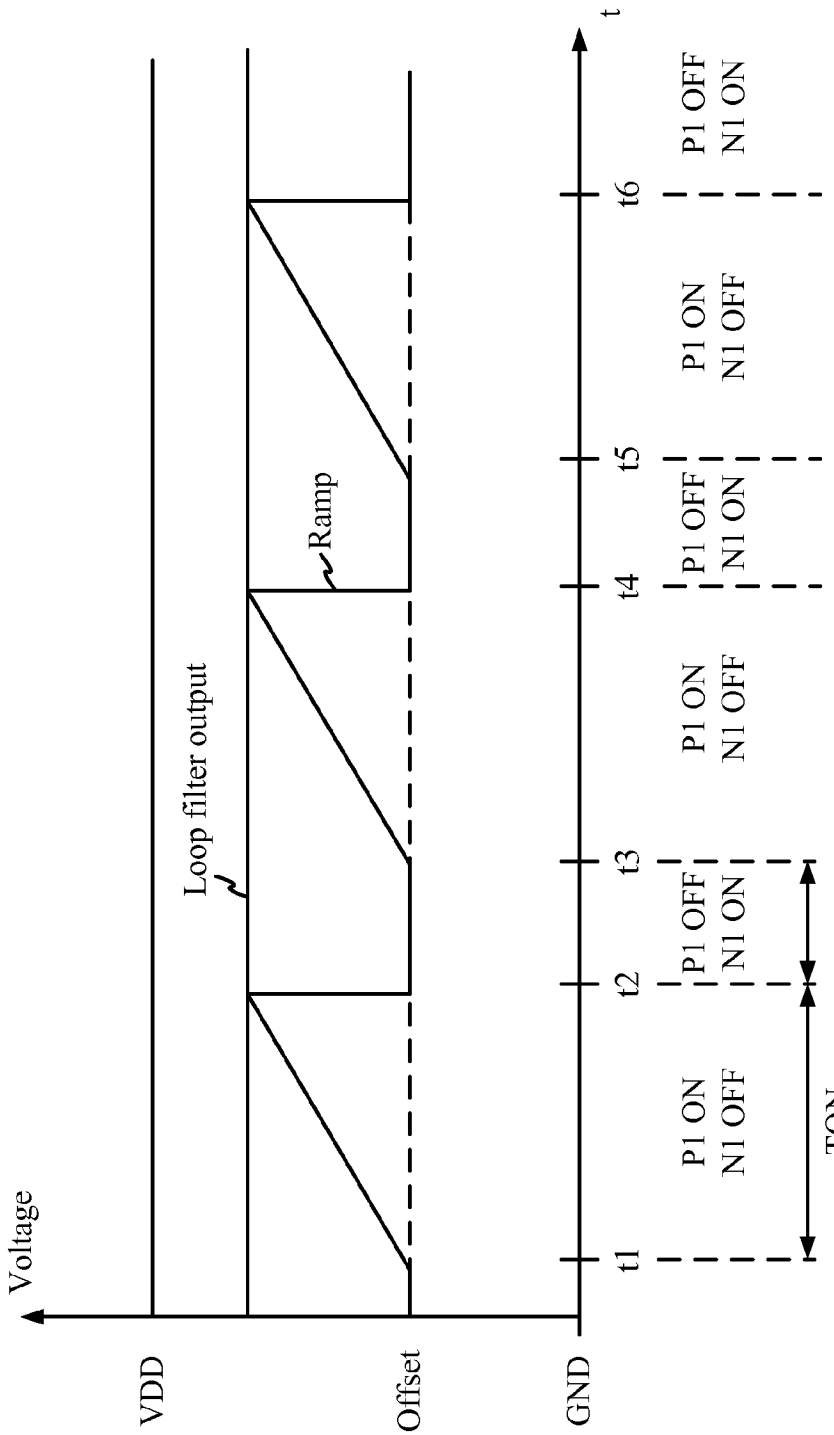

Voltage
VDD
Offset
GND
Loop filter output
Ramp
t
t1
t2
t3
t4
t5
t6
P1 ON
N1 OFF
P1 OFF
N1 ON
TON
TOFF
Charging phase
Discharging phase

FIG 2

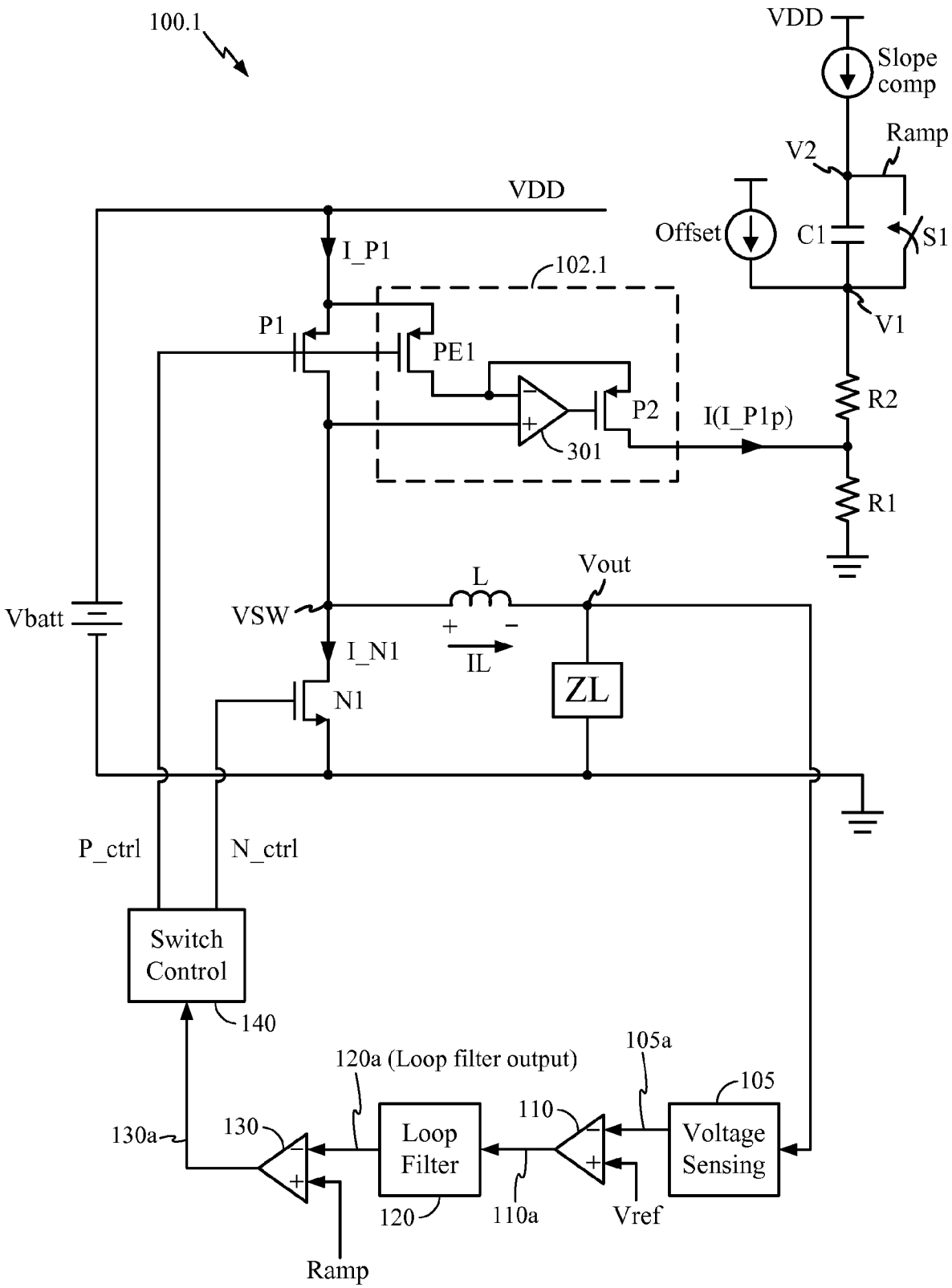

100.1
VDD
Slope comp
Ramp
V2
VDD
Offset
C1
S1
I_P1
102.1
V1
P1
PE1
P2
I(I_P1p)
R2
301
R1
Vout
L
Vbatt
VSW
I_N1
IL
ZL
N1
P_ctrl
N_ctrl
Switch Control
140
120a (Loop filter output)
105a
105
110
130a
130
Loop Filter
Voltage Sensing
120
110a
Vref
Ramp

FIG 3

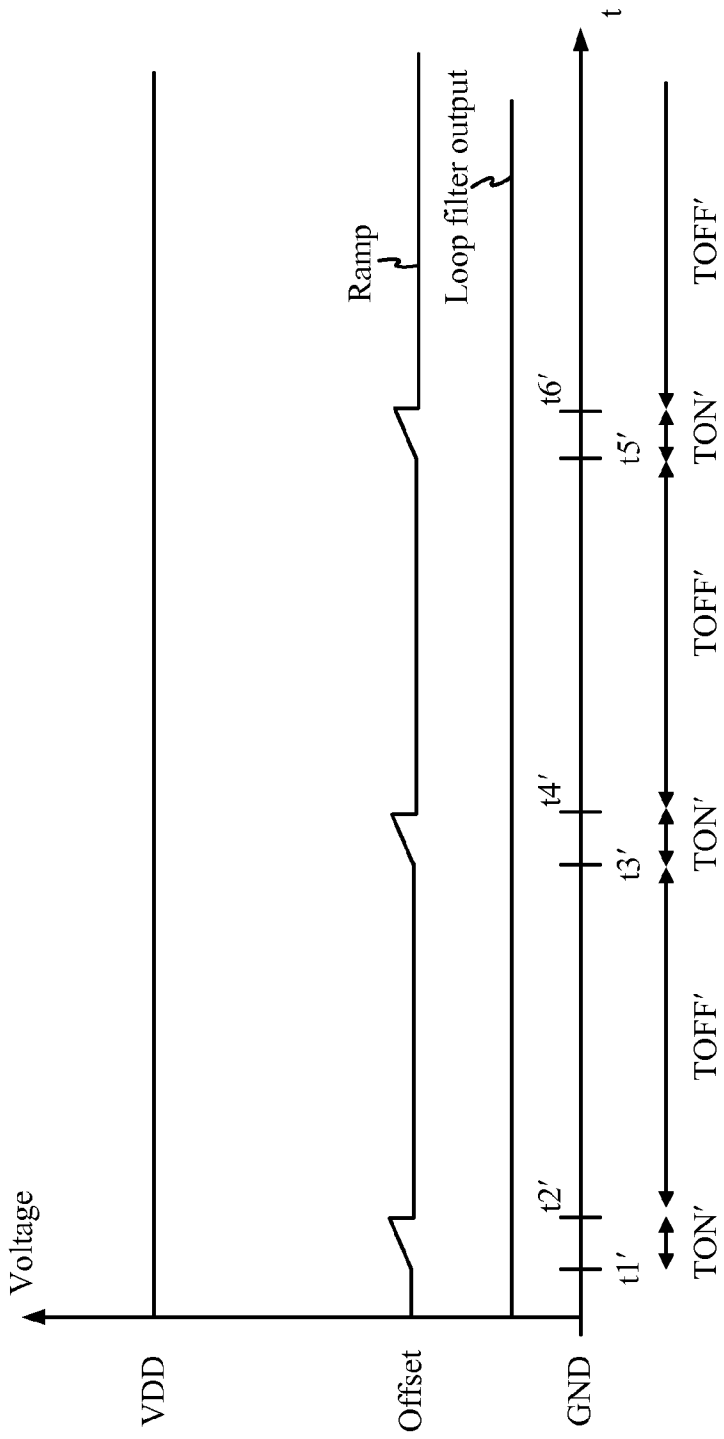

Voltage
VDD
Offset
GND
Ramp
Loop filter output
t
t1′
t2′
t3′
t4′
t5′
t6′
TON′
TOFF′
TON′
TOFF′
TON′
TOFF′

FIG 4

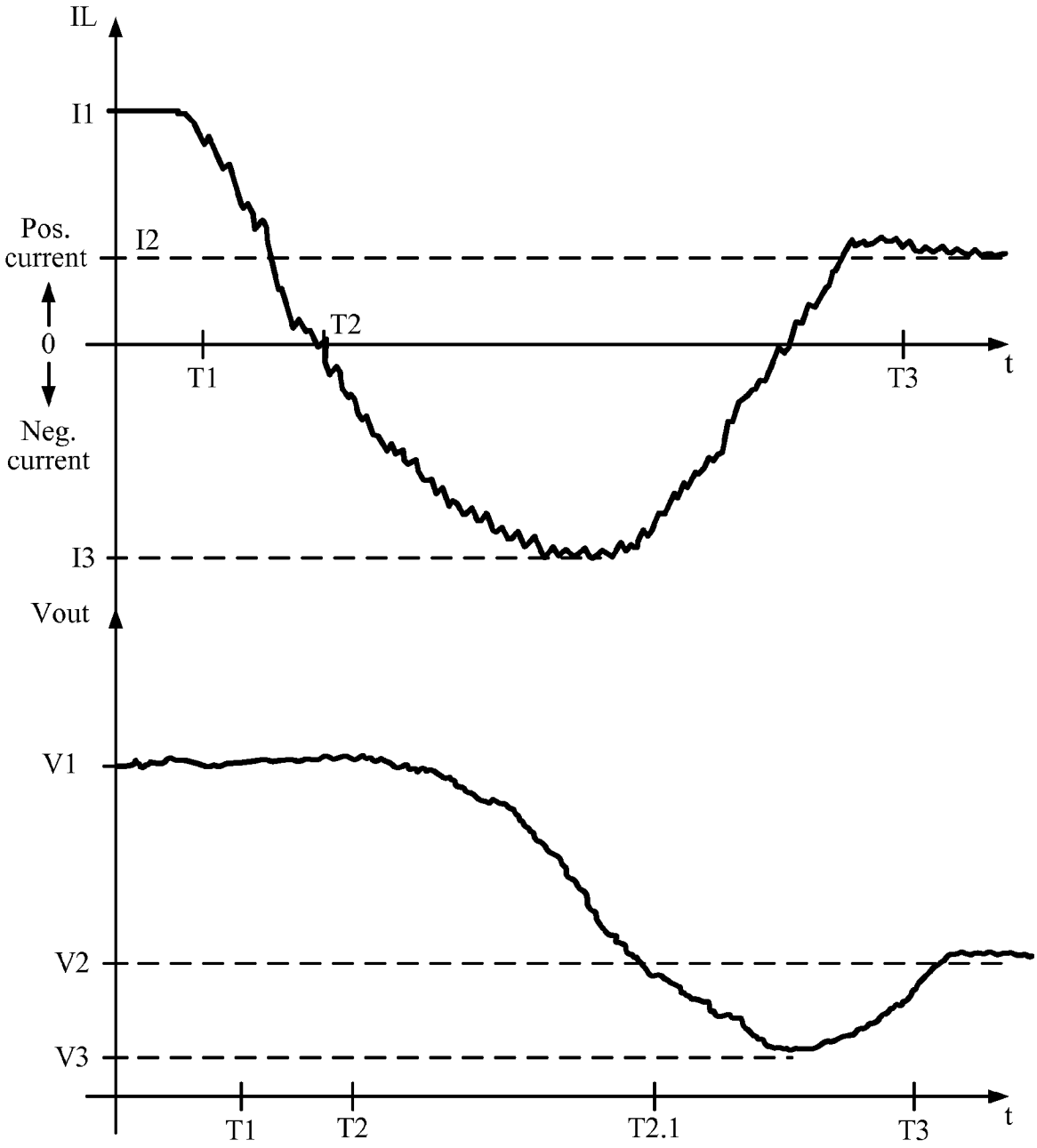

IL
I1
Pos.
current
I2
0
T1
T2
T3
t
Neg.
current
I3
Vout
V1
V2
V3
T1
T2
T2.1
T3
t

FIG 5

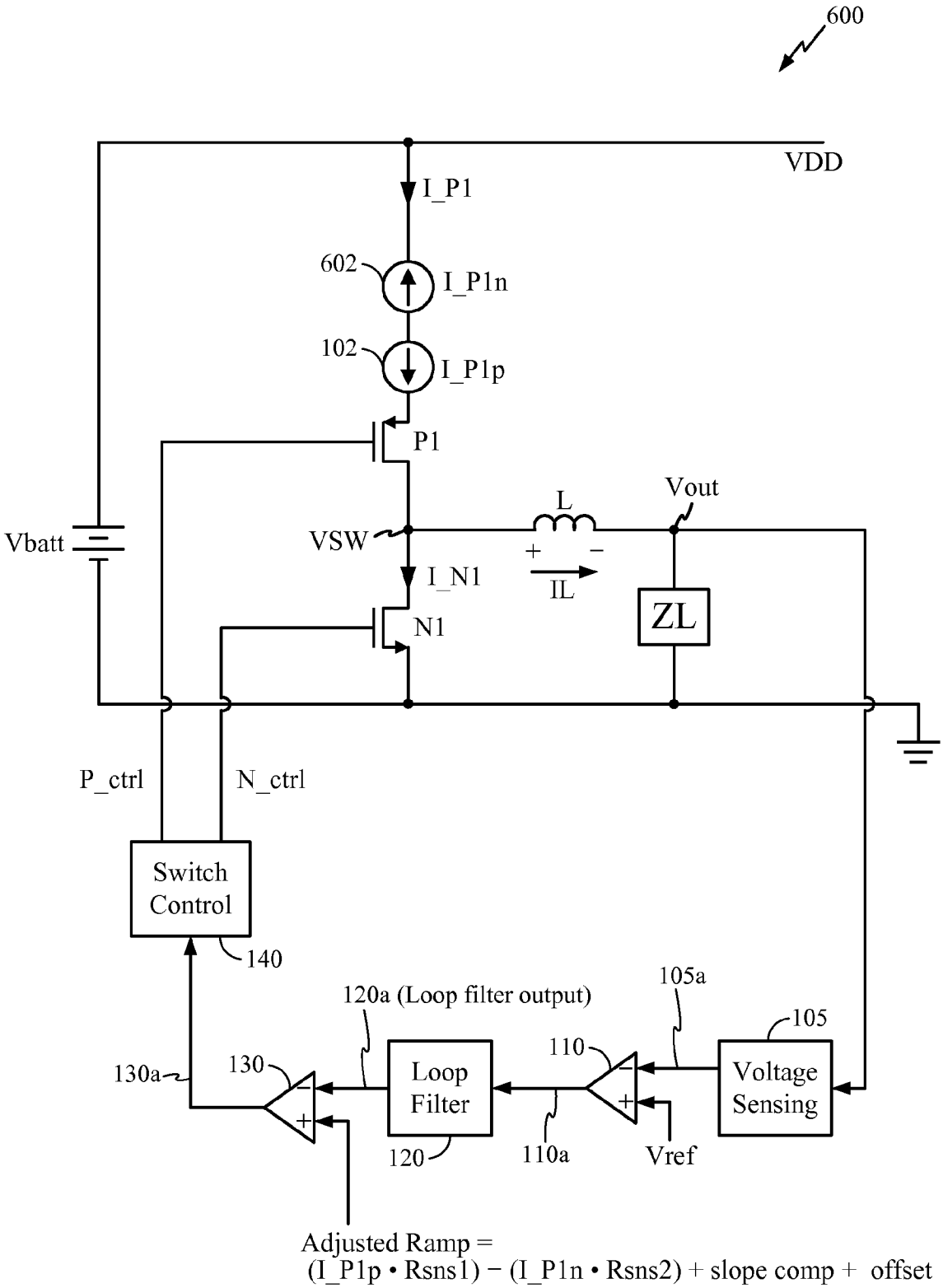

600
VDD
I_P1
602
I_P1n
102
I_P1p
P1
Vout
L
Vbatt
VSW
I_N1
IL
ZL
N1
P_ctrl
N_ctrl
Switch Control
140
120a (Loop filter output)
105a
105
110
130a
130
Loop Filter
Voltage Sensing
120
110a
Vref
Adjusted Ramp =
(I_P1p • Rsns1) − (I_P1n • Rsns2) + slope comp + offset

FIG 6

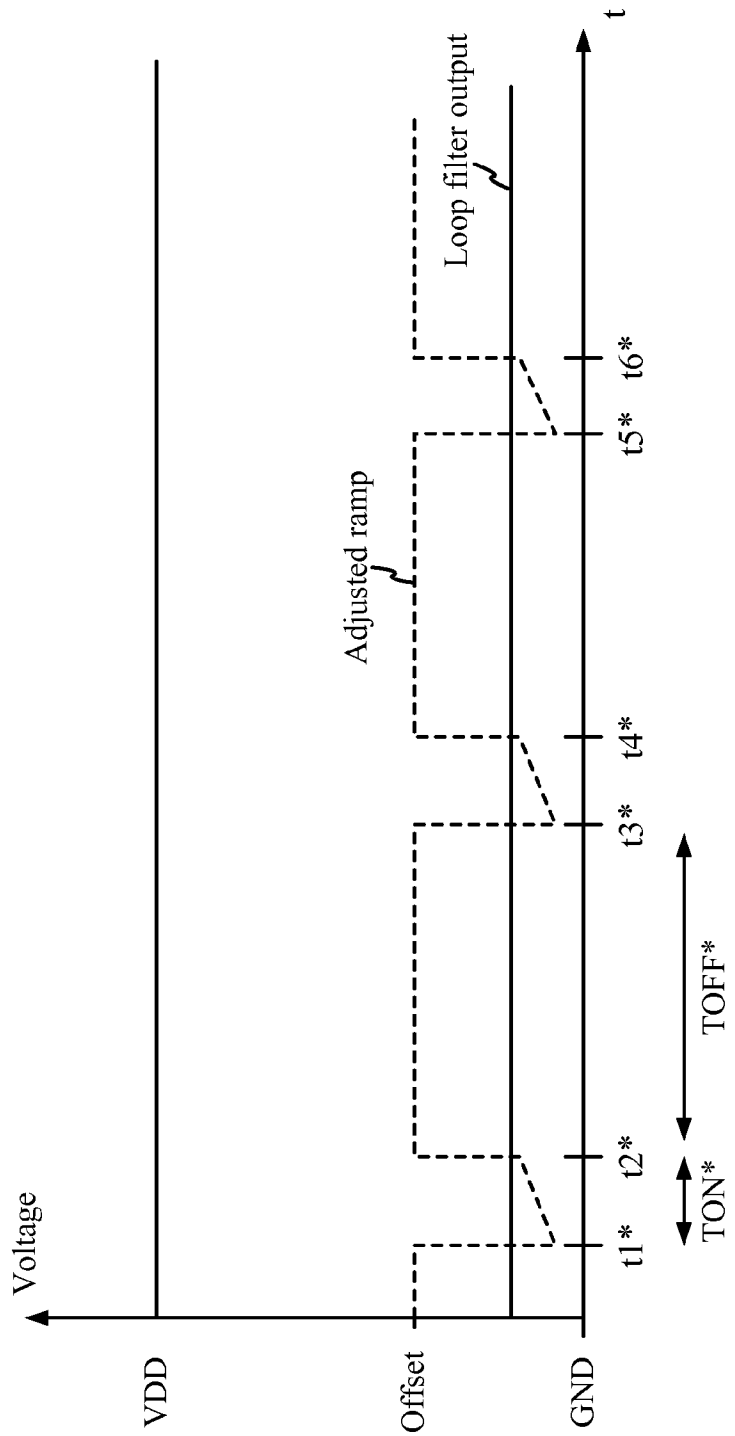

Voltage
VDD
Offset
GND
t
Loop filter output
Adjusted ramp
t1*
t2*
t3*
t4*
t5*
t6*
TON*
TOFF*

FIG 7

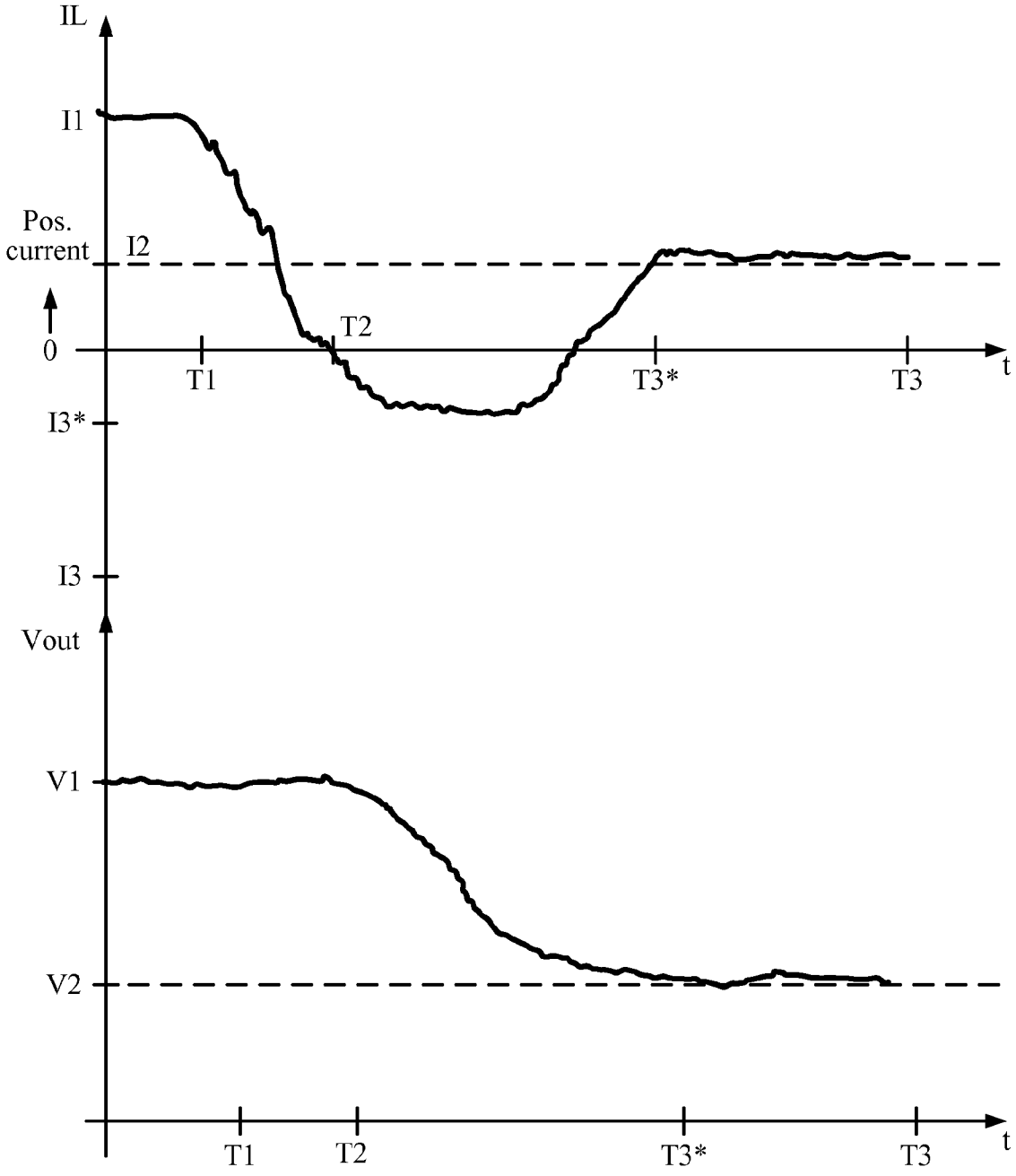


FIG 8

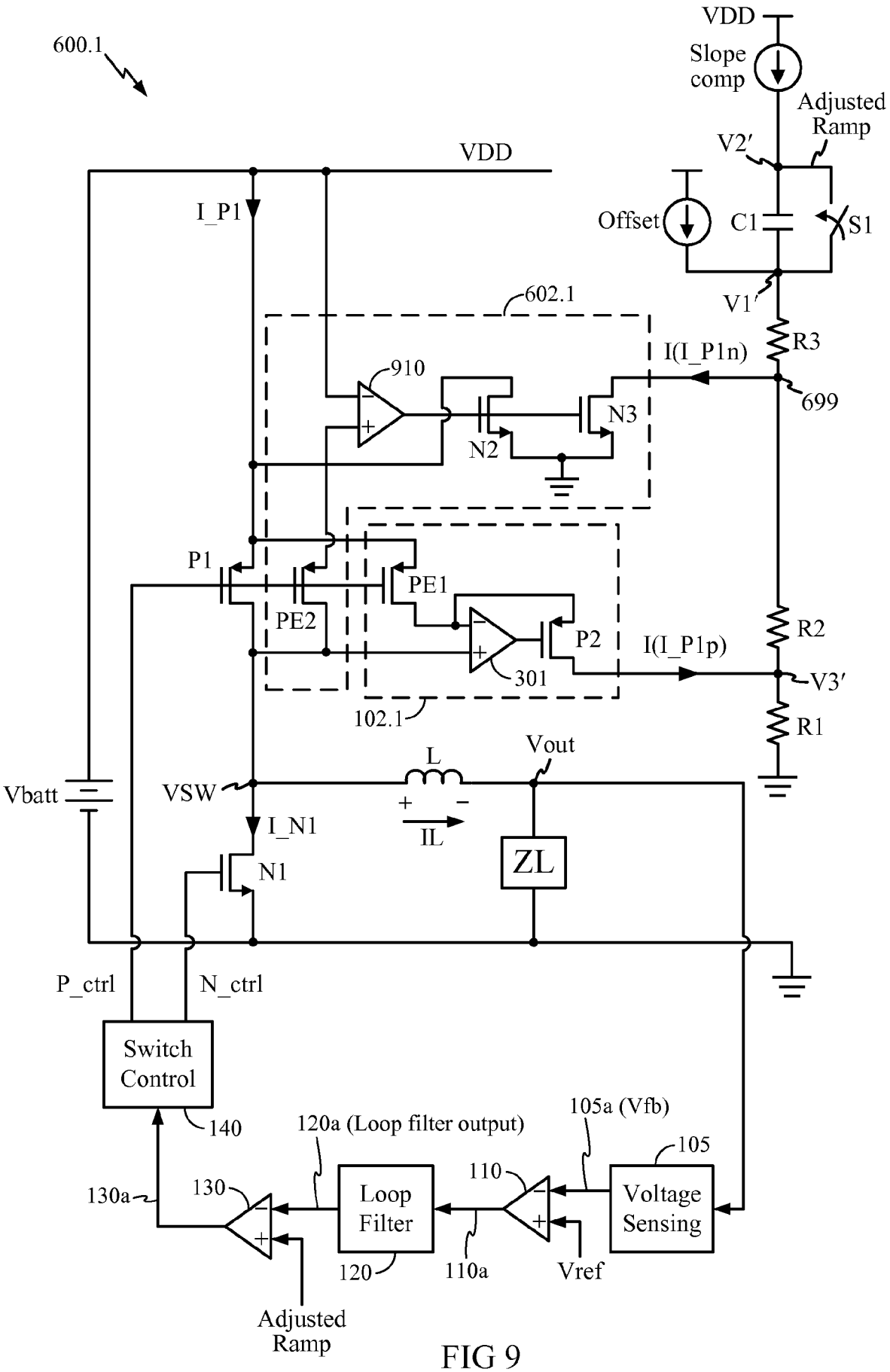

600.1
VDD
Slope comp
Adjusted Ramp
V2′
VDD
I_P1
Offset
C1
S1
602.1
V1′
R3
I(I_P1n)
910
699
N3
N2
P1
PE1
PE2
P2
I(I_P1p)
R2
301
V3′
102.1
R1
Vout
L
Vbatt
VSW
I_N1
IL
N1
ZL
P_ctrl
N_ctrl
Switch Control
140
120a (Loop filter output)
105a (Vfb)
105
110
130a
130
Loop Filter
Voltage Sensing
120
110a
Vref
Adjusted Ramp

FIG 9

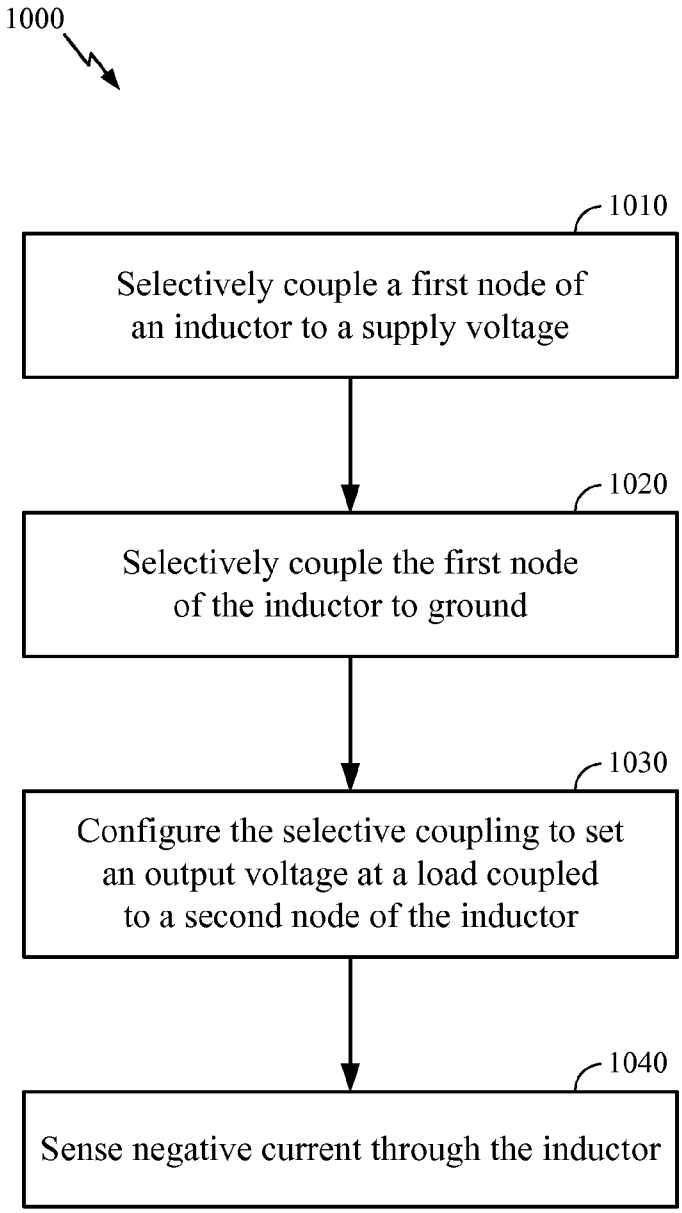

1000
1010
Selectively couple a first node of an inductor to a supply voltage
1020
Selectively couple the first node of the inductor to ground
1030
Configure the selective coupling to set an output voltage at a load coupled to a second node of the inductor
1040
Sense negative current through the inductor

FIG 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/012392

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/156
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2012/109680 A2 (DE VRIES IAN DOUGLAS [ZA]) 16 August 2012 (2012-08-16) figures 1,12	1-3,8-10
X	ENRICO DALLAGO ET AL: "Lossless Current Sensing in Low-Voltage High-Current DC/DC Modular Supplies", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 47, no. 6, 1 December 2000 (2000-12-01), XP011023747, ISSN: 0278-0046 figure 4	1-3,8-10
A	US 3 417 321 A (CLAPP WILLIAM M) 17 December 1968 (1968-12-17) the whole document	1

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 May 2014	22/05/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Taccoen, J

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/012392

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 472 111 A (WOLFSON MICROELECTRONICS PLC [GB]) 26 January 2011 (2011-01-26) page 24, line 5 - line 16; figure 2 -----	11-20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/012392

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/012392

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2012109680 A2	16-08-2012	CN 103392131 A	13-11-2013
		EP 2673648 A2	18-12-2013
		JP 2014506776 A	17-03-2014
		US 2013307511 A1	21-11-2013
		WO 2012109680 A2	16-08-2012
US 3417321 A	17-12-1968	NONE	
GB 2472111 A	26-01-2011	CN 102498653 A	13-06-2012
		CN 102714462 A	03-10-2012
		EP 2457317 A2	30-05-2012
		GB 2472111 A	26-01-2011
		GB 2472112 A	26-01-2011
		GB 2472113 A	26-01-2011
		GB 2472114 A	26-01-2011
		GB 2472115 A	26-01-2011
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		GB 2483003 A	22-02-2012
		GB 2486827 A	27-06-2012
		KR 20120039726 A	25-04-2012
		TW 201108580 A	01-03-2011
		US 2011018507 A1	27-01-2011
		US 2011018515 A1	27-01-2011
		US 2011018516 A1	27-01-2011
		US 2011018588 A1	27-01-2011
		US 2011050185 A1	03-03-2011
		US 2013314062 A1	28-11-2013
		WO 2011010141 A2	27-01-2011
		WO 2011010142 A2	27-01-2011
		WO 2011010143 A2	27-01-2011
		WO 2011010144 A2	27-01-2011
		WO 2011010151 A2	27-01-2011

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-10

An apparatus comprising:
a charging switch configured to selectively couple a first node of an inductor to a supply voltage;
a discharging switch configured to selectively couple the first node of the inductor to ground;
a control block configured to control the charging and discharging switches to set an output voltage at a load coupled to a second node of the inductor, the control loop comprising a comparator comparing a filtered error voltage to an adjusted ramp voltage;
a negative current sense block configured to sense negative current through the inductor, wherein the adjusted ramp voltage comprises an additive term that reduces the adjusted ramp voltage in response to negative current being sensed.

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2. claims: 11-20

An apparatus comprising:
means for selectively coupling a first node of an inductor to a supply voltage;
means for selectively coupling the first node of the inductor to ground;
means for configuring the selective coupling to set an output voltage at a load coupled to a second node of the inductor, the configuring comprising comparing a filtered error voltage to an adjusted ramp voltage; and
means for sensing negative current through the inductor.
