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(54) **MULTI-CHIP STACK PACKAGE AND FABRICATING METHOD THEREOF**

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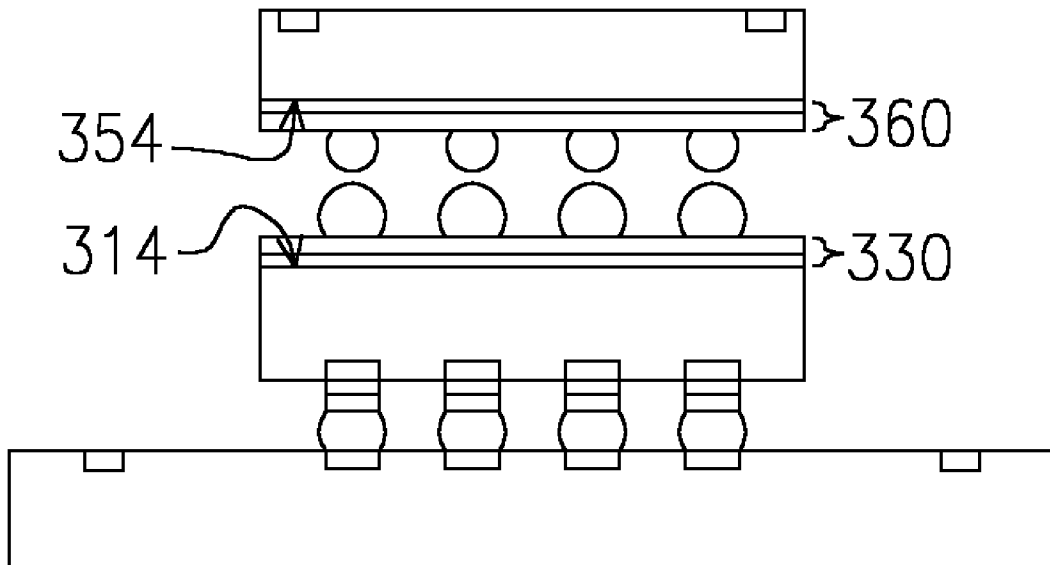
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(57) **ABSTRACT**

A multi-chip stack package having a substrate, a first chip, a second chip, a plurality of bumps, a plurality of junction

interface bumps, a plurality of conductive wires, a first filler material, a second filler material and an encapsulating material is provided. The substrate has a substrate surface with a plurality of first contacts and a plurality of second contacts. The first chip has a first active surface with a plurality of bonding pads thereon and a first chip back surface. The first chip is positioned over the substrate surface. The second chip has a second active surface with a plurality of bonding pads thereon and a second chip back surface. The second chip is positioned over the first chip back surface. The bumps are positioned between the first bonding pads and the first contacts. The junction interface bumps are positioned between the first chip back surface and the second chip back surface. The conductive wires electrically connect the second bonding pads and the second contacts. The first filler material encloses the bumps and the second filler material encloses the junction interface bumps. The encapsulating material encloses the first chip, the second chip and the conductive wires.



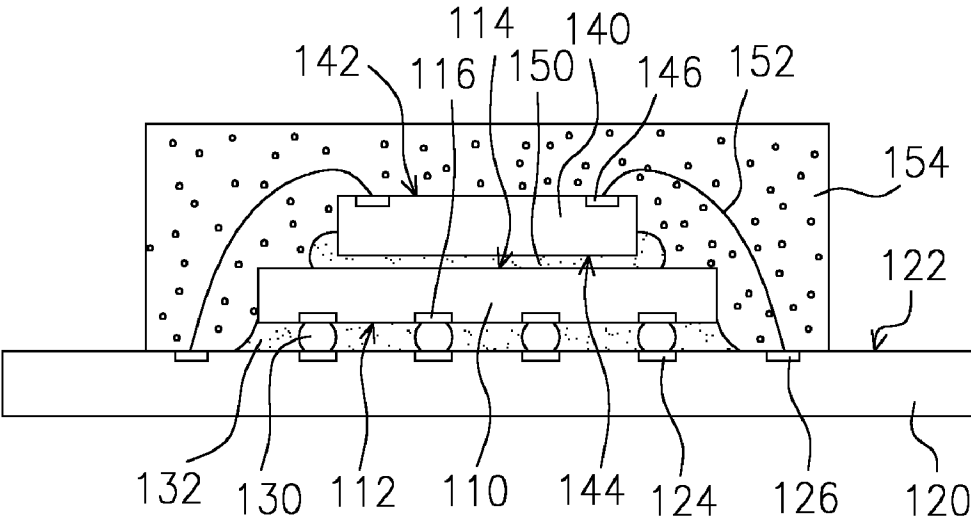


FIG. 1 (PRIOR ART)

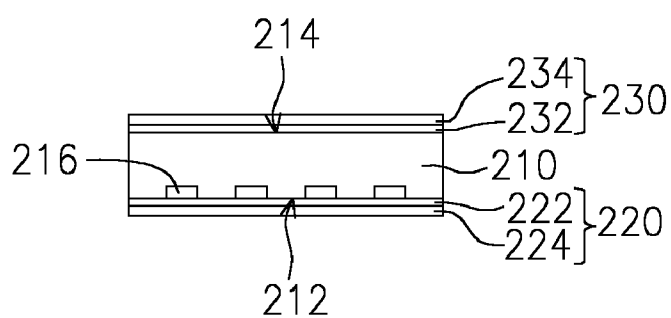


FIG. 2

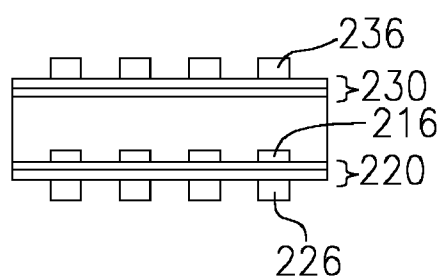


FIG. 3

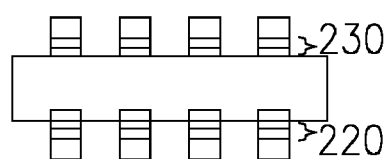


FIG. 4

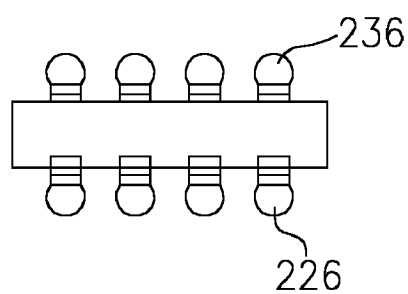


FIG. 5

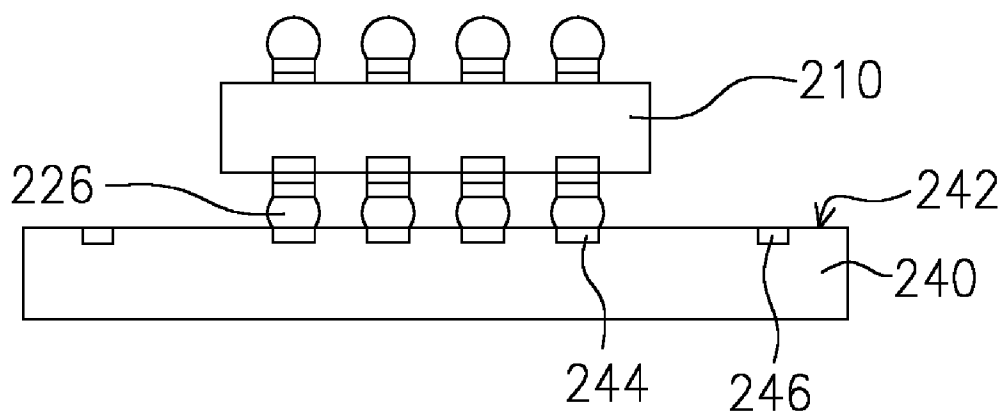


FIG. 6

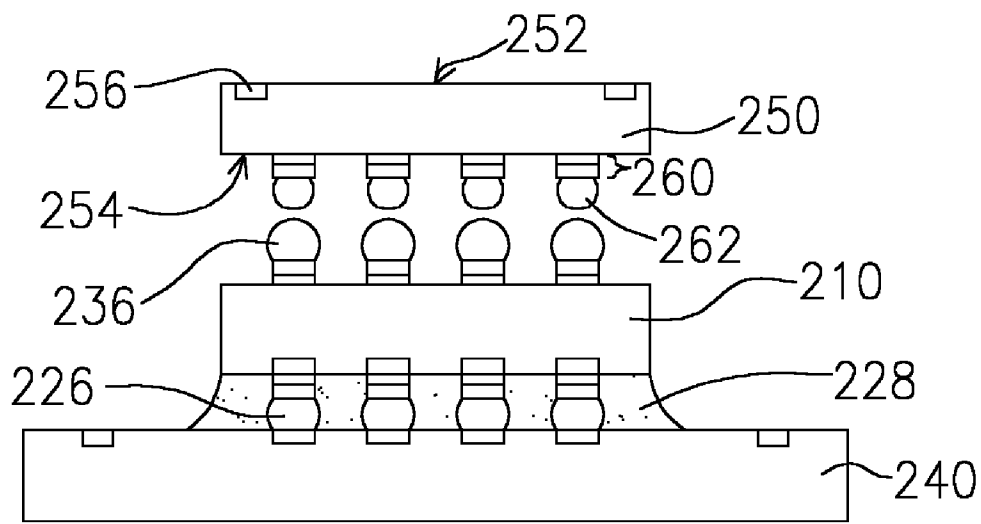


FIG. 7

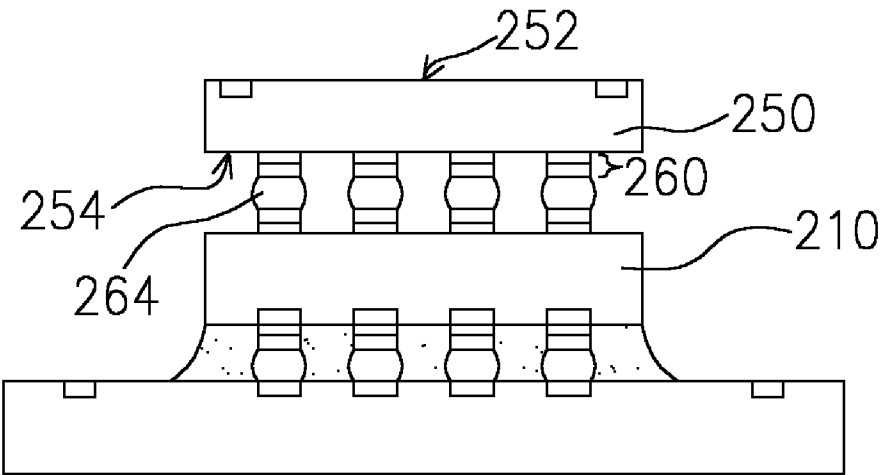


FIG. 8

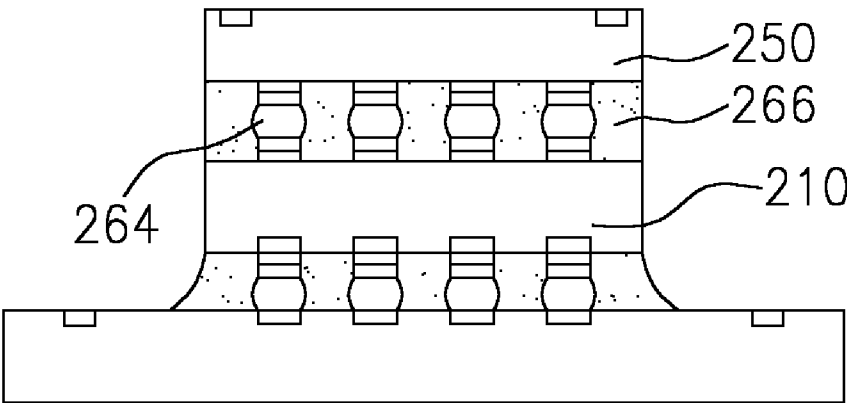


FIG. 9

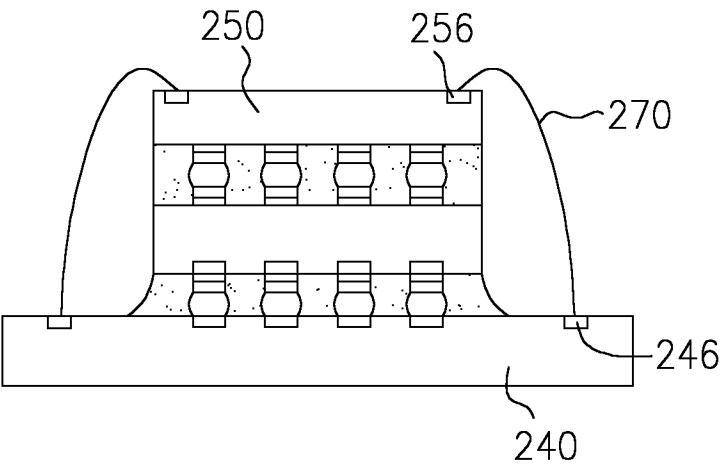


FIG. 10

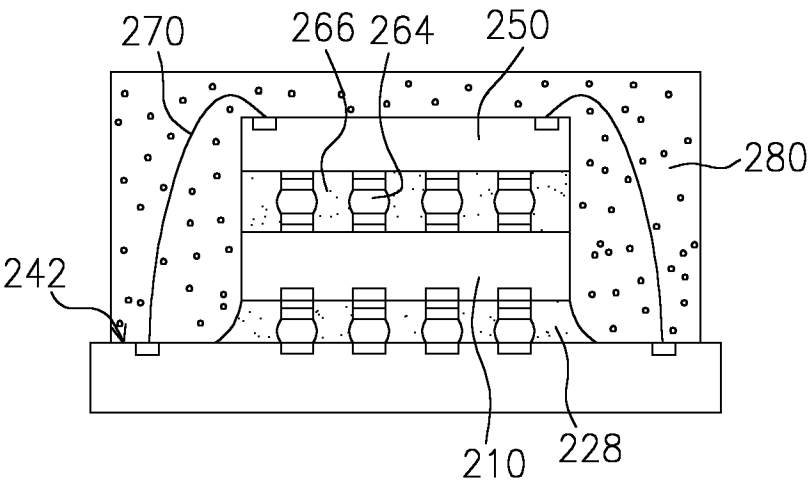


FIG. 11

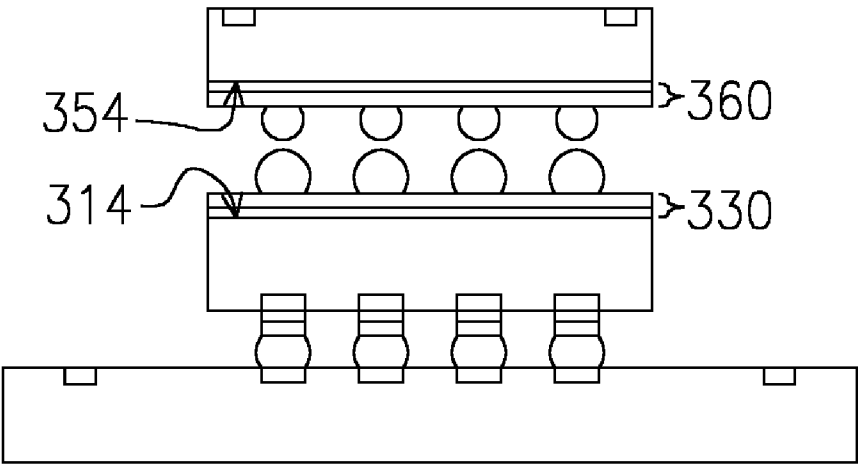


FIG. 12

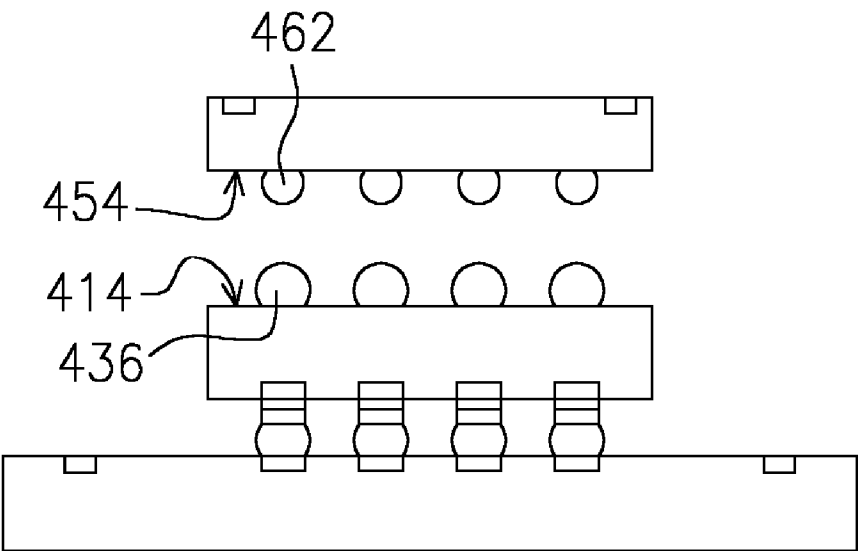


FIG. 13

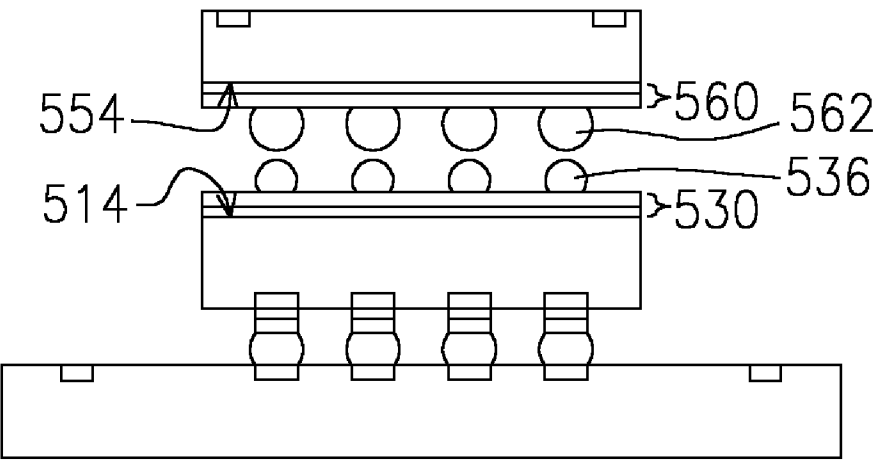


FIG. 14

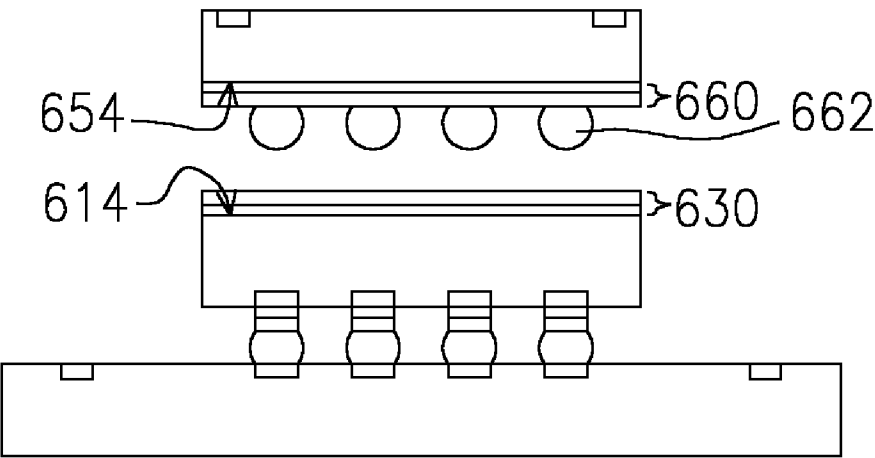


FIG. 15

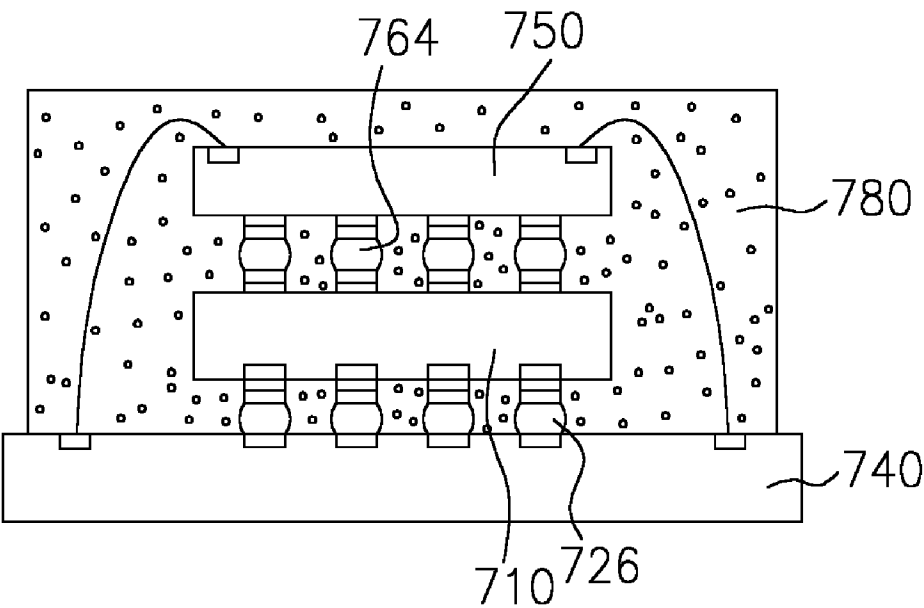


FIG. 16

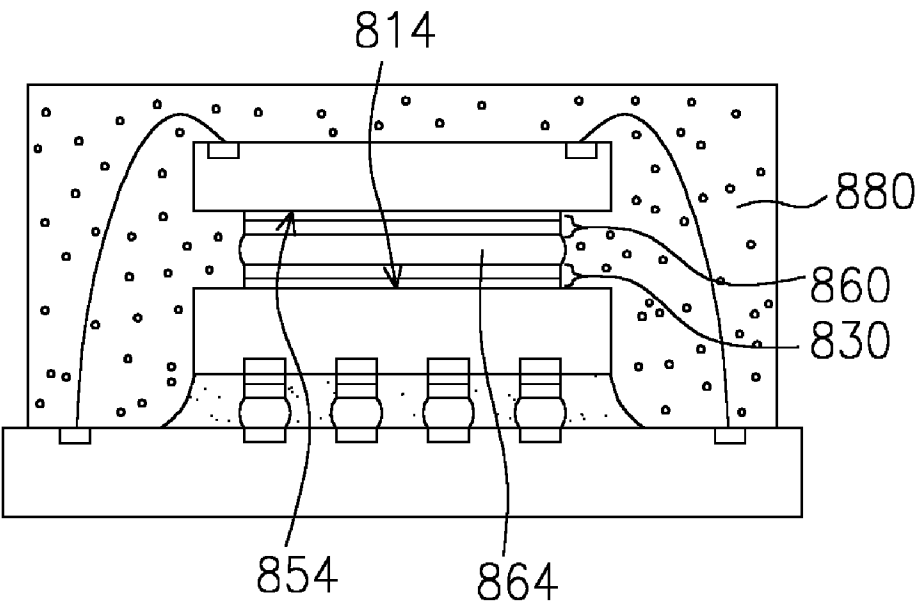


FIG. 17

MULTI-CHIP STACK PACKAGE AND FABRICATING METHOD THEREOF

Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no. 91100096, filed January 7, 2002.

Background of Invention

[0002] Field of Invention

[0003] The present invention relates to a multi-chip stack package. More particularly, the present invention relates to a multi-chip stack package and fabricating method thereof that can improve the quality of a multi-chip stack package.

[0004] Description of Related Art

[0005] As electronic technologies continue to advance, more personalized, multi-functional high-tech electronic products are being introduced into the market. The newer electronic products are characteristically smaller, lighter and slimmer so that the product will occupy less space and be more portable. In semiconductor manufacturing, many types of packages now incorporate a multi-chip concept so that volume occupation of an integrated circuit is reduced and electrical performance is improved. In a multi-chip stack package, a few chips are stacked over each other and enclosed inside the package so that horizontal sectional area of the package is greatly reduced.

[0006] Fig. 1 is a cross-sectional view of a conventional multi-chip stack package. To fabricate a multi-chip stack package, a first chip 110 having a first active surface 112 and a first chip back surface 114 is provided. The first chip 110 further includes a plurality of first bonding pads 116 positioned over the active surface 112. A substrate 120 having a substrate surface 122 is also provided. The substrate 120 has a plurality of first contacts 124 and a plurality of second contacts 126 on the substrate surface 122. The first chip 110 and the substrate 120 are joined together using a conventional flip chip method. First, a plurality of bumps 130 are formed over the first bonding pads 116 of the first chip 110. Thereafter, the first chip 110 is positioned over the substrate 120 such that each bump 130 is aligned with a corresponding first contact 124 on the substrate surface 122. A reflow process is conducted so that the bumps 130 and the first contacts 124 are bonded together. Afterwards, filler material 132 is injected into the space between the chip 110 and the substrate 120 so that the filler material 132 encloses the bumps 130. A second chip 140 having a second active surface 142 and corresponding second chip back surface 144 is provided. The second chip 140 further includes a plurality of second bonding pads 146 positioned on the second active surface 142. Through an adhesive glue 150, the second chip back surface 144 of the second chip 140 is attached to the first chip back surface 114. A wire-bonding operation is conducted to form a plurality of conductive wires 152 with one end bonded to the second bonding pads 146 of the second chip 140 and the other end bonded to the second contacts 126 on the substrate 120. Finally, the first chip 110, the second chip 140 and the conductive wires 152 are encapsulated by injecting a packaging glue 150 in a molding process.

[0007] In the aforementioned fabrication process, adhesive glue 150 is spread over the first chip back surface 114

before attaching the second chip 140 onto the first chip back surface 114 in the process of joining the first chip 110 and the second chip 140. However, if too much attaching pressure is applied to the second chip 140, some adhesive material 150 will bleed out. That is, some of the adhesive glue 150 may be forced out from the attachment region of the second chip 140. In some cases, the adhesive glue 150 may "climb" to the second active surface 142 and hence affect the wire-bonding operation. If the adhesive glue 150 creeps into the second bonding pad 146 surface, the conductive wire 152 is no longer able to bond with the second bonding pad 146. In addition, the wire-bonding head (not shown) of the wire-bonding machine (not shown) may also drag up some adhesive material. Ultimately, the quality of electrical connections between the first chip 110 and the second chip 140 is likely to be affected.

Summary of Invention

[0008] Accordingly, one object of the present invention is to provide a multi-chip stack package and a fabricating method thereof that can improve bonding quality of the multi-chip stack.

[0009] To achieve these and other advantages and in accordance with the purpose of the invention as embodied and broadly described herein, the invention provides a multi-chip stack package. The multi-chip stack package includes at least a substrate, a first chip, a second chip, a plurality of bumps, a plurality of junction interface bumps, a plurality of conductive wires, some first filler material, some second filler material and some packaging material. The substrate has a substrate surface with a plurality of first contacts and a plurality of second contacts thereon. The first chip has a first active surface and a first chip back surface. The first chip also has a plurality of first bonding pads on the first active surface. The first chip is attached to the empty area on the substrate surface such that the first active surface faces the substrate surface. The second chip has a second active surface and a corresponding second chip back surface. The second chip has a plurality of second bonding pads on the second active surface. The second chip is attached to the empty area on the first chip back surface such that the second chip back surface faces the first chip back surface. The bumps are positioned between the first bonding pads and the first contacts. The junction interface bumps are positioned between first chip back surface and the second chip back surface. One end of each conductive wire is bonded to one of the second bonding pads while the other end of the conductive wire is bonded to the second contact. The first filler material encloses the bumps. The second filler material encloses the junction interface bumps. The packaging material encloses the first chip, the second chip and the conductive wires.

[0010] According to the embodiment of this invention, an under-bump-metallurgy layer also may be formed on the first chip back surface and the second chip back surface. The under-bump-metallurgy layer includes a barrier layer and a seed layer. The barrier layer is fabricated using a material such as titanium, tungsten-titanium or chromium and the seed layer is fabricated using a material such as copper. In addition, the junction interface bumps are fabricated using a material such as lead-tin alloy.

[0011] It is to be understood that both the foregoing general description and the following detailed description

are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0012] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0013] **Fig. 1** is a cross-sectional view of a conventional multi-chip stack package;

[0014] **Figs. 2** to **11** are schematic cross-sectional views showing the progression of steps for fabricating a multi-chip stack package according to a first preferred embodiment of this invention;

[0015] **Fig. 12** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a second preferred embodiment of this invention;

[0016] **Fig. 13** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a third preferred embodiment of this invention;

[0017] **Fig. 14** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a fourth preferred embodiment of this invention;

[0018] **Fig. 15** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a fifth preferred embodiment of this invention;

[0019] **Fig. 16** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a sixth preferred embodiment of this invention; and

[0020] **Fig. 17** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a seventh preferred embodiment of this invention.

Detailed Description

[0021] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or similar parts.

[0022] **Figs. 2** to **11** are schematic cross-sectional views showing the progression of steps for fabricating a multi-chip stack package according to a first preferred embodiment of this invention. As shown in **Fig. 2**, a first chip 210 having a first active surface 212 and a first chip back surface 214 is provided. The first chip 210 further includes a plurality of first bonding pads 216 positioned on the first active surface 212 of the first chip 210. Thereafter, a process is carried out to form an under-bump-metallurgy layer. To form the under-bump-metallurgy layer, a sputtering process is conducted to form a first barrier layer 222 and a second barrier layer 232 over the first active surface 212 and the first chip back surface 214 of the first chip 210 respectively. The first barrier layer 222 and the second barrier layer 232 are fabricated

using a material such as titanium, tungsten titanium or chromium. Thereafter, an electroplating is carried out to form a first seed layer 224 and a second seed layer 234 over the first barrier layer 222 and the second barrier layer 232 respectively. The first seed layer and the second seed layer are fabricated using a metallic material such as copper. Hence, a first under-bump-metallurgy layer 220 comprising of the first barrier layer 222 and the first seed layer 224 and a second under-bump-metallurgy layer 230 comprising of the second barrier layer 232 and the second seed layer 234 are formed.

[0023] As shown in **Fig. 3**, a process for fabricating bumps is carried out. A screen printing or a photolithographic/electroplating method is used to form a plurality of first bumps 226 over the first under-bump-metallurgy layer 220 and a plurality of second bumps 236 over the second under-bump-metallurgy layer 230. The first bumps 226 must be positioned to correspond with the first bonding pads 216. The first bumps 226 and the second bumps 236 are fabricated using a lead-tin alloy having a high lead content such as a tin-lead content of 5/95.

[0024] As shown in **Figs. 3** and **4**, an etching operation is carried out using an etchant (not shown) that can remove the exposed first under-bump-metallurgy layer 220 and the second under-bump-metallurgy layer 230.

[0025] As shown in **Fig. 5**, a reflow operation is carried out so that the first bumps 226 and the second bumps 236 are transformed into mass of lumps having a spherical profile.

[0026] As shown in **Fig. 6**, a substrate 240 having a first substrate surface 242 is provided. The substrate 240 also has a plurality of first contacts 244 and a plurality of second contacts 246 positioned on the substrate surface 242. The second contacts 246 are located in a band that surrounds the first contacts 244. Next, a flip chip attachment process is carried out. The first bumps 226 are aligned with the first contacts 244 and then a reflow process is conducted so that the first bumps 226 bond with corresponding first contacts 244. Hence, the first chip 210 is firmly attached to the substrate 240.

[0027] As shown in **Fig. 7**, a first filler material 228 is injected into the space between the first chip 210 and the substrate 240. The first filler material 228 encloses the first bumps 226.

[0028] As shown in **Figs. 7** and **8**, a second chip 250 having a second active surface 252 and a corresponding second chip back surface 254 is provided. The second chip 250 further includes a plurality of second bonding pads 256 positioned around the peripheral region over the second active surface 252. Before carrying out a chip bonding process, a third under-bump-metallurgy layer 260 and a plurality of third bumps 262 are formed on the second chip back surface 254. The third under-bump-metallurgy layer 260 and the third bumps 262 are formed in a similar way as the second under-bump-metallurgy layer 230 and the second bumps 236 with one major difference. The third bumps are fabricated using a lead-tin alloy having a low lead content such as a lead-tin alloy with a lead-tin ratio of 37/63. In the chip bonding process, the third bumps 262 and the second bumps 236 are properly aligned and then a reflow operation is carried out so that the third bumps 262 and their corresponding second bumps 236 are bonded together to form a

plurality of junction interface bumps 264. Hence, the second chip 250 is firmly attached to the first chip 210.

[0029] As shown in **Fig. 9**, a second filler material 266 is injected into the space between the first chip 210 and the second chip 250. The second filler material 266 encloses the interface junction bumps 264.

[0030] As shown in **Fig. 10**, a wire-bonding operation is carried out to form a plurality of bonding wires 270. One end of each wire 270 bonded to one of the second bonding pads on the second chip 250 and the other end bonded to one of the second contacts 246 on the substrate 240.

[0031] As shown in **Fig. 11**, a packaging process is carried out by injecting a packaging material 280 to enclose the first chip 210, the second chip 250, the conductive wires 270, the first filler material 228, the second filler material 266 and the substrate surface 242. Thus, fabrication of the multi-chip stack package 200 is complete.

[0032] In the aforementioned fabrication process, the junction interface bumps 264 creates a space between the first chip 210 and the second chip 250. Filling the space with the second filler material 266 prevents any filler material from squeezing out to form a patch of bled plastic material and improves the quality of junction between the first chip 210 and the second chip 250. Furthermore, since the junction interface bumps 264 are fabricated using lead-tin alloy, the junction interface bumps 264 provide better electrical properties than the conventional thermal conductive glue.

[0033] In addition, an etching step is conducted in the aforementioned fabrication process to remove the exposed second under-bump-metallurgy layer and the third under-bump-metallurgy layer. However, the step of etching the second under-bump-metallurgy layer or the third under-bump-metallurgy layer may be deleted in a second preferred embodiment of this invention. **Fig. 12** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a second preferred embodiment of this invention. Without conducting an etching operation, the second under-bump-metallurgy layer 330 and the third under-bump-metallurgy layer 360 cover the entire surface of the first chip back surface 314 and the second chip back surface 354 respectively.

[0034] In the aforementioned fabrication process, an under-bump-metallurgy layer is formed on the back surface of both the first chip and the second chip. However, the package still functions even if the first chip back surface has no second under-bump-metallurgy layer and the second chip back surface has no third under-bump-metallurgy layer. In the third embodiment of this invention, no under-bump-metallurgy layer is formed on the first chip back surface and the second chip back surface. **Fig. 13** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a third preferred embodiment of this invention. Without an under-bump-metallurgy layer, the second bumps 436 and the third bumps 462 are directly formed on the first chip back surface 414 and the second chip back surface 454 respectively.

[0035] In the aforementioned fabrication process, second bumps with a relatively high lead content are formed over the second under-bump-metallurgy layer on the first chip back surface and third bumps with a relatively low lead content are formed over the third under-bump-metallurgy

layer on the second chip back surface. However, an alternative arrangement as shown in **Fig. 14** may be used. **Fig. 14** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a fourth preferred embodiment of this invention. In **Fig. 14**, the second bumps 536 over the second under-bump-metallurgy layer 530 on the first chip back surface 514 have a relatively low lead content and the third bumps 562 over the third under-bump-metallurgy layer 560 on the second chip back surface 554 have a relatively high lead content. With this arrangement, the second bumps 536 and the third bumps 562 may still join together to form a plurality of junction interface bumps.

[0036] In the aforementioned fabrication process, bumps with relatively high lead content and bumps with relatively low lead content are formed on the back surface of the two chips before joining the chips together. However, it is equally feasible to form a plurality of bumps over the under-bump-metallurgy layer on the back surface of just one chip before joining the first and the second chips together as shown in **Fig. 15**. **Fig. 15** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a fifth preferred embodiment of this invention. In **Fig. 15**, a plurality of bumps 662 is formed over the third under-bump-metallurgy layer 660 on the second chip back surface 654 only. Through a reflow process, the bumps 662 bond with the second under-bump-metallurgy layer 630 on the first chip back surface 614 to form junction interface bumps. One end of the interface junction bump joins up with the third under-bump-metallurgy layer 660 while the other end joins up with the second under-bump-metallurgy layer 630. The bumps 662 may be fabricated using a lead-tin alloy having a low lead content.

[0037] In the aforementioned fabrication process, a first filler material is injected into the space between the first chip and the substrate after joining the first chip and the substrate together. Similarly, a second filler material is injected into the space between the second chip and the first chip after joining the second chip and the first chip together. Finally, packaging material is used to enclose the chips. However, an alternative processing arrangement as shown in **Fig. 16** may be implemented. **Fig. 16** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a sixth preferred embodiment of this invention. In **Fig. 16**, the first bumps 726 and the junction interface bumps 764 are enclosed when packaging material 780 flows into the space between the first chip 710 and the substrate 740 and the space between the second chip 750 and the first chip 710 in the final packaging process.

[0038] In the aforementioned fabrication process, a plurality of junction interface bumps is used to bond the first chip and the second chip together. However, the fabrication process in this invention need not be restricted as such. **Fig. 17** is a schematic cross-sectional view showing a step in the fabrication of a multi-chip stack package according to a seventh preferred embodiment of this invention. In **Fig. 17**, only one junction interface bump 864 with one end joining to the second under-bump-metallurgy layer 830 on the first chip back surface 814 and the other end joining to the third under-bump-metallurgy layer 860 on the second chip back surface 854 is used. In addition, the packaging material 880 directly encloses the junction interface bump 864.

[0039] Anyone familiar with fabrication technologies may notice that the multi-chip stack package according to this invention is not limited to the structural layout as shown in the figures. In fact, each embodiment may be applied singly or in combination with others to form a complete package.

[0040] One major aspect of this invention is the positioning of at least one bump to join up the back surface of two chips. In general, the two chips have very similar expansion coefficient. Hence, the bump will not detach from the chip surfaces after repeated cyclic expansion and contraction even if the bumps joining the two chips are not enclosed by a filler material.

[0041] In summary, major advantages of this invention include:

[0042] 1. The multi-chip stack package has a plurality of junction interface bumps that creates a space between the first chip and the second chip. The space is subsequently filled with a second filler material. In this way, out-bleeding of second filler material from a space is prevented and hence junction quality between the first chip and the second chip is improved.

[0043] 2. Since the junction interface bumps are fabricated using a lead-tin alloy, electrical properties of the interface junction bumps are much better than the chips joined by conventional thermal conductive plastics. Hence, electrical performance between the first and the second chip is improved.

[0044] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

Claims

1. A multi-chip stack package, comprising: a substrate having a substrate surface with a plurality of first contacts and a plurality of second contacts thereon; a first chip having a first active surface and a corresponding first chip back surface, wherein the first chip has a plurality of first bonding pads on the first active surface and the first chip is over the substrate surfaces such that the first active surface faces the substrate surface; a second chip having a second active surface and a corresponding second chip back surface, wherein the second chip has a plurality of second bonding pads on the second active surface and the second chip is over the first chip back surface such that the second chip back surface faces the first chip back surface; a plurality of bumps connecting the first bonding pads and the first contacts; a plurality of junction interface bumps connecting the first chip back surface and the second chip back surface; a plurality of conductive wires with one end bonded to one of the second bonding pads and the other end bonded to one of the second contacts; a first filler material enclosing the bumps; a second filler material enclosing the junction interface bumps; and an encapsulate material at least enclosing the first chip, the second chip and the conductive wires.

2. The multi-chip stack package of claim 1, wherein the package further includes an under-bump-metallurgy layer on the first chip back surface.

3. The multi-chip stack package of claim 2, wherein the under-bump-metallurgy layer includes a barrier layer over the first chip back surface.

4. The multi-chip stack package of claim 3, wherein the barrier layer is fabricated using a metallic material selected from the group consisting of titanium, titanium tungsten and chromium.

5. The multi-chip stack package of claim 4, wherein the under-bump-metallurgy layer further includes a seed layer over the barrier layer and the seed layer is fabricated using a metallic material.

6. The multi-chip stack package of claim 1, wherein the package further includes an under-bump-metallurgy layer on the second chip back surface.

7. The multi-chip stack package of claim 6, wherein the under-bump-metallurgy layer includes a barrier layer over the second chip back surface and the barrier layer is fabricated using a metallic material selected from the group consisting of titanium, titanium tungsten and chromium.

8. The multi-chip stack package of claim 7, wherein the under-bump-metallurgy layer further includes a seed layer over the barrier layer.

9. The multi-chip stack package of claim 8, wherein the seed layer is fabricated using a metallic material.

10. The multi-chip stack package of claim 1, wherein the junction interface bumps are fabricated using a lead-tin alloy.

11. A multi-chip bonded structure, at least comprising: a first chip having a first chip back surface; a second chip over the first chip back surface, wherein the second chip has a second chip back surface and the second chip back surface faces the first chip back surface; and at least one bump between the first chip back surface and the second chip back surface.

12. The multi-chip bonded structure of claim 11, wherein the structure further includes an under-bump-metallurgy layer on the first chip back surface.

13. The multi-chip bonded structure of claim 12, wherein the under-bump-metallurgy layer includes a barrier layer over the first chip back surface.

14. The multi-chip bonded structure of claim 13, wherein the barrier layer is fabricated using a metallic material selected from the group consisting of titanium, titanium tungsten and chromium.

15. The multi-chip bonded structure of claim 13, wherein the under-bump-metallurgy layer further includes a seed layer over the barrier layer and that the seed layer is fabricated using a metallic material.

16. The multi-chip bonded structure of claim 11, wherein the package further includes an under-bump-metallurgy layer on the second chip back surface.

17. The multi-chip bonded structure of claim 16, wherein the under-bump-metallurgy layer includes a barrier layer over the second chip back surface and the barrier layer is fabricated using a metallic material selected from a group consisting of titanium, titanium tungsten and chromium.

18. The multi-chip bonded structure of claim 17, wherein the under-bump-metallurgy layer further includes a seed layer over the barrier layer.

19. The multi-chip bonded structure of claim 18, wherein the seed layer is fabricated using a metallic material including copper.

20. The multi-chip bonded structure of claim 11, wherein the bumps are fabricated using a lead-tin alloy.

21. The multi-chip bonded structure of claim 11, wherein the structure further includes a filler material that encloses the bumps.

* * * * *