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(54) **Title**: METHOD AND APPARATUS FOR COMPENSATING OFFSET DRIFT WITH TEMPERATURE

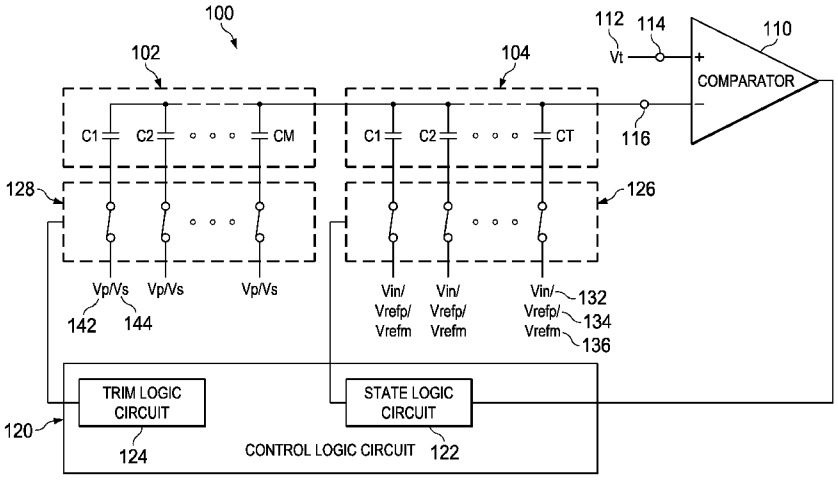

FIG. 1

(57) **Abstract**: In described examples of an analog to digital converter (ADC) (100), the ADC (100) includes a comparator (110) that receives a threshold voltage (112). A set of elementary capacitors (104) is coupled to the comparator (110) and receives one of an input voltage (132) and a set of reference voltages. A set of M offset capacitors (102) is coupled to the comparator (110) and receives one of a primary voltage (142) and a secondary voltage (144). M is an integer. A difference in the primary voltage (142) and the secondary voltage (144) varies linearly with temperature.

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METHOD AND APPARATUS FOR COMPENSATING OFFSET DRIFT WITH TEMPERATURE

[0001] This relates generally to an analog front end (AFE), and more particularly to compensating offset drift with temperature in the AFE.

BACKGROUND

[0002] Analog systems and digital systems are commonly implemented in an integrated circuit using system on-chip (SOC) technology. Such systems commonly include an analog front end (AFE) circuit. The AFE circuit operates as an interface between an external input terminal, through which analog signals are input, and a digital signal processing unit that processes the received signals in digital format.

[0003] The AFE circuit is widely used in various devices, such as down converters for wireless digital communication devices, digital image scanners, digital cameras and voice codecs. The AFE circuit includes an amplifier and an analog to digital converter (ADC). The amplifier amplifies the received analog signals, and the ADC converts the amplified analog signals into digital signals. The AFE along with the ADC has an associated offset. This offset drifts with temperature. The existing techniques provide dynamic storing of offset. However, these techniques have at least the following inherent shortcomings.

[0004] First, dynamically storing of offset requires an offset storing phase. If sampling mode of the ADC is used for storing offset, then a comparator in the ADC cannot be powered down during sampling phase. If conversion mode of the ADC is used for storing offset, it slows down the ADC.

[0005] Second, all devices in the AFE are required to store their offset individually to avoid saturation. This increases the complexity of the AFE; and/or

[0006] Third, dynamic storing of offset results in storage of noise also. This increases a white noise of the AFE.

SUMMARY

[0007] In described examples of an analog to digital converter (ADC), the ADC includes a comparator that receives a threshold voltage. A set of elementary capacitors is coupled to the

comparator and receives one of an input voltage and a set of reference voltages. A set of M offset capacitors is coupled to the comparator and receives one of a primary voltage and a secondary voltage. M is an integer. A difference in the primary voltage and the secondary voltage varies linearly with temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 illustrates an analog to digital converter (ADC) of example embodiments.

[0009] FIG. 2 is a graph of how voltages vary with temperature in example embodiments.

[0010] FIG. 3 illustrates an analog front end (AFE), according to example embodiments.

[0011] FIG. 4 illustrates a primary voltage generation circuit.

[0012] FIG. 5 illustrates a secondary voltage generation circuit.

[0013] FIG. 6 is a flowchart of a method of compensating offset drift, according to example embodiments.

[0014] FIG. 7 illustrates a computing device of example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0015] FIG. 1 illustrates an analog to digital converter (ADC) 100 of example embodiments. The ADC 100 includes a comparator 110 that receives a threshold voltage Vt 112. The comparator 110 includes a non-inverting terminal 114 and an inverting terminal 116. The comparator 110 receives the threshold voltage Vt 112 at the non-inverting terminal 114. The ADC 100 also includes a set of elementary capacitors 104 represented as C1, C2 to CT. The ADC 100 includes a set of M offset capacitors 102 represented as CO1, CO2 to COM. M is an integer. The set of elementary capacitors 104 and the set of M offset capacitors 102 are coupled to the inverting terminal 116 of the comparator 110.

[0016] A control logic circuit 120 is coupled to the comparator 110. The control logic circuit 120 includes a state logic circuit 122 and a trim logic circuit 124. The state logic circuit 122 is coupled to a first set of switches 126. The set of elementary capacitors 104 receives one of an input voltage Vin 132 and a set of reference voltages through the first set of switches 126. The set of reference voltages includes a positive reference voltage Vrefp 134 and a negative reference voltage Vrefm 136.

[0017] The trim logic circuit 124 is coupled to a second set of switches 128. The set of M offset capacitors 102 receive a primary voltage Vp 142 and a secondary voltage Vs 144 through the second set of switches 128. The ADC 100 may include one or more additional components.

[0018] The operation of the ADC 100 illustrated in FIG. 1 is explained now. A difference in the primary voltage Vp 142 and the secondary voltage Vs 144 varies linearly with temperature. The primary voltage Vp 142 increases linearly with increase in temperature, and the secondary voltage Vs 144 decreases linearly with increase in temperature. In one example, the secondary voltage Vs 144 increases linearly with increase in temperature, and the primary voltage Vp 142 decreases linearly with increase in temperature. The property of linear dependence of the primary voltage Vp 142 and the secondary voltage Vs 144 on temperature is used for compensating offset drift with temperature of ADC 100. In one example, the property is used for compensating offset drift with temperature of an analog front end (AFE) of which ADC 100 is a part.

[0019] The ADC 100 operates in a set of trim phases. Each trim phase of the set of trim phases includes a sampling mode and a conversion mode. The set of trim phases includes a first trim phase, a second trim phase, a third trim phase and a fourth trim phase. The first trim phase and the second trim phase occur at a first temperature (T1), and the third trim phase and the fourth trim phase occur at a second temperature (T2). The control logic circuit 120 synchronizes the state logic circuit 122 and the trim logic circuit 124 during the sampling mode and the conversion mode.

[0020] In each trim phase of the set of trim phases, the set of elementary capacitors 104 are coupled to the input voltage Vin 132 in the sampling mode. The state logic circuit 122 generates a set of first control signals to activate the first set of switches 126 which couple bottom plates of the set of elementary capacitors 104 to the input voltage Vin 132 in the sampling mode. Also, in each trim phase, the set of elementary capacitors 104 are coupled to one of the positive reference voltage Vrefp 134 and the negative reference voltage Vrefm 136 in the conversion mode. The state logic circuit 122 generates the set of first control signals to activate the first set of switches 126 which couple bottom plates of the set of elementary capacitors 104 to one of the positive reference voltage Vrefp 134 and the negative reference voltage Vrefm 136.

[0021] In the first trim phase, the set of M offset capacitors 102 are coupled to the primary voltage Vp 142 both in the sampling mode and in the conversion mode. The ADC 100 generates a first digital code in the first trim phase. The trim logic circuit 124 generates a set of second control signals to activate the second set of switches 128 which couple bottom plates of the set of M offset capacitors 102 to the primary voltage Vp 142 both in the sampling mode and the

conversion mode. The first trim phase occurs at the first temperature (T1).

[0022] The sampling mode and the conversion mode during the first trim phase are explained now. A similar methodology is followed in each trim phase of the set of trim phases. In the sampling mode, the state logic circuit 122 generates the set of first control signals which couple bottom plates of the set of elementary capacitors 104 to the input voltage Vin 132. The trim logic circuit 124 generates the set of second control signals which couple bottom plates of the set of M offset capacitors 102 to the primary voltage Vp 142.

[0023] In the conversion mode, the ADC 100 generates a digital output corresponding to the input voltage Vin 132 and the primary voltage Vp 142 using a binary search technique. The binary search technique includes multiple cycles. In a cycle of multiple cycles, the state logic circuit 122 generates the set of first control signals to couple bottom plates of the set of elementary capacitors 104 to one of the positive reference voltage Vrefp 134 and the negative reference voltage Vrefm 136. The trim logic circuit 124 generates the set of second control signals which couple bottom plates of the set of M offset capacitors 102 to the primary voltage Vp 142.

[0024] A weighted voltage is generated at the inverting terminal 116 of the comparator 110. An estimated DAC (digital to analog converter) voltage is a weighted sum of the positive reference voltage Vrefp 134 and the negative reference voltage Vrefm 136 applied at the bottom plates of the set of elementary capacitors 104 and the primary voltage Vp 142 applied at the bottom plates of the set of M offset capacitors 102. Thus, the weighted voltage is an error or a difference between the input voltage Vin 132 and the estimated DAC voltage.

[0025] The comparator 110 compares the weighted voltage and the threshold voltage Vt 112 to generate a digital bit. The digital bit is provided to the state logic circuit. In each cycle of the binary search technique, the state logic circuit 122 generates the set of first control signals to couple a different number of capacitors in the set of elementary capacitors 104 to the positive reference voltage Vrefp 134 based on the digital bit.

[0026] The multiple cycles of the binary search technique further reduce the error in binary scaled steps. The digital bits generated after each cycle together forms the digital output. A 12 bit resolution ADC requires 12 successive cycles to resolve the input voltage Vin 132 to a 12 bit digital output.

[0027] The above description of the sampling mode and the conversion mode in the first trim

phase is analogously applicable to each trim phase of the set of trim phases.

[0028] In the second trim phase, the set of M offset capacitors 102 are coupled to the primary voltage Vp 142 in the sampling mode and to the secondary voltage Vs 144 in the conversion mode. The ADC 100 generates a second digital code in the second trim phase. The trim logic circuit 124 generates the set of second control signals to activate the second set of switches 128 which couple bottom plates of the set of M offset capacitors 102 to the primary voltage Vp 142 in the sampling mode and to the secondary voltage Vs 144 in the conversion mode. The second trim phase occurs at the first temperature (T1).

[0029] After the second trim phase, the secondary voltage Vs 144 is modified such that the first digital code is equal to the second digital code. This ensures that the primary voltage Vp 142 is equal to the secondary voltage Vs 144 at the first temperature (T1). Thus, any offset added to the ADC 100 because of the set of M offset capacitors 102 is cancelled after the second trim phase.

[0030] In the third trim phase, the set of M offset capacitors 102 are coupled to the primary voltage Vp 142 both in the sampling mode and in the conversion mode. The ADC 100 generates a third digital code in the third trim phase. The trim logic circuit 124 generates the set of second control signals to activate the second set of switches 128 which couple bottom plates of the set of M offset capacitors 102 to the primary voltage Vp 142 both in the sampling mode and the conversion mode. The ADC 100 generates a third digital code in the third trim phase. The third trim phase occurs at the second temperature (T2).

[0031] A sign of the third digital code is used to determine a direction of the offset drift. If the third digital code is positive, the offset drift of the ADC 100 is positive, and if the third digital code is negative then the offset drift of the ADC 100 is negative. The fourth trim phase uses the sign of the third digital code to compensate offset drift with temperature of the ADC 100.

[0032] In the fourth trim phase, if the third digital code is positive, the set of M offset capacitors 102 are coupled to the secondary voltage Vs 144 in the sampling mode and to the primary voltage Vp 142 in the conversion mode. In the fourth trim phase, if the third digital code is negative, the set of M offset capacitors 102 are coupled to the primary voltage Vp 142 in the sampling mode and to the secondary voltage Vs 144 in the conversion mode. Thus, the primary voltage Vp 142 is used in one of the sampling mode and conversion mode based on the direction of the offset drift which may be positive or negative. The ADC 100 generates a fourth

digital code in the fourth trim phase. The fourth trim phase occurs at the second temperature (T2).

[0033] After the fourth trim phase, N offset capacitors of the set of M offset capacitors are coupled to a ground terminal such that the fourth digital code is equal to a defined value. N is an integer. In one example, the defined value is 0. In another example, the defined value is fixed at the time of manufacturing a device with the ADC 100. Thus, the N offset capacitors coupled to the ground terminal are used to cancel the offset drift of the ADC 100. A slope of the offset drift is taken into consideration by changing a number of capacitors in the set of M offset capacitors.

[0034] An offset voltage provided by the set of M offset capacitors is defined as:

$$Voff = (sign) \times (Vp(T) - Vs(T)) \times \frac{(M-N)Coff}{Csamp} - Do \quad (1)$$

where, sign is the sign of the third digital code, Coff is a capacitance of each capacitor in the set of M offset capacitors 102, Csamp is a capacitance of the set of elementary capacitors 104, T is ambient temperature and Do is an offset at the first temperature T1. Thus, at the first temperature T1, any offset added to the ADC 100 because of the set of M offset capacitors 102 is cancelled by making the primary voltage Vp 142 equal to the secondary voltage Vs 144. Also, at temperature T2, the offset voltage (Voff) provided by the set of M offset capacitors is made equal to the offset associated with the ADC 100. Thus, the offset voltage (Voff) linearly tracks the offset associated with the ADC 100 at all temperatures. Accordingly, this feature is used to cancel the offset drift with temperature of the ADC 100.

[0035] Thus, any offset drift with temperature of ADC 100 is compensated. This technique is also applicable to a switched capacitor circuit with any analog front end (AFE). The ADC 100 also overcomes the problem of dynamic offset storing. Also, the technique does not result in increase in white noise of an AFE of which the ADC 100 is a part.

[0036] FIG. 2 is a graph 200 of how voltages vary with temperature in example embodiments. The graph 200 is explained in connection with the primary voltage Vp 142 and the secondary voltage Vs 144 used in ADC 100 illustrated in FIG. 1. The primary voltage Vp 142 and the secondary voltage Vs 144 varies linearly with temperature. The primary voltage Vp 142 increases linearly with increase in temperature, and the secondary voltage Vs 144 decreases linearly with increase in temperature. In one example, a difference in the primary voltage Vp 142 and the secondary voltage Vs 144 varies linearly with temperature. In another example, one of the primary voltage Vp 142 and the secondary voltage Vs 144 varies linearly with temperature

while the other one is constant with temperature. The property of linear dependence of the primary voltage Vp 142 and the secondary voltage Vs 144 on temperature is used for compensating offset drift with temperature of ADC 100. In one example, the property is used for compensating offset drift with temperature of an analog front end (AFE) of which ADC 100 is a part.

[0037] The ADC 100 operates in the set of trim phases. The first trim phase and the second trim phase occur at a first temperature (T1) 202, and the third trim phase and the fourth trim phase occur at a second temperature (T2) 204. After the second trim phase, the secondary voltage Vs 144 is modified such that the first digital code is equal to the second digital code. This ensures that the primary voltage Vp 142 is equal to the secondary voltage Vs 144 at the first temperature (T1) 202. After the fourth trim phase, N offset capacitors of the set of M offset capacitors are coupled to a ground terminal such that the fourth digital code is equal to a defined value. N is an integer. In one example, the defined value is 0.

[0038] FIG. 3 illustrates an analog front end (AFE) 300, according to example embodiments. The AFE includes a programmable gain amplifier (PGA) 302, a low pass filter (LPF) 304, an analog to digital converter (ADC) driver 306 and an ADC 308. The PGA 302 receives an input signal IN 301. The LPF 304 is coupled to the PGA 302. The ADC driver 306 is coupled to the LPF 304, and the ADC 308 is coupled to the ADC driver 306. The ADC 308 generates a digital output Dout 310.

[0039] The PGA 302 amplifies the input signal IN 301 to generate an amplified signal. The LPF 304 filters the amplified signal with a low frequency band to generate a filtered signal. The ADC driver 306 amplifies the filtered signal to generate a processed signal with a fixed center power at a fixed set point of the ADC 308. The ADC 308 generates the digital output Dout 310 from the processed signal. The ADC 308 is analogous to the ADC 100 in connection and operation.

[0040] The ADC 308 is used for compensating offset drift with temperature of the AFE 300. The offset drift compensation is applied on the ADC 308 which cancels the offset drift of the AFE 300. The ADC 308 includes a set of M offset capacitors similar to the ADC 100 which are used for compensating offset drift with temperature in the AFE 300. Because the ADC 308 is a last element in the AFE 300, it cancels the offset drift associated with other devices in the AFE 300.

[0041] FIG. 4 illustrates a primary voltage generation circuit 400. The primary voltage generation circuit 400, in one example, is used to generate the primary voltage Vp 142 illustrated in FIG. 1. The primary voltage generation circuit 400 includes a current mirror circuit 410 that receives a power supply VDD 408. The current mirror circuit 410 includes a first transistor N1 402 and a second transistor N2 404. In one version, when an area of the first transistor N1 402 is A, the area of the second transistor N2 404 is N*A, where N is a positive integer. Both the first transistor N1 402 and the second transistor N2 404 operate at a same current, so a first current I1 is generated across a first resistor R1 412. The current mirror circuit 410 mirrors the first current I1 across a second resistor R2 416. Thus, a primary current Ip flows through the second resistor R2 416. The primary current Ip is equal to the first current I1. A primary voltage Vp 420 is generated across the second resistor R2 416. The primary current Ip is defined as:

$$Ip = \frac{(Vbe1 - Vbe2)}{R1} = \frac{V_T \ln\left(\frac{I1}{Is1}\right) - V_T \ln\left(\frac{I1}{Is2}\right)}{R1} = \frac{V_T \ln\left(\frac{Is2}{Is1}\right)}{R1} = \frac{V_T \ln(N)}{R1} \quad (2)$$

where Vbe1 is a voltage across base-emitter terminals of the first transistor N1 402, Vbe2 is a voltage across base-emitter terminals of the second transistor N2 404, Is1 is saturation current in the first transistor N1 402, Is2 is saturation current in the second transistor N2 404.

[0042] The primary voltage Vp 420 is defined as:

$$Vp = Ip * R2 = V_T \ln(N)\frac{R2}{R1} = \frac{KT}{q}\ln(N)\frac{R2}{R1} = T * CONSTANT \quad (3)$$

Where, V_T =KT/q, K is the Boltzmann constant, T is the temperature in Kelvin and q is the charge of electron.

[0043] Thus, the primary voltage Vp 420 is directly proportional to the temperature (T). The primary voltage Vp 420 increases linearly with increase in temperature. The primary voltage Vp 420 is similar to the primary voltage Vp 142. The primary voltage generation circuit 400 is one of one of the many ways of generating the primary voltage Vp, and variations are possible.

[0044] FIG. 5 illustrates a secondary voltage generation circuit 500. The secondary voltage generation circuit 500, in one example, is used to generate the secondary voltage Vs 144 illustrated in FIG. 1. The secondary voltage generation circuit 500 includes a current mirror circuit 510 that receives a power supply VDD 508. The current mirror circuit 510 includes a first transistor N1 502. A first current I1 flows through a first resistor R1 512. The current mirror circuit 510 mirrors the first current I1 across a second resistor R2 516. Thus, a secondary current Is flows through the second resistor R2 516. The secondary current Is is equal to the first current

I1. A secondary voltage Vs 520 is generated across the second resistor R2 516. A voltage across base-emitter terminals of the first transistor N1 502 is defined as

$$Vbe = V_T \ln(\frac{Ic}{Is}) \quad (4)$$

where, Ic is current through collector terminal of the first transistor N1 502 and Is is saturation current. The collector current variation with temperature is defined as:

$$Ic = DT^{\alpha} \quad (5)$$

where, D and α are constants. The saturation current variation with temperature is defined as:

$$Is = CT^{\eta}\exp(-\frac{qEg}{KT}) \quad (6)$$

where, Eg is bandgap, C, K, q and η are constants with respect to temperature variations. By replacing equations (5) and (6) in equation (4), the following equation (7) is obtained:

$$Vbe = Eg + \frac{Vbe(To)-Eg}{To} T + (\alpha - \eta)\frac{kT}{q}\ln(\frac{T}{To}) \quad (7)$$

where To is a defined temperature.

[0045] On differentiating equation (7), Vbe is inversely proportional to the temperature (T). The secondary voltage Vs 520 is defined as

$$V_s = \frac{R4*V_{be}}{R3} \quad (8)$$

[0046] Thus, the secondary voltage Vs 520 is proportional to Vbe. The secondary voltage Vs 520 is similar to Vbe and decreases linearly with increase in temperature. The secondary voltage Vs 520 is similar to the secondary voltage Vs 144. The secondary voltage generation circuit 500 is one of one of the many ways of generating the secondary voltage Vs, and variations are possible.

[0047] FIG. 6 is a flowchart 600 of a method of compensating offset drift, according to example embodiments. The flowchart 600 is explained in connection with the ADC 100 illustrated in FIG. 1. The ADC 100 is operated in a set of trim phases. Each trim phase includes a sampling mode and a conversion mode. Each trim phase includes the following steps. At step 602, an input voltage is provided to a set of elementary capacitors in the ADC in the sampling mode. A set of reference voltages is provided to the set of elementary capacitors in the ADC in the conversion mode, at step 604. The set of reference voltages includes a positive reference voltage and a negative reference voltage.

[0048] In ADC 100, the set of elementary capacitors 104 are coupled to the input voltage Vin 132 in the sampling mode. The state logic circuit 122 generates a set of first control signals to

activate the first set of switches 126 which couple bottom plates of the set of elementary capacitors 104 to the input voltage Vin 132 in the sampling mode. Also, in each trim phase, the set of elementary capacitors 104 are coupled to one of the positive reference voltage Vrefp 134 and the negative reference voltage Vrefm 136 in the conversion mode. The state logic circuit 122 generates the set of first control signals to activate the first set of switches 126 which couple bottom plates of the set of elementary capacitors 104 to one of the positive reference voltage Vrefp 134 and the negative reference voltage Vrefm 136.

[0049] At step 606, one of a primary voltage and a secondary voltage are provided to a set of M offset capacitors in the SAR ADC. M is an integer. The primary voltage and the secondary voltage varies linearly with temperature. The primary voltage increases linearly with increase in temperature, and the secondary voltage decreases linearly with increase in temperature. In one example, a difference in the primary voltage and the secondary voltage varies linearly with temperature. The set of trim phases includes a first trim phase and a second trim phase occurring at a first temperature, and a third trim phase and a fourth trim phase occurring at a second temperature.

[0050] A first digital code is generated in the first trim phase. A second digital code is generated in the second trim phase. A third digital code is generated in the third trim phase and a fourth digital code is generated in the fourth trim phase. In the first trim phase, the set of M offset capacitors are coupled to the primary voltage both in the sampling mode and in the conversion mode. In the second trim phase, the set of M offset capacitors are coupled to the primary voltage in the sampling mode and to the secondary voltage in the conversion mode.

[0051] After the second trim phase, the secondary voltage provided to the set of M offset capacitors in the second trim phase is modified such that the first digital code is equal to the second digital code. This ensures that the primary voltage is equal to the secondary voltage at the first temperature. Thus, any offset added to the ADC 100 because of the set of M offset capacitors is cancelled after the second trim phase.

[0052] In the third trim phase, the set of M offset capacitors are coupled to the primary voltage both in the sampling mode and in the conversion mode. In the fourth trim phase, if the third digital code is positive, the set of M offset capacitors are coupled to the secondary voltage in the sampling mode and to the primary voltage in the conversion mode. In the fourth trim phase, if the third digital code is negative, the set of M offset capacitors are coupled to the primary voltage

in the sampling mode and to the secondary voltage in the conversion mode.

[0053] After the fourth trim phase, N capacitors of the set of M capacitors are coupled to a ground terminal such that the fourth digital code is equal to a defined value, where N is an integer. In one example, the defined value is 0. Thus, the N offset capacitors coupled to the ground terminal are used to cancel the offset drift of the ADC 100. The fourth trim phase uses the sign of the third digital code to compensate offset drift with temperature of the ADC 100.

[0054] FIG. 7 illustrates a computing device 700 of example embodiments. The computing device 700 is, or is incorporated into, a mobile communication device, such as a mobile phone, a personal digital assistant, a transceiver, a personal computer, or any other type of electronic system. The computing device 700 may include one or more additional components.

[0055] In some embodiments, the computing device 700 includes a megacell or a system-on-chip (SoC) which includes a processing unit 712 such as a CPU (central processing unit), a memory module 714 (e.g., random access memory (RAM)) and a tester 710. For example, the processing unit 712 can be a CISC-type (complex instruction set computer) CPU, RISC-type CPU (reduced instruction set computer), or a digital signal processor (DSP).

[0056] The memory module 714 (which can be memory such as RAM, flash memory, or disk storage) stores one or more software applications 730 (e.g., embedded applications) that, when executed by the processing unit 712, performs any suitable function associated with the computing device 700. The tester 710 includes logic that supports testing and debugging of the computing device 700 executing the software applications 730.

[0057] For example, the tester 710 is useful to emulate a defective or unavailable component(s) of the computing device 700 to allow verification of how the component(s), if actually existing on the computing device 700, would perform in various situations (e.g., how the component(s) would interact with the software applications 730). In this way, the software applications 730 can be debugged in an environment which resembles post-production operation.

[0058] The processing unit 712 usually includes memory and logic, which store information frequently accessed from the memory module 714. The computing device 700 includes a logic unit 720. The logic unit 720 is coupled to the processing unit 712 and the memory module 714. The logic unit 720 includes an analog to digital converter (ADC) 718. The ADC 718 is similar in connection and operation to the ADC 100. The ADC 718 includes a set of M offset capacitors. The set of M offset capacitors receive a primary voltage and a secondary voltage.

[0059] The primary voltage and the secondary voltage varies linearly with temperature. The primary voltage increases linearly with increase in temperature, and the secondary voltage decreases linearly with increase in temperature. In one example, a difference in the primary voltage and the secondary voltage varies linearly with temperature. The property of linear dependence of the primary voltage and the secondary voltage on temperature is used for compensating offset drift with temperature of ADC 718. In one example, the property is used for compensating offset drift with temperature of an analog front end (AFE) of which ADC 718 is a part.

[0060] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An analog to digital converter (ADC) comprising:

a comparator configured to receive a threshold voltage;

a set of elementary capacitors coupled to the comparator, and configured to receive one of an input voltage and a set of reference voltages; and

a set of M offset capacitors coupled to the comparator, and configured to receive one of a primary voltage and a secondary voltage, M is an integer, wherein a difference in the primary voltage and the secondary voltage varies linearly with temperature.

2. The ADC of claim 1, wherein the set of reference voltages includes a positive reference voltage and a negative reference voltage.

3. The ADC of claim 1, wherein the primary voltage increases linearly with increase in temperature, and the secondary voltage decreases linearly with increase in temperature.

4. The ADC of claim 1, wherein the comparator includes:

a non-inverting terminal configured to receive the threshold voltage; and

an inverting terminal coupled to the set of elementary capacitors and the set of M offset capacitors.

5. The ADC of claim 1 is configured to operate in a set of trim phases and each trim phase of the set of trim phases includes a sampling mode and a conversion mode, the set of trim phases includes: a first trim phase, the ADC is configured to generate a first digital code in the first trim phase; a second trim phase, the ADC is configured to generate a second digital code in the second trim phase; a third trim phase, the ADC is configured to generate a third digital code in the third trim phase; and a fourth trim phase, the ADC is configured to generate a fourth digital code in the fourth trim phase.

6. The ADC of claim 1, wherein the first trim phase and the second trim phase occur at a first temperature, and the third trim phase and the fourth trim phase occur at a second temperature.

7. The ADC of claim 1, wherein in each trim phase of the set of trim phases: the set of elementary capacitors are coupled to the input voltage in the sampling mode; and the set of elementary capacitors are coupled to one of the positive reference voltage and the negative reference voltage in the conversion mode.

8. The ADC of claim 1, wherein in the first trim phase the set of M offset capacitors is coupled to the primary voltage both in the sampling mode and in the conversion mode.

9. The ADC of claim 1, wherein in the second trim phase the set of M offset capacitors are coupled to the primary voltage in the sampling mode and to the secondary voltage in the conversion mode.

10. The ADC of claim 9, wherein after the second trim phase, the secondary voltage provided to the set of M offset capacitors is modified such that the first digital code is equal to the second digital code.

11. The ADC of claim 1, wherein in the third trim phase the set of M offset capacitors are coupled to the primary voltage both in the sampling mode and in the conversion mode.

12. The ADC of claim 1, wherein in the fourth trim phase, if the third digital code is positive, the set of M offset capacitors are coupled to the secondary voltage in the sampling mode and to the primary voltage in the conversion mode, and if the third digital code is negative, the set of M offset capacitors are coupled to the primary voltage in the sampling mode and to the secondary voltage in the conversion mode.

13. The ADC of claim 12, wherein after the fourth trim phase, N offset capacitors of the set of M offset capacitors are coupled to a ground terminal such that the fourth digital code is equal to a defined value, where N is an integer.

14. A method of compensating offset drift, comprising:

operating an analog to digital converter (ADC) in a set of trim phases, each trim phase of the set of trim phases including a sampling mode and a conversion mode, and each trim phase further including: providing an input voltage to a set of elementary capacitors in the ADC in the sampling mode; providing a set of reference voltages to the set of elementary capacitors in the ADC in the conversion mode; and providing one of a primary voltage and a secondary voltage to a set of M offset capacitors in the ADC, M is an integer, wherein a difference in the primary voltage and the secondary voltage varies linearly with temperature.

15. The method of claim 14, wherein:

the set of reference voltages includes a positive reference voltage and a negative reference voltage; and

the primary voltage increases linearly with increase in temperature, and the secondary voltage decreases linearly with increase in temperature.

16. The method of claim 14, wherein the set of trim phases further includes a first trim phase and a second trim phase occurring at a first temperature, and a third trim phase and a fourth trim phase occurring at a second temperature.

17. The method of claim 16 further comprising:

generating a first digital code in the first trim phase;

generating a second digital code in the second trim phase;

generating a third digital code in the third trim phase; and

generating a fourth digital code in the fourth trim phase.

18. The method of claim 17 further comprising:

coupling the set of M offset capacitors to the primary voltage both in the sampling mode and in the conversion mode, in the first trim phase;

coupling the set of M offset capacitors to the primary voltage in the sampling mode and to the secondary voltage in the conversion mode, in the second trim phase; and

modifying the secondary voltage provided to the set of M offset capacitors in the second trim phase such that the first digital code is equal to the second digital code.

19. The method of claim 17 further comprising:

coupling the set of M offset capacitors to the primary voltage both in the sampling mode and in the conversion mode, in the third trim phase;

coupling the set of M offset capacitors to the secondary voltage in the sampling mode and to the primary voltage in the conversion mode, in the fourth trim phase if the third digital code is positive;

coupling the set of M offset capacitors to the primary voltage in the sampling mode and to the secondary voltage in the conversion mode, in the fourth trim phase if the third digital code is negative; and

coupling N capacitors of the set of M capacitors to a ground terminal such that the fourth digital code is equal to a defined value, where N is an integer.

20. A computing device comprising:

a processing unit;

a memory module coupled to the processing unit; and

a logic unit coupled to the processing unit and the memory module, the logic unit including an analog to digital converter (ADC), the ADC including: a comparator configured to

receive a threshold voltage; a set of elementary capacitors coupled to the comparator, and configured to receive one of an input voltage and a set of reference voltages; and a set of M offset capacitors coupled to the comparator, and configured to receive one of a primary voltage and a secondary voltage, M is an integer, wherein a difference in the primary voltage and the secondary voltage varies linearly with temperature.

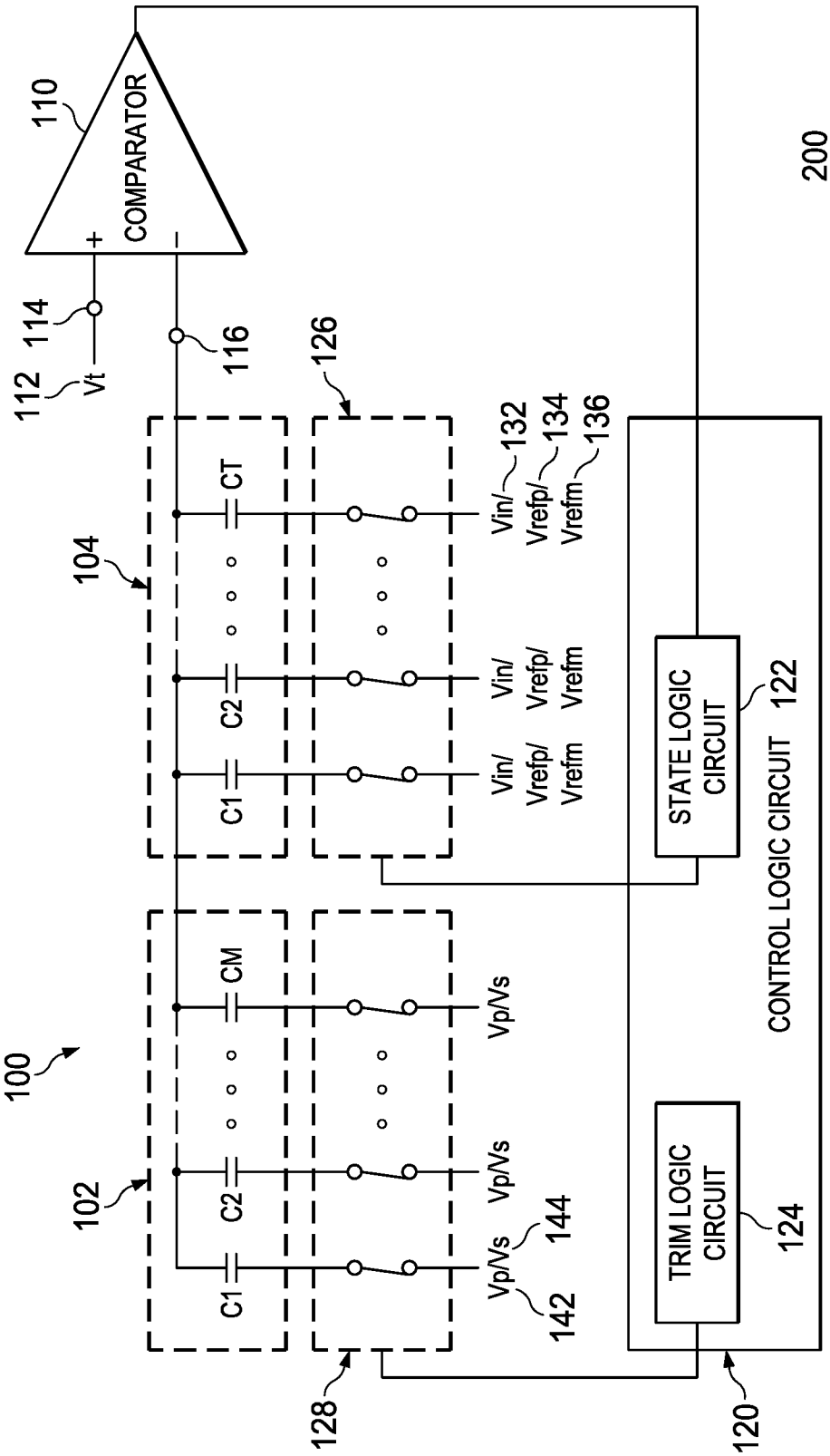
100
102
104
110
COMPARATOR
112
Vt
114
116
126
128
120
C1
C2
CM
CT
Vp/Vs
Vin/
Vrefp/
Vrefm
132
134
136
142
144
STATE LOGIC CIRCUIT
122
TRIM LOGIC CIRCUIT
124
CONTROL LOGIC CIRCUIT

FIG. 1

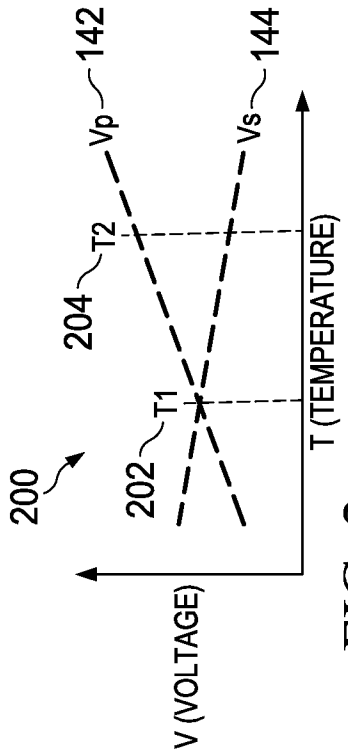
200
202
204
T1
T2
Vp
Vs
142
144
T (TEMPERATURE)
V (VOLTAGE)

FIG. 2

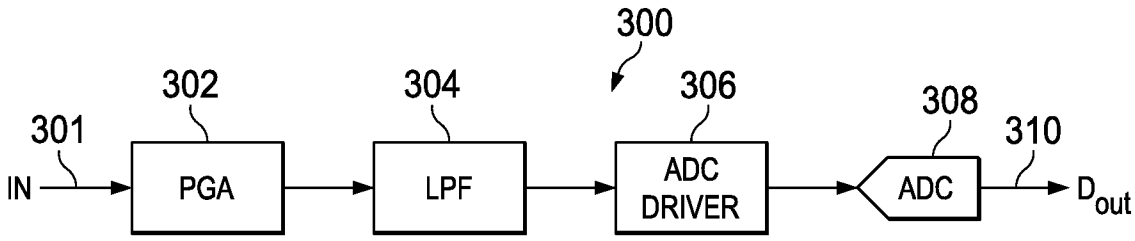

FIG. 3

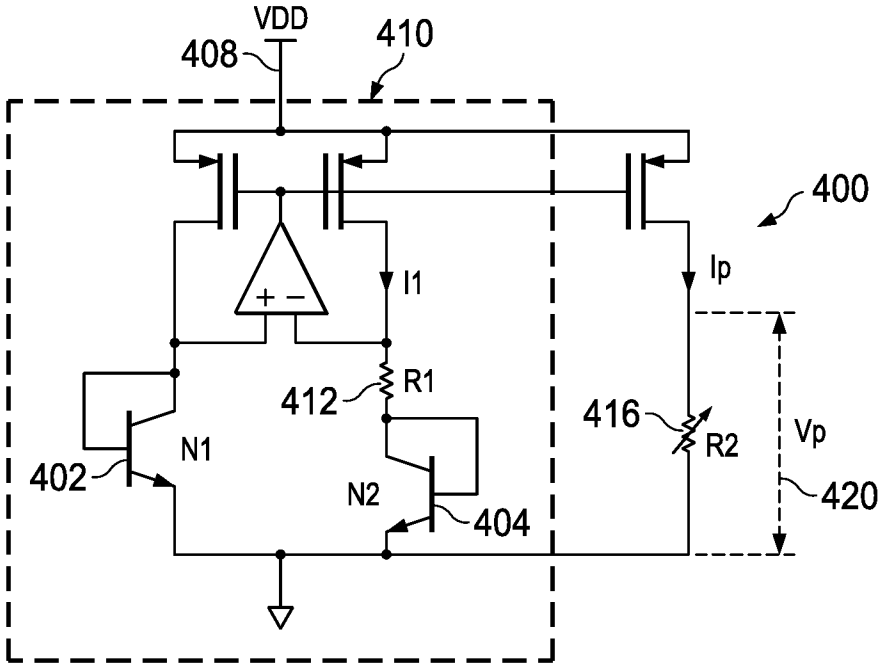

FIG. 4

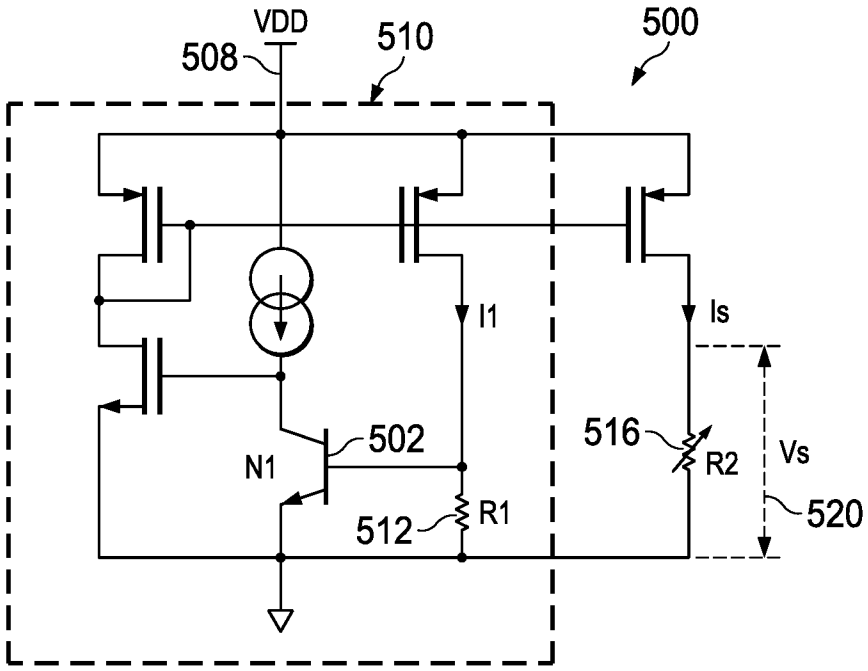

FIG. 5

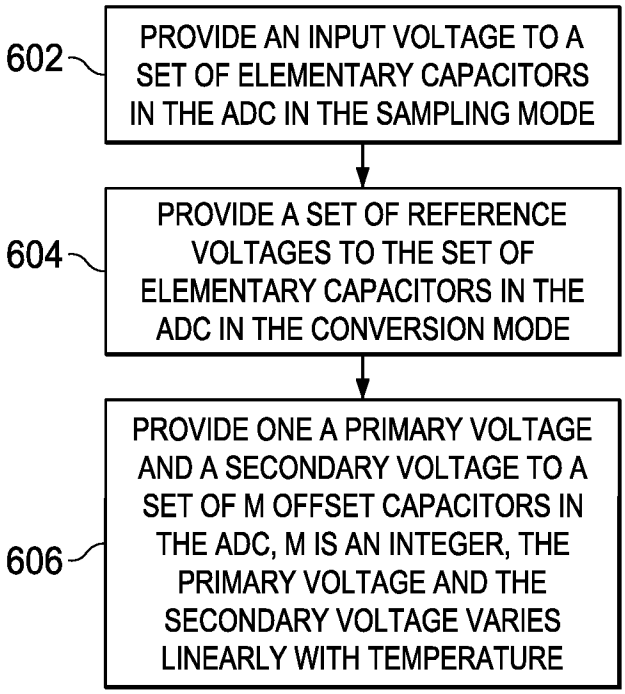
602
PROVIDE AN INPUT VOLTAGE TO A SET OF ELEMENTARY CAPACITORS IN THE ADC IN THE SAMPLING MODE
604
PROVIDE A SET OF REFERENCE VOLTAGES TO THE SET OF ELEMENTARY CAPACITORS IN THE ADC IN THE CONVERSION MODE
606
PROVIDE ONE A PRIMARY VOLTAGE AND A SECONDARY VOLTAGE TO A SET OF M OFFSET CAPACITORS IN THE ADC, M IS AN INTEGER, THE PRIMARY VOLTAGE AND THE SECONDARY VOLTAGE VARIES LINEARLY WITH TEMPERATURE

FIG. 6

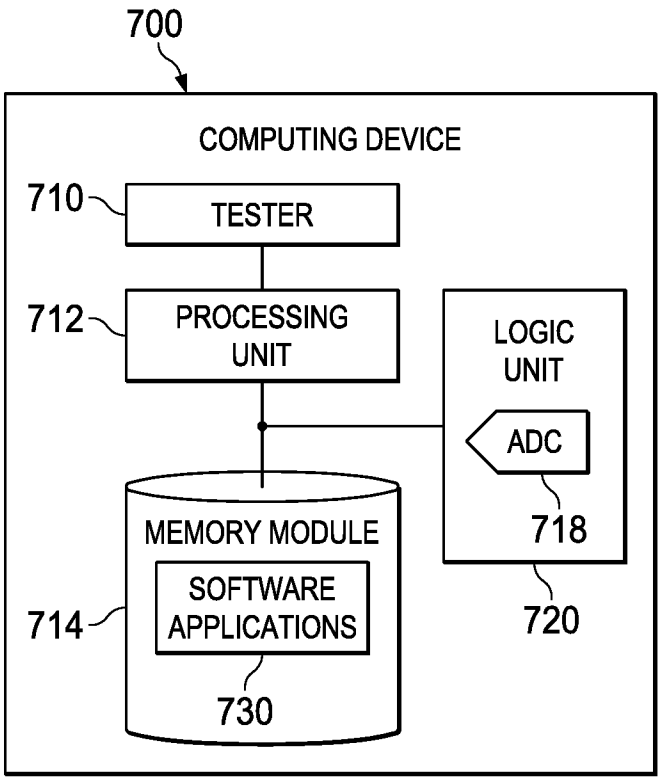
700
COMPUTING DEVICE
710
TESTER
712
PROCESSING UNIT
LOGIC UNIT
ADC
718
720
MEMORY MODULE
SOFTWARE APPLICATIONS
714
730

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/028465

A. CLASSIFICATION OF SUBJECT MATTER

H03M 1/08 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M 1/00, 1/06, 1/08, 1/10, 1/12, H03K 3/00, 3/01, 3/011

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 4799042 A (SGS MICROELETTRONICA SPA) 17.01.1989, col. 1, lines 8-11, col. 3, lines 40-59, col. 4, lines 57-59, fig. 4	1-4, 7, 14-15, 20 5-6, 8-13, 16-19
Y	US 2011/0057718 A1 (TEXAS INSTRUMENTS DEUTSCHLAND GMBH) 10.03.2011, paragraph [0007], fig. 2	1-4, 7, 14-15, 20
Y	US 2007/0035431 A1 (ANALOG DEVICES, INC) 15.02.2007, paragraphs [0018]-[0019], fig. 1	4, 6, 14, 15
Y	US 2012/0194368 A1 (HYNIX SEMICONDUCTOR INC) 02.08.2012, paragraphs [0020]-[0023], fig. 1	20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 July 2016 (22.07.2016)	11 August 2016 (11.08.2016)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer T. Mukhina Telephone No. (495) 531-64-81

Form PCT/ISA/210 (second sheet) (January 2015)