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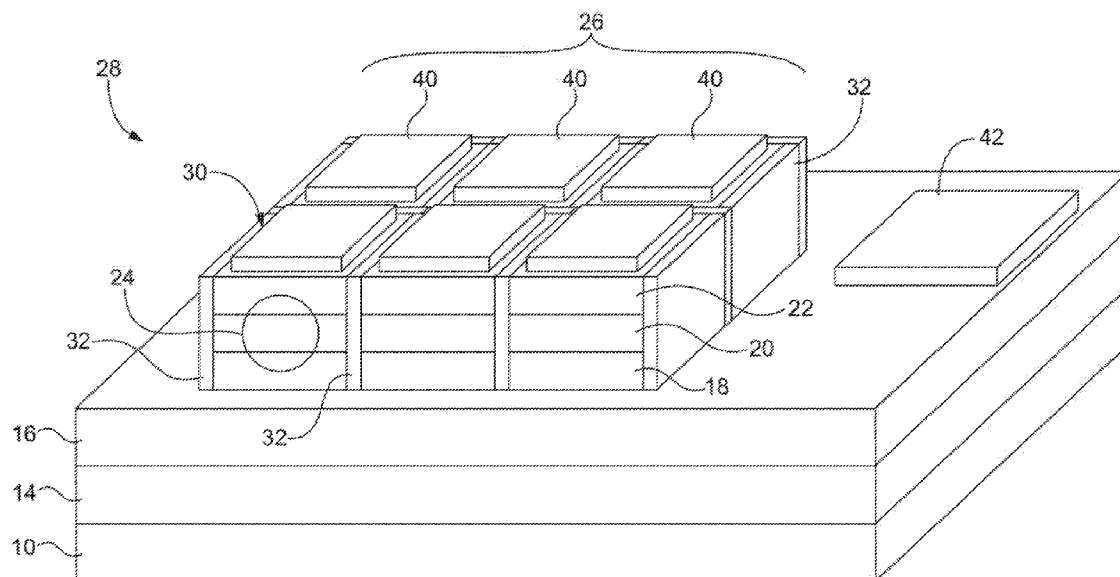


FIG. 2

(57) Abstract: Embodiments can include a light emitting diode (LED) with at least one isolation region formed adjacent the LED. In some embodiments, the isolation region can be formed via ion implantation. Further embodiments can include a plurality of LEDs that may be arranged in an array and/or a plurality of arrays. At least one isolation region can be formed adjacent any one or combination of LEDs and/or arrays. Any one or combination of isolation barriers can be formed without generating gaps in the mesa region of the LED. In some embodiments, the gap-free surface can facilitate generating LED arrays with planar surface configurations.

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GAP-FREE MICRODISPLAY BASED ON III-NITRIDE LED ARRAYS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This utility application is related to and claims the benefit of U.S. Provisional Application Serial No. 62/324,529 titled GAP-FREE MICRODISPLAY BASED ON III-NITRIDE LED ARRAYS filed on April 19, 2016, the entire contents of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention can related to a light emitting diode (LED) with at least one isolation region formed adjacent the LED.

BACKGROUND OF THE INVENTION

[0003] Micro-sized light emitting diode arrays (μ LED array) can have potential for advancement in many technology areas. For example, μ LED arrays may be used in self-emissive microdisplays, single-chip high voltage alternating current LEDs, light sources for optogenetic neuromodulation, etc. Other applications can include use in active driving μ LED array-microdisplays, which may include integrating the μ LED onto complementary metal-oxide-semiconductor (CMOS) substrates.

[0004] μ LED arrays, and in particular III-nitride μ LED arrays, may exhibit superior brightness, contrast, resolution, and reliability when compared to other display systems, such as liquid crystal displays, organic LEDs, digital light processing units, laser beam steering based microdisplay technologies, etc. W. E. Howard and O. F. Prache, *IBM J. RES. & DEV.* 45, 115 (2001); D. Vettese, *Nature Photonics* 4, 752 (2010). Some μ LED array systems may exhibit

longer-lifetimes, be fabricated in a more compact unit, exhibit superior operation-under-harsh-environment, and exhibit superior under-bright daylight characteristics when compared to other microdisplay technologies.

[0005] An LED array generally includes at least one LED formed in or on a substrate. LED arrays configured for displays (or μ LED configured for micro-displays) can include at least one LED forming a pixel. With conventional displays each pixel may be bordered by a physical gap. The physical gaps may be formed by etching the mesa region of the LED array structure. The physical gaps may be used for electrical isolation pixels relative to adjacent pixels. This technique can generate an LED array having a non-planar structure (e.g., physical gaps within a surface of the array structure). J. Day, J. Li, D. Y. C. Lie, C. Bradford, J. Y. Lin and H. X. Jiang, *Appl. Phys. Lett.*, 99, 031116 (2011); H. X. Zhang, D. Massoubre, J. Mckendry, Z. Gong, B. Guilhabert, C. Griffin, E. Gu, P. E. Jessop, J. M. Girkin, and M. D. Dawson, *Optical Express*, 16, 9918, (2008).

[0006] The non-planar configuration of conventional LED arrays can limit the performance and/or the operability of the LED and/or LED array. For example, the etching process can place limits on reducing the pitch dimensions (e.g., distance from a center of one pixel to a center of an adjacent pixel) of μ LED array. For instance, reducing the pitch dimension can allow for an increase in pixels per surface area, which may lead to increased resolution. However, the existence of physical gaps can occupy space in or on the LED array that could otherwise be used to provide more pixels. With some etching techniques, the gaps can be limited in dimension (e.g., the gap may have to have a minimal dimension to be effective). Thus, it may not be possible to reduce the gap's dimension beyond a certain point, which can hinder efforts to reduce pitch dimensions.

[0007] Additionally, each gap can generate a mesa sidewall. For example, a gap may be formed between two LEDs, where one mesa sidewall of the gap is adjacent a first LED and another mesa sidewall of the gap is adjacent a second LED. Light scattering and/or reflecting from the etched mesa sidewalls can reduce the contrast and/or resolution of a display that includes LEDs with isolation gaps. Furthermore, etching processes can cause surface damage to the mesa structure. Surface damage may limit yield output of the LED and/or LED array.

[0008] In addition, the following documents may be helpful in understanding certain embodiments of the invention (with the benefit of the foregoing specification), and they are incorporated by reference herein. This is not an admission that any listed document is prior art for any purpose. If any listed document is contradicted by the body of this specification, the body of this specification shall control. S. C. Binari, H. B. Dietrich, G. Kelner, L. B. Rowland, K. J. Doverspike, and D. K. Wickenden, "H, He and N implant isolation of n-type GaN," *J. Appl. Phys.*, *J. Appl. Phys.*, vol. 78, no. 5, pp. 3008–3011, Sep. 1995; S. J. Pearton, C. B. Vartuli, J. C. Zolper, C. Yuan, and R. A. Stall, "Ion implantation doping and isolation of GaN," *Appl. Phys. Lett.*, vol. 67, no. 10, pp. 1435–1437, Sep. 1995; R. G. Wilson, C. B. Vartuli, C. R. Abernathy, S. J. Pearton, and J. M. Zavada, "Implantation and redistribution of dopants and isolation species in GaN and related compounds," *Solid State Electron.*, vol. 38, no. 7, pp. 1435–1437, Jul. 1995; J. C. Zolper, "Ion implantation in group III-nitride semiconductors: A tool for doping and defect studies," *J. Cryst. Growth*, vol. 178, no. 1/2, pp. 157–167, Jun. 1997; B. Boudart, Y. Guhel, J. C. Pesant, P. Dhamelincourt, and M. A. Poisson, "Raman characterization of Ar⁺ ion-implanted GaN," *J. Raman Spectrosc.*, vol. 33, no. 4, pp. 283–286, Apr. 2002; B. Boudart, Y. Guhel, J. C. Pesant, P. Dhamelincourt, and M. A. Poisson, "Raman characterization of Mg⁺ ion-implanted GaN," *J. Phys., Condens. Matter*, vol. 16, no. 2, pp. s49–s55, Jan. 2004; T. Oishi, N. Miura, M.

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SUMMARY OF THE INVENTION

[0009] Embodiments can include a substrate having at least one LED formed in or on the substrate. The LED can be formed by generating a mesa structure of at least one semiconductor layer that may be doped with at least one dopant to form an emissive layer. The LED can be configured as a μ LED. In some embodiments, the substrate can include a plurality of LEDs. The plurality of LEDs can be arranged in an array. In some embodiments, the array may be configured as a display. At least one LED can be configured to form a pixel.

[0010] At least one LED, pixel, and/or array of LEDs can be isolated (e.g., electrically and/or photonically insulated) from at least one other LED, pixel, and/or array of LEDs. In some embodiments, isolation can be achieved via ion implantation. For example, ion implantation can be performed in or on the substrate and/or in or on at least one layer of the mesa structure. In some embodiments, ion implantation can be used to generate an isolation barrier comprising

implanted ion species. The ion implanted isolation barrier can be used to isolate at least a portion of an LED, a pixel, and/or an array from another portion of an LED, a pixel, and/or an array. In some embodiments, the isolation region can be formed via ion implantation. Further embodiments can include a plurality of LEDs that may be arranged in an array and/or a plurality of arrays. At least one isolation region can be formed adjacent any one or combination of LEDs and/or arrays.

[0011] Some embodiments can include isolation barriers formed by etching. This can include isolation barriers formed as gaps. Some embodiments can include a plurality of isolation barriers formed by a combination of etching and ion implantation. Isolation barriers formed by ion implantation can be used to form isolation barriers within a portion of the mesa structure so as to generate a planar region. Portions of the mesa structure without any gaps can be referred to as planar regions. Portions of the mesa structure with gaps can be referred to as non-planar regions.

[0012] Some embodiments can include generating an LED array. An LED array can include a plurality of LEDs and/or pixels. Any one or combination of LEDs, pixels, and/or LED arrays can be isolated from any other or combination of other LEDs, pixels, and/or LED arrays via an isolation barrier. Some embodiments of the LED array can include a mesa structure with at least one planar region. In some embodiments, the entire mesa structure can be configured as a planar region.

[0013] In some embodiments, the LED array may be used to generate a display. The display may be configured as a microdisplay.

[0014] In one exemplary embodiment, a LED can include a substrate having a mesa structure. The mesa structure can include at least one layer formed in or on a portion of the substrate. At

least one LED can be formed in or on at least a portion of the mesa structure. At least one isolation barrier can be formed in or on at least a portion of the substrate and/or the mesa structure. In some embodiments at least a portion of the at least one LED and at least a portion of the at least one isolation barrier can form a planar region.

[0015] In some embodiments, the at least one isolation barrier can include a volume of space within the substrate and/or the mesa structure having a concentration of ions configured to at least one of electrically isolate and photonically isolate at least a portion of the at least one LED. In some embodiments, the at least one LED can be configured as a pixel. Some embodiments can include a plurality of LEDs. In some embodiments, the plurality of LEDs can form at least one LED array.

[0016] Some embodiments can include a p-contact connected to the at least one LED. Some embodiments can include an n-contact connected to at least a portion of the at least one layer. Some embodiments can include a plurality of LEDs. An n-contact can be configured as a common contact shared by each LED. Some embodiments can include an integrated circuit bonded to the LED display via the p-contact and the n-contact.

[0017] In some embodiments, the at least one isolation barrier can include at least one deep level trap. In some embodiments, the at least one layer can include a quantum well. In some embodiments, the quantum well can include a quantum heterostructure.

[0018] In some embodiments, the at least one isolation barrier can include at least one ion species selected from the group consisting of H⁺, He⁺, N⁺, F⁺, Mg⁺, Ar⁺, Zn⁺, O⁺, Ti⁺, Fe⁺, Cr⁺, Mn⁺, and Co⁺.

[0019] In some embodiments, the at least one isolation barrier can be configured to at least one of electrically isolate and photonically isolate one LED and/or one LED array from another LED and/or LED array.

[0020] In another exemplary embodiment, a light emitting diode (LED) display can include a pixel unit having at least one LED. The LED may include a substrate. The LED may include a buffer layer. The buffer layer may be formed in or on at least a portion of the substrate. The LED may include a first n-type layer. The first n-type layer may be formed in or on at least a portion of the buffer layer. The LED may include a second n-type layer. The second n-type layer may be formed in or on at least a portion of the first n-type layer. The LED may include an emissive layer. The emissive layer may be formed in or on at least a portion of the second n-type layer. The LED may include a p-type layer. The p-type layer may be formed in or on at least a portion of the emissive layer. Some embodiments can include at least one region bordering at least one of the LED and the pixel unit. In some embodiments, the at least one region can be implanted with at least one ion species via ion implantation. In some embodiments, the at least one ion species can be caused to enter at least one of the p-type layer, the emissive layer, and the n-type layer. In some embodiments, the at least one ion species can be configured to serve an isolation function of the at least one region.

[0021] In another exemplary embodiment, a method for creating a light emitting diode (LED) display can include generating a mesa structure on a substrate. The mesa structure may include at least one layer formed in or on at least a portion of the substrate. The method can further include forming at least one LED in or on at least a portion of the substrate and/or mesa structure. The method can further include generating at least one isolation barrier in or on at

least a portion of the substrate and/or the mesa structure. In some embodiments, at least a portion of the at least one LED and the at least one isolation barrier can form a planar region.

[0022] In some embodiments, generating the at least one isolation barrier can further include forming a concentration of ions within a volume of space of the substrate and/or the mesa structure configured to at least one of electrically isolate and photonically isolate at least a portion of the at least one LED. In some embodiments, generating the at least one isolation barrier can further include generating at least one deep level trap. In some embodiments, generating the mesa structure can further include generating at least one quantum well within the at least one layer.

[0023] Some embodiments can further include forming a plurality of LEDs. Some embodiments can further include forming the at least one isolation barrier to isolate at least one LED from another LED.

[0024] Further features, aspects, objects, advantages, and possible applications of the present invention will become apparent from a study of the exemplary embodiments and examples described below, in combination with the Figures, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The above and other objects, aspects, features, advantages and possible applications of the present invention will be more apparent from the following more particular description thereof, presented in conjunction with the following drawings, in which:

[0026] FIG. 1 shows a schematic of an embodiment of an LED structure that may be used to form an embodiment of a pixel.

[0027] FIG. 2 shows an embodiment of an LED array structure that may be used to form an embodiment of a display.

[0028] FIG. 3 shows an embodiment of a single LED formed in or on a substrate.

[0029] FIG. 4 shows an embodiment of a display having two arrays adjacent each other.

[0030] FIG. 5 shows an embodiment of a display with isolation barriers formed as gaps.

[0031] FIG. 6 shows an a schematic of an exemplary flip-chip bonding set up that may be used to form a microdisplay with an embodiment of the LED array.

[0032] FIG. 7 shows simulation data of leakage current vs. numbers of OFF pixels in the same row to the ON pixel as a function of ion implantation dose.

[0033] FIG. 8 shows simulation data of pixel resolution vs. the isolation barrier width for different screen sizes.

[0034] FIG. 9 shows simulation data of 2-dimension current density distribution for an implantation dose of $1\text{E}17$ ions/ cm^2 and implantation energy of 200 Kev in the isolation barriers.

[0035] FIG. 10 shows simulation data of 2-dimension current density distribution for an implantation dose of $2\text{E}17$ ions/ cm^2 and implantation energy of 200 Kev in the isolation barriers.

DETAILED DESCRIPTION OF THE INVENTION

[0036] The following description is of an embodiment presently contemplated for carrying out the present invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles and features of the present invention. The scope of the present invention should be determined with reference to the claims.

[0037] Referring to FIG. 1, embodiments can include a substrate 10. The substrate 10 can be a semiconductor material. This can include silicon, silicon dioxide, aluminum oxide, sapphire,

germanium, gallium, semiconductor compound etc. In some embodiments, the substrate 10 can include a transparent crystalline substrate. This can include a (1000) sapphire substrate, for example. The substrate 10 can be used as a wafer. For example, the substrate 10 can include an upper surface 10a and a lower surface 10b. At least one surface 10a, 10b can include a mesa structure. The mesa structure can include at least one layer. A layer can be a portion of the substrate that includes other material (e.g., dopants) to change the electrical properties of the substrate 10. A layer can be a material that is grown, coated, or is some other formation that is the result of transferring the material into or onto the substrate 10. For example the layer can be a growth layer, a deposition layer, a coating layer, etc.

[0038] For example, the mesa structure can include a buffer layer 14. The buffer layer 14 may be formed in or on a surface 10a, 10b of the substrate 10. The buffer layer 14 may be formed by doping at least a portion of the surface 10a, 10b. Dopants can include Group III and/or Group V elements. For example, a buffer layer 14 can be doped to form an III-V compound semiconductor layer. This may include an III-nitride layer. For example, the buffer layer 14 may include dopants such as gallium nitride (GaN), aluminum nitride (AlN), boron nitride (BN), indium phosphide (InP), etc. The buffer layer 14 can include a doping profile that is defined by the dopant concentration. At least a portion of the buffer layer 14 can have a doping profile that is constant throughout that portion of the buffer layer 14. At least a portion of the buffer layer 14 can have a doping profile that is variable throughout that portion of the buffer layer 14.

[0039] The mesa structure can include a first n-type layer 16. The first n-type layer 16 may be formed in or on a portion of the buffer layer 14. The first n-type layer 16 may be formed by doping a portion of the buffer layer 14 with dopants to modify its conductivity. The n-type dopants can include silicon, carbon, etc. These may have a concentration of $1\text{E}18\text{ stoms-cm}^{-3}$,

for example. At least a portion of the first n-type layer 16 can have a doping profile that is constant throughout that portion of the first n-type layer 16. At least a portion of the first n-type layer 16 can have a doping profile that is variable throughout that portion of the first n-type layer 16.

[0040] The mesa structure can include a second n-type layer 18. The second n-type layer 18 may be formed in or on a portion of the first n-type layer 16. The second n-type layer 18 may be formed by doping a portion of the first n-type layer 16 with dopants to modify its conductivity. The n-type dopants can include Si, C, etc. Doping concentrations may be within a range from $1\text{E}17$ to $1\text{E}21$ atoms- cm^{-3} . In some embodiments, the first n-type layer 16 can have the same configuration as the second n-type layer 18. Some portions of the device can be etched for fabrication purposes. When such etching is performed, the second n-type layer 18 can represent the n-type portions that are not etched. At least a portion of the second n-type layer 18 can have a doping profile that is constant throughout that portion of the second n-type layer 18. At least a portion of the second n-type layer 18 can have a doping profile that is variable throughout that portion of the second n-type layer 18.

[0041] The mesa structure can include an emissive layer 20. The emissive layer 20 may be formed in or on a portion of the second n-type layer 18. The emissive layer 20 can be configured to emit electromagnetic radiation in response to an electric current. The emissive layer 20 may be formed by epitaxial growth, liquid phase epitaxy, vapor phase epitaxy, etc. Metal-organic chemical vapor deposition may be used with embodiments having III-V compound semiconductor material (e.g., III-nitrides) to avail the superior crystalline quality that may be exhibited by III-nitride semiconductor materials. With some embodiments, metal-organic chemical vapor deposition may be used to better control formation of a doping profile, as

compared to other deposition techniques. The emissive layer 20 may be configured to include at least one quantum well. The quantum well may be used to cause charge carriers to be placed into quantum confinement. A quantum well can be configured to occur at a heterojunction interface formed by dissimilar crystalline semiconductor material. This may be done to form a quantum heterostructure. Heterostructures used to generate a quantum heterostructure may include, but are not limited to, InGaN/GaN, In_xGa_{1-x}N/In_{x'}Ga_{1-x'}N (x not equal to x'), GaN/AlGa_xN, Al_xGa_{1-x}N/Al_{x'}Ga_{1-x'}N, In_xAl_yGa_{1-x-y}N/In_{x'}Al_{y'}Ga_{1-x'-y'}N (x not equal to x', y not equal to y'), GaN/In_xAl_yGa_{1-x-y}N, etc.

[0042] The mesa structure can include a p-type layer 22. The p-type layer 22 may be formed in or on a portion of the emissive layer 20. The p-type layer 22 may be formed by doping a portion of the emissive layer 20 with dopants to modify its conductivity. The p-type dopants can include Mg, Be, etc. Doping concentrations may be within a range from 1E17 to 1E21 cm⁻³. At least a portion of the p-type layer 22 can have a doping profile that is constant throughout that portion of the p-type layer 22. At least a portion of the p-type layer 22 can have a doping profile that is variable throughout that portion of the p-type layer 22.

[0043] Any one or combination of layers 14, 16, 18, 20, 22 can be formed as a single layer or a multi-layer. Any one or combination of layers 14, 16, 18, 20, 22 may include dimensions, dopant types, dopant concentrations, doping profiles, etc. that differ from any other layer 14, 16, 18, 20, 22 or combination of layers 14, 16, 18, 20, 22. Any portion of a layer 14, 16, 18, 20, 22 may include dimensions, dopant types, dopant concentrations, doping profiles, etc. that differ from any other portion of a layer 14, 16, 18, 20, 22.

[0044] Referring to FIG. 2, at least one light emitting diode (LED) 24 can be formed in or on at least a portion of the substrate 10 and/or mesa structure. In some embodiments, the second n-

type layer 18, emissive layer 20, and the p-type layer 22 can be used to form at least one LED 24. The LED 24 can be a micro-LED (μ LED). In some embodiments, a plurality of LEDs 24 can be formed in or on at least a portion of the substrate 10 and/or mesa structure. In some embodiments, the plurality of LEDs 24 can be arranged in an array 26. Any one or combination of LEDs 24 and/or arrays 26 can be defined and/or patterned via lithography techniques, for example.

[0045] The array 26 may be configured as a display 28. This can include a micro-display 28. At least one LED 24 can be configured to form a pixel 30 or pixel unit of the display 28. For example, the LED 24 can be configured as a controllable element of a display 28. For instance, the LED 24 can be controlled by manipulating emission amplitude, emission intensity, emission wavelength, pulse cycle, etc. of the LED 24. In some embodiments, a pixel 30 can include a single LED 24 and/or a plurality (e.g., cluster) of LEDs 24. Any one LED 24 and/or pixel 30 may be isolated. This can include being isolated by an isolation barrier 32.

[0046] An array 26 can include at least one LED 24 and/or pixel 30. Any one or combination of the LEDs 24 and/or pixels 30 may be adjacent any other one or combination of LEDs 24 and/or pixels 30. The LEDs 24 and/or pixels 30 can be orthogonally arrange or arranged in any other geometric configuration. A display 28 can include at least one array 26. Any one or combination of the arrays 26 may be adjacent any other one or combination of arrays 26. The arrays 26 can be orthogonally arrange or arranged in any other geometric configuration. The number and/or configuration of LEDs 24 and/or pixels 30 in one array 26 can be the same as or different from the number and/or configuration of LEDs 24 and/or pixels 30 in another array 26. The LED 24, pixel 30, and/or array 26 can include a square cross-sectional shape. Other cross sectional shapes can be used. This can include circular, oblong, rectangular, triangular, etc.

[0047] At least one LED 24, pixel 30, and/or array 26 can be isolated from at least one other LED 24, pixel 30, and/or array 26. This can include an LED 24, pixel 30, and/or array 26 being isolated from an adjacent LED 24, pixel 30, and/or array 26. In some embodiments, each LED 24, pixel 30, and/or array 26 can be isolated from each other LED 24, pixel 30, and/or array 26. In some embodiments, only a portion of an LED 24, a pixel 30, and/or an array 26 may be isolated from a portion of another LED 24, pixel 30, and/or array 26. Isolation can include being electrically and/or photonically insulated.

[0048] As shown in FIG. 2, an embodiment can include a substrate 10 and/or mesa structure having an array 26 formed in or on at least a portion thereof. The array 26 can include a plurality of LEDs 24. The plurality of LEDs 24 can be arranged in a grid formation. For example, a two-row by three-column LED 24 grid formation can be generated. This can include a first row having three LEDs 24 and a second row having three LEDs 24. More or less rows, columns, and LEDs 24 can be used.

[0049] Referring to FIGS. 3-4, some embodiments can include each LED 24 being formed into a square cross sectional shape. For example, each LED 24 can include a first LED side 24a, a LED second side 24b, a LED third side 24c, and a LED fourth side 24d. The array 26 may be formed to have a square cross sectional shape. For example, the array 26 can include a first array side 26a, a second array side 26b, a third array side 26c, and a fourth array side 26d. Any side of the LED 24 and/or array 26 can include an isolation barrier 32. The isolation barrier 32 can be configured to isolate at least a portion of the LED 24 and/or array 26 from a side 24a, 24b, 24c, 24d, 26a, 26b, 26c, 26d of another LED 24 and/or array 26. This can include isolating at least a portion of the LED 24 and/or array 26 from an adjacent side 24a, 24b, 24c, 24d, 26a, 26b, 26c, 26d of another LED 24 and/or array 26. An isolation barrier 32 can be formed on any one or

combination of sides 24a, 24b, 24c, 24d, 26a, 26b, 26c, 26d. In some embodiments, an isolation barrier 32 can be formed on each side 24a, 24b, 24c, 24d, 26a, 26b, 26c, 26d of each LED 24 and/or each array 26. An isolation barrier 32 formed on each side 24a, 24b, 24c, 24d, 26a, 26b, 26c, 26d of an LED 24 and/or array 26 can be considered to “surround” the LED 24 and/or array 26.

[0050] In some embodiments, at least one isolation barrier 32 can be formed by ion implantation. In some embodiments, at least one isolation barrier 32 can be formed by etching. In some embodiments, a combination of ion implantation and etching can be used to form an isolation barrier 32. An isolation barrier 32 can be formed in any portion of the substrate 10 and/or mesa structure. For example, an isolation barrier 32 can be formed so as to extend from any layer 14, 16, 18, 20, 22 of the mesa structure or intermediate portion of a layer 14, 16, 18, 20, 22 of the mesa structure to any other layer 14, 16, 18, 20, 22 of the mesa structure and/or any intermediate portion of a layer 14, 16, 18, 20, 22 of the mesa structure. For instance, an isolation barrier 32 can be formed to extend from a top surface of the p-type layer 22 to a bottom surface of the second n-type layer 18. As another example, an isolation barrier 32 can be formed to extend from a top surface of the p-type layer 22 to an intermediate portion of the emissive layer 20. As another example, an isolation barrier 32 can be formed to extend from a bottom surface of the second n-type layer 18 to an intermediate portion of the emissive layer 20.

[0051] Referring to FIG. 5, forming isolation barriers 32 by etching can include dry etching, wet etching, plasma etching, etc. Etching may be used to generate at least one gap 34 in the mesa structure. The gap 34 can act as an isolation barrier 32. The isolation barrier 32 formed by a gap 34 can be defined by a volume of space (length 32a, width 32b, and depth 32c) of the gap 34 formed within the substrate 10 and/or mesa structure.

[0052] Referring back to FIG. 3, forming isolation barriers 32 by ion implantation can be achieved by implantation of at least one ion species into a portion of the mesa structure. The species may include, but are not limited to, H⁺, He⁺, N⁺, F⁺, Mg⁺, Ar⁺, Zn⁺, O⁺, Ti⁺, Fe⁺, Cr⁺, Mn⁺, and Co⁺. The level of electrical and/or photonic insulation exhibited by the isolation barrier 32 may be dependent upon the type, amount, and or concentration of species used. An isolation barrier 32 may be defined by a volume of space (length 32a, width 32b, and depth 32c) of the substrate 10 and/or mesa structure that has a certain concentration of ion species implanted therein.

[0053] An ion implantation process can include an ion source to generate at least one ion. An accelerator may be used to accelerate the ions to a high energy. The ions can be caused to impinge on at portion of the substrate 10 and/or mesa structure and be implanted therein. Generally, the longer the ions are accelerated toward the mesa structure, the more ions per unit volume are caused to occupy the substrate 10 and/or mesa structure. The acceleration energy, the ion species, and the composition of the structure 10 and/or mesa structure can determine the depth at which the ions can be implanted and the concentration of ions within a given volume of space. Using these factors, an ion implantation profile can be generated. The ion implantation profile can be defined by the amount, depth, concentration, etc. of the ions that make up the isolation barrier 32. At least a portion of the isolation barrier 32 can have an ion implantation profile that is constant throughout that portion of the isolation barrier 32. At least a portion of the isolation barrier 32 can have an ion implantation profile that is variable throughout that portion of the isolation barrier 32.

[0054] As noted above, the isolation barrier 32 can be used to isolate at least a portion of an LED 24, a pixel 30, and/or an array 26. Isolation can include electrically and/or photonicall

insulating that portion of the LED 24, the pixel 30, and/or the array 26. Electrically insulating can include providing an isolation barrier 32 with a predetermined level of electrical resistance. Photonically insulating can include providing an isolation barrier 32 with a predetermined level of opacity. This can include a predetermined level of opacity for at least one wavelength of electromagnetic radiation.

[0055] In some embodiments, the electrical resistance provided by an isolation barrier 32 formed by ion implantation can be sufficient to isolate an LED 24, a pixel 30, and/or an array 26 from another LED 24, pixel 30, and/or array 26. This can include isolating an LED 24, pixel 30, and/or array 26 from an adjacent LED 24, pixel 30, and/or array 26. Certain ion species and/or concentrations of ion species can generate electrical resistance within a portion of the substrate 10 and/or any of the layers 14, 16, 18, 20, 22 of the mesa structure. This may be used to modify and/or control the electrical properties of the semiconductor material in the substrate 10 and/or any of the layers 14, 16, 18, 20, 22 of the mesa structure. For example, an isolation barrier 32 within a mesa structure can be configured to have an electrical resistance (measured in sheet resistance) within a range from $10^6 \Omega/\square$ to $10^{16} \Omega/\square$. Other electrical resistance levels may be created, as demonstrated in FIGS. 7-10 which are discussed in detail below.

[0056] In some embodiments, the opacity provided by the isolation barrier 32 formed by ion implantation can be sufficient to isolate an LED 24, pixel 30, and/or array 26 from another LED 24, pixel 30, and/or array 26. This can include isolating an LED 24, pixel 30, and/or array 26 from an adjacent LED 24, pixel 30, and/or array 26. For example, ion implantation may cause deep level defects and/or amorphization of the crystalline structure. This may further generate at least one deep level trap. The deep level trap can be formed within the isolation barrier 32. Deep level traps may be used to modify and/or control the optical properties of the

semiconductor material in the substrate 10 and/or any of the layers 14, 16, 18, 20, 22 of the mesa structure. For example, electromagnetic radiation with photon energy smaller than the semiconductor bandgap of the deep level trap may be absorbed by the semiconductor material. Thus, a deep level trap can be formed in an isolation barrier 32 and be configured to absorb electromagnetic radiation of a predetermined wavelength or predetermined wavelengths. For example, a deep level trap of an isolation barrier 32 can be used to absorb electromagnetic radiation generated from at least one of an LED 24, a pixel 30, and/or an array 26. This can include absorbing electromagnetic radiation generated from an LED 24, a pixel 30, and/or an array 26 that the deep level trap is adjacent to.

[0057] In some embodiments, an isolation barrier 32 with deep level traps can be configured to absorb electromagnetic radiation generated from an LED 24, a pixel 30, and/or an array 26 the isolation barrier 32 is surrounding. For example, the deep level trap can be configured such that the semiconductor bandgap is greater than the photon energy of the electromagnetic radiation that can be emitted from the LED 24, the pixel 30, and/or the array 26 it is adjacent to and/or the LED 24, the pixel 30, and/or the array 26 the isolation barrier 32 is surrounding. Thus, the isolation barrier 32 formed by ion implantation can be configured to function as an opaque wall that prevents light propagation from one LED 24, pixel 30, and/or array 26 to another LED 24, pixel 30, and/or array 26. This may be done to prevent cross talk behavior that may otherwise exist between one LED 24, pixel 30, and/or array 26 and another LED 24, pixel 30, and/or array 26.

[0058] In at least one embodiment, the depth 32c of an isolation barrier 32 can range from 0.01 μ m to 19 μ m. The width 32b of an isolation barrier 32 can be at least 0.1 μ m, for example. The length 32a may depend on the size of the LED 24, pixel 30, and/or array 26 used for a

particular application. An isolation barrier 32 width 32b of approximately $0.1\mu\text{m}$ used to isolate at least one of an LED 24, a pixel 30, and/or an array 26 of a display 28 may facilitate diffraction-limited resolution (e.g., the display device 28 may be able to produce images with angular resolution commensurate with that of the display device's 28 theoretical limit) for the display 28. It should be noted that $0.1\text{ }\mu\text{m}$ is an exemplary value. In general, the pitch of an LED 24 matrix can be determined by the sum of the pixel 30 size and the distance between each pixel 30. Smaller the distance between pixels 30 is generally results in higher that display quality. This may be due to a reduction of the non-emission area in the display panel.

[0059] Any isolation barrier 32 and/or portion of an isolation barrier 32 can be the same as or different from any other isolation barrier 32 and/or portion of an isolation barrier 32. For example, an isolation barrier 32, a portion of an isolation barrier 32, and/or a combination of isolation barriers 32 may be formed by etching and/or by ion implantation. For instance, it may be beneficial for a first portion of the LED 24, pixel 30 and/or LED array 26 to include isolation barriers 32 formed by etching, while a second portion of the LED 24, pixel 30, and/or LED array 26 includes isolation barriers 32 formed by ion implantation. As another example, a portion of an isolation barrier 32 along one side of an LED 24 and/or array 26 can be formed by ion implantation while another portion of the same or different side can be formed by etching. As another example, longitudinal arrange isolation barriers 32 can be etched while latitudinal isolation barriers 32 can be formed by ion implantation. As another example, ions used for ion implantation in one isolation barrier 32 and/or portion of an isolation barrier 32 can be the same as or different from ions used for ion implantation in another isolation barrier 32 and/or portion of the isolation barrier 32. As another example, etching techniques used to form gaps 34 that may be used any isolation barrier 32 and/or portion of an isolation barrier 32 can be the same as

or different from etching techniques used in any other isolation barrier 32 and/or portion of the isolation barrier 32. Any parameter (e.g., length 32a, width 32b, depth 32c, electrical resistance, opacity, ion concentration, etc.) of any isolation barrier 32 and/or portion of an isolation barrier 32 can be the same as or different from another parameter in any other isolation barrier 32 and/or portion of the isolation barrier 32.

[0060] The inventive ion implantation-based isolation approach can eliminate the need for dry etching into the semiconductor. Generally, dry etching requires a passivation process to fix or deactivate the surface defects and deep energy levels induced by the dry etching process. Thus, the inventive ion implantation-based isolation approach can eliminate the need for passivation processes.

[0061] In some implementations, the inventive method can be used for ion etching into the active region of an LED 24 so as to introduce dislocation defects and deep energy levels in the quantum wells of the LED active region. This may lead to the deactivation of the LED 24.

[0062] As noted above, an isolation barrier 32 can be generated as gaps 34 and/or as ion implantation zone. Portions of the substrate 10 and/or mesa structure without any gaps 34 can be referred to as planar regions 36. (See FIG. 4). Portions of the substrate 10 and/or mesa structure with gaps 34 can be referred to as non-planar regions 38. (See FIG. 5). Some embodiments can include a substrate 10 and/or mesa structure with at least one planar region 36 and/or at least one non-planar region 38. In some embodiments, the entire structure 10 and/or mesa structure can be configured as a planar region 36 and/or a non-planar region 38. For example, a substrate 10 can include at least one array 26 formed in or on a portion thereof. The array 26 can include a plurality of LEDs 24 and/or pixels 30 arranged in a grid formation. Each LED 24, pixel 30, and/or array 26 can be isolated from each other LED 24, pixel 30, and/or array 26 via isolation

barriers 32. Each isolation barrier 32 can be formed by ion implantation. The entire top surface of the array 26 can be a planar region 36 (e.g., free from gaps). Some embodiments can include a plurality of arrays 26 arranged in a grid formation. (See FIG. 4). An isolation barrier 32 can be formed between adjacent arrays 26. The entire top surface of the array 26 grid formation can be a planar region 36.

[0063] In some embodiments, contrast and/or resolution of a display 28 can be improved by generating a display 28 having at least one LED 24, pixel 30, and or array 26 with isolation barriers 32 that form at least one planar region 36. Contrast and/or resolution may be improved (as compared to a display 28 with a non-planar region 38) due to the absences of gaps 34 in the planar region 36. The absence of gaps 34 can improve contrast and/or resolution because etching used to form the gaps 34 can cause surface damage to a surface of the substrate 10 and/or mesa structure. For example, etching can cause surface roughness, surface contamination, surface stoichiometry changes, etc. Furthermore, gaps 34 can cause light scattering and/or reflection of light from the mesa sidewalls of the gaps 34. The absence of gaps 34 can also facilitate generating an LED 24, pixel 30, and/or array 26 with high yield. For example, the ion implantation-based isolation process may eliminate the procedure of dry etching. Dry etching typically forms air gaps in the LED array 26 during fabrication. Air gaps can lead to “dead” LEDs 24 in the array 26 due to short current through the mesa side walls of the LED pixels 30 (even after passivation). The inventive method, with the elimination of dry etching, can potentially avoid the dead LED pixels in the matrix.

[0064] Referring back to FIG. 2, a display 28 can include a substrate 10. The substrate 10 can include a mesa structure formed in or on a portion thereof. At least a portion of the mesa structure can include at least one LED 24. At least one LED 24 can be configured as a pixel 30.

At least one LED 24 and/or pixel 30 can be configured as an array 26. Each LED 24, pixel 30 and or array 26 can be defined and/or patterned via lithography. This can include forming an array 26 with a plurality of LEDs 24 and/or pixels 30 in a grid formation. Each LED 24, pixel 30, and or array 26 can be isolated from another LED 24, pixel 30, and/or array 26 by at least one isolation barrier 32. A p-type layer 22 of at least one LED 24 and/or pixel 30 can include at least one p-contact 40. A portion of the first n-type layer 16 can include at least one n-contact 42. Any of the p-contacts 40 and/or n-contacts 42 can be an electrical junction. This can include a rectifying and/or a non-rectifying contact junction. Electrical junctions can include, but are not limited to, low resistance ohmic contacts, tunnel contacts, other metal-semiconductor junction contacts, etc. The p-contact 40 and n-contact 42 configurations can allow for control of the emission and/or operation of the LED 24. This may facilitate the LED 24 acting as a pixel 30 in the array 26.

[0065] Referring to FIG. 6, some embodiments of the display 28 can be configured as a microdisplay. With a microdisplay 28, practical top surface dimensions of a pixel 30 can be $1\mu\text{m}$ by $1\mu\text{m}$. This may facilitate generating a display 28 that exhibits diffraction-limited resolution. The pitch distance 44 (e.g., distance from a center of one pixel 30 to a center of an adjacent pixel 30) can be $1.1\mu\text{m}$. Generally, the overall resolution and/or the surface area of the display 28 can be determined by pixel dimensions and pitch distances 44. Some embodiments of a display 28 can provide a $4\text{mm}\times 3\text{mm}$ screen panel having a retina resolution of 2560×1920 .

[0066] In some embodiments, at least one LED 24 and/or pixel 30 may be configured to share a common n-contact 42 (e.g., a common cathode). Each LED 24 and/or pixel 30 may be in connection with an individually controllable p-contact 40 (e.g., an individual anode). This may be achieved by bonding each individual p-contact 40 and the common n-contact 42 of the array

26 to complementary contacts 46 of a complementary metal-oxide-semiconductor (“CMOS”) backplane circuitry 48. FIG. 6 s shows an a schematic of a flip-chip bonding setup that may be used to bond an array 26 to a CMOS backplane 48. In some embodiments, the array 26 may be integrated into an integrated circuit (IC). The IC may be a silicon-CMOS IC, for example. In some embodiments, the array 26 may be integrated onto the Si-CMOS IC backplane of an active matrix driver (not shown). The active matrix driver may be configured to serve as an addressing scheme (e.g., activating and de-activating individual LEDs 24 and/or pixels 30) for the display 28.

[0067] Integration of the array 26 into an IC may be achieved via flip-chip bonding. This can include using eutectic bonding metal pads or bonding bumps between corresponding contacts 40, 42, 46 of the array 26 and the IC. Examples of bonding metal that may be used can include Sn, Sn alloys, Au, Ag, In, Ag, Au, In, etc. In some embodiments, several millions of signal connections between the array 26 and the active matrix driver may be established by the technique of flip-chip bonding.

[0068] Referring to FIG. 7, the leakage current of LEDs 24, pixels 30, and/or arrays 26 under forward bias can be simulated. Since the ion implantation of isolation barriers 32 is not uniformly distributed across the barrier and take the shape of the Gaussian distribution, the current can leak out from one LED 24 and/or pixel 30 to the neighboring ones through the isolation barriers 32 under forward bias, which may affect the performance of all the pixels 30 in the same array 26. The isolation of the leakage current can depend on three key parameters, including ion dose, ion energy, and/or the isolation barrier width 32b. In semiconductor materials, ion dose may be within a range from $1\text{E}11\text{ cm}^{-2}$ to $1\text{E}18\text{ cm}^{-2}$ and the ion energy may be within a range from 5 KeV to tens of MeV. The width 32b of an isolation barrier 32 can be at

least $0.1\mu\text{m}$. If the value of one of the three parameters increases while keeping the values of the other two parameters constants, the leakage current can decrease significantly and also the number of the affected pixels by the leakage current may be reduced. Another important parameter to control for the isolation of the leakage current can be the isolation barrier depth 32c. If a depth 32c of an isolation barrier 32 increases, high ion energy and/or high ion dose may be needed to isolate the leakage current at a certain depth from one LED 24 and/or pixel 30 to other LEDs 24 and/or pixels 30 since ion implantation offers a precise control of dose and depth profile.

[0069] For example, five pixels 30 can be simulated with a width 32b of an isolation barrier 32 of $0.1\mu\text{m}$. The depth 32c of the isolation barrier can be $1\mu\text{m}$. Also, the ion energy of a Nitrogen implants for example can be fixed at 200 KeV. The leakage current decreases by increasing the ion dose from $1\text{E}17$ to $2\text{E}17$ ions/ cm^2 and the affected pixels 30 by the working one in the same row is reduced as it is shown in FIG. 7. This is because the significant increase of the defect concentration in the isolation barriers 32 by the introduction of deep level traps as the ion dose increases, which results in higher resistivity and hence, the current becomes isolated.

[0070] Referring to FIG. 8, the resolution of the pixels 30 versus the isolation barrier 30 width 32b for different screen sizes can be simulated. For instance, a width 32b of an isolation barrier 32 can be changing from $0.1\mu\text{m}$ to $2\mu\text{m}$. The resolution of the pixels 30 can be determined by the pixel dimension and the pitch distance 44. For a pixel 30 of $3\mu\text{m}$ width with an isolation barrier 32 width 32b of $0.1\mu\text{m}$, the pitch distance can be $3.1\mu\text{m}$ and for an isolation barrier 32 width 32b of $2\mu\text{m}$, the pitch distance can be $5\mu\text{m}$. For a screen size of a 24 inch as an example, the resolution decreases from 391 Pixel Per Inch (PPI) for an isolation barrier width 32b of 0.1

μm to 242 PPI for an isolation barrier width 32b of 2 μm . Also, the resolution decreases for the same isolation barrier 32 width 32b as the screen size increases (see FIG. 8) since the resolution is inversely proportional to the diagonal size of a screen.

[0071] Referring to FIGS. 9-10, the current density distribution of LEDs 24, pixels 30, and/or arrays 26 under forward bias for different ion implantation dose while keeping the ion energy constants can be simulated. For example, the structure of LEDs 24, pixels 30, and/or arrays 26 can include a sapphire substrate 10, first n-type GaN layer 16, second n-type GaN layer 18, emissive layer 20, p-type GaN layer, and Indium Tin Oxide (ITO) transparent layer as a current spreading and light transmitting layer. A width 32b of an isolation barrier 32 can be 0.1 μm and a depth 32c of an isolation barrier 32 can be 1 μm . Each LED 24 and/or pixel 30 can be connected to a separate p-contact 40. All the LEDs 24 and/or pixels 30 can share the same n-contact 42. The current density of the simulated five pixels 30 for instance decreases and the number of the affected pixels 30 by the working pixel 30 in the same row is also reduced as the implantation dose increases from $1\text{E}17$ to $2\text{E}17$ ions/ cm^2 at ions energy of 200 KeV, as shown from FIG 9 and FIG 10.

[0072] It should be understood that modifications to the embodiments disclosed herein can be made to meet a particular set of design criteria. For instance, the number of substrates 10, layers 14, 16, 18, 20, 22, mesa structures, LEDs 24, pixels 30, arrays 26, isolation barriers 32, contacts 40, 42, displays 28, or other features and components can be any suitable number of each to meet a particular objective. The particular configuration of such elements can also be adjusted to meet a particular set of design criteria. Therefore, while certain exemplary embodiments of devices and methods of making and using the same have been discussed and illustrated herein, it is to be

distinctly understood that the invention is not limited thereto but may be otherwise variously embodied and practiced within the scope of the following claims.

[0073] It will be apparent to those skilled in the art that numerous modifications and variations of the described examples and embodiments are possible in light of the above teachings of the disclosure. The disclosed examples and embodiments are presented for purposes of illustration only. Other alternate embodiments may include some or all of the features disclosed herein.

Therefore, it is the intent to cover all such modifications and alternate embodiments as may come within the true scope of this invention, which is to be given the full breadth thereof.

Additionally, the disclosure of a range of values is a disclosure of every numerical value within that range, including the end points.

WE CLAIM:

1. A light emitting diode (LED) display, comprising:
a substrate having a mesa structure comprising at least one layer formed in or on a portion of the substrate;
at least one LED formed in or on at least a portion of the mesa structure; and,
at least one isolation barrier formed in or on at least a portion of the substrate and/or the mesa structure;
wherein at least a portion of the at least one LED and at least a portion of the at least one isolation barrier forms a planar region.
2. The LED display recited in claim 1, wherein the at least one isolation barrier comprises a volume of space within the substrate and/or the mesa structure having a concentration of ions configured to at least one of electrically isolate and photonically isolate at least a portion of the at least one LED.
3. The LED display recited in claim 1, wherein the at least one LED is configured as a pixel.
4. The LED display recited in claim 1, further comprising a plurality of LEDs.
5. The LED display recited in claim 4, wherein the plurality of LEDs forms at least one LED array.

6. The LED display recited in claim 1, further comprising:
a p-contact connected to the at least one LED; and,
a n-contact connected to at least a portion of the at least one layer.
7. The LED display recited in claim 6, further comprising a plurality of LEDs,
wherein the n-contact is configured as a common contact shared by each LED.
8. The LED display recited in claim 6, further comprising an integrated circuit
bonded to the LED display via the p-contact and the n-contact.
9. The LED display recited in claim 1, wherein the at least one isolation barrier
comprises at least one deep level trap.
10. The LED display recited in claim 1, wherein the at least one layer comprises a
quantum well.
11. The LED display recited in claim 10, wherein the quantum well comprises a
quantum heterostructure.
12. The LED display recited in claim 1, wherein the at least one isolation barrier
comprises at least one ion species selected from the group consisting of H⁺, He⁺, N⁺, F⁺, Mg⁺,
Ar⁺, Zn⁺, O⁺, Ti⁺, Fe⁺, Cr⁺, Mn⁺, and Co⁺.

13. The LED display recited in claim 5, wherein the at least one isolation barrier at least one of electrically isolate and photonically isolate one LED and/or one LED array from another LED and/or LED array.

14. A light emitting diode (LED) display, comprising:
a pixel unit having at least one LED, the LED comprising:
a substrate;
a buffer layer formed in or on at least a portion of the substrate;
a first n-type layer formed in or on at least a portion of the buffer layer;
a second n-type layer formed in or on at least a portion of the first n-type layer;
an emissive layer formed in or on at least a portion of the second n-type layer;
and,
a p-type layer formed in or on at least a portion of the emissive layer; and,
at least one region bordering at least one of the LED and the pixel unit, wherein the at least one region is implanted with at least one ion species via ion implantation, wherein the at least one ion species enters at least one of the p-type layer, the emissive layer, and the n-type layer;
wherein the at least one ion species is configured to serve an isolation function of the at least one region.

15. A method for creating a light emitting diode (LED) display, the method comprising:

generating a mesa structure on a substrate, the mesa structure comprising at least one layer formed in or on at least a portion of the substrate;

forming at least one LED in or on at least a portion of the substrate and/or mesa structure;
and,

generating at least one isolation barrier in or on at least a portion of the substrate and/or the mesa structure;

wherein at least a portion of the at least one LED and the at least one isolation barrier forms a planar region.

16. The method recited in claim 15, wherein generating the at least one isolation barrier further comprises forming a concentration of ions within a volume of space of the substrate and/or the mesa structure configured to at least one of electrically isolate and photonically isolate at least a portion of the at least one LED.

17. The method recited in claim 15, wherein generating the at least one isolation barrier further comprises generating at least one deep level trap.

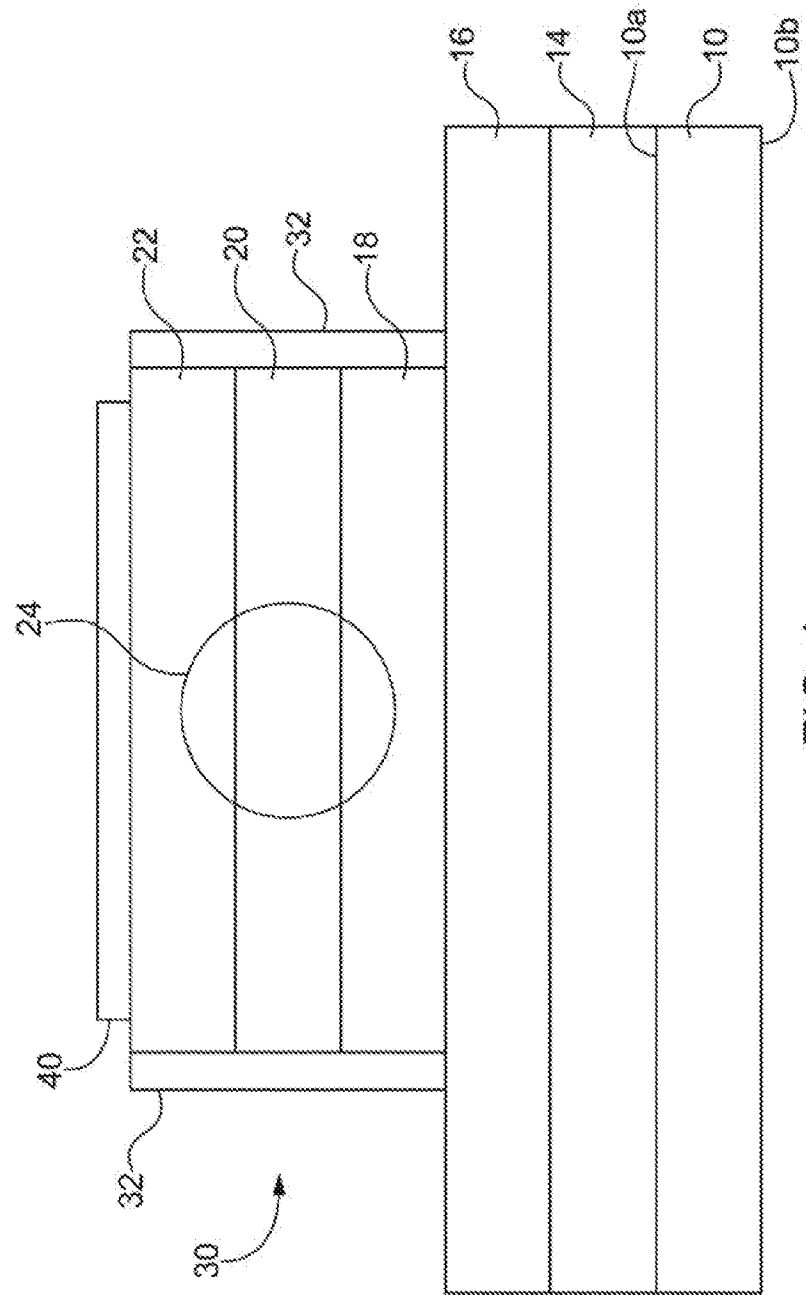
18. The method recited in claim 15, wherein generating the mesa structure further comprises generating at least one quantum well within the at least one layer.

19. The method recited in claim 15, further comprising forming a plurality of LEDs.

20. The method recited in claim 16, further comprising:

forming a plurality of LEDs; and,

forming the at least one isolation barrier to isolate at least one LED from another LED.



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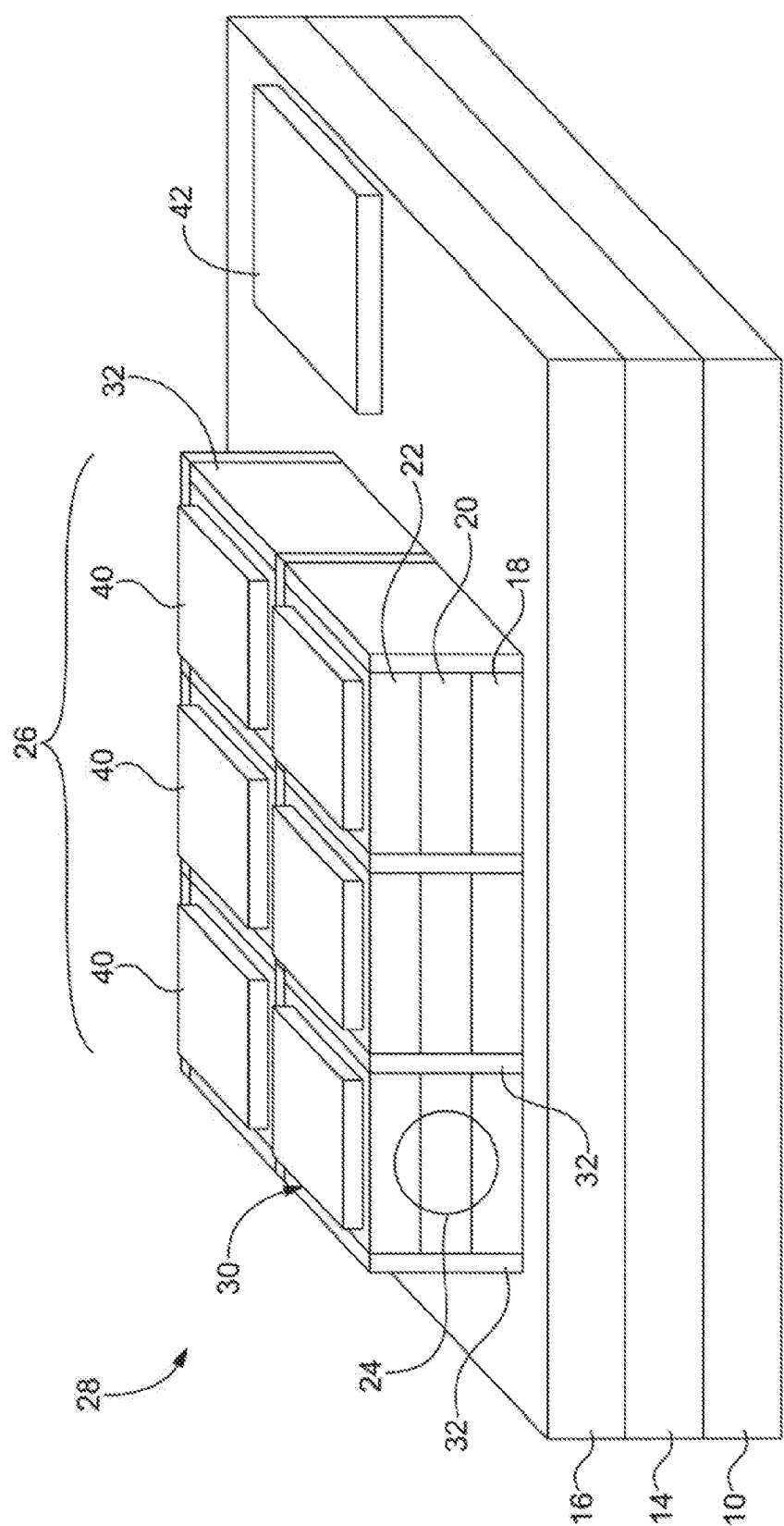


FIG. 2

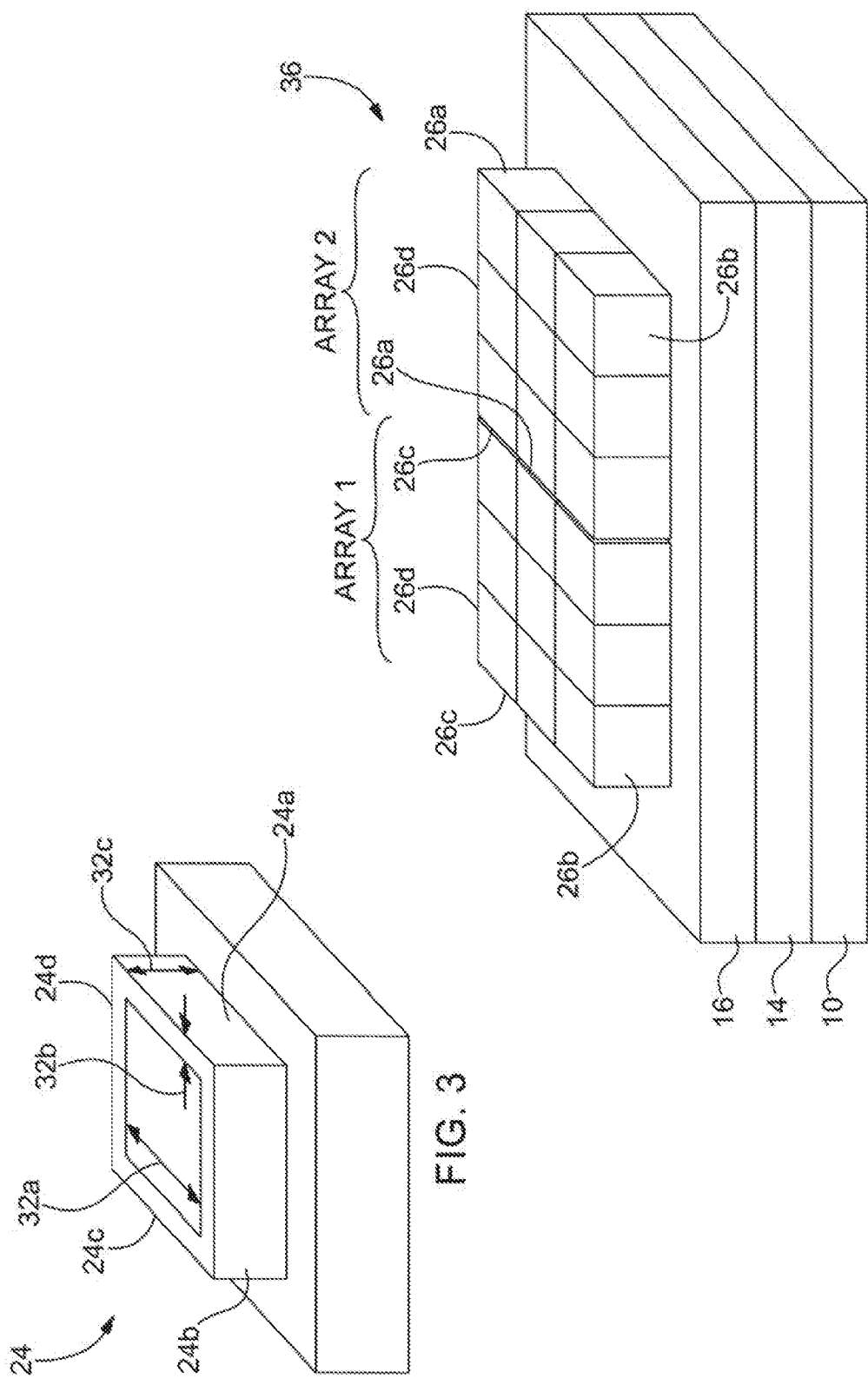


FIG. 4

FIG. 3

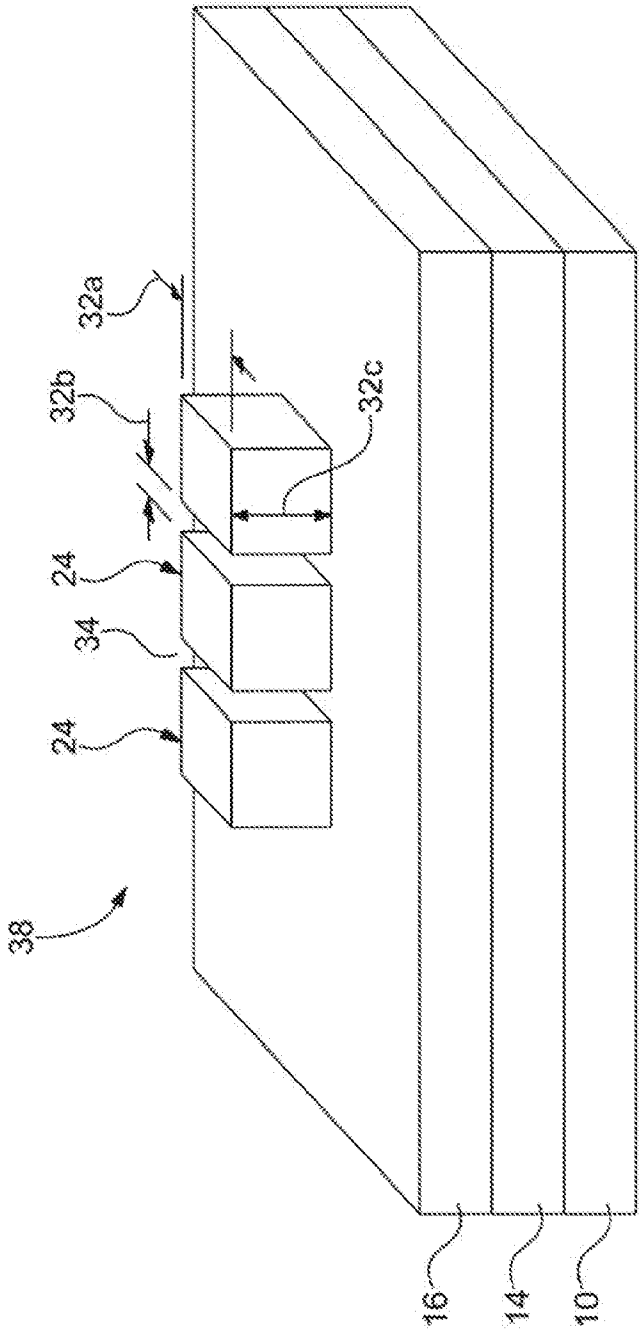


FIG. 5

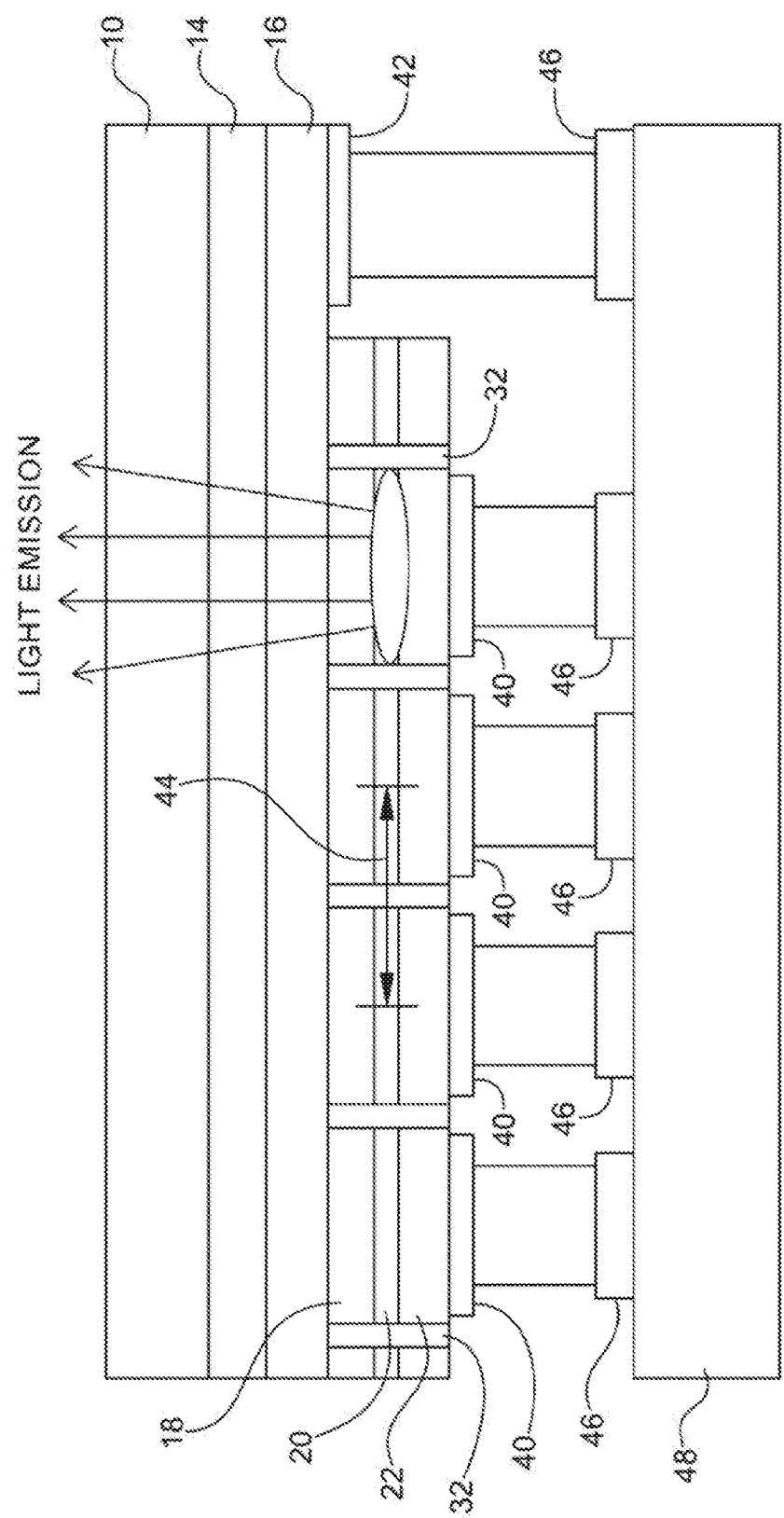
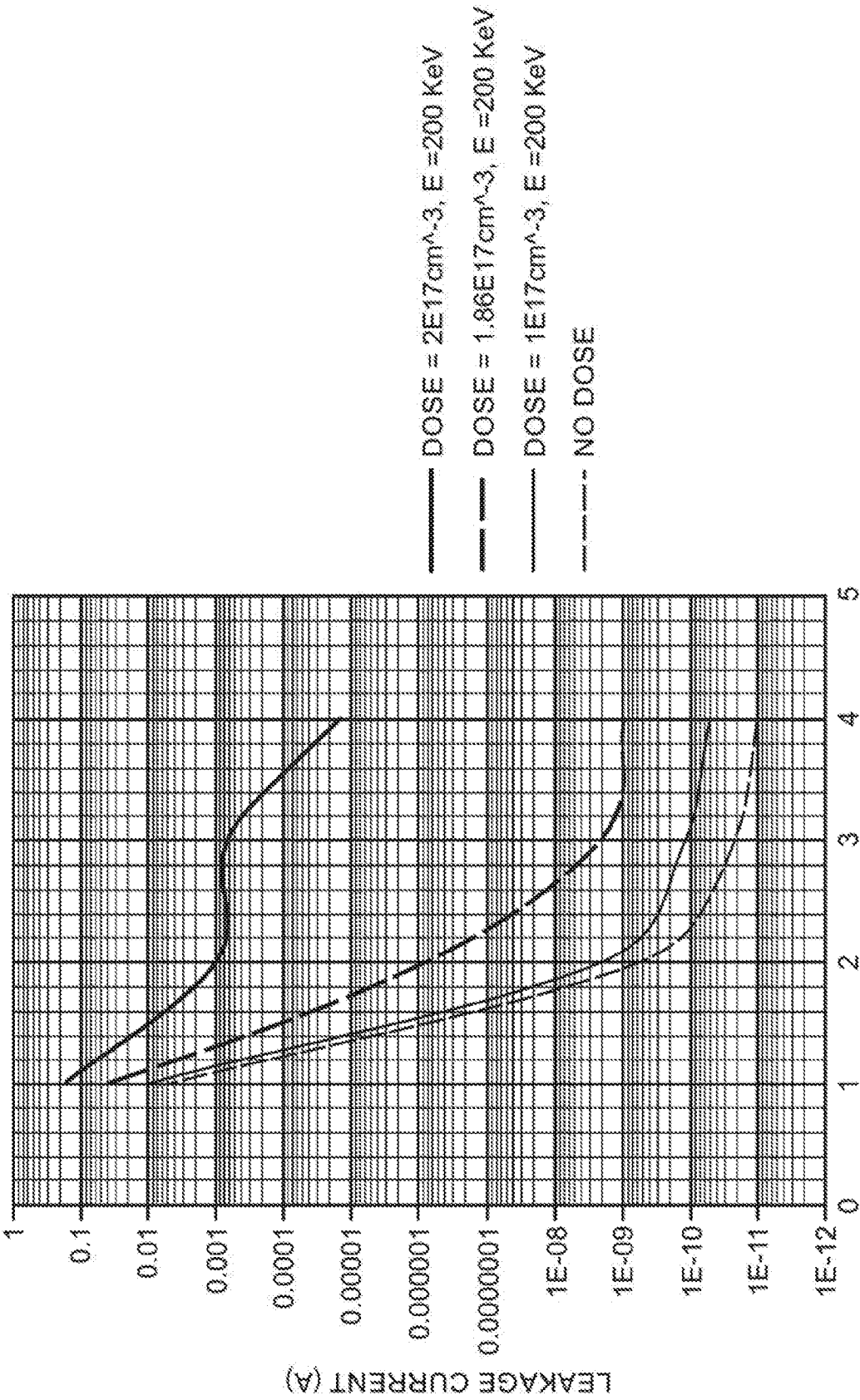


FIG. 6



NUMBER OF THE AFFECTED PIXELS BY THE WORKING PIXEL IN THE SAME ROW FIG. 7

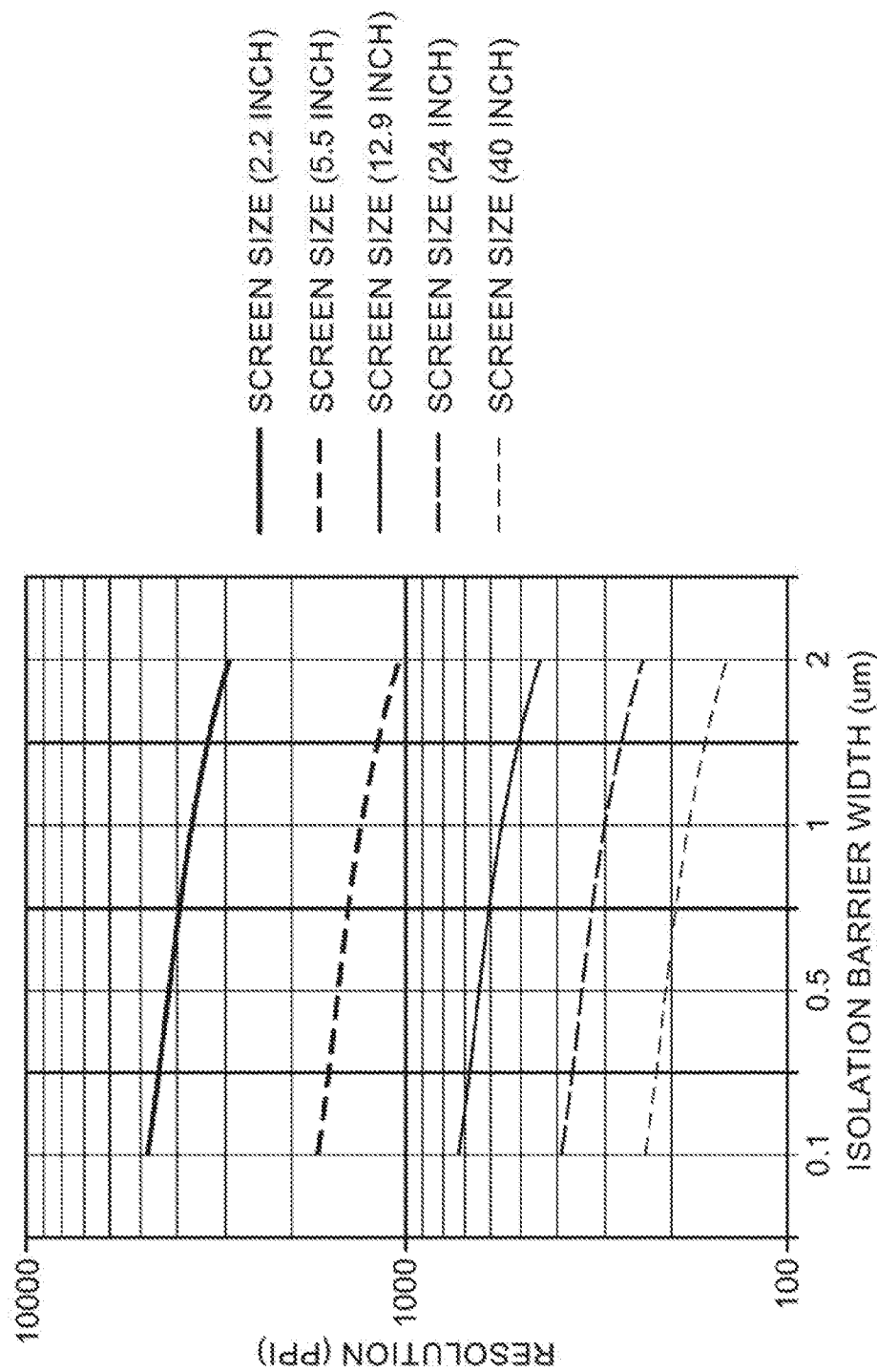


FIG. 8

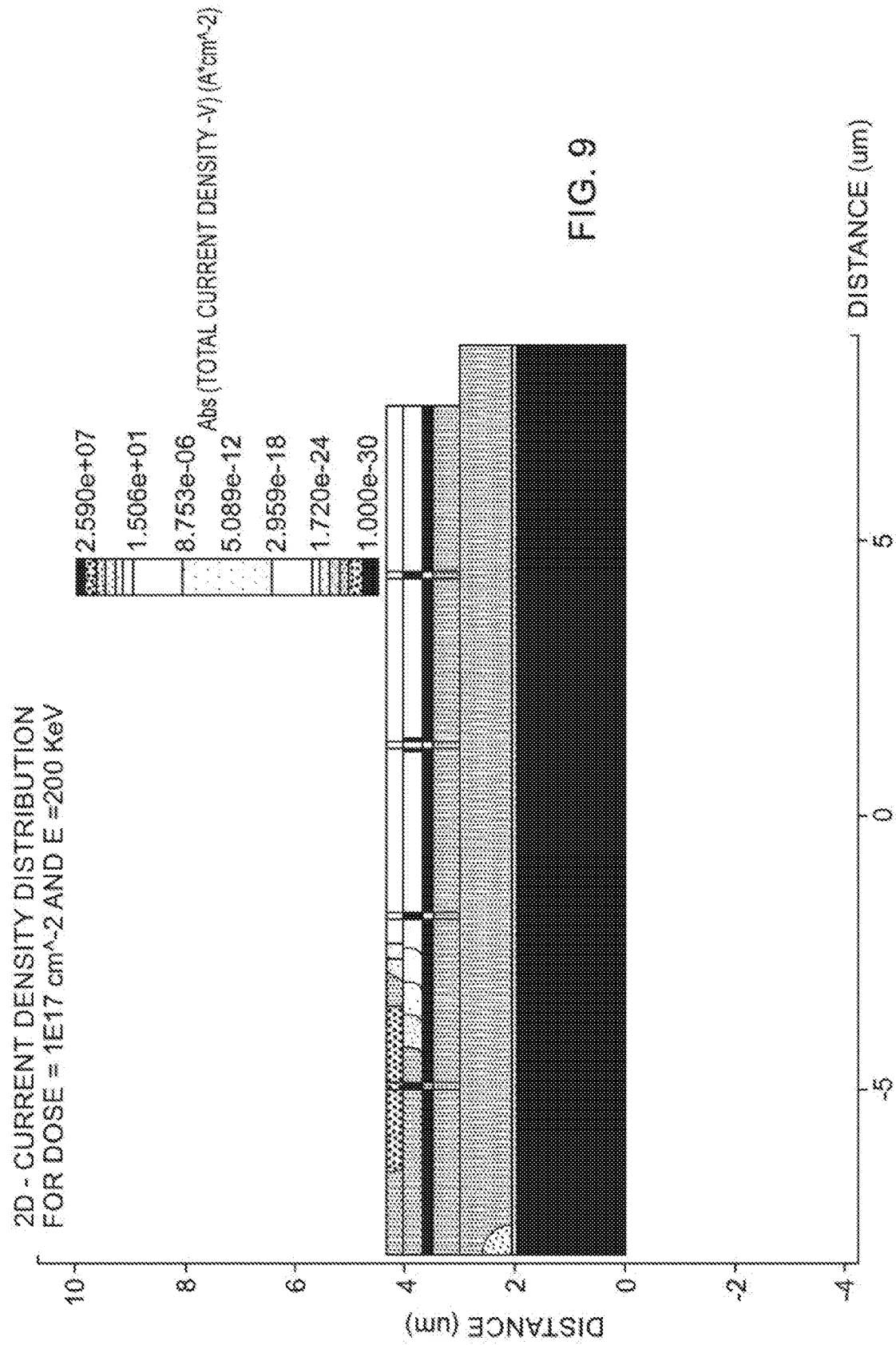


FIG. 9

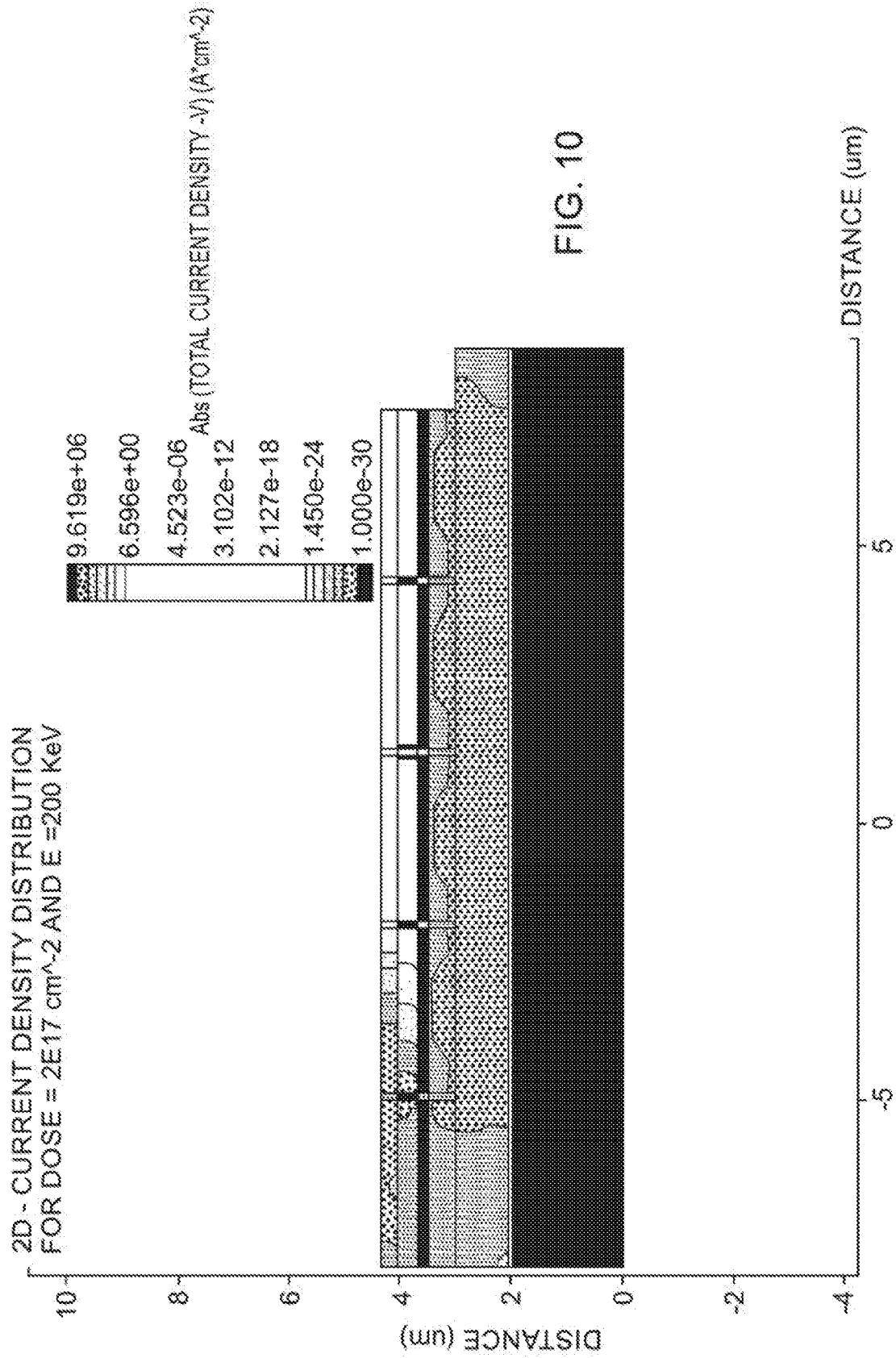


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/028287

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32 (2016.01)**G09F 9/33 (2006.01)****H01L 27/15 (2006.01)**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3/00, 3/32, 5/00, 5/08, G09F 9/00, 9/33, F21V 7/00, 7/04, H01L 21/00, 27/00, 27/12, 27/15, 29/201, 31/12, 33/00-33/4

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/0104726 A1 (CREE, INC.) 23.04.2009, paragraphs [0030], [0032], [0034]-[0036], [0039], [0041]-[0043], [0047], [0050], [0053], [0054], [0072]	1-20
A	US 2014/0061687 A1 (LUXVUE TECHNOLOGY CORPORATION) 06.03.2014	1-20
A	US 2014/0167089 A1 (CREE, INC) 19.06.2014	1-20
A	US 6091195 A1 (THE TRUSTEES OF PRINCETON UNIVERSITY) 18.07.2000	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search

25 September 2017 (25.09.2017)

Date of mailing of the international search report

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