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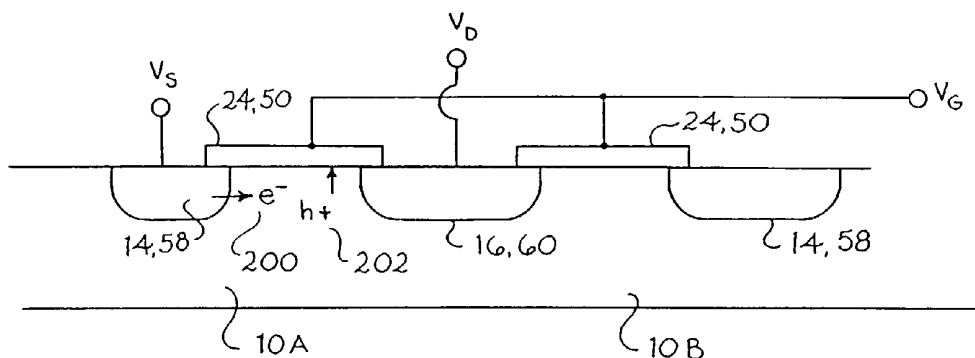
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(54) Title: SELECTIVE ERASURE OF A NON-VOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE



(57) Abstract: A method of selectively erasing a bit of an individual memory cell of an array of non-volatile memory cells by providing an array of non-volatile memory cells that include a first non-volatile two bit memory cell (10A) that is connected in series with a second non-volatile memory cell (10B). The method includes erasing a first bit of the first non-volatile two bit memory cell (10A) while not erasing a second bit of the first non-volatile memory cell (10A).



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## SELECTIVE ERASURE OF A NON-VOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE

### Technical Field

5           The present invention relates to the field of non-volatile memory devices. More particularly, the invention relates to a method of erasing multi-bit flash electrically erasable programmable read only memory (EEPROM) cells that utilize the phenomena of hot electron injection to trap charge within a trapping dielectric material within the gate.

### Background Art

10           Memory devices for non-volatile storage of information are currently in widespread use today, being used in a myriad of applications. A few examples of non-volatile semiconductor memory include read only memory (ROM), programmable read only memory (PROM), erasable programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM) and flash EEPROM.

15           Semiconductor EEPROM devices involve more complex processing and testing procedures than ROM, but have the advantage of electrical programming and erasing. Using EEPROM devices in circuitry permits in-circuit erasing and reprogramming of the device, a feat not possible with conventional EPROM memory. Flash EEPROMs are similar to EEPROMs in that memory cells can be programmed (i.e., written) and erased electrically but with the additional ability of erasing all memory cells at once, hence the term flash EEPROM.

20           An example of a single transistor Oxide-Nitrogen-Oxide (ONO) EEPROM device is disclosed in the technical article entitled "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," T.Y. Chan, K.K. Young and Chenming Hu, IEEE Electron Device Letters, March 1987. The memory cell is programmed by hot electron injection and the injected charges are stored in the oxide-nitride-oxide (ONO) layer of the device. This article teaches programming and reading in the forward direction. Thus, a wider charge trapping region is required to achieve a sufficiently large difference in threshold voltages between programming and reading.  
25           This, however, makes it much more difficult to erase the device.

          Erasure of EEPROM devices in general is disclosed in U.S. Patents Nos. 5,077,691; 5,561,620; 5,598,369; 5,617,357; 5,708,588 and for ONO EEPROM devices is disclosed in both U.S. Patent No. 5,768,192 and PCT patent application publication WO 99/07000, the contents of each reference identified above are hereby incorporated herein by reference. In those disclosed devices, a cell is erased by applying a negative  
30           voltage to the gate or a zero bias on the gate in conjunction with a large, positive bias on the drain over a plurality of cycles.

          As shown in FIG. 1, a well known technique for erasing an array of non-volatile memory cells 41 in a flash memory device 102 is to apply a large positive voltage to the drains 34 along each of the bit lines 104 while simultaneously grounding or applying a small negative voltage to the gates 42 along each of the word  
35           lines 106. This results in all of the memory cells 41 being erased simultaneously. It is believed that erasure of the memory cells 41 is accomplished by "hot" or "warm" holes, generated through band-to-band tunneling, being injected into the nitride trapping layer of the memory cells 41 resulting in the neutralization or compensation for trapped electrons in the nitride trapping layer. This simultaneous erasure of multiple memory cells is disadvantageous in that individual cells cannot be erased.

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**DISCLOSURE OF THE INVENTION**

One aspect of the invention regards a method of selectively erasing a bit of an individual memory cell of an array of non-volatile memory cells by providing an array of non-volatile memory cells that include a first non-volatile two bit memory cell that is connected in series with a second non-volatile memory cell. The method includes erasing a first bit of the first non-volatile two bit memory cell while not erasing a second bit of the first non-volatile memory cell.

The above aspect of the present invention provides the advantage of allowing individual cells of an array of non-volatile memory cells.

The present invention, together with attendant objects and advantages, will be best understood with reference to the detailed description below in connection with the attached drawings.

**BRIEF DESCRIPTION OF DRAWINGS**

FIG. 1 schematically illustrates an array of memory cells that have the structure of FIG. 2 and that are erased in a known manner;

FIG. 2 illustrates a sectional view of a single bit flash EEPROM cell of the prior art utilizing Oxide-Nitride-Oxide (ONO) as the gate dielectric;

FIG. 3 illustrates a sectional view of a two bit flash EEPROM cell constructed in accordance with an embodiment of the present invention utilizing ONO as the gate dielectric;

FIG. 4 illustrates a sectional view of a two bit flash EEPROM cell constructed in accordance with an embodiment of the present invention utilizing a silicon rich silicon dioxide with buried polysilicon islands as the gate dielectric;

FIG. 5A illustrates a sectional view of a flash EEPROM cell of the prior art showing the area of charge trapping under the gate;

FIG. 5B illustrates a sectional view of a flash EEPROM cell constructed in accordance with an embodiment of the present invention showing the area of charge trapping under the gate;

FIG. 6 is a sectional view of a two bit EEPROM cell showing the area of charge trapping under the gate for both the right and the left bus;

FIG. 7 schematically illustrates an array of the two bit EEPROM memory cells of FIGS. 3, 4, 5B and 6 that is selectively erased in a manner according to the present invention; and

FIG. 8 is a sectional view of the array of FIG. 7 that is selectively erased in a manner according to the present invention.

**MODE(S) FOR CARRYING OUT THE INVENTION AND INDUSTRIAL APPLICABILITY**

The structure of a two bit flash EEPROM cell that employs the method of erasure of the present invention can best be understood with an understanding of how single bit charge trapping dielectric flash EEPROM memory cells are constructed, programmed and read. For example, a conventional ONO EEPROM memory cell is shown in FIG. 2 and is disclosed in the technical article entitled "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," TX. Chan, K.K. Young and Chenming Hu, IEEE Electron Device Letters, March 1987, incorporated herein by reference. The memory cell 41 comprises a P-type silicon substrate

30, two PN junctions between N+ source and drain regions 32, 34 and P type substrate 30, a non-conducting nitride layer 38 sandwiched between the two oxide layers 36, 40 and a polycrystalline conducting layer 42.

To program or write the memory cell 41, voltages are applied to the drain 34 and the gate 42 and the source 32 is grounded. For example, 10V is applied to the gate and 9V is applied to the drain. These voltages generate a vertical and lateral electric field along the length of the channel from the source to the drain. This electric field causes electrons to be drawn off the source and begin accelerating toward the drain. As they move along the length of the channel, they gain energy. If they gain enough energy, they are able to jump over the potential barrier of the oxide layer 36 into the silicon nitride layer 38 and become trapped. The probability of this occurring is a maximum in the region of the gate next to the drain 34 because it is near the drain that the electrons gain the most energy. These accelerated electrons are termed hot electrons and once injected into the nitride layer 38 they become trapped and remain stored there. The trapped electrons cannot spread through the nitride layer 38 because of the low conductivity of the nitride layer 38 and the low lateral electric field in the nitride layer. Thus, the trapped charge remains in a localized trapping region in the nitride layer 38 typically located close to the drain 34.

In order to achieve an effective delta in threshold voltage between the unprogrammed and the programmed state of each cell, the charge trapping region of prior art flash EEPROM cells must be made fairly wide. Thus, electrons are trapped in areas far from the drain that directly affects the effectiveness of the erase. In some cases, the device cannot be erased at all because the charge trapping region was programmed too wide.

In memory cells constructed using a conductive floating gate, the charge that gets injected into the gate is distributed equally across the entire gate. The threshold voltage of the entire gate increases as more and more charge is injected into the gate. The threshold voltage increases because the electrons that become stored in the gate screen the gate voltage from the channel.

In devices with low conductivity or non conductive floating gates like the embodiment shown in FIG. 2, the injection of hot electrons into the silicon nitride layer causes the gate threshold voltage to increase only in the localized trapping region. This is in contrast to the conductive floating gate memory cells of EPROMs and EEPROMs wherein the gate threshold voltage of the entire channel rises as programming time increases. In both conductive and non conductive floating gate memory cell designs, an increase in the gate threshold voltage causes the current flowing through the channel to decrease for a given gate voltage. This reduces programming efficiency by lengthening the programming time. However, due to the localized electron trapping in the non conductive floating gate memory cell design, the programming time is reduced less than with the conductive floating gate memory cell design. The technique of programming flash EEPROM memory cells with either conductive or low conductivity or non conductive floating gates is well known in the art and is currently used to program EEPROM and flash EEPROM memory cells.

The conventional technique of reading both prior art conductive floating gate and non conductive localized trapping gate EEPROM or flash EEPROM memory cells is to apply read voltages to the gate and drain and to ground the source. This is similar to the method of programming with the difference being that lower level voltages are applied during reading than during programming. Since the floating gate is conductive, the trapped charge is distributed evenly throughout the entire floating conductor. In a programmed device, the threshold is therefore high for the entire channel and the process of reading becomes symmetrical. It makes no

difference whether voltage is applied to the drain and the source is grounded or vice versa. A similar process is also used to read prior art non conductive localized gate flash EEPROM devices.

The process of programming EPROM and EEPROM memory devices typically includes writing followed by reading. For instance, a short programming pulse is applied to the device followed by a read. The read is actually used to effectively measure the gate threshold voltage. By convention, the gate threshold voltage is measured by applying a voltage to the drain and a separate voltage to the gate, with the voltage on the gate being increased from zero while the channel current flowing from drain to source is measured. The gate voltage that provides 1 pA of channel current is termed the threshold voltage.

Typically, programming pulses (i.e., write pulses) are followed by read cycles wherein the read is performed in the same direction that the programming pulse is applied. This is termed symmetrical programming and reading. Programming stops when the gate threshold voltage has reached a certain predetermined point (i.e., the channel current is reduced to a sufficiently low level). This point is chosen to ensure that a '0' bit can be distinguished from a '1' bit and that a certain data retention time has been achieved.

An embodiment of a two bit flash EEPROM cell that can be employed in an array of memory cells that utilize a method of erasure in accordance with an embodiment of the present invention is shown in Figure 3. The flash EEPROM memory cell 10 includes a P-type substrate 12 having two buried PN junctions, one being between the source 14 and substrate 12, termed the left junction and the other being between the drain 16 and the substrate 12, termed the right junction. Above the channel is a layer of silicon dioxide 18 that has a thickness that ranges between approximately 60 to 100 Angstroms, and which forms an electrical isolation layer over the channel. On top of the silicon dioxide layer 18 is a charge trapping layer 20 that has a thickness ranging from 20 to 100 Angstroms thick and preferably is comprised of silicon nitride, Si<sub>3</sub>N<sub>4</sub>. The charge trapping layer can be constructed using silicon nitride, silicon dioxide with buried polysilicon islands or implanted oxide, for example or it can be made of an oxide implanted with arsenic, for example. The hot electrons are trapped as they are injected into the charge trapping layer so that the charge trapping layer serves as the memory retention layer. The thickness of layer 18 is chosen to be in excess of 50 angstrom to prevent electrons from tunneling through the oxide and leaving charge trapping layer 20 during the operation of the cell. Thus, the lifetime of the cell of this invention is greatly extended relative to prior art MNOS devices. The memory cell 10 is capable of storing two bits of data, a right bit represented by the dashed circle 23 and a left bit represented by the dashed circle 21.

It is important to note that the two bit memory cell is a symmetrical device. For example, the left junction serves as the source terminal and the right junction serves as the drain terminal for the right bit. Similarly, for the left bit, the right junction serves as the source terminal and the left junction serves as the drain terminal. Thus, the terms left, or first junction and right or second junction are used herein rather than source and drain. When the distinction between left and right bits is not crucial to the particular discussion, the terms source and drain are utilized. However, it should be understood that the source and drain terminals for the second bit are reversed compared to the source and drain terminals for the first bit.

Another layer of silicon dioxide 22 is formed over the charge trapping layer, (i.e., silicon nitride layer), and has a thickness that ranges between approximately 60 to 100 Angstroms thick. The silicon dioxide layer 22 functions to electrically isolate a conductive gate 24 formed over the silicon dioxide layer 22 from charge

trapping layer 20. The thickness of gate 24 is approximately 4,000 Angstroms. Gate 24 can be constructed from polycrystalline silicon, commonly known as polysilicon.

Charge trapping dielectric materials other than nitride may also be suitable for use as the asymmetric charge trapping medium. One such material is silicon dioxide with buried polysilicon islands. The silicon dioxide with polysilicon islands is sandwiched between two layers of oxide in similar fashion to the construction of the ONO memory cell in FIG. 3. A sectional view of such a two bit flash EEPROM cell is shown in FIG. 4 where there is a silicon rich silicon dioxide layer 54 with buried polysilicon islands 57 as the gate dielectric is illustrated in FIG. 4. A P-type substrate 62 has buried N+ source 58 and N+ drain 60 regions. The silicon dioxide 54 with buried polysilicon islands 57 is sandwiched between two layers of silicon dioxide 52, 56.

Covering oxide layer 52 is polysilicon gate 50. Gate 50 is typically heavily doped with an N-type impurity such as phosphorus in the 10<sup>19</sup> to 10<sup>20</sup> atom/cc range. Similar to the two bit memory cell of Figure 3, the memory cell of Figure 4 is capable of storing two data bits, a right bit represented by the dashed circle 55 and a left bit represented by the dashed circle 53. The operation of the memory cell of Figure 4 is similar to that of the memory cell illustrated in Figure 3 with programming and reading occurring in opposite directions for each bit.

Alternatively, the charge trapping dielectric can be constructed by implanting an impurity, such as arsenic, into a middle layer 54 of silicon dioxide deposited on top of the bottom oxide 56.

Rather than performing symmetrical programming and reading, the flash EEPROM memory cell of Figure 3 is programmed and read asymmetrically rather than symmetrically as with the cell of Figure 2. This means that programming and reading occur in opposite directions as denoted by the oppositely pointing arrows labeled PROGRAM and READ for each bit (i.e. the left bit and the right bit) in Figure 3. Thus, programming is performed in what is termed the forward direction and reading is performed in what is termed the opposite or reverse direction.

It is noted that throughout the discussion of the EEPROM memory cell of the present invention presented below, the voltage levels discussed in connection therewith are assumed to be independent of the power supply voltage. Thus, the power supply voltages supplied to the chip embodying the EEPROM memory device may vary while the voltages applied to the gate, drain and source thereof will be supplied from regulated voltage sources.

As previously mentioned, the flash EEPROM memory cell 10 of Figure 3 is programmed similarly to the prior art flash EEPROM memory cell of Figure 2. Voltages are applied to the gate 24 and drain 16 creating vertical and lateral electrical fields that accelerate electrons from the source 14 along the length of the channel. As the electrons move along the channel some of them gain sufficient energy to jump over the potential barrier of the bottom silicon dioxide layer 18 and become trapped in the silicon nitride layer 20. For the right bit, for example, the electron trapping occurs in a region near the drain 16 indicated by the dashed circle 23 in Figure 3. Thus, the trapped charge is self-aligned to the junction between the drain 16 and the substrate. Electrons are trapped in the portion of nitride layer 20 near but above and self-aligned with the drain region 16 because the electric fields are the strongest there. Thus, the electrons have a maximum probability of being sufficiently energized to jump the potential barrier of the silicon dioxide layer 18 and become trapped in the nitride layer 20 near the drain 16. The threshold voltage of the portion of the channel between the source 14 and drain 16 under the region of trapped charge increases as more electrons are injected into the nitride layer 20.

It is important to note that in order to be able to subsequently erase memory device 10 effectively, the programming time period must be limited. As the device continues to be programmed, the width of the charge trapping region increases. If programming continues past a certain point the charge trapping region becomes too wide whereby erasing is ineffective in removing trapped charge from the nitride layer 20.

5 However, by reading in the reverse direction an amplification of the effect of the trapped charge injected into the nitride layer results and which leads to dramatically shortened programming times. Reading in the reverse direction permits a much narrower charge trapping region. This in turn greatly increases the erase efficiency since fewer electrons need to be removed to erase the device. In addition, the trapped electrons are stored in a narrower region near the drain also improving the effectiveness of the erase.

10 A description of what occurs during programming is presented first followed by what occurs during reading. Note that the description that follows also pertains to the memory cell of Figure 4 comprising the silicon dioxide layer 54 having buried polysilicon islands 57 substituting for the nitride layer 20 of Figure 3. During programming, hot electrons are injected into the nitride layer 20, as described above. Since the nitride 20 is a nonconductor, the trapped charge remains localized to the region near the drain 34 (Figure 5A) or 16 (Figure 5B). The region of trapped charge is indicated by the cross hatched area 66 in Figure 5A and by the cross hatched area 68 in Figure 5B. Thus, the threshold voltage rises, for example, to approximately 4 V, only in the portion of the channel under the trapped charge. The threshold voltage of the remainder of the channel under the gate remains at, for example, approximately 1 V.

20 In order to read the flash EEPROM memory cell 10 (Figure 5B) in the reverse direction, i.e., the direction opposite that of programming, voltages are applied to the source 14 and the gate 24 and the drain 16 is grounded. Similar to the prior art memory device of Figure 5A, the memory device of Figure 5B is programmed in the forward direction by injecting hot electrons into region 68 of the nitride layer 20. Since nitride 20 is a nonconductor, the trapped charge remains localized to the region near the drain, for the right bit, for example. The left bit is similar except that source and drain functionality are reversed. The region of trapped charge is indicated by the cross hatched area 68 in Figure 5B. Thus, the threshold voltage rises, for example, to approximately 4V only in the portion of the channel under the trapped charge 68. The threshold voltage of the remainder of the channel remains at, for example, approximately 1 V.

25 To read the right bit of the device of Figure 5B in the reverse direction, a voltage is applied to the source 14 and the gate 24, for example 2V and 3V, respectively, and the drain 16 is grounded. A major difference between reading in the forward direction and reading in the reverse direction is that when reading in the reverse direction, the gate voltage required to put the channel of the memory device into inversion increases significantly. For the same applied gate voltage of 3V, for example, there will be no inversion but rather the channel of the memory device will be in depletion. The reason for this is that the channel region next to the drain 16 (which functions as the source in read) is not inverted due to the electron charge in region 68 of the nitride 20. The channel adjacent the source 14 (which functions as the drain in read) is not inverted because 2V is applied to the source 14 and the channel, to be inverted, must be inverted relative to 2 V. In the case of reading in the reverse direction, in order to sustain a higher voltage in the channel, a much wider depletion region must be sustained. A wider depletion region translates to more fixed charge that must be compensated for before there can be inversion. When reading in the reverse direction, to achieve a voltage drop across the charge trapping region 66 of the prior art memory device shown in Figure 5A similar to the voltage drop

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achieved when reading the same device in the forward direction, a higher gate voltage is required, for example, 4 V. A much higher gate voltage is required to pin the voltage in the channel to a higher voltage, i.e., the 2V that is applied to the source terminal rather than ground. In other words, the present invention recognizes and takes advantage of the fact that for the same magnitude potential across the drain and the source, the voltage across the portion of the channel under the trapped charge region 68 (Figure 5B) is significantly reduced when reading occurs in a reverse direction to writing (programming) directly resulting in less punch through and greater impact of the programming charge injected in region 68 of the nitride layer 20 (Figure 5B) on the threshold voltage of the transistor. As an example, for the threshold voltage  $V_T$  equaling 3v during reverse read, a programming time of approximately 2 microseconds is required which is three orders of magnitude less than the programming time required for the same threshold voltage when the cell is read in the forward direction.

By reading in the reverse direction, the amount of charge required to be stored on the nitride to achieve the same increase in threshold voltage in a programmed cell read in the forward direction is reduced in some cases by a factor of two or three. Accordingly, the internal electric fields generated by the charge in the nitride when the memory cell is to be read in the reverse direction are much less than the internal electric fields associated with the charge stored on the nitride when the memory cell is to be read in the forward direction. Consequently electron hopping is exponentially reduced and the small amount of charge stored in the nitride does not disperse laterally through the nitride due to the internally self generated electric fields even during retention bake. Consequently, the memory cell of Figure 3 does not suffer the degradation in performance and reliability of prior art ONO memory cells like those of Figure 2 which are programmed and read in the same direction.

In programming the two bit cell, each bit, i.e., the left and right bit, is treated as if the device was a single bit device. For the right bit, for example, programming voltages are applied to the gate 24 and drain 16 and hot electrons are injected into and trapped in the charge trapping layer 20 in the region near the drain defined by the dashed circle 23. Correspondingly, the threshold voltage of the portion of the channel under the trapped charge increases as more and more electrons are injected in the nitride layer. The programming of the right bit is represented in Figure 3 by the right-pointing arrow labeled 'PROGRAM.' This arrow represents the flow of electrons to the right during programming of the right bit.

Similarly, the left bit is programmed by applying programming voltages to the gate 24 and source 14, which now functions as the drain for the left bit. Hot electrons are injected into and trapped in the charge trapping layer 20 in the region defined by the dashed circle 21. The threshold voltage of the portion of the channel under the trapped charge comprising the left bit increases as more and more electrons are injected into the nitride layer. The programming of the left bit is represented in Figure 3 by the left-pointing arrow labeled 'PROGRAM.' This arrow represents the flow of electrons to the left during programming of the left bit.

The threshold voltage for a programmed left bit will be relatively low compared to the threshold voltage for the right bit and thus the state of the right bit can be read without interference from the left bit. During programming of the right bit, the unprogrammed left bit remains unprogrammed.

Programming the right bit does not affect the unprogrammed left bit. During a second pass or phase, the left bit is programmed and the right bit remains programmed and can still be read. The gate voltage during programming is sufficiently high (typically around 10V) that the programmed right bit does not interfere with



the programming of the left bit except to increase somewhat the time required to reach a given threshold voltage relative to the time required to reach the same threshold voltage for the right bit when the right bit is programmed. In addition, the right bit can be programmed through during programming of the left bit. Further, the programming of the left bit does not disturb the programmed right bit. This is possible because program  
5 through (i.e. the programming of the one bit substantially without interference from the other bit when the other bit is programmed) and read through (i.e. the reading of one bit without interference from the other bit when the other bit is programmed) occurs through both the left and the right bits.

Program through and read through are possible due to the relatively low gate voltages required to turn on each programmed bit when read in the forward direction as occurs when the other bit is read in the reverse  
10 direction. Another way to look at this is that a narrow charge trapping region permits punch through to be more effective. Thus the small amount of charge 68 trapped on the right edge of charge trapping layer 20 (Figure 6) and self-aligned with the junction between region 16 and the substrate 12 and a comparable amount of charge 70 trapped on the left edge of charge trapping layer 20 and self-aligned with the junction between region 14 and the substrate 12 cause a narrow charge trapping region to be formed at both the right side and the left side of charge  
15 trapping layer 20 which is easy to be punched through when the bit is read in the forward direction. Thus when left bit 70 (the charge trapping region 70 is referred to as a bit because the presence or absence of charge in region 70 would represent either a zero or a one) is read in the forward direction, bit 68 is being read in the reverse direction. The punch-through under charge trap region 70 is quite easily achieved with a low gate voltage thereby allowing the charge trapped in bit 68 to control the state of the signal read out of the device.  
20 Thus for equal amounts of charge trapped in regions 70 and 68, reading a bit in the reverse direction results in the opposite bit having no effect on the state of the signal being read.

Another reason that the bit not being programmed is not disturbed is that the programming voltage is not being applied to the drain for the bit previously programmed. When programming the other bit, the programming voltage is applied to the drain for the bit on the other side of the device.

As discussed earlier, the programming duration must be limited for each bit in order the other bit can still be read. For example, in the case when the right bit is programmed, i.e., a logic '0', and the left bit is not programmed, i.e., a logic '1', if the right bit was programmed for too long a time then when the left bit is read, there may be insufficient current for the sense amps to detect a logic '1' because the channel is not sufficiently conductive. In other words, if the right bit is programmed too long, a left logic '1' bit becomes slower, i.e.,  
30 takes longer to read due to lower channel current, or, in the worst case, may appear to be a logic '0' because the over-programmed right bit prevents the left bit from being read. Thus, a window exists in the programming time within which a logic '0' bit must fall. One of the variable parameters is the voltage that is applied to the functional drain region during read. As the drain voltage is increased, a longer programming time, i.e., longer area of trapped charge, is required in order to avoid punch through. Thus, a longer trapping region is equivalent to increasing the programming time. The upper limit of the programming time for the window is the programming time such that a forward read does not change the read current by more than a predetermined percentage compared to the read current for a reverse read. Preferably, the percentage change to the read current should be limited to 10%. This percentage, although not arbitrary, can be optimized according to the design goals of the chip designer. For example, a designer may wish to have three orders of magnitude margin between  
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the threshold voltage of a forward read and the threshold for a reverse read. To achieve this, the gate voltage, drain voltage and implant level are all adjusted accordingly to determine a maximum programming time.

5 The effect of programming one of the bits is that both programming and reading for the second bit is slowed somewhat. The second bit can be programmed as long as the gate voltage during programming is higher than the threshold voltage of the channel with the first bit programmed and sufficient voltage is placed on the drain. The channel resistance, however, is raised due to the programming of the first bit. As long as programming parameters are tuned properly, the higher channel resistance does not prevent the second bit from being programmed and read. The higher channel resistance, however, does cause programming and reading of the second bit to take longer.

10 Reading the two bit cell of FIG. 6, as in programming, each bit is treated as if the device was a single bit device. The area of trapping for the right bit is reference 68 and that of the left bit is referenced 70. Also shown in Figure 6 are two arrows labeled 'READ', one pointed in the left direction indicating the direction for reading of the right bit and one pointed in the right direction indicating the direction for reading of the left bit.

15 The right bit is read in the reverse direction by applying read voltages to the source 14 and the gate 24 and grounding the drain 16. For example, a gate voltage of 3V and a source voltage of 2V is applied. The resulting voltage in the channel VX will be something less than two volts. Similarly, to read the left bit in the reverse direction, read voltages are applied to the gate 234 and to the drain 16 and the source 14 is grounded, e.g., 3V on the gate and 2V on the drain.

20 Should the drain voltage VD is made too low and the first bit is programmed, insufficient voltage exists in the channel for read through to occur. In addition, the second bit to be programmed, in this case the left bit, experiences slower programming due to the increased series resistance of the channel. Even if the second bit is unprogrammed, when the drain voltage is too low and the first bit is programmed, the second bit cannot be read properly. Insufficient voltage exists in order for punch through to occur. If punch through does not occur, the second bit looks as if it is programmed whether it really is or not.

25 Punch through is very sensitive to the length of the trapped charge region, such as regions 68 and 70 of the structure shown in FIG. 6. Should these regions be too wide or not self-aligned with the appropriate region 16 or 14 (depending on whether the charge represents the right bit 68 or the left bit 70), then punch through would not be able to be guaranteed to occur and this concept would not work. Thus, the self-alignment of the trapped charge to the junction between region 16 and the substrate (for the trapped charge 68) and region 14 and the substrate (for the trapped charge region 70) is crucial to the functioning of this invention.

30 A read of the two bit memory device of the present invention falls into one of three cases: (1) neither of the two bits are programmed (2) one of the bits is programmed and the other is not or (3) both of the bits are programmed. The first case does not require a read through. The second case requires reading through the programmed bit to read the unprogrammed bit. In this case the margin is the delta between reading a single bit in the forward direction versus the reverse direction.

The third case requires read through to read both programmed bits. Programming the second bit, in fact, improves the conditions for reading the first bit. This is so because the voltage in the channel is further reduced over the case of reading a single bit. This increases the read margins between programmed and unprogrammed bits.

It is important to note that although the EEPROM cell of FIG. 6 stores two bits, support circuitry and concepts designed to work with single bit memory cells can still be used. For example, the sense amplifier circuitry needed for the two bit memory cell is basically no different than that for the single bit memory cell. In the single bit memory cell, the sense amplifier circuitry is required to distinguish between two states, the programmed and unprogrammed states. Likewise, in the two bit memory cell of FIG. 6, the sense amplifiers must also distinguish between only two states: programmed and unprogrammed. Accurately detecting multiple current levels in a memory device is a complex and difficult task to accomplish. The memory cell of FIG. 6, requires that the sense amplifiers only distinguish between two states as in the single bit memory cell. In the case when one of the bits is unprogrammed, i.e., no charge injected into charge trapping layer for that bit, a read of the other bit will be unaffected by this unprogrammed bit. On the other hand, however, in the case when one bit is programmed, a read of the other bit will be affected by this other programmed bit to some extent. Depending on various process parameters, the programmed bit may cause the channel to be less conductive. However, as long as the channel is sufficiently conductive both bits can still be programmed and read correctly.

With reference to Figure 6, the two bit memory device utilizes a punch through or read through technique to read one bit when the other bit is in a programmed state. In order to read, for example, the right bit 68, the read current must be able to read through or punch through the left bit 70, assuming that both the left bit and the right bit have been programmed. Thus, there is a limit on the length of the charge trapping region that can be programmed. The charge trapping region must be short enough to permit punch through of the bit not being read. If a bit is in the unprogrammed state, there is no constraint on the read current of the other bit from the unprogrammed bit.

It is important to note that when a semiconductor device is scaled, the channel lengths become shorter and short channel effects take hold. Thus, in the two bit memory cell, because each bit is stored in different areas of the transistor, short channel effects may become prevalent sooner than in the case of the single bit transistor. In order to retain the usable range of drain voltage, the two bit transistor may need to be scaled by a smaller factor.

A key concept associated with the two bit EEPROM memory cell of FIG. 6 is that for the device to operate properly, both bits must be able to be written and read. If one of the bits is programmed, a reverse read on the programmed bit must sense a high  $V_T$ , i.e., a '0' and a reverse read on the unprogrammed bit must sense a low  $V_T$ , i.e., a '1'. Thus, a reverse read on the unprogrammed bit, which is equivalent to a forward read on the programmed bit, must punch through the region of trapped charge in order to generate a high enough read current. If this does not happen, the unprogrammed bit will not be able to be read as a '1', i.e., a conductive bit.

In order to achieve this goal, a sufficient margin is generated between reading in the forward and reverse directions. In order to store two bits, there must be sufficient difference between forward read of one of the bits and reverse read of the other bit. In addition, the reverse read current for one of the bits when the other bit is and is not programmed should be sufficient to distinguish between the two bits. For example, for a gate voltage of 3V, punch through for reading in the reverse direction occurs at approximately 1V. Thus, a drain voltage of 1.6V creates a suitable safety margin ensuring that the second bit can be read when the first bit is programmed.

There are two parameters that can be used to ensure punch through of the charge trapping region. The first is the  $V_G$ , applied during reading and the second is the width of the charge trapping region. A low  $V_G$

used during reading combined with a narrow charge trapping region makes a punch through more effective. The lower gate voltage produces a weaker vertical electric field that causes the lateral electric field to be stronger.

5 It is more important to use a low VG during reading in the two bit memory cell than in the single bit memory cell. In the single bit case, it only had to be ensured that the reverse read was better than the forward read, meaning that the VT of a given bit during forward reading was lower than the VT of this bit during reverse reading. In the two bit case, however, it is not enough that the VT drops in the forward case, it must drop sufficiently to be able to punch through when reading the other bit. If the delta VT between the forward and reverse read is not sufficient, one bit cannot be read when the other bit is programmed.

10 The mechanism used to erase the two bit flash EEPROM memory cell of FIG. 6 involves the movement of electrons as opposed to the movement of holes. For the right bit, an erase is performed by removing electrons from the charge trapping nitride region 68 either through the gate 24 via the top oxide 22 or through the drain 16 via the bottom oxide 18. For the left bit, an erase is performed by removing electrons from the charge trapping nitride region 70 either through the gate 24 via the top oxide 22 or through the source 14 via the bottom oxide 18.

15 A known technique of erasing the memory cells of FIGS. 3, 4, 5B and 6 and the array of FIG. 6 involves the movement of electrons as opposed to the movement of holes. For the right bit, an erase is performed by removing electrons from the charge trapping nitride region 68 either through the gate 24 via the top oxide 22, 52 or through the drain 16, 60 via the bottom oxide 18, 56. For the left bit, an erase is performed by removing electrons from the charge trapping nitride region 70 either through the gate 24, 50 via the top oxide 22, 52 or through the source 14, 58 via the bottom oxide 18, 56.

20 Using the right bit as an example, erasing is accomplished by simultaneously applying a negative potential to the gate 24, 50 and a positive potential to the drain 16, 60 such that electron tunneling occurs from the charge trapping nitride layer 20 to the drain 16, 60 via the bottom oxide 18, 56. The left bit is erased in a similar fashion except that a positive potential is applied to the source 14, 58 rather than the drain 16, 60. The electron tunneling is substantially confined to a local area near the drain 16, 60. To facilitate the erasing of the memory cell 10 using this technique, the thickness of the bottom layer 18, 56 is suitably constructed (i.e., has a thickness of about seventy (70) Angstroms) to optimize the removal of electrons from the nitride charge trapping layer 20 into the drain 16, 60.

25 Using the right bit as an example, a second technique of erasing is to simultaneously apply a positive voltage potential to the gate 24, 50 and zero potential, i.e., ground, to the drain 16, 60 such that electron tunneling occurs from the charge trapping nitride layer 20 through the top oxide 22, 52 to the gate 24, 50. The right bit is erased in a similar fashion with zero potential applied to the source 14, 58. In this case, the top oxide 22, 52 is suitably constructed (again with a thickness of about seventy (70) Angstroms) to optimize the tunneling of electrons from the nitride charge trapping layer 20 into the gate 24, 50 in order to facilitate the erasing of the memory cell 10. In one embodiment, the top oxide 22, 52 has a thickness of 50 Angstroms to 80 Angstroms for a voltage on gate 24, 50 of 10 to 18 volts.

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35 The above mentioned two erasure techniques regard the erasure of a single memory cell 10. When the non-volatile memory cells 10 as described with respect to FIGS. 3, 4, 5B and 6 are placed in an array, such as that shown in FIG. 7, it is possible to selectively erase a single memory cell 10 in the array. This is in contrast

with the array of FIG. 1 where all of the memory cells 41 are erased simultaneously in the manner described previously. The technique of selective erasure is described below.

As shown in FIG. 7, a plurality of non-volatile memory cells 10, such as those described previously with respect to FIGS. 3, 4, 5B and 6, are arranged in array so that any individual memory cell 10 will be  
5 connected in series with at least one other memory cell 10 so that the two memory cells 10 form part of a column or row of the array. In the erasure technique schematically shown in FIG. 8, a particular memory cell 10A can be erased while all other memory cells 10B are not erased by 1) applying a positive voltage  $V_D$  to the drains 16, 60 along each of the bit lines 104 except grounding the bit line associated with the drain of a memory cell adjacent to the bit of the particular memory cell 10A to be erased while 2) simultaneously grounding or  
10 applying a small negative voltage to the gates 24, 50 along each of the word lines 106 and 3) simultaneously applying a positive bias to the source 14, 58 of the particular cell 10A to be erased. The magnitudes of the drain voltage  $V_D$  and source voltage  $V_S$  are chosen to have a magnitude and polarity to create a forward bias at the source so as to accelerate electrons 200 from the source 14, 58 to the drain 16, 60 of the memory cell 10A to be  
15 erased so as to attain an energy sufficient to generate hot holes 202 via impact ionization within the memory cell 10A while not producing significant band-to-band currents with the memory cell 10A. In addition, the grounding of the bit line of the adjacent memory cell 10B results in the formation of a large lateral electric field that results in the erasure of the bit associated with the drain of the memory cell 10A to be erased. Applying the positive bias at the source of the memory cell 10A to be erased suppresses erasure of the bit associated with the source due to the high voltage (7 V) applied to the adjacent bit line. Thus, a single bit of a memory cell can be  
20 erased while the other bit of the memory cell is not erased. A drain voltage of approximately 7 V and a gate voltage of approximately -2 V for the cell to be erased should be sufficient for this purpose.

The magnitude and polarity of the gate voltage  $V_G$  and the forward bias are chosen such that the vertical field created by the gate voltage inhibits the accelerated electrons 200 from being injected into the gate  
24, 50 of the cell 10A. However, the magnitude and polarity of the gate voltage is sufficient to allow the hot  
25 holes 202 created by impact ionization to be injected into the layers 24 and 54 so as to neutralize the trapped charge and erase the memory cell 10A. Please note that while the above description regards the selective erasure of a bit of a single memory cell, the process can be applied to other individual memory cells as well in a manner similar to that described above.

Even when the device is programmed to the same threshold voltage, the time to complete the reverse  
30 erase is much less than the time to complete the forward erase. The forward erase (i.e. the time to remove the trapped charge associated with a given threshold voltage when the device is read in the forward direction) is slower than the reverse erase (i.e., the time to remove the trapped charge associated with a given threshold voltage when the device is read in the forward direction). In addition, there is residual charge left in the charge  
35 trapping region. This is due to the larger wider charge trapping region formed during the forward programming that was required to generate a threshold voltage of 4V. The forward erase is approximately an order of magnitude slower than the reverse erase. For the same amount of charge trapping, the equivalent threshold voltage for reverse reading is much higher than that for forward reading. Reading in the reverse direction requires trapped charge so much smaller than does reading in the forward direction that the erase of the trapped charge is approximately 10 to 20 times faster. Also the cell does not enter deep depletion. This is a huge

advantage of the memory cell of FIG. 6 over prior art memory cells especially floating gate cells where over-erase can cause a failure of the memory array due to deep depletion of the charge on the floating gate.

The erase mechanism in the memory cell is self limiting due to the fact that as the memory cell is erased, more and more positive charge is stored in the trapping region 68 (Figure 6) (for the right bit) of the nitride layer thereby neutralizing the negative charge stored there while the remainder of the nitride layer 20 remains unaffected. Thus, the threshold voltage of the channel keeps dropping until it levels off at the threshold voltage of an unprogrammed memory cell that is the threshold voltage of the larger majority of the channel closer to the source. Over-erasing the memory cell of the present invention only affects (i.e., lowers) the threshold voltage of the portion of the channel under the charge trapping region 68 which is a relatively narrow region while leaving the threshold voltage of the remainder of the channel at its normal value.

As explained previously, a result of reading in the reverse direction is that a narrower charge trapping region is required due to the higher efficiency of the reverse read. Since erasing is always performed through the effective drain region 16 (for trapped charge 68 and region 14 for trapped charge 70), less charge needs to be moved off the charge trapping layer 20 and directed through the drain 16 (charge 68) or effective drain 14 (charge 70). Thus, reading the memory cell 10 in the reverse direction enables much faster erase times. This makes the entire erase process much easier than in prior art memory devices.

Reading the memory device of FIG. 6 in the reverse direction does not just enable simpler and faster erasing, but in fact, if the device is to be read in the forward direction and the trapped charge is so adjusted to give the desired threshold voltage  $V_T$ , erasing is likely to be not possible at all. This is because much more charge must be trapped on the dielectric 20 beneath the gate 24 to achieve a usable difference in threshold voltage  $V_T$  between the programmed and the unprogrammed state when reading in the forward direction than when reading in the reverse direction. This makes erasing the memory device at best difficult if not impossible thus making the forward programming/forward read impractical for this type of memory device that must be erasable.

In terms of optimization, three parameters can be varied to give the quickest programming time and the widest margins. The first parameter is the channel length. A longer channel length, for a given programming time when reading in the reverse direction, increases the distance between the drain and the trapped charge (effectively, the source and drain designations are flipped). This lowers the level of the lateral electric field even lower.

The second parameter is the gate voltage that can be set to minimize the voltage drop in the channel across the channel region beneath the trapped charge. This further reduces the lateral electric field in the channel beneath the trapped charge. Within limits, the voltage in the channel can be 'dialed in' by varying the voltage on the gate. This allows control over the voltage drop in the channel beneath the region of trapped charge. If the gate voltage is made too low then reading a logic '1', i.e., the unprogrammed state, becomes problematic. The gate voltage for reading a logic '1' must be still high enough to generate inversion in order to produce sufficient read current for each sense amplifier. Thus, a lower limit for the gate voltage is approximately 1V above the threshold voltage. The lower limit for the gate voltage is determined by the maximum time required to sense the channel current that represents one state of the memory cell. For example, for fast access time, the maximum time would be in the range of 10 to 30 nanoseconds while for a mass storage device the maximum access time could be as high as 1 microsecond. The actual gate voltage to achieve these

maximum times would depend upon the device structure, the dielectric thickness, the bit line capacitance, the doping concentration in the channel and other parameters associated with the device. An upper limit on the gate voltage is the voltage at which the voltage in the channel just beneath the edge of the region of trapped charge is just below the voltage potential applied to the source terminal during reading in the reverse direction. A too high gate voltage will cause inversion in the channel and the benefits of the present invention are lost. Thus, it is not recommended to apply a gate voltage that generates such a high voltage in the channel beneath the edge of the charge trapping region because it defeats the benefits of having a lower potential across the portion of the channel beneath this charge trapping region with the accompanying reduction in leakage current and shortened programming time. The gate voltage used for reading is approximately 3V that represents an optimized tradeoff between programming time and leakage current.

The third optimization method, previously described and which is known in the art, is to vary the boron doping of the channel region under the gate. An increase in the doping concentration results in a higher threshold voltage  $V_T$  and a lower voltage generated in the channel. This is due to the reduction in the width of the depletion region formed. Thus a higher doping concentration permits a higher gate voltage to be applied for the same voltage across the portion of the channel beneath the charge trapping region.

In addition, an increase in the NA doping concentration for the same length trapping region will improve the punch through behavior of the device. By varying the level of boron implanted in the channel region, the width of the depletion region under the gate can be varied. An increase in the doping concentration results in a reduction in the width of the depletion region for the same applied gate voltage. The reduction in the width of the depletion region occurs because there is now more fixed charge in the substrate. Thus, varying the doping concentration can be used to limit the length of the pinchoff region under the gate. In addition, the doping concentration can be used to increase or decrease the initial threshold voltage of the device.

Optimization parameters specific to programming and reading two bits in the memory cell of the present invention will now be described. The optimizations for programming include utilizing a longer minimum effective channel length  $L_{eff}$  in order to physically separate the two bits better. In addition, the implant level can be reduced in the channel in order to increase the delta between forward and reverse programming. On the other hand, the implant level can be increased in the channel in order to reduce the impact of the first bit on the programming of the second bit. Thus, the implant level in the channel is a compromise between the forward and reverse delta on the one hand and the programming speed on the other hand.

The optimizations for reading include lowering the gate voltage in order to enhance the punch through during reading. As described previously, punch through is necessary to program and read the second bit. A lower implant level in the channel serves to increase punch through. Also, a higher drain voltage during read functions to increase punch through. These three optimizations relate to reading in the forward direction, which is equivalent to reading the second bit in the reverse.

In addition, a lower gate voltage reduces the number of electrons that need to be injected into the charge trapping region. This improves erasing because it eliminates residual charge remaining trapped after erasure. Any residual charge that remains in the charge trapping layer after erasure degrades cycling.

The foregoing description is provided to illustrate the invention, and is not to be construed as a limitation. Numerous additions, substitutions and other changes can be made to the invention without departing from its scope as set forth in the appended claims.

## I CLAIM:

1. A method of selectively erasing a bit of an individual memory cell of an array of non-volatile memory cells, the method comprising:  
providing an array of non-volatile memory cells that comprises a first non-volatile  
5 two bit memory cell (10A) that is connected in series with a second non-volatile memory cell (10B);  
said method characterized by,  
erasing a first bit of said first non-volatile two bit memory cell (10A) while not  
erasing a second bit of said first non-volatile memory cell (10A).
- 10 2. The method of claim 1, comprising applying a positive bias to a source (14, 58) of  
said first non-volatile memory cell (10A).
3. The method of claim 2, comprising applying a positive voltage to a drain (16, 60) of  
15 said first non-volatile memory cell (10A).
4. The method of claim 2, wherein the second non-volatile memory cell (10B) is  
adjacent to said first bit and is simultaneously grounded when said positive bias is applied to said source (14,  
58) of said first non-volatile memory cell (10A).
- 20 5. The method of claim 2, comprising applying a non-positive voltage to gates (24, 50)  
of said first non-volatile memory cell (10A) and said second non-volatile memory cell (10B).
6. The method of claim 3 wherein said positive bias has a magnitude such that hot holes (202)  
25 are generated in said first non-volatile memory cell (10A).
7. The method of claim 6, wherein said positive bias has a magnitude that accelerates electrons  
(200) within said first non-volatile memory cell (10A) to generate said hot holes (202) via impact ionization  
within said first non-volatile memory cell (10A) while not producing significant band-to-band currents with said  
30 first non-volatile memory cell (10A).
8. The method of claim 2, wherein the magnitude of said positive bias is such as to accelerate  
electrons (200) toward a drain (16, 60) of said first non-volatile memory cell (10A), and said electrons (200) are  
not injected into a gate (24, 50) of said first non-volatile memory cell (10A).
- 35 9. The method of claim 6, wherein said hot holes (202) are injected into a gate (24, 50) of said  
first non-volatile memory cell (10A) so as to erase said first bit.
10. The method of claim 1, wherein said first non-volatile memory cell (10A) comprises:  
a substrate (12, 62) that comprises a first region and a second region with a  
40 channel therebetween;



5 trapping region (20, 54); and  
a gate (24, 50) above said channel;  
a charge trapping region (20, 54) that contains a first amount of charge;  
a dielectric layer (18, 56) that lies between said channel and said charge  
an electrical isolation layer (22, 52) located above said channel.

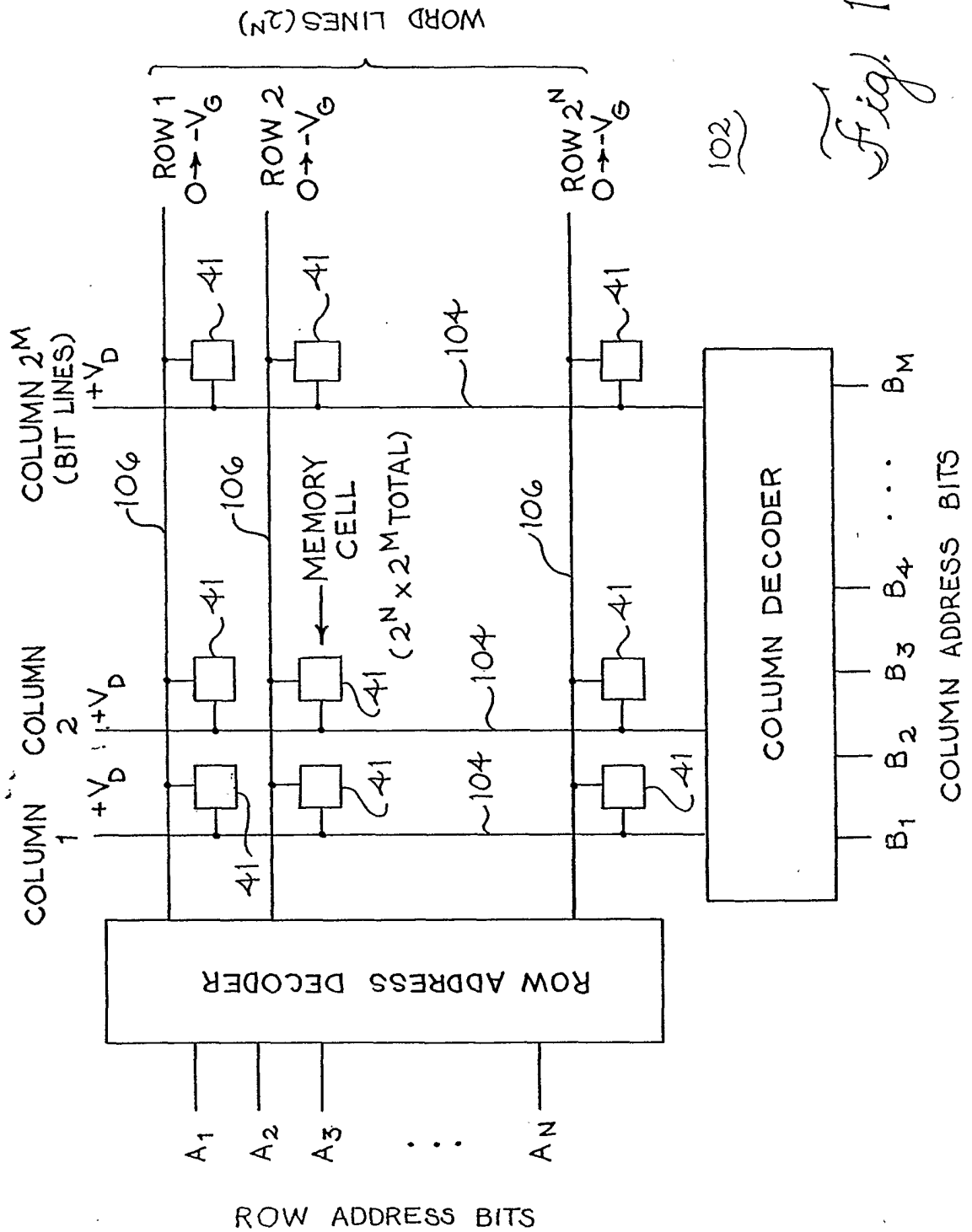
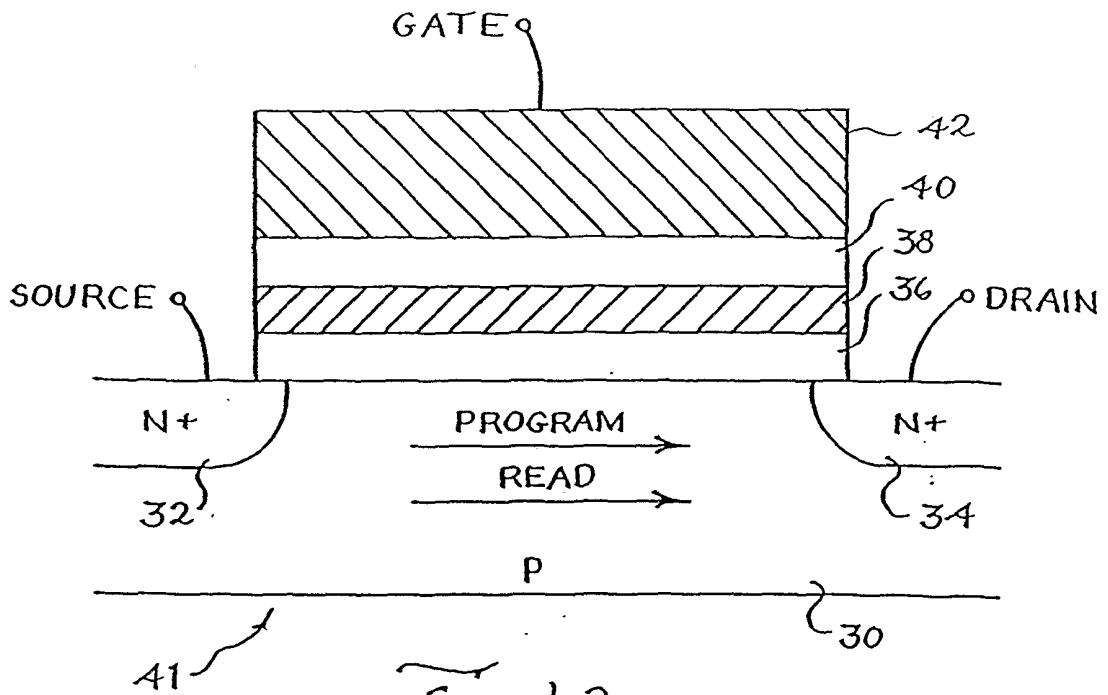


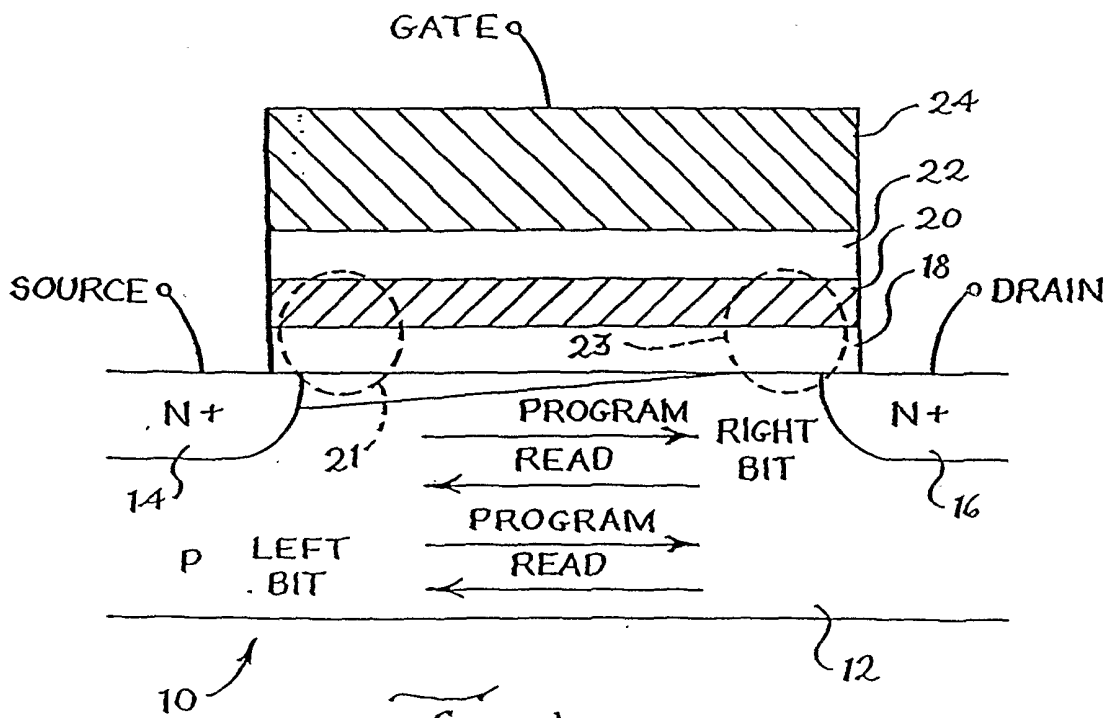
Fig. 1

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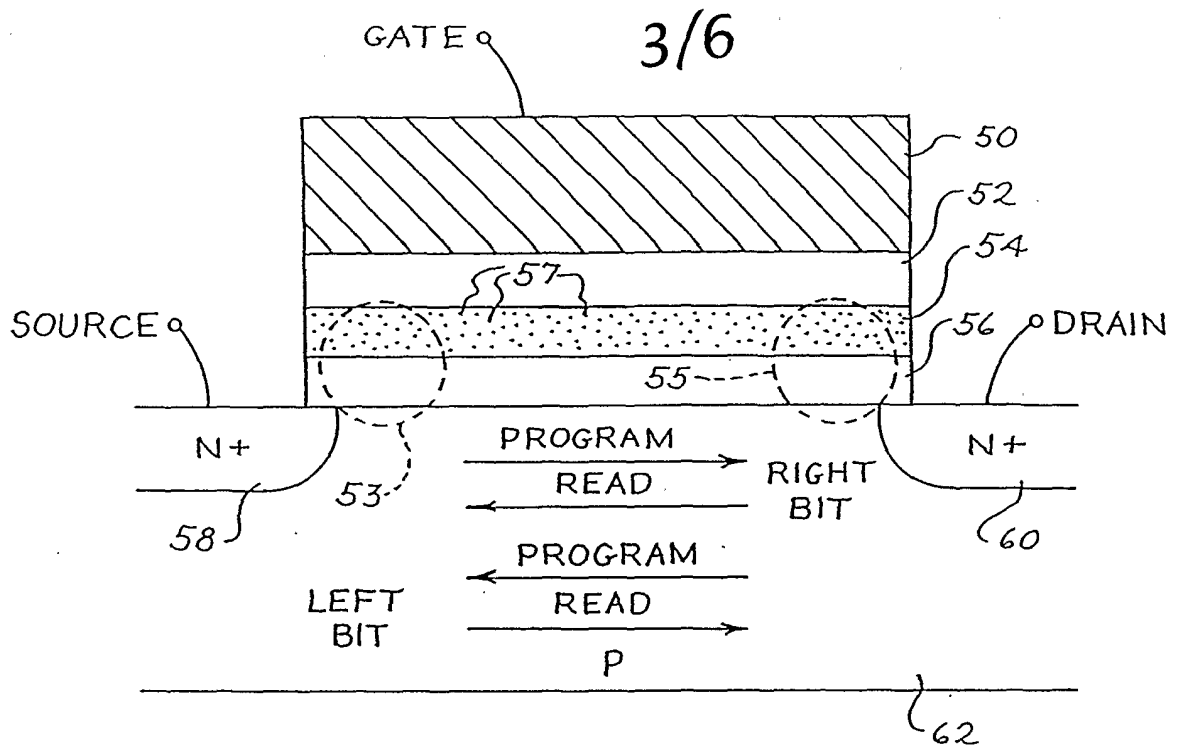
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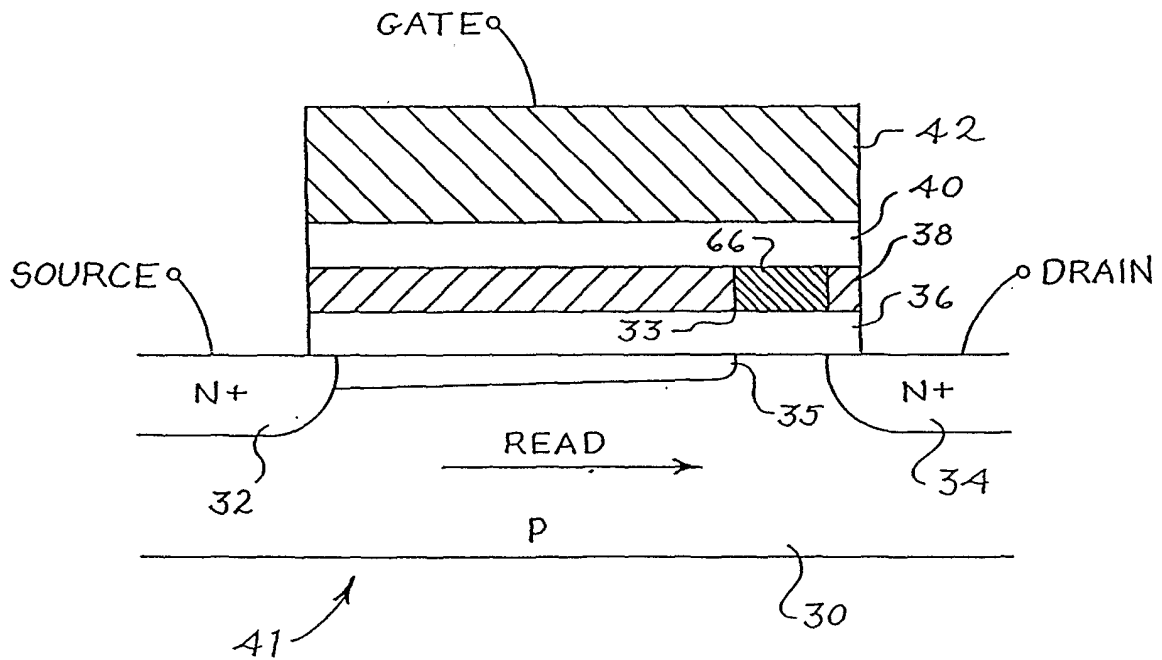
*Fig. 2 (PRIOR ART)*



*Fig. 3*



*Fig. 4*



*Fig. 5 A (PRIOR ART)*

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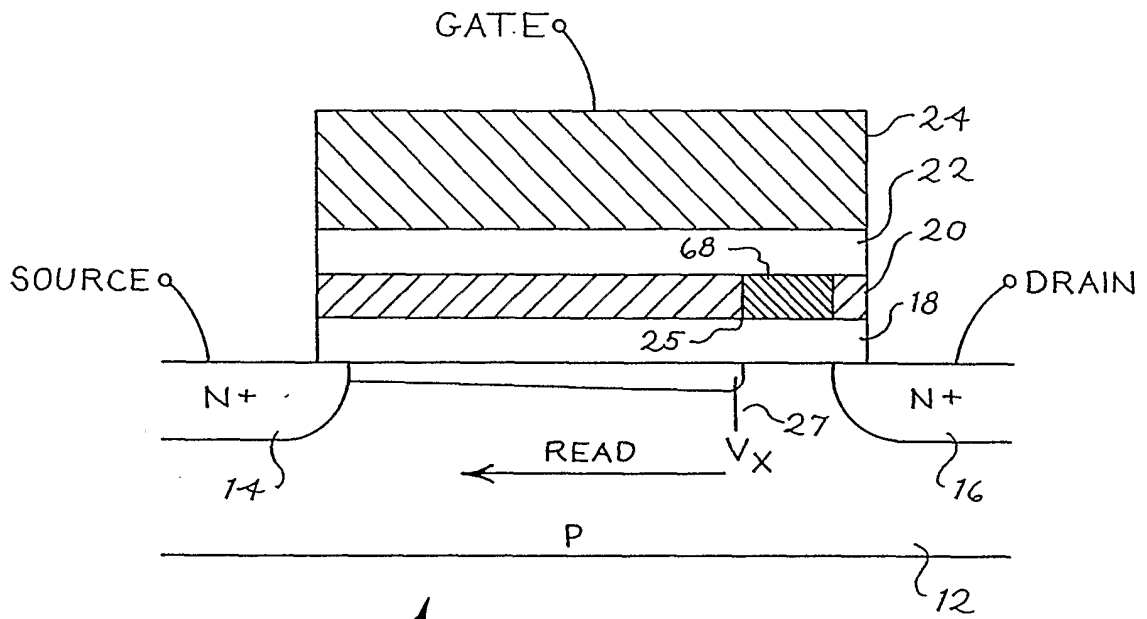


Fig. 5 B

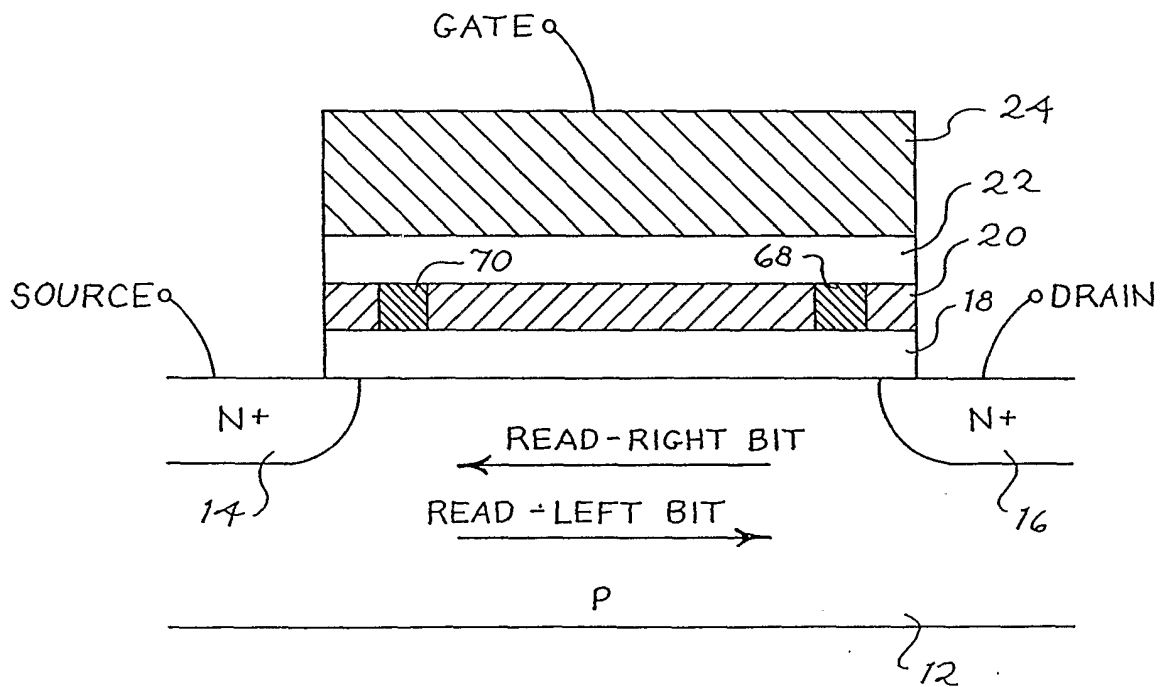
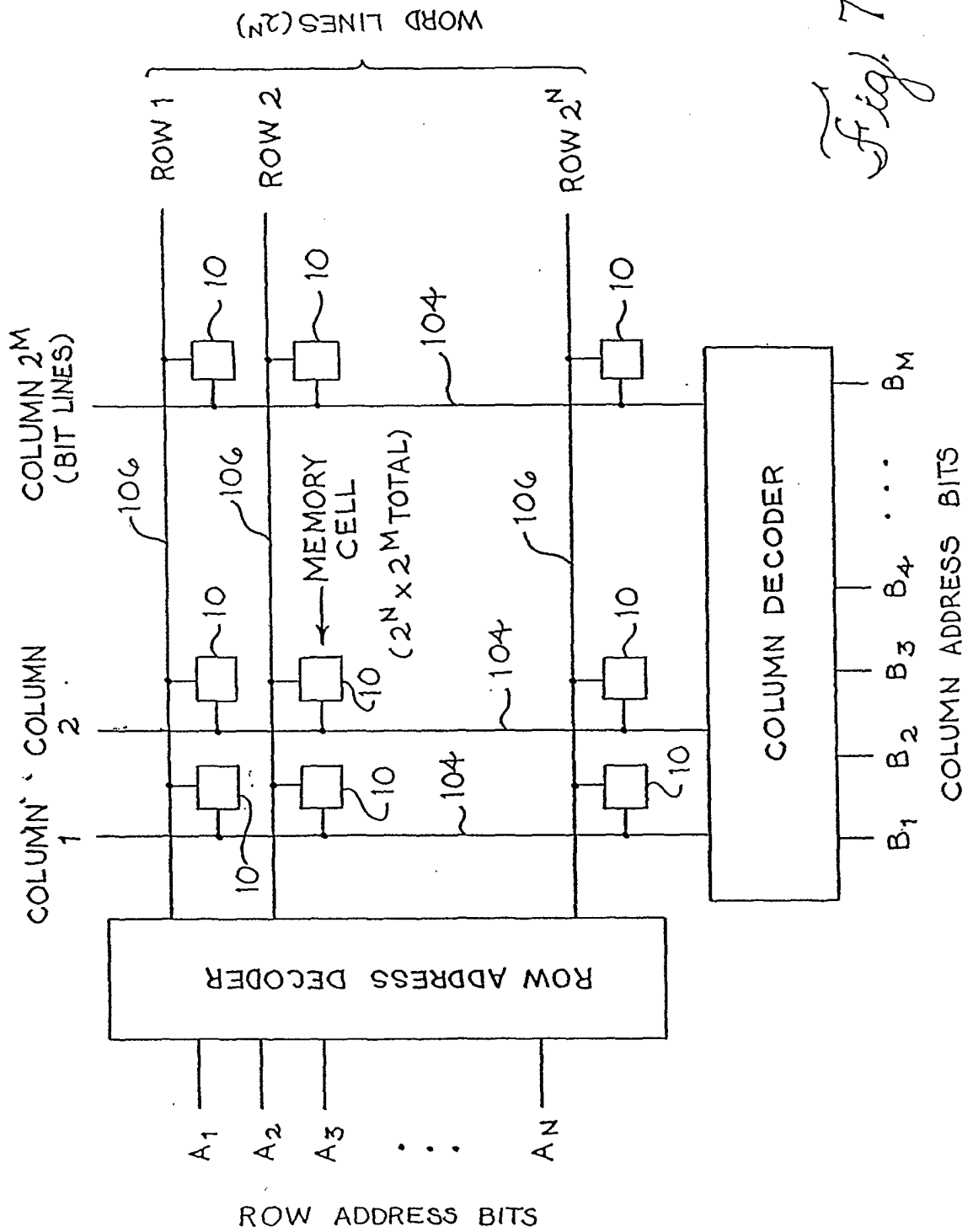


Fig. 6

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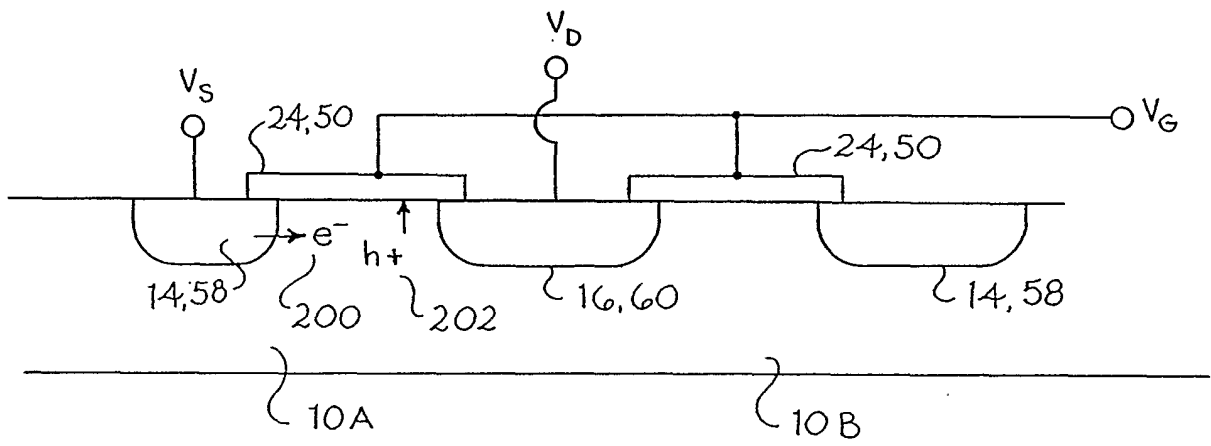


Fig. 8