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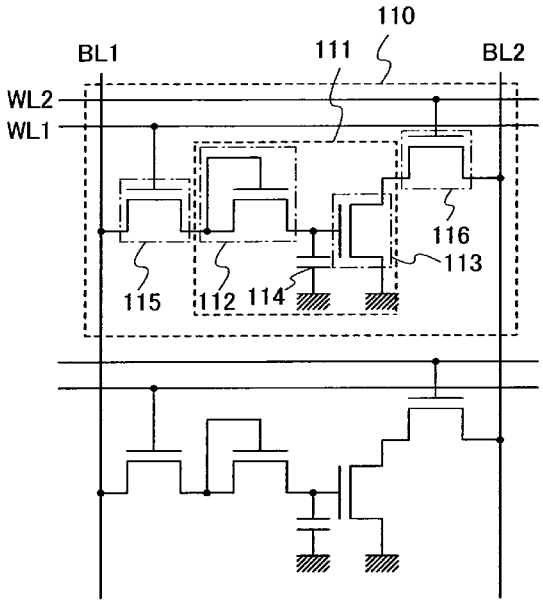
[Continued on next page]

(54) Title: SEMICONDUCTOR MEMORY DEVICE

FIG. 2A



(57) Abstract: It is to provide a semiconductor memory device in which high voltage is not needed in writing, a defect is less likely to occur, the writing time is short, and data cannot be rewritten without an increase in cost. The semiconductor memory device includes a memory element which includes a diode-connected first transistor, a second transistor whose gate is connected to one terminal of a source electrode and a drain electrode of the diode-connected first transistor, and a capacitor connected to the one terminal of the source electrode and the drain electrode of the diode-connected first transistor and the gate of the second transistor.

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DESCRIPTION

SEMICONDUCTOR MEMORY DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to semiconductor memory devices and to a manufacturing method thereof.

BACKGROUND ART

[0002]

In recent years, most electronic devices such as computers can perform desired operations by using a variety of data. When the data is held in, for example, a semiconductor memory device (also referred to as a memory) or the like, the data can be used temporarily or permanently.

[0003]

A semiconductor memory device also includes an external memory device (an auxiliary memory device) such as a hard disk or a flexible disk in a broad sense. However, a semiconductor memory device almost always refers to a semiconductor memory device such as a CPU (central processing unit).

[0004]

Two main types of semiconductor memory devices are a volatile memory and a nonvolatile memory. A volatile memory refers to a semiconductor memory device in which data is lost when the power is turned off. In addition, a nonvolatile memory is a semiconductor memory device in which data is continuously held even after power is turned off and in which data can be held semi-permanently after the data is written.

[0005]

Although a volatile memory has a possibility of losing data, it has an advantage of short access time. In addition, although a nonvolatile memory can hold data, it has a disadvantage of high power consumption. Semiconductor memory devices each have features in this manner, and each of the semiconductor memory devices is used in accordance with the kind or usage of data.

[0006]

There are various kinds of nonvolatile memories such as an unwritable read only memory (ROM), a flash memory in which writing and erasing can be performed multiple times, and an electronically erasable and programmable read only memory (EEPROM). Of these, a write-once memory in which writing can be performed only once is preferable because data is difficult to falsify and high security can be provided in this memory.

[0007]

An example of a write-once memory is an anti-fuse type memory in which voltage is applied to both terminals of an element formed using amorphous silicon to form silicide in the terminals and to short-circuit. Further, a rewritable memory such as a flash memory or an EEPROM is used and a memory region where erasure is not performed is provided, whereby the rewritable memory is logically used as a write-once memory in some cases (see Patent Document 1).

[Reference]

[0008]

Patent Document 1: Japanese Published Patent Application No. H7-297293

DISCLOSURE OF INVENTION

[0009]

However, in a conventional write-once memory, there is a problem in that high-voltage writing is needed. It is necessary to apply voltage which is larger than voltage used for reading operation in order to make a permanent change in a memory element in the write-once memory. For example, in writing, a silicide-type write-once memory in which silicide is used as a memory element needs a voltage of 6 V to 8 V, whereas a voltage of 15 V to 18 V is needed when the flash memory or the EEPROM is used as a write-once memory. Accordingly, a boosting circuit is necessary for generation of such a high potential; therefore, power consumption in writing increases. In order to apply high voltage to the memory element, it is also necessary to apply high-potential voltage to a peripheral circuit such as a decoder in writing. Consequently, in order to increase withstand voltage so that the peripheral circuit may withstand high voltage, an increase in a channel length, formation of an LDD region,

and the like should be performed, which increases the number of manufacturing steps and hinders high integration.

[0010]

In some cases, the silicide-type write-once memory becomes in a semi-short-circuit state with high resistance (the state in which resistance is high such that data is not recognized as data 1 described later by a reading operation) due to shortage of writing voltage or the like. An element which becomes a semi-short-circuit state with high resistance is a substantially defective element.

[0011]

In addition, the silicide-type write-once memory cannot write data in a plurality of memory cells at the same time, and it is difficult to write data in many memory elements in a short time. Further, in the case of the flash memory or the EEPROM, it is possible to write data in a plurality of memory cells at the same time, but the writing time is as long as approximately 100 μs.

[0012]

In the flash memory or the EEPROM which can be used as a write-once memory by the operation of a logic circuit, data stored in the write-once memory might be rewritten due to the malfunction of the logic circuit. In particular, when a rewritable memory and a write-once memory in a semiconductor memory device are formed using memory cells having the same structure, this problem easily occurs. Further, malfunction of the logic circuit might occur by the operation of a malicious user, and data in the write-once memory might be falsified.

[0013]

In view of the above problems, an object of one embodiment of the present invention is to provide a semiconductor memory device in which high voltage is not needed in writing, a defect is less likely to occur, the writing time is short, and data cannot be rewritten without an increase in cost.

[0014]

One embodiment of the present invention is a semiconductor memory device including a memory element which includes a diode-connected first transistor and a second transistor whose gate is connected to one terminal of a source electrode and a drain electrode of the diode-connected first transistor. Note that one terminal of a

source electrode and a drain electrode of the second transistor and the one terminal of the source electrode and the drain electrode of the diode-connected first transistor form a parasitic capacitance.

[0015]

Another embodiment of the present invention is a semiconductor memory device including a memory element which includes a diode-connected first transistor, a second transistor whose gate is connected to one terminal of a source electrode and a drain electrode of the diode-connected first transistor, and a capacitor connected to the one terminal of the source electrode and the drain electrode of the diode-connected first transistor and the gate of the second transistor.

[0016]

When the second transistor is on, that is, voltage higher than threshold voltage is applied to the gate thereof, a state of writing data is set. When the second transistor is off, that is, voltage lower than the threshold voltage is applied to the gate thereof, a state of non-writing data is set. One terminal of the source electrode and the drain electrode of the diode-connected first transistor functions as an anode. When a channel region of the diode-connected first transistor is formed using an oxide semiconductor, whereby off-state current can be reduced to less than or equal to 1×10^{-19} A/μm, and further, less than or equal to 1×10^{-20} A/μm. Therefore, a potential of the gate of the second transistor which rises by writing of data, or the potential of the gate of the second transistor and the capacitor, which rises by writing of data, is less likely to leak from the diode-connected first transistor, and the potential of the gate of the second transistor can be held. In other words, the data which is written once can be held.

[0017]

Therefore, the writing voltage can be set to voltage with which the second transistor can be turned on, that is, greater than or equal to the threshold voltage of the second transistor, and the writing voltage can be reduced. A boosting circuit for writing voltage is not necessarily provided. Power consumption in writing can be reduced, and an increase in a channel length for higher withstand voltage and formation of an LDD region are unnecessary. Therefore, the size of a memory element can be

reduced, and high integration can be achieved.

[0018]

Unlike the silicide-type write-once memory, a memory element can be formed using a transistor; therefore, writing defects can be reduced.

[0019]

In a semiconductor memory device of one embodiment of the present invention, the writing time is determined by the on-state current of the diode-connected first transistor and the capacitance of the capacitor, and writing of data is finished in approximately 1 μs even when the on-state current of the first transistor is 10^{-6} A and the capacitance of the capacitor is 1 pF. Further, writing of data in a plurality of memory elements can be performed at the same time. Therefore, the writing time is greatly reduced.

[0020]

The memory cell included in a semiconductor memory device of one embodiment of the present invention is a write-once memory; therefore, rewriting of data due to the malfunction of a logic circuit does not occur. In addition, a rewritable memory can be formed only by modification in the wiring layout of the memory element in the write-once memory; therefore, a semiconductor memory device in which a rewritable memory and a write-once memory are combined can be formed. Accordingly, the security of holding data in the semiconductor memory device can be improved.

[0021]

A semiconductor memory device in which high voltage is not needed in writing, a defect is less likely to occur, the writing time is short, and data cannot be rewritten can be formed without an increase in cost.

BRIEF DESCRIPTION OF DRAWINGS

[0022]

FIGS. 1A and 1B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 2A and 2B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIG. 3 is an equivalent circuit illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 4A and 4B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 5A and 5B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIG. 6 is an equivalent circuit illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 7A and 7B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIG. 8 is an equivalent circuit illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 9A and 9B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 10A and 10B are block diagrams each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 11A and 11B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 12A and 12B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 13A and 13B are equivalent circuits each illustrating a semiconductor memory device according to one embodiment of the present invention.

FIG. 14 is a top view illustrating a semiconductor memory device according to one embodiment of the present invention.

FIG. 15 is a cross-sectional view illustrating a semiconductor memory device according to one embodiment of the present invention.

FIGS. 16A to 16E are cross-sectional views illustrating a method for manufacturing a semiconductor memory device according to one embodiment of the present invention.

FIG. 17 is a diagram illustrating an RFID tag.

FIG. 18 is a diagram illustrating an RFID tag.

FIGS. 19A to 19F are diagrams illustrating application examples of RFID tags.

FIGS. 20A to 20C are equivalent circuits used for simulation and a graph showing results thereof.

FIG. 21 is a graph showing characteristics of a transistor including an oxide semiconductor.

FIG. 22 is a circuit diagram for evaluating characteristics of a transistor including an oxide semiconductor.

FIG. 23 is a timing chart for evaluating characteristics of a transistor including an oxide semiconductor.

FIG. 24 is a graph showing characteristics of a transistor including an oxide semiconductor.

FIG. 25 is a graph showing characteristics of a transistor including an oxide semiconductor.

FIG. 26 is a graph showing characteristics of a transistor including an oxide semiconductor.

BEST MODE FOR CARRYING OUT THE INVENTION

[0023]

Hereinafter, the embodiments and the examples of the present invention will be described with reference to the accompanying drawings. Note that the present invention is not limited to the following description, and those skilled in the art can easily understand that modes and details of the present invention can be changed in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention should not be limited to the descriptions of the embodiments and the examples below. In describing structures of the present invention with reference to the drawings, reference numerals denoting the same components are used in different drawings.

[0024]

Note that the size, the thickness of a layer, and a region of each structure illustrated in the drawings and the like in the embodiments and the examples are exaggerated for simplicity in some cases. Therefore, the embodiments and the examples of the present invention are not limited to such scales.

[0025]

Note that terms with ordinal numbers such as "first", "second", and "third" in this specification are used in order to identify components, and the terms do not limit the components numerically.

[0026]

In addition, voltage refers to a potential difference between a given potential and a reference potential (e.g., a ground potential) in many cases. Accordingly, voltage, potential, and a potential difference can be referred to as potential, voltage, and a voltage difference, respectively.

[0027]

Note that both a source electrode and a drain electrode in a transistor are connected to a semiconductor layer. Current flows in accordance with a potential difference between the source electrode and the drain electrode when voltage is applied to a gate electrode; therefore, the source electrode and the drain electrode may be exchanged for each other depending on an operation, and it is sometimes difficult to identify where a source electrode and a drain electrode are from their positions. Thus, when a structure of a transistor is described, names "source electrode" and "drain electrode" are used. Alternatively, names "one of a source electrode and a drain electrode" and "the other of the source electrode and the drain electrode" are used. Further alternatively, names "first electrode" and "second electrode" are used. Note that there is no particular difference in meaning depending on such names.

[0028]

(Embodiment 1)

In this embodiment, a structure of a semiconductor memory device which is one embodiment of the present invention will be described with reference to drawings. Note that in this embodiment, the case where an n-channel transistor in which electrons are majority carriers is used is described; it is needless to say that a p-channel transistor in which holes are majority carriers can be used instead of the n-channel transistor.

[0029]

A memory element which is one embodiment of the present invention is illustrated in each of FIGS. 1A and 1B. A memory element 101 illustrated in FIG. 1A includes a diode-connected transistor 102, a transistor 103, and a capacitor 104. A gate of the transistor 103 is connected to a first electrode of the capacitor 104 and a first

electrode of the transistor 102. A second electrode of the transistor 102 is connected to a gate of the transistor 102. Here, a connection region where the gate of the transistor 103, the first electrode of the capacitor 104, and the first electrode of the transistor 102 are connected is referred to as a node A, whereas a connection region where the second electrode of the transistor 102 and the gate thereof are connected is referred to as a node B.

[0030]

In the memory element described in this embodiment, the first electrode of the diode-connected transistor 102 functions as an anode. A channel region of the diode-connected transistor 102 is formed using an oxide semiconductor. The transistor 102 including an oxide semiconductor in the channel region has low off-state current. The transistor 102 is diode-connected, and the gate of the transistor 102 is connected to the second electrode of the transistor 102. Therefore, current flows from the node B to the node A when the transistor 102 is on; however, current which flows from the node A to the node B is extremely small when the transistor 102 is off.

[0031]

Here, in the memory element 101, a state in which the potential of the node A is low (that is, the transistor 103 is turned off) is data 0, whereas a state in which the potential of the node A is high (that is, the transistor 103 is turned on) is data 1.

[0032]

The diode-connected transistor 102 is on, and the voltage which is higher than the threshold voltage of the transistor 103 is charged in the capacitor 104, that is, voltage which makes the transistor 103 turn on is applied to the node A, whereby data 1 can be written to the memory element 101.

[0033]

On the other hand, after the writing of data is finished, the transistor 102 is turned off. Even when the potential of the node B where the gate of the transistor 102 is connected to the second electrode thereof decreases, the transistor 102 has very low off-state current and is diode-connected; therefore, current is less likely to flow from the first electrode of the transistor 102 to the second electrode thereof. Accordingly, voltage charged in the node A does not decrease, and voltage of the node A can be held for a long period of time. Consequently, written information (data 1) cannot be

rewritten, and the memory element 101 can be operated as a write-once memory substantially. Note that the capacitance of the capacitor 104 is set as appropriate in accordance with the required retention time of data.

[0034]

Note that when a parasitic capacitance is formed in a first electrode or a second electrode of the transistor 103 and the first electrode of the diode-connected transistor 102, the capacitor 104 is not necessarily provided. The memory element in that case includes the diode-connected transistor 102 and the transistor 103, and the gate of the transistor 103 is connected to the first electrode of the transistor 102, as illustrated in FIG. 1B. In addition, the second electrode of the transistor 102 is connected to the gate of the transistor 102.

[0035]

Next, an embodiment of a memory cell array in which memory cells each having the memory element of FIG. 1A are arranged in matrix is illustrated in each of FIGS. 2A and 2B and FIG. 3.

[0036]

FIG. 2A is a diagram illustrating one embodiment of a NOR memory cell array.

[0037]

A memory cell 110 includes a memory element 111; a transistor 115 whose gate is connected to a word line WL1 for writing, whose first electrode is connected to the memory element 111, and whose second electrode is connected to a bit line BL1 for writing; and a transistor 116 whose gate is connected to a word line WL2 for reading, whose first electrode is connected to a bit line BL2 for reading, and whose second electrode is connected to the memory element 111. The transistor 115 functions as a selection transistor for writing, and the transistor 116 functions as a selection transistor for reading.

[0038]

The memory element 111 includes a diode-connected transistor 112, a transistor 113, and a capacitor 114. A second electrode of the transistor 112 is connected to a gate thereof and is connected to the first electrode of the transistor 115. A gate of the transistor 113 is connected to a first electrode of the capacitor 114 and a first electrode of the transistor 112. In addition, a first electrode of the transistor 113 is

connected to the second electrode of the transistor 116, and a second electrode of the transistor 113 has a fixed potential. A second electrode of the capacitor 114 also has a fixed potential.

[0039]

FIG. 2B is a diagram illustrating one embodiment of a NOR memory cell array which is different from that in FIG. 2A.

[0040]

A memory cell 130 includes a memory element 131; and a transistor 135 whose gate is connected to the word line WL1 for writing, whose first electrode is connected to the memory element 131, and whose second electrode is connected to the bit line BL1 for writing. The transistor 135 functions as a selection transistor for writing.

[0041]

The memory element 131 includes a diode-connected transistor 132, a transistor 133, and a capacitor 134. A second electrode of the transistor 132 is connected to a gate thereof and is connected to the first electrode of the transistor 135. A gate of the transistor 133 is connected to a first electrode of the capacitor 134 and a first electrode of the transistor 132. A first electrode of the transistor 133 is connected to the bit line BL2 for reading, and a second electrode thereof has a fixed potential. A second electrode of the capacitor 134 is connected to the word line WL2 for reading.

[0042]

FIG. 3 is a diagram illustrating one embodiment of a NAND memory cell array.

[0043]

A memory cell 120 includes a memory element 121; and a transistor 125 whose gate is connected to a word line WL for writing, whose first electrode is connected to the memory element 121, and whose second electrode is connected to a bit line BL for writing. The transistor 125 functions as a selection transistor for writing.

[0044]

The memory element 121 includes a diode-connected transistor 122, a transistor 123, and a capacitor 124. A second electrode of the transistor 122 is connected to a gate thereof and is connected to the first electrode of the transistor 125. A gate of the transistor 123 is connected to a first electrode of the capacitor 124 and a first electrode of the transistor 122. A first electrode of the transistor 123 is connected

to a data line DL for reading, and a second electrode of the transistor 123 is connected to a first electrode of the transistor 123 of the next line. A second electrode of the capacitor 124 has a fixed potential.

[0045]

Channel regions of the diode-connected transistors 112, 122, and 132 are each formed using an oxide semiconductor. The transistors 112, 122, and 132 each including an oxide semiconductor in the channel region have low off-state current. The transistors 112, 122, and 132 are diode-connected, and the gates of the transistors 112, 122, and 132 are connected to the second electrodes of the transistors 112, 122, and 132, respectively. Therefore, current flows from the node B to the node A when the transistors 112, 122, and 132 are on; however, extremely small current flows from the node A to the node B when the transistors 112, 122, and 132 are off.

[0046]

Each of channel regions of the transistors 113, 115, 116, 123, 125, 133, and 135 can be formed using any of an amorphous silicon layer, a micro-crystalline silicon layer, a polysilicon layer, and a single crystal silicon layer. In a manner similar to that in which the diode-connected transistors 112, 122, and 132 are formed, each of the channel regions of the transistors 113, 115, 116, 123, 125, 133, and 135 may be formed using an oxide semiconductor.

[0047]

In the semiconductor memory device described in this embodiment, the channel region of the diode-connected first transistor is formed using an oxide semiconductor, whereby off-state current can be reduced to less than or equal to 1×10^{-19} A/μm, and further, less than or equal to 1×10^{-20} A/μm. Therefore, the potential of the gate of the second transistor and the capacitor, which rises by writing of data, is less likely to leak from the diode-connected first transistor, and the potential of the gate of the second transistor can be held. In other words, the data which is written once can be held.

[0048]

The data writing voltage can be set to voltage with which the second transistor can be turned on, that is, greater than or equal to the threshold voltage of the second

transistor, and the writing voltage can be reduced. A boosting circuit for writing voltage is not necessarily provided. Power consumption in writing can be reduced, and an increase in a channel length for higher withstand voltage and formation of an LDD region are unnecessary. Therefore, the size of a memory element can be reduced, and high integration can be achieved.

[0049]

The writing time of the semiconductor memory device described in this embodiment is determined by the on-state current of the diode-connected first transistor and the capacitance of the capacitor, and writing of data is finished in approximately 1 μs in the case where the on-state current of the first transistor is 10^{-6} A and the capacitance of the capacitor is 1 pF. Further, writing of data in a plurality of memory elements can be performed at the same time. Therefore, the writing time can be greatly reduced.

[0050]

The memory cell included in the semiconductor memory device described in this embodiment is a write-once memory; therefore, rewriting of data due to the malfunction of a logic circuit does not occur. Accordingly, the security of holding data in the semiconductor memory device can be improved.

[0051]

Note that the memory cell and the memory cell array which are described in this embodiment are one embodiment, and the structures are not limited thereto.

[0052]

(Embodiment 2)

In this embodiment, writing and reading of data in the semiconductor memory device described in Embodiment 1 will be described with reference to drawings.

[0053]

The writing of data in the NOR memory cell 110 illustrated in FIG. 2A will be described with reference to FIG. 4A.

[0054]

First, a first potential is applied to the bit line BL1 for writing and the word line WL1 for writing, which are connected to the memory cell 110 in which data is written, and the bit line BL2 for reading and the word line WL2 for reading are each set at a

ground potential. The first potential is a potential at which the transistors 113 and 115 are turned on. The first potential is a potential which is higher than the threshold voltage of each of the transistors 113 and 115, and is 2 V here.

[0055]

When the potential of the word line WL1 for writing is the first potential, the transistor 115 functioning as a selection transistor for writing and the diode-connected transistor 112 are turned on, so that the potential of the node A, that is, the potential of the capacitor 114 and the gate of the transistor 113, increases to approximately the same as the potential of the bit line BL1 for writing; accordingly, the transistor 113 is turned on. Through the above steps, data 1 can be written.

[0056]

Note that as long as electric charge enough to turn on the transistor 113 is charged in the node A in order to write data 1, a boosting circuit for writing data is unnecessary, and the writing voltage is applied to a logic circuit which drives the memory cell 110 from a power source. Time enough to charge the capacitor 104 is sufficient as the writing time; therefore, when the on-state current of the transistors 112 and 115 is 10^{-6} A and the capacitance of the capacitor 114 is 1 pF, writing of data is finished in a short time of approximately 1 μs.

[0057]

After the writing of data is finished, the potential of the bit line BL1 for writing and the potential of the word line WL1 for writing are 0 V as illustrated in FIG. 4B. Accordingly, although the transistor 115 functioning as a selection transistor for writing and the diode-connected transistor 112 are off, the off-state current of the transistor 112 which is formed using an oxide semiconductor is very low; therefore, the voltage of the node A is held for a long period of time. Specifically, the off-state current of the transistor 112 formed using an oxide semiconductor is less than or equal to 1×10^{-19} A/μm, preferably less than or equal to 1×10^{-20} A/μm. Therefore, when a capacitance of 1 pF is added to the capacitor 114, data can be held for 20 days to 200 days, and the memory element 111 functions as a write-once memory. Note that "to hold data" here means a state in which the potential of the capacitor 114 is greater than or equal to 90 % of the potential in writing of data 1, namely, greater than or equal to 1.8 V.

[0058]

Next, reading of data in the memory cell 110 illustrated in FIG. 2A will be described with reference to FIGS. 5A and 5B. FIG. 5A illustrates a method for reading data 1, and FIG. 5B illustrates a method for reading data 0. In reading of data, the potential of the word line WL2 for reading is changed to turn on the transistor 116 functioning as a selection transistor for reading, so that an output from a readout circuit 117 is determined in accordance with the voltage of the bit line BL2 for reading. Note that the bit line BL1 for writing and the word line WL1 for writing are each set at a ground potential in reading, and the transistors 112 and 115 are off.

[0059]

In the case of reading data 1, a second potential is applied to the word line WL2 for reading which belongs to a column through which data is read, and the transistor 116 is turned on as illustrated in FIG. 5A. A third potential which is a negative potential is also applied to word lines WL2 for reading which belong to columns through which data is not read. The second potential is a potential at which the transistor 116 is turned on. The second potential is set as a potential which is higher than the threshold voltage of the transistor 116, and is 2 V here. In the case of data 1, the transistor 113 is turned on; therefore, the output from the readout circuit 117 is determined by comparison between resistance of a resistor (referred to as R1) included in the readout circuit 117 and the sum of on-resistance of the transistor 113 and on-resistance of the transistor 116. Here, when the resistance of the resistor R1 in the readout circuit is higher than the sum of the on-resistance of the transistor 113 and the on-resistance of the transistor 116, the potential of a node C of the bit line BL2 for reading is approximately 0 V. The potential of the node C is inverted by an inverter 118 included in the readout circuit 117 to be output as data 1.

[0060]

In the case of reading data 0, the second potential is applied to the word line WL2 for reading, and the transistor 116 is turned on as illustrated in FIG. 5B. In the case of data 0, the transistor 113 is off; therefore, the output from the readout circuit 117 is determined by comparison between the resistance of the resistor R1 included in the readout circuit 117 and the sum of off-resistance of the transistor 113 and on-resistance of the transistor 116. Here, when the resistance of the resistor R1 included in the

readout circuit 117 is lower than the sum of the off-resistance of the transistor 113 and the on-resistance of the transistor 116, the potential of the node C of the bit line BL2 for reading is set to approximately 2 V by the readout circuit 117. The potential is inverted by the inverter 118 included in the readout circuit 117 to be output as data 0.

[0061]

Note that in memory cells which belong to columns through which data is not read, the third potential which is a negative potential is applied to word lines WL2 for reading. The third potential is a potential at which the transistor 116 is turned off. The third potential is a negative potential which is lower than the threshold voltage of the transistor 116, and is –2 V here. The transistor 116 is turned off. Therefore, there is no possibility of reading data in the memory cells in which reading of data is not selected.

[0062]

Next, writing and reading of data in the NOR memory cell 130 illustrated in FIG. 2B according to Embodiment 1 will be described with reference to drawings.

[0063]

First, writing of data in the NOR memory cell 130 illustrated in FIG. 2B will be described with reference to FIG. 6.

[0064]

First, the first potential is applied to the bit line BL1 for writing and the word line WL1 for writing which belong to the memory cell 130 in which data is written, and the word line WL2 for reading is set at a ground potential. The first potential is a potential at which the transistors 133 and 135 are turned on. The first potential is a potential higher than the threshold voltage of each of the transistors 133 and 135, and is 2 V here.

[0065]

When the potential of the word line WL1 for writing and the bit line BL1 for writing is the first potential, the transistor 135 and the diode-connected transistor 132 are turned on, so that electric charge is charged in the node A, that is, the capacitor 134 and the gate of the transistor 133, and the potential increases to approximately the same as the potential of the bit line BL1 for writing; accordingly, the transistor 133 is turned on. Through the above steps, data 1 can be written.

[0066]

After the writing of data is finished, the potential of the bit line BL1 for writing and the potential of the word line WL1 for writing are 0 V. Accordingly, although the transistor 135 functioning as a selection transistor for writing and the diode-connected transistor 132 are off, the off-state current of the transistor 132 which is formed using an oxide semiconductor is very low; therefore, the voltage of the node A is held for a long period of time. Consequently, the memory element 131 functions as a write-once memory.

[0067]

Next, reading of data in the memory cell 130 illustrated in FIG. 2B will be described with reference to FIGS. 7A and 7B. FIG. 7A illustrates a method for reading data 1, and FIG. 7B illustrates a method for reading data 0. In reading of data, the potential of the word line WL2 for reading is changed, and data is read in accordance with the voltage of the bit line BL2 for reading.

[0068]

In the case of reading data 1, the word line WL2 for reading which belongs to a column through which data is read is set at a ground potential, and the other word lines WL2 for reading are set at the third potential which is a negative potential as illustrated in FIG. 7A.

[0069]

When data 1 is stored in the memory cell 130 in which data is read, that is, the first voltage is charged in the capacitor 134 of the memory cell 130, the transistor 133 is turned on, and the potential of the node C of the bit line BL2 for reading is approximately 0 V. The potential of the node C is inverted by the inverter included in the readout circuit 117 to be output as data 1.

[0070]

In the case of reading data 0, the word line WL2 for reading which belongs to a column through which data is read is set at a ground potential, and the other word lines WL2 for reading are set at the third potential which is a negative potential as illustrated in FIG. 7B.

[0071]

When data 0 is stored in the memory cell 130 in which data is read, that is,

electric charge is not charged in the capacitor 134 of the memory cell 130, the transistor 133 is turned off, and the potential of the node C of the bit line BL2 for reading is set to approximately 2 V by the readout circuit 117. The potential is inverted by the inverter included in the readout circuit 117 to be output as data 0.

[0072]

Note that the third potential which is a negative potential is applied to the word lines WL2 for reading in the memory cells which belong to the columns through which data is not read. The potential of the capacitor 134 of the memory cell is a value in which the third potential is added to the potential stored in the node A. Because the third potential is a negative potential, the potential of the capacitor 134 of the memory cell decreases, and the transistor 133 is turned off regardless of data written to the memory cell. Therefore, there is no possibility of reading data in the memory cell which is not selected for reading.

[0073]

Next, writing and reading of data in the NAND memory cell 120 illustrated in FIG. 3 according to Embodiment 1 will be described with reference to drawings.

[0074]

The writing of data in the NAND memory cell 120 illustrated in FIG. 3 will be described with reference to FIG. 8.

[0075]

First, the first potential is applied to the bit line BL and the word line WL which belong to the memory cell 120 in which data is written. The first potential is a potential at which the transistors 123 and 125 are turned on. The second electrode of the capacitor 124, which is not connected to the transistors 123 and 125, is a ground potential.

[0076]

When the potential of the word line WL for writing is the first potential, the transistor 125 and the diode-connected transistor 122 are turned on, so that the potential of the node A, that is, the potential of the capacitor 124 and the gate of the transistor 123, increases to approximately the same as the potential of the bit line BL for writing; accordingly, the transistor 123 is turned on. Through the above steps, data 1 can be written.

[0077]

After the writing of data is finished, the potential of the bit line BL for writing is 0 V. Accordingly, although the transistor 125 functioning as a selection transistor for writing and the diode-connected transistor 122 are off, the off-state current of the transistor 122 which is formed using an oxide semiconductor is very low; therefore, the potential of the node A is held for a long period of time. Consequently, the memory element 121 functions as a write-once memory.

[0078]

Next, reading of data in the memory cell 120 illustrated in FIG. 3 will be described with reference to FIGS. 9A and 9B. FIG. 9A illustrates a method for reading data 1, and FIG. 9B illustrates a method for reading data 0. Reading of data is performed in such a manner that voltages are applied to all the second electrodes of the capacitor 124, which are electrodes not connected to the transistor 123 in all the memory cells connected to a given bit line, that is, in the capacitors 124 included in the memory cells 120 which are included in a region 129. A ground potential is applied to the second electrode of the capacitor 124 of the memory cell which belongs to a line and in which data is read, and a fourth potential is applied to the second electrode of the capacitor 124 of the other of the memory cells included in the region 129, and an output from the readout circuit 117 is determined in accordance with the voltage of the bit line BL for reading. The fourth potential is a potential which is higher than the threshold voltage of the transistor 123, and the fourth potential is 2 V here.

[0079]

In the case of reading data 1, electric charge is stored in the capacitor 124 of the memory cell in which data is read and the first potential is applied to the first electrode of the capacitor 124 as illustrated in FIG. 9A. Therefore, when the second electrode of the capacitor 124 is a ground potential, the transistor 123 is turned on. In contrast, when the fourth potential is applied to the second electrode of the capacitor 124 of the memory cell in which data is not read and which is in the region 129, the potential of the first electrode of the capacitor 124 increases, whereby the transistor 123 is turned on. As a result, all the transistors 123 connected to the data line DL are on, and the potential of the node C of the data line DL is 0 V. The potential of the node C is inverted by the inverter included in the readout circuit 117 to be output as data 1.

[0080]

In the case of reading data 0, the first electrode of the capacitor 124 of the memory cell 120 in which data is read is 0 V as illustrated in FIG. 9B. Therefore, the transistor 123 of the memory cell in which data is read is off. On the other hand, when the fourth potential is applied to the second electrode of the capacitors 124 of the memory cells in which data is not read in the region 129, the potential of the first electrode of the capacitor 124 increases, whereby the transistor 123 is turned on. As a result, the potential of the node C of the data line DL is set to approximately 2 V by the readout circuit 117.

[0081]

According to this embodiment, a semiconductor memory device in which high voltage is not needed in writing, a defect is less likely to occur, the writing time is short, and data cannot be rewritten can be provided.

[0082]

(Embodiment 3)

In this embodiment, one embodiment of the semiconductor memory device described in Embodiments 1 and 2 will be described with reference to drawings.

[0083]

FIG. 10A is an example of a semiconductor memory device including the memory cell array described in Embodiment 1. A semiconductor memory device 300 includes a memory cell array 301, a column decoder 302, a row decoder 303, and an interface circuit 304. The memory cell array 301 includes a plurality of memory cells 305 arranged in matrix.

[0084]

The interface circuit 304 generates signals for driving the column decoder 302 and the row decoder 303 from external signals and outputs data which is read from the memory cell 305 to the outside.

[0085]

The column decoder 302 receives a signal for driving the memory cell 305 from the interface circuit 304 and generates a signal for writing or reading which is to be transmitted to a bit line. The row decoder 303 receives a signal for driving the memory cell 305 from the interface circuit 304 and generates a signal for writing or

reading which is to be transmitted to a word line. With the signal which is to be output to the bit line from the column decoder 302 and the signal which is to be output to the word line from the row decoder 303, the memory cell which performs access in the memory cell array 301 is uniquely determined.

[0086]

Further, as illustrated in FIG. 10B, it is possible to form a semiconductor memory device including a memory cell array in which the write-once memory described in Embodiment 1 and Embodiment 2 and a rewritable memory are combined. A semiconductor memory device 310 illustrated in FIG. 10B includes a first memory cell array 311, a second memory cell array 312, the column decoder 302, the row decoder 303, and the interface circuit 304. In the first memory cell array 311, memory cells 313 each having the write-once memory described in Embodiment 1 and Embodiment 2 are arranged in matrix. In the second memory cell array 312, memory cells 314 each having a rewritable memory element are arranged in matrix.

[0087]

The rewritable memory element can be formed by the same process as that of the write-once memory described in Embodiment 1 and Embodiment 2. The structure of the rewritable memory element is described with reference to FIG. 11A and FIG. 11B.

[0088]

FIG. 11A is a diagram illustrating a memory cell having a rewritable memory element of NOR type and a memory cell array. A memory cell 400 includes a memory element 401; a transistor 402 whose gate is connected to the word line WL1 for writing, whose first electrode is connected to the memory element 401, and whose second electrode is connected to the bit line BL1 for writing; and a transistor 406 whose gate is connected to the word line WL2 for reading, whose first electrode is connected to the bit line BL2 for reading, and whose second electrode is connected to the memory element 401. The transistor 406 functions as a selection transistor for reading.

[0089]

The memory element 401 includes a transistor 403 and a capacitor 404. A gate of the transistor 403 is connected to a first electrode of the capacitor 404 and the first electrode of the transistor 402. In addition, a first electrode of the transistor 403 is connected to the second electrode of the transistor 406, and a second electrode of the

transistor 403 has a fixed potential. A second electrode of the capacitor 404 also has a fixed potential.

[0090]

The transistor 402 is formed using an oxide semiconductor in a manner similar to that of the transistor 102 described in Embodiment 1. The transistors 403 and 406 can be formed in a manner similar to that of the transistor 103 described in Embodiment 1.

[0091]

The writing of data in the NOR memory cell 400 illustrated in FIG. 11A is described with reference to FIGS. 12A and 12B. FIG. 12A illustrates a method for writing data 1, and FIG. 12B illustrates a method for writing data 0.

[0092]

In the case of writing of data 1 as illustrated in FIG. 12A, the first potential is applied to the bit line BL1 for writing and the word line WL1 for writing which are connected to the memory cell 400 in which data is written, and the word line WL2 for reading has a ground potential. The first potential is a potential at which the transistors 402 and 403 are turned on and which is higher than the threshold voltage of each of the transistors 402 and 403, and is 2 V here.

[0093]

When the potential of the word line WL1 for writing is the first potential, the transistor 402 is turned on, and the potential of the node A, that is, the potential of the capacitor 404 and the gate of the transistor 403 increases to a potential which is approximately the same as the potential of the bit line BL1 for writing, whereby the transistor 403 is turned on. By the above steps, data 1 can be written.

[0094]

In the case of writing of data 0 as illustrated in FIG. 12B, the bit line BL1 for writing which is connected to the memory cell 400 in which data is written has a ground potential, the first potential is applied to the word line WL1 for writing, and the word line WL2 for reading has a ground potential. The first potential is a potential at which the transistor 402 is turned on and which is higher than the threshold voltage of the transistor 402, and is 2 V here.

[0095]

When the potential of the word line WL1 for writing is the first potential, the transistor 402 is turned on, and the potential of the node A, that is, the potential of the capacitor 404 and the potential of the gate of the transistor 403 decreases to a potential of the bit line BL1 for writing which is a ground potential. Thus, the transistor 403 is turned off, and data 0 can be written. Note that to prevent unintended reading of data, the word line WL2 for reading is made to have a ground potential and the transistor 406 is turned off in a writing period.

[0096]

Next, reading of data in the memory cell 400 illustrated in FIG. 11A is described with reference to FIGS. 13A and 13B. FIG. 13A illustrates a method for reading data 1, and FIG. 13B illustrates a method for reading data 0. In reading of data, the potential of the word line WL2 for reading is changed, the transistor 406 functioning as a selection transistor for reading is turned on, and an output from the readout circuit 117 is determined in accordance with the voltage of the bit line BL2 for reading.

[0097]

In the case of reading data 1 as illustrated in FIG. 13A, the second potential is applied to the word line WL2 for reading which belongs to a line through which data is read, and the transistor 406 is turned on. In the case of data 1, the transistor 403 is on; therefore, the node C of the bit line BL2 for reading has a ground potential in a manner similar to that of the reading method of the write-once memory element of NOR type illustrated in FIG. 2A according to Embodiment 2. The potential of the node C is inverted by the inverter included in the readout circuit 117 and is output as data 1.

[0098]

In the case of reading data 0 as illustrated in FIG. 13B, the second potential is applied to the word line WL2 for reading, and the transistor 406 is turned on. In the case of data 0, the transistor 403 is off; therefore, the bit line BL2 for reading is set to approximately 2 V by the readout circuit 117. The potential is inverted by the inverter included in the readout circuit 117 and is output as data 0.

[0099]

Note that in memory cells in which data is not read of columns, the third potential which is a negative potential is applied to the word line WL2 for reading. The third potential is a potential at which the transistor 406 is turned off and a negative

potential that is lower than the threshold voltage of the transistor 406, and is −2 V here. The transistor 406 is turned off. Therefore, there is no possibility of reading data in the memory cell in which reading of data is not selected.

[0100]

FIG. 11B is a diagram illustrating a memory cell including a rewritable memory element of NOR type which is different from the memory cell in FIG. 11A. The memory cell illustrated in FIG. 11B has a structure including a transistor 405 between the transistor 402 and the bit line BL1 for writing which are illustrated in FIG. 11A. In this structure, a connection of the gate of the transistor 112 described in Embodiment 1 is changed, and the gate is merely connected to the word line WL1 for writing. In other words, with a slight variation in wirings, the write-once memory can be replaced with the rewritable memory or the rewritable memory can be replaced with the write-once memory. Since a method for writing data and a method for reading data are in common with FIG. 11A, these are omitted.

[0101]

Note that in this embodiment, the write-once memory and the rewritable memory element are of NOR type; however, a NAND type can be used as appropriate.

[0102]

In this manner, the write-once memory and the rewritable memory can be provided on the same semiconductor memory device. The rewritable memory can be formed by the same process as that of the write-once memory described in Embodiment 1 and Embodiment 2, and the write-once memory can be used as a write-once memory and the rewritable memory can be used as a rewritable memory without depending on the operation by a logic signal. Therefore, it is possible to provide a semiconductor memory device in which rewriting of data due to malfunction of a logic circuit does not occur in principle.

[0103]

(Embodiment 4)

In this embodiment, a structure of the semiconductor memory device described in Embodiments 1 to 3 and a manufacturing method thereof are described with reference to FIG. 14, FIG. 15, and FIGS. 16A to 16E.

[0104]

In this embodiment, the structure of the semiconductor memory device described in Embodiment 1 is described using a top view and a cross-sectional view, and the structure can be applied to Embodiment 2 and Embodiment 3, as appropriate.

[0105]

FIG. 14 is one embodiment of a top view of the memory cell 110 in the semiconductor memory device described in Embodiment 1, and a cross-sectional view taken along lines A-B, C-D, and E-F of FIG. 14 is illustrated in FIG. 15.

[0106]

A transistor 502 illustrated in FIG. 14 corresponds to the transistor 113 illustrated in FIG. 2A, a transistor 503 corresponds to the transistor 116 illustrated in FIG. 2A, a diode-connected transistor 505 corresponds to the diode-connected transistor 112 illustrated in FIG. 2A, and a transistor 506 corresponds to the transistor 115 illustrated in FIG. 2A. In addition, a capacitor 504 corresponds to the capacitor 114 illustrated in FIG. 2A.

[0107]

Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. Further, the technical nature of the present invention disclosed herein is to form a channel region of the diode-connected transistor 505 using an oxide semiconductor layer; therefore, a specific structure of a semiconductor memory device is not necessarily limited to the structure described herein.

[0108]

As illustrated in FIG. 15, the transistor 502 and the capacitor 504 are provided over an insulating layer 510 and an insulating layer 512 which are stacked over a substrate 508; the transistor 505 is provided over the insulating layer 510, the insulating layer 512, an insulating layer 536, an insulating layer 538, and an insulating layer 540 which are stacked.

[0109]

The semiconductor memory device described in this embodiment includes the transistor 502, the transistor 503 (not illustrated), the capacitor 504, and the transistor 506 (not illustrated) in the lower part, and the diode-connected transistor 505 in the upper part. Note that the capacitor 504 may be provided in the upper part instead of in

the lower part but.

[0110]

The transistor 502 includes a semiconductor layer 519 formed over the insulating layer 512, a gate insulating layer 522 provided over the semiconductor layer 519, a gate electrode 526 provided over the gate insulating layer 522, and wirings 534a and 534b which are electrically connected to the semiconductor layer 519. The semiconductor layer 519 is formed with a channel region 514, and low-concentration impurity regions 516 and high-concentration impurity regions 518 (these are also collectively referred to simply as impurity regions) which are provided so as to sandwich the channel region 514.

[0111]

Here, a sidewall insulating layer 530 is provided on a side surface of the gate electrode 526. Further, the sidewall insulating layer 530 overlaps with the low-concentration impurity regions 516.

[0112]

The capacitor 504 includes a semiconductor layer 520 which is formed over the insulating layer 512 and with a high-concentration impurity region, a gate insulating layer 524 provided over the semiconductor layer 520, a capacitor electrode 528 provided over the gate insulating layer 524, a wiring 534c electrically connected to the semiconductor layer 520, and the wiring 534b connected to the capacitor electrode 528. Here, a sidewall insulating layer 532 is provided on a side surface of the capacitor electrode 528.

[0113]

The insulating layer 536, the insulating layer 538, and the insulating layer 540 are provided so as to cover the transistor 502 and the capacitor 504.

[0114]

The diode-connected transistor 505 includes an oxide semiconductor layer 542 electrically connected to the wiring 534c and a wiring 534d which are provided over the insulating layer 540; a gate insulating layer 544 covering the wiring 534c, the wiring 534d, and the oxide semiconductor layer 542; and a gate electrode 546a which is provided over the gate insulating layer 544 and which overlaps with the oxide semiconductor layer 542. Further, the gate electrode 546a seals an opening formed in

the gate insulating layer 544, and the gate electrode 546a is electrically connected to the wiring 534d to be diode-connected.

[0115]

An insulating layer 552 and an insulating layer 554 are provided so as to cover the transistor 505.

[0116]

Further, as illustrated in FIG. 14, a wiring 546b functioning as a ground wiring and the wiring 546b is electrically connected to the wiring 534a of the transistor 502 through an opening formed in the gate insulating layer 544. The capacitor electrode 528 is electrically connected to the wiring 534a; therefore, the capacitor electrode 528 of the capacitor 504 is electrically connected to the wiring 546b.

[0117]

The wiring 534a is electrically connected to the high-concentration impurity region 518 and the capacitor electrode 528 of the capacitor 504 through openings formed in the insulating layer 536, the insulating layer 538, and the insulating layer 540. The wiring 534b is electrically connected to the high-concentration impurity region 518 through an opening formed in the insulating layer 536, the insulating layer 538, and the insulating layer 540. The wiring 534c is electrically connected to the semiconductor layer 520 which is a high-concentration impurity semiconductor and the gate electrode 526 (see FIG. 14) of the transistor 502 through openings formed in the insulating layer 536, the insulating layer 538, and the insulating layer 540.

[0118]

In addition, as illustrated in FIG. 14, the wiring 534d is electrically connected to a high-concentration impurity region of the transistor 506 through an opening formed in the insulating layer 536, the insulating layer 538, and the insulating layer 540, and is electrically connected to the oxide semiconductor layer 542 of the transistor 505. A wiring 534e is electrically connected to the high-concentration impurity region of the transistor 506 through an opening formed in the insulating layer 536, the insulating layer 538, and the insulating layer 540. A wiring 534f is electrically connected to a high-concentration impurity region of the transistor 503 through an opening formed in the insulating layer 536, the insulating layer 538, and the insulating layer 540.

[0119]

It is necessary that the substrate 508 have at least heat resistance high enough to withstand heat treatment performed later. When a glass substrate is used as the substrate 508, a glass substrate whose strain point is higher than or equal to 730 °C is preferably used. As the glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. Note that a glass substrate containing BaO and B_2O_3 so that the amount of BaO is larger than that of B_2O_3 is preferably used.

[0120]

Instead of the glass substrate, a substrate formed of an insulator, such as a ceramic substrate, a quartz substrate, or a sapphire substrate can be used. Alternatively, crystallized glass or the like may be used. Further alternatively, a semiconductor substrate, such as a silicon wafer, whose surface is provided with an insulating layer, or a conductive substrate formed of a metal material, whose surface is provided with an insulating layer can be used. Further alternatively, a plastic substrate can be used. Note that in the case where a plastic substrate is used for the substrate 508, an adhesive agent may be provided between the substrate 508 and the insulating layer 510.

[0121]

The insulating layer 510 is preferably formed using a nitride insulating layer, and the insulating layer 512 is preferably formed using an oxide insulating layer. As the nitride insulating layer, there are a silicon nitride layer, a silicon nitride oxide layer, an aluminum nitride layer, and the like. As the oxide insulating layer, there are a silicon oxide layer, a silicon oxynitride layer, an aluminum oxide layer, and the like.

[0122]

The semiconductor layer 519 of the transistor 502 and the semiconductor layer 520 of the capacitor 504, which is a high-concentration impurity semiconductor, can be formed using an amorphous silicon layer, a microcrystalline silicon layer, a polycrystalline silicon layer, or a single crystal silicon layer. Note that as a transistor in which a single crystal silicon layer is used for a channel region, in addition to a transistor in which a single crystal semiconductor substrate is used for a channel region, a transistor formed using a so-called silicon-on-insulator (SOI) substrate in which a single crystal silicon layer used for a channel region is formed on an insulating region can be employed. Alternatively, the semiconductor layer 519 of the transistor 502 may

be formed using an oxide semiconductor layer which is similar to an oxide semiconductor layer in the diode-connected transistor 505 to be described.

[0123]

The gate insulating layer 522 and the gate insulating layer 524 can be formed in a single layer or a stacked layer using a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, or an aluminum oxide layer.

[0124]

Alternatively, the gate insulating layer 522 and the gate insulating layer 524 may be formed using a high-k material such as hafnium silicate ($HfSiO_x$), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$), hafnium aluminate to which nitrogen is added ($HfAl_xO_yN_z$), hafnium oxide, or yttrium oxide, whereby gate leakage current can be reduced. Further alternatively, a stacked structure in which a high-k material and one or more of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, and an aluminum oxide layer are stacked can be used. The thickness of each of the gate insulating layer 522 and the gate insulating layer 524 can be greater than or equal to 10 nm and less than or equal to 300 nm.

[0125]

The gate electrode 526 and the capacitor electrode 528 can be formed using a metal element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy containing any of these metal elements as a component; an alloy containing these metal elements in combination; or the like. Further, one or more metal elements selected from manganese, magnesium, zirconium, and beryllium may be used. Further, each of the gate electrode 526 and the capacitor electrode 528 may have a single-layer structure or a stacked structure of two or more layers. For example, there are a single-layer structure of an aluminum layer containing silicon; a two-layer structure in which a titanium layer is stacked over an aluminum layer; a two-layer structure in which a titanium layer is stacked over a titanium nitride layer; a two-layer structure in which a tungsten layer is stacked over a titanium nitride layer; a two-layer structure in which a tungsten layer is stacked over a tantalum nitride layer; and a three-layer structure in which a titanium layer, an aluminum layer, and a titanium layer are stacked in that order. Alternatively, a layer, an alloy layer, or a nitride layer which contains aluminum and one or more elements selected from titanium,

tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used.

[0126]

Alternatively, the gate electrode 526 and the capacitor electrode 528 can be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. The gate electrode 526 and the capacitor electrode 528 can have a stacked structure having a layer containing the above light-transmitting conductive material and a layer containing the above metal element.

[0127]

The sidewall insulating layer 530 and the sidewall insulating layer 532 can be formed using a material similar to that of the gate insulating layer 522 and the gate insulating layer 524. Note that a sidewall insulating layer is not formed in some cases for integration of the transistor and the capacitor.

[0128]

The insulating layer 536 and the insulating layer 540 can be formed in a manner similar to that of the gate insulating layer 522 and the gate insulating layer 524. The insulating layer 538 can be formed using an organic resin layer. Examples of the organic resin layer include acrylic, epoxy, polyimide, polyamide, polyvinylphenol, and benzocyclobutene. Alternatively, a siloxane polymer can be used.

[0129]

The wirings 534a to 534f can be formed using a metal element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy containing any of these metal elements as a component; an alloy containing these metal elements in combination; or the like. Further, one or more metal elements selected from manganese, magnesium, zirconium, and beryllium may be used. Further, each of the wirings 534a to 534f may have a single-layer structure or a stacked structure of two or more layers. For example, there are a single-layer structure of an aluminum layer containing silicon; a two-layer structure in which a titanium layer is stacked over an aluminum layer; a two-layer structure in which a titanium layer is stacked over a titanium nitride layer; a two-layer structure in which a tungsten layer is stacked over a

titanium nitride layer; a two-layer structure in which a tungsten layer is stacked over a tantalum nitride layer; and a three-layer structure in which a titanium layer, an aluminum layer, and a titanium layer are stacked in that order. Alternatively, a layer, an alloy layer, or a nitride layer which contains aluminum and one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used.

[0130]

Alternatively, the wirings 534a to 534f can be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible to have a stacked structure having a layer containing the above light-transmitting conductive material and a layer containing the above metal element.

[0131]

Note that the transistor 505 and the transistor 506 can each have a structure which is similar to the structure of the transistor 502.

[0132]

As the oxide semiconductor layer 542, an oxide semiconductor layer using any of the followings can be used: a four-component metal oxide such as an In-Sn-Ga-Zn-O-based metal oxide; a three-component metal oxide such as an In-Ga-Zn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, or a Sn-Al-Zn-O-based metal oxide; or a two-component metal oxide such as an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, or an In-Mg-O-based metal oxide. Here, an *n*-component metal oxide includes an oxide of *n* kinds of metals. Note that the oxide semiconductor may contain, as an impurity, an element other than the metal oxide that is the main component at less than or equal to 1 %, preferably at less than or equal to 0.1 %.

[0133]

Further, the oxide semiconductor layer 542 may be formed using a

three-component metal oxide, and a metal oxide represented by $InM_XZn_YO_Z$ (Y = 0.5 to 5) may be used. Here, M represents one or more elements selected from the elements of Group 13 such as gallium (Ga), aluminum (Al), and boron (B). Note that the contents of In, M, Zn, and O can be set freely, and the case where the M content is zero (that is, X = 0) is included. On the other hand, the contents of In and Zn are not zero. In other words, the above-described expression includes In-Ga-Zn-O-based metal oxide, In-Zn-O-based metal oxide, and the like.

[0134]

In addition, the energy gap of the metal oxide which forms the oxide semiconductor layer 542 is 2 eV or more, preferably 2.5 eV or more, more preferably 3 eV or more.

[0135]

For the oxide semiconductor layer 542, an oxide semiconductor with an amorphous structure, a microcrystalline structure, a polycrystalline structure, or a single crystal structure can be used as appropriate. In addition, an oxide semiconductor having a crystal in which the c-axis is approximately parallel to a direction which is perpendicular to a surface of the oxide semiconductor can be used.

[0136]

The oxide semiconductor layer 542 is formed using an i-type or substantially i-type oxide semiconductor layer. The carrier density of the i-type or substantially i-type oxide semiconductor layer is less than 5×10^{14} /cm^3, preferably less than 1×10^{12} /cm^3, more preferably less than or equal to 1×10^{11} /cm^3. In addition, it is preferable that hydrogen or oxygen deficiency serving as a donor be little and the hydrogen concentration be less than or equal to 1×10^{16} /cm^3. Note that the carrier density can be obtained by the Hall effect measurement. Lower carrier density can be obtained from the measurement results of capacitance-voltage (CV) measurement. The hydrogen concentration in the oxide semiconductor layer can be measured by secondary ion mass spectrometry (SIMS).

[0137]

The i-type or substantially i-type oxide semiconductor layer 542 is used for a channel region of the transistor 505, and the off-state current of the transistor 505 can be

less than or equal to 1×10^{-19} A/μm, further less than or equal to 1×10^{-20} A/μm. The i-type or substantially i-type oxide semiconductor layer has a wide band gap and requires a large amount of thermal energy for electronic excitation; therefore, direct recombination and indirect recombination are less likely to occur. Therefore, the number of holes which are minority carriers is substantially zero in a state where a negative potential is applied to a gate electrode (i.e., in an off state); accordingly, direct recombination and indirect recombination are less likely to occur, and the amount of current is very small. As a result, a circuit can be designed with the oxide semiconductor layer that can be considered as an insulator in a state where the transistor is in a non-conducting state (also referred to as an OFF state). On the other hand, when the transistor is in a conducting state, the current supply capability of the i-type or substantially i-type oxide semiconductor layer is expected to be higher than the current supply capability of a semiconductor layer formed of amorphous silicon. Therefore, the transistor 505 serves as a normally-off transistor with very low leakage current in an off state, and has excellent switching characteristics.

[0138]

For the gate insulating layer 544, a material used for the gate insulating layer 522 and the gate insulating layer 524 can be used as appropriate. Note that in the case where the gate insulating layer 544 has a stacked structure, a layer on a side which is in contact with the oxide semiconductor layer 542 is formed using an oxide insulating layer, whereby oxygen can be supplied to the oxygen deficiency included in the oxide semiconductor layer 542, and the oxide semiconductor layer 542 can be made to be an i-type or substantially i-type oxide semiconductor layer.

[0139]

The insulating layer 552 and the insulating layer 554 can be formed in a manner similar to that of the insulating layer 536, the insulating layer 538, or the insulating layer 540.

[0140]

In this embodiment, a channel region of the diode-connected transistor 505 is formed using an i-type or substantially i-type oxide semiconductor layer; thus, off-state current can be extremely reduced. Therefore, voltage applied to the capacitor 504 can be held for a long time.

[0141]

Next, a manufacturing process of the transistor 505 in the semiconductor memory device illustrated in FIG. 15 is described with reference to FIGS. 16A to 16E. Note that a known manufacturing process of a transistor may be employed as appropriate for each manufacturing process of the transistor 502, the transistor 503, and the transistor 506.

[0142]

As illustrated in FIG. 16A, the wiring 534c and the wiring 534d which function as a source electrode and a drain electrode of the transistor 505 are formed over the insulating layer 540.

[0143]

The insulating layer 540 can be formed by a sputtering method, a CVD method, a printing method, a coating method, or the like. Alternatively, the dense high-quality insulating layer 540 having high withstand voltage can be formed by high-density plasma-enhanced CVD using microwaves (e.g., a frequency of 2.45 GHz). A close contact between an oxide semiconductor layer and the high-quality gate insulating layer 540 can reduce interface states and produce desirable interface characteristics. In addition, since the insulating layer 540 formed by the high-density plasma-enhanced CVD can have a uniform thickness, the insulating layer 540 has excellent step coverage. Further, the thickness of the insulating layer 540 formed using the high-density plasma-enhanced CVD can be controlled precisely. Note that the i-type or substantially i-type oxide semiconductor layer is extremely sensitive to an interface state or interface charge; therefore, formation of the insulating layer 540 by the high density plasma-enhanced CVD using microwaves can reduce interface states and produce desirable interface characteristics.

[0144]

Note that the substrate 508 is heated when the insulating layer 540 is formed, whereby the amount of hydrogen, water, a hydroxyl group, hydride, or the like included in the insulating layer 540 can be reduced.

[0145]

Further, in the case where the insulating layer 540 is formed by a sputtering method, the insulating layer 540 is preferably formed while hydrogen, water, a hydroxyl

group, hydride, or the like remaining in a treatment chamber is removed in order to reduce the amount of hydrogen, water, a hydroxyl group, hydride, or the like included in the insulating layer 540. It is preferable to use an entrapment vacuum pump in order to remove hydrogen, water, a hydroxyl group, hydride, or the like remaining in the treatment chamber. Typical examples of entrapment vacuum pumps are a cryopump, an ion pump, and a titanium sublimation pump. Alternatively, a turbo pump provided with a cold trap can be used as the evacuation unit.

[0146]

The purity of the sputtering gas used in forming the insulating layer 540 is preferably 6N (99.9999 %) or higher, more preferably 7N (99.99999 %) or higher (that is, the concentration of the impurities is 1 ppm or lower, preferably 0.1 ppm or lower), whereby the amount of hydrogen, water, a hydroxyl group, hydride, or the like included in the insulating layer 540 can be reduced.

[0147]

The wiring 534c and the wiring 534d are formed using a printing method, an ink-jet method, or the like, whereby the number of steps can be reduced. Alternatively, after a conductive layer is formed over the insulating layer 540 by a sputtering method, a CVD method, an evaporation method, or the like, the conductive layer is etched using, as a mask, a resist formed in a photolithography process, whereby the wiring 534c and the wiring 534d can be formed.

[0148]

Next, as illustrated in FIG. 16B, an oxide semiconductor layer 541 is formed over the insulating layer 540, the wiring 534c, and the wiring 534d. The oxide semiconductor layer 541 can be formed by a printing method, an ink-jet method, or the like. Alternatively, an oxide semiconductor layer is formed over the insulating layer 540 by a sputtering method, a CVD method, a coating method, a pulsed laser evaporation method, or the like, and the oxide semiconductor layer is etched using, as a mask, a resist formed in a photolithography process, whereby the island-shaped oxide semiconductor layer 541 can be formed.

[0149]

The carrier density of the oxide semiconductor layer depends on the hydrogen concentration in a source gas and a target under deposition conditions and the oxygen

concentration therein, a material to be deposited and the composition thereof, heat treatment conditions, and the like. The hydrogen concentration in the oxide semiconductor layer is decreased or the oxygen concentration in the oxide semiconductor layer is increased to reduce oxygen deficiencies, whereby the oxide semiconductor layer is made to be an i-type or substantially i-type oxide semiconductor layer. In this embodiment, since treatment by which the oxide semiconductor layer is made to be i-type or substantially i-type is performed later, the oxide semiconductor layer 541 may be either an i-type oxide semiconductor layer or an n-type oxide semiconductor layer.

[0150]

Note that in the case where the oxide semiconductor layer is formed by a sputtering method, the substrate is heated, whereby impurities such as hydrogen, water, a hydroxyl group, or hydride included in the oxide semiconductor layer can be reduced. Further, in the first heat treatment, crystal growth can be promoted.

[0151]

In addition, in the case where the oxide semiconductor layer is formed by a sputtering method, the relative density of a metal oxide in the metal oxide target is set to greater than or equal to 80 %, preferably greater than or equal to 95 %, more preferably greater than or equal to 99.9 %. Accordingly, the impurity concentration in the oxide semiconductor layer can be reduced, and a transistor which has excellent electrical characteristics or high reliability can be obtained.

[0152]

Further, when preheat treatment is performed before the oxide semiconductor layer is formed, hydrogen, water, a hydroxyl group, hydride, or the like which remains on the inner wall of the sputtering apparatus, on a surface of a target, or inside a target material can be removed. Accordingly, impurities such as hydrogen, water, a hydroxyl group, or hydride included in the oxide semiconductor layer can be reduced.

[0153]

In a manner similar to that of the insulating layer 540, before, during, or after the oxide semiconductor layer is formed, an entrapment vacuum pump is preferably used so as to remove hydrogen, water, a hydroxyl group, hydride, or the like remaining

in the sputtering apparatus. Accordingly, hydrogen, water, a hydroxyl group, hydride, or the like is removed, whereby the concentration of hydrogen, water, a hydroxyl group, hydride, or the like included in the oxide semiconductor layer can be reduced.

[0154]

Next, the first heat treatment is performed, and impurities such as hydrogen, water, a hydroxyl group, or hydride included in the oxide semiconductor layer 541 are removed. That is, at least one of dehydration and dehydrogenation can be performed. Note that in the first heat treatment, an oxygen deficiency is formed in the oxide semiconductor layer 541.

[0155]

The temperature of the first heat treatment is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. The heat treatment apparatus for the first heat treatment is not limited to a particular apparatus, and the apparatus may be provided with a device for heating an object to be processed by heat radiation or heat conduction from a heating element such as a resistance heating element. For example, an electric furnace, or a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used as the heat treatment apparatus. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas.

[0156]

It is preferable that in the first heat treatment, hydrogen, water, a hydroxyl group, hydride, or the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. Alternatively, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is preferably 6N (99.9999 %) or higher, more preferably 7N (99.99999 %) or higher (that is, the concentration of the impurities is 1 ppm or lower, preferably 0.1 ppm or lower).

[0157]

At the time of increasing the temperature in the first heat treatment, an atmosphere in a furnace may be a nitrogen atmosphere, and the atmosphere may be switched to an oxygen atmosphere at the time of performing cooling. By changing the atmosphere to an oxygen atmosphere after the dehydration or dehydrogenation in a nitrogen atmosphere, oxygen can be supplied into the oxide semiconductor layer, so that the hydrogen concentration can be reduced and oxygen can be supplied to the oxygen deficiency formed in the oxide semiconductor layer; accordingly, an i-type or substantially i-type oxide semiconductor layer can be formed.

[0158]

Further, depending on the conditions of the first heat treatment or the material of the oxide semiconductor layer, the oxide semiconductor layer might be crystallized to be an oxide semiconductor layer including crystals. For example, an oxide semiconductor layer including crystals with a crystallinity of 90 % or higher, or 80 % or higher, is formed in some cases.

[0159]

In addition, depending on the conditions of the first heat treatment or the material of the oxide semiconductor layer, the oxide semiconductor layer having a crystal in which the c-axis is approximately parallel to a direction which is perpendicular to a surface is formed in a superficial portion of the amorphous oxide semiconductor layer in some cases.

[0160]

Here, the substrate is introduced into an electric furnace, and heat treatment is performed in an inert gas atmosphere, such as a nitrogen atmosphere or a rare gas atmosphere, at 450 °C for one hour.

[0161]

Next, as illustrated in FIG. 16C, the gate insulating layer 544 is formed.

[0162]

The gate insulating layer 544 can be formed in a manner similar to that of the insulating layer 540. Note that when a silicon oxide layer is formed as the gate insulating layer 544 by a sputtering method, oxygen can be supplied from the silicon oxide layer to the oxygen deficiency which is included in the oxide semiconductor layer

541 and is generated by the first heat treatment, the oxygen deficiency which contributes to the formation of a donor can be reduced, and a structure which satisfies a stoichiometric mixture ratio can be formed. As a result, the i-type or substantially i-type oxide semiconductor layer 542 can be formed. A close contact between the oxide semiconductor layer and the high-quality insulating layer 540 can reduce interface states and produce desirable interface characteristics.

[0163]

Note that the i-type or substantially i-type oxide semiconductor layer is extremely sensitive to an interface state or interface charge; therefore, formation of the insulating layer 540 by the high density plasma-enhanced CVD using microwaves can reduce interface states and produce desirable interface characteristics.

[0164]

Then, second heat treatment (preferably, at a temperature higher than or equal to 200 °C and lower than or equal to 400 °C, for example, at a temperature higher than or equal to 250 °C and lower than or equal to 350 °C) is preferably performed in an inert gas atmosphere or in an oxygen gas atmosphere. The second heat treatment may be performed after a protective insulating layer or a planarization insulating layer is formed over the gate insulating layer 544. With the heat treatment, oxygen can be supplied from the oxide insulating layer of the gate insulating layer 544 to the oxygen deficiency which is included in the oxide semiconductor layer and is generated by the first heat treatment, the oxygen deficiency which contributes to the formation of a donor can be reduced, and a structure which satisfies a stoichiometric mixture ratio can be formed. As a result, the i-type or substantially i-type oxide semiconductor layer 542 can be formed.

[0165]

In this embodiment, the second heat treatment is performed at 250 °C for 1 hour in a nitrogen atmosphere.

[0166]

Next, as illustrated in FIG. 16D, after an opening is formed in the gate insulating layer 544, the gate electrode 546a is formed over the gate insulating layer 544 and the wiring 534d. Through the above steps, a transistor in which the gate electrode

546a and the wiring 534d are diode-connected can be formed. The gate electrode 546a can be formed in a manner similar to that of the wiring 534c and the wiring 534d.

[0167]

Next, as illustrated in FIG. 16E, the insulating layer 552 and the insulating layer 554 are formed over the gate insulating layer 544 and the gate electrode 546a.

[0168]

Further, heat treatment may be performed at a temperature higher than or equal to 100 °C and lower than or equal to 200 °C for more than or equal to 1 hour and less than or equal to 30 hours in the air. With the heat treatment, reliability of the transistor can be improved.

[0169]

Note that in FIGS. 16A to 16E, the oxide semiconductor layer 541 is formed after the wiring 534c and the wiring 534d are formed; however, the wiring 534c and the wiring 534d may be formed after the oxide semiconductor layer 541 is formed over the insulating layer 540.

[0170]

In FIGS. 16A to 16E, a structure may be employed in which the gate electrode 546a is formed over the insulating layer 540, the gate insulating layer 544 is formed over the gate electrode 546a, the oxide semiconductor layer 541 is formed over the gate insulating layer 544, and wirings functioning as a source electrode and a drain electrode are formed over the oxide semiconductor layer 541. In that case, one of the wirings functioning as a source electrode and a drain electrode is electrically connected to the wiring 534c. Further, the other of the wirings functioning as a source electrode and a drain electrode is electrically connected to the gate electrode 546a.

[0171]

Through the above steps, the transistor 505 in which a channel region includes the i-type or substantially i-type oxide semiconductor layer and which has very low off-state current can be formed.

[0172]

(Embodiment 5)

In this embodiment, an embodiment of an RFID tag including the semiconductor memory device described in Embodiments 1 to 4 will be described with

reference to drawings.

[0173]

A circuit illustrated in FIG. 17 is an RFID tag. Radio frequency identification (RFID: non-contact automatic identification technique using radio frequency) has features such as capability of reading stored information without contact, operation without a battery, and superiority in durability and weatherability. The reason why operation is possible without a battery is a radio wave (including an operation instruction or the like) received by an antenna included in the RFID tag is rectified in a circuit, so that power can be generated. In the RFID tag, a memory to which data can be written or rewritten by a user is frequently provided in order to improve its function.

[0174]

An RFID tag 1520 includes an antenna circuit 1521 and a signal processing circuit 1522. The signal processing circuit 1522 includes a rectifier circuit 1523, a power supply circuit 1524, a demodulation circuit 1525, an oscillator circuit 1526, a logic circuit 1527, a memory control circuit 1528, a memory circuit 1529, a logic circuit 1530, an amplifier 1531, and a modulation circuit 1532. The memory circuit 1529 includes the semiconductor memory device of any of the above embodiments.

[0175]

Communication signals received by the antenna circuit 1521 are input into the demodulation circuit 1525. The frequency of the communication signal received, that is, the frequency of a signal transmitted and received between the antenna circuit 1521 and a reader/writer is, for example, 13.56 MHz, 915 MHz, or 2.45 GHz in UHF (ultra high frequency) band, which is determined on the basis of the ISO standards or the like. Needless to say, the frequency of a signal transmitted and received between the antenna circuit 1521 and the reader/writer is not limited to this, and for example, any of the following frequencies can be used: 300 GHz to 3 THz which is a submillimeter wave, 30 GHz to 300 GHz which is a millimeter wave, 3 GHz to 30 GHz which is a microwave, 300 MHz to 3 GHz which is an ultra high frequency, and 30 MHz to 300 MHz which is a very high frequency. Further, a signal transmitted and received between the antenna circuit 1521 and the reader/writer is a signal obtained by modulating a carrier wave. A carrier wave is modulated by analog modulation or digital modulation, and any of amplitude modulation, phase modulation, frequency

modulation, and spread spectrum may be used. Preferably, amplitude modulation or frequency modulation is used.

[0176]

An oscillation signal output from the oscillator circuit 1526 is supplied as a clock signal to the logic circuit 1527. In addition, the carrier wave which has been modulated is demodulated in the demodulation circuit 1525. The demodulated signal is transmitted to the logic circuit 1527 and analyzed. The signal analyzed in the logic circuit 1527 is transmitted to the memory control circuit 1528. The memory control circuit 1528 controls the memory circuit 1529, extracts data stored in the memory circuit 1529, and transmits the data to the logic circuit 1530. The signal sent to the logic circuit 1530 is amplified by the amplifier 1531 after being encoded by the logic circuit 1530. With the signal amplified by the amplifier 1531, the modulation circuit 1532 modulates a carrier wave. By the modulated carrier wave, the reader/writer recognizes a signal from the RFID tag 1520.

[0177]

A carrier wave input to the rectifier circuit 1523 is rectified and input to the power supply circuit 1524. Power supply voltage obtained in this manner is supplied from the power supply circuit 1524 to the demodulation circuit 1525, the oscillator circuit 1526, the logic circuit 1527, the memory control circuit 1528, the memory circuit 1529, the logic circuit 1530, the amplifier 1531, the modulation circuit 1532, and the like.

[0178]

A connection between the signal processing circuit 1522 and the antenna in the antenna circuit 1521 is not specifically limited. For example, the antenna and the signal processing circuit 1522 are connected by wire bonding or bump connection. Alternatively, the signal processing circuit 1522 is formed to have a chip shape and one surface thereof is used as an electrode and attached to the antenna. The signal processing circuit 1522 and the antenna can be attached to each other by the use of an anisotropic conductive film (ACF).

[0179]

The antenna is either stacked over the same substrate as the signal processing circuit 1522, or formed as an external antenna. Needless to say, the antenna is

provided on the above or below of the signal processing circuit.

[0180]

The rectifier circuit 1523 converts AC signals that are induced by carrier waves received by the antenna circuit 1521 into DC signals.

[0181]

The RFID tag 1520 may include a battery 1581 as illustrated in FIG. 18. When power supply voltage output from the rectifier circuit 1523 is not high enough to operate the signal processing circuit 1522, the battery 1581 also supplies power supply voltage to each circuit of the signal processing circuit 1522, such as the demodulation circuit 1525, the oscillator circuit 1526, the logic circuit 1527, the memory control circuit 1528, the memory circuit 1529, the logic circuit 1530, the amplifier 1531, and the modulation circuit 1532.

[0182]

Surplus voltage of the power supply voltage output from the rectifier circuit 1523 may be charged in the battery 1581. When an antenna circuit and a rectifier circuit are provided in the RFID tag in addition to the antenna circuit 1521 and the rectifier circuit 1523, energy stored in the battery 1581 can be obtained from electromagnetic waves and the like that are generated randomly.

[0183]

Electric power is charged in the battery, whereby the RFID tag can be continuously used. As the battery, a battery formed into a sheet form can be used. For example, by using a lithium polymer battery that includes a gel electrolyte, a lithium ion battery, a lithium secondary battery, or the like, a reduction in the size of the battery can be realized. In addition, a nickel-hydrogen battery, a nickel-cadmium battery, a capacitor having high capacitance, or the like can be used as the battery.

[0184]

(Embodiment 6)

In this embodiment, a use example of the RFID tag 1520 described in Embodiment 5 will be described with reference to drawings.

[0185]

The RFID tag 1520 can be employed for a wide range of uses and can be used by being provided for bills, coins, securities, bearer bonds, certificates (driver's licenses,

resident cards, and the like; see FIG. 19A), recording media (DVD software, video tapes, and the like; see FIG. 19B), containers for wrapping objects (wrapping paper, bottles, and the like; see FIG. 19C), vehicles (bicycles and the like; see FIG. 19D), personal belongings (bags, glasses, and the like), foods, plants, animals, human bodies, clothes, daily necessities, or products such as electronic devices (liquid crystal display devices, EL display devices, television units, mobile phones, and the like); tags of each product (see FIGS. 19E and 19F); or the like.

[0186]

The RFID tag 1520 is fixed to a product by being mounted on a printed board, attached to a surface of the product, or embedded in the product. For example, the RFID tag 1520 is incorporated in paper of a book or an organic resin package to be fixed to each object. Since the RFID tag 1520 can be reduced in size, thickness, and weight, it can be fixed to a product without spoiling the design of the product. Further, bills, coins, securities, bearer bonds, documents, or the like can have an identification function by being provided with the RFID tag 1520, and the identification function can be utilized to prevent counterfeiting. Further, when the RFID tag of the present invention is attached to containers for wrapping objects, recording media, personal belongings, foods, clothes, daily necessities, electronic devices, or the like, a system such as an inspection system can be efficiently used. Vehicles can also have higher security against theft or the like by being provided with the RFID tag 1520.

[Example 1]

[0187]

In this example, the data retention time of the memory element described in Embodiments 1 to 3 is verified by circuit simulation, and the results are described.

[0188]

Circuit diagrams for simulation and the results thereof are illustrated in FIGS. 20A to 20C. A circuit illustrated in FIG. 20A is the memory element which is one embodiment of the present invention, and the circuit includes a diode-connected transistor 601, a transistor 602, and a capacitor 603. A circuit for simulation which is equivalent to this circuit is illustrated in FIG. 20B. The circuit illustrated in FIG. 20B includes a resistor 611, a transistor 612, a capacitor 613, a resistor 614, and a resistor 615. The resistor 611 is equivalent to the diode-connected transistor 601 in an off state,

and the resistor 614 shows a gate leakage component of the transistor 612, and the resistor 615 shows a leakage component between electrodes of the capacitor 613.

[0189]

Simulation in which the state just after data is written was assumed and the initial voltage of the node A was 2 V was done. As simulation software, Gateway Version 2.6.12.R produced by Simucad Design automation, Inc. was used. The potential of the node A monotonically decreases over time by the resistor 611 assumed to show the off-state current of the diode-connected transistor 601, the resistor 614 assumed to show the gate leakage component of the transistor 612, and the resistor 615 assumed to show the leakage component between the electrodes of the capacitor 613. The period up until the point when the potential decreases and the off state of the transistor 612 cannot be kept is a period in which data can be held. In this example, a period up until the point when voltage decreases by 10 %, that is, decreases to 1.8 V is defined as a period in which data 1 can be held, that is, retention time of data 1.

[0190]

Under a condition 1 and a condition 2, the resistance value of the resistor 611 was seen as a value of the off-state current of the diode-connected transistor 601 whose channel region was formed using an oxide semiconductor layer. Under a condition 3, the resistance value of the resistor 611 was a value of the off-state current of the diode-connected transistor 601 whose channel region was not formed using an oxide semiconductor layer.

The condition 1: 2×10^{20} Ω (in terms of off-state current, 10^{-20} A);

The condition 2: 2×10^{19} Ω (in terms of off-state current, 10^{-19} A); and

The condition 3: 2×10^{9} Ω (in terms of off-state current, 10^{-9} A).

Each of the resistance value of the resistor 614 and the resistance value of the resistor 615 was assumed to be 10 times as large as that of the resistor 611.

[0191]

FIG. 20C shows the simulation results. FIG. 20C is a graph in which the horizontal axis represents elapsed time and the vertical axis represents the voltage of the node A. The retention time of data 1 under the condition 3 was 176.3 μs, while the retention time of data 1 under the condition 1 was 17.63×10^{6} s (approximately 200

days) and the retention time of data 1 under the condition 2 was 1.763×10^6 s (approximately 20 days). As a result, it is found that, when the channel region of the diode-connected transistor 601 is formed using an oxide semiconductor layer, data 1 can be held for a significantly long period or time.

[Example 2]

[0192]

In this example, results obtained by measuring the off-state current of a transistor in which an i-type or substantially i-type oxide semiconductor layer is used for a channel region will be described.

[0193]

First, a transistor with a channel width *W* of 1 m, which was sufficiently large, was prepared in consideration of the very low off-state current of a transistor in which an i-type or substantially i-type oxide semiconductor layer was used for a channel region, and the off-state current was measured. FIG. 21 shows the results obtained by measuring the off-state current of the transistor with a channel width *W* of 1 m. In FIG. 21, the horizontal axis represents a gate voltage VG and the vertical axis represents a drain current ID. In the case where the drain voltage VD is +1 V or +10 V and the gate voltage VG is within the range of −5 V to −20 V, the off-state current of the transistor was found to be less than or equal to 1×10^{-12} A. Moreover, it is found that the off-state current of the transistor (per unit channel width (1 μm)) is less than or equal to 1 aA/μm (1×10^{-18} A/μm).

[0194]

Next will be described the results obtained by measuring the off-state current of the transistor in which the i-type or substantially i-type oxide semiconductor layer was used more accurately. As described above, it is found that the off-state current of the transistor in which the i-type or substantially i-type oxide semiconductor layer was used for the channel region is less than or equal to 1×10^{-12} A. Here, the results obtained by measuring more accurate off-state current (the value less than or equal to the detection limit of measurement equipment in the above measurement), with the use of an element for characteristic evaluation, will be described.

[0195]

First, the element for characteristic evaluation used for a method for measuring current will be described with reference to FIG. 22.

[0196]

In the element for characteristic evaluation illustrated in FIG. 22, three measurement systems 800 are connected in parallel. The measurement system 800 includes a capacitor 802, a transistor 804, a transistor 805, a transistor 806, and a transistor 808. The transistor in which the i-type or substantially i-type oxide semiconductor layer was used for the channel region was used as each of the transistors 804, 805, and 806.

[0197]

In the measurement system 800, one of a source terminal and a drain terminal of the transistor 804, one of terminals of the capacitor 802, and one of a source terminal and a drain terminal of the transistor 805 are connected to a power source (for supplying V2). The other of the source terminal and the drain terminal of the transistor 804, one of a source terminal and a drain terminal of the transistor 808, the other of the terminals of the capacitor 802, and a gate terminal of the transistor 805 are connected to one another. The other of the source terminal and the drain terminal of the transistor 808, one of a source terminal and a drain terminal of the transistor 806, and a gate terminal of the transistor 806 are connected to a power source (for supplying V1). The other of the source terminal and the drain terminal of the transistor 805 and the other of the source terminal and the drain terminal of the transistor 806 are connected to each other, and the node serves as an output terminal Vout.

[0198]

A potential Vext_b2 for controlling an on state and an off state of the transistor 804 is supplied to a gate terminal of the transistor 804. A potential Vext_b1 for controlling an on state and an off state of the transistor 808 is supplied to a gate terminal of the transistor 808. A potential Vout is output from the output terminal.

[0199]

Next, a method for measuring current with the use of the element for characteristic evaluation will be described.

[0200]

First, an initialization period in which a potential difference is applied to measure the off-state current will be described briefly. In the initialization period, the potential Vext_b1 for turning on the transistor 808 is input to the gate terminal of the transistor 808, and the potential V1 is supplied to the node A that is a node connected to the other of the source terminal and the drain terminal of the transistor 804 (that is, the node connected to one of the source terminal and the drain terminal of the transistor 808, the other of the terminals of the capacitor 802, and the gate terminal of the transistor 805). Here, the potential V1 is set to, for example, high. The transistor 804 is off.

[0201]

After that, the potential Vext_b1 for turning off the transistor 808 is input to the gate terminal of the transistor 808, so that the transistor 808 is turned off. After the transistor 808 is turned off, the potential V1 is set to low. Still, the transistor 804 is off. The potential V2 is the same as the potential V1. Thus, the initialization period is completed. When the initialization period is completed, a potential difference is generated between the node A and one of the source terminal and the drain terminal of the transistor 804. In addition, a potential difference is generated between the node A and the other of the source terminal and the drain terminal of the transistor 808. Accordingly, a small amount of electric charge flows through the transistor 804 and the transistor 808. That is, the off-state current is generated.

[0202]

Next, a measurement period of the off-state current is briefly described. In the measurement period, the potential (that is, V2) of one of the source terminal and the drain terminal of the transistor 804 and the potential (that is, V1) of the other of the source terminal and the drain terminal of the transistor 808 are fixed to be low. On the other hand, the potential of the node A is not fixed (the node A is in a floating state) in the measurement period. Accordingly, electric charge flows through the transistor 804, and the amount of electric charge stored in the node A varies as time passes. The potential of the node A varies depending on the variation in the amount of electric charge stored in the node A. In other words, the output potential Vout of the output terminal also varies.

[0203]

FIG. 23 illustrates details of the relation between potentials in the initialization period in which the potential difference is applied and in the following measurement period (timing chart).

[0204]

In the initialization period, first, the potential Vext_b2 is set to a potential (high potential) at which the transistor 804 is turned on. Thus, the potential of the node A comes to be V2, that is, a low potential (VSS). After that, the potential Vext_b2 is set to a potential (low potential) at which the transistor 804 is turned off, whereby the transistor 804 is turned off. Next, the potential Vext_b1 is set to a potential (high potential) at which the transistor 808 is turned on. Thus, the potential of the node A comes to be V1, that is, a high potential (VDD). After that, the potential Vext_b1 is set to a potential at which the transistor 808 is turned off. Accordingly, the node A is brought into a floating state and the initialization period is completed.

[0205]

In the following measurement period, the potential V1 and the potential V2 are individually set to potentials at which electric charge flow to or from the node A. Here, the potential V1 and the potential V2 are low potentials (VSS). Note that at the timing of measuring the output potential Vout, it is necessary to operate an output circuit; thus, V1 is set to a high potential (VDD) temporarily in some cases. The period in which V1 is a high potential (VDD) is set to be short so that the measurement is not influenced.

[0206]

When the potential difference is generated and the measurement period is started as described above, the amount of electric charge stored in the node A varies as time passes, which changes the potential of the node A. This means that the potential of the gate terminal of the transistor 805 varies; thus, the output potential Vout of the output terminal also varies as time passes.

[0207]

A method for calculating the off-state current on the basis of the obtained output potential Vout is described below.

[0208]

The relation between the potential VA of the node A and the output potential Vout is obtained in advance before the off-state current is calculated. With this, the potential VA of the node A can be obtained using the output potential Vout. In accordance with the above relation, the potential VA of the node A can be expressed as a function of the output potential Vout by the following equation.

[0209]

[formula 1]

$$V_A = F(Vout)$$

[0210]

Electric charge QA of the node A can be expressed by the following equation with the use of the potential VA of the node A, capacitance CA connected to the node A, and a constant (const). Here, the capacitance CA connected to the node A is the sum of the capacitance of the capacitor 802 and other capacitance.

[0211]

[formula 2]

$$Q_A = C_A V_A + const$$

[0212]

Since a current IA of the node A is obtained by differentiating electric charge flowing to the node A (or electric charge flowing from the node A) with respect to time, the current IA of the node A is expressed by the following equation.

[0213]

[formula 3]

$$I_A \equiv \frac{\Delta Q_A}{\Delta t} = \frac{C_A \cdot \Delta F(Vout)}{\Delta t}$$

[0214]

In this manner, the current IA of the node A can be obtained from the capacitance CA connected to the node A and the output potential Vout of the output terminal.

[0215]

In accordance with the above method, it is possible to measure leakage current (off-state current) which flows between a source and a drain of a transistor in an off

state.

[0216]

In this example, the transistor 804, the transistor 805, the transistor 806, and the transistor 808 were fabricated using a highly purified oxide semiconductor with a channel length L of 10 μm and a channel width W of 50 μm. In each of the measurement systems 800 arranged in parallel, capacitance values of capacitors 802a, 802b, and 802c were 100 fF, 1pF, and 3pF, respectively.

[0217]

Note that the measurement according to this example was performed assuming that VDD = 5 V and VSS = 0 V were satisfied. In the measurement period, the potential V1 was basically set to VSS and set to VDD only in a period of 100 msec every 10 to 300 seconds, and Vout was measured. Further, Δt which was used in calculation of current I which flowed through the element was approximately 30000 sec.

[0218]

FIG. 24 shows the relation between elapsed time *Time* and the output potential Vout in the current measurement. According to FIG. 24, the potential varies as time passes.

[0219]

FIG. 25 shows the off-state current at room temperature (25 °C) calculated based on the above current measurement. FIG. 25 shows the relation between a source-drain voltage V and an off-state current I. According to FIG. 25, it is found that the off-state current was approximately 40 zA/μm under the condition that the source-drain voltage was 4 V. In addition, it is found that the off-state current was less than or equal to 10 zA/μm under the condition that the source-drain voltage was 3.1 V. Note that 1 zA represents 10^{-21} A.

[0220]

Further, FIG. 26 shows the off-state current in an environment at a temperature of 85 °C, which was calculated based on the above current measurement. FIG. 26 shows the relation between the source-drain voltage V and the off-state current I in an environment at a temperature of 85 °C. According to FIG. 26, it is found that the

off-state current was less than or equal to 100 zA/μm under the condition that the source-drain voltage was 3.1 V.

[0221]

According to this example, it was confirmed that the off-state current can be sufficiently low in the transistor in which the i-type or substantially i-type oxide semiconductor layer was used for the channel region. In addition, it is found that the off-state current is also sufficiently low in the diode-connected transistors 102, 112, 122, and 132 in each of which the i-type or substantially i-type oxide semiconductor layer is used for the channel region as described in Embodiments 1 to 3.

This application is based on Japanese Patent Application serial no. 2010-019386 filed with the Japan Patent Office on January 29, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor memory device comprising a memory element including a first transistor and a second transistor,

wherein a gate of the first transistor is electrically connected to one of a source and a drain of the first transistor,

wherein the other of the source and the drain of the first transistor is electrically connected to a gate of the second transistor, and

wherein the first transistor includes an oxide semiconductor film.

2. The semiconductor memory device according to claim 1,

wherein the memory element further includes a capacitor, and

wherein a first electrode of the capacitor is electrically connected to the gate of the second transistor.

3. The semiconductor memory device according to claim 2,

wherein a potential of a second electrode of the capacitor is a fixed potential.

4. The semiconductor memory device according to claim 2,

wherein the semiconductor memory device is a NAND type memory.

5. The semiconductor memory device according to claim 1, wherein carrier density of the oxide semiconductor film is less than 5×10^{14} /cm^3.

6. The semiconductor memory device according to claim 1,

wherein the second transistor includes a semiconductor film, and

wherein a material included in the semiconductor film is different from that included in the oxide semiconductor film.

7. The semiconductor memory device according to claim 1, wherein the semiconductor memory device is a write-once memory.

8. A semiconductor device including the semiconductor memory device according to claim 1.

9. A semiconductor memory device comprising:

a first wiring;

a second wiring;

a third wiring; and

a memory element including a first transistor, a second transistor, a third transistor, and a capacitor,

wherein a gate of the first transistor is electrically connected to one of a source and a drain of the first transistor,

wherein the other of the source and the drain of the first transistor is electrically connected to a gate of the second transistor,

wherein one of a source and a drain of the second transistor is electrically connected to the first wiring,

wherein one of a source and a drain of the third transistor is electrically connected to the gate of the first transistor,

wherein the other of the source and the drain of the third transistor is electrically connected to the second wiring,

wherein a gate of the third transistor is electrically connected to the third wiring,

wherein a first electrode of the capacitor is electrically connected to the gate of the second transistor, and

wherein the first transistor includes an oxide semiconductor film.

10. The semiconductor memory device according to claim 9, wherein carrier density of the oxide semiconductor film is less than 5×10^{14} /cm^3.

11. The semiconductor memory device according to claim 9,

wherein the second transistor includes a semiconductor film, and

wherein a material included in the semiconductor film is different from that included in the oxide semiconductor film.

12. The semiconductor memory device according to claim 9, wherein the semiconductor memory device is a write-once memory.

13. A semiconductor device including the semiconductor memory device according to claim 9.

14. A semiconductor memory device comprising:

a first wiring;

a second wiring;

a third wiring; and

a memory element including a first transistor, a second transistor, a third transistor, and a fourth transistor,

wherein a gate of the first transistor is electrically connected to one of a source and a drain of the first transistor,

wherein the other of the source and the drain of the first transistor is electrically connected to a gate of the second transistor,

wherein one of a source and a drain of the third transistor is electrically connected to the gate of the first transistor,

wherein one of a source and a drain of the second transistor is electrically connected to one of a source and a drain of the fourth transistor,

wherein the other of the source and the drain of the fourth transistor is electrically connected to the first wiring,

wherein the other of the source and the drain of the third transistor is electrically connected to the second wiring,

wherein a gate of the third transistor is electrically connected to the third wiring, and

wherein the first transistor includes an oxide semiconductor film.

15. The semiconductor memory device according to claim 14,

wherein the memory element further includes a capacitor, and

wherein a first electrode of the capacitor is electrically connected to the gate of

the second transistor.

16. The semiconductor memory device according to claim 15,
wherein a potential of a second electrode of the capacitor is a fixed potential.

17. The semiconductor memory device according to claim 15, wherein carrier density of the oxide semiconductor film is less than 5×10^{14} /cm^3.

18. The semiconductor memory device according to claim 15,
wherein the second transistor includes a semiconductor film, and
wherein a material included in the semiconductor film is different from that included in the oxide semiconductor film.

19. The semiconductor memory device according to claim 15, wherein the semiconductor memory device is a write-once memory.

20. A semiconductor device including the semiconductor memory device according to claim 15.

FIG. 1A

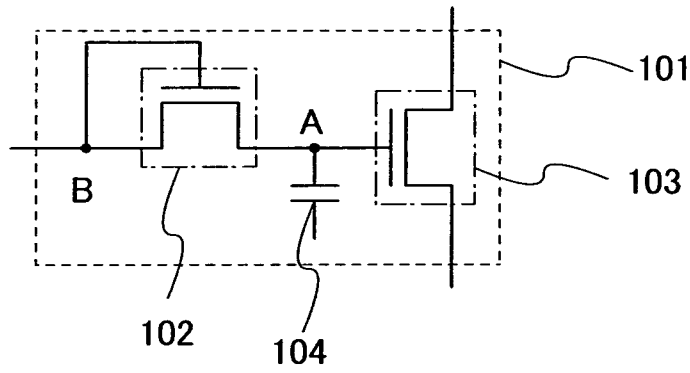


FIG. 1B

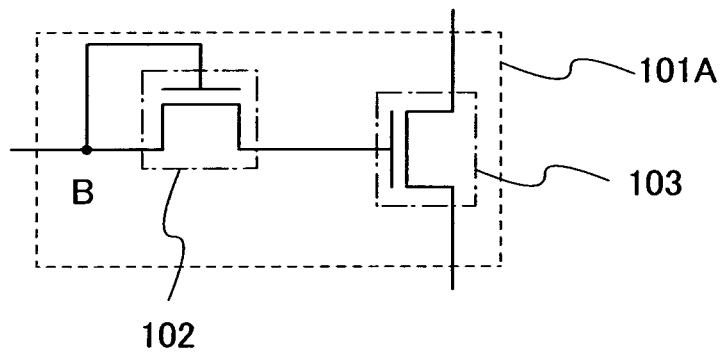


FIG. 2A

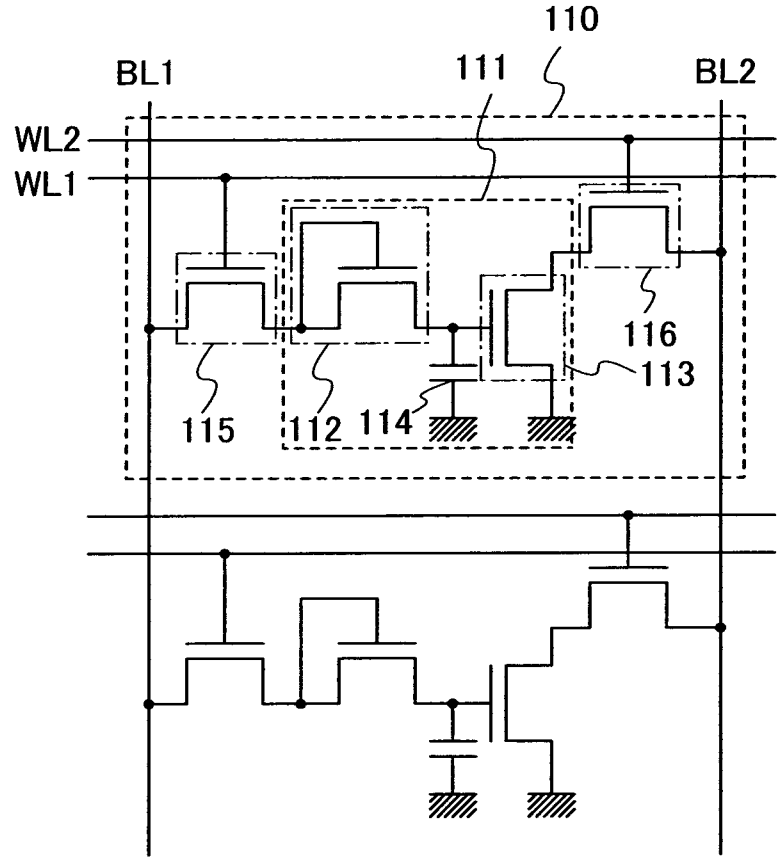

110
BL1
111
BL2
WL2
WL1
116
113
115
112
114

FIG. 2B

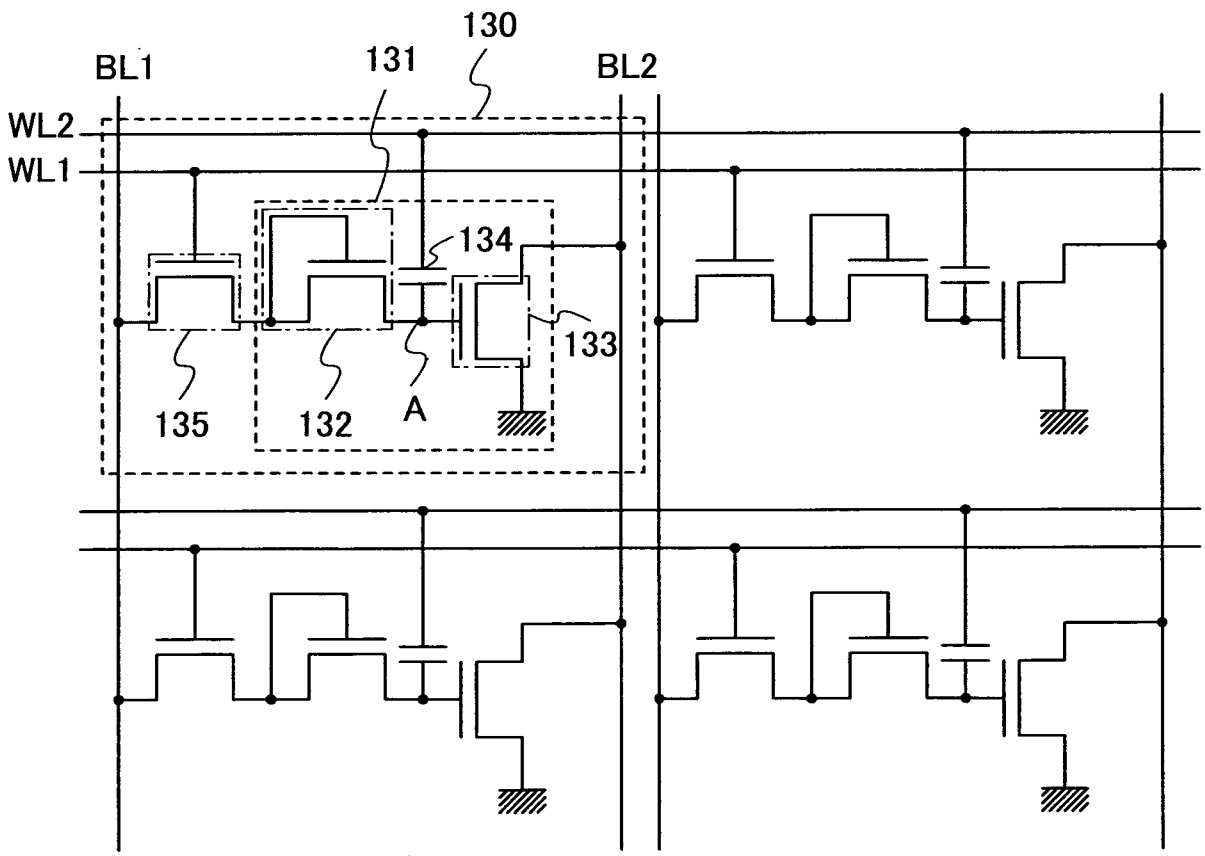

130
BL1
131
BL2
WL2
WL1
134
133
135
132
A

FIG. 3

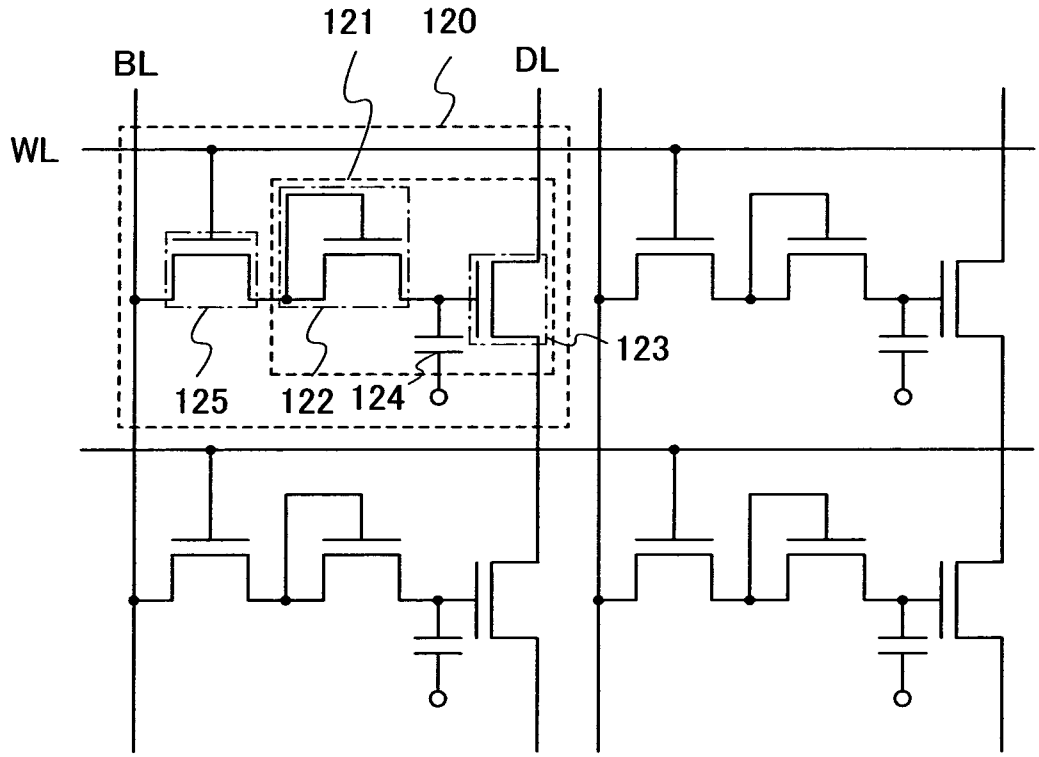


FIG. 4A

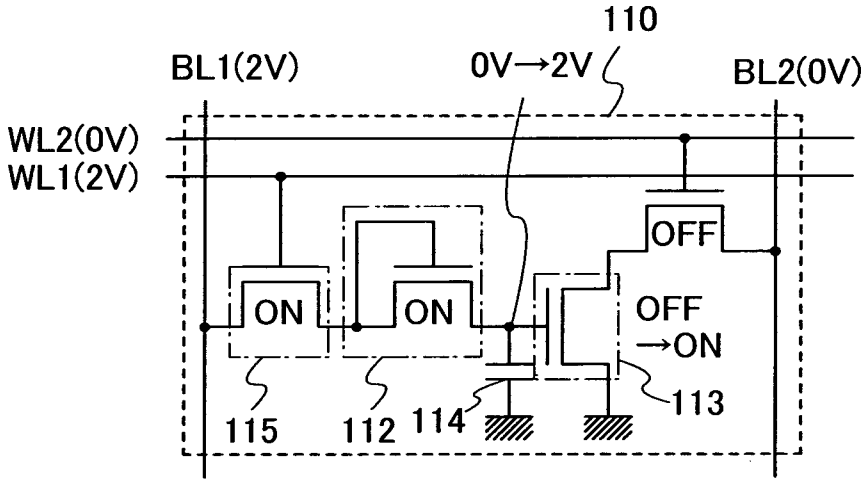

110
BL1(2V)
0V→2V
BL2(0V)
WL2(0V)
WL1(2V)
OFF
ON
ON
OFF
→ON
113
115
112
114

FIG. 4B

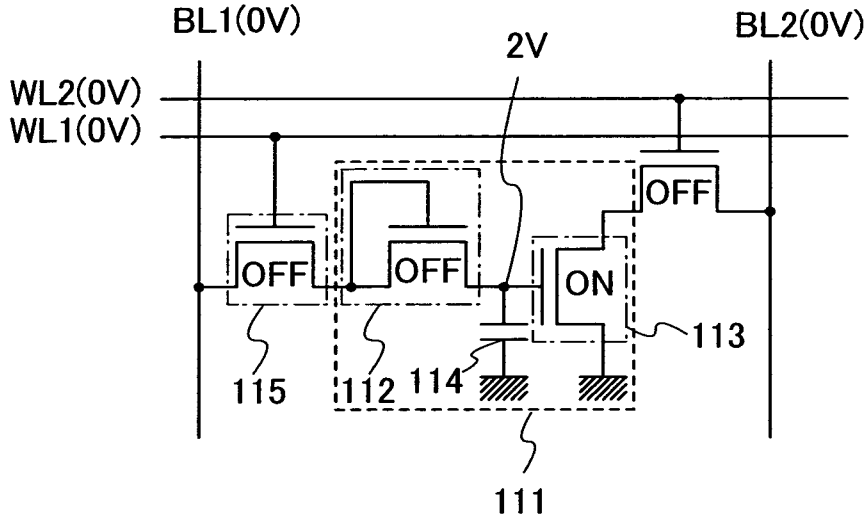

BL1(0V)
2V
BL2(0V)
WL2(0V)
WL1(0V)
OFF
OFF
OFF
ON
113
115
112
114
111

FIG. 5A

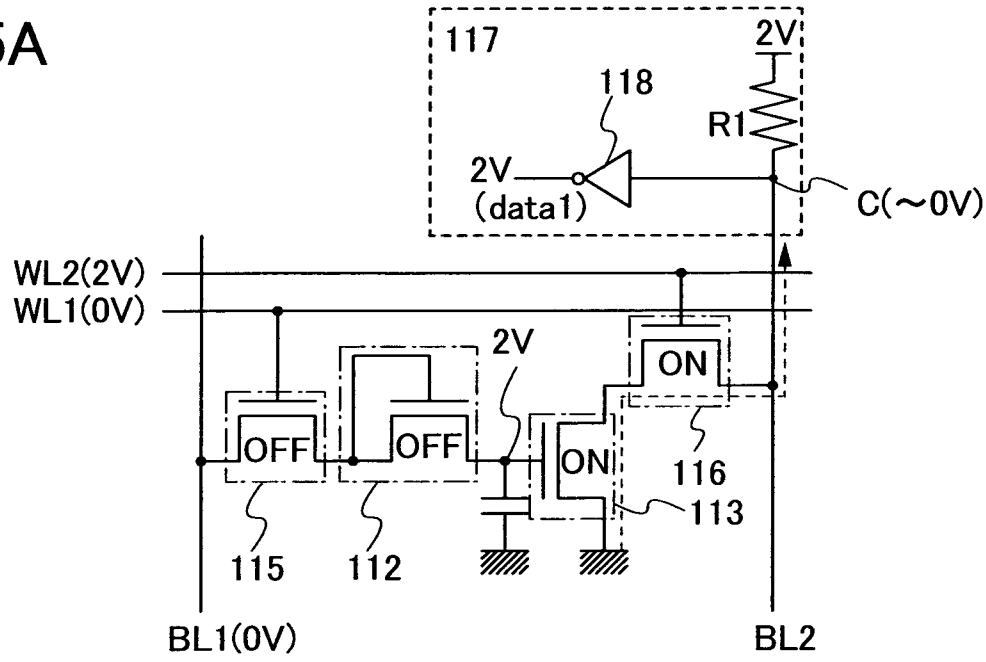

117
2V
118
R1
2V
(data1)
C(~0V)
WL2(2V)
WL1(0V)
2V
ON
OFF
OFF
ON
116
113
115
112
BL1(0V)
BL2

FIG. 5B

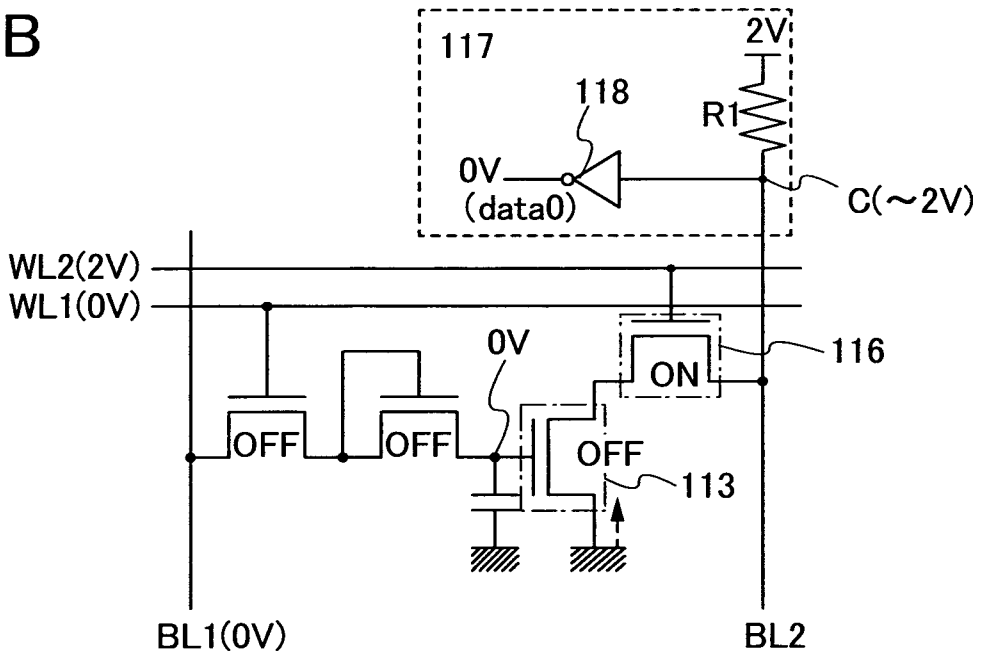

117
2V
118
R1
0V
(data0)
C(~2V)
WL2(2V)
WL1(0V)
0V
116
ON
OFF
OFF
OFF
113
BL1(0V)
BL2

FIG. 6

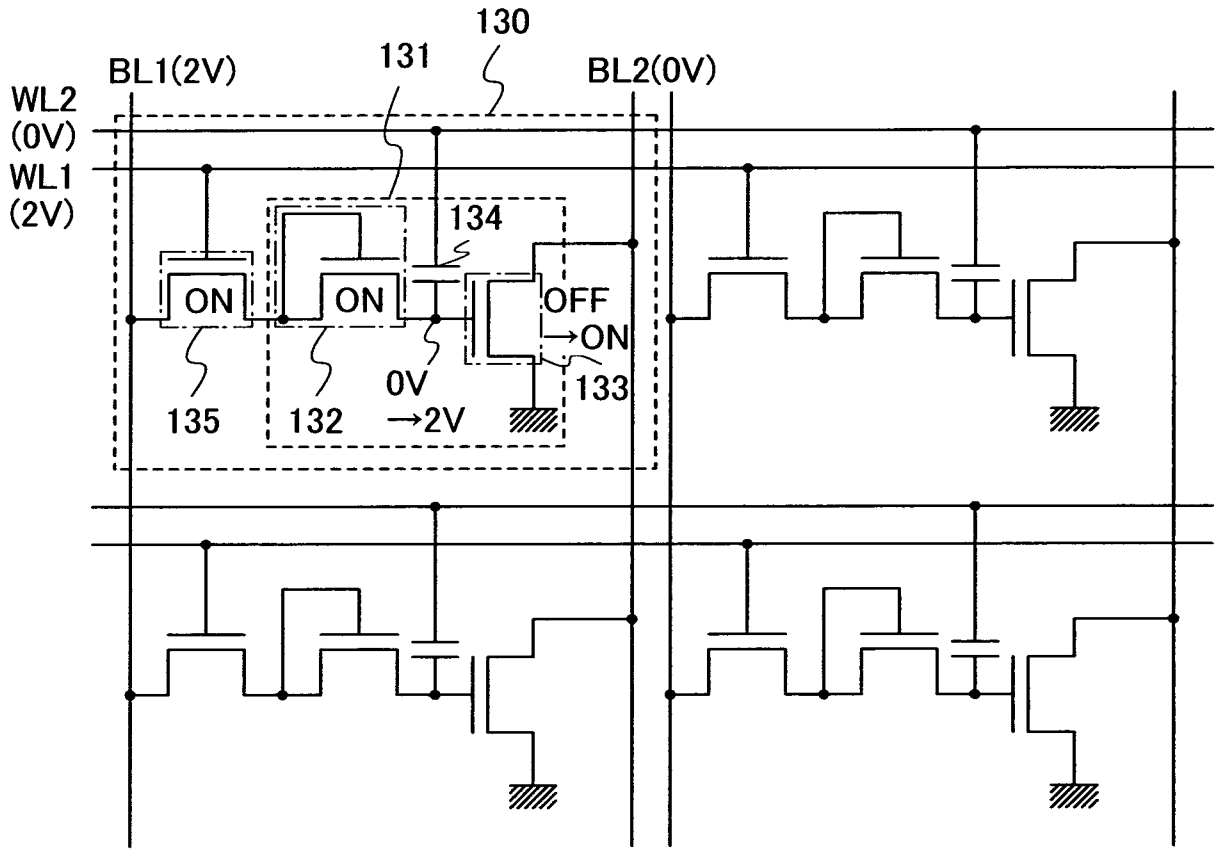

130
131
BL1(2V)
BL2(0V)
WL2
(0V)
WL1
(2V)
134
ON
ON
OFF
→ON
133
135
132
0V
→2V

FIG. 7A

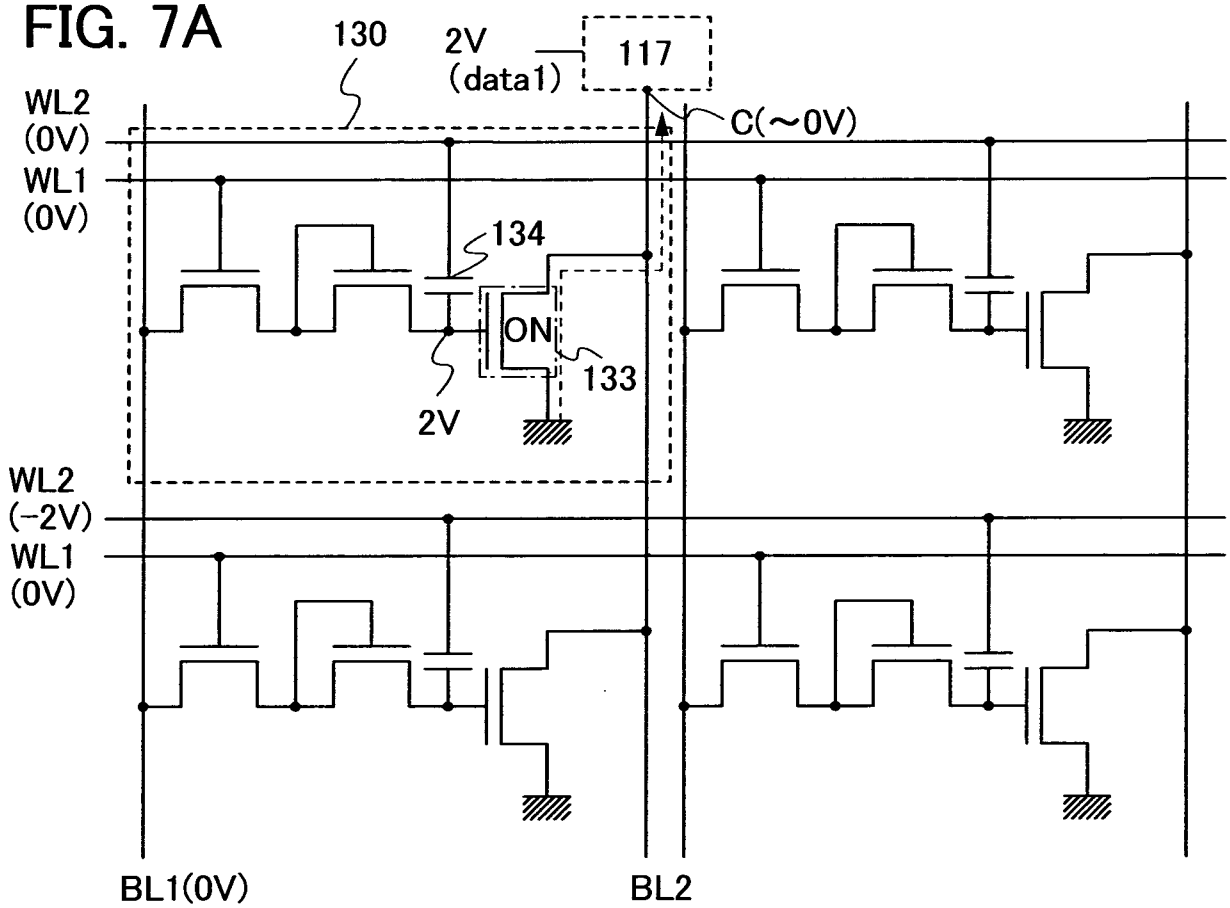

130
2V
(data1)
117
C(~0V)
WL2
(0V)
WL1
(0V)
134
ON
133
2V
WL2
(-2V)
WL1
(0V)
BL1(0V)
BL2

FIG. 7B

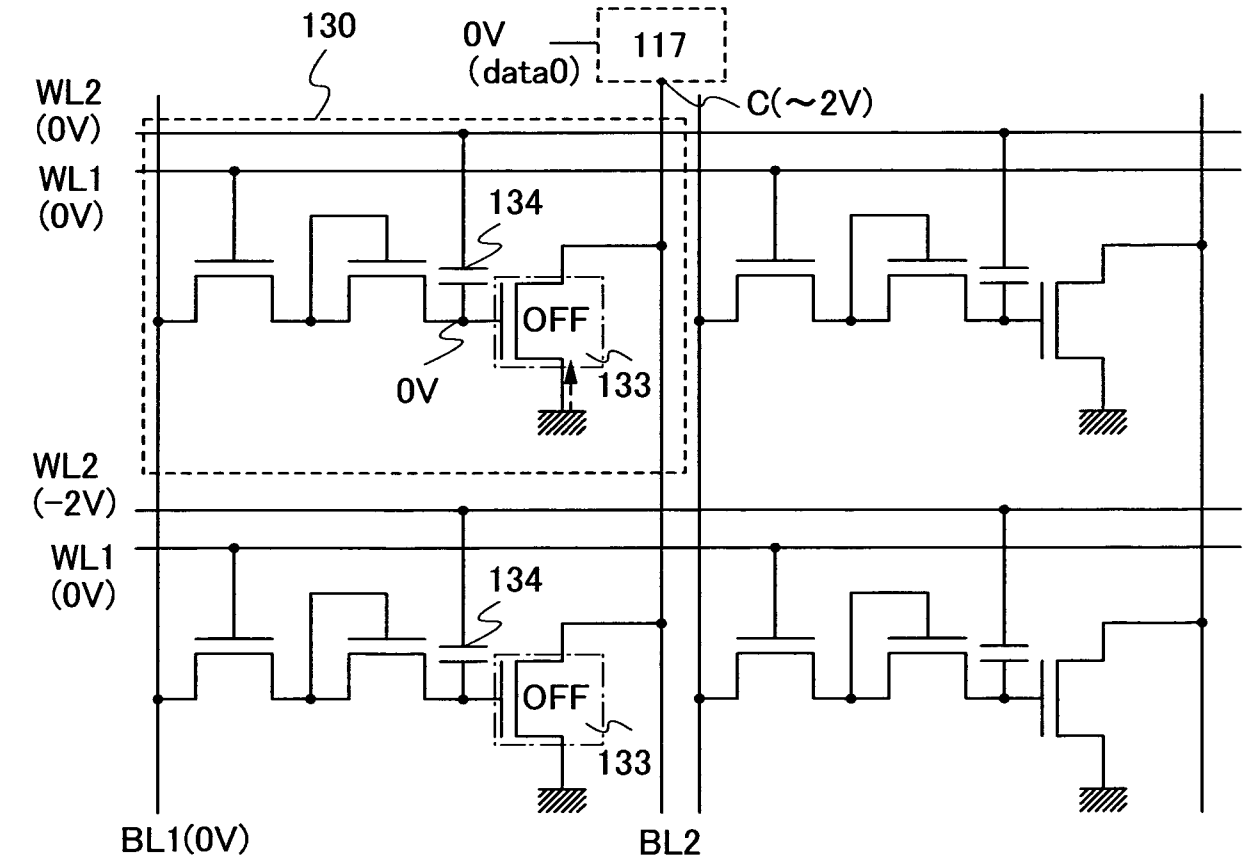

130
0V
(data0)
117
C(~2V)
WL2
(0V)
WL1
(0V)
134
OFF
0V
133
WL2
(-2V)
WL1
(0V)
134
OFF
133
BL1(0V)
BL2

FIG. 8

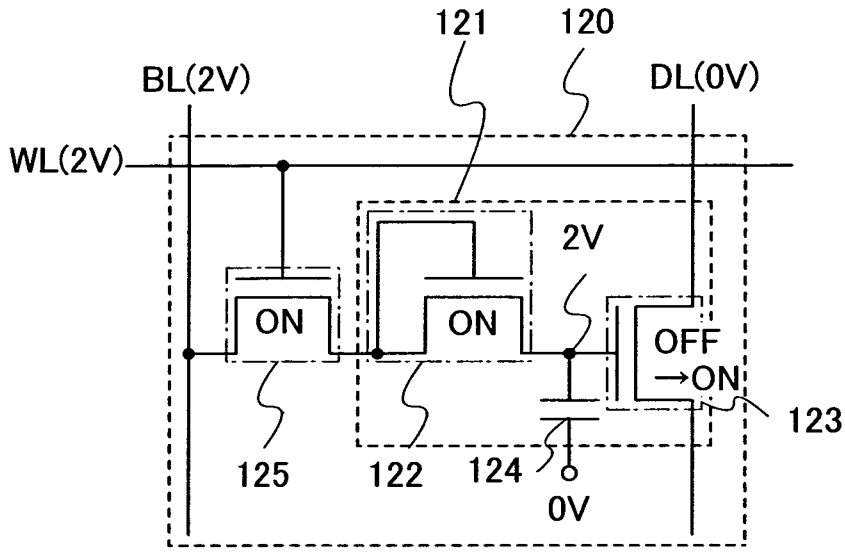


FIG. 9A

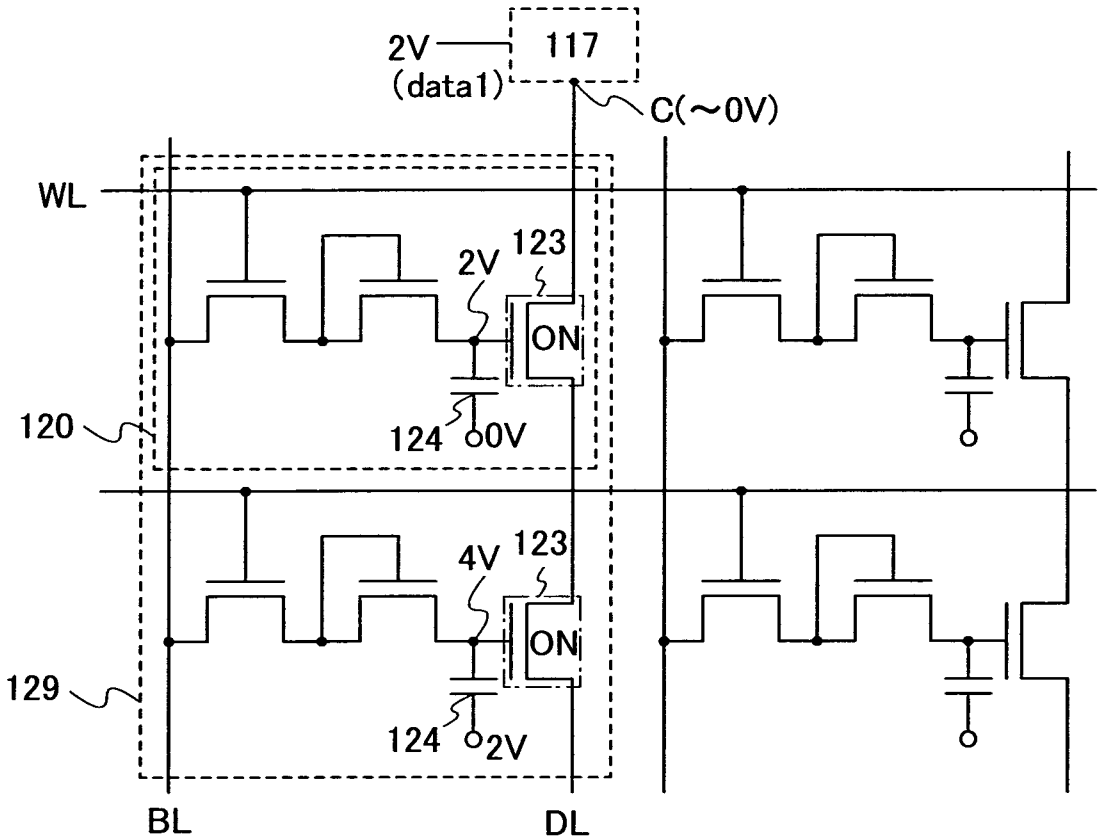

2V
(data1)
117
C(~0V)
WL
2V
123
ON
120
124
0V
4V
123
ON
129
124
2V
BL
DL

FIG. 9B

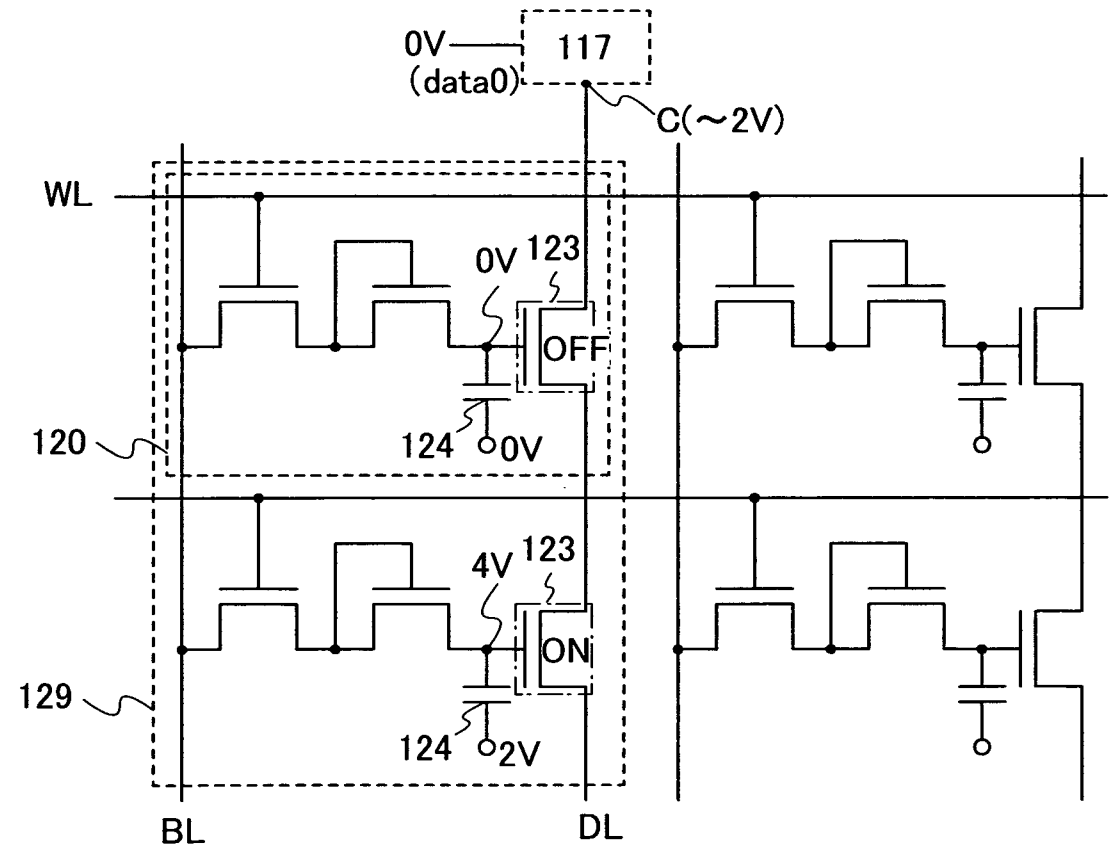

0V
(data0)
117
C(~2V)
WL
0V
123
OFF
120
124
0V
4V
123
ON
129
124
2V
BL
DL

FIG. 10A

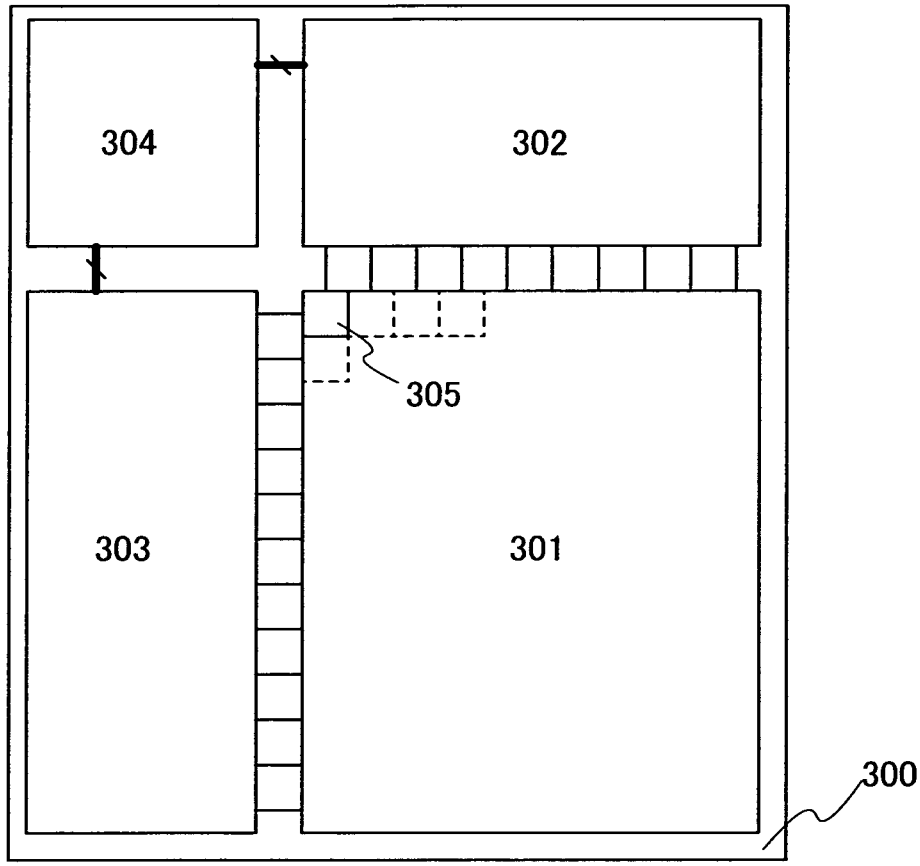


FIG. 10B

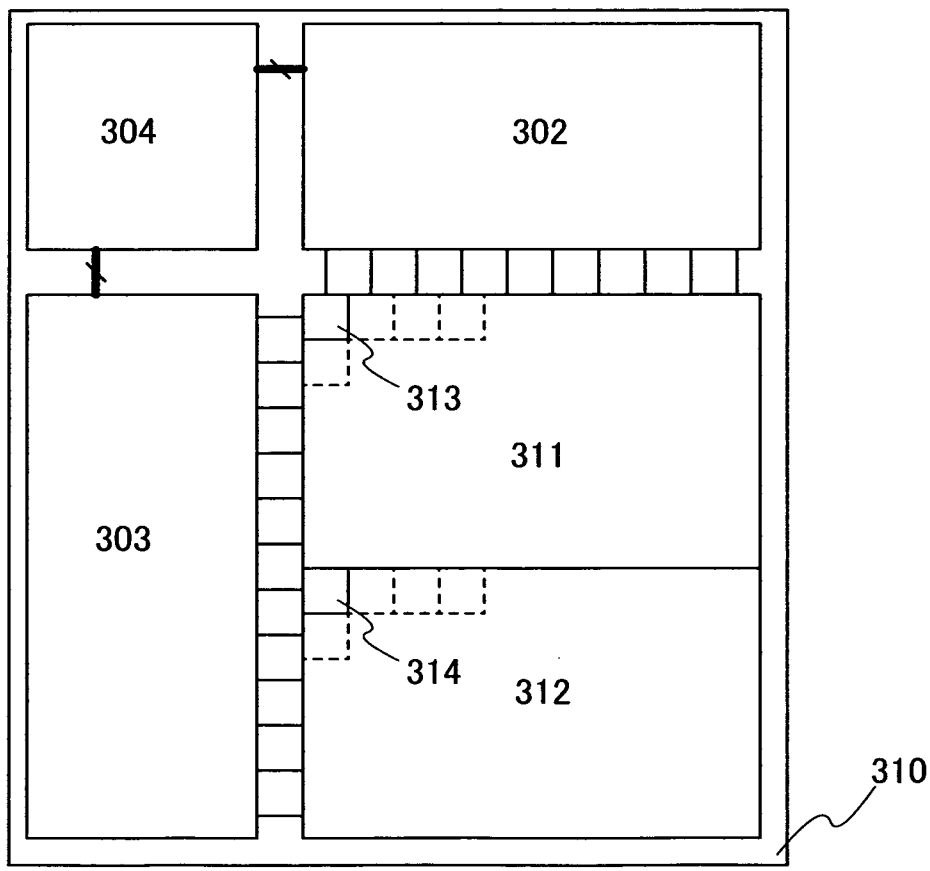


FIG. 11A

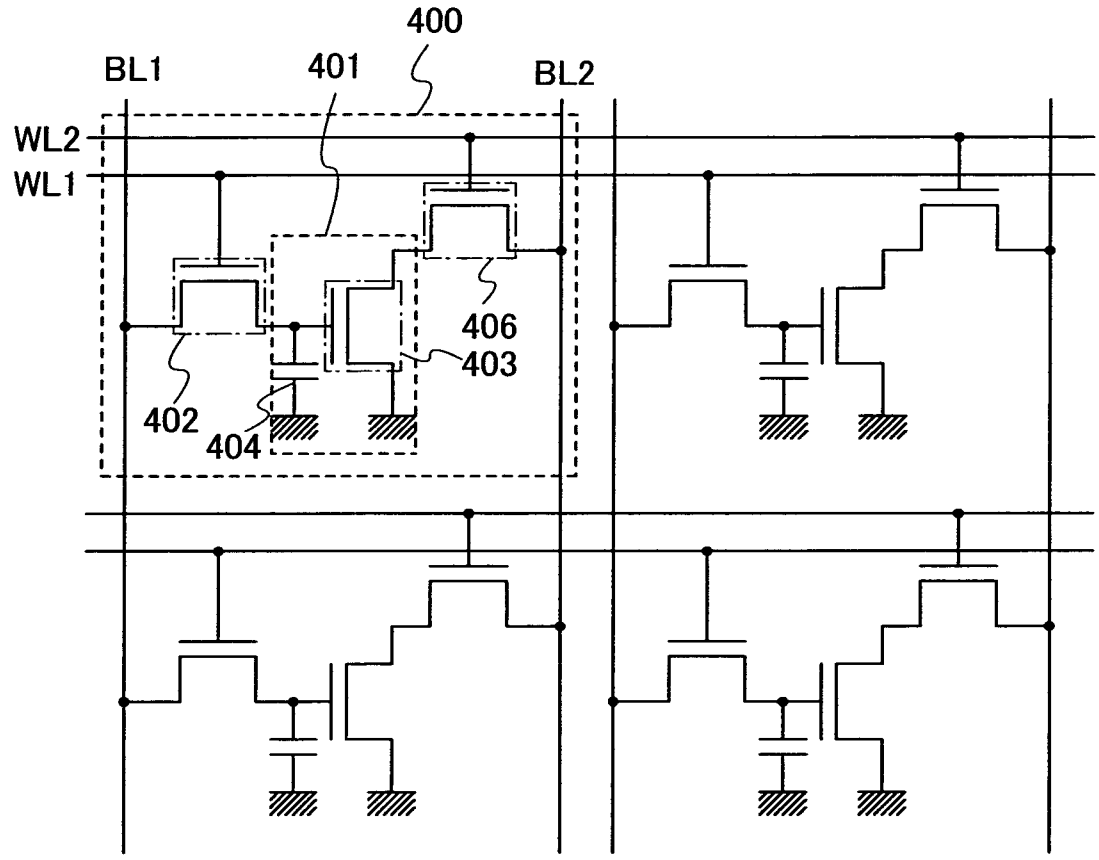


FIG. 11B

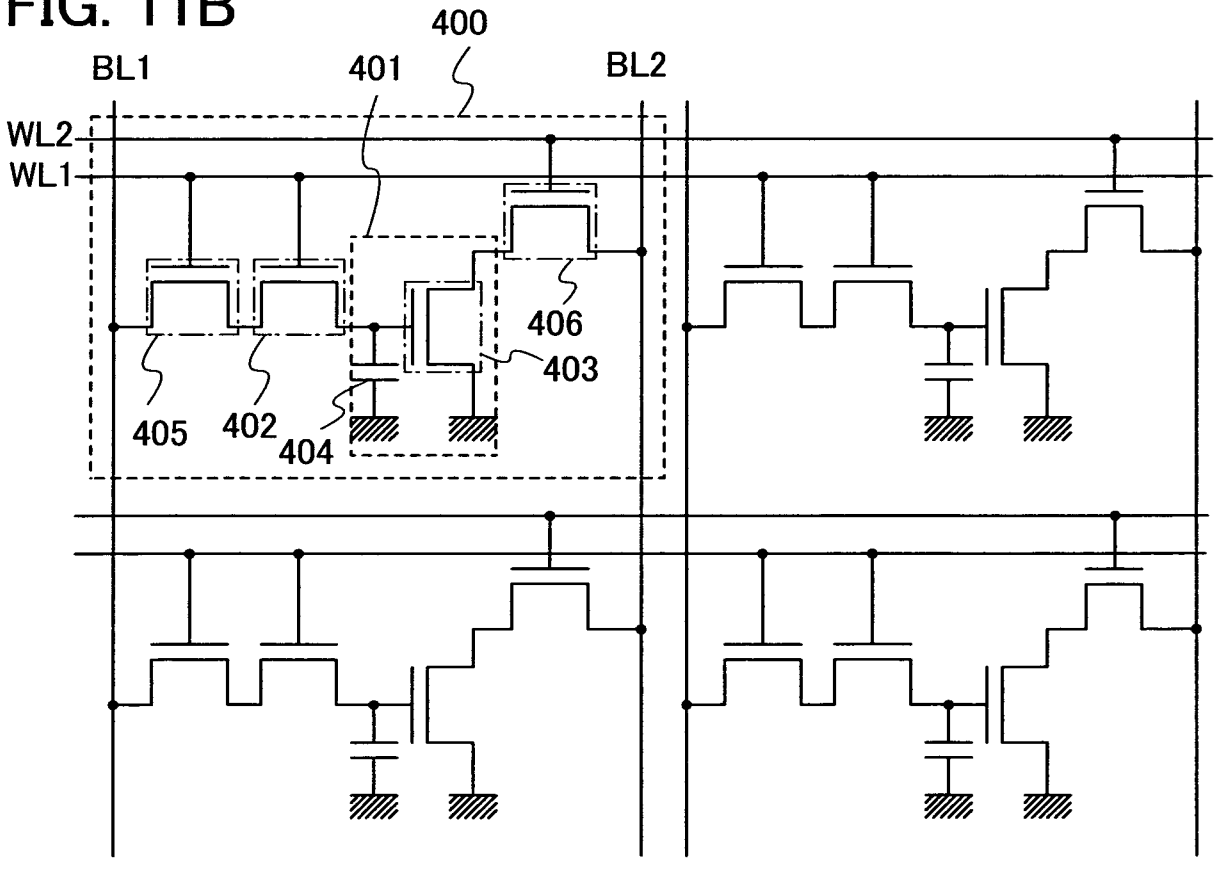


FIG. 12A

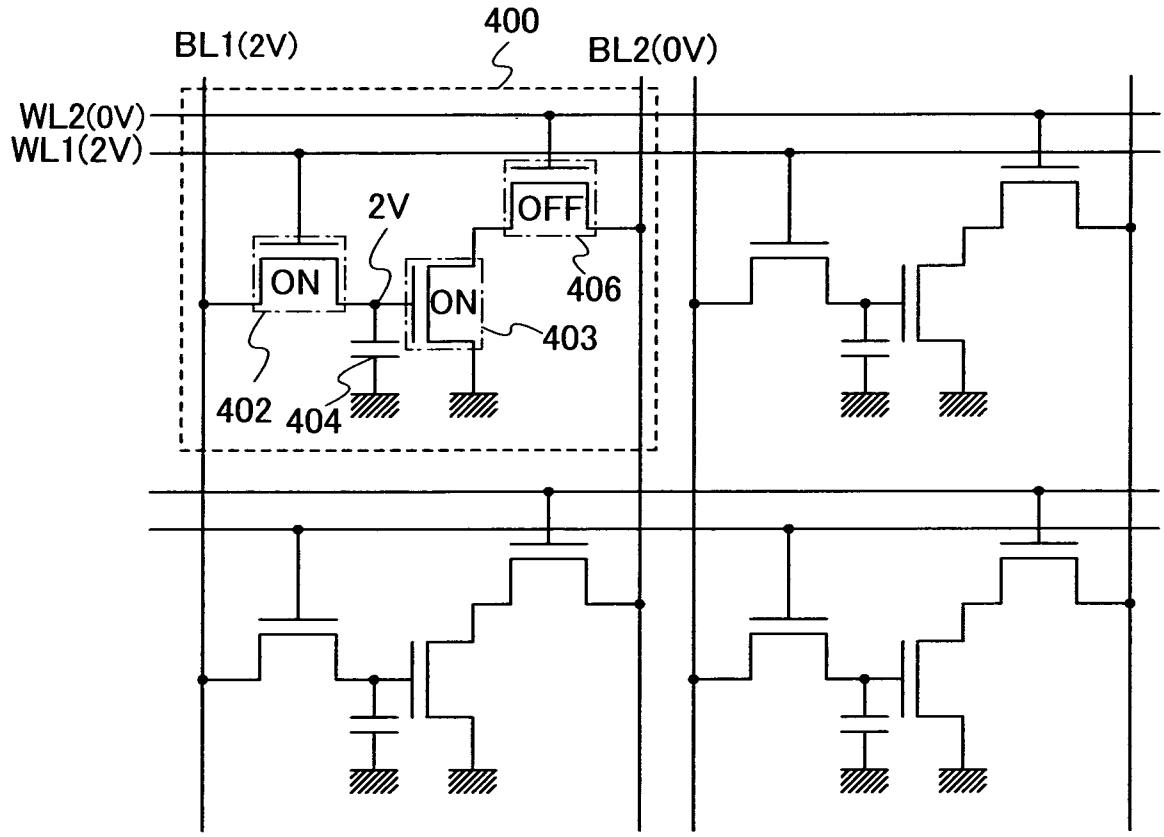


FIG. 12B

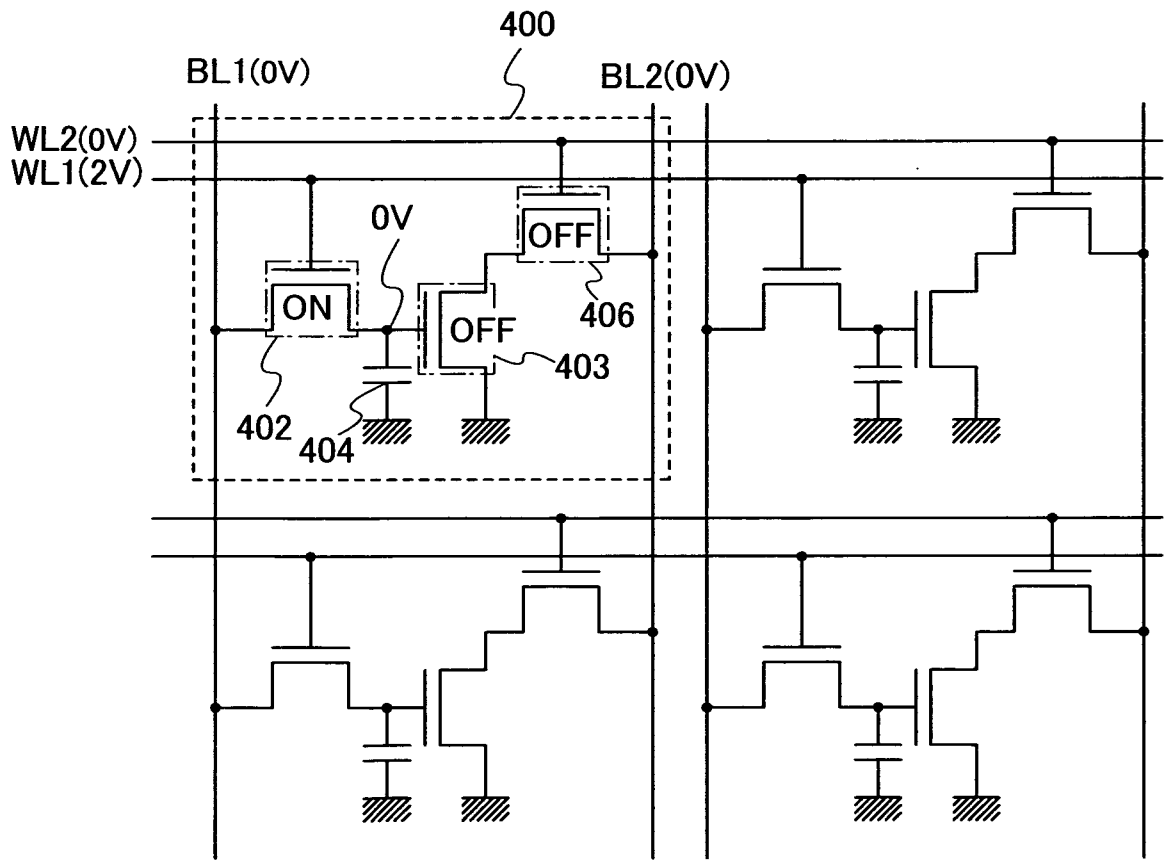


FIG. 13A

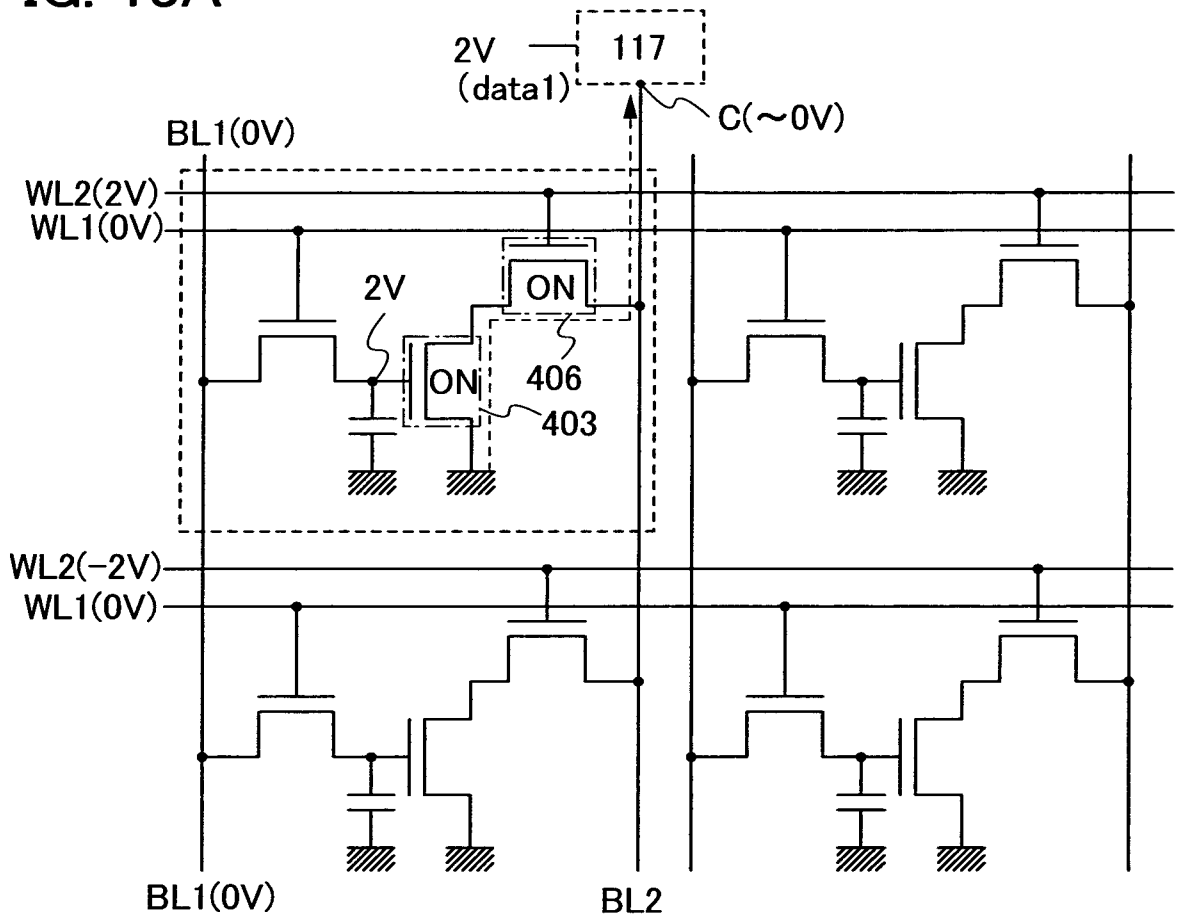


FIG. 13B

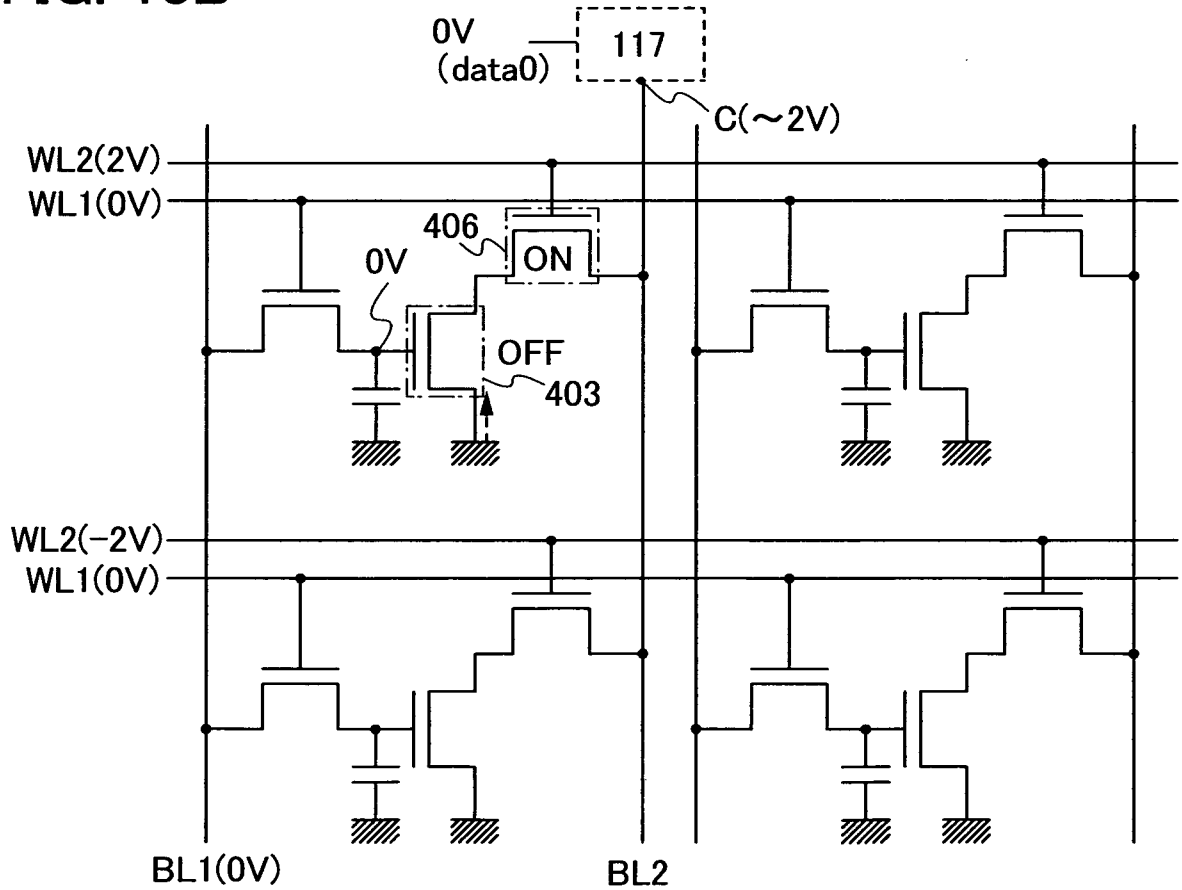


FIG. 14

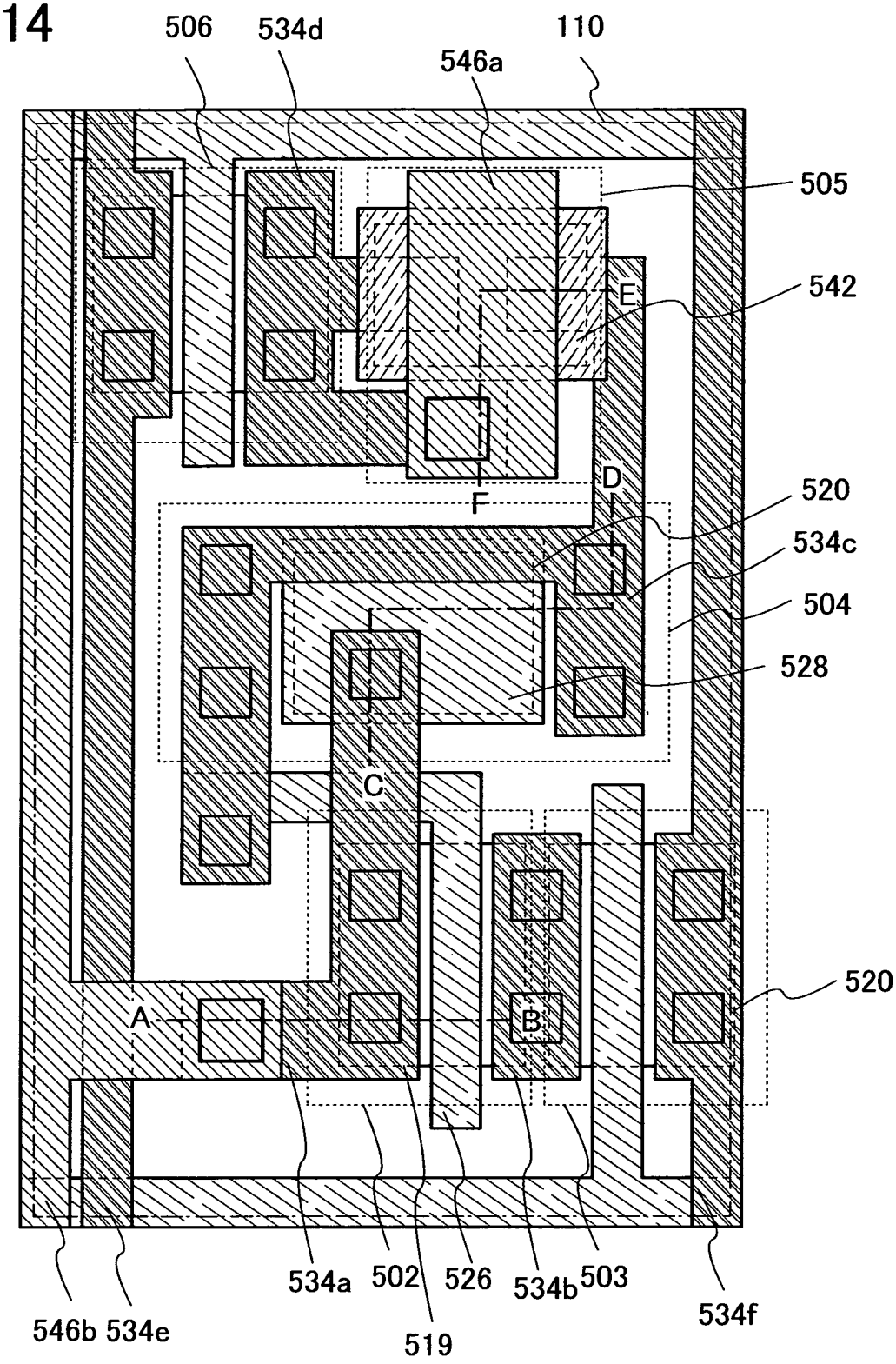

506
534d
546a
110
505
542
E
D
F
520
534c
504
528
C
520
A
B
546b
534e
534a
502
519
526
534b
503
534f

FIG. 15

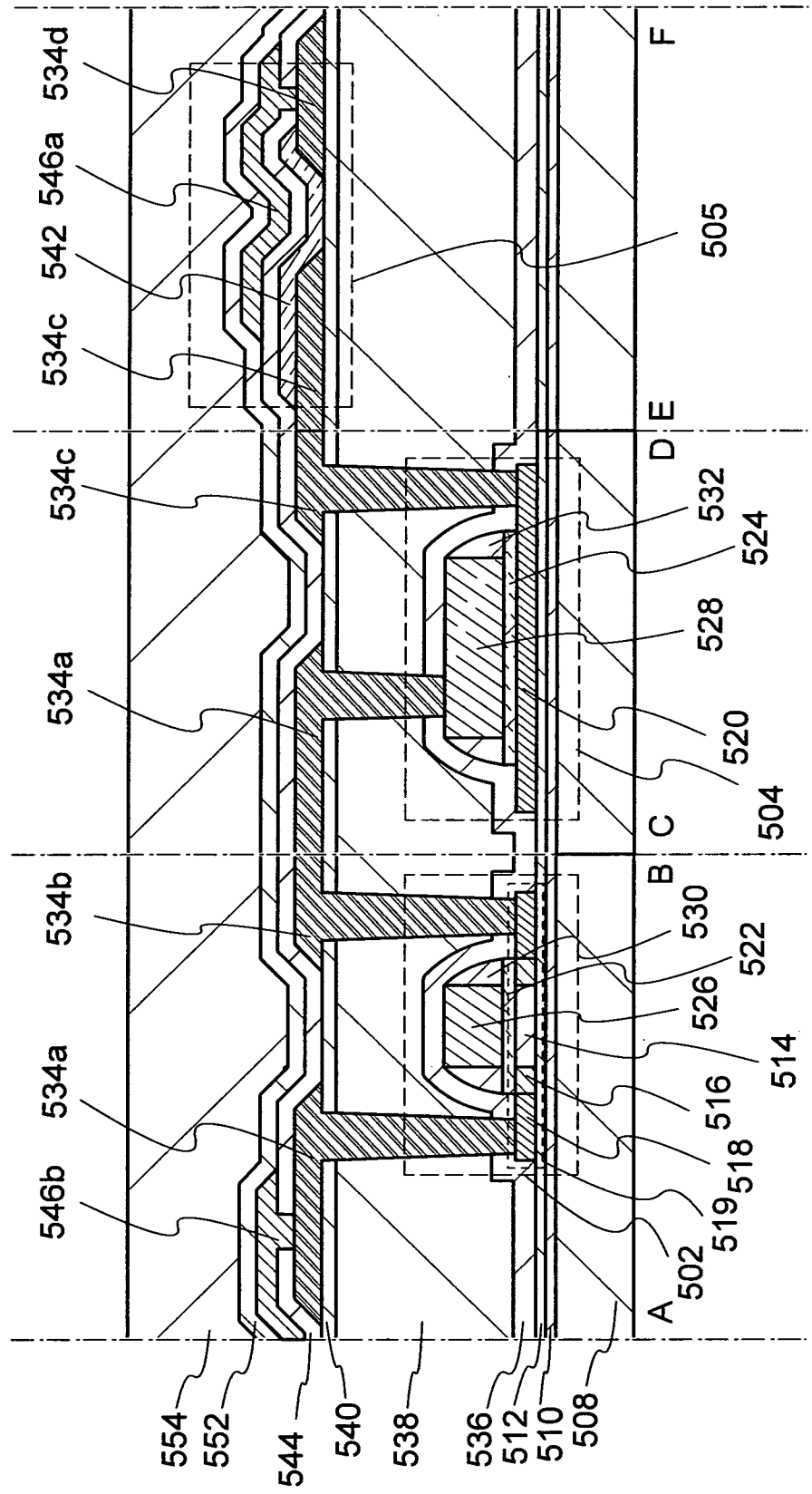

534d
546a
542
534c
534c
534a
546b
534b
534a
505
532
524
528
520
504
530
522
526
514
516
518
519
502
554
552
544
540
538
536
512
510
508
A
B
C
D
E
F

FIG. 16A

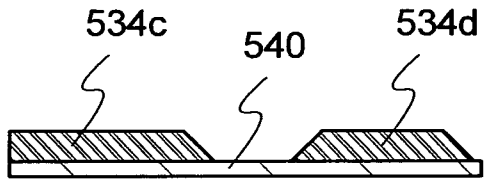


FIG. 16B

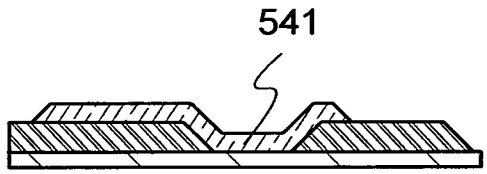


FIG. 16C

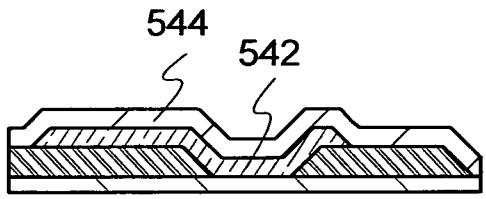


FIG. 16D

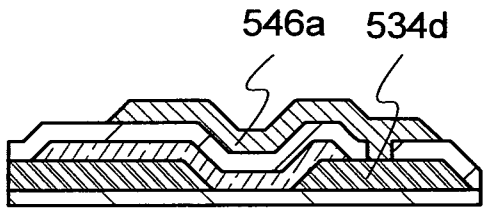


FIG. 16E

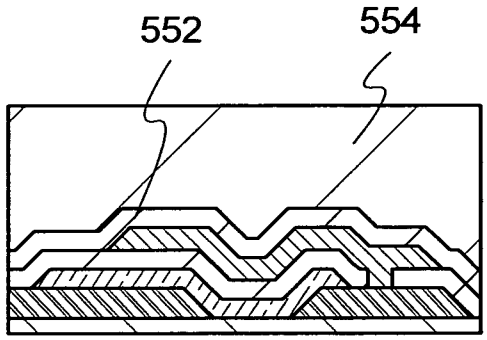


FIG. 17

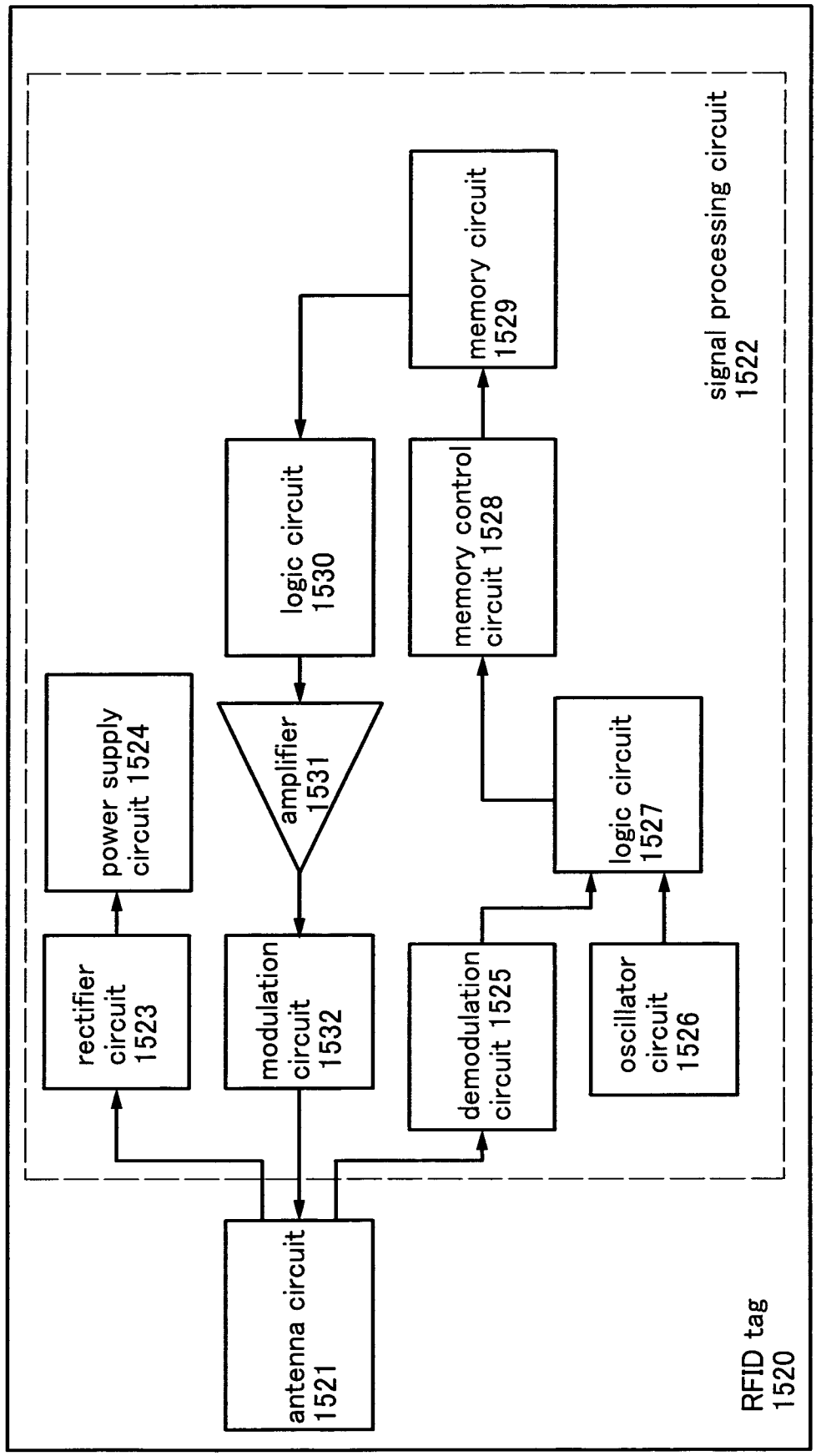

RFID tag
1520
signal processing circuit
1522
antenna circuit
1521
rectifier circuit
1523
power supply circuit 1524
modulation circuit
1532
amplifier
1531
logic circuit
1530
memory circuit
1529
demodulation circuit 1525
oscillator circuit
1526
logic circuit
1527
memory control circuit 1528

FIG. 18

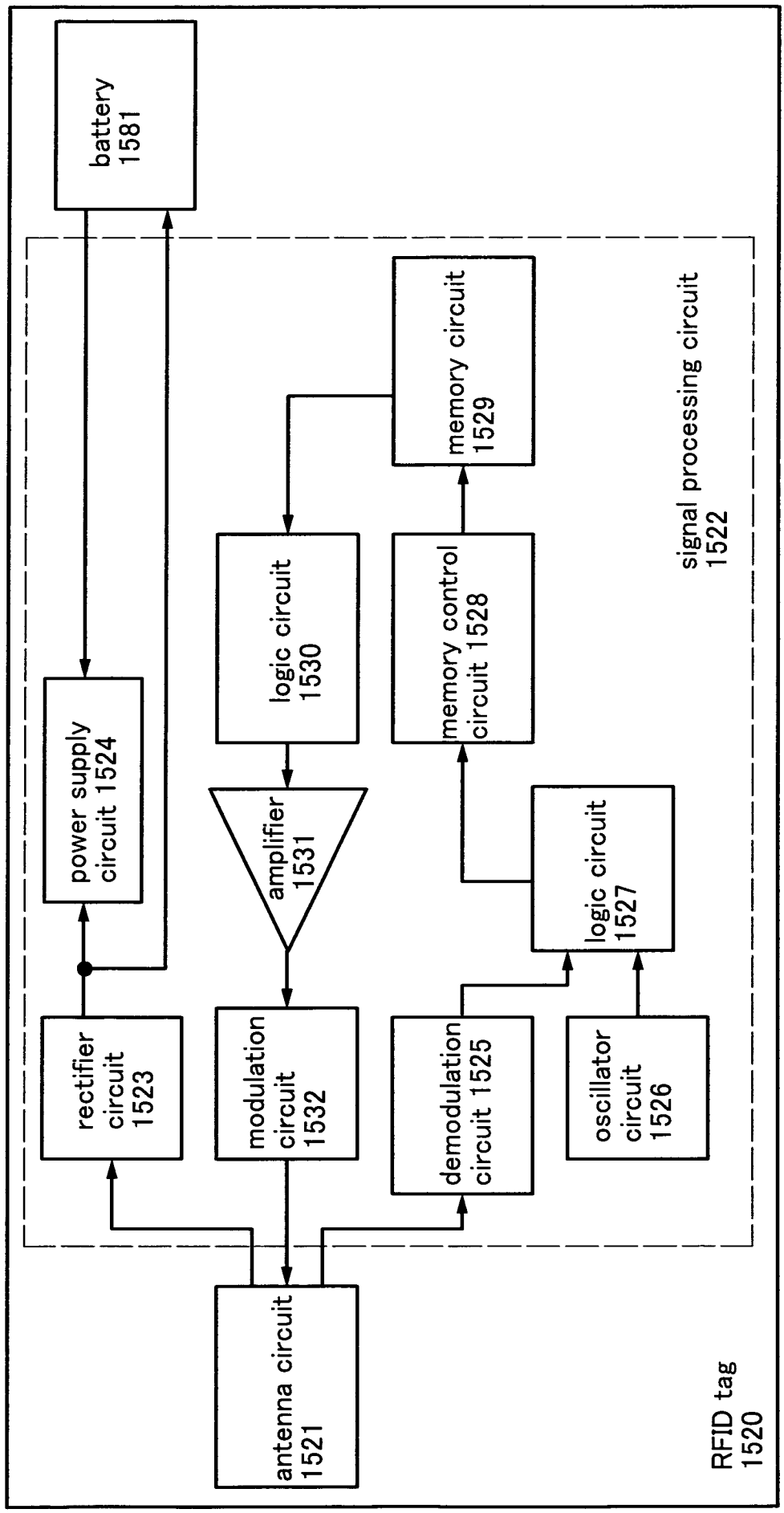

battery
1581
memory circuit
1529
signal processing circuit
1522
logic circuit
1530
memory control
circuit 1528
power supply
circuit 1524
amplifier
1531
logic circuit
1527
rectifier
circuit
1523
modulation
circuit
1532
demodulation
circuit 1525
oscillator
circuit
1526
antenna circuit
1521
RFID tag
1520

FIG. 19A

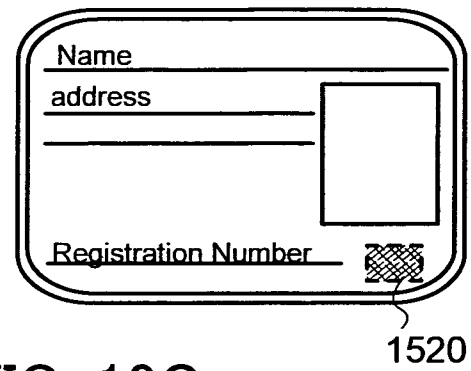


FIG. 19B

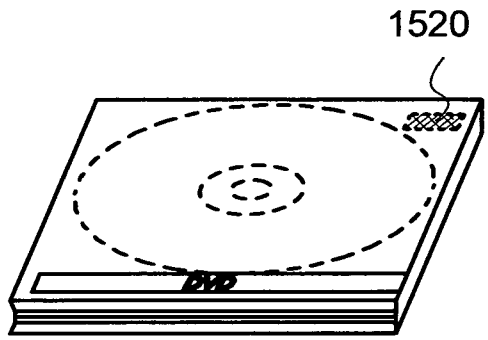


FIG. 19C

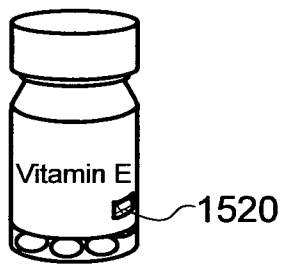


FIG. 19D

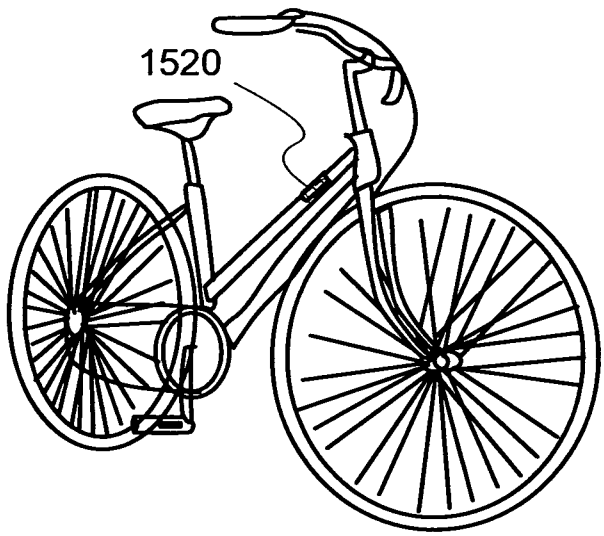


FIG. 19E

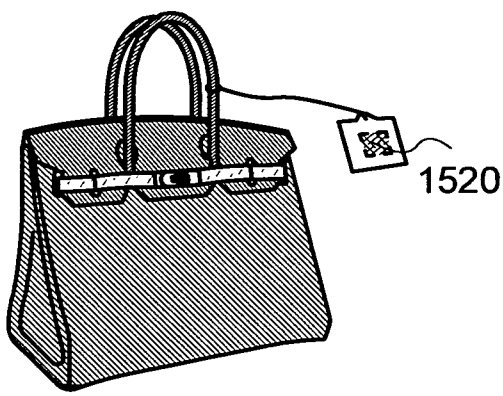


FIG. 19F

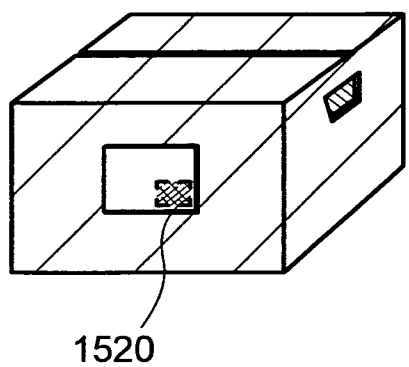


FIG. 20A

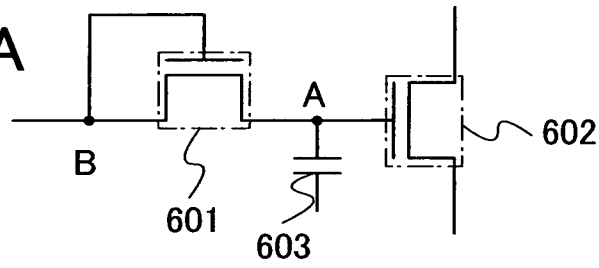


FIG. 20B

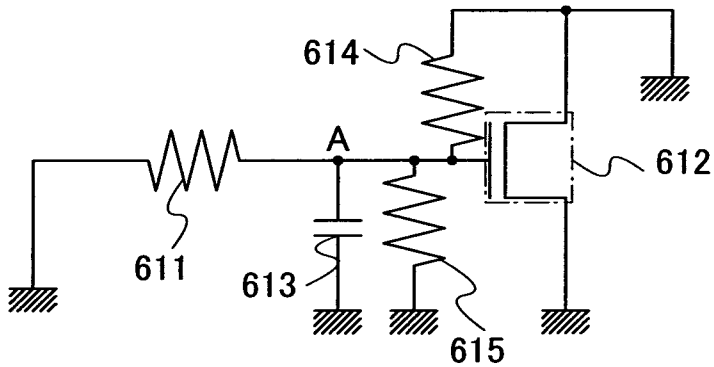


FIG. 20C

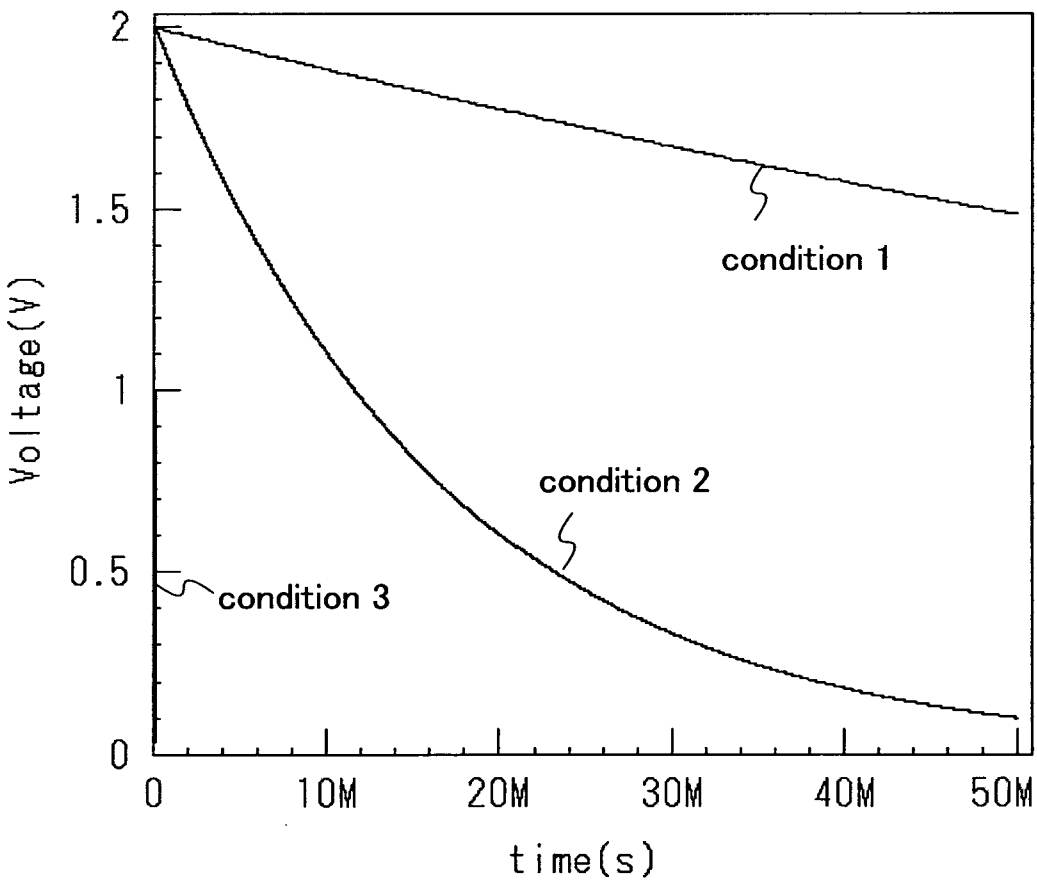


FIG. 21

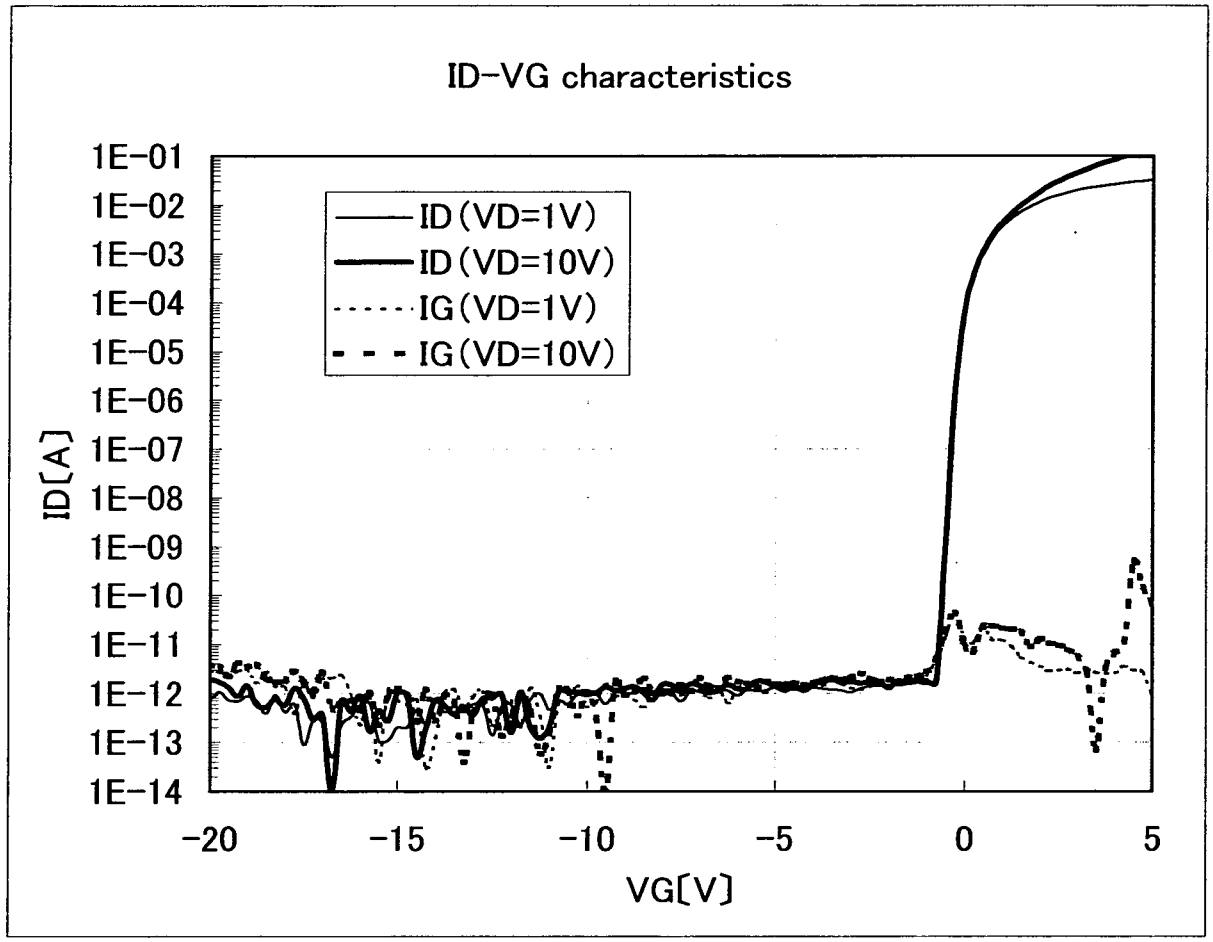

ID-VG characteristics
ID(VD=1V)
ID(VD=10V)
IG(VD=1V)
IG(VD=10V)
ID[A]
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
1E-14
-20
-15
-10
-5
0
5
VG[V]

FIG. 22

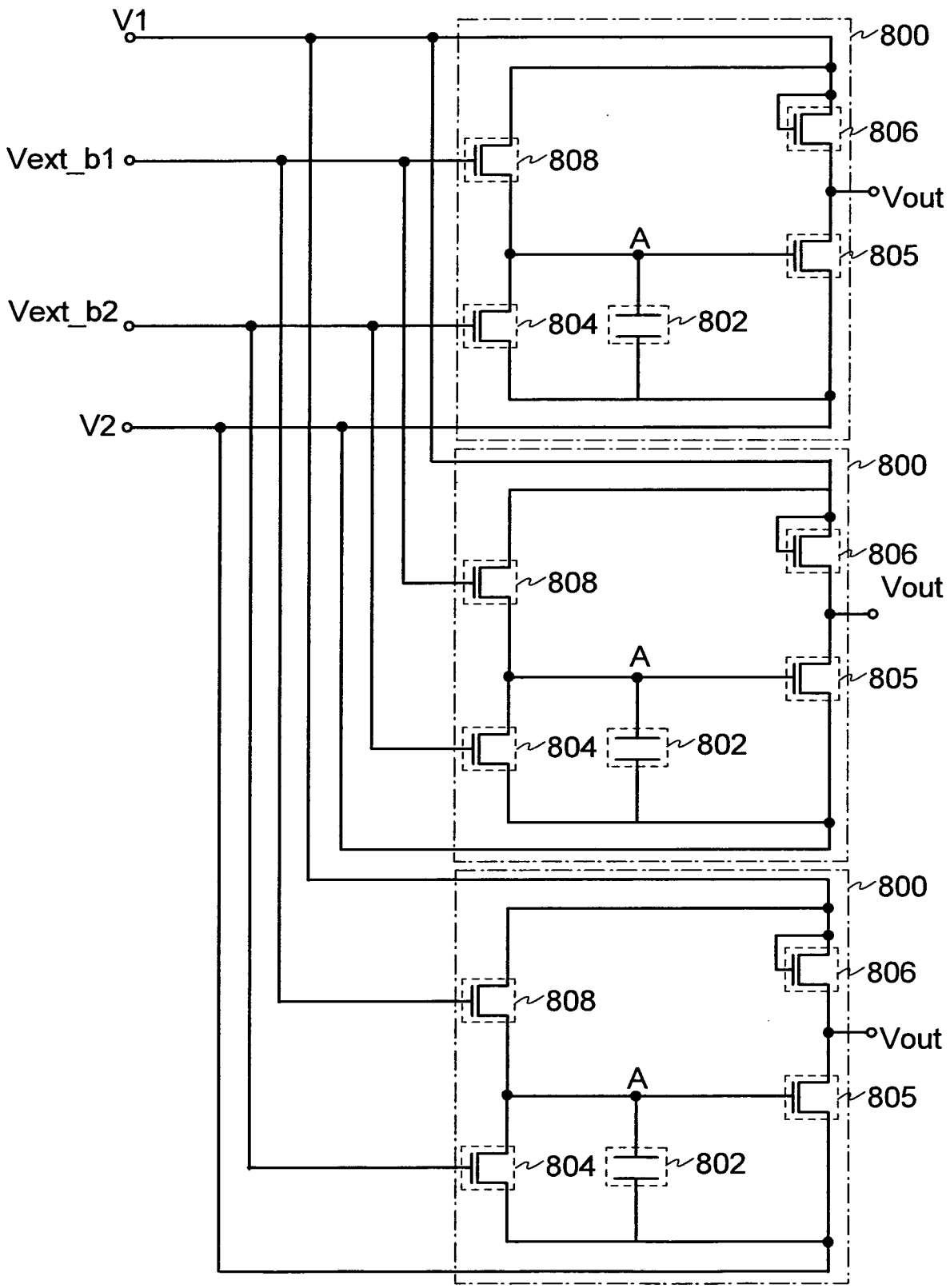

V1
Vext_b1
Vext_b2
V2
800
806
808
Vout
A
805
804
802
800
806
808
Vout
A
805
804
802
800
806
808
Vout
A
805
804
802

FIG. 23

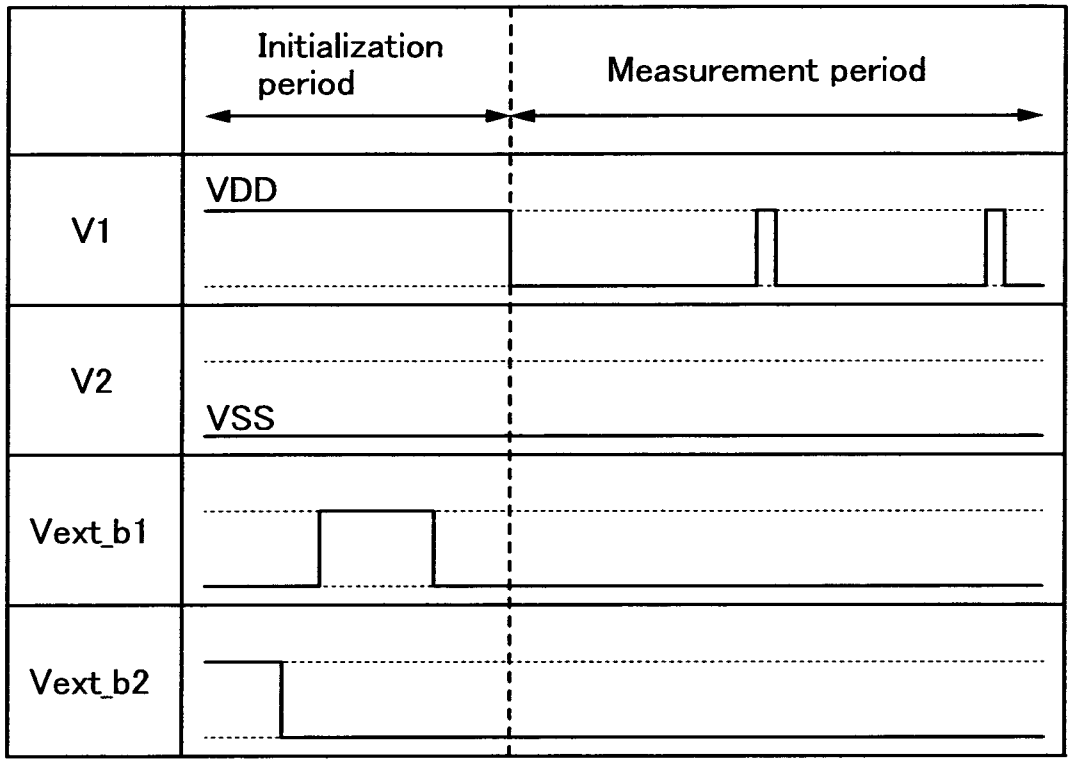

Initialization period
Measurement period
V1
VDD
V2
VSS
Vext_b1
Vext_b2

FIG. 24

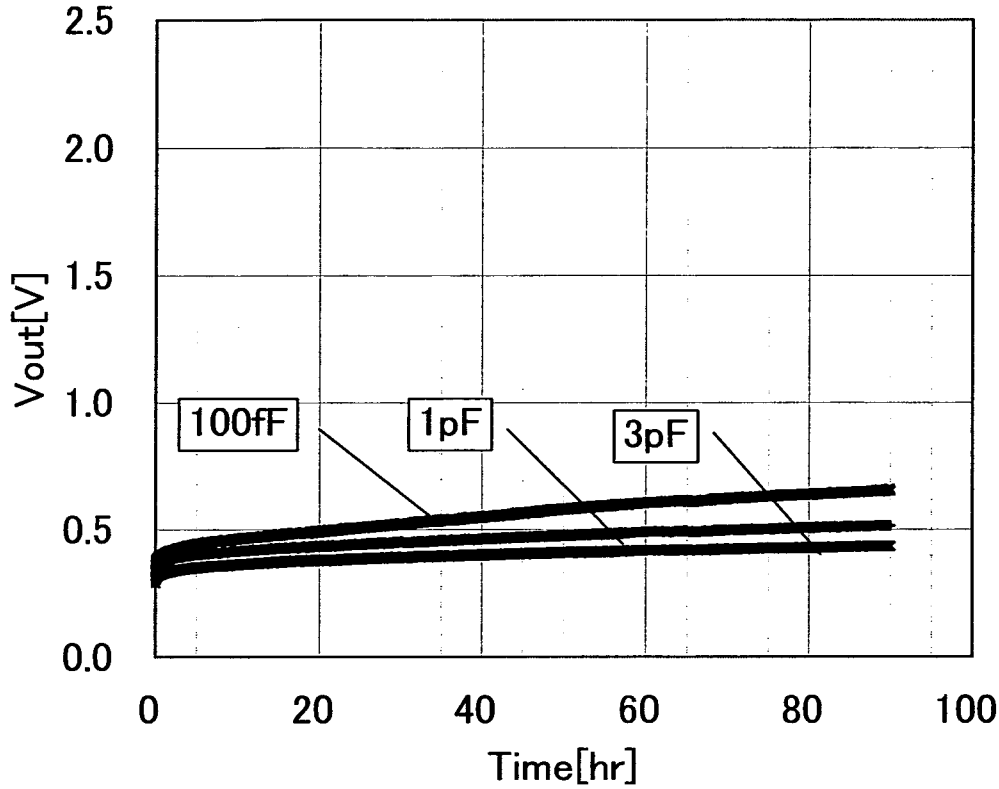


FIG. 25

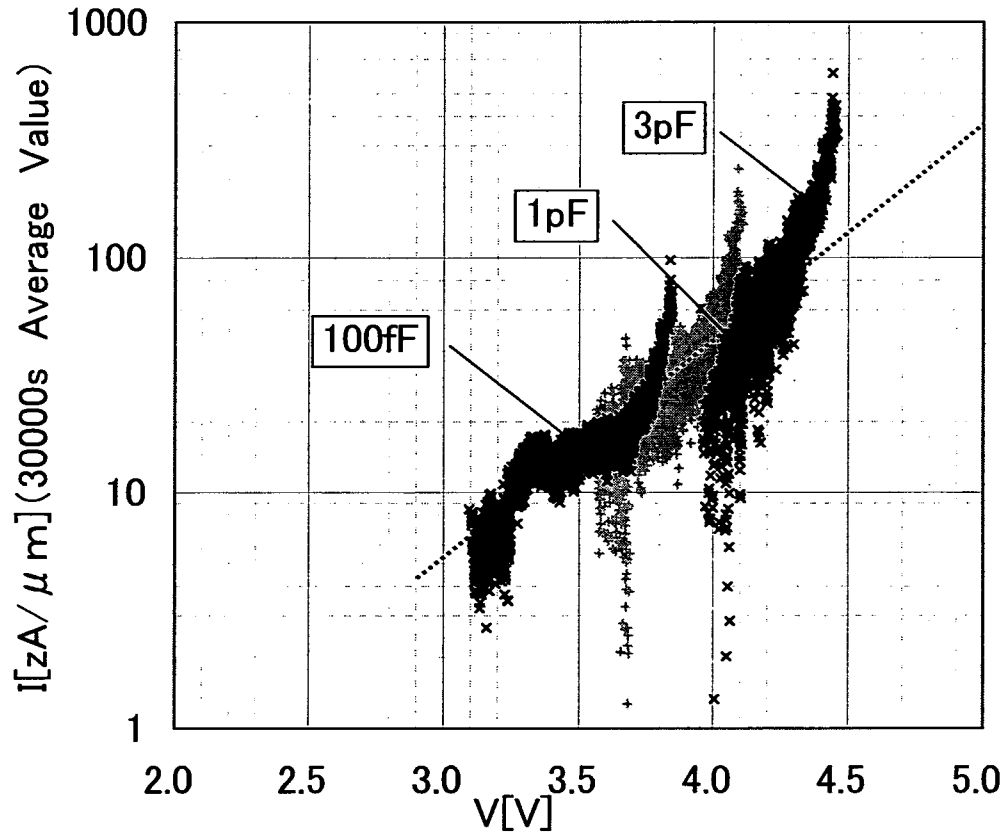
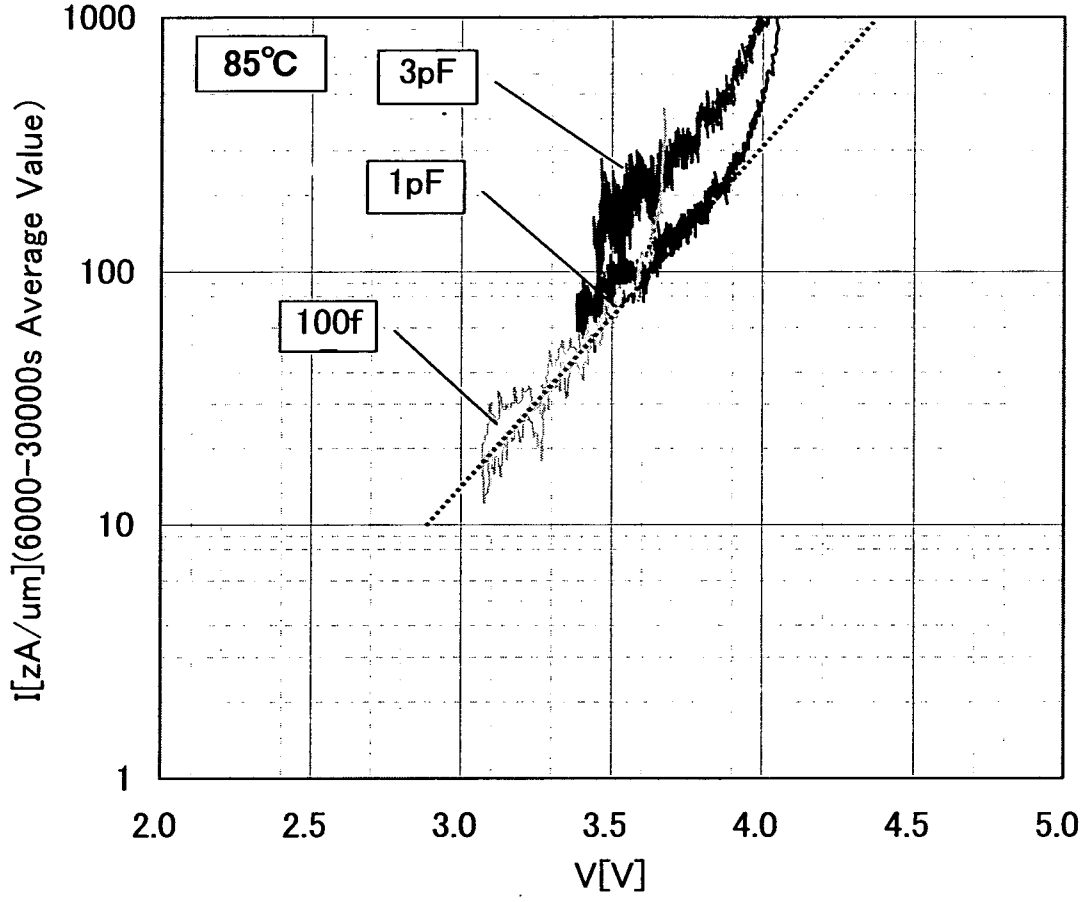

1000
100
10
1
I[zA/μm](30000s Average Value)
2.0
2.5
3.0
3.5
4.0
4.5
5.0
V[V]
3pF
1pF
100fF

FIG. 26


1000
100
10
1
85℃
3pF
1pF
100f
I[zA/um](6000-30000s Average Value)
2.0
2.5
3.0
3.5
4.0
4.5
5.0
V[V]

EXPLANATION OF REFERENCE

101: memory element, 102: transistor, 103: transistor, 104: capacitor, 110: memory cell, 111: memory element, 112: transistor, 113: transistor, 114: capacitor, 115: transistor, 116: transistor, 117: circuit, 118: inverter, 120: memory cell, 121: memory element, 122: transistor, 123: transistor, 124: capacitor, 125: transistor, 129: region, 130: memory cell, 131: memory element, 132: transistor, 133: transistor, 134: capacitor, 135: transistor, 300: semiconductor memory device, 301: memory cell array, 302: column decoder, 303: row decoder, 304: interface circuit, 305: memory cell, 310: semiconductor memory device, 311: memory cell array, 312: memory cell array, 313: memory cell, 314: memory cell, 400: memory cell, 401: memory element, 402: transistor, 403: transistor, 404: capacitor, 405: transistor, 406: transistor, 502: transistor, 503: transistor, 504: capacitor, 505: transistor, 506: transistor, 508: substrate, 510: insulating layer, 512: insulating layer, 514: channel region, 516: low-concentration impurity region, 518: high-concentration impurity region, 519: semiconductor layer, 520: semiconductor layer, 522: gate insulating layer, 524: gate insulating layer, 526: gate electrode, 528: capacitor electrode, 530: sidewall insulating layer, 532: sidewall insulating layer, 534a: wiring, 534b: wiring, 534c: wiring, 534d: wiring, 534e: wiring, 534f: wiring, 536: insulating layer, 538: insulating layer, 540: insulating layer, 541: oxide semiconductor layer, 542: oxide semiconductor layer, 544: gate insulating layer, 546a: gate electrode, 546b: wiring, 552: insulating layer, 554: insulating layer, 601: transistor, 602: transistor, 603: capacitor, 611: resistor, 612: transistor, 613: capacitor, 614: resistor, 615: resistor, 800: measurement system, 802: capacitor, 802a: capacitor, 802b: capacitor, 802c: capacitor, 804: transistor, 805: transistor, 806: transistor, 808: transistor, 1520: RFID tag, 1521: antenna circuit, 1522: signal processing circuit, 1523: rectifier circuit, 1524: power supply circuit, 1525: demodulation circuit, 1526: oscillator circuit, 1527: logic circuit, 1528: memory control circuit, 1529: memory circuit, 1530: logic circuit, 1531: amplifier, 1532: modulation circuit, and 1581: battery.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/073903

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. See extra sheet

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2002-368226 A (SHARP CORPORATION) 2002.12.20, [0045]-[0054],Figs.5-8 (No Family)	1-20
A	JP 2007-103918 A (CANON KABUSHIKI KAISHA) 2007.04.19, [0157]-[0208],Fig.1 & US 2009/0045397 A1 & WO 2007/029844 A1 & KR 10-2008-0053355 A & CN 101258607 A	1-20
A	JP 2001-028443 A (HITACHI, LTD.) 2001.01.30, [0102],Fig.34 & US 2003/0209739 A1 & WO 2000/070683 A1 & TW 461096 B	4
A	JP 2008-042067 A (CANON KABUSHIKI KAISHA) 2008.02.21, [0025] & US 2008/0038929 A1 & CN 101123194 A	5,10,17

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01.04.2011	12.04.2011

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Yasuko YOSHIDA Telephone No. +81-3-3581-1101 Ext. 3462

4M 4494

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/073903

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 11-126491 A (FUJITSU LIMITED) 1999.05.11, [0003]-[0004],[0024],Fig.1 & US 5936881 A	9-20
A	JP 10-084092 A (KABUSHIKI KAISHA TOSHIBA) 1998.03.31, [0025]-[0027],Fig.6 & US 5978301 A & EP 828295 A2 & TW 445635 B	1-20
A	JP 2002-082656 A (HITACHI, LTD.) 2002.03.22, [0018]-[0019],Fig.2 & US 2002/0047826 A1 & KR 10-2002-0021312 A	1-20
A	JP 2002-538572 A (INFINEON TECHNOLOGIES AG) 2002.11.12, [0042],Fig.1 & US 2002/0075723 A1 & EP 1153394 A & WO 2000/051133 A1 & DE 50000728 D & TW 466489 B	1-20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/073903

CLASSIFICATION OF SUBJECT MATTER
H01L27/105(2006.01)i, G11C11/405(2006.01)i, G11C14/00(2006.01)i,
H01L21/8234(2006.01)i, H01L21/8242(2006.01)i, H01L21/8247(2006.01)i,
H01L27/08(2006.01)i, H01L27/088(2006.01)i, H01L27/108(2006.01)i,
H01L27/115(2006.01)i, H01L29/786(2006.01)i, H01L29/788(2006.01)i,
H01L29/792(2006.01)i

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/073903

Minimum documentation searched

H01L27/105, G11C11/405, G11C14/00, H01L21/8234, H01L21/8242, H01L21/8247, H01L27/08, H01L27/088, H01L27/108, H01L27/115, H01L29/786, H01L29/788, H01L29/792