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(54) Title: SEMICONDUCTOR DEVICE WITH THROUGH-SUBSTRATE VIA AND CORRESPONDING METHOD OF MANUFACTURE

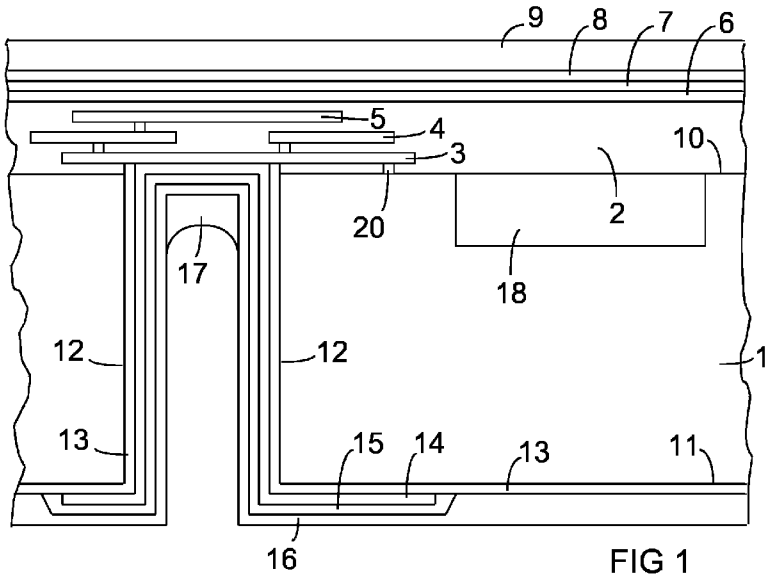


FIG 1

(57) Abstract: A dielectric layer (2) is arranged on the main surface (10) of a semiconductor substrate (1), and a passivation layer (6) is arranged on the dielectric layer. A metal layer (3) is embedded in the dielectric layer above an opening (12) in the substrate, and a metallization (14) is arranged in the opening. The metallization contacts the metal layer and forms a through- substrate via to a rear surface (11) of the substrate. A layer or layer sequence (7, 8, 9) comprising at least one further layer is arranged on the passivation layer above the opening. In this way the bottom of the through-substrate via is stabilized. A plug (17) may additionally be arranged in the opening without filling the opening.

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Description

SEMICONDUCTOR DEVICE WITH THROUGH-SUBSTRATE VIA AND CORRESPONDING METHOD OF MANUFACTURE

DE 10 2011 013 228 A1 discloses a manufacturing method for semiconductor devices. Two stop layers are arranged on a passivation layer above a semiconductor substrate. A handling wafer is applied and thinned until the upper stop layer is reached. The upper stop layer is then removed selectively with respect to the lower stop layer, which can be TiN or tungsten. The passivation layer and the lower stop layer cover an area above a through-substrate via.

WO 2012/031845 A1 discloses a manufacturing method for semiconductor devices with a through-substrate via. A metal plane embedded in a dielectric layer is arranged on a semiconductor substrate. A base substrate comprising a contact area on an insulated connection metal plane is connected to the semiconductor substrate. A contact hole is formed through the dielectric layer and the semiconductor substrate, and the contact area is thereby exposed. A metallization is applied to form a connection contact on the contact area and a through-contact in the contact hole.

If a through-silicon via is completely filled, it may be damaged by thermomechanical stress between the filler and the silicon owing to different coefficients of thermal expansion. For reference see the publication of M. Bouchoucha et. al., "Reliability Study of 3D-WLP Through Silicon Via with Innovative Polymer Filling Integration", 2011 IEEE 61st Electronic Components and Technology Conference, pp. 567-572.

It is an object of the present invention to disclose a semiconductor device with a through-substrate via of enhanced robustness. It is a further object to disclose a method of producing such a semiconductor device.

These objects are achieved with the semiconductor device according to claim 1 and with the method of producing a semiconductor device according to claim 15. Embodiments and variants derive from the dependent claims.

The semiconductor device comprises a substrate of semiconductor material. The substrate has a main surface, a rear surface opposite the main surface, and an opening penetrating the substrate between the main surface and the rear surface. A dielectric layer is arranged on the main surface, and a passivation layer is arranged on the dielectric layer. A metal layer is embedded in the dielectric layer above the opening, and a metallization is arranged in the opening. The metallization contacts the metal layer and forms a through-substrate via to the rear surface. A layer or layer sequence comprising at least one further layer is arranged on the passivation layer above the opening. The through-substrate via is not filled, so that an inner volume of the opening remains void or contains a gas like ambient air.

In an embodiment of the semiconductor device, the at least one further layer is a bond oxide layer.

In a further embodiment of the semiconductor device, the layer or layer sequence comprises at least two further layers.

In a further embodiment of the semiconductor device, a plug is arranged in the opening near the metal layer and partially fills the opening.

In a further embodiment the plug is a polymer.

In a further embodiment the plug is a photosensitive dielectric material.

In a further embodiment the layer or layer sequence comprises a further dielectric layer of a material different from the passivation layer. The further dielectric layer may be formed from an oxide of the semiconductor material.

In a further embodiment the layer or layer sequence comprises a filter layer, which may be formed from a material of an interference filter. In particular, the filter layer may comprise at least one combination of oxides selected from the group consisting of TiO_2/SiO_2, Nb_2O_5/SiO_2 and HfO/SiO_2.

A further embodiment comprises a sensor in the substrate, the sensor is provided for the detection of radiation, and the filter layer is arranged above the sensor.

In a further embodiment the layer or layer sequence comprises a protection coating.

In a further embodiment the protection coating comprises at least one material selected from the group consisting of benzocyclobutene, polybenzoxazoles, siloxane-based polymers or silicones, epoxies, polyimides, polynorbornenes and materials based on phenol resin.

In a further embodiment the protection coating comprises a photosensitive material or a photoresist.

In a further embodiment the protection coating is recessed above the opening.

The method of producing a semiconductor device comprises the steps of providing a substrate of semiconductor material having a main surface and a rear surface opposite the main surface, applying a dielectric layer and a metal layer embedded in the dielectric layer on the main surface, applying a passivation layer on the dielectric layer, forming an opening from the rear surface to the metal layer, and arranging a metallization in the opening, so that the metallization contacts the metal layer and forms a through-substrate via to the rear surface. A layer or layer sequence comprising at least one further layer is deposited on the passivation layer above the opening. The through-substrate via is not filled, so that an inner volume of the opening remains void or contains a gas like ambient air.

In a variant of the method, the opening is partially filled with a dielectric polymer.

In a further variant of the method the layer or layer sequence is applied including a protection coating, which is formed from a dielectric polymer and at least partially removed above the opening.

In a further variant of the method, a sensor provided for the detection of radiation is arranged in the substrate, the layer or layer sequence is applied including a filter layer formed from a material comprising at least one combination of oxides selected from the group consisting of TiO_2/SiO_2, Nb_2O_5/SiO_2 and HfO/SiO_2, and a protection coating above the filter layer. The protection coating is completely removed from an area above the sensor.

The following is a detailed description of examples of the semiconductor device and the method.

Figure 1 is a cross section of an embodiment of the semiconductor device comprising a filter layer and a protection coating over a partially filled through-substrate via.

Figure 2 is a cross section according to Figure 1 for an embodiment wherein the protection coating is open in an area above the through-substrate via.

Figure 3 is a cross section according to Figure 2 for an embodiment wherein the protection coating is only partially recessed above the through-substrate via.

Figure 4 is a cross section according to Figure 1 for an embodiment wherein upper layers are removed over an integrated sensor.

Figure 1 is a cross section of an embodiment of the semiconductor device, which comprises a substrate 1 of semiconductor material like silicon, for example. A dielectric layer 2 is arranged on or above a main surface 10 of the substrate 1. A metal layer 3 is embedded in the dielectric layer 2. Any number of further metal layers 4, 5 may also be embedded in the dielectric layer 2 as a wiring, and the dielectric layer 2 forms an intermetal dielectric. The metal layers 3, 4, 5 are structured and connected via vertical interconnects 20, which may be formed as metal plugs, for example. A passivation layer 6 is applied on the dielectric layer 2.

A layer or layer sequence comprising at least one further layer is arranged on the passivation layer 6. In the embodiment shown in Figure 1 as an example, the layer or layer sequence comprises a further dielectric layer 7, a filter layer 8 and a protection coating 9. These layers represent the layer or layer sequence in the appended figures as an example. The layer or layer sequence of further embodiments may differ by the number and/or the materials of the layers. In some embodiments at least one of the layers of the layer sequence comprises an oxide of the semiconductor material and may in particular be a bond oxide layer. In other embodiments none of the layers that are arranged above the passivation layer 6 comprises an oxide of the semiconductor material.

In the embodiment according to Figure 1, the further dielectric layer 7 comprises a material that is different from the passivation layer 6. The further dielectric layer 7 may be an oxide like silicon dioxide, for example, and may especially be a bond oxide used for the application of a handling wafer or the like during the manufacturing process. But the further dielectric layer 7 is optional and need not be applied even if a handling wafer is used, because the handling wafer may instead be bonded by a polymer layer, for example.

The filter layer 8 may be provided for an integrated sensor 18 detecting radiation like a photodetector, for example, and may be formed from a material of an interference filter. If a sensor 18 is integrated and a layer forming an interference filter is arranged above the sensor 18, this layer can thus serve to stabilize the through-substrate via as part of the layer sequence above the opening 12. In particular, the filter layer 8 may be formed as a stack of at least two layers of different indices of refraction and may especially comprise at least one oxide. Combinations of materials that are suitable

for the filter layer 8 are TiO_2/SiO_2, Nb_2O_5/SiO_2 or HfO/SiO_2, for example. The filter layer 8 has a typical thickness of a few micrometers up to about 10 µm, preferably a thickness in the range from 3 µm to 12 µm, for example. If the dielectric layer 7 is not present, the filter layer 8 may be arranged immediately on the passivation layer 6.

A further oxide layer, in particular a layer comprising an oxide that is also applied in the filter layer 8, may be applied above the filter layer 8, especially between the filter layer 8 and the protection coating 9. The further oxide layer is preferably thicker than the corresponding oxide layer of the filter layer 8.

The protection coating 9 may be a permanent dielectric polymer, for example. In particular, materials suitable for the protection coating 9 are benzocyclobutene (BCB), polybenzoxazoles (PBO), siloxane-based polymers or silicones, epoxies, polyimides, polynorbornenes and materials based on phenol resin. The protection coating 9 may especially be a photoresist, especially a UV-curable photoresist, which can be hardened by ultraviolet radiation, for example. Suitable photoresists are commercially available.

The layer sequence 7, 8, 9 may comprise other materials, and the number of layers may be varied. The materials can be selected with the aim of optimizing the robustness of the through-substrate via.

An opening 12 extends through the substrate 1 between the main surface 10 and the rear surface 11. A dielectric layer 13 is preferably provided to insulate the semiconductor material of the substrate 1 in the opening 12 and at the rear surface 11. A metallization 14 is arranged in the opening 12 so that the

metallization 14 contacts the metal layer 3 and forms a through-substrate via from the metal layer 3 to the rear surface 11. The metallization 14 may be covered by a dielectric layer 15, and a passivation layer 16 may be applied to the entire area of the rear surface 11. Contact areas of the metallization 14 can be uncovered to allow an external electrical connection. The through-substrate via is preferably not filled, so that an inner volume of the opening 12 remains void or contains a gas like ambient air.

A plug 17 can be arranged in the opening 12 near the metal layer 3 to stabilize the bottom of the through-substrate via. The plug 17 is preferably confined to a small volume near the metal layer 3. The plug 17 can be the same material as the protection coating 9, like a polymer, for example, in particular a photosensitive dielectric material, which is commercially available. As the opening 12 is not filled, thermomechanical stress is avoided. Otherwise stress might occur because of different coefficients of thermal expansion of the plug 17 and the semiconductor material, especially during thermal steps of the manufacturing process. A layer of photoresist may be applied to form the plug 17. If a portion of the photoresist layer is also applied over the rear surface 11, it is exposed to radiation, developed and removed, so that only the portion of the photoresist layer that is intended to form the plug 17 remains. The remaining portion of the photoresist layer is preferably cured, typically for one hour at 200°C, for example, to produce the plug 17.

Figure 2 is a cross section according to Figure 1 for a further embodiment. Elements of the embodiment according to Figure 2 that are similar to corresponding elements of the embodiment according to Figure 1 are designated with the same reference numerals. In the embodiment according to Figure 2,

the protection coating 9 is removed in an area 19 above the opening 12 of the through-substrate via and forms a recess 22. The further dielectric layer 7 and, optionally, the filter layer 8 or similar layers of different materials suffice to stabilize the bottom of the through-substrate via. The recess 22 of the protection coating 9 is intended to mitigate the accidental presence of small particles in the region above the opening 12. A small particle may transfer a force exerted by some manufacturing tool to the bottom of the through-substrate via and thus damage the electrical connection between the metal layer 3 and the metallization 14. If the particle enters the recess 22 and if the size of the particle does not exceed the thickness of the protection coating 9, which may typically be in the range from 15 µm to 30 µm, especially about 20 µm, for example, the particle will not protrude from the recess 22 and will not exceed the level of the upper surface plane of the protection coating 9. Consequently the particle is out of reach of a flat tool that is larger than the dimension of the recess 22 and therefore cannot transfer pressure to the bottom of the through-substrate via.

Figure 3 is a cross section according to Figure 2 for a further embodiment. Elements of the embodiment according to Figure 3 that are similar to corresponding elements of the embodiment according to Figure 2 are designated with the same reference numerals. In the embodiment according to Figure 3, the protection coating 9 is only partially removed in an area 19 above the opening 12 of the through-substrate via. Thus a thin layer portion of the protection coating 9 remains in the area 19, and a recess 22 is only formed within the protection coating 9. Hence the recess 22 is shallower than the recess 22 of the embodiment according to Figure 2. The shallow recess 22 still accomodates a particle of sufficiently small size, while the reinforcement of the bottom of the through-substrate via

is stronger than in the embodiment according to Figure 2. The depth of the recess 22 can be adapted to obtain an optimal compromise.

Figure 4 is a cross section according to Figure 1 for a further embodiment. Elements of the embodiment according to Figure 4 that are similar to corresponding elements of the embodiment according to Figure 1 are designated with the same reference numerals. In the embodiment according to Figure 4, a sensor 18 is integrated in the substrate 1. The layer or layer sequence 7, 8, 9 is at least partially recessed in an area 21 above the sensor 18. This embodiment may be especially suitable if an opaque material or materials that are not transparent for the radiation that is to be detected by the sensor 18 are used in the layer or layer sequence 7, 8, 9. Some or all of the opaque layers are removed from the sensor area 21. If a filter layer 8 is provided for the sensor 18, the layers arranged above the filter layer 8, in particular the protection coating 9, can be removed above the sensor 18 to enhance the incidence of radiation.

This invention allows to improve the robustness of the membrane formed by the bottom region of a through-substrate via and to enhance the resistance against the action of an external mechanical force on the membrane. One or more additional layers on top of the through-substrate via, in particular on the side where circuit components like CMOS components are integrated in the semiconductor device, and a partial filling inside the through-substrate via provide a mechanical and thermomechanical reinforcement. Embodiments are additionally provided with cavities created over the through-substrate via in order to prevent particles from pushing onto the membrane.

List of reference numerals

1	substrate
2	dielectric layer
3	metal layer
4	further metal layer
5	further metal layer
6	passivation layer
7	further dielectric layer
8	filter layer
9	protection coating
10	main surface
11	rear surface
12	opening
13	dielectric layer
14	metallization
15	dielectric layer
16	passivation layer
17	plug
18	sensor
19	area above the opening
20	vertical interconnect
21	area above the sensor
22	recess

Claims

1. A semiconductor device, comprising:
- a substrate (1) of semiconductor material with a main surface (10), a rear surface (11) opposite the main surface (10), and an opening (12) through the substrate (1) between the main surface (10) and the rear surface (11),
- a dielectric layer (2) on the main surface (10),
- a passivation layer (6) on the dielectric layer (2),
- a metal layer (3) embedded in the dielectric layer (2) above the opening (12), and
- a metallization (14) arranged in the opening (12), the metallization (14) contacting the metal layer (3) and forming a through-substrate via to the rear surface (11),

characterized in that
- a layer or layer sequence (7, 8, 9) comprising at least one further layer is arranged on the passivation layer (6) above the opening (12), and
- the through-substrate via is not filled, so that an inner volume of the opening (12) remains void or contains a gas like ambient air.

2. The semiconductor device of claim 1, wherein the at least one further layer (7) is a bond oxide layer.

3. The semiconductor device of claim 1 or 2, wherein the layer or layer sequence (7, 8, 9) comprises at least two further layers.

4. The semiconductor device of one of claims 1 to 3, further comprising a plug (17) partially filling the opening (12), the plug (17) being arranged near the metal layer (3) and the opening (12) not being filled.

5. The semiconductor device of claim 4, wherein the plug (17) is a polymer.

6. The semiconductor device of claim 4, wherein the plug (17) is a photosensitive dielectric material.

7. The semiconductor device of one of claims 1 to 6, wherein the layer or layer sequence (7, 8, 9) comprises a further dielectric layer (7) of a material different from the passivation layer (6).

8. The semiconductor device of one of claims 1 to 7, wherein the layer or layer sequence (7, 8, 9) comprises a filter layer (8).

9. The semiconductor device of claim 8, wherein the filter layer (8) comprises at least one combination of oxides selected from the group consisting of TiO_2/SiO_2, Nb_2O_5/SiO_2 and HfO/SiO_2.

10. The semiconductor device of claim 8 or 9, further comprising a sensor (18) in the substrate (1), the sensor (18) being provided for the detection of radiation, and the filter layer (8) being arranged above the sensor (18).

11. The semiconductor device of one of claims 1 to 10, wherein the layer or layer sequence (7, 8, 9) comprises a protection coating (9).

12. The semiconductor device of claim 11, wherein the protection coating (9) comprises at least one material selected from the group consisting of benzocyclobutene, polybenzoxazoles, siloxane-based polymers or silicones,

epoxies, polyimides, polynorbornenes and materials based on phenol resin.

13. The semiconductor device of claim 11, wherein the protection coating (9) comprises a photosensitive material or a photoresist.

14. The semiconductor device of one of claims 11 to 13, wherein the protection coating (9) is recessed above the opening (12).

15. A method of producing a semiconductor device, comprising:

- providing a substrate (1) of semiconductor material having a main surface (10) and a rear surface (11) opposite the main surface (10)
- applying a dielectric layer (2) and a metal layer (3) embedded in the dielectric layer (2) on the main surface (10)
- applying a passivation layer (6) on the dielectric layer (2),
- forming an opening (12) from the rear surface (11) to the metal layer (3), and
- arranging a metallization (14) in the opening (12), the metallization (14) contacting the metal layer (3) and forming a through-substrate via to the rear surface (11),

characterized in that

- a layer or layer sequence (7, 8, 9) comprising at least one further layer is deposited on the passivation layer (6) above the opening (12), and
- the through-substrate via is not filled, so that an inner volume of the opening (12) remains void or contains a gas like ambient air.

16. The method of claim 15, further comprising:
partially filling the opening (12) with a dielectric polymer, the opening (12) not being filled.

17. The method of claim 15 or 16, wherein the layer or layer sequence (7, 8, 9) includes a protection coating (9), which is formed from a dielectric polymer and at least partially removed above the opening (12).

18. The method of claim 15 or 16, further comprising:
arranging a sensor (18) provided for the detection of radiation in the substrate (1),
wherein the layer or layer sequence (7, 8, 9) includes a filter layer (8) comprising at least one combination of oxides selected from the group consisting of TiO_2/SiO_2, Nb_2O_5/SiO_2 and HfO/SiO_2, and a protection coating (9) above the filter layer (8), the protection coating (9) being removed from an area (21) above the sensor (18).

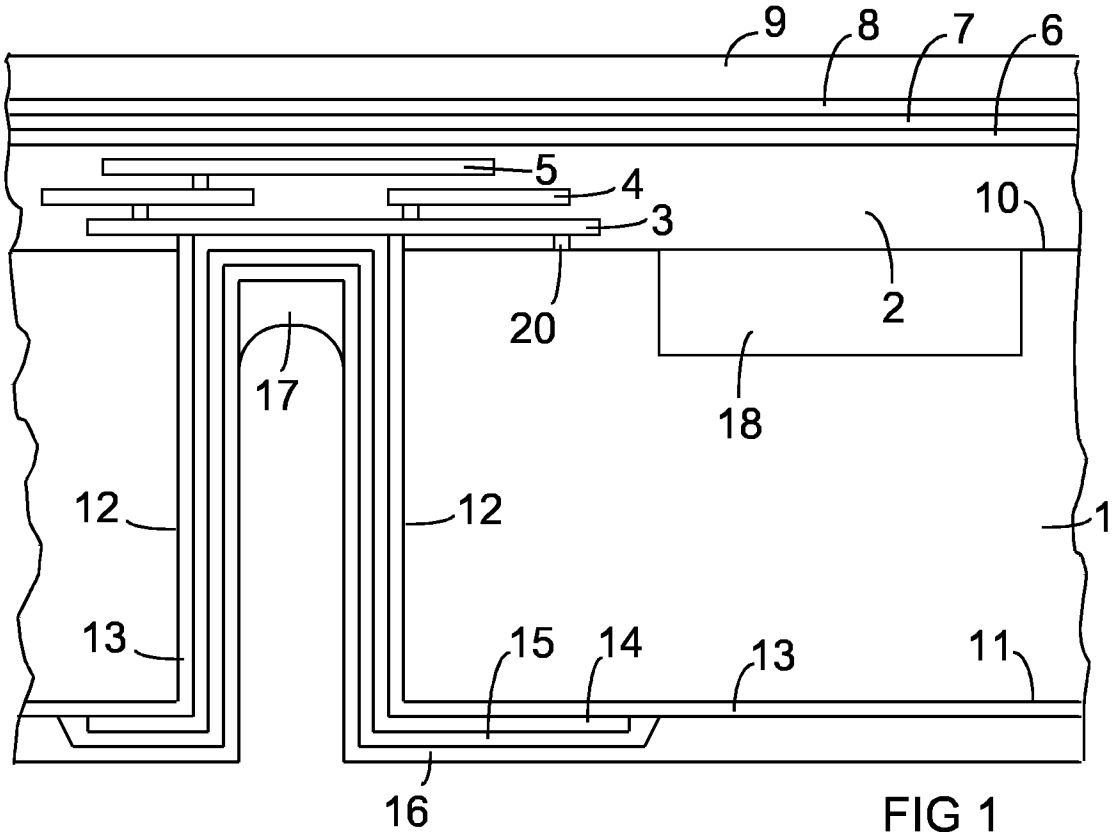

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FIG 1

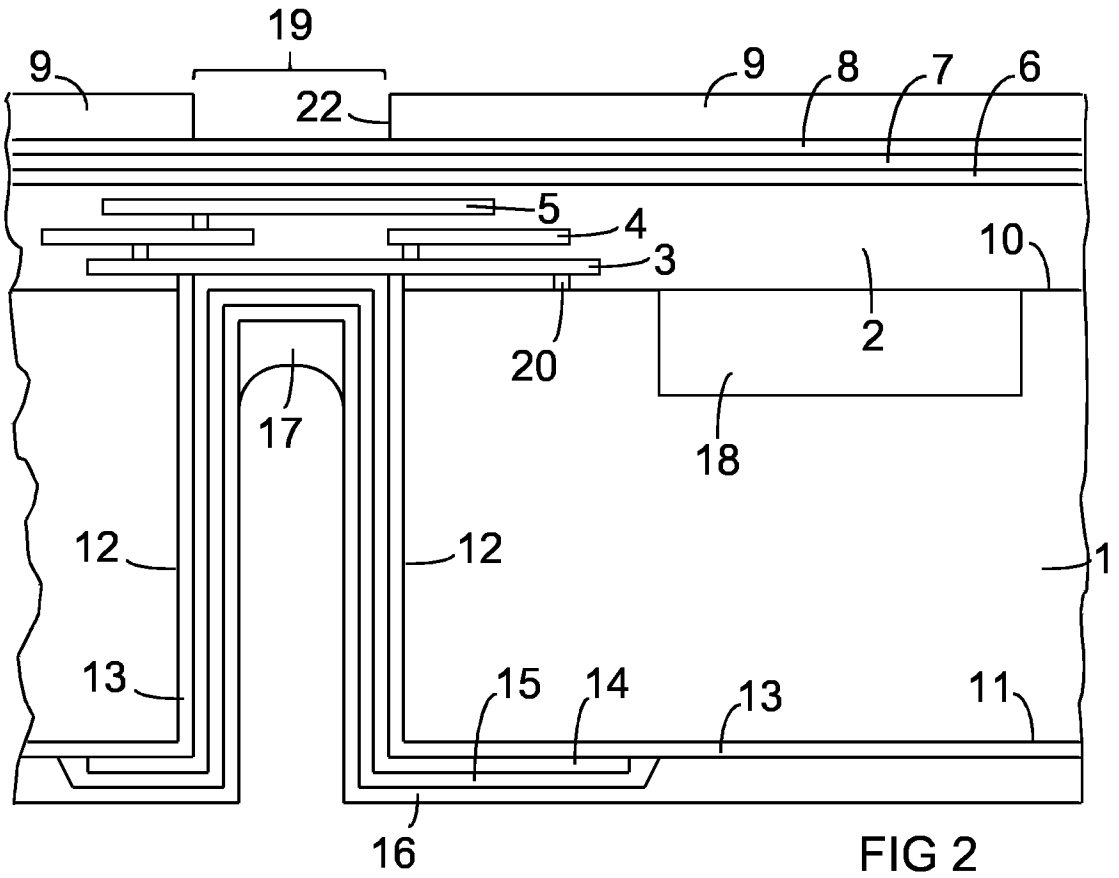

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FIG 2

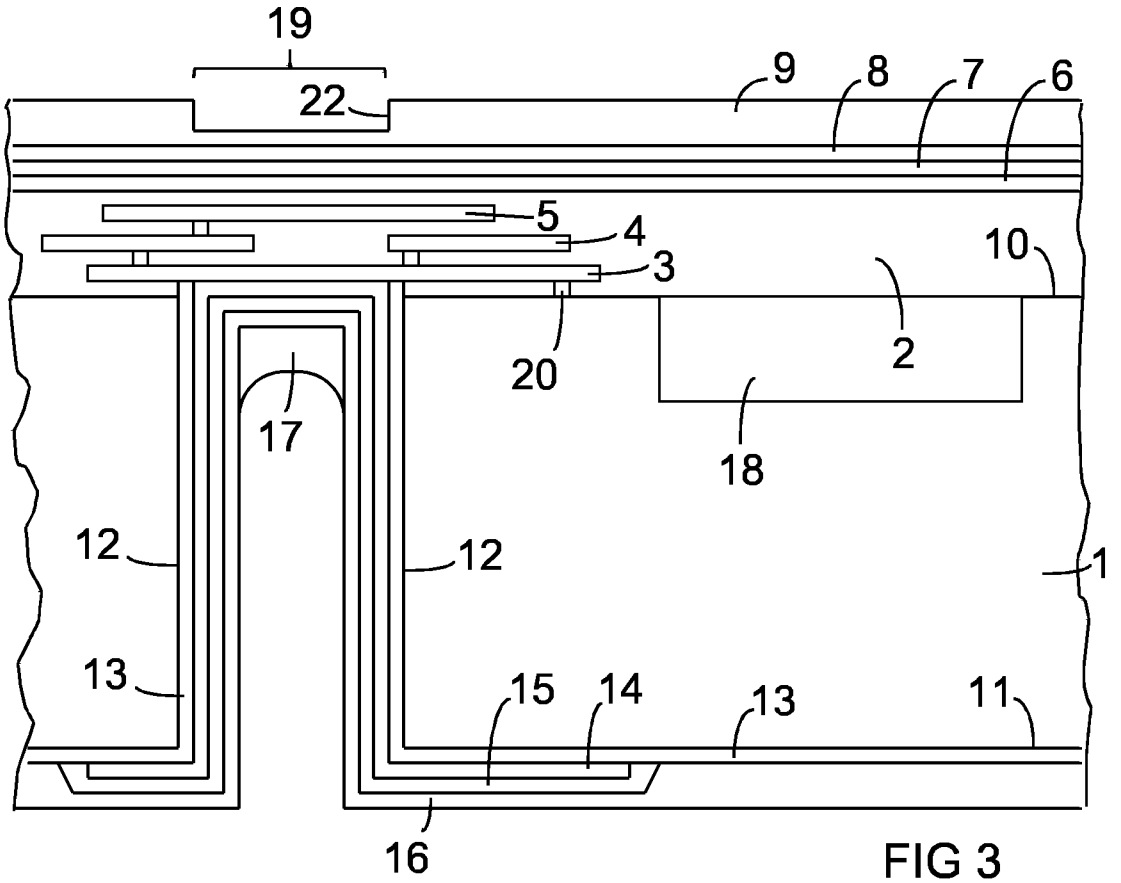

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FIG 3

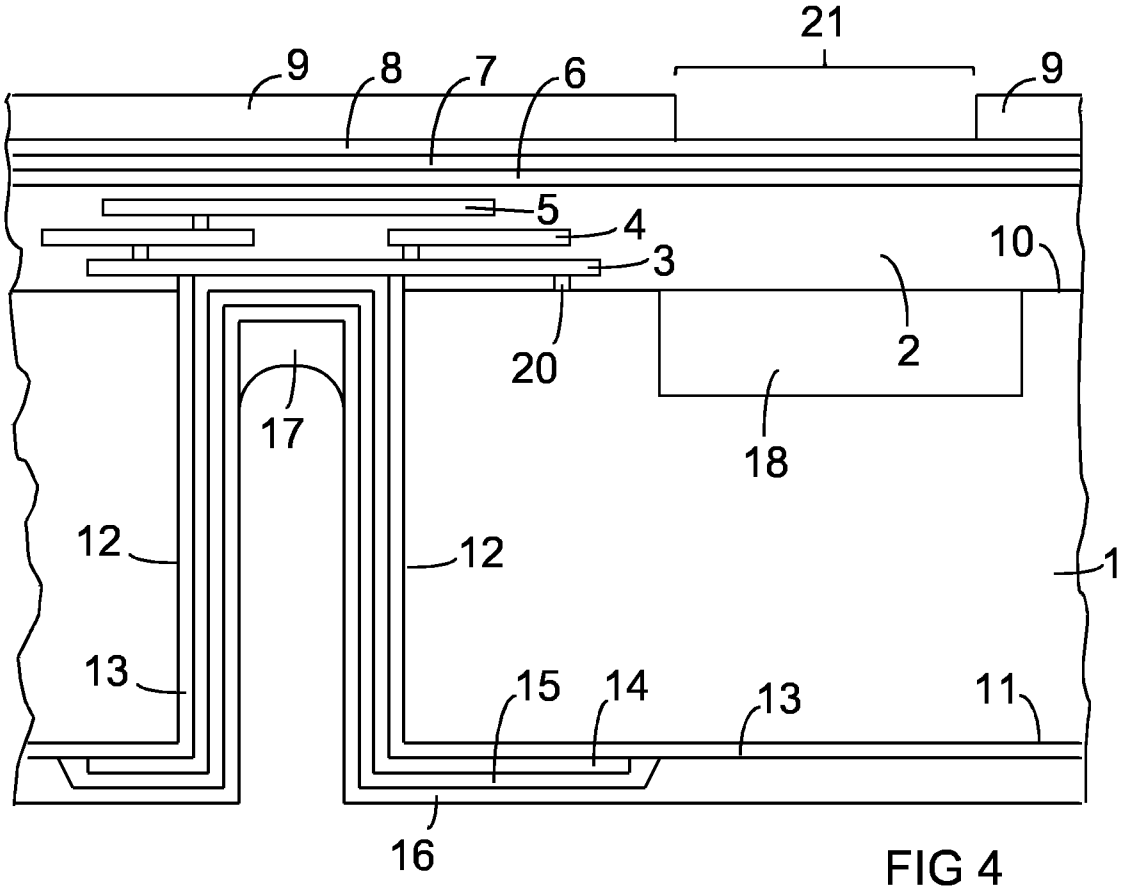

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FIG 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/077587

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/768 H01L23/48 H01L27/146
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/327383 A1 (HAYASAKI YUKO [JP] ET AL) 30 December 2010 (2010-12-30)	1,3,4, 7-12, 14-18
Y	paragraphs [0022] - [0071]; figures 2-13	13
X	US 2009/302480 A1 (BIRNER ALBERT [DE] ET AL) 10 December 2009 (2009-12-10)	1-4,7,11
A	paragraphs [0027] - [0039]; figures 1a, 2a	15-18
X	US 2002/019069 A1 (WADA KENJI [JP]) 14 February 2002 (2002-02-14)	1,4-6, 11,12
A	paragraphs [0071] - [0079], [0123] - [0126]; figures 1, 9	15-18

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 April 2015	22/04/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ploner, Guido

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 10 2011 013228 A1 (AUSTRIAMICROSYSTEMS AG [AT]) 13 September 2012 (2012-09-13) cited in the application paragraphs [0030] - [0045]; figures 6, 11, 12	1-3,7, 11,15
Y	US 2010/321544 A1 (MATSUO MIE [JP] ET AL) 23 December 2010 (2010-12-23) paragraph [0056]; figure 4B	13
A	US 2011/169139 A1 (LIN CHIA-SHENG [TW] ET AL) 14 July 2011 (2011-07-14) paragraphs [0015] - [0021]; figure 1	1-18

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2014/077587

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010327383 A1	30-12-2010	CN 101937894 A	05-01-2011
		JP 2011009645 A	13-01-2011
		TW 201117346 A	16-05-2011
		US 2010327383 A1	30-12-2010
US 2009302480 A1	10-12-2009	DE 102009012594 A1	24-12-2009
		US 2009302480 A1	10-12-2009
		US 2010230818 A1	16-09-2010
		US 2013267093 A1	10-10-2013
US 2002019069 A1	14-02-2002	CN 1333570 A	30-01-2002
		JP 2002094082 A	29-03-2002
		US 2002019069 A1	14-02-2002
		US 2004147051 A1	29-07-2004
		US 2006208331 A1	21-09-2006
		US 2008009087 A1	10-01-2008
		US 2009221108 A1	03-09-2009
DE 102011013228 A1	13-09-2012	NONE	
US 2010321544 A1	23-12-2010	CN 101930986 A	29-12-2010
		JP 5150566 B2	20-02-2013
		JP 2011003863 A	06-01-2011
		TW 201117345 A	16-05-2011
		US 2010321544 A1	23-12-2010
US 2011169139 A1	14-07-2011	NONE	