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[Continued on next page]

(54) Title: TRANSITION TIME LOCK LOOP WITH REFERENCE ON REQUEST

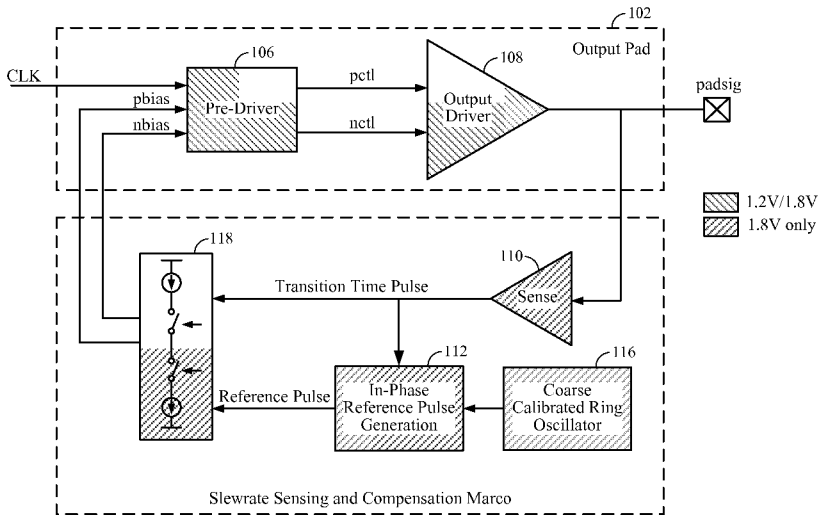

FIG. 1A

(57) Abstract: Output driver feedback circuitry limits output slew rates across a wide range of output loads. A transition time lock loop architecture of the feedback circuitry compares a transition time pulse with a reference pulse to adjusts transition time of an output signal for various process-voltage-temperature (PVT) process corners, output voltage domains and output capacitances. Reference pulse generation circuitry provides a reference pulse in phase with the transition time pulse for each rise and fall of the output signal.

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TRANSITION TIME LOCK LOOP WITH REFERENCE ON REQUEST

CROSS REFERENCE TO RELATED APPLICATION

[0001] The present application claims the benefit of U.S. Provisional Patent Application No. 61/588,717 to Chen et al. filed on January 20, 2012.

TECHNICAL FIELD

[0002] The present disclosure relates generally to semiconductor output driver circuitry. More specifically, the present disclosure relates to controlling the transition time of an output from semiconductor output driver circuitry.

BACKGROUND

[0003] Integrated circuit design specifications generally include limits for the transition times and slew rates of output signals. For example, recent Mobile Industry Processor Interface (MIPI) input/output (I/O) interface standards, such as Serial Low-power Inter-chip Media Bus (SLIMBus), have called for limited output slew rates across a very wide range of output loads (e.g., 15pF-75pF) and across process, voltage and temperature (PVT) variations. Such standards also call for multiple output voltage modes.

[0004] Variations in the load capacitance coupled to output circuitry on an integrated circuit chip affect the slew rates and transition times of the output signals. Output interface circuitry on a chip may include capacitive feedback, which compensates for some variations in load capacitance but may not be capable of meeting tight transition time specifications. For interfaces that are designed to provide a limited output slew rate across a very wide range of output capacitive loads, general purpose input/output (GPIO) circuitry may not be able to provide output signals that satisfy the transition time requirements, even if such circuitry includes output drivers with capacitive feedback.

[0005] Because of the continued rapid scaling of complementary metal oxide semiconductor (CMOS) technology, the use of off-chip components is becoming more expensive. Compensation techniques that involve off-chip calibration are therefore increasingly expensive to implement. Thus, the use

of off-chip components is generally limited to applications that rely on highly accurate delay calibration. Even presently known off-chip calibration techniques may not be effective to compensate for very wide variations in output load capacitance.

SUMMARY

[0006] Aspects of the present disclosure include feedback circuitry configured to provide limited output slew rates across a wide range of output loads. The feedback circuitry locks output transition time regardless of the PVT process corner, the output voltage domain or the output capacitance. The feedback circuit may provide sufficient adjustment of the output driver within a single cycle in which the output capacitance is not expected to change much over time.

[0007] An output driver time lock loop apparatus, according to an aspect of the present disclosure, includes output driver circuitry coupled between a first output node and a second output node and feedback circuitry coupled to the output driver circuitry. The feedback circuitry is configured to generate a first analog bias voltage in response to a signal on the second output node. The output driver circuitry includes a first current source biased by the first analog bias voltage.

[0008] A method for locking output transition timing of interface circuitry, according to an aspect of the present disclosure, includes generating a first transition time pulse having a pulse width equal to a characteristic of an output driver output and generating a reference pulse having a pulse width equal to a desired signal characteristic. The method also includes generating a first analog bias voltage in response to a difference between the first transition time pulse width and the reference pulse width, and biasing a first pre-driver current source with the first analog bias voltage.

[0009] An apparatus for locking output transition timing of interface circuitry, according to an aspect of the present disclosure, includes means for generating a first transition time pulse having a pulse width equal to a characteristic of an output driver output and means for generating a reference pulse having a pulse

width equal to a desired signal characteristic. The apparatus also includes means for generating a first analog bias voltage in response to a difference between the first transition time pulse width and the reference pulse width and means for biasing a first pre-driver current source with the first analog bias voltage.

[00010] This has outlined, rather broadly, the features and technical advantages of the present disclosure in order that the detailed description that follows may be better understood. Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[00011] The features, nature, and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout.

[00012] FIGURE 1A is a schematic diagram conceptually illustrating a general example of interface circuitry according to aspects of the present disclosure.

[00013] FIGURE 1B is a schematic diagram conceptually illustrating a general example of reference pulse generation circuitry according to aspects of the present disclosure.

[00014] FIGURE 2 is schematic diagram conceptually illustrating output pre-driver current source circuitry according to aspects of the present disclosure.

[00015] FIGURE 3 is schematic diagram conceptually illustrating sensor circuitry according to aspects of the present disclosure

[00016] FIGURE 4 is a schematic diagram conceptually illustrating a general example of bias generating circuitry according to aspects of the present disclosure.

[00017] FIGURE 5 is a signal timing diagram conceptually illustrating the operation of bias generating circuitry according to aspects of the present disclosure.

[00018] FIGURE 6 is schematic diagram conceptually illustrating timing according to aspects of the present disclosure

[00019] FIGURE 7 is a process flow diagram illustrating a reference pulse generating technique according to an aspect of the present disclosure.

[00020] FIGURE 8 shows an exemplary wireless communication system in which a configuration of the disclosure may be advantageously employed.

[00021] FIGURE 9 is a block diagram illustrating a design workstation for circuit, layout, and logic design of a semiconductor component according to one aspect of the present disclosure.

DETAILED DESCRIPTION

[00022] FIGURE 1A shows a top level block diagram of a design architecture including circuitry 100 for locking output transition time according to aspects of the present disclosure. The circuitry 100 includes output pad circuitry 102 and slew rate sensing and compensation circuitry 104. According to aspects of the present disclosure, the output pad circuitry 102 is configured to support multiple output voltage domains. The output pad circuitry 102 includes a pre-driver 106 coupled to an output driver 108.

[00023] According to aspects of the present disclosure, slew rate sensing and compensation circuitry 104 is coupled in a feedback loop from an output node of the output driver 108 to inputs of the pre-driver 106. The slew rate sensing and compensation circuitry 104 includes sense circuitry 110 and in-phase

reference pulse generation circuitry 112 coupled to bias generating circuitry 114. The slew rate sensing and compensation circuitry 104 also includes coarse calibrated ring oscillator circuitry 116 coupled to the in-phase reference pulse generation circuitry 112.

[00024] According to aspects of the present disclosure, two analog voltages (pbias and nbias) are generated by a bias generation circuitry 118 within the slew rate sensing and compensation circuitry 104. The bias generation circuitry 118 provides the voltages to the output pad circuitry 102 in response to input from the sense circuitry 110 and the in-phase reference pulse generation circuitry 112. The output pad circuitry 102 uses the two analog voltages to adjust output transition time towards the target. The two analog voltages (pbias and nbias) are used to bias current sources in the pre-driver 106. The slew rate sensing and compensation circuitry 104 operates at one voltage, e.g., 1.8 V, while the output pad circuitry 102 operates at two different voltages, e.g., 1.2V and 1.8V.

[00025] Referring to FIGURE 2, one of the analog voltages (pbias) is applied to a first current source 202 and the other analog voltage (nbias) is applied to a second current source 204. The analog voltages control the amount of current in the pre-driver 106. By controlling the amount of current in the pre-driver 106 the slew rate of the pre-driver 106 and the output slew rate are also controlled by the analog voltages pbias and nbias. Further, by biasing current sources in the pre-driver 106 according to aspects of the present disclosure instead of biasing the output driver 108 directly, the use of a stacked output driver design, which could consume up to 75% more area, is avoided.

[00026] Referring to FIGURE 3, exemplary sensor circuitry is described. The sensor circuitry 110 includes a pair of comparators 302, 304 coupled to digital logic circuitry 306. To generate the correct pbias and nbias for the pre-driver, the comparators 302, 304 and digital logic circuitry 306 first sense the current output transition time of the output driver 108 and convert the transition time into a digital pulse. A first reference voltage is applied to a first one of the comparators 302 and a second reference voltage is applied to a second one of the comparators 304. In one example, the first reference voltage is 0.2 times

the current source supply voltage (vddpx) and the second reference voltage is 0.8 times the current source supply voltage (vddpx). The first reference voltage and second reference voltage can be generated by a resistor divider.

[00027] The comparators 302, 304 compare the present output of the output driver 108 with the reference voltages, and convert the 20%-80% rise time (hereinafter "rise time") of the output and 80%-20% fall time (hereinafter "fall time) of the output into a respective digital pulse with a pulse width that is the same as the corresponding rise time or fall time. According to aspects of the disclosure, such a transition time pulse is generated every time the pad output rises and falls.

[00028] Referring to FIGURE 4, exemplary bias generation circuitry is described. In the bias generation circuitry 118, the transition time pulse is compared with a reference pulse having a pulse width equal to the desired rise/fall time. According to aspects of the disclosure, comparison of the transition time pulse and the reference pulse is performed by XOR circuitry 402.

[00029] The bias generating circuitry 118 includes a charge pump 404 coupled to the XOR circuitry 402. The charge pump circuitry 404 adjusts one of the analog bias voltages for the pre-driver 106, i.e., either pbias or nbias, based on the output of the XOR circuitry 402 until the transition time pulse has the same pulse width as the reference pulse. This condition occurs when the output transition time at padsig is the same as the pulse width of the reference pulse. For transition time pulses corresponding to a fall time of the output, the charge pump circuitry 404 adjusts the pbias analog voltage. For transition time pulses corresponding to a rise time of the output, the charge pump circuitry 404 adjusts the nbias analog voltage.

[00030] The operation of the bias generation circuitry 118 is further described with reference to FIGURE 5. During a rising output 502 from the output driver 108, a transition time pulse 504 is generated by the sense circuitry 110. The width of the transition time pulse 504 corresponds to the rise time of the output from 20% of the supply voltage (vddpx) to 80% of the supply voltage

(vddpx) (using the exemplary 20% and 80% voltages described above). The pulse width of the transition time pulse 504 is independent of the supply voltage (vddpx). In response to the difference between the width of the transition time pulse 504 and the width of a reference pulse 506, the nbias analog voltage 508 is adjusted.

[00031] During a falling output 512 from the output driver 108, a transition time pulse 514 is generated by the sense circuitry 110. The width of the transition time pulse 514 corresponds to the fall time of the output from 80% of the supply voltage (vddpx) to 20% of the supply voltage (vddpx) (again using the exemplary 20% and 80% voltages described above). In response to the difference between the width of the transition time pulse 514 and the width of a reference pulse 516, the pbias analog voltage 518 is adjusted. In this example, the rise/fall time was too fast so the analog bias voltages, pbias and nbias, are adjusted to increase the rise/fall time in the next transition.

[00032] Aspects of the present disclosure include circuitry for generating the reference pulse that has a pulse width equal to the desired rise/fall time. A predefined clock reference is not suitable for providing the reference pulse according to the present disclosure because a predefined clock would not follow the operation frequency of the output and would not provide a pulse whenever a rise or fall of the output occurs. In addition, even if the frequency of a predefined clock reference could be adjusted to follow the output frequency, the clock pulse reference may not be in phase with the transition time pulse and may cause a glitch which could severely impact the final locked output transition time.

[00033] According to aspects of the present disclosure, the reference pulse is generated based on the actual rise/fall time of the output using ring oscillator circuitry 116. The ring oscillator circuitry 116 is suitable for use in the disclosed architecture because the in-phase reference pulse generation circuitry 112 does not rely on a highly accurate oscillation frequency. For example, a suitable reference pulse can be generated using ring oscillator circuitry 116 as long as the pulse width of the ring oscillator circuitry outputs is within the transition time targets. In accordance with SLIMBus standards,

for example, the transition time targets are 3.0 ns – 5.3 ns so oscillation frequencies in the range of 95 MHz – 167 MHz may be used to generate the reference pulses. A coarse delay calibration can calibrate the ring oscillator circuitry to achieve the targeted frequency range across process corners.

[00034] A more detailed block diagram of the in-phase reference pulse generation circuitry 112 is now described with reference to FIGURES 1A and 1B. The in-phase reference pulse generation circuitry 112 includes a set of pulse samplers 119 coupled to the ring oscillator circuitry 116. Each pair of consecutive outputs from the ring oscillator circuitry 116 is connected to one of the pulse samplers 119. In addition, each of the pulse samplers 119 also receives a transition time pulse from the sensing circuitry 110.

[00035] According to aspects of the present disclosure, each pulse sampler 119 can individually determine whether to generate a reference pulse based on the pair of consecutive outputs from the ring oscillator circuitry 116 and the transition time pulse from the sensing circuitry 110. In one aspect of the disclosure, a sufficient number of the pulse samplers 119 can be provided to cover all the outputs from the ring oscillator (phase of 2π). In this aspect, only one pulse sampler 119 is activated at a time to generate a reference pulse. The pulse selector circuitry 120 selects the activated pulse sampler 119 and feeds the reference pulse to the bias generating circuitry 118.

[00036] A method of generating the reference pulse using ring oscillator circuitry 116 according to aspects of the present disclosure is described with reference to FIGURE 6. Ring oscillator circuitry 116 provides a first phase output 602 and consecutively provides a second phase output 604. If the transition time pulse 606 occurs between the first phase output 602 and the second phase output 604, generation of a reference pulse is triggered. The rising edge of the transition time pulse 606 is used as the rising edge of the reference pulse 608 and the falling edge of the first phase output 602 from the ring oscillator circuitry 116 is used as the falling edge of the reference pulse. This process is repeated to generate a new reference pulse for every rise and fall at the pad output. The generated reference pulse has a slightly smaller pulse width than the ring oscillator output, but it is acceptably accurate for

implementing the transition time lock loop architecture of the present disclosure. For implementation in which increased accuracy is desired, additional delay stages can be added to the ring oscillator circuitry 116 to reduce the delay between the first phase output 602 and the second phase output 604.

[00037] A method for locking output transition time of interface circuitry according to an aspect of the present disclosure is described with reference to FIGURE 7. In block 702, a first transition time pulse having a pulse width equal to a rise/fall time of an output driver output is generated. In block 704, a reference pulse having a pulse width equal to a desired rise/fall time is generated. In block 706, a first analog bias voltage is generated in response to a difference between the first transition time pulse width and the reference pulse width. In block 708, a first pre-driver current source is biased with the first analog bias voltage.

[00038] In one configuration, an apparatus for locking output transition timing of interface circuitry includes means for generating a first transition time pulse. The means for generating a first transition time pulse may be the sensor circuitry 110, for example. The apparatus may include means, such as the in-phase reference pulse generation circuitry 112, for generating a reference pulse. The apparatus may also include means, for example the bias generation circuitry 118, for generating a first analog bias voltage. The apparatus may also have means for biasing a first pre-driver current source. In one configuration, the biasing means may be the pre-driver 106. In another configuration, the aforementioned means may be any module or any apparatus configured to perform the functions recited by the aforementioned means. Although specific means have been set forth, it will be appreciated by those skilled in the art that not all of the disclosed means are required to practice the disclosed configurations. Moreover, certain well known means have not been described, to maintain focus on the disclosure.

[00039] FIGURE 8 shows an exemplary wireless communication system 800 in which a configuration of the disclosed calibration method may be advantageously employed. For purposes of illustration, FIGURE 8 shows

three remote units 820, 830, and 850 and two base stations 840. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 820, 830, and 850 include the timing locking circuitry 825A, 825B, and 825C, respectively. FIGURE 8 shows forward link signals 880 from the base stations 840 and the remote units 820, 830, and 850 and reverse link signals 890 from the remote units 820, 830, and 850 to base stations 840.

[00040] In FIGURE 8, the remote unit 820 is shown as a mobile telephone, remote unit 830 is shown as a portable computer, and remote unit 850 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be cell phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, or fixed location data units such as meter reading equipment. Although FIGURE 8 illustrates remote units, which may employ timing locking circuitry according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. For instance, timing locking circuitry according to configurations of the present disclosure may be suitably employed in any device.

[00041] FIGURE 9 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component, such as the timing locking circuitry disclosed above. A design workstation 900 includes a hard disk 901 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 900 also includes a display 902 to facilitate design of a circuit 910 or a semiconductor component 912 such as the timing locking circuitry. A storage medium 904 is provided for tangibly storing the circuit design 910 or the semiconductor component 912. The circuit design 910 or the semiconductor component 912 may be stored on the storage medium 904 in a file format such as GDSII or GERBER. The storage medium 904 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 900 includes a drive apparatus 903 for accepting input from or writing output to the storage medium 904.

[00042] Data recorded on the storage medium 904 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 904 facilitates the design of the circuit design 910 or the semiconductor component 912 by decreasing the number of processes for designing semiconductor wafers.

[00043] Although specific circuitry has been set forth, it will be appreciated by those skilled in the art that not all of the disclosed circuitry is required to practice the disclosed configurations. Moreover, certain well known circuits have not been described, to maintain focus on the disclosure.

[00044] For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. A machine-readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software codes may be stored in a memory and executed by a processor unit. Memory may be implemented within the processor unit or external to the processor unit. As used herein the term "memory" refers to types of long term, short term, volatile, nonvolatile, or other memory and is not to be limited to a particular type of memory or number of memories, or type of media upon which memory is stored.

[00045] If implemented in firmware and/or software, the functions may be stored as one or more instructions or code on a computer-readable medium. Examples include computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be an available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or other medium that can be used to store desired program code in the form of instructions or data structures and

that can be accessed by a computer; disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[00046] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[00047] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular configurations of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding configurations described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

1. An output driver time lock loop apparatus comprising:

output driver circuitry coupled between a first output node and a second output node;

feedback circuitry coupled to the output driver circuitry, the feedback circuitry configured to generate a first analog bias voltage in response to a signal on the second output node;

the output driver circuitry including a first current source biased by the first analog bias voltage.

2. The output driver time lock loop apparatus of claim 1, in which the feedback circuitry generates the first analog bias voltage in response to a fall time of the signal.

3. The output driver time lock loop apparatus of claim 2, in which the feedback circuitry is further configured to generate a second analog bias voltage in response to a rise time of the signal on the second output node,

the output driver circuitry further including a second current source biased by the second analog bias voltage.

4. The output driver time lock loop apparatus of claim 1, in which the feedback circuitry comprises:

sensing circuitry coupled to the second output node, the sensing circuitry configured for sensing a first characteristic of the signal on the second output node;

reference pulse generation circuitry configured to generate a reference pulse having a pulse width equal to a desired signal characteristic; and

charge pump circuitry coupled to the sensing circuitry and coupled to the reference pulse generation circuitry, the charge pump circuitry configured to generate the first analog bias voltage in response to the first characteristic and the reference pulse.

5. The output driver time lock loop apparatus of claim 4, in which the sensing circuitry further comprises:

a first comparator configured for comparing the signal on the second output node with a high threshold voltage to generate a high signal voltage indication;

a second comparator configured for comparing the signal on the second output node with a low threshold voltage to generate a low signal voltage indication; and

digital logic circuitry coupled to an output of the first comparator and an output of the second comparator, the digital logic circuitry configured to output a transition time pulse having a width equal to a rise time between the low signal voltage indication and the high signal voltage indication when the signal on the second output node is rising and having a pulse width equal to a fall time between the high signal voltage indication and the low signal voltage indication when the signal on the second output node is falling.

6. The output driver time lock loop apparatus of claim 4, in which the reference pulse generation circuitry further comprises:

a chain of inverting stages configured as a ring oscillator;

a plurality of pulse samplers coupled to the ring oscillator, each of the pulse samplers receiving the transition time pulse and receiving input from a pair of consecutive inverting stages in the chain of inverting stages; each pulse sampler configured to trigger generation of the reference pulse when a rising edge of the transition time pulse is received between the input from the pair of consecutive inverting stages.

7. The output driver time lock loop apparatus of claim 1, integrated in at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

8. A method for locking output transition timing of interface circuitry, comprising:

generating a first transition time pulse having a pulse width equal to a characteristic of an output driver output;

generating a reference pulse having a pulse width equal to a desired signal characteristic;

generating a first analog bias voltage in response to a difference between a first transition time pulse width and the reference pulse width; and

biasing a first pre-driver current source with the first analog bias voltage.

9. The method of claim 8, in which the characteristic of the output driver output comprises a rise time.

10. The method of claim 9, further comprising:

generating a second transition time pulse having a pulse width equal to a fall time of the output driver output;

generating a second analog bias voltage in response to a difference between a second transition time pulse width and the reference pulse width; and

biasing a second pre-driver current source with the second analog bias voltage.

11. The method of claim 10, further comprising:

comparing the output driver output with a high threshold voltage to generate a high signal voltage indication;

comparing the output driver output with a low threshold voltage to generate a low signal voltage indication;

generating the first transition time pulse when the output driver output is rising between the low signal voltage indication and the high signal voltage indication; and

generating the second transition time pulse when the output driver output is falling between the high signal voltage indication and the low signal voltage indication.

12. The method of claim 10, in which generating the reference pulse further comprises:

comparing timing of a pair of consecutive ring oscillator stages with timing of the first transition time pulse; and

generation a rising edge of the reference pulse when a rising edge of the first transition time pulse occurs between an input from the pair of consecutive ring oscillator stages; and

generating a falling edge of the reference pulse when a next falling edge occurs on the pair of consecutive ring oscillator stages.

13. The method of claim 8, further comprising integrating the interface circuitry into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

14. An apparatus for locking output transition timing of interface circuitry, comprising:

means for generating a first transition time pulse having a pulse width equal to a characteristic of an output driver output;

means for generating a reference pulse having a pulse width equal to a desired signal characteristic;

means for generating a first analog bias voltage in response to a difference between a first transition time pulse width and the reference pulse width; and

means for biasing a first pre-driver current source with the first analog bias voltage.

15. The apparatus of claim 14, in which the characteristic of the output driver output comprises a rise time.

16. The apparatus of claim 15, further comprising:

means for generating a second transition time pulse having a pulse width equal to a fall time of the output driver output;

means for generating a second analog bias voltage in response to a difference between a second transition time pulse width and the reference pulse width; and

means for biasing a second pre-driver current source with the second analog bias voltage.

17. The apparatus of claim 16, in which the means for generating the reference pulse further comprises:

means for comparing timing of a pair of consecutive ring oscillator stages with timing of the first transition time pulse; and

means for generation a rising edge of the reference pulse when a rising edge of the first transition time pulse occurs between an input from the pair of consecutive ring oscillator stages; and

means for generating a falling edge of the reference pulse when a next falling edge occurs on the pair of consecutive ring oscillator stages.

18. The apparatus of claim 14, integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

19. A method for locking output transition timing of interface circuitry, comprising the steps of:

generating a first transition time pulse having a pulse width equal to a rise time of an output driver output;

generating a reference pulse having a pulse width equal to a desired rise time;

generating a first analog bias voltage in response to a difference between a first transition time pulse width and the reference pulse width; and

biasing a first pre-driver current source with the first analog bias voltage.

20. The method of claim 19 further comprising the step of integrating the interface circuitry into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

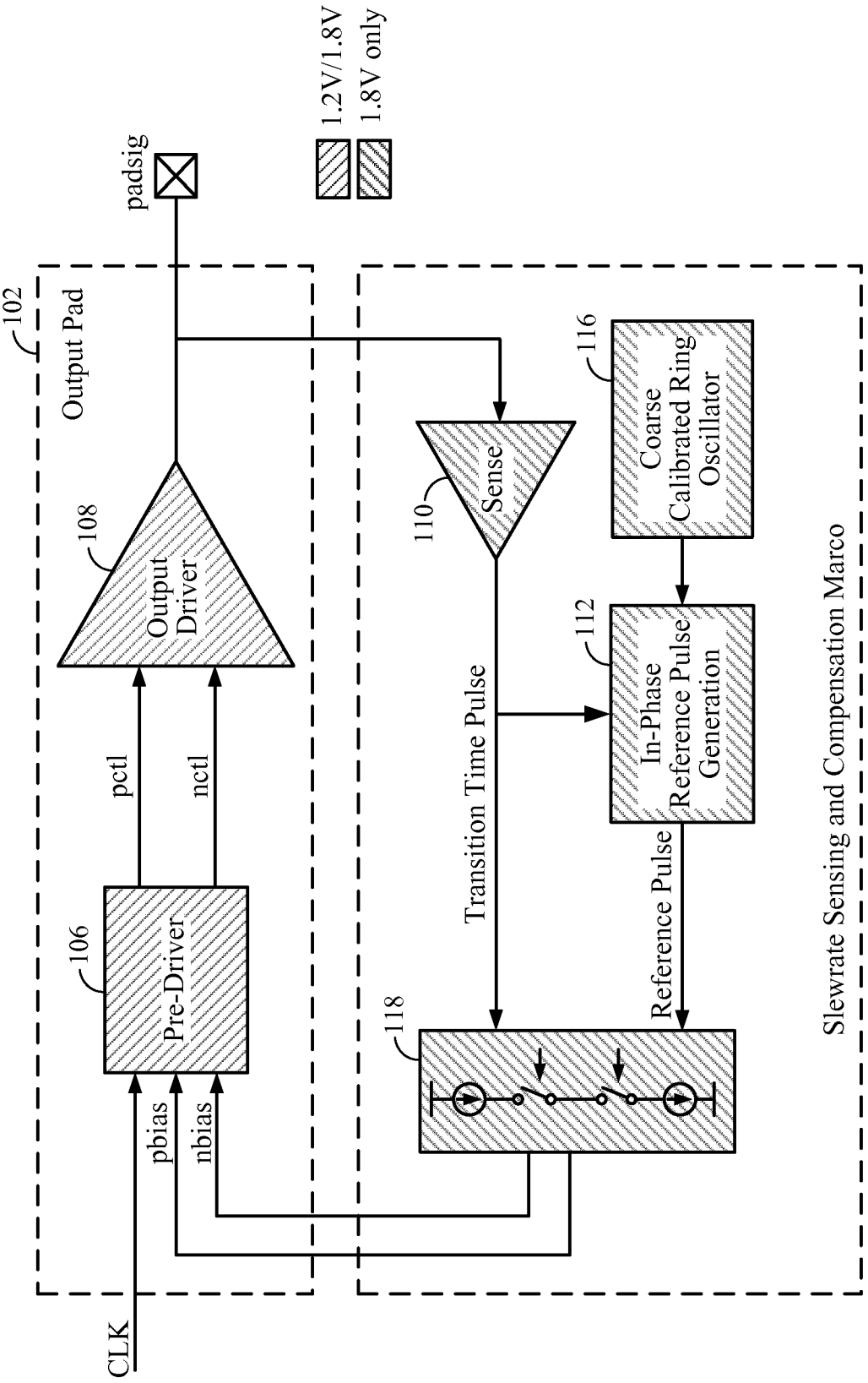
1.2V/1.8V
1.8V only
padsig
102
Output Pad
108
Output Driver
110
Sense
116
Coarse Calibrated Ring Oscillator
112
In-Phase Reference Pulse Generation
pctl
nctl
Transition Time Pulse
Reference Pulse
106
Pre-Driver
118
pbias
nbias
CLK
Slewrate Sensing and Compensation Marco

FIG. 1A

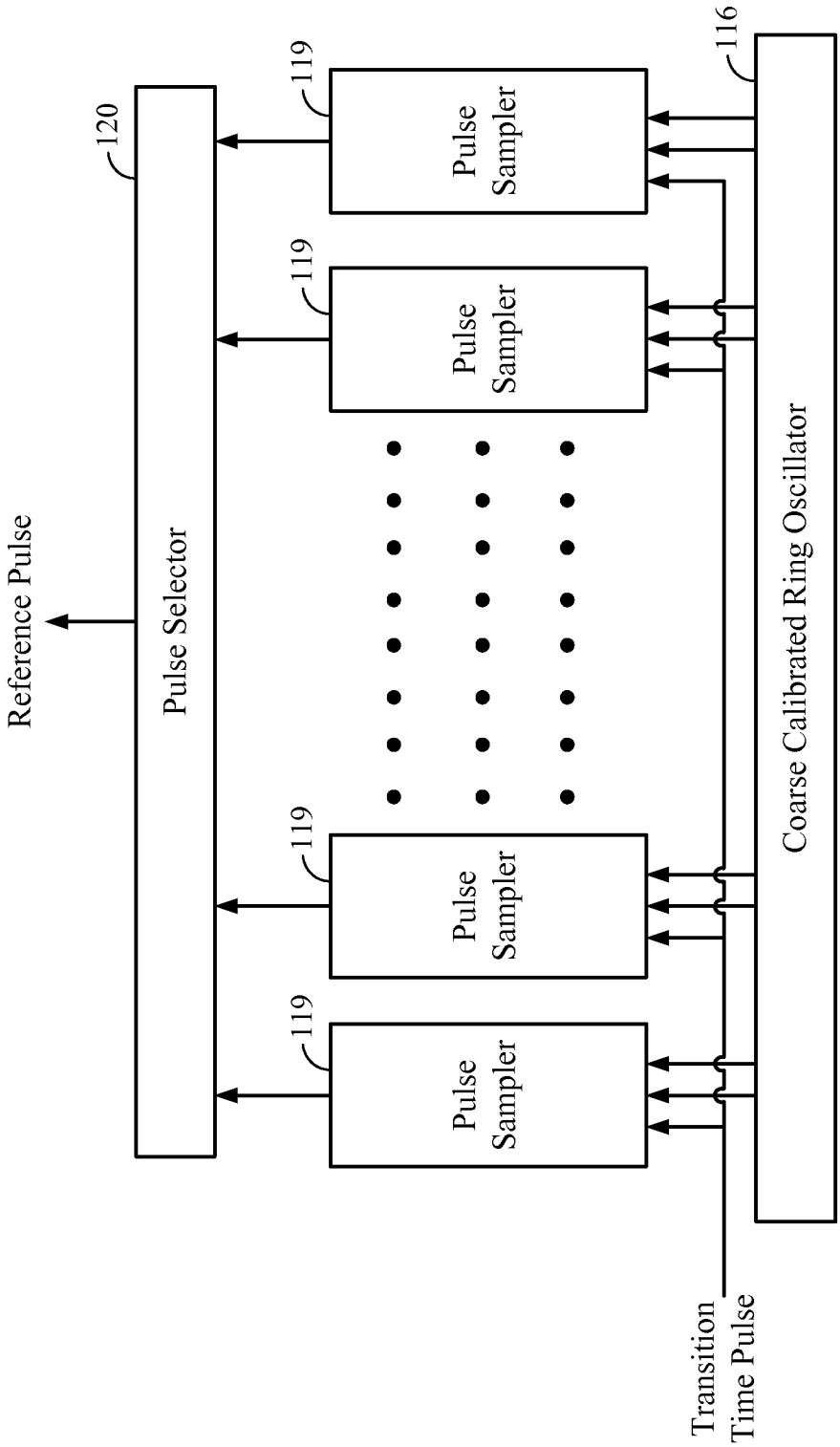
Reference Pulse
Pulse Selector
120
Pulse Sampler
119
Pulse Sampler
119
Pulse Sampler
119
Pulse Sampler
119
Coarse Calibrated Ring Oscillator
116
Transition Time Pulse

FIG. 1B

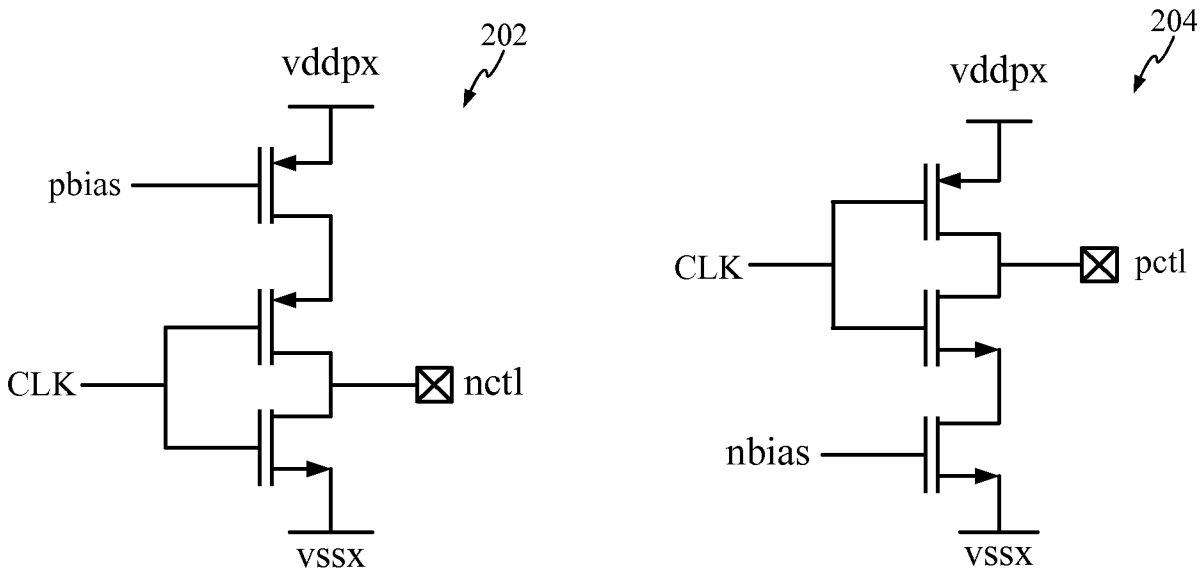
202
vddpx
pbias
CLK
nctl
vssx
204
vddpx
CLK
pctl
nbias
vssx

FIG. 2

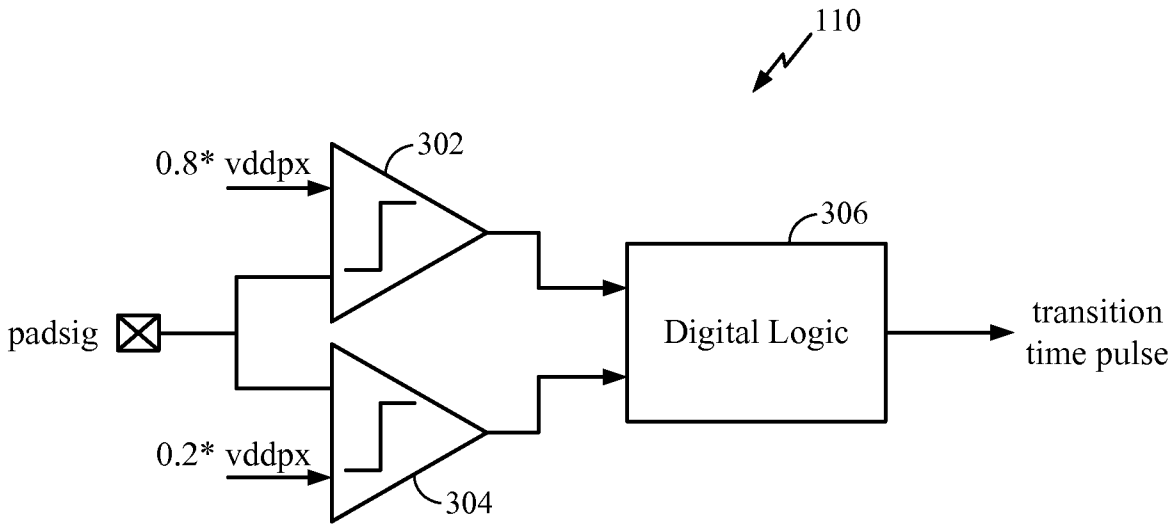
110
0.8* vddpx
302
306
padsig
Digital Logic
transition
time pulse
0.2* vddpx
304

FIG. 3

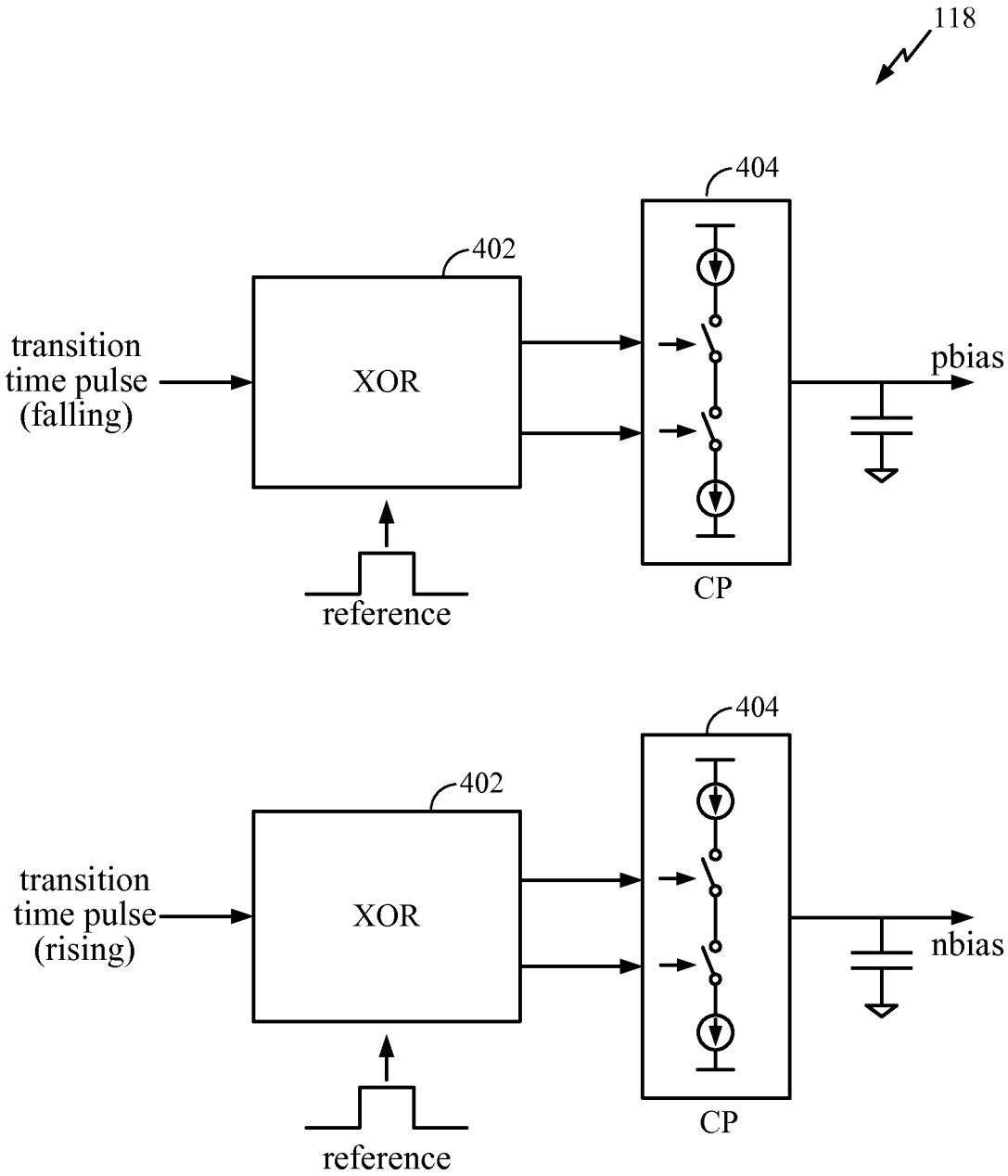
118
404
402
transition
time pulse
(falling)
XOR
pbias
reference
CP
404
402
transition
time pulse
(rising)
XOR
nbias
reference
CP

FIG. 4

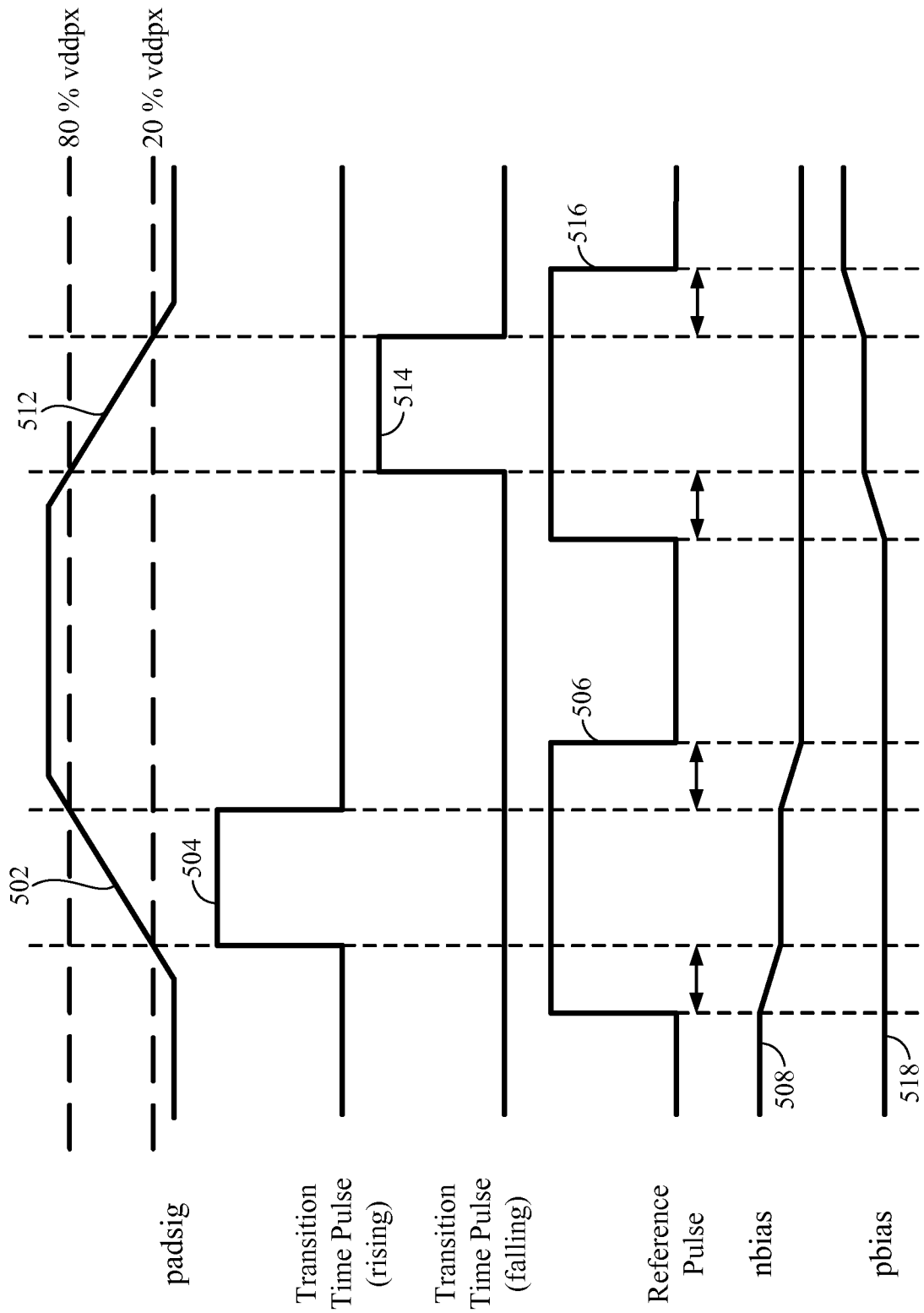
80 % vddpx
20 % vddpx
512
514
516
502
504
506
508
518
padsig
Transition Time Pulse (rising)
Transition Time Pulse (falling)
Reference Pulse
nbias
pbias

FIG. 5

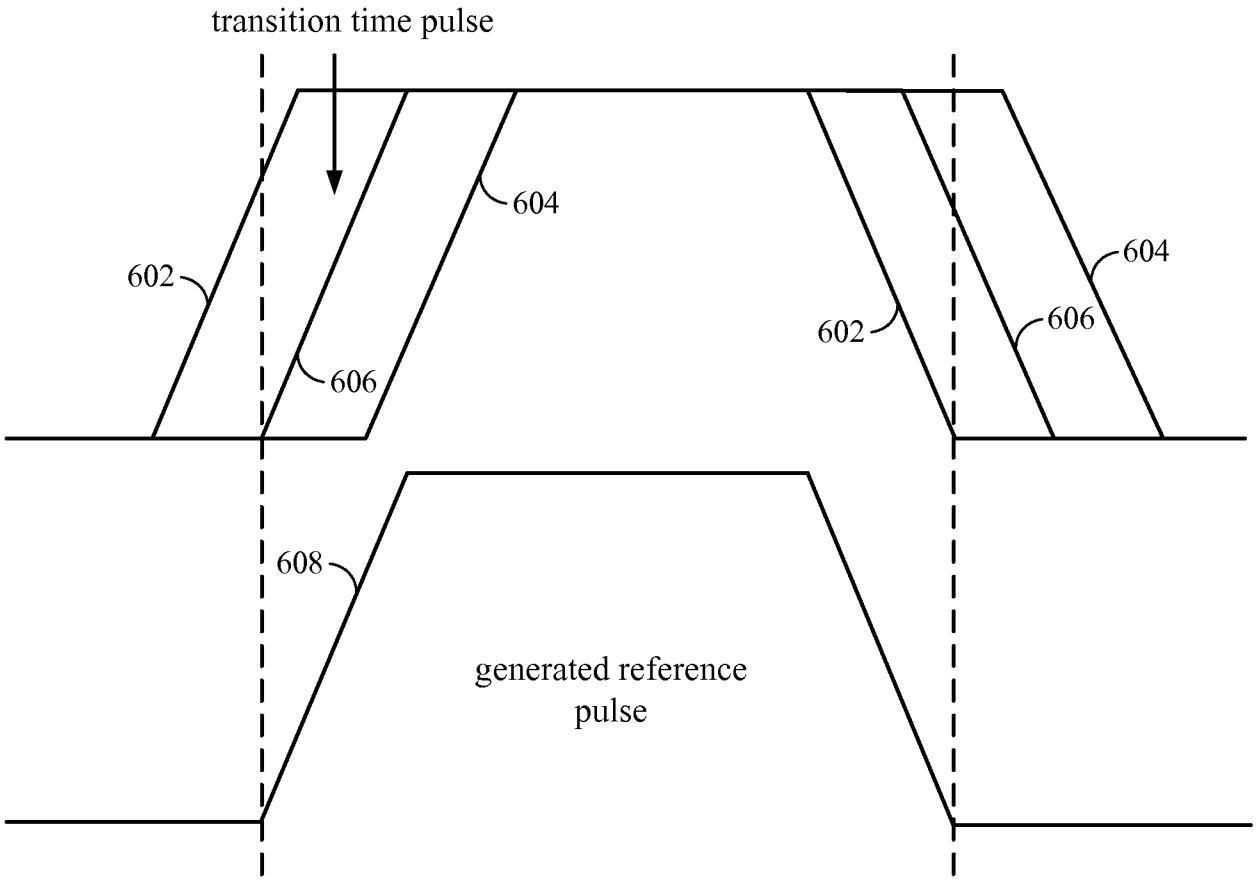
transition time pulse
602
604
606
602
606
604
608
generated reference pulse

FIG. 6

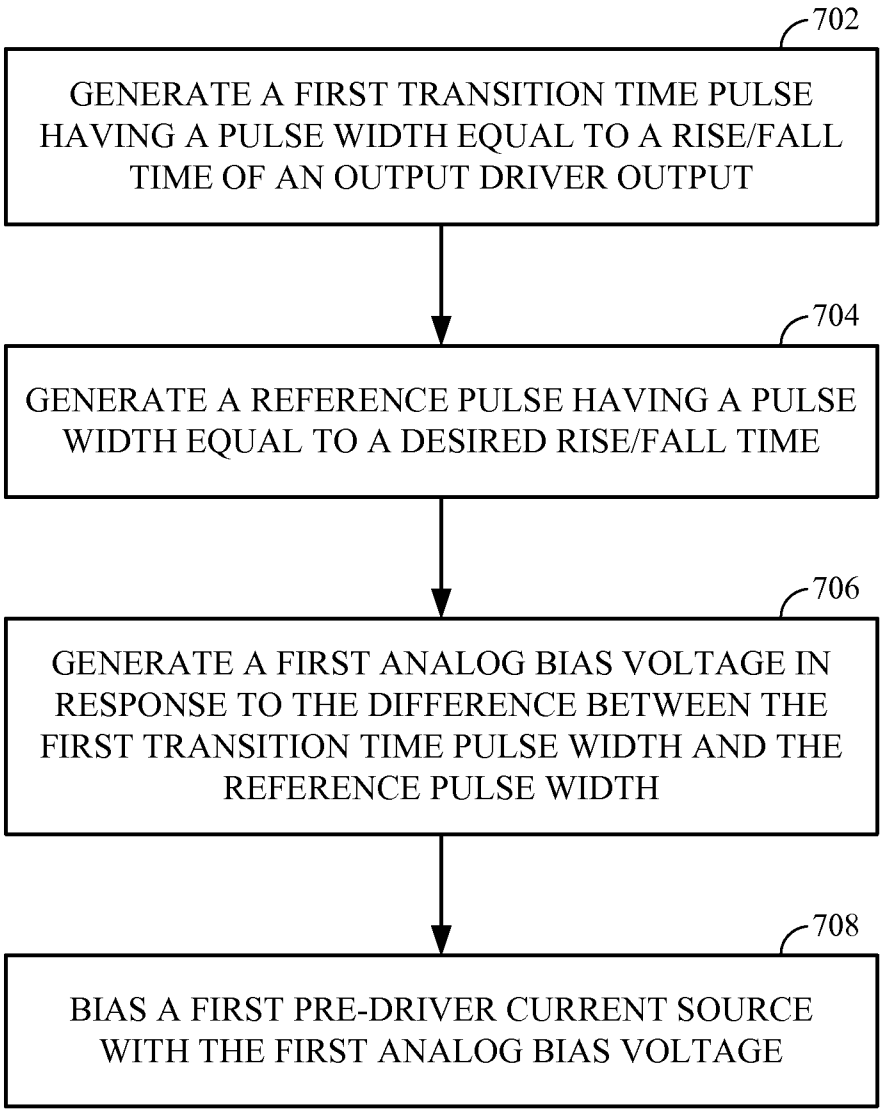
702
GENERATE A FIRST TRANSITION TIME PULSE HAVING A PULSE WIDTH EQUAL TO A RISE/FALL TIME OF AN OUTPUT DRIVER OUTPUT
704
GENERATE A REFERENCE PULSE HAVING A PULSE WIDTH EQUAL TO A DESIRED RISE/FALL TIME
706
GENERATE A FIRST ANALOG BIAS VOLTAGE IN RESPONSE TO THE DIFFERENCE BETWEEN THE FIRST TRANSITION TIME PULSE WIDTH AND THE REFERENCE PULSE WIDTH
708
BIAS A FIRST PRE-DRIVER CURRENT SOURCE WITH THE FIRST ANALOG BIAS VOLTAGE

FIG. 7

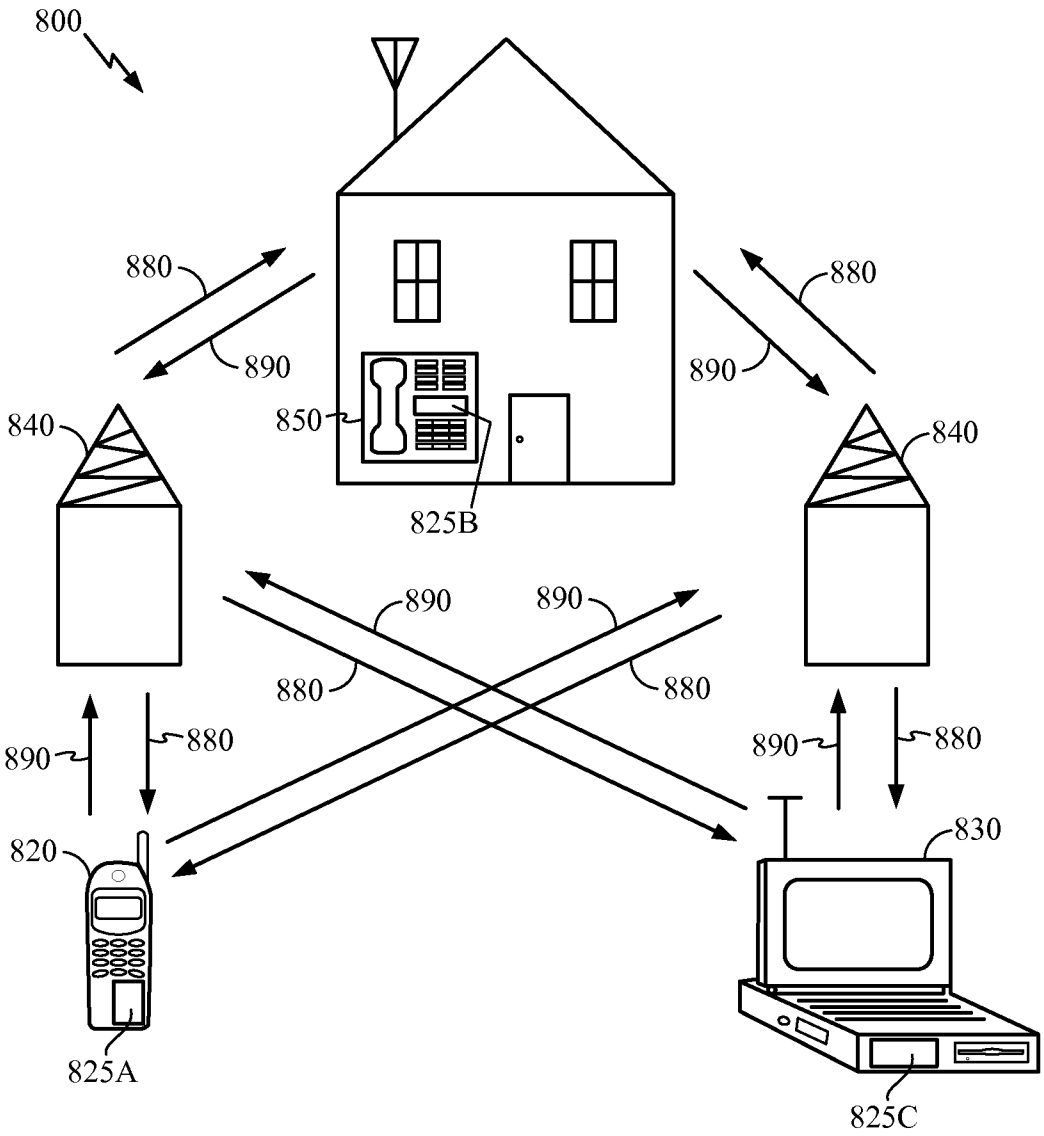
800
880
890
840
850
825B
880
890
840
890
880
890
880
890
880
820
825A
830
825C

FIG. 8

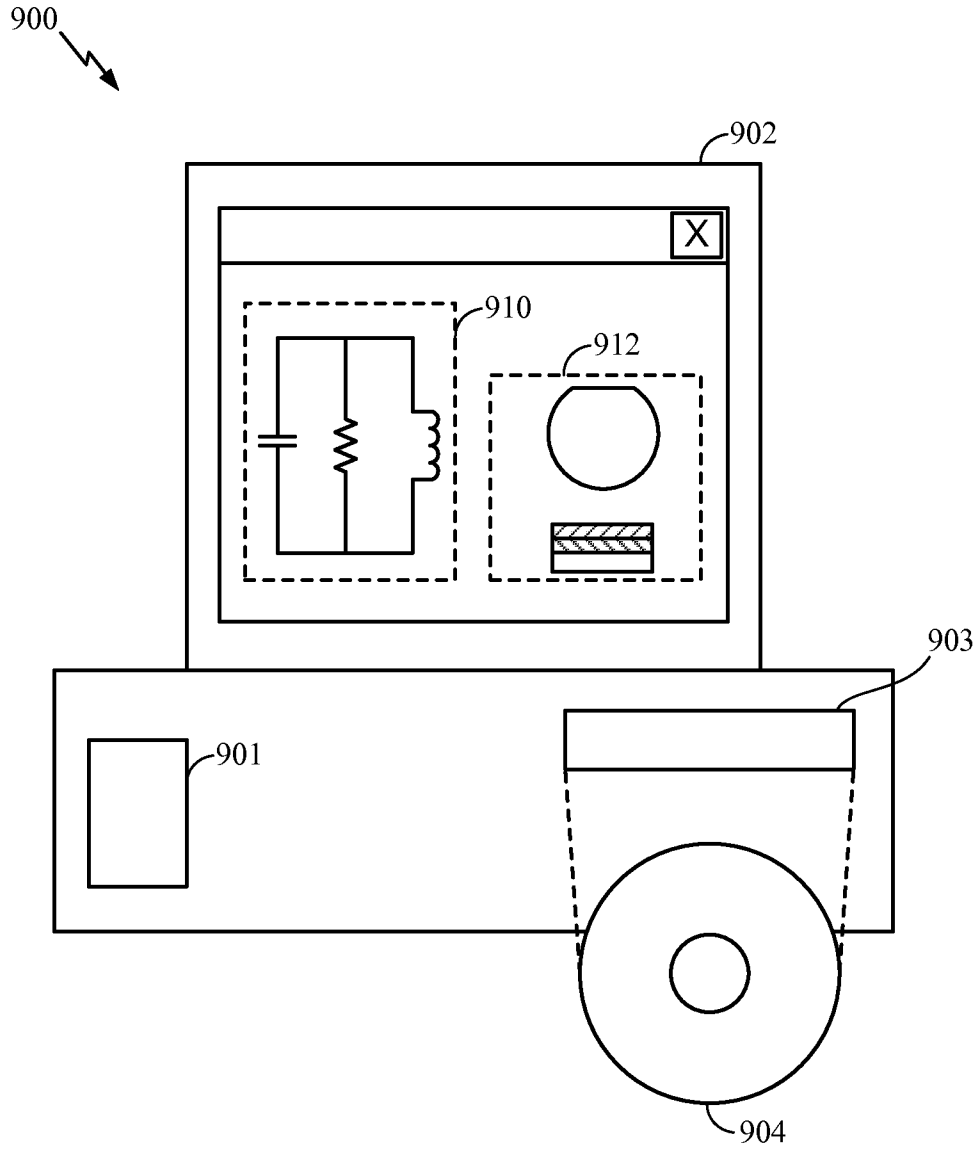

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/022344

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K19/003
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/164924 A1 (BUCOSSI WILLIAM L [US] ET AL) 10 July 2008 (2008-07-10)	1-5, 7-11, 13-16, 18-20
A	figures 5,6	6,12,17

X	US 2005/285647 A1 (WILSON TIMOTHY M [US] ET AL) 29 December 2005 (2005-12-29)	5,7,11, 13,18,20
Y	the whole document	1-4, 8-10, 14-16,19
A		6,12,17

Y	US 2003/179029 A1 (EICHFELD HERBERT [DE] ET AL) 25 September 2003 (2003-09-25)	1-4, 8-10, 14-16,19
	the whole document	

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 May 2013	24/05/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Santos, Paulo

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/022344

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4 972 101 A (PARTOVI HAMID [US] ET AL) 20 November 1990 (1990-11-20) figure 1 -----	1-4, 8-10, 14-16,19
X	US 2007/001725 A1 (ATHA MOHAMMED M [US] ET AL) 4 January 2007 (2007-01-04) figure 7 -----	1-3

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/022344

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008164924 A1	10-07-2008	US 2008164924 A1	10-07-2008
		US 2008284464 A1	20-11-2008
US 2005285647 A1	29-12-2005	NONE	
US 2003179029 A1	25-09-2003	EP 1264401 A1	11-12-2002
		US 2003179029 A1	25-09-2003
		WO 0154275 A1	26-07-2001
US 4972101 A	20-11-1990	NONE	
US 2007001725 A1	04-01-2007	NONE	