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Sevilla et al.

[11] **3,729,730**

[45] **Apr. 24, 1973**

[54] DISPLAY SYSTEM

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[52] **U.S. Cl.** .....**340/324 AD,** 340/172.5

[51] **Int. Cl.**.....**G06f 3/14**

[58] **Field of Search**.....340/324 A

[56] **References Cited**

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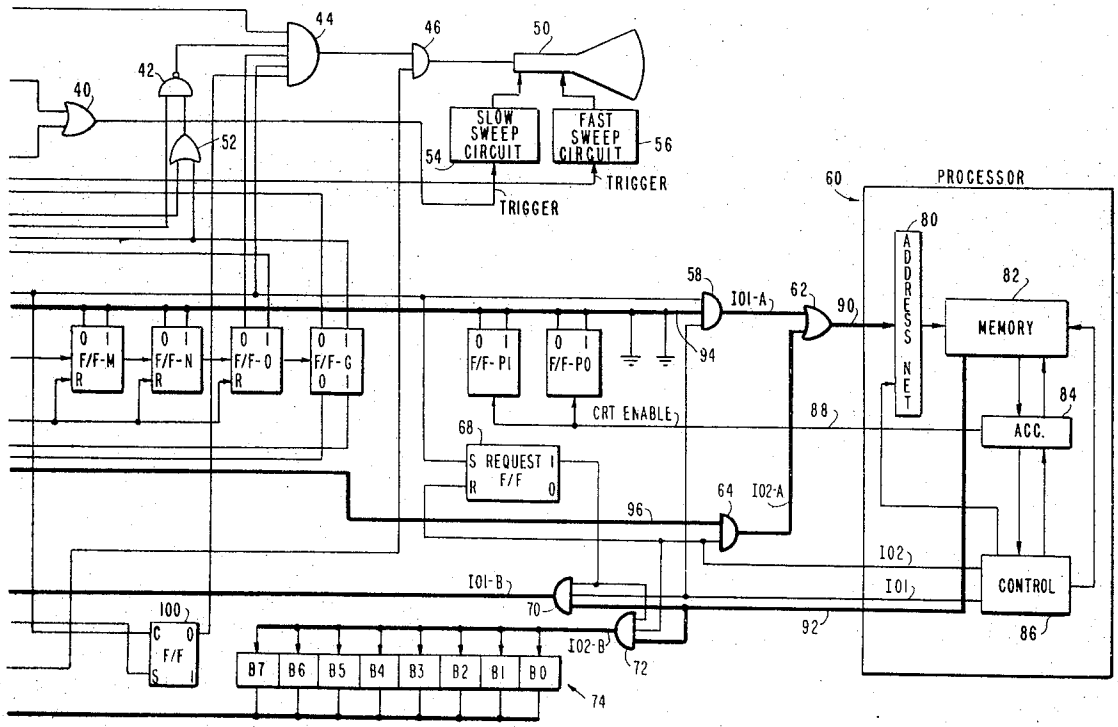
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[57] **ABSTRACT**

A display system of very low cost and whose character set is program alterable. A processor memory has two areas which control the display — a character buffer for representing the code of the character to be formed in each position of the display, and a dot pattern storage area which includes the dot patterns for all of the characters. Slow and fast sweeps across the face of a CRT occur in synchronism with a display system counter. During each cycle, a first address corresponding to the position of a character to be displayed is transmitted to the memory and a code representative of the character to be displayed is returned to the display system. This code is then combined with additional positional information derived from the counter to form a second address for transmission to the memory. The data word received back from the memory determines the locations of dots to be displayed in one line segment. The data word is shifted out of a shift register in synchronism with the fast sweep across the face of the CRT, each 1 bit in the data word causing the display of a dot. The character set can be altered under program control simply by changing the dot patterns in the second area of the memory. Because the character information is not hard-wired, maximum flexibility in the character set can be achieved. Provision is also made for selecting one of several character buffers and one of several character sets, both under program control.

119 Claims, 8 Drawing Figures



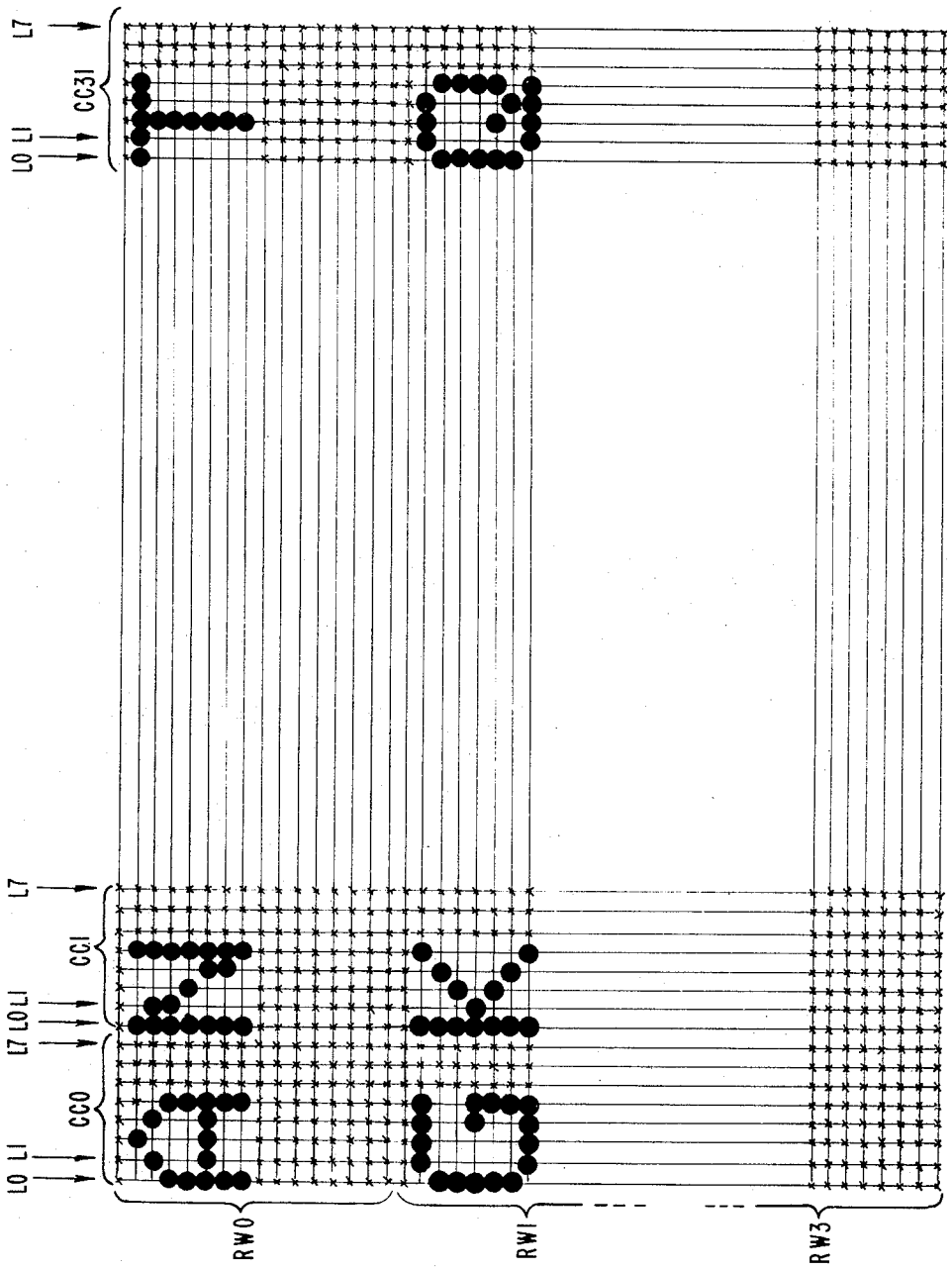


FIG. 1

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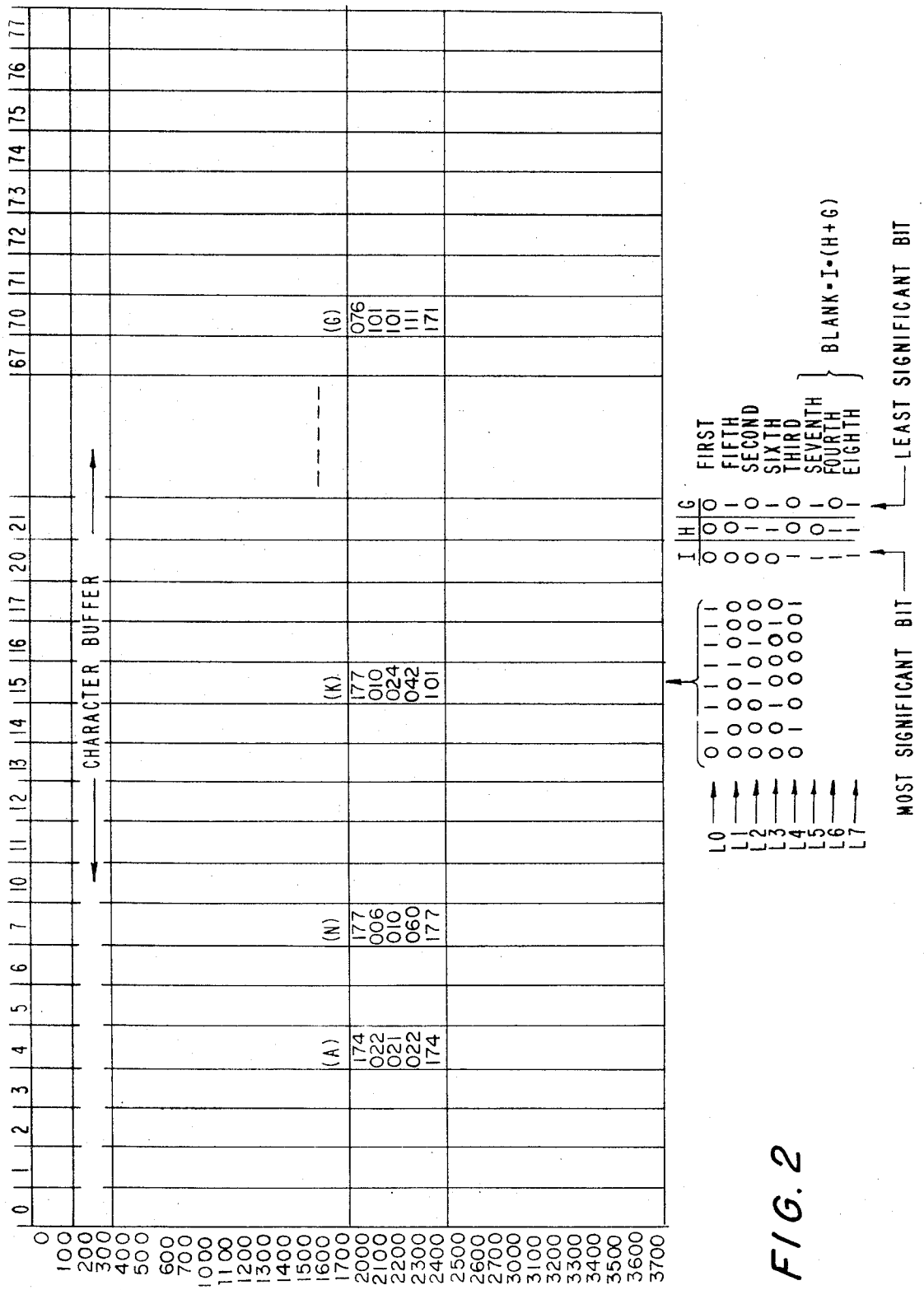
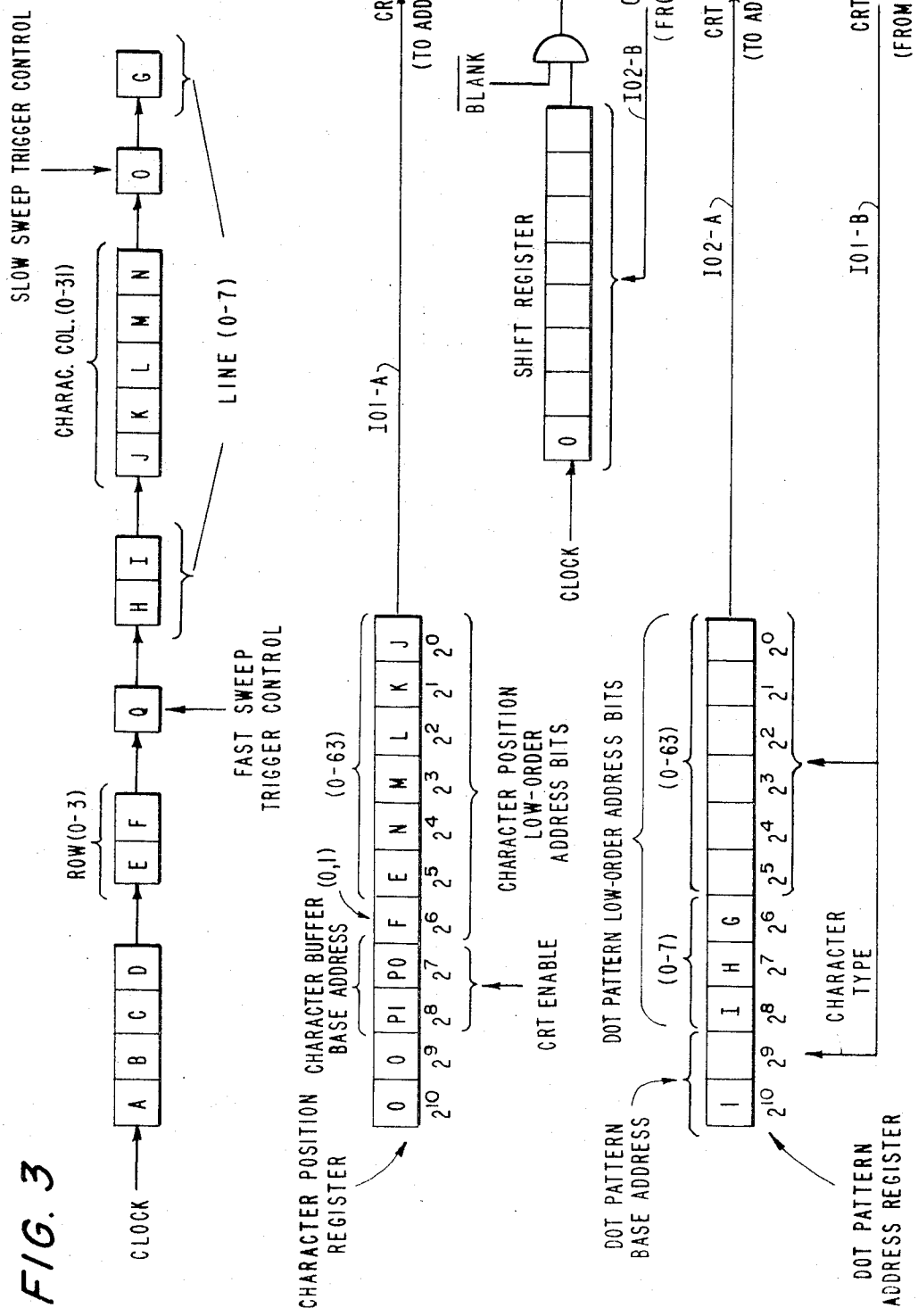

0 1 2 3 4 5 6 7 10 11 12 13 14 15 16 17 20 21 67 70 71 72 73 74 75 76 77
0 100 200 300 400 500 600 700 1000 1100 1200 1300 1400 1500 1600 1700 2000 2100 2200 2300 2400 2500 2600 2700 3000 3100 3200 3300 3400 3500 3600 3700
CHARACTER BUFFER
(A) 174 022 021 022 174
(N) 177 006 010 060 177
(K) 177 010 024 042 101
(G) 076 101 101 111 171
L0 L1 L2 L3 L4 L5 L6 L7
0 1 1 1 1 1 1 1
0 0 0 0 1 0 0 0
0 0 0 0 1 0 1 0
0 0 0 0 1 1 0 0
0 0 0 1 0 0 0 0
0 0 0 1 0 0 1 0
0 0 1 0 0 0 0 0
0 1 0 0 0 0 0 1
I H G
0 0 0 FIRST
0 0 1 FIFTH
0 1 0 SECOND
0 1 1 SIXTH
1 0 0 THIRD
1 0 1 SEVENTH
1 1 0 FOURTH
1 1 1 EIGHTH
BLANK-I·(H+G)
LEAST SIGNIFICANT BIT
MOST SIGNIFICANT BIT

FIG. 2

FIG. 3


CLOCK
A B C D
ROW(0-3)
E F
Q
FAST SWEEP TRIGGER CONTROL
H I
LINE (0-7)
J K L M N
CHARAC. COL.(0-31)
O
SLOW SWEEP TRIGGER CONTROL
G
CHARACTER POSITION REGISTER
CHARACTER BUFFER BASE ADDRESS
(0,1)
(0-63)
0 0 PI P0 F E N M L K J
2^{10} 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0
CHARACTER POSITION LOW-ORDER ADDRESS BITS
CRT ENABLE
IO1-A
CRT ADDRESS
(TO ADDRESS NET)
BLANK
TO VIDEO
SHIFT REGISTER
0
CLOCK
IO2-B
CRT DATA
(FROM MEMORY)
DOT PATTERN BASE ADDRESS
DOT PATTERN LOW-ORDER ADDRESS BITS
(0-7)
(0-63)
I I H G
2^{10} 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0
CHARACTER TYPE
IO2-A
CRT ADDRESS
(TO ADDRESS NET)
IO1-B
CRT DATA
(FROM MEMORY)
DOT PATTERN ADDRESS REGISTER

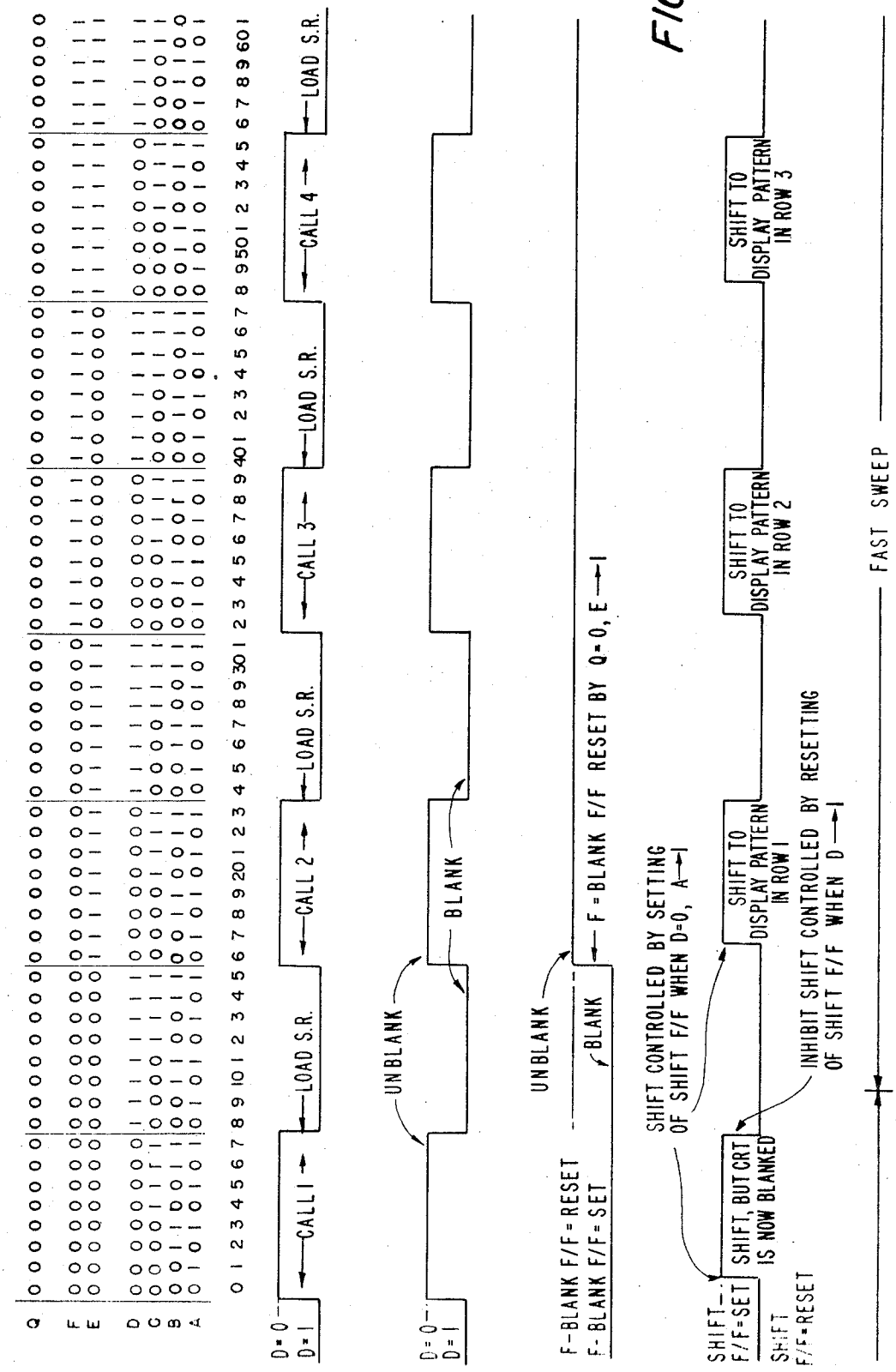

Q
F
E
D
C
B
A
0 1 2 3 4 5 6 7 8 9 10 1 2 3 4 5 6 7 8 9 20 1 2 3 4 5 6 7 8 9 30 1 2 3 4 5 6 7 8 9 40 1 2 3 4 5 6 7 8 9 50 1 2 3 4 5 6 7 8 9 60 1
D=0
D=1
CALL 1
LOAD S.R.
CALL 2
LOAD S.R.
CALL 3
LOAD S.R.
CALL 4
LOAD S.R.
UNBLANK
BLANK
F-BLANK F/F=RESET
F-BLANK F/F=SET
F=BLANK F/F RESET BY Q=0, E=1
SHIFT CONTROLLED BY SETTING OF SHIFT F/F WHEN D=0, A=1
SHIFT F/F=SET
SHIFT F/F=RESET
SHIFT, BUT CRT IS NOW BLANKED
SHIFT TO DISPLAY PATTERN IN ROW 1
SHIFT TO DISPLAY PATTERN IN ROW 2
SHIFT TO DISPLAY PATTERN IN ROW 3
INHIBIT SHIFT CONTROLLED BY RESETTING OF SHIFT F/F WHEN D=1
FAST SWEEP

FIG. 4

WHEN Q=1, F→1, STAGES F AND Q ARE IMMEDIATELY RESET TO 0 AND A CARRY IS EXTENDED TO STAGE H. STAGES A B C D E F Q ARE AS THEY WERE WHEN CALL 1 WAS GENERATED SO ANOTHER CALL IS MADE FOR ROW 1. BUT BECAUSE STAGE H HAS BEEN TRIGGERED, THE CALL IS FOR THE NEXT LINE IN ROW 1.
AS SOON AS STAGES A-Q REPRESENT 96, THEY ARE RESET TO REPRESENT 0.
Q
F
E
D
C
B
A
62 3 4 5 6 7 8 9 70 1 2 3 4 5 6 7 8 9 80 1 2 3 4 5 6 7 8 9 90 1 2 3 4 5 96 0 1 2
CALL 5
LOAD S.R.
(WILL NOT BE USED)
CALL 6
LOAD S.R.
(WILL NOT BE USED)
CALL 1
UNBLANK
BLANK
F-BLANK F/F SET BY Q=1, E→1
SHIFT TO DISPLAY PATTERN IN ROW 4
SHIFT, BUT CRT IS NOW BLANKED
RETRACE

FIG. 5

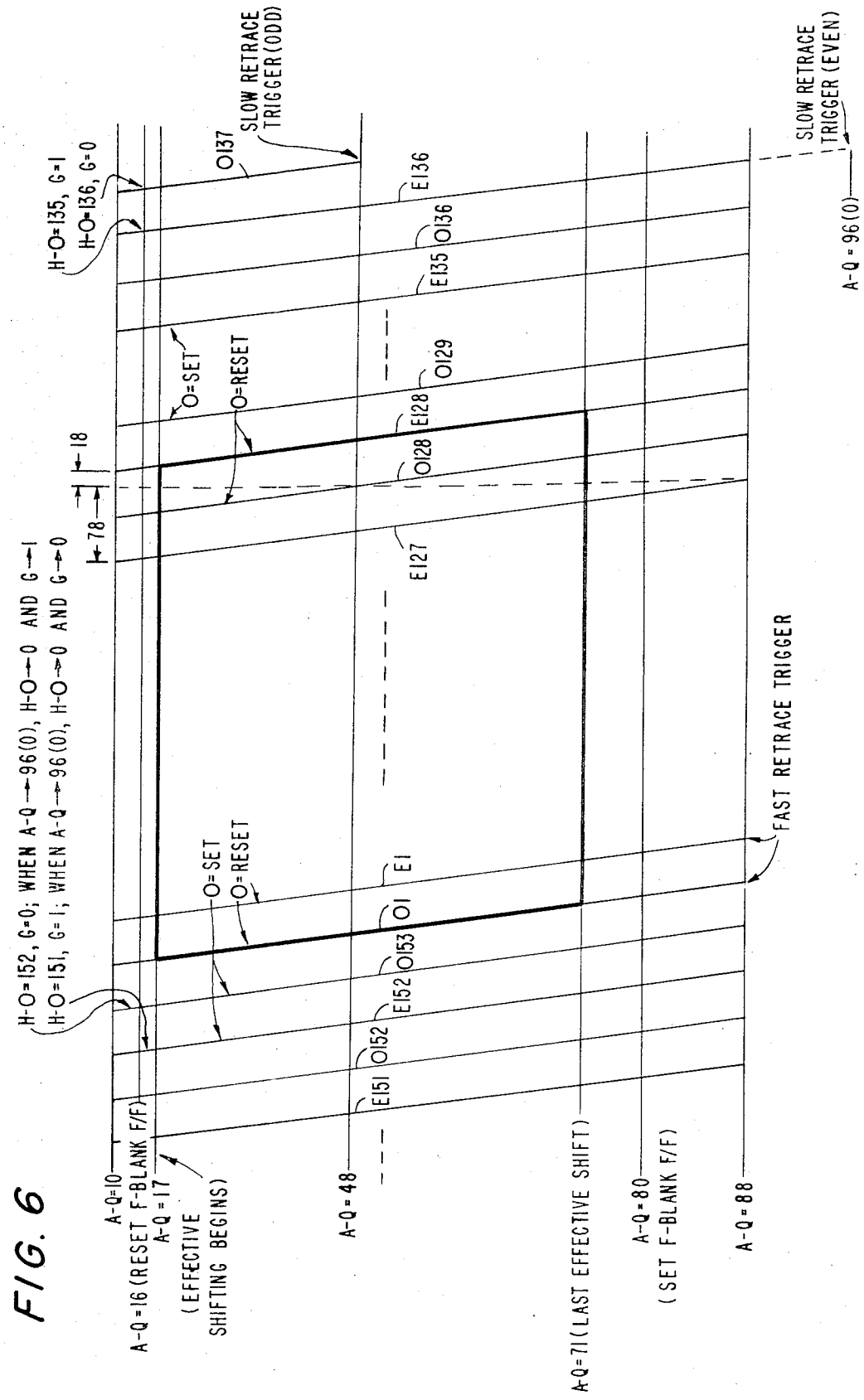

H-O=152, G=0; WHEN A-Q→96(0), H-O→0 AND G→1
H-O=151, G=1; WHEN A-Q→96(0), H-O→0 AND G→0
H-O=135, G=1
H-O=136, G=0
O137
SLOW RETRACE TRIGGER(ODD)
E136
O136
E135
O129
E128
O128
E127
E1
O1
O153
E152
O152
E151
O=SET
O=RESET
18
78
A-Q=10
A-Q=16 (RESET F-BLANK F/F)
A-Q=17
(EFFECTIVE SHIFTING BEGINS)
A-Q=48
A-Q=71 (LAST EFFECTIVE SHIFT)
A-Q=80
(SET F-BLANK F/F)
A-Q=88
FAST RETRACE TRIGGER
SLOW RETRACE TRIGGER (EVEN)
A-Q=96(0)

FIG. 6

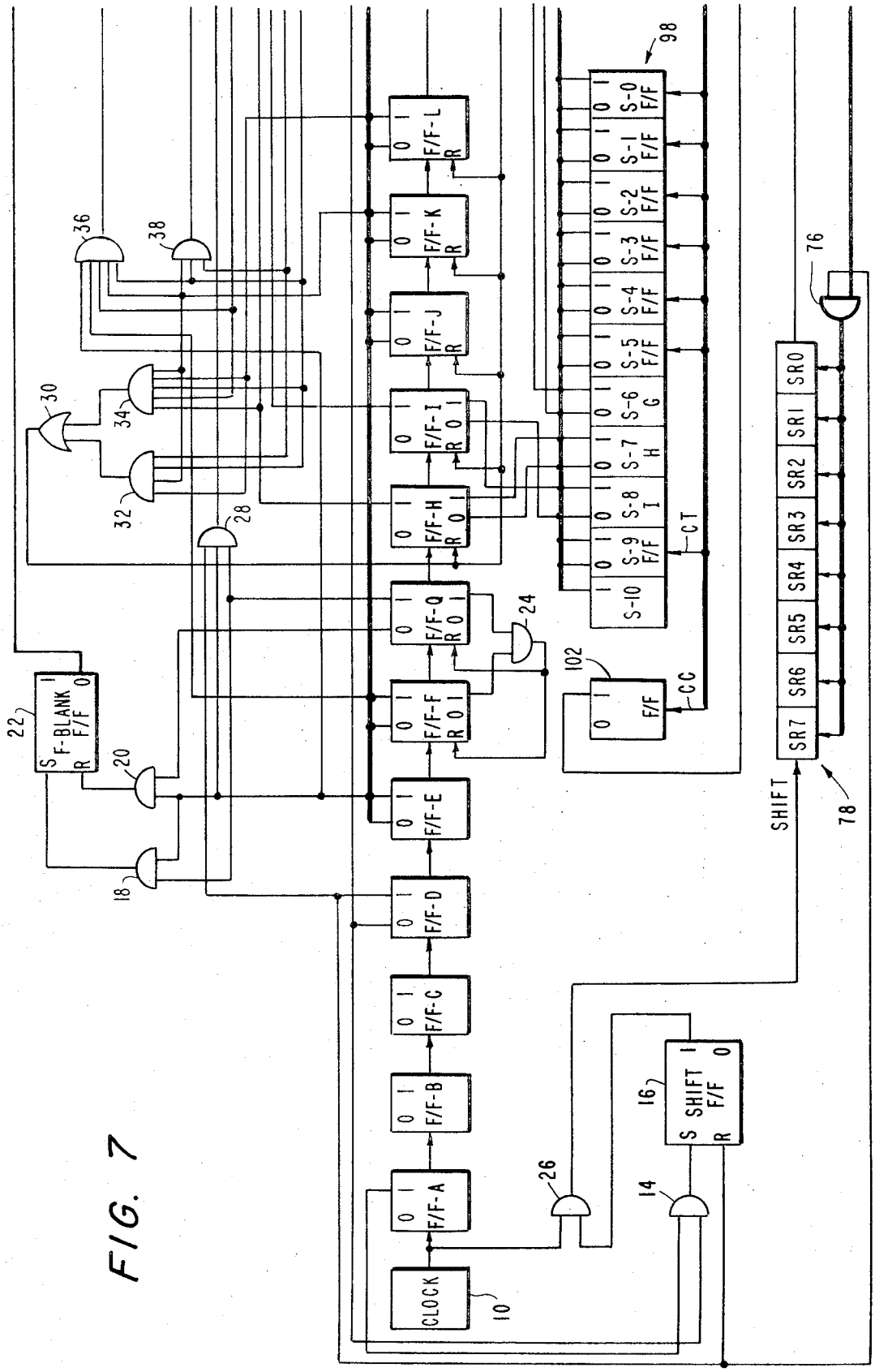
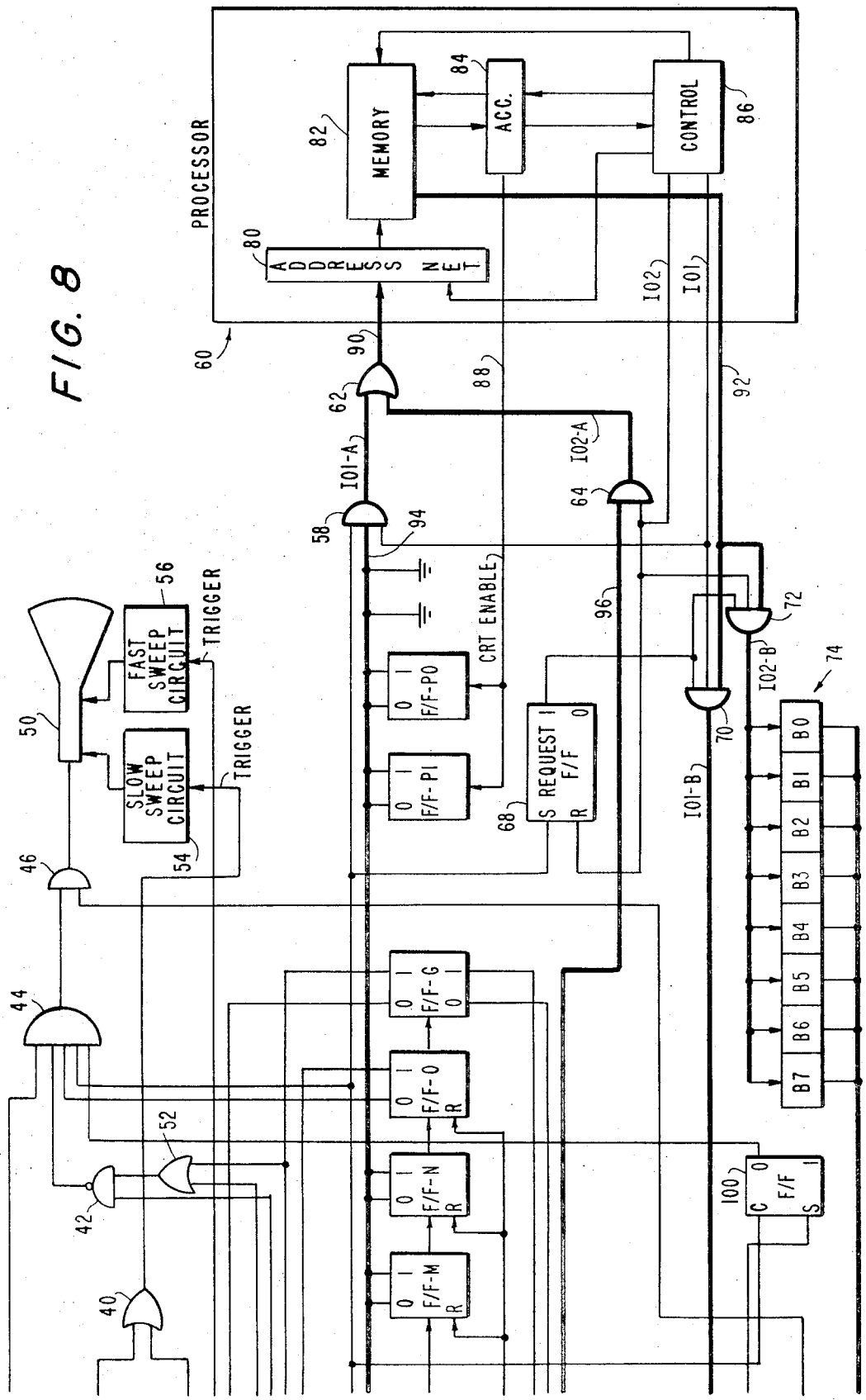

CLOCK
10
F/F-A
F/F-B
F/F-C
F/F-D
F/F-E
F/F-F
F/F-Q
F/F-H
F/F-I
F/F-J
F/F-K
F/F-L
S F-BLANK R F/F
22
18
20
24
28
30
32
34
36
38
26
14
S SHIFT R F/F
16
98
S-0 F/F
S-1 F/F
S-2 F/F
S-3 F/F
S-4 F/F
S-5 F/F
S-6 G
S-7 H
S-8 I
S-9 F/F
S-10
CT
102
F/F
CC
76
SR0
SR1
SR2
SR3
SR4
SR5
SR6
SR7
SHIFT
78

FIG. 7

FIG. 8


PROCESSOR
MEMORY
ACC.
CONTROL
ADDRESS NET
82
84
86
80
60
90
62
88
92
I02
I01
I01-A
I02-A
64
58
94
96
72
70
I02-B
I01-B
74
B0
B1
B2
B3
B4
B5
B6
B7
CRT ENABLE
F/F-PO
F/F-PI
S REQUEST F/F
68
FAST SWEEP CIRCUIT
SLOW SWEEP CIRCUIT
TRIGGER
TRIGGER
56
54
50
46
44
42
40
52
F/F-G
F/F-O
F/F-N
F/F-M
100
F/F

DISPLAY SYSTEM

This invention relates to display systems, and more particularly to low-cost display systems having program-alterable character sets.

At the present time, in many computer installations a display system provides visual information to the computer user. In a typical installation, the display system includes some kind of hard-wired or permanent memory which contains the information necessary to control the display of all of the characters in a predetermined set (for example, the letters of the alphabet, the numerals and punctuation marks). The processor with which the display system is employed may maintain a record of the character required at each position on the face of a cathode ray tube. Whenever a character is to be formed at a particular position on the screen, the character identification is transmitted from the processor to the display system. The character identification is then used to retrieve the necessary information from the permanent memory in the display system for controlling the writing of the character.

One of the problems with prior art display systems is that they are very costly; the cost of the display system, separate and apart from the cost of the processor with which the display system is used, can be upward of several thousand dollars. Although high-cost display systems can be very sophisticated in several respects (resolution, dimensional accuracy, etc.), there are many situations in which the display system need do nothing more than communicate questions, answers or other word information to the user. In such cases, all that need be formed on the screen are letters and numerals, for example, rather than architectural drawings, mask layouts, etc. Especially for use with low-cost processors, there is a great need for very low-cost display systems.

It is a general object of our invention to provide a display system of very low cost.

Another problem with conventional display systems is that the character set cannot be changed easily. The character set which can be displayed is determined by the permanent memory in the system. This memory defines a dot pattern or line segment arrangement for each character to be depicted. In order to change the character set, it is necessary to physically change the memory in the display.

It is another object of our invention to provide a program-alterable processor display system, that is, a system in which the characters which can be depicted can be altered under program control.

In accordance with the principles of our invention, two areas of the processor memory are allocated to the display. The first area is a character buffer having one location associated with each character position on the face of the CRT. Each location in the character buffer contains a code which represents the identity of a character to be displayed. The codes in the buffer are continuously changed under program control depending upon the information to be displayed at any time. In the illustrative embodiment of the invention, there are 128 character positions on the screen and thus there are 128 locations in the character buffer area of the memory. There is a total of 64 different characters which can be displayed. Consequently, each of the 128 locations in the character buffer contains one of 64 different codes.

The second memory area contains dot pattern codes for each character which can be displayed. Each character is formed on the face of the CRT by five adjacent line sweeps. In each line, a series of dots is formed. For each character to be displayed, the second storage area of the memory includes five words, the 1's in each word corresponding to the dots which should be displayed on the screen in the respective line segment.

The CRT itself is a conventional CRT used in a television receiver, although the yoke is rotated so that the fast sweeps are in the vertical direction. The fast and slow sweeps across the face of the CRT are synchronized to a counter in the display system. The instantaneous count at any time is related not only to the position on the screen of the character through which the electron beam is passing, but also to the particular one of the five lines which make up the character. To form a series of dots in a line segment of a character, the display system counter causes a first address to be transmitted to the processor memory. This address is the address of a location in the first area of the processor memory — the character buffer. The address identifies the location in the character buffer which contains the code of the character to be displayed in the position on the face of the CRT through which the electron beam will sweep. The processor memory then transmits a first data word to the display system which is a code identifying the particular character to be displayed.

The display system then combines this character code with the identity of that one of the five possible line segments forming the character through which the electron beam will pass, and transmits a second address to the processor memory. This second address identifies a location in the second memory area — the dot pattern storage area — which contains the dot pattern for the particular line segment in the character previously identified. The processor memory then transmits a second data word to the display system, this data word representing the dot pattern which should be displayed. The display system then causes the electron beam to be pulsed on and off in accordance with the dot pattern data so that the required series of dots will be formed on the face of the CRT as the electron beam sweeps through the identified line segment in the character position under consideration.

In order to change the character set, all that is required is to change the dot pattern codes in the dot pattern storage area of the memory. Since this can be accomplished under program control — the dot patterns are nothing more than data words stored in the processor memory — it is apparent that the character set which can be displayed is program-alterable.

The processor with which the display system of the invention is utilized ordinarily functions without regard to the display system when a display is not required. In order to turn on the display, a "CRT Enable" command must be executed. This command causes the processor to change its mode of operation. At the start of each processor cycle, the processor interrupts its ordinary operation and allows the display system to interrogate the processor memory twice in succession. Thus it is at the start of a processor cycle that the two address and data transmissions between the display system and the processor memory take place. Since the interrup-

tions necessarily slow down the overall speed of the processor, they take place only when a display is required, that is, only after a CRT-Enable command is given. When the display is no longer required, a "CRT Disable" command is executed. At this time, the processor reverts to its normal mode of operation and does not allow communication directly between the display system and the processor memory. In this way, the processor operates at maximum speed when a display is not required.

In the description above, it was assumed that the processor includes only a single character buffer (the first memory storage area). However, it may be desirable to provide two or more character buffers in the memory. For example, a first character buffer may be loaded with character codes to represent a particular display. While a particular message is thus being displayed on the face of the CRT, it may be necessary to compose another message. If it takes a considerable time to compose this other message, and if the complete message should be displayed in its entirety after it is formed, it is apparent that the message can be composed by writing the necessary character codes in the second character buffer. As soon as the message is fully composed and should be displayed, all that is necessary is for the first address transmitted to the processor memory from the display system to identify a location in the second character buffer corresponding to the position of each character to be displayed on the screen, rather than a corresponding location in the first character buffer. The first address which is transmitted to the memory includes not only the address of a particular one of the 128 locations in a character buffer, but also the base address of the character buffer. It is the base address which selects a particular character buffer to the exclusion of all others. The display system includes a set of flip-flops whose states represent the base address of the character buffer to be used. The CRT-Enable command, when executed, loads these display system flip-flops with the base address of the character buffer to be used. Thereafter, all of the first addresses transmitted to the processor memory include the previously determined character buffer base address. The use of multiple character buffers in the processor memory, and the transmission to the display system of a character buffer base address when a CRT-Enable command is executed, permits instantaneous changes in the overall display and the saving of a previously composed message while a new message is displayed in the event the previous message will soon be needed once again.

The first CRT-Enable command not only turns on the display system (by causing the processor to interrupt its operation at the start of each cycle so that the processor memory can be interrogated twice by the display system), it also selects the character buffer to be used. Each subsequent CRT-Enable command is operative to change the character buffer to be used; the display system is not turned on by the command since it is already on. The display system is only turned off by the execution by the processor of the CRT-Disable command.

In the description above, a single dot pattern storage area was assumed. The dot pattern storage area consists of five dot patterns for each of 64 different characters. Although the character set can be altered simply by changing the various dot patterns (data words) in the dot pattern storage area, in some applications it may be necessary to provide for more than one character set of 64 different characters. For example, it may be necessary to provide two 64-character sets. For this reason, an additional aspect of flexibility is provided for in illustrative embodiment of the invention. Consider the case in which two dot pattern storage areas are utilized. The character buffer which is in use contains 128 character codes. it will be recalled that during any cycle, after the first address is transmitted to the processor memory, a character code is sent back to the display system. This character code is then combined with line information represented by the display system counter (the line information being the identity of one of the five lines in the character position under consideration), and the second address which is thus formed and transmitted to the processor memory identifies a location in a dot pattern storage area. If two dot pattern storage areas are utilized, it is necessary to identify in the second address transmitted to the processor memory not only a specific one of the locations in the dot pattern storage area to be interrogated, but also the identity of the dot pattern storage area itself. For this reason, the character code which is stored in each location of a character buffer includes two types of bit information. The first type represents the base address of the dot pattern storage area to be interrogated. The second type is a code representative of a particular character stored in this area. The second address transmitted to the processor memory from the display system thus fully identifies the required line for any one of 128 different characters rather than only 64. It is thus possible to select a particular character set from several different character sets simply by storing the appropriate dot pattern storage area base address in every location of each character buffer. It is even possible to mix character sets (so that the resulting display may include some characters in one 64- character set and some characters in another) simply by storing different dot pattern storage area base addresses in different locations of the same character buffer.

The CRT itself is a modified television unit. The yoke is rotated 90° and the sweep circuits are converted from synchronized to triggered circuits. That is, instead of the sweep circuits being synchronized to external sync signals, each retrace is triggered (under control of the display system counter). As will be described below, the time of the slow sweep is the same as it is in a television receiver. The time of the fast sweep is lengthened although, as will be apparent to those skilled in the art, this simply entails the change of a time constant. The magnitudes of both sweeps are adjusted in accordance with the size of the desired display. It is the use of a conventional television unit, with minor modifications, that to a great extent contributes to the low cost of the overall system. As will be described below, the rotation of the yoke by 90° so that the fast sweeps are in the vertical direction reduces the memory capacity required for each dot pattern storage area.

It is a feature of our invention to provide, in a processor-display system, character buffers and dot pattern storage areas in the processor memory, the character

codes represented in a character buffer and the dot patterns stored in a dot pattern storage area both being alterable under program control.

It is a further feature of our invention to provide a counter in the display system which counts in synchronism with sweeps across the face of a CRT, the state of the counter at any time representing a character position on the display and a particular one of the line segments to be swept through the character position.

It is a further feature of our invention to retrieve the dot pattern for each line segment in the display by interrogating the processor memory twice in succession — a first time by interrogating a character buffer in accordance with the character position represented by the counter in order to derive a character code, and a second time by interrogating the dot pattern storage area in accordance with the character code and the line to be displayed at the character position in order to derive a dot pattern for the line.

It is a further feature of our invention to allow the display system to be turned on (by permitting direct addressing of the processor memory by the display system) only subsequent to the execution of a CRT-Enable command, the display system being turned off by the execution of a CRT-Disable command.

It is a further feature of our invention to provide two or more character buffers in the processor memory, the execution of a CRT-Enable command causing the display system subsequently to address an identified one of the character buffers during the first interrogation of the memory in each cycle.

It is a further feature of our invention to provide two or more dot pattern storage areas, with each location in a character buffer including a dot pattern storage area base address so that a selected one of the dot pattern storage areas can be interrogated during the second interrogation in each cycle.

It is a further feature of our invention to provide a special 1-bit code in each character code data word transmitted to the display system for controlling the blanking of the CRT to thereby conceal a character.

It is a still further feature of our invention to provide a television-type display in which the fast sweeps are in the vertical direction, and both of the fast and slow sweeps are triggered sweeps under control of the display system counter.

Further objects, features and advantages of our invention will become apparent upon consideration of the following detailed description in conjunction with the drawing, in which:

FIG. **1** depicts the form of the CRT display;

FIG. **2** illustrates a character buffer area and a dot pattern storage area of the processor memory;

FIG. **3** illustrates symbolically the manner in which the display is controlled;

FIGS. **4** and **5**, with FIG. **4** being placed to the left of FIG. **5**, is a timing diagram illustrating certain timing aspects of the display system operation;

FIG. **6** depicts symbolically other aspects of the timing of the system operation; and

FIGS. **7** and **8**, with FIG. **7** being placed to the left of FIG. **8**, depicts the illustrative embodiment of the invention.

GENERAL DESCRIPTION — FIGS. 1–3

As shown in FIG. 1, the CRT display consists of four rows RWO-RW3 each having 32 character columns CCO–CC31. Each row comprises 16 horizontal grid lines and each character column consists of eight vertical line sweeps LO–L7. The CRT sweeps are the converse of the conventional television sweeps; the fast sweep is in the vertical direction and the slow sweep is in the horizontal direction. However, as in the television practice, an interlace scanning technique is utilized.

Each vertical scan down the screen is synchronized to a clock. Each time a clock pulse is generated, a dot can be formed on the face of the screen. A total of 16×4 or 64 dot positions appear in each column line of the display. However, in each row, no dots (represented by "X's" in FIG. 1) are generated as the electron beam sweeps through grid lines **0** and **8–15** of each row group **0–15**. In other words, characters are formed only in grid lines 1–7 of each row. Similarly, the electron beam is blanked, that is, no dots can be formed, in vertical lines L5–L7 of each character column. This provides the necessary vertical and horizontal separation between letters or numerals. It is apparent that each letter or numeral comprises selected dots in a 5×7 matrix. The dot patterns for the letters A, N, T, G, K and Q are shown in FIG. 1.

FIG. 2 depicts the overall organization of processor memory 82 (FIG. 8). The memory is a 2K, 8-bit memory; 11 address bits are required to specify any memory location. Memory addresses in FIG. **2** are written in octal code. In octal code, an 11-bit binary address provides a range of addresses from 0 through 3777. The column numbers in FIG. 2 represent the six least significant binary bits in each address (having a range in octal code from 0 through 77), and the row numbers represent the five most significant bits — the hundreds and thousands digits in octal code. For example, address 10010001101 when written in octal code is 2215. In memory location **2215** in FIG. **2** there is stored the octal number **024**. (The various illustrative numbers shown stored in the memory of FIG. 2 are also in octal code. The octal number 024 in binary form is actually 00010100.)

Consider the letter K shown in FIG. **1** in row **RW1** and character column **CC1**. The letter if formed, as are all letters, by sweeps through lines LO–L4 of the associated column. Of the seven positions in each vertical line which can be used to form part of a character, let it be assumed that a 1 represents a dot and a 0 represents the absence of a dot. Since a maximum of only seven "1's" is required to represent a line segment of a character and each memory word has eight bits, the most significant bit is always a 0. The vertical line in the "K" in line L0 can thus be represented as 01111111, where the rightmost portion of the 8-bit sequence corresponds to the top of the line. The dot pattern code for line L1 in the letter "K" is **00001000**. The dot patterns for the next three lines are respectively 00010100, 00100010 and 01000001.

The dot patterns for lines L0–L4 in the letter "K" are shown at the bottom of FIG. 2. The letter "K" can be seen by drawing lines through all of the 1's in the pattern. Of course, since the bit sequences are shown

horizontally rather than vertically, the letter "K" appears to be rotated 90°. Before the electron beam sweeps through line L0 in character column CC1 in the upper half of row RW1, the bit sequence 01111111 is placed in a shift register, and bits are then shifted out in synchronism with the sweep. Consequently, seven dots are formed on the display as shown in FIG. 1. During the sweep through line L1 in the same character position, the bit pattern 00001000 is placed in the shift register and as shown in FIG. 1 only a single dot is formed. Similar remarks apply to the three other bit sequences shown in FIG. 2.

The bit sequences (dot pattern codes) for the letter "K" are contained in memory locations **2015**, **2115**, **2215**, **2315** and **2415** as shown in FIG. 2. For example, the dot pattern code 01111111, which when written in octal code takes the form 177, is stored in memory location **2015**. As another example, the dot pattern 01000001, which when written in octal code takes the form 101, is stored in memory location **2415**. The dot pattern codes for the letters, A, N and G are also shown in FIG. 2 in respective 5-location groups.

As will be described below, the CRT includes a counter which controls the formation of addresses which in turn control the read-out of dot pattern codes from the dot pattern storage area (locations **2000–2477**). Three stages of the counter — H, I and G — determine the octal value in the hundreds positions. For example, if the six low-order bits in the 11-bit address represent octal code **15** (for the character "K") and the two high-order bits represent the value 2 in the thousands position of the octal code (to identify the dot pattern storage area), the three bit values represented by stages H, I and G of the counter represent the digit in the hundreds position of the octal address. As will be described below, the three stages H, I and G are cycled such that they sequence in the order shown by the notations "first" through "eighth" in FIG. 2. (The stages are contained in the counter in the sequence H, I, G.) With interlaced scanning, during each odd sub-frame, sweeps are made through lines Lo, L2, L4 and L6. During each even sub-frame, sweeps are made through lines L1, L3, L5 and L7. In order of significance, as far as identifying a line is concerned, the stages are in the sequence IHG with stage I being the most significant. When the first vertical sweep in any character column is being made, the bits represented by stages IHG of the counter are 000. When the second sweep is being made, the stages represent 010, etc. The notations "-first" through "eighth" in FIG. 2 show the actual order in which lines Lo and L7 are traced. During the first sweep, bits I, H and G represent the digit 0 in the hundreds position of the dot pattern address. During the second sweep, they represent the digit 2. During the third sweep, they represent the digit 4, etc. In this manner, for the letter "K" as shown in FIG. 2, the correct ones of the five dot patterns are read out from memory locations **2015**, **2215**, **2415**, **2115** and **2315** during the first, second, third, fifth and sixth line sweeps through each character column. During the fourth, seventh and eighth line sweeps, that is, the sweeps through lines L5, L6, and L7, bits I, H and G cause memory locations other than those comprising the dot pattern storage area to be identified. (These locations have addresses in the range **2500–2777**). However, no matter what 8-bit words are retrieved from the specified locations, no dot patterns are formed on the screen because the video circuitry is blanked when lines L5, L6 and L7 are being traced. It will be seen from the I, H and G codes for lines L5, L6 and L7 that whenever the I bit is a 1, together with either of the H or G bits being a 1, the video should be blanked. The blanking signal cuts off the electron beam even though during the sweeps through lines L5, L6 and L7 8-bit words are actually transmitted to the CRT shift register and shifted out from this register in the ordinary manner; the three rightmost lines in each character column are always blanked.

FIG. 2 also depicts a character buffer — a 128-word area of the memory. Each word in the character buffer is associated with one of the 128 character positions in the display. Since there are 128 character positions in the display, 7 bits are required to identify them. The five low-order bits identify the columns CCo through CC31 and the two higher order bits identify rows RWO through RW3. In the counter from which the 7 bits are derived, the high-order stages precede the low-order stages. That is, the row identification cycles from **0** through **3** before an advance is made in the column identification. This is as desired since sweeps are made in the vertical direction. After four sweeps are made through lines L0, L2, L4 and L6 in any column, an advance is made to the next column where the same four line sweeps occur. After the odd sub-frame, the entire sequence is repeated but this time sweeps are made through lines L1, L3, L5 and L7 in each column. This will become apparent upon consideration of FIG. 3 which shows how the two addresses required during each cycle are formed.

The CRT unit includes a counter having **16** stages bearing the designations shown at the top of FIG. 3 and being ordered in the sequence A through G. The system clock pulses are applied to the input of stage A. The clock pulses are synchronized to the vertical sweeps down the face of the CRT. Stages A, B, C and D provide a total of 16 counts in the time that it takes to sweep vertically through one of the four rows RWO–RW3. The time period between successive clock pulses corresponds to the distance that the electron beam moves downward in FIG. 1 between two of the horizontal grid lines.

Stages E and F represent one of the four rows RWO–RW3. It is thus apparent that the six stages A–F define the position of the electron beam in the vertical dimension, that is, they define one of the 16×4 or 64 horizontal grid lines.

From a theoretical point of view, following a cycle of **64** counts it would be possible to start counting another sequence corresponding to the next vertical trace. However, it takes time for the electron beam to retrace to the top of the display. For this reason, a "dummy" stage Q is introduced between stages F and H. After stages A–F cycle from 0 to 63, the count is returned to 0 and stage Q is switched to the 1 state. Stages A–F then start their cycle once again, and shortly thereafter the sweep returns to the top of the display. A logic circuit in the CRT system determines when stages A–Q have counted to a maximum value of 96. At this time, all of stages A–Q are reset in the 0 state and the state of stage H is switched. In this manner, stages A–Q are ena-

bled to cycle once again after stages H–G have been advanced to control a sweep through the next line. As will be described below, of each cycle of 96 counts (0–95) the fast sweep occurs during counts 10–87, and the retrace occurs during counts 88–95 of the cycle and counts 0–9 of the next cycle. The actual display is formed during counts 17–71.

It should be noted that the vertical sweep does not begin precisely when all of stages A–Q are reset to 0. In fact, the sweep circuitry is synchronized to the counter only insofar as the start of the retrace begins. After stages A–F have represented a count of 63, with the generation of the next clock pulse they recycle to 0 and stage Q is switched to the 1 state. Shortly thereafter, with a total count of 88, the retrace begins. The actual flyback time depends on characteristics of the sweep circuit. The next vertical sweep actually starts at a count of 10 during the next cycle, and the next line display actually starts at a count of 17. Provided that the retrace time is constant during each cycle, stages A–Q will represent a count of 17 to start a new line display when every sweep is at the same horizontal position on the screen.

It should also be noted that the blanking signal which turns off the electron beam is derived from various sources. For example, the video is blanked during the fast retrace, at the beginning and end of each vertical sweep when no character segments should be displayed, while the sweep is passing between characters (horizontal grid lines **0** and **8–15** in each row), and while sweeps are made through lines L5, L6 and L7 in every character column.

The system necessarily includes both vertical and horizontal sweep circuits. Stages H, I, J–N and G determine the horizontal position of each fast (vertical) line sweep. Stages J–N define one of the character columns CC0–CC31 and stages H, I and G define one of the seven lines L0–L7 within the column. Stages H and I precede stage J, while stage G follows stage N (for the moment stage 0 can be ignored). At the start of each odd sub-frame, all of stages H–G are reset in the 0 state. Consequently, the eight stages define character column CC0 and line L0. Following the first line sweep, and after all of stages A–Q have been reset and stage H has been advanced to the 1 state, character column CC0 is still defined by stages J–N but now line L2 is defined rather than line L0. Of the three bits H, I and G which define lines L0–L7, bit H has a binary weight of 2. Consequently, at the start of the second line sweep, stages H, I AND G define binary number 010. This represents decimal 2. The first line sweep (when the three bits represent a decimal 0) corresponded to line L0. The second sweep corresponds to line L2. This is because with interlaced scanning every other line is swept through during any sub-frame as in conventional sweep circuits.

After the second sweep (of line L2, line L1 being skipped during the first sub-frame), stages H, I and G, in their weighted order of IHG, represent the binary number 100. Since this represents a decimal 4, following the display of line L2 there occurs a display of line L4. At the end of the third sweep, stages H, I and G represent the binary number 110 (in the order IHG) and the fourth line which is swept is line L6. As shown in FIG. 2, the display is blanked at this time.

Stages H and I are then reset to 00, and stages J–N are advanced to represent 10000 (character column CC1). Since stages H, I and G now represent the binary number 000, line L0 is swept in character column CC1. During the next three sweeps, stages H and I are advanced from 00 through 11 and lines L2, L4 and L6 are swept in character column CC2. Thereafter, stages J–N are advanced to represent 01000 while stages H, I and G are in the 0 state. The sequence begins all over again with lines L0, L2, L4 and L6 being swept in character column CC2. This process continues until stages H–I, J–N and G represent the binary numbers 11, 11111, 0. (Stage 0 is still reset.) At this time, line L6 in character column CC31 is displayed.

Following the sweep through this line, since stages A–F represent 111111, they are reset and stage Q is switched to the 1 state. The vertical retrace following the last sweep in the sub-frame begins. At a count of 96, all of stages A–Q are reset and a trigger pulse is extended to stage H. Since stages H–N represent 1111111 at the start of the sweep, the trigger pulse at the input of stage H resets all of them and stage 0 is switched to the 1 state to signal that the horizontal (slow) retrace is required. At the same time, the video is blanked. Several vertical sweeps then take place and not only do stages A–I advance but so do some of the five stages which represent the character column. When the count of stages H–O has reached a value of 136 and stages E and F have advanced to the 1 state as well, the slow retrace is triggered. When stages H–O represent a count of 153, they are all reset and a stage G is triggered and switches to the 1 state to represent an even sub-frame. The first sweep in character column CC0 then begins and the video is unblanked. The sweep is through line L1 since stage G is in the 1 state. In every character column sweeps are made through lines L1, L3, L5 and L7.

Stage 0 serves a function similar to that of stage Q. It will be recalled that stage Q allows a count in excess of 64 for each fast sweep to account for the fast retrace time. Stage 0 allows a count in excess of 128 for each sub-frame to account for the slow retrace time. Stage 0 also serves to blank the video until the horizontal retrace is completed, and in fact until the slow sweep has actually begun and is in its linear region.

During even sub-frames, lines L1, L3, L5 and L7 are swept in each column character. For proper interlacing, the sweep for line L1 in character column CC0 should begin at some point in the horizontal sweep which is slightly after that point in the horizontal sweep at which the sweep through line L0 in character column CC0 began during the previous (odd) sub-frame. The state of stage G determines the two respective counts through which stages A–O must cycle before a slow retrace trigger signal is generated and before all stages are reset (with stage G being triggered) to start the display of a new sub-frame. At the end of every even sub-frame, the retrace trigger is generated at an earlier count than in the case of the odd sub-frame, and all stages are reset when stages H–O reach a count of 152 rather than 153 as in the case of the odd sub-frame. As will be described below, this provides for proper interlacing. Thus stage G not only controls whether odd or even lines are displayed in every character column, it also controls the generation of the

horizontal trigger pulses and the start of each subframe display at different times during alternate subframes so that proper interlacing will be present.

A first 11-bit character position register is provided for identifying a memory location in the character buffer. This register is shown symbolically on FIG. 3. The two most significant bits (2^{10} and 2^9) in the register are 0, the next two bits are labeled P1 and P0, and the seven low-order bits are those represented by stages F–J in the overall counter comprising stages A–G. Bit positions PO and P1 represent the base address of the character buffer. In FIG. 2, the character buffer consists of the 128 memory locations **200–377**. Bit F distinguishes between the 64 locations **200–277** and the 64 locations **300–377**. To fetch a character code from the character buffer shown in FIG. 2, bits P1 and PO must be 1 and O respectively. Thus when bit F is a 0, bit positions 2^8–2^6 represent octal base address **200** and when bit F is a 1 the three bits represent octal base address **300**. The six low order bits E–J represent one of the 64 columns in FIG. 2.

Where the character buffer consists of locations **200–377**, bits P1 and PO must be a 1 and 0 respectively. But it is possible to have additional character buffers in the processor memory. For example, it may be desirable to use one character buffer for actually controlling the display while the system is preparing another character buffer with a new set of character codes. To control the display of the characters represented by the second character buffer, all that would be required is to change bits P1 and PO. The processor is provided with an instruction for changing bits P1 and PO in the 11-bit character position register. If the character buffer shown in FIG. 2 is to be used, the bits **10** are stored in the character position register (in positions 2^8 and 2^7) by the processor. At some other time, if it is desired to use another character buffer for controlling the display, another processor command can be given with another one of the three remaining bit combinations (00, 01 and 11) being specified. The four groups of memory locations which can be used as character buffers are **0–177**, **200–377**, **400–577** and **600–777**.

Bit F in the register is used to identify the first group or the second group of 64 locations in the character buffer being used to up-date the display. (Bit F controls a selection of the "hundreds" digit (**200** or **300**, in the example of FIG. 2). Since in the actual counter stage E precedes stage F, of the two stages E and F which identify rows RWO–RW3 of the display, stage F is the most significant. It is for this reason that the bit represented by stage F identifies either the first group of 64 locations (row **200**) or the second group (row **300**) in the character buffer. The bit represented by stage E represents the first 32 or the last 32 locations of the 64 identified by bit F. Finally, of the 32 locations identified by bits E and F, the bits represented by stages J–N identify one location.

Stages E, F and J–N cycle in a sequence and are incorporated in the character position buffer in an order such that if the 128 characters in the display are numbered as

1 2 3.....32
33 34 35...64
65 66 67...96
97 98 99..128

then the character representations should be stored in the character buffer in the sequence

200: 1,2,3...32,33,34,35...64
300: 65,66,67...96,97,98,99...128.

When stages A–D represent a count of 0000 during each 16-count cycle, the address represented in the 11-bit character position register is transmitted to the address net of the processor. This occurs during a processor phase designated **I01**. It is the first thing which occurs during the phase, and the designation **I01–A** is used in FIG. **3** to show it.

At the end of phase **I01**, as indicated by the notation **I01–B**, the processor transmits an 8-bit word to the CRT which is used to form the address of the location from which the next dot pattern can be retrieved. The dot pattern address register also has eleven stages, and the CRT data delivered during subphase **I01–B** is stored in bit positions 2^0–2^5, 2^9 and 2^{10}. The most significant bits transmitted represent the character type and these bits comprise a dot pattern storage area base address. The dot pattern storage area in FIG. **2** has a base address of **2000**. For an octal value of 2 in the thousands positions, the two most significant bits in the overall address must be 10. Assuming that at most two dot pattern sets will be required, the most significant bit in the dot pattern address register can always be a 1 (as shown in FIG. **3**) with the bit in position 2^9 being set to a 0 or 1 depending on the type of character set to be displayed. If bit 2^9 is a 1, rather than a 0, then the dot pattern storage area will comprise memory locations **3000–3477**. Of course, if two dot pattern sets are stored in the memory, a considerable portion of the total memory is necessarily allocated to the storage of dot patterns. The important thing to note is that to control the display of a different character set all that is required is to control the processor to write the appropriate 2^6 bit in each of the 128 locations in the character buffer in use. (Characters in different sets can be mixed in the display if different dot pattern base address bits are written in the two most significant positions of the various words in the character buffer.)

The second part of the CRT data transmitted back to the display system during sub-phase **101–B** is a 6-bit address which identifies one of the 64 columns **0–77** in FIG. **2**. For example, if the 6-bit address in octal code represents the number **15**, then the letter "K" will be displayed; referring to FIG. **2**, if the two most significant bits in the dot pattern address represent octal value 2 (for the thousands position) and the six least significant bits in the dot pattern address represent octal value 15 (for the units and tens positions), then depending on the value in the hundreds position (determined by stages I, H and G) one of the five dot pattern codes for the letter "K" will be called from the memory during phase **I02** of the processor. As shown in FIG. **3**, the two most significant bits in the overall address in effect identify the character set, while the six least significant bits identify one of 64 possible characters, and one of five (actually eight, but three are not used) dot pattern codes for this character.

The eighth bit (2^7) in the character code is not required for deriving a dot pattern address. Instead, as will be described below, it is used to blank the CRT in the case of a "concealed" character. This bit is not shown as being transmitted during sub-phase **I01–B** on FIG. **3**, although it is transmitted and used as will be described with reference to FIGS. **7** and **8**.

The bit values represented by stages I, H and G are actually used to specify the address of a particular dot pattern code — these three bits determine which line in the character is to be displayed. Referring to FIG. 2, since bit I is the most significant and bit G is the least significant of the three bits which define line numbers L0–L7, the bit values are represented in stages 2^8–2^6 of the dot pattern address register as shown.

At the start of phase I02, as shown by the designation 102–A, the dot pattern address formed during phase I01 is sent to the address net. This dot pattern address is used to retrieve the dot pattern code for the line segment to be displayed and in sub-phase I02–B the 8-bit word (the most significant bit of which is always 0) is prepared for storage in the shift register. The clock pulses are later used to shift the bits out serially through a gate to the video circuit. However, the gate operates only if a blanking signal is not developed. As will be described below, bits are shifted out of the register even when they are not to be displayed. It is for this reason that a blanking signal is required.

It is the clock pulse which causes all of stages A–D to be reset that controls the transmission of an address to the memory to fetch a character code. By the time the character code comes back and is used to form part of the dot pattern address, the dot pattern address is sent to the memory and the dot pattern code is transmitted back to the CRT, stages A–D are no longer in the 0000 state. The dot pattern code is stored in the shift register and is not shifted out of the register to the video circuit until the next cycling of stages A–D. Thus it would appear that the actual display lags behind the counter. In fact, this is true but it is of no moment; it simply means that the entire display is "moved" downward relative to where it would be were there no delay between the initial fetching of a character code and the actual formation of a character line. It should also be noted that each 8-bit dot pattern code results in a 16-dot position display, the last eight of which are always blanked. Each transmission back and forth between the CRT and the memory controls a single 16-dot position display even though only an 8-bit word is sent to the display system. This is because the last 8 bit positions of each 16-bit position display are blanked. The timing is controlled by stages A–D which cycle through a total count of 16 (not 8) each time that only 8 bits are shifted out of the shift register.

The CRT itself is similar to commercially available television units except that the yoke is rotated 90° so that the fast sweep is vertical. Were the yoke not rotated, more memory would be required to store the dot pattern codes. For each character, seven (8-bit) words would be required, one word for each of the horizontal lines in the character. Three of the eight bits in each word would not be used since the last three bit positions of each 8 × 8 matrix are always blanked. On the other hand, by rotating the yoke, only five (8-bit) words are required, with only one bit in each word not being used. The fast and slow sweep rates of the CRT are adjusted to the frequency of the system clock, as will be described. Also, the sweep circuits are of the triggered type rather than of the synchronized type as in conventional television receivers.

SYSTEM TIMING — FIGS. 4–6

FIG. 6 depicts various timing aspects of the fast line sweeps which are made across the face of the CRT. The line sweeps are in the vertical direction from the top of the screen to the bottom of the screen; the slow sweep is from left to right. The border of the display itself is shown in heavy outline. FIG. 6 will be most helpful in an analysis of the slow sweep circuit and the manner in which the odd and even sub-frames are interlaced. But first the fast sweep timing will be considered. Although the timing circuits themselves will be described with reference to the illustrative embodiment of the invention shown in FIGS. 7 and 8, an understanding of the system timing insofar as the fast sweeps are concerned can be appreciated from the symbolic drawing of FIG. 3 and the timing diagram of FIGS. 4 and 5 (with FIG. 4 being placed to the left of FIG. 5).

It will be recalled that counter stages A–Q of FIG. 3 are synchronized to the fast sweeps. These seven stages can cycle from 0000000 through 1111111 (decimal 127), a total of 128 counts. However, the system includes a logic circuit which controls the resetting of all stages in the 0 state as soon as a count of 96 is reached. Thus the stages actually cycle from a count of 0 through a count of 95; the next count of 96 immediately causes all stages to be reset so that a new cycle begins with a count of 0. At the top of FIGS. 4 and 5, the states of stages A–Q are shown as successive clock pulses are applied to the trigger input of stage A, with each overall binary state depicted in the timing diagram being the state of the system following the leading edge of the clock pulse. Adjacent to each entry for the various register stages is a decimal number indicating the decimal state of the system, the decimal states ranging between 0 and 95 during each complete cycle of the counter comprising stages A–Q.

As soon as the counter represents a count of 88, a fast retrace trigger pulse is generated. This shown in FIG. 5 as controlling the start of retrace. Similarly, in FIG. 6 the fast retrace trigger at the end of each sweep is shown as occuring when stages A–Q represent a count of 88.

During the retrace, stages A–Q are still cycled. After a count of 95, all of the stages are reset and they start counting from 0 once again. This occurs while the retrace is still in progress as is shown in FIGS. 4 and 5.

At the same time that the retrace is taking place, a first call is made. The 11-bit address stored in the character position register is transmitted during phase I01 to the address net of the processor. With a clock rate of approximately 1 microsecond (the exact clock rate will be discussed below), it requires 8 microseconds before the counter advances from a count of 0 to a count of 8. During these 8 microseconds, the first CRT data is transmitted from the processor and stored in the dot pattern address register. The exact time when this is accomplished depends on when phase I01 of the processor occurs but a call and a response are always made sometime between counts of 0 and 8. The call is controlled by the state of stage D in the counter. Whenever this stage is in the 0 state, a call is made. The second call is thus made when the total count is somewhere in the range 16 through 23. Similar remarks apply to calls 3–6. Of course, only four calls are required for each line sweep, namely calls

1–4. The last two are ignored as will be described below.

Each of phases I01 and I02 of the processor requires 1 microsecond for execution. Thus 2 microseconds are required for each complete call: 1 microsecond for phase I01 and another microsecond for phase I02, with the final dot pattern being stored in a buffer register (not shown in FIG. 3) by the end of phase I02. While FIG. 3 shows the dot pattern received from the memory as being loaded in the shift register, in reality it is stored in a buffer. It is only when stage D switches to the 1 state that the shift register is loaded from the buffer as will be described with reference to FIGS. 7 and 8. Thus the shift register is loaded at counts of 8, 24, 40, etc. — whenever stage D switches from the 0 state to the 1 state.

Although the shift register is loaded when stage D switches to the 1 state, no bits are shifted out of the register at this time. Instead, the bits in the shift register are shifted out to control the formation of dots in the display at the same time that a call is made for the next dot pattern. Thus between the successive calls, during counts 8 through 15, 24 through 31, etc., nothing should be displayed on the CRT and a blanking signal is generated. This blanking signal, controlled by stage D being in the 1 state, cuts off the electron beam in the CRT. It is only when stage D is in the 0 state that the CRT is unblanked and any 1's which are shifted out of the shift register can control the formation of respective dots in the display.

The system is provided with a shift flip-flop, the state of this flip-flop determining whether or not any bits are shifted out of the shift register under control of the clock pulses. Only when the shift flip-flop is set can bits be shifted out of the register. The setting of the shift flip-flop is controlled when stage D is in the 0 state and stage A switches to the 1 state. This occurs at counts of 1, 17, 33, etc. The resetting of the shift flip-flop is controlled by stage D switching to the 1 state, at counts of 8, 24, 40, etc. Thus the shift flip-flop remains set only during 7 clock periods out of every 16 clock periods. It will be recalled that although each data word in the memory is 8 bits in length, only the first 7 bits which are shifted out of the shift register contain dot pattern information. The eighth bit is always a 0 as shown in FIG. 3. For this reason, only 7 clock periods are required for the shifting; the eighth bit stored in the register need not be shifted out of the register since it never controls the display of a dot. It should also be noted that in FIG. 1 the top row in each 8×8 character position is shown as being blanked. This corresponds to the delay in the shifting by one clock period after stage D switches to the 0 state and the blanking signal controlled by this stage is removed. Following each character display, the CRT is blanked for 8 clock periods, and an additional (ninth) clock period while the blanking signal controlled by stage D is removed but the shift flip-flop is not yet set.

In addition to the blanking signal controlled by the state of stage D, an additional blanking signal is controlled by an F-blank flip-flop. This flip-flop is set when stage Q is in the 1 state and stage E first switches to the 1 state. This occurs at a count of 80. The flip-flop remains set to blank the CRT until a count of 16 is reached — when stage Q is in the 0 state and stage E first switches to the 1 state. Thus, despite the fact that the shift flip-flop is set during clock times 1 through 7, and 81 through 87, the bits which are shifted out of the shift register are not displayed because the CRT is blanked under control of the F-blank flip-flop. Effective shifting occurs only during clock periods 17–23, 33–39, 49–55, and 65–71. During these respective time intervals, the bit patterns which are shifted out of the register correspond to those retrieved during calls 1 through 4. This is as required because it is the first four calls in each overall cycle which correspond to the four character rows of the display. The fifth dot pattern retrieved is stored in the shift register and shifted out of it during clock times 81–87. But at this time the F-blank flip-flop insures that the CRT is blanked. Similarly, the sixth dot pattern stored in the shift register toward the end of each cycle is shifted out of the register at the start of the next cycle, but once again the F-blank flip-flop blanks the CRT. The fifth and sixth dot patterns are actually the same as the first and second dot patterns respectively since bits E and F identify the row containing the character to be displayed and by the second time that stages E and F start recycling at 00 during each overall count from 0 through 95, the stages of the overall counter following stage Q have not been advanced. Consequently, the same character positions are identified during calls 5 and 6 as are identified during respective calls 1 and 2. While the same dot patterns are thus stored in the shift register, they are not used because of the blanking of the CRT by the F-blank flip-flop.

It should be noted that the retrace starts at a count of 88 and terminates by the end of clock period 9 in the next cycle. The fast sweep starts with a count of 10. This allows the fast sweep to progress until the counter represents a count of 17 before any part of the display is actually formed since it is only at a count of 17 that shifting out of the shift register begins. Allowing the fast sweep to progress in this manner before the display starts insures that the sweep is most linear during the actual display portion of each cycle. The exact time that the retrace terminates and the fast sweep begins is not important. Starting the sweep earlier or later would simply shift the entire display up or down on the face of the CRT.

As shown in FIG. 5, when stages A–Q represent a count of 95, the next clock pulse cycles them to represent a count of 96. Immediately, all of the stages are reset to represent 0's, and a trigger pulse is extended to stage H. A count of 96 is detected when stage Q is in the 1 state and stage F switches from the 0 to the 1 state. These stages are immediately reset and the succeeding stages of the counter are advanced. Since stages A–Q are as they were when call 1 was generated, another call is made for row 1, but because stage H has now been triggered the call is for the next line in row 1 in the sub-frame being displayed.

FIG. 6 shows each fast sweep as starting when stages A–Q represent a count of 10 as depicted in FIG. 4. When stages A–Q represent a count of 16, the F-blank flip-flop is reset so that dots can be displayed on the face of the CRT. It is when stages A–Q reach a count of 17 that the first bit which can control the display of a dot is actually shifted out of the shift register. The upper bound of the display is thus controlled by stages

A–Q representing a count of 17. The last shift of a bit out of the shift register during each overall cycle occurs during clock period **71**. Thus, when stages A–Q represent a count of 71 the last effective shift takes place; the lower bound of the display is coincident with the horizontal line on FIG. **6** labeled "last effective shift". The F-blank flip-flop is set at the start of count **80** and nothing more can be displayed even if any bits are shifted out of the shift register and even if the blanking signal controlled by the state of stage D is not developed. Finally, when a count of 88 is reached, the retrace begins. The fast sweep thus takes place during counts 10 through 87 — for a total of 78 counts. The retrace takes place during counts 88 through 95 of one cycle and during counts 0 through 9 of the next cycle for a total of 18 counts. This is shown in FIG. **6**: along the X-axis, the distances between the upper left end of each fast sweep and the lower right end, and between the lower right end of each sweep and the upper left end of the next sweep in the same sub-frame, are in the ratio 78:18.

FIG. **6** shows the interlacing of the lines in the odd and even sub-frames. There are 153 line sweeps in each odd sub-frame (**01–0153**) and 152 line sweeps in each even sub-frame (**E1–E152**) for a total of 305 line sweeps in each frame. The display itself consists of 256 line sweeps (**01–0128** and **E1–E128**) with each even line following the same numbered odd line. The line number is determined by stages H–G. Stages J–N represent one of 32 columns, and stages H and I represent one of the four lines **L0**, **L2**, **L4**, **L6**, or **L1**, **L3**, **L5**, **L7** (depending on the state of stage G). It is the state of stage G which determines whether an odd or even sub-frame is taking place. Stages H–N cycle from a count of 0000000 through a count of 1111111 (**127**) after which they are reset and stage 0 is switched to the 1 state. Fast sweeps continue to be generated and at the end of each sweep stage H is triggered. Stages H–N start to cycle once again from their initial states. When a predetermined count is reached, a slow retrace pulse is generated. A different count generates the trigger pulse during odd and even sub-frames. During the retrace, stages H–N continue to cycle and when another predetermined count is reached (152 in the case of an even sub-frame, and 153 in the case of an odd sub-frame), all of stages H–O are reset and stage G is triggered to switch states. At this time, a sweep is made through the first line of the next sub-frame.

The leftmost and rightmost bounds of the display are along lines **01** and **E128**. Since stages H–N cycle from a decimal count of 0 through a decimal count of 127, stage 0 is switched to the 1 state after 128 lines have been swept in each sub-frame. Stage 0 is not reset until the last line in the sub-frame (**E152** or **0153**) is completed, at which time all of stages H–O are reset. Stage 0 is thus in the 0 state only when the lines which are being formed are within the bounds of the display. For this reason stage 0 is used to develop a blanking signal; when stage 0 is set in the 1 state, the lines sweeping across the face of the CRT are to the left or the right of the display area and the CRT is blanked even though characters would otherwise be formed on the face of the CRT as determined by stages A–Q of the counter and as depicted in the timing waveforms of FIGS. **4** and **5**.

During an even sub-frame, while stage G is in the 1 state, the CRT is blanked at the end of line sweep **E128**, but the slow retrace trigger signal is not generated until some time during the fast retrace following line sweep **E136**. During sweep **E136**, stages H–O represent a count of 135. Twelve counts after the end of the sweep, when the counter stages advance to represent a count of 136 (with stages A–Q being reset after they reach a count of 96 and a trigger pulse being extended to stage H), a slow retrace trigger pulse is generated to signify the end of the even sub-frame. This is shown in FIG. **6** by the dashed line extension of line sweep **E136**. The horizontal retrace begins but vertical sweeps still take place. These vertical sweeps, all the way to the left of the screen, are not shown on FIG. **6**. Some of the vertical sweeps take place during the actual horizontal retrace and others take place after the slow sweep has begun once again, The last two line sweeps in each sub-frame are shown at the left side of FIG. **6**. In the case of an even sub-frame, the last two lines which are swept are **E151** and **E152**. While line **E152** is being formed, stages H–O represent a count of **151**, and since an even sub-frame is still in progress stage G is in the 1 state. As soon as stages A–Q cycle to a count of 96 and then immediately are reset to a count of 0, all of stages H–O are reset and stage G is triggered so that it switches from the 1 state to the 0 state. This is indicated in FIG. **6** by the notation: "H–O=151, G=1; when A–Q → **96(0)**, H–O → 0 and G → 0". With all of stages H–O reset and stage G in the 0 state, it is apparent that the next vertical trace is through line **01**--- the first line in the odd sub-frame. In the usual manner, stages A–Q cycle from an initial count of 0 to a count of 16 at which time the F-blank flip-flop is reset, and at a count of 17 effective shifting begins.

The odd sub-frame now takes place but unlike the case of an even sub-frame the slow retrace trigger pulse is not generated 12 counts after the end of the 136th sweep in the sub-frame. Instead the slow sweep continues and the initial portion of line **0137** is formed. At this time, stages H–O represent a count of 136 and stage G is in the 0 state. It will be recalled that stages A–Q cycle from 0 to 96 each time that the count represented by stages H–O advances by unity. The slow retrace trigger pulse is not generated during an odd sub-frame until stages A–Q represent a count of 48. (This occurs when stages E and F are both first in the 1 state). It is only when stages A–Q reach a count of **48** during the sweep through line **0137** in the odd sub-frame that the slow retrace trigger pulse is generated. At this time the slow retrace begins even as the vertical sweep through line **0137** continues. (The CRT is of course blanked at this time since stage 0 is in the 1 state). As the vertical sweeps continue, the slow sweep begins once again; the last two vertical sweeps **0152** and **0153** in the odd sub-frame are shown in FIG. **6**. During the sweep through line **0153** stages H–O represent a count of **152** and stage G is still in the 0 state. During the fast retrace following the sweep, when stages A–Q are reset to 0 and stages H–O are advanced to represent a count of 153, all of stages H–O are reset and stage G is switched to the 1 state. With stages H–O representing a count of 0 and stage G in the 1 state, an even sub-frame begins, with the next line sweep being **E1** as shown in FIG. **6**.

It is thus apparent that during odd and even sub-frames there are two timing differences. The first relates to when the slow retrace trigger pulse is generated and the second relates to the total number of lines in the sub-frame. In the case of an even sub-frame, the slow retrace trigger pulse is generated 12 counts after the end of line sweep **E136**, and stages H–O are reset (with stage G being triggered to indicate the start of an odd sub-frame) after 152 line sweeps. In the case of an odd sub-frame, the slow retrace trigger pulse is not generated until 38 counts (**48–10**) after line sweep **0137** has begun, and stages H–O are not reset (with stage G being triggered) until after 153 line sweeps have taken place. The odd sub-frames include an additional line (line **0158** has no comparable even line); this extra line is necessary for line **E1** to be displaced to the right relative to line **01**. The reason for delaying the generation of the slow retrace trigger pulse in the case of an odd sub-frame by 48 counts (one-half of the fast sweep period) is that if the trigger pulse is delayed as indicated in FIG. **6**, proper interlacing is achieved — with even and odd lines being displaced from each other by the same distance in the horizontal direction.

In a typical processor, each machine cycle is broken up into a number of phases. The number of phases in each cycle depends on the particular instruction to be executed; certain instructions require more phases during certain cycles than other instructions. The processor with which the illustrative display system is utilized requires 1 microsecond for each phase. The maximum number of phases required during any cycle is seven. Ordinarily, the processor operates with no consideration being given to the display system and there is no display. When a display is desired, a "CRT-Enable" instruction is executed. This instruction informs the processor that a display is to be formed. The CRT-Enable instruction also informs the processor to load the character position register (FIG. **3**) with two bits (**P1** and **P0**) which identify the character buffer in the memory to be used to control the display. Following a CRT-Enable command, the processor adds two phases during each machine cycle — the phases designated as **I01** and **I02**. During phases **I01** and **I02**, the processor ceases to operate in its usual manner. Instead, two 1-microsecond pulses are extended over two respective conductors to the display system to identify phases **I01** and **I02**. During these two phases, addresses and data are transmitted back and forth between the display system and the processor memory as described above with reference to FIG. **3**. The processor memory can be directly accessed from an external source of addresses during phases **I01** and **I02**, and is operative to transmit 8-bit data words over a cable to the external system during these two phases. Such external addressing of the memory and direct transmission to an external system is well understood by those skilled in the art.

With phases **I01** and **I02** now included in each cycle, a maximum of 9 microseconds are required for any cycle. The display system clock is independent of the processor timing. Stage A, the first in the 16-stage counter, is triggered at a fixed rate. Referring to FIGS. **4** and **5**, it is the switching of stage D to the 0 state that initiates a call. The succeeding stages at this time represent a certain count which will control the retrieval of a specific dot storage pattern. Referring to FIG. **3**, the state of stage E in part determines the position in the character buffer which is examined to determine the character which is to be displayed. Stage E must not change state before phase **I01** occurs because otherwise a call will be skipped. (Stage E can change state after phase **I01** because during phase **I02** the state of stage E is not required; the only stages of interest in the formation of the dot pattern address are stages I, H and G.) It is thus necessary that at least one **I01** phase occur during the eight clock periods that stage D is in the 0 state. Since a maximum of 9 microseconds may elapse between **I01** phases, the minimum clock period for the display system is 9/8 microseconds, or 1.125 microseconds. This corresponds to a maximum clock frequency of 888,888 Hz. Since there are 96 clock periods during each fast line sweep and there are 305 line sweeps during each complete frame, the minimum time for each frame is (305)(96)(1.125) microseconds or 32.94 milliseconds. This corresponds to a maximum frame rate of a little more than 33 frames per second. This allows a frame rate of 30 per second to be selected, which is that used in standard television receivers (a sub-frame rate of 60 per second). In the illustrative embodiment of the invention, the basic clock frequency is 878,400 Hz to give rise to a frame rate of 30 per second. Since each clock time is just under 1.14 microseconds, each fast sweep (during which the counter cycles from 0 through 95) requires slightly less than 109.5 microseconds. This time is longer than the conventional fast sweep time in a television receiver but by little more than 50 percent. This allows the conventional fast sweep circuitry to be used with an appropriate change being made in the time constant. Of course, the sweep must be triggered rather than synchronized as in conventional television receivers.

DISPLAY SYSTEM — FIGS. 7 AND 8

In the illustrative system of FIGS. **7** and **8**, various cables are shown by heavy lines. This is intended to indicate that parallel transmission takes place over these paths. Similarly, several of the gates are shown in heavy lines to indicate that in implementing the system a plurality of gates should be utilized. For example, an 8-bit word is transmitted over cable **92** from processor **60** to one input of gate **72**. This gate is provided with another input connected to conductor **I02**. In reality, eight separate gates would be used instead of gate **72**, each having one input connected to conductor **I02** and each having its second input connected to one of the eight conductors in cable **92**. When conductor **I02** is pulsed, gate **72** on FIG. **8** operates to transmit the data word on cable **92** to cable **I02–B**. At this time, each bit is stored in a respective one of stages **B0–B7** of buffer **74**. The operations of the other gates shown in the heavy lines are similar to the operation of gate **72**.

Processor **60** is shown only symbolically as including an address net **80**, a memory **82**, an accumulator **84**, and a control unit **86**. As in conventional processors, the control is connected to all of the various units in the processor to govern their sequential operations. An address transmitted through the address net to the memory determines the location in the memory into which a word is written, or out of which a word is read. During the ordinary operation of the processor, words read from the memory are directed to accumulator **84**

(typically, via other registers) and words in the accumulator can be written into the memory. As described above, a maximum of seven phases are required during each machine cycle depending on the instruction being executed. (The instructions are contained in the memory and are read out in succession and stored in various registers, not shown, the contents of which determine the system operation.)

One of the commands which the processor can execute is a CRT-Enable command. When this command is executed, the control modifies its own operation so that an additional two phases occur at the start of each machine cycle. During these phases — I01 and I02 — the processor ceases to operate in the ordinary fashion. Instead, an address appearing on cable 90 is directed through the address net to the memory and the 8-bit word stored at that address in the memory is transmitted directly over cable 92 to the display system. Also, during each of phases I01 and I02, 1-microsecond pulses are applied by control 86 in the processor to respective conductors I01 and I02.

The CRT-Enable instruction includes a specification for bits P0 and P1. (See the character position register, FIG. 3.) The processor causes the accumulator to transmit these two bits over CRT Enable cable 88 to flip-flops F/F-P0 and F/F–P1. These two flip-flops are set appropriately in order to identify the base address in memory 82 of the character buffer to be used. Either the 0 or the 1 output of each flip-flop is energized to form two of the 11 address bits on the 11 respective conductors in cable 94. In order to select a new character buffer, all that is required is to execute a new CRT-Enable command with new values specified for bits P0 and P1.

Once the CRT-Enable command is executed, the processor injects phases I01 and I02 in each machine cycle until a CRT-Disable command is executed. It is only at this time that the CRT display is turned off and phases I01 and I02 are no longer executed during each machine cycle. In this manner, the extra time required to control the display, during which time the processor does not function in its ordinary mode, is not wasted.

Clock 10 applies clock pulses to the trigger input of flip-flop F/F–A. The 16 flip-flops F/F–A through F/F–G form a counter and function as described with reference to the counter depicted at the top of FIG. 3. Each time a stage switches from the 1 state to the 0 state, a trigger pulse is applied to the input of the succeeding stage.

The cathode ray tube 50 is shown only symbolically as including a fast sweep circuit 56 and a slow sweep circuit 54. Each of these circuits functions to generate a sweep voltage as is known in the art and as described with reference to FIG. 6 responsive to the application of a pulse to its trigger input. The trigger pulse first causes a retrace which is then followed by a sweep. The display of a dot is controlled by gate 46. Whenever the output of the gate is energized, the electron beam is turned on. One input to gate 46 is connected to the output of gate 44. The output of this latter gate is high whenever the display is not to be blanked. The other input to gate 46 is connected to the output of shift register 78. This register comprises eight stages SR0–SR7. Each pulse applied to the shift input of the register shifts the contents of the register to the right with the rightmost bit being shifted out to the input of gate 46. Every bit of value 1 shifted out of stage SR0 of the register causes gate 46 to pulse its output and a corresponding dot to be displayed on the face of the CRT.

Referring to FIGS. 4 and 5, it will be recalled that whenever stage D switches to the 0 state a call is made to the processor memory. The 0 output of stage D is extended to the S input of request flip-flop 68. This flip-flop is set in the 1 state when a positive step is applied to its S input to indicate that a call must be made. In the event the processor cycles are very short, it is possible for there to be two and even three I01 phases during the eight clock times that stage D is in the 0 state. The purpose of the request flip-flop is to control only a single call in such a case. When the 1 output of the request flip-flop goes high, it causes one input of gates 70 and 72 to be energized. During phase I01, conductor I01 is energized to enable the operation of gate 70. Any data which appears on cable 92 from memory 82 are transmitted through the gate to cable I01–B. At the end of phase I01 conductor I02 is pulsed, and since this conductor is connected to the R input of flip-flop 68, the flip-flop is reset. Consequently, gate 70 cannot operate again until the request flip-flop is switched to the 1 state when stage D is switched from the 0 to the 1 state once again. Although an address may be transmitted to the address net several times during successive I01 phases which occur while stage D is in the 0 state, the data which are returned by the processor are not transmitted through gate 70.

Cable 94 is connected to the outputs of flip-flops F/F–E, F/F–F, and F/F–J through F/F–N. The CRT address (character position) which is transmitted to the processor during phase I01 of each cycle, as shown in FIG. 3, consists not only of the bits represented by these seven flip-flops, but also of the P1 and P0 bits, and 0's in positions 2^9 and 2^{10}. Thus cable 94 is shown as also being connected to the outputs of flip-flops F/F–P1 and F/F–P0 and to two grounded conductors. These conductors are merely symbolic and serve to indicate that the two most significant bits in the CRT address are 0's.

Cable 94 is one input to gate 58. The other input to the gate is connected to the 0 output of flip-flop F/F–D. Consequently gate 58 is enabled during the eight clock times comprising each call period in FIGS. 4 and 5. The third input to gate 58 is connected to conductor I01. Thus, it is during the 1-microsecond I01 phase that the CRT address is transmitted through gate 58 and over cable I01–A to one input of OR gate 62. The CRT address is then transmitted over cable 90 to the address net of the processor.

The identity of the character to be displayed is also transmitted during phase I01 from the memory over cable 92 to one input of gate 70. During the first I01 phase that occurs during the call time, the input of gate 70 connected to the 1 output of flip-flop 68 is energized. Since the third input of gate 70 is connected to the I01 conductor, it is during the latter part of the I01 phase that the data from the memory is transmitted through gate 70 over cable I01–B to dot pattern address register 98. As shown in FIG. 3, the six low-order bits of the 8-bit memory word are stored in the low-order positions of the register, namely, in flip-flop stages S–0 through S–5. The 2^6 bit in the data word is

stored in stage S–9 of the character buffer word. Together with stage S–10 of the register (a wired "1"), stage S–9 represents one of two dot pattern base addresses. Since two different character sets are stored in two different dot pattern storage areas (if there are two), the 2^6 bit on the CT conductor connected to flip-flop stage S–9 of the dot pattern address register **98** represents one of two character sets.

Stages I, H, and G of register **98** are shown in the drawing only for the sake of completeness; the register does not include three such physical stages. The I, H, and G bits are represented by flip-flops F/F–I, F/F–H, and F/F–G, and the 0 and 1 outputs of these flip-flops are simply extended to respective conductors in cable **96** so that the complete dot pattern address can be formed.

Immediately after the memory data is stored in register **98**, conductor **101** is de-energized and a 1-microsecond pulse appears on conductor **102**. At this time, request flip-flop **68** is reset, gates **58** and **70** are disabled, and gates **64** and **72** are enabled instead. The dot pattern address on cable **96** is transmitted through gate **64** and over conductor **102–A** to the second input of OR gate **62**. The 11-bit address transmitted over cable **90** to the address net identifies the address of the dot pattern to be displayed when the next call is in progress. The dot pattern is transmitted back over cable **92** and through gate **72** to cable **102–B**. The dot pattern is then stored in buffer **74**. Gate **72** is enabled to operate by both the **102** pulse and the 1 output of the request flip-flop. The **102** pulse resets the flip-flop, but the flip-flop is such that its resetting is delayed slightly after its R input is triggered. This allows the data on cable **92** to be transmitted through gate **72** before the request flip-flop inhibits the gate from further operations before the next call time (D → 0).

When stage D switches to the 1 state at the end of each call, one input of gate **76** is enabled. It is at this time that the contents of buffer **74** are transmitted through the gate to the eight stages of shift register **78**. At the same time, as flip-flop D switches to the 1 state, the R input of shift flip-flop **6** is energized. The 1 output of the flip-flop goes low and gate **26** is disabled. Consequently, clock pulses cannot be transmitted through this gate. Thus, after each call period, there is no shifting. Nor is a shift pulse extended to the shift input of register **78** eight clock periods later when stage D switches to the 0 state at the start of the next call. The switching of flip-flop D to the 0 state energizes one input of gate **14**. But flip-flop F/F-A is in the 0 state at this time and the second input of gate **14** is de-energized. It is the next clock pulse which causes flip-flop F/F–A to switch to the 1 state and the second input of gate **14** to be energized. This sets shift flip-flop **16** in the 1 state and causes one input of gate **26** to be energized. The flip-flop is set before the clock pulse terminates so that the same clock pulse is transmitted through gate **26** to the shift input of register **78**. Consequently, the first bit is shifted out of the shift register during clock times **1**, **17**, **33**, etc. Thereafter, another six shifts take place so that a maximum of seven dots can be displayed on the face of the CRT for each call.

The F-blank flip-flop **22** is used to blank the CRT beginning with clock period **80** and ending after clock period **15** in the next cycle, as shown in FIGS. **4** and **5**. As long as the flip-flop is reset, the 0 output is high and one input of gate **44** is enabled. Provided the other inputs to gate **44** are similarly high, dots can be formed on the face of the CRT. Flip-flop **22** causes the CRT to be blanked when it is set in the 1 state with the operation of gate **18**. One input to gate **18** is connected to the 1 output of flip-flop F/F–A and the other input to the gate is connected to the 1 output of flip-flop F/F–E. Both of these flip-flops are in the 1 state for the first time during each cycle at a count of 80. Consequently, it is at the count of 80 that blanking begins. Blanking ends the first time that gate **20** operates to extend a positive step to the R input of the flip-flop. The two inputs of gate **20** are connected to the 1 output of flip-flop F/F–E and the 0 output of flip-flop F/F–Q. The first time that both inputs to gate **20** are energized following the setting of flip-flop **22** is at a count of 16. Consequently, it is at this time that the F-blank flip-flop is reset so that a display can take place provided that the other four inputs to gate **44** are all high. As seen in FIG. **4**, the first effective shift begins at a count of 17 and consequently by resetting flip-flop **22** at a count of 16 the first dot pattern that is displayed is that corresponding to call **1**. Similarly, because flip-flop **22** is set at a count of 80, referring to FIG. **5**, it is apparent that the last dot pattern that is displayed is that corresponding to call **4**.

A second input of gate **44** is connected directly to the 0 output of flip-flop F/F–D. As shown in FIGS. **4** and **5**, it is only when this flip-flop is in the 0 state that the CRT should be unblanked.

Gate **28** is used to derive the fast sweep trigger pulse. The three inputs to gate **28** are connected to the 1 output of flip-flop F/F–Q, the 1 output of flip-flop F/F–E and the 1 output of flip-flop F/F–D. All three of these flip-flops are in the 1 state for the first time during each cycle at a count of 88. Consequently, as shown in FIG. **5**, retrace begins at a count of 88 with the operation of gate **28** and the application of a positive step to the trigger input of fast sweep circuit **56**. The fast sweep begins at a time controlled by sweep circuit characteristics and, as shown in FIG. **4**, starts at a count of 10. This, of course, assumes that stages A–Q count no higher than to a count of **95**. As soon as clock time **95** (the **96**th clock time in each cycle) is over, stages A–Q represent a count of 96. At this time, all of the stages are in the 0 state except stages F/F–F, and F/F–Q. Both of these stages are in the 1 state and since the two inputs of gate **24** are connected respectively to the 1 outputs of the two flip-flops, this gate operates. The output of the gate is extended back to the reset input of each of the flip-flops and consequently these two flip-flops are immediately reset so that all of stages F/F–A through F/F–Q now represent a count of 0 for the next cycle. The switching of stage F/F–Q from the 1 state to the 0 state causes a trigger pulse to be extended to the input of stage F/F–H. It is this trigger pulse that advances the count of the succeeeding stages and causes the next line in the same sub-frame to be displayed.

Gates **36**, **38** and **40** on FIGS. **7** and **8** control the generation of a retrace trigger pulse for the slow sweep. During even sweeps, stage G is in the 1 state and thus one input of gate **38** is energized. The other two inputs of the gate are connected respectively to the 1 outputs of stages F/F–K and F/F–O. Both of these stages switch

to the 1 state at a count of 136, and with the operation of gate **38** a pulse is extended through OR gate **40** to the trigger input of slow sweep circuit **54**. Thus, during an even sub-frame, the slow sweep circuit is triggered after stages A–Q have cycled to a count of 96(0), the resetting of stage F/F–Q controlling the advance of the count in the succeeding stages to provide a total count of 136. Consequently, as shown in FIG. **6**, the slow retrace trigger pulse during an even sub-frame occurs at a count of 96(0). The dashed extension of line **E136** in FIG. **6** is intended to show that the slow even trigger occurs during the fast retrace following line sweep **E136**.

Gate **36** serves to control the generation of the slow retrace trigger pulse during odd sub-frames. While the 1 output of stage F/F–G is connected to one input of gate **38**, it is the 0 output of the flip-flop which is connected to one input of gate **36**. Consequently, this gate can operate only during odd sub-frames. Two of the other inputs of gate **36** are connected to the 1 outputs of flip-flops F/F–O and F/F–K. Thus gate **36** can operate only during an odd sub-frame when the count represented in stages F/F–H through F/F–G represent a count of **136**, that is, at some time following line sweep **0136**. The fourth and fifth inputs of gate **36** are connected to the 1 outputs of stages F/F–E and F/F–F. Thus it is only when these stages are both first in the 1 state during the sweep through line **0137** that gate **36** can operate. This occurs when stages A–Q have cycled to a count of 48. It is at this time that the pulse at the output of gate **36** is extended through OR gate **40** to the trigger input of slow sweep circuit **54**.

Gates **30**, **32** and **34** control the resetting of flop-flops F/F–H through F/F–O and the triggering of flip-flop F/F–G at the end of each sub-frame. One of the inputs of gate **32** is connected to the 1 output of stage F/F–G. Consequently, gate **32** can operate only during even sub-frames. The other three inputs to gate **32** are connected to the 1 outputs of flip-flops F/F–L, F/F–K and F/F–O. At the end of the sweep through line **E152**, all three of these flip-flops are placed in the 1 state to represent a count of **152**. At this time a step is extended through OR gate **30** to the reset input of each of flip-flops F/F–H through F/F–O. Consequently, all of these flip-flops are reset. The resetting of flip-flop F/F–O from the 1 state to the 0 state causes a trigger pulse to be extended to the input of flip-flop F/F–G; this flip-flop is switched to the 0 state to indicate the start of an odd sub-frame.

One input of gate **34** is connected to the 1 output of flip-flop F/F–G. Consequently, this gate can operate only during odd sub-frames. Three of the other inputs to this gate are connected to the 1 outputs of the K, L and O stages of the counter. These are the same three stages which control the operation of gate **32**. But gate **34** has a fifth input connected to the 1 output of flip-flop F/F–H. Thus the count represented by stages H–O must advance to **153** before gate **34** operates. This occurs at the end of the sweep through line **0153** during each odd sub-frame. With the operation of gate **34**, a reset pulse is transmitted through OR gate **30** once again to control the resetting of stages F/F–H through F/F–O, and the switching of flip-flop F/F–G to the 0 state. Thus the next line which is traced is line E1 in the even sub-frame.

There are five blanking signals, each of which is coupled to a respective input of gate **44**. One of these is the 0 output of flip-flop F/F–D and another is the 0 output of the F-blank flip-flop **22**, both of which have been described. The third input to gate **44** is the 0 output of flip-flop F/F–o. As described with reference to FIG. **6**, only when stage 0 of the counter is reset should the display be formed —during the sweeps through lines **01–0128** and E1–E128.

The fourth blanking signal is derived from stages I, H and G of the counter, as described above with reference to FIG. **2**. The display should be blanked whenever stage I is in the 1 state, and either of stages H or G is in the 1 state. The 1 output of flip-flop F/F–I is connected to one input of gate **42**. The 1 outputs of flip-flops F/F–H and F/F–G are connected to the two inputs of OR gate **52**. Consequently, both inputs of gate **42** are energized when stage I is in the 1 state. and at least one of stages G or H is in the 1 state. At this time the output of gate **42** goes low to blank the CRT. It is only when at least one of the inputs of gate **42** is de-energized that the output of gate **42** remains high so that gate **44** is enabled.

The fifth blanking signal, the 0 output of flip-flop **100**, relates to the use of the eighth bit of each character code data word. It is sometimes desirable to "conceal" a character even though it is represented in the character buffer storage area. This is accomplished by having the processor write a 1 in the eighth (most significant) bit of the character code. It will be recalled that bit 2^7 of the character code is not required to form the dot pattern address. It is thus available for another purpose, namely, to conceal the character.

During sub-phase **I01–B**, the most significant bit in the character code is transmitted over the CC conductor to flip-flop **102**. The 1 output of this flip-flop is connected to the S input of flip-flop **100**. This latter flip-flop switches to the 1 state only if its S input is energized (flip-flop **102** is in the 1 state) when a negative step is applied to the clock (C) input. If the S input is not energized (flip-flop **102** is in the 0 state), the negative clock pulse resets flip-flop **100** in the 0 state.

Since the clock input of flip-flop **100** is connected to the 0 output of flip-flop F/F–D, flip-flop **102** can change state only at counts of 0, 16, 32, etc. (see FIGS. **4** and **5**). Each call is initiated with the start of the first **I01** phase of the processor after flip-flop F/F–D switches to the 0 state. Consequently, the character code is not actually stored in register **98**, and bit 2^7 of the character code does not appear in flip-flop **102** until after flip-flop F/F–D switches to the 0 state. Is is only at the start of the next call, with shifting of a dot pattern for the previously called character, that bit 2^7 of this previously called character code can cause flip-flop **100** to be set in the 1 state. In such a case, the 0 output of the flip-flop is de-energized and gate **44** is not enabled. With the blanking of the CRT, the dot pattern for the previously called character is not displayed. On the other hand, if bit 2^7 of a character code is a 0, then just when shifting of one of its dot patterns begins flip-flop **100** is reset in the 0 state (if it is not already there) to enable gate **44**.

Although the invention has been described with reference to a particular embodiment, it is to be understood that this embodiment is merely illustrative of

the application of the principles of the invention. Numerous modifications may be made therein and other arrangements may be devised without departing from the spirit and scope of the invention.

What we claim is:

1. A processor-display system comprising a processor and a display system; said processor having an externally addressable read-write memory and means for transmitting externally data contained in said memory, said memory including at least one character buffer each location of which contains a code for the particular character to be displayed in a respective position of a display, and at least one dot pattern storage area each location of which contains a data word representative of the dot pattern required for one line of an associated character; said display system having a CRT, a cycling counter, means for causing an electron beam to sweep through successive lines on the face of said CRT in a raster pattern in synchronism with the cycling of said counter, the count in said counter representing a character position on the face of said CRT and a particular line in said character position, means for transmitting to said memory the address of a location in said character buffer in accordance with the character position represented by said counter to control the transmission of a character code from said memory to said display system, means for deriving and transmitting to said memory the address of a location in said dot pattern storage area in accordance with a previously received character code and the particular line represented by said counter to control the transmission of a dot pattern data word from said memory to said display system, and means for controlling the display of a dot pattern corresponding to a transmitted dot pattern data word when said electron beam sweeps through the particular line in said represented character position.

2. A processor-display system in accordance with claim 1 wherein said processor is operative to change the data contained in the locations of said dot pattern storage area under program control.

3. A processor-display system in accordance with claim 2 wherein said processor is operative to change the character codes contained in said character buffer under program control.

4. A processor-display system in accordance with claim 3 wherein said processor normally inhibits the external addressing of said memory and responsive to the execution of an enabling instruction thereafter allows the periodic external addressing of said memory by said display system.

5. A processor-display system in accordance with claim 4 wherein responsive to the execution of said enabling instruction said processor thereafter allows the external addressing by said display system of both a character buffer location and a dot pattern storage area location during each processor cycle.

6. A processor-display system in accordance with claim 5 wherein said processor is responsive to the execution of a disabling instruction for thereafter inhibiting the external addressing of said memory by said display system.

7. A processor-display system in accordance with claim 6 wherein said memory includes at least two character buffers, and further including means responsive to the execution of said enabling instruction for thereafter controlling said display system to address locations in only a specified one of said character buffers.

8. A processor-display system in accordance with claim 7 wherein said memory includes at least two dot pattern storage areas, and the character code contained in each location of a character buffer includes the specification of the base address of that one of said dot pattern storage areas which contains the location to be addressed following the transmission of said character code to said display system.

9. A processor-display system in accordance with claim 8 wherein each character code contained in a location of a character buffer includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern transmitted to said display system from a location whose address was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

10. A processor-display system in accordance with claim 9 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

11. A processor-display system in accordance with claim 10 wherein said CRT is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

12. A processor-display system in accordance with claim 11 wherein said counter includes two series of stages, the count in a first series of stages corresponding to dot positions along any vertical line and the count in a second series of stages corresponding to a line position in the horizontal direction, said electron beam is controlled by said sweep means to retrace at the end of each vertical line sweep and at the end of each horizontal line sweep, and the maximum count in each cycle of operation of each series of stages is reached in a time period equal to the total time required for the respective sweep and the respective retrace.

13. A processor-display system in accordance with claim 12 further including means controlled by said counter for blanking said CRT during horizontal and vertical retraces, and during the time that said electron beam is sweeping through a region of the face of said CRT which is not part of a character position.

14. A processor-display system in accordance with claim 13 wherein said sweep means is controlled by said counter such that said electron beam sweeps across the face of said CRT in an interlaced fashion during successive sub-frames.

15. A processor-display system in accordance with claim 14 wherein said display controlling means includes a shift register for containing each transmitted dot pattern data word, means for shifting bits out of said shift register in synchronism with said counter, and means responsive to the shifting out of said shift register of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

16. A processor-display system in accordance with claim 1 wherein said processor normally inhibits the external addressing of said memory and responsive to the execution of an enabling instruction thereafter allows the periodic external addressing of said memory by said display system.

17. A processor-display system in accordance with claim 16 wherein responsive to the execution of said enabling instruction said processor thereafter allows the external addressing by said display system of both a character buffer location and a dot pattern storage area location during each processor cycle.

18. A processor-display system in accordance with claim 17 wherein said processor is responsive to the execution of a disabling instruction for thereafter inhibiting the external addressing of said memory by said display system.

19. A processor-display system in accordance with claim 18 wherein said memory includes at least two character buffers, and further including means responsive to the execution of said enabling instruction for thereafter controlling said display system to address locations in only a specified one of said character buffers.

20. A processor-display system in accordance with claim 16 wherein said processor is responsive to the execution of a disabling instruction for thereafter inhibiting the external addressing of said memory by said display system.

21. A processor-display system in accordance with claim 20 wherein said memory includes at least two character buffers, and further including means responsive to the execution of said enabling instruction for thereafter controlling said display system to address locations in only a specified one of said character buffers.

22. A processor-display system in accordance with claim 16 wherein said memory includes at least two character buffers, and further including means responsive to the execution of said enabling instruction for thereafter controlling said display system to address locations in only a specified one of said character buffers.

23. A processor-display system in accordance with claim 1 wherein said memory includes at least two character buffers, and further including means responsive to the execution of a predetermined enabling instruction for thereafter controlling said display system to address locations in only a specified one of said character buffers.

24. A processor-display system in accordance with claim 23 wherein said memory includes at least two dot pattern storage areas, and the character code contained in each location of a character buffer includes the specification of the base address of that one of said dot pattern storage areas which contains the location to be addressed following the transmission of said character code to said display system.

25. A processor-display system in accordance with claim 24 wherein each character code contained in a location of a character buffer includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern transmitted to said display system from a location whose address was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

26. A processor-display system in accordance with claim 25 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

27. A processor-display system in accordance with claim 1 wherein said memory includes at least two dot pattern storage areas, and the character code contained in each location of said character buffer includes the specification of the base address of that one of said dot pattern storage areas which contains the location to be addressed following the transmission of said character code to said display system.

28. A processor-display system in accordance with claim 27 wherein each character code contained in a location of said character buffer includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern transmitted to said display system from a location whose address was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

29. A processor-display system in accordance with claim 28 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

30. A processor-display system in accordance with claim 1 wherein each character code contained in a location of said character buffer includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern transmitted to said display system from a location whose address was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

31. A processor-display system in accordance with claim 30 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

32. A processor-display system in accordance with claim 31 wherein said CRT is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

33. A processor-display system in accordance with claim 1 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

34. A processor-display system in accordance with claim 33 wherein said CRT is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

35. A processor-display system in accordance with claim 1 wherein said counter includes two series of stages, the count in a first series of stages corresponding to dot positions along any vertical line and the count in a second series of stages corresponding to a line position in the horizontal direction, said electron beam is controlled by said sweep means to retrace at the end of each vertical line sweep and at the end of each horizontal line sweep, and the maximum count in each cycle of operation of each series of stages is reached in a time period equal to the total time required for the respective sweep and the respective retrace.

36. A processor-display system in accordance with claim 35 further including means controlled by said counter for blanking said CRT during horizontal and vertical retraces, and during the time that said electron beam is sweeping through a region of the face of said CRT which is not part of a character position.

37. A processor-display system in accordance with claim 36 wherein said sweep means is controlled by said counter such that said electron beam sweeps across the face of said CRT in an interlaced fashion during successive sub-frames.

38. A processor-display system in accordance with claim 37 wherein said display controlling means includes a shift register for containing each transmitted dot pattern data word, means for shifting bits out of said shift register in synchronism with said counter, and means responsive to the shifting out of said shift register of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

39. A processor-display system in accordance with claim 35 wherein said sweep means is controlled by said counter such that said electron beam sweeps across the face of said CRT in an interlaced fashion during successive sub-frames.

40. A processor-display system in accordance with claim 35 wherein said display controlling means includes a shift register for containing each transmitted dot pattern data word, means for shifting bits out of said shift register in synchronism with said counter, and means responsive to the shifting out of said shift register of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

41. A processor-display system in accordance with claim 1 wherein said sweep means is controlled by said counter such that said electron beam sweeps across the face of said CRT in an interlaced fashion during successive sub-frames.

42. A processor-display system in accordance with claim 1 wherein said display controlling means includes a shift register for containing each transmitted dot pattern data word, means for shifting bits out of said shift register in synchronism with said counter, and means responsive to the shifting out of said shift register of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

43. A processor-display system comprising a processor and a display system; said processor having an addressable read-write memory and means for transmitting data contained in said memory to said display system, said memory including at least one character buffer each location of which contains a code for the particular character to be displayed in a respective position of a display, and at least one dot pattern storage area containing data representative of the dot patterns required for the characters of a predetermined set; said display system having a CRT, a cycling counter, means for causing an electron beam to sweep through successive lines on the face of said CRT in a raster pattern in synchronism with the cycling of said counter, the count in said counter representing a character position on the face of said CRT, means for transmitting to said memory the address of a location in said character buffer in accordance with the character position represented by said counter to control the transmission of a character code from said memory to said display system, means for deriving and transmitting to said memory address information for data in said dot pattern storage area in accordance with a previously received character code to control the transmission of dot pattern data from said memory to said display system, and means for controlling the display of a dot pattern character corresponding to transmitted dot pattern data when said electron beam sweeps through said represented character position.

44. A processor-display system in accordance with claim 43 wherein said processor normally inhibits the addressing of said memory by said display system and responsive to the execution of an enabling instruction thereafter allows the periodic addressing of said memory by said display system.

45. A processor-display system in accordance with claim 44 wherein responsive to the execution of said enabling instruction said processor thereafter allows the addressing by said display system of both a character buffer location and said dot pattern storage area during each processor cycle.

46. A processor-display system in accordance with claim 44 wherein said processor is responsive to the execution of a disabling instruction for thereafter inhibiting the addressing of said memory by said display system.

47. A processor-display system in accordance with claim 44 wherein said memory includes at least two character buffers, and further including means responsive to the execution of a predetermined enabling instruction for thereafter controlling said display system to address locations in only a specified one of said character buffers.

48. A processor-display system in accordance with claim 47 wherein said memory includes at least two dot pattern storage areas, and the character code contained in each location of a character buffer includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said display system.

49. A processor-display system in accordance with claim 48 wherein each character code contained in a location of a character buffer includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

50. A processor-display system in accordance with claim 43 wherein said memory includes at least two dot pattern storage areas, and the character code contained in each location of said character buffer includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said display system.

51. A processor-display system in accordance with claim 50 wherein each character code contained in a location of said character buffer includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

52. A processor-display system in accordance with claim 51 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

53. A processor-display system in accordance with claim 43 wherein each character code contained in a location of said character buffer includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

54. A processor-display system in accordance with claim 43 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

55. A processor-display system in accordance with claim 54 wherein said CRT is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

56. A processor-display system in accordance with claim 43 wherein said electron beam is controlled by said sweep means to retrace at the end of each vertical line sweep and at the end of each horizontal line sweep, and further including means controlled by said counter for blanking said CRT during horizontal and vertical retraces, and during the time that said electron beam is sweeping through a region of the face of said CRT which is not part of a character position.

57. A processor-display system in accordance with claim 56 wherein said sweep means is controlled by said counter such that said electron beam sweeps across the face of said CRT in an interlaced fashion during successive subframes.

58. A processor-display system in accordance with claim 57 wherein said display controlling means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with said counter, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

59. A processor-display system in accordance with claim 43 wherein said display controlling means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with said counter, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

60. A processor-display system comprising a processor and a display system; said processor having an addressable read-write memory and means for transmitting data contained in said memory to said display system, said memory including at least one character code storage area for representing the particular characters to be displayed in respective positions of a display, and at least one dot pattern storage area containing data representative of the dot patterns required for the characters of a predetermined set; said display system having a CRT, means for causing an electron beam to sweep through successive lines on the face of said CRT in a raster pattern, means for transmitting to said memory address information for character data to control the transmission of a character code from said memory to said display system, means for deriving and transmitting to said memory address information for dot pattern data in accordance with a previously received character code to control the transmission of dot pattern data form said memory to said display system, and means for controlling the display of a dot pattern character corresponding to transmitted dot pattern data when said electron beam sweeps through the character position of said display in which the character corresponding to said received character code should be displayed.

61. A processor-display system in accordance with claim 60 wherein said processor normally inhibits the addressing of said memory by said display system and responsive to the execution of an enabling instruction thereafter allows the periodic addressing of said memory by said display system.

62. A processor-display system in accordance with claim 61 wherein responsive to the execution of said enabling instruction said processor thereafter allows the addressing by said display system of both said character code storage area and said dot pattern storage area during each processor cycle.

63. A processor-display system in accordance with claim 61 wherein said processor is responsive to the execution of a disabling instruction for thereafter inhibiting the addressing of said memory by said display system.

64. A processor-display system in accordance with claim 61 wherein said memory includes at least two character code storage areas and further including means responsive to the execution of a predetermined enabling instruction for thereafter controlling said display system to address only a specified one of said character code storage areas.

65. A processor-display system in accordance with claim 64 wherein said memory includes at least two dot

pattern storage areas, and each character code contained in said character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said display system.

66. A processor-display system in accordance with claim 65 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

67. A processor-display system in accordance with claim 60 wherein said memory includes at least two dot pattern storage areas, and each character code contained in said character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said display system.

68. A processor-display system in accordance with claim 67 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

69. A processor-display system in accordance with claim 68 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

70. A processor-display system in accordance with claim 60 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and said display system further includes means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

71. A processor-display system in accordance with claim 60 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

72. A processor-display system in accordance with claim 71 wherein said CRT is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

73. A processor display system in accordance with claim 60 wherein said electron beam is controlled by said sweep means to retrace at the end of each vertical line sweep and at the end of each horizontal line sweep, and further including means for blanking said CRT during horizontal and vertical retraces, and during the time that said electron beam is sweeping through a region of the face of said CRT which is not part of a character position.

74. A processor-display system in accordance with claim 73 wherein said sweep means is operative to control said electron beam to sweep across the face of said CRT in an interlaced fashion during successive subframes.

75. A processor-display system in accordance with claim 74 wherein said display controlling means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with sweeps of said electron beam, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

76. A processor-display system in accordance with claim 60 wherein said display controlling means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with sweeps of said electron beam, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

77. A display system comprising register means, an addressable read-write memory, means for transmitting data contained in said memory to said register means, said memory including at least one character code storage area for representing the particular characters to be displayed in respective positions of a display, and at least one dot pattern storage area containing data representative of the dot patterns required for the characters of a predetermined set, a CRT, a cycling counter, means for causing an electron beam to sweep through successive lines on the face of said CRT in a raster pattern in synchronism with the cycling of said counter, the count in said counter representing a character position on the face of said CRT, means for transmitting to said memory address information for character data in accordance with character position represented by said counter to control the transmission of a character code from said memory to said register means, display control means, and means for deriving and transmitting to said memory address information for data in said dot pattern storage area in accordance with a previously received character code to control the transmission of dot pattern data from said memory to said display control means, said display control means being operative to control the display of a dot pattern character corresponding to transmitted dot pattern data when said electron beam sweeps through said represented character position.

78. A display system in accordance with claim 77 wherein said memory includes at least two character code storage areas and further including means for selectively controlling the addressing of only a specified one of said character code storage areas.

79. A display system in accordance with claim 78 wherein said memory includes at least two dot pattern storage areas, and each character code contained in a character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said register means.

80. A display system in accordance with claim 79 wherein each character code contained in a character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

81. A display system in accordance with claim 77 wherein said memory includes at least two dot pattern storage areas, and each character code contained in said character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said register means.

82. A display system in accordance with claim 81 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

83. A display system in accordance with claim 82 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

84. A display system in accordance with claim 77 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

85. A display system in accordance with claim 77 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

86. A display system in accordance with claim 85 wherein said CRT is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

87. A display system in accordance with claim 77 wherein said electron beam is controlled by said sweep means to retrace at the end of each vertical line sweep and at the end of each horizontal line sweep, and further including means controlled by said counter for blanking said CRT during horizontal and vertical retraces, and during the time that said electron beam is sweeping through a region of the face of said CRT which is not part of a character position.

88. A display system in accordance with claim 87 wherein said sweep means is controlled by said counter such that said electron beam sweeps across the face of said CRT in an interlaced fashion during successive subframes.

89. A display system in accordance with claim 88 wherein said display control means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with said counter, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

90. A display system in accordance with claim 77 wherein said display control means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with said counter, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

91. A display system comprising register means, an addressable read-write memory, means for transmitting data contained in said memory to said register means, said memory including at least one character code storage area for representing the particular characters to be displayed in respective positions of a display, and at least one dot pattern storage area containing data representative of the dot patterns required for the characters of a predetermined set, a CRT, means for causing an electron beam to sweep through successive lines on the face of said CRT in a raster pattern, means for transmitting to said memory address information for character data to control the transmission of a character code from said memory to said register means, display control means, and mean for deriving and transmitting to said memory address information for dot pattern data in accordance with a previously received character code to control the transmission of dot pattern data from said memory to said display control means, said display control means being operative to control the display of a dot pattern character corresponding to transmitted dot pattern data when said electron beam sweeps through the character position of said display in which the character corresponding to said received character code should be displayed.

92. A display system in accordance with claim 91 wherein said memory includes at least two character code storage areas and further including means for selectively controlling the addressing of only a specified one of said character code storage areas.

93. A display system in accordance with claim 92 wherein said memory includes at least two dot pattern storage areas, and each character code contained in a character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said register means.

94. A display system in accordance with claim 93 wherein each character code contained in a character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

95. A display system in accordance with claim 91 wherein said memory includes at least two dot pattern storage areas, and each character code contained in said character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for the character code transmitted to said register means.

96. A display system in accordance with claim 95 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

97. A display system in accordance with claim 96 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

98. A display system in accordance with claim 91 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

99. A display system in accordance with claim 91 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said electron beam makes fast sweeps across the face of said CRT in the vertical direction and slow sweeps across the face of said CRT in the horizontal direction.

100. A display system in accordance with claim 99 wherein said CRT is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

101. A display system in accordance with claim 91 wherein said electron beam is controlled by said sweep means to retrace at the end of each vertical line sweep and at the end of each horizontal line sweep, and further including means for blanking said CRT during horizontal and vertical retraces, and during the time that said electron beam is sweeping through a region of the face of said CRT which is not part of a character position.

102. A display system in accordance with claim 101 wherein said sweep means is operative to control said electron beam to sweep across the face of said CRT in an interlaced fashion during successive subframes.

103. A display system in accordance with claim 102 wherein said display control means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with sweeps of said electron beam, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

104. A display system in accordance with claim 91 wherein said display control means includes shift register means for containing transmitted dot pattern data, means for shifting bits out of said shift register means in synchronism with sweeps of said electron beam, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said CRT.

105. A display system comprising read-write memory means, said memory means including at least one character code storage area for representing the particular characters to be displayed in respective positions of a display, and at least one dot pattern storage area containing data representative of the dot patterns required for the characters of a predetermined set, display means, means for enabling the display of successive lines on the face of said display means in a raster pattern, means for transmitting to said memory means address information for character data to retrieve a character code from said memory means, means for deriving and transmitting to said memory means address information for dot pattern data in accordance with a previously retrieved character code to control the retrieval of dot pattern data from said memory means, and means for turning on and off said enabling means to control the display of a dot pattern character corresponding to retrieved dot pattern data in a character position of said display in which the character corresponding to said retrieved character code should be displayed.

106. A display system in accordance with claim 105 wherein said memory means includes at least two character code storage areas and further including means for selectively controlling the addressing of only a specified one of said character code storage areas.

107. A display system in accordance with claim 106 wherein said memory means includes at least two dot pattern storage areas, and each character code contained in a character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for said character code.

108. A display system in accordance with claim 107 wherein each character code contained in a character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

109. A display system in accordance with claim 105 wherein said memory means includes at least two dot pattern storage areas, and each character code contained in said character code storage area includes the specification of the base address of that one of said dot pattern storage areas which contains the dot pattern data for said character code.

110. A display system in accordance with claim 109 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

111. A display system in accordance with claim 110 wherein for a fully displayed charaCter position there are more dots in the vertical direction than in the horizontal direction and said enabling means makes fast line sweeps across the face of said display means in the vertical direction and slow line sweeps across the face of said display means in the horizontal direction.

112. A display system in accordance with claim 105 wherein each character code contained in said character code storage area includes an auxiliary code for specifying whether a character should be displayed at the respective position in said display, and further including means for inhibiting the display of any dot pattern character whose dot pattern address information was derived in accordance with a character code whose auxiliary code specifies that a character should not be displayed at the corresponding position in said display.

113. A display system in accordance with claim 105 wherein for a fully displayed character position there are more dots in the vertical direction than in the horizontal direction and said enabling means makes fast line sweeps across the face of said display means in the vertical direction and slow line sweeps across the face of said display means in the horizontal direction.

114. A display system in accordance with claim 113 wherein said display means is a television receiver CRT modified to have triggered sweeps rather than synchronized sweeps.

115. A display system in accordance with claim 105 wherein said enabling means is controlled to retrace at the end of each vertical line sweep and at the end of each horizontal line sweep, and further including means for blanking said display means during horizontal and vertical retraces, and during the time that said enabling means is sweeping through a region of the face of said display means which is not part of a character position.

116. A display system in accordance with claim 115 wherein said enabling means is operative to control sweeps across the face of said display means in an interlaced fashion during successive subframes.

117. A display system in accordance with claim 116 wherein said turning on and off means includes shift register means for containing retrieved dot pattern data, means for shifting bits out of said shift register means in synchronism with sweeps of said enabling means, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said display means.

118. A display system in accordance with claim 105 wherein said turning on and off means includes shift register means for containing retrieved dot pattern data, means for shifting bits out of said shift register means in synchronism with sweeps of said enabling means, and means responsive to the shifting out of said shift register means of a bit of predetermined value for controlling the display of a dot on the face of said display means.

119. In a display system the improvement comprising read-write memory means, said memory means including at least one character code storage area for representing the particular characters to be displayed in respective positions of a display, and at least one dot pattern storage area containing data representative of the dot patterns required for the characters of a predetermined set.

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