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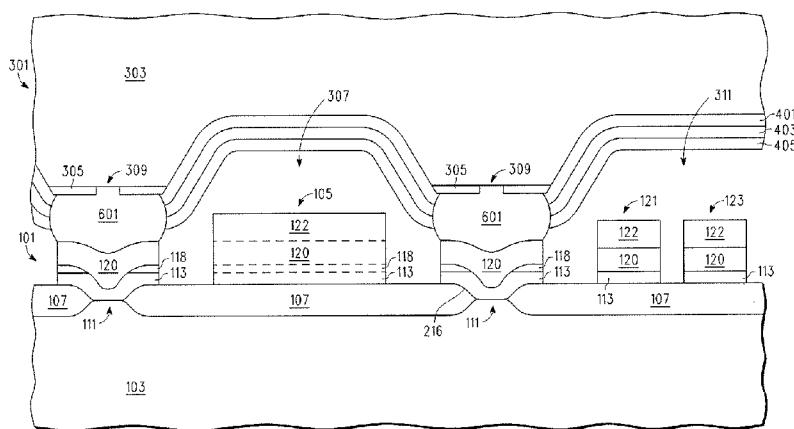


FIG. 6

(57) Abstract: A method that in one embodiment is useful in bonding a first substrate (103) to a second substrate (303) includes forming a layer including metal over the first substrate. The layer including metal in one embodiment surrounds a semiconductor device, which can be a micro electromechanical system (MEMS) device. On the second substrate (303) is formed a first layer comprising silicon (401). A second layer (403) comprising germanium and silicon is formed on the first layer. A third layer (405) comprising germanium is formed on the second layer. The third layer is brought into contact with the layer including metal. Heat (and pressure in some embodiments) is applied to the third layer and the layer including metal to form a mechanical bond material between the first substrate and the second substrate in which the mechanical bond material is electrically conductive. In the case of the mechanical bond surrounding a semiconductor device such as a MEMS, the mechanical bond can be particularly advantageous as a hermetic seal for protecting the MEMS.

## SUBSTRATE BONDING WITH METAL GERMANIUM SILICON MATERIAL

### BACKGROUND OF THE INVENTION

#### Field of the Invention

**[0001]** This invention relates in general to semiconductor devices and more specifically for techniques for bonding enclosures of a semiconductor device.

#### Description of the Related Art

**[0002]** With some types of semiconductor devices such as micro electrical mechanical system (MEMS) devices, it is desirable to seal the device (e.g. 5 hermetically) for the device to perform properly over time. For example, with some types of MEMS accelerometers, it is desirable to seal the MEMS accelerometer in a chamber to prevent contamination of the moving parts of a MEMS accelerometer during subsequent processes.

**[0003]** One method for sealing a MEMS device is to bond a cap wafer to a 10 second wafer that includes the MEMS device. The cap wafer and the second wafer form a cavity for the MEMS device. The cap wafer may include a lead glass frit located around the cavity that bonds to the second wafer under pressure and temperature.

**[0004]** What is needed is an improved technique for bonding two wafers together 20 to seal a semiconductor device such as a MEMS device.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0005]** The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

**[0006]** Figure 1 is a partial cutaway side view of a device wafer at one stage of 25 manufacture according to one embodiment of the present invention.

**[0007]** Figure 2 is a partial top view of a device wafer at one stage of manufacture according to one embodiment of the present invention.

**[0008]** Figure 3 is a partial cutaway side view of a cap wafer at a stage of manufacture according to one embodiment of the present invention.

5 **[0009]** Figure 4 is a partial cutaway side view of a cap wafer at another stage of manufacture according to one embodiment of the present invention.

**[0010]** Figure 5 is a partial cutaway side view of a cap wafer placed against the device wafer at a stage of manufacture according to one embodiment of the present invention.

10 **[0011]** Figure 6 is a partial cutaway side view of a cap wafer pressed against the device wafer at another stage of manufacture according to one embodiment of the present invention.

**[0012]** The use of the same reference symbols in different drawings indicates identical items unless otherwise noted. The Figures are not necessarily  
15 drawn to scale.

### **DETAILED DESCRIPTION**

**[0013]** The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

20 **[0014]** A cap wafer is bonded to a device wafer by a metal poly silicon germanium material to form a sealed chamber around a semiconductor device. On one wafer, a stack of silicon (Si), poly silicon germanium (SiGe), and poly germanium (Ge) is formed. A metal structure is formed on a second wafer. The metal silicon germanium material is formed by placing the metal structure and germanium structure in contact and applying heat (and pressure in some embodiments).

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**[0015]** Figure 1 is a side view of a device wafer 101 that includes a semiconductor device 105 to be sealed with a cap wafer (e.g. 301 of Figure 3). In one embodiment, device 105 is a MEMS device such as e.g. an accelerometer or switch. In one example of a MEMS device, device 5 105 includes a proof mass (not shown) made of polysilicon that is supported by springs and is movable with respect to substrate 103. In such an embodiment, device 105 includes capacitive structures whose capacitance can be measured to detect the movement of the proof mass. However, device 105 may be of other types of semiconductor devices in 10 other embodiments. For example, in one embodiment, device 105 may be a transducer.

**[0016]** Wafer 101 includes a substrate 103 which in one embodiment is made of bulk monocrystalline silicon. An insulator layer 107 (e.g.  $\text{SiO}_2$ ) is formed on substrate 103. In the embodiment shown, layer 107 is formed by a 15 local oxidation of silicon (LOCOS) process, but may be formed by other methods in other embodiments. In one embodiment, the back side (not shown) of wafer 101 may be ground and polished. Layer 107 is formed with opening 111 located around the location of the subsequently formed semiconductor device 105. In other embodiments, opening 111 maybe 20 formed by patterning layer 107. In one embodiment, layer 107 has a thickness of 25K Angstroms, but may be of other thicknesses in other embodiments.

**[0017]** After the formation of layer 107, polysilicon layers 113 and 120 (polycrystalline layers of silicon) and metal layer 122 are formed over 25 layer 107. In one embodiment, layers 113, 120, and 122 are formed separately and then patterned prior to forming the next layer to form the desired structures of those layers. In some embodiments, dielectric layers e.g. layer 118 may be formed subsequently or prior to the forming of polysilicon layers 113 and 120 for the isolation of various structures 30 formed from those layers. Also, sacrificial layers (not shown) may be used for forming the desired structures that are later removed in

subsequent processes. In one embodiment, layer 118 may be of a silicon rich nitride material

5 [0018] In the embodiment shown, device 105 includes layers 113, 118, 120, 122. In such a device, those layers maybe patterned to remove a portion of the layer at various locations in the device. However, for simplicity, device 105 is shown with those layers located in dashed lines all the way across device 105. In other embodiments, wafer 101, including device 105, may include other semiconductor layers and metal layers.

10 [0019] Wafer 101 includes a seal ring 117 surrounding device 105. Ring 117 is located over opening 111 wherein the polysilicon material of layer 113 is in contact with the silicon material of substrate 103 at opening 111.

15 [0020] Electrical contacts are also formed on wafer 101 with contacts 121 and 123 shown in Figure 1. In the embodiment shown, contacts 121 and 123 include poly silicon layer 113, poly silicon layer 120, and metal layer 122 but do not include dielectric layer 118. Each contact is electrically coupled to a structure of device 105 by a polysilicon runner (e.g. 211 of Figure 2) formed from layer 113.

20 [0021] In one embodiment, polysilicon layer 113 is 3500 Angstroms thick, but may be of other thicknesses in other embodiments. In one embodiment, layer 113 is doped with an impurity e.g. phosphorus to increase conductivity by ion implantation but may be doped with other impurities and by other methods in other embodiments.

25 [0022] In one embodiment, polysilicon layer 120 is 32K Angstroms thick but may be of other thicknesses in other embodiments. In one embodiment, layer 120 is doped with e.g. phosphorus by a doped oxide diffusion process, but may be doped with other impurities to improve conductivity and by other methods in other embodiments.

[0023] Metal layer 122 is formed over a patterned layer 120. In one embodiment, layer 122 is formed of aluminum. In one embodiment, layer 122 is formed of 99.5% aluminum (by atomic weight) and .5% copper (by atomic weight). However, layer 122 may be made of other metals or include other metals in other embodiments such gold, platinum, tungsten, titanium, cobalt, nickel, tin, and tantalum. In some embodiments, layer 122 may include some non metal materials such as germanium or silicon. In one embodiment, layer 122 includes 98% atomic weight or greater of a primary metal material (e.g. aluminum in some embodiments). In one embodiment, layer 122 has a thickness in the range of 3-4 microns, but maybe of other thicknesses in other embodiments.

[0024] In one embodiment, device 105 includes a portion of metal layer 122. In one embodiment, a portion of layer 122 is utilized to add weight to a proof mass of device 105.

[0025] In some embodiments, layer 122 is formed by physical vapor deposition, sputtering, evaporation, or plating. Layer 122 is subsequently patterned to form desired structures including on seal ring 117 and contacts 121 and 123.

[0026] Figure 2 shows a top view of wafer 101. Ring 117 is shown as having a rectangle shape located around device 105. Wafer 101 includes a number of contacts 201, 203, 121, 123, 205, and 207 that are electrically coupled by polysilicon runners 211, 213, 215, 221, 219 and 217 respectively, to structures of device 105. The runners are made of poly silicon from layer 113.

[0027] In the embodiment shown, runners 213, 215, 221, and 219 pass through ring 117. At these locations, layer 113 of ring 117 is electrically isolated from the runners by nitride layer 118 and by other dielectric material at locations lateral to the runners. In the embodiment shown, ring 117 includes two parts of layer 113. Part 212 appears a "C" structure starting

at sidewall 218 and extending for three whole sides around device 105 to sidewall 220. The second part 216 is located between a first set of runners 211, 213, and 215, and a second set of runners 221, 219, and 217. Part 216 is separated from sidewall 218 to form an opening from runners 213 and 215 and part 216 is separated from sidewall 220 from an opening for runners 221 and 219.

5 [0028] Runners 211 and 217 are contiguous with the portion of layer 113 of ring 117. Thus, there are no dashed lines shown for these runners as crossing through ring 117 from the portion of the runners on the outside to the portion of the runners on the inside of the ring. Accordingly, ring 117 is 10 electrically coupled to contacts 205 and 201. In one embodiment, contacts 205 and 201 serve as ground pads and are electrically coupled to substrate 103 by the runners and through conductive material in opening 111.

15 [0029] Opening 111 is located under those portions of layer 113 of ring 117 and runners 211 and 217 to provide ohmic contact to substrate 103. Opening 111 is not located under runners 213, 215, 221, and 219 in order to isolate those structures from substrate 103.

20 [0030] In other embodiments, the openings to the substrate 103 maybe at different locations, maybe of different sizes, and/or maybe of different shapes. For example, in one embodiment, openings 111 are located under ring 117 only at the locations where runners 211 and 217 extend through ring 117. In other embodiments, the substrate openings may be located under runners 211 and 217 at locations outside of ring 117. In 25 one embodiment, substrate openings may be located under contacts 201 and 205.

[0031] After the formation of nitride dielectric layer 118, a dielectric layer e.g. silicon dioxide (not shown) is deposited over wafer 101. An opening is then formed in nitride layer 118 at those portions of ring 117. Layer 120 is

subsequently formed over wafer 101. The portion of layer 120 of ring 117 is in contact with the portion of layer 113 of ring 117 via the openings of nitride layer 118.

5 [0032] Figure 3 is a partial side cutaway view of cap wafer 301. In the embodiment shown, cap wafer 301 includes a bulk silicon substrate 303 and a layer of oxide 305 formed there over. In one embodiment, layer 305 is thermally grown, but in other embodiments, it may be deposited. Layer 305 is 4950 Angstroms thick, but may be of other thicknesses in other embodiments.

10 10 [0033] After the formation of layer 305, openings are formed in layer 305 at the locations of trenches 311 and 307. Wafer 301 is then subjected to an etch process (either wet or dry) to form trenches 311 and 307 in substrate 303. Afterwards, opening 309 is formed in layer 305 to expose substrate 303.

15 15 [0034] Referring to Figure 4, a polysilicon layer 401 is formed over wafer 301. In one embodiment, layer 401 has a thickness in the range of 750-2500 Angstroms, but may have other thicknesses in other embodiments. In one embodiment, layer 401 is formed by a chemical vapor deposition process (CVD), but may be formed of other processes in other embodiments. In one embodiment, layer 401 is formed by a process at a temperature greater than 550 degrees Celsius.

20 20 [0035] In some embodiments, Layer 401 acts as a seed layer for subsequently formed layer 403. Layer 403 is made of silicon germanium. In one embodiment, layer 403 includes germanium in a range of 20-40 atomic percent with the remainder being of silicon. However, other embodiments may have a different atomic percentage of germanium. In one embodiment, the germanium concentration of layer 403 may vary with a lower concentration of germanium at the bottom of layer 403 and a higher concentration of germanium at the top of layer 403, relative to the view shown in Figure 4. In one embodiment, layer 403 is formed by a CVD

process, but may be formed by other processes in other embodiments. In one embodiment, silicon germanium layer 403 has a thickness in the range of 500-2000 Angstroms, but may be of other thickness in other embodiments.

5 [0036] Layer 405 is formed over layer 403. Layer 405 is made of poly crystalline germanium. In one embodiment, layer 405 has a thickness in the range of 2000-4000 Angstroms, but may be of other thicknesses in other embodiments. In one embodiment, layer 405 is formed by a CVD process, but may be formed by other processes in other embodiments.

10 [0037] In some embodiments, the back side of wafer 301 may be ground and polished. Also in some embodiments, trenches (not shown) may be formed in the backside of wafer 301.

[0038] In one embodiment, polycrystalline layers 401, 403, and 405 are not doped with conductivity impurities (e.g. boron, phosphorous, arsenic). In 15 other embodiments, they may be doped with conductivity or other types of impurities.

[0039] Figure 5 is a partial cutaway side view showing wafer 301 being brought into contact with wafer 101 where ring 117 is aligned to opening 309, trench 311 is located over contacts 121 and 123, and trench 307 is located over device 105. Figure 5 shows both wafers just prior to the application 20 of heat (and pressure in some embodiments) for bonding the two wafers together.

[0040] Figure 6 is a partial cutaway side view after wafer 101 and 301 have been bonded together by applying heat to the wafers. During the bonding 25 process, the metal material of layer 122 of ring 117 reacts with the polysilicon of layer 401, the polycrystalline silicon germanium of layer 403, and the polycrystalline germanium of layer 405 to form a bonding material 601 of aluminum, silicon, and germanium. In one embodiment, this material 601 is a ternary system of aluminum (or other metal in other

embodiments), silicon, and germanium. In one embodiment, aluminum (or other material of layer 122 in other embodiments) is the largest component by volume, followed by germanium, and then silicon. Material 601 is conductive. In one embodiment, material 601 may be described as a Al-Ge-Si eutectic compound. In one embodiment, material 601 may be described as a compound film. In one embodiment, the percentage by atomic weight of silicon of the material 601 is greater than 5%.

5 [0041] In embodiments where ring 117 completely surrounds device 105, material 601 provides for a hermetic seal for device 105 between wafers 101 and 10 301. In addition, because material 601 is conductive, in some embodiments, it provides for a conductive path (e.g. a ground path) between the two wafers.

10 [0042] The wafers are bonded at a temperature in the range of 425-500 C, and more preferably at a temperature in the range 450-475 C. However other 15 temperatures may be used in other embodiments. The use of aluminum for layer 122 is preferable in that it may allow for the use of bonding temperatures below 500 degrees Celsius. In some embodiments, during the bonding process, the gap between substrate 303 and substrate 103 is reduced from its position shown in Figure 5.

20 [0043] In some embodiments, the wafers are bonded together under pressure in addition to the application of heat. In one embodiment, a tool force pressure in the range of 5000-10,000 milibars is applied, with a preferable pressure in some embodiments of 6500 milibars. However in other embodiments, other applied bonding force pressures may be used.

25 [0044] In some embodiments, forming layer 405 of poly crystalline germanium by a CVD process (including plasma enhanced CVD processes) provides for a method of forming such a layer by a process that generates less particulates, which results in lower defect densities.

**[0045]** Furthermore, utilizing a CVD deposited, poly crystalline germanium layer provides the layer with a roughness that allows for better bonding with the material of layer 122 in some embodiments.

5       **[0046]** Forming a polycrystalline layer of germanium (e.g. layer 405) on a polycrystalline layer of silicon germanium (e.g. layer 403) may in some embodiments avoid the formation of voids in material 601 at the location where seed layer 401 is located. It is believed that using the intermediate silicon germanium layer 403 inhibits silicon migration from seed polysilicon layer 401 to layer 405 during the bonding process. Accordingly, utilizing the intermediate silicon germanium layer 403 results in material 601 being of a stronger and more uniform material.

10      **[0047]** The resultant wafer (wafer 101 and wafer 301 bonded together in Figure 6) is further processed subsequent to the stage shown in Figure 6. For example, the portion of substrate 303 may be removed to expose contacts 121 and 123 for external connection of those bond pads. Afterwards the resultant wafer is singulated into multiple die where each of the die includes a device similar to device 105 that is sealed with a material similar to material 601. Such die may be packaged for incorporation in electronic systems.

15      **[0048]** In some embodiments, cap wafer 301 may include semiconductor devices of an integrated circuit formed there on. For example, an integrated circuit (e.g. a microprocessor) may be formed in trench 307. The integrated circuit may be electrically coupled to device 105.

20      **[0049]** In the embodiment shown, the metal layer 122 of the ring 117 is formed on device wafer 101 and the polycrystalline layers 401, 403, and 405 are formed on wafer 301. In other embodiments, layers 401, 403, and 405 may be formed on the device wafer and be bonded to a metal ring formed on cap wafer 301.

**[0050]** In one embodiment, a method includes forming a layer including metal over a first substrate, providing a second substrate, and forming a first layer comprising silicon supported by the second substrate. The method also includes forming a second layer comprising germanium and silicon on the first layer, forming a third layer comprising germanium on the second layer, and contacting the third layer to the layer including metal. The method further includes after contacting the third layer to the layer including metal, forming a mechanical bonding material between the first substrate and the second substrate. The forming a mechanical bonding material includes applying heat to the third layer and the layer including metal. The bonding material includes a metal of the layer including metal and material of the third layer.

**[0051]** In another embodiment, a method for providing a seal between a first substrate and a second substrate includes contacting the first substrate to the second substrate through a bonding stack. The bonding stack includes a first layer comprising silicon, a second layer comprising germanium and silicon in contact with the first layer, a third layer comprising germanium in contact with the second layer, and a layer including metal in contact with the third layer. The method includes applying heat and pressure to the bonding stack so that the bonding stack becomes a bond between the first and second substrates.

**[0052]** In another embodiment, a semiconductor structure includes a first substrate, a semiconductor device on the first substrate, a second substrate, and a conductive bond between the first substrate and the second substrate that surrounds the semiconductor device to seal the semiconductor device between the first substrate and the second substrate. The conductive bond comprises metal, silicon, and germanium. An atomic percent of silicon in the conductive bond is greater than 5%.

**[0053]** While particular embodiments of the present invention have been shown and described, it will be recognized to those skilled in the art that, based

upon the teachings herein, further changes and modifications may be made without departing from this invention and its broader aspects, and thus, the appended claims are to encompass within their scope all such changes and modifications as are within the true spirit and scope of this invention.

## **CLAIMS**

What is claimed is:

1. A method, comprising:  
forming a layer including metal over a first substrate;  
providing a second substrate;  
forming a first layer comprising silicon supported by the second substrate,  
forming a second layer comprising germanium and silicon on the first layer;  
forming a third layer comprising germanium on the second layer;  
contacting the third layer to the layer including metal; and  
after contacting the third layer to the layer including metal, forming a mechanical  
bonding material between the first substrate and the second substrate, wherein  
the forming a mechanical bonding material includes applying heat to the third  
layer and the layer including metal, wherein the bonding material includes a  
metal of the layer including metal and material of the third layer.
2. The method of claim 1, wherein the metal of the layer including metal is aluminum.
3. The method of claim 2, wherein the mechanical bonding material includes a material  
that is a ternary system including aluminum, silicon, and germanium.
4. The method of claim 1 wherein the forming the mechanical bonding material includes  
applying a bonding force pressure to the first substrate and the second substrate.
5. The method of claim 4 wherein the bonding force pressure is greater than 5000  
millibars.
6. The method of claim 1 wherein the applying heat includes applying heat at a  
temperature of 500 C or less.
7. The method of claim 1, wherein the steps of forming the first layer, the second layer,  
and the third layer are further characterized by the first layer, the second layer, and the third  
layer being polycrystalline.
8. The method of claim 1, further comprising forming a layer of polysilicon over the first  
substrate prior to forming the layer including metal, wherein the step of forming the layer

including metal is further characterized as the layer including metal being formed on the layer of polysilicon.

9. The method of claim 1, wherein:

the step of forming the first layer is further characterized as forming the first layer to a thickness less than that of the third layer;

the step of forming the second layer is further characterized as forming the second layer to a thickness less than that of the third layer.

10. The method of claim 1, further comprising:

forming a semiconductor device over the first substrate which is surrounded by a ring including the layer including metal; and

forming a cavity in the second substrate, wherein the step of contacting is further characterized as aligning the cavity with the semiconductor device.

11. The method of claim 10, wherein the step of forming the semiconductor device is further characterized by the semiconductor device being a micro electromechanical system (MEMS) device.

12. The method of claim 1, wherein a percentage of aluminum of the layer including metal is 98% or greater by atomic weight.

13. The method of claim 1, further comprising forming a layer of polysilicon over the first substrate prior to forming the layer including metal, wherein the step of forming the layer including metal is further characterized as the layer including metal being formed on the layer of polysilicon.

14. A method for providing a seal between a first substrate and a second substrate, comprising:

contacting the first substrate to the second substrate through a bonding stack,

wherein the bonding stack comprises:

a first layer comprising silicon;

a second layer comprising germanium and silicon in contact with the first layer;

a third layer comprising germanium in contact with the second layer; and a layer including metal in contact with the third layer;

applying heat and pressure to the bonding stack so that the bonding stack becomes a bond between the first and second substrates.

15. The method of claim 14, further comprising forming a semiconductor device on the first substrate in which the bonding stack surrounds the semiconductor device, wherein the step of contacting is further characterized by the layer including metal being formed over the first substrate and the first layer being formed over the second substrate.

16. The method of claim 14, wherein the step of contacting is further characterized by the first, second, and third layers being polycrystalline.

17. The method of claim 14 wherein the step of contacting is further characterized by the layer including metal comprising aluminum.

18. The method of claim 14, wherein the step of contacting is further characterized by the first and second layers being less thick than the third layer.

19. The method of claim 14 wherein the applying heat includes applying heat at a temperature of 500 C or less.

20. A semiconductor structure, comprising:  
a first substrate;  
a semiconductor device on the first substrate,  
a second substrate;  
a conductive bond between the first substrate and the second substrate that surrounds the semiconductor device to seal the semiconductor device between the first substrate and the second substrate, wherein:  
the conductive bond comprises metal, silicon, and germanium; and  
a percentage by atomic weight of silicon in the conductive bond is greater than 5%.

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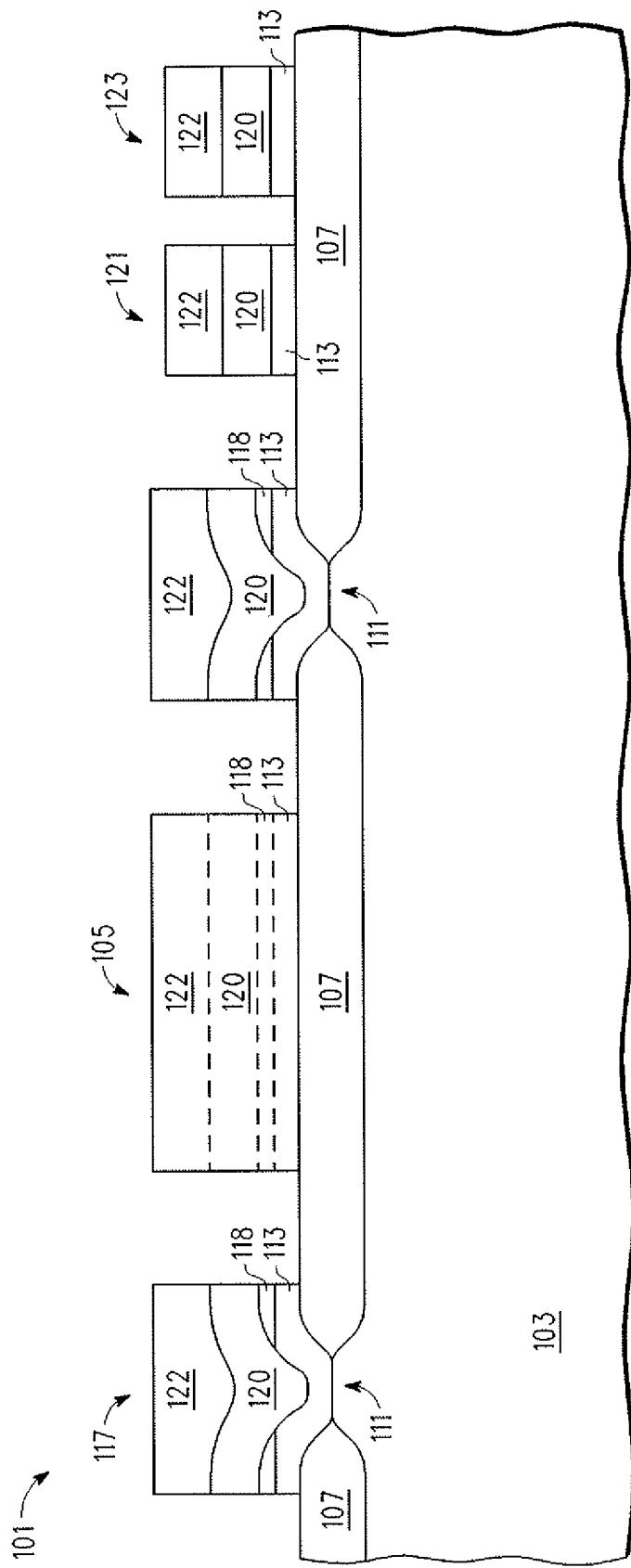
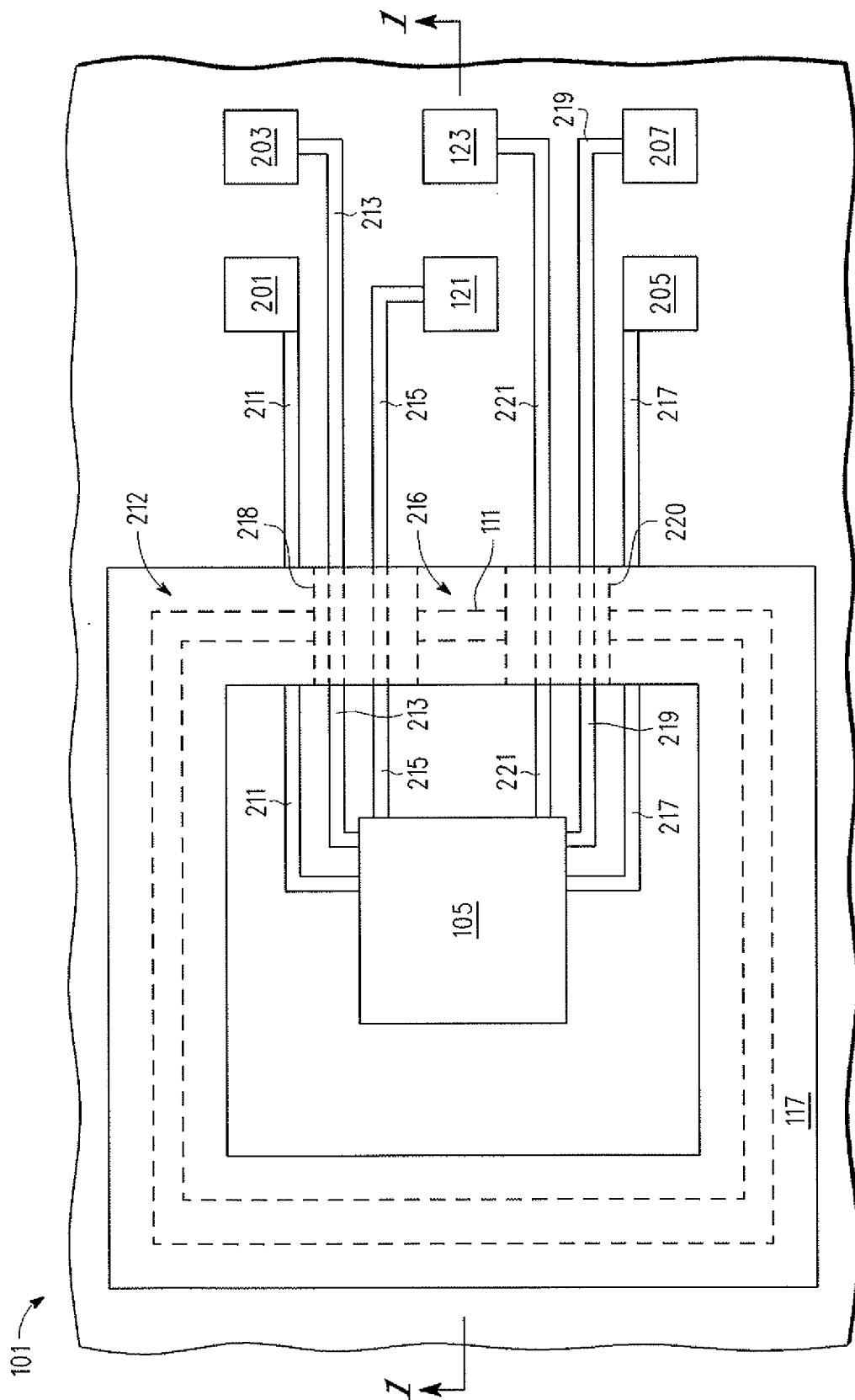


FIG. 1

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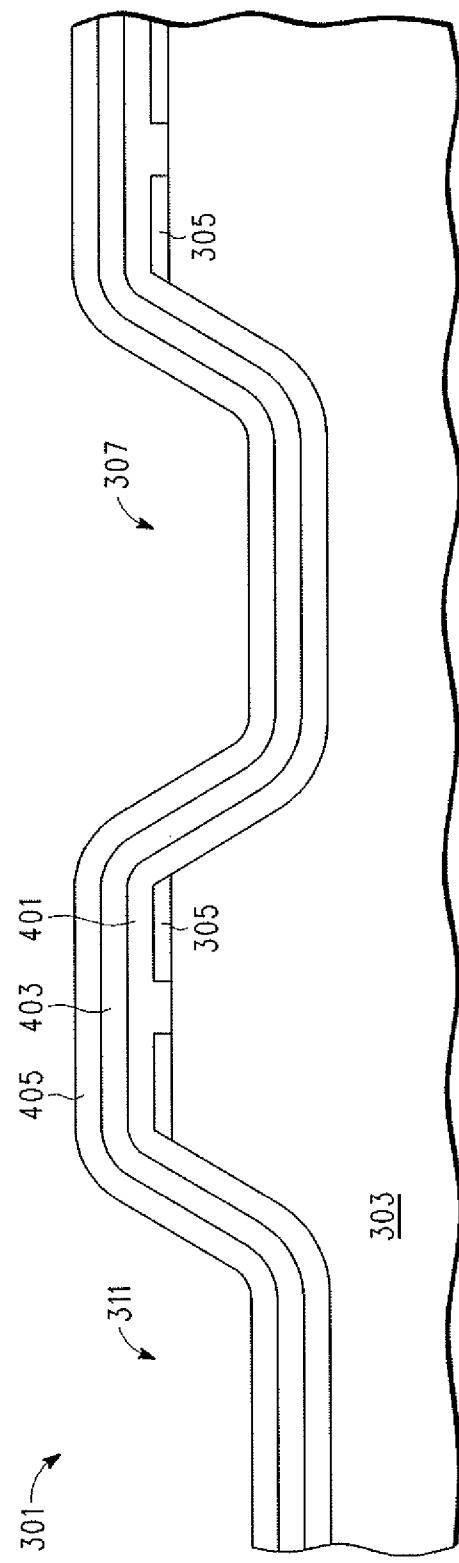
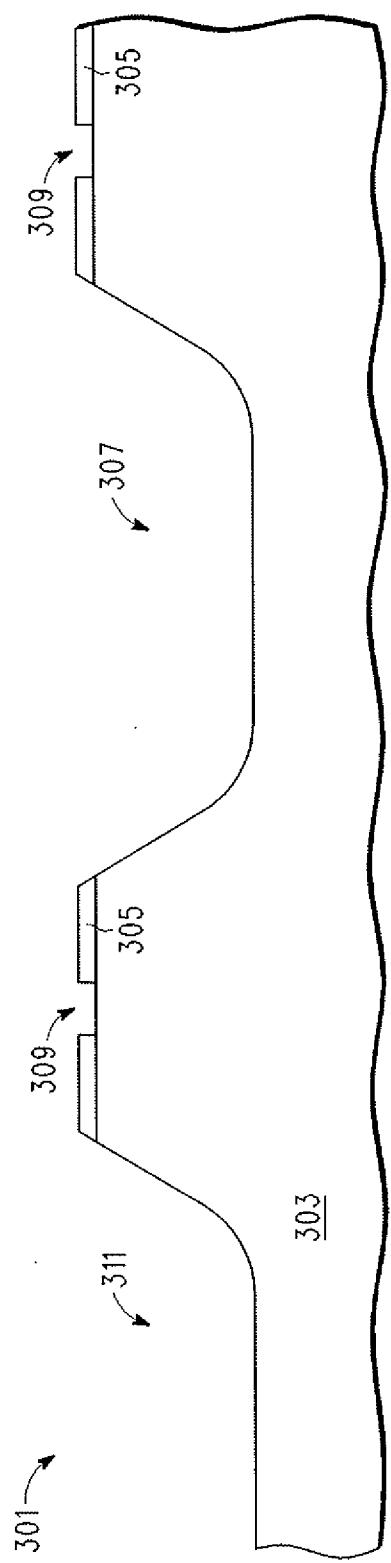


FIG. 4

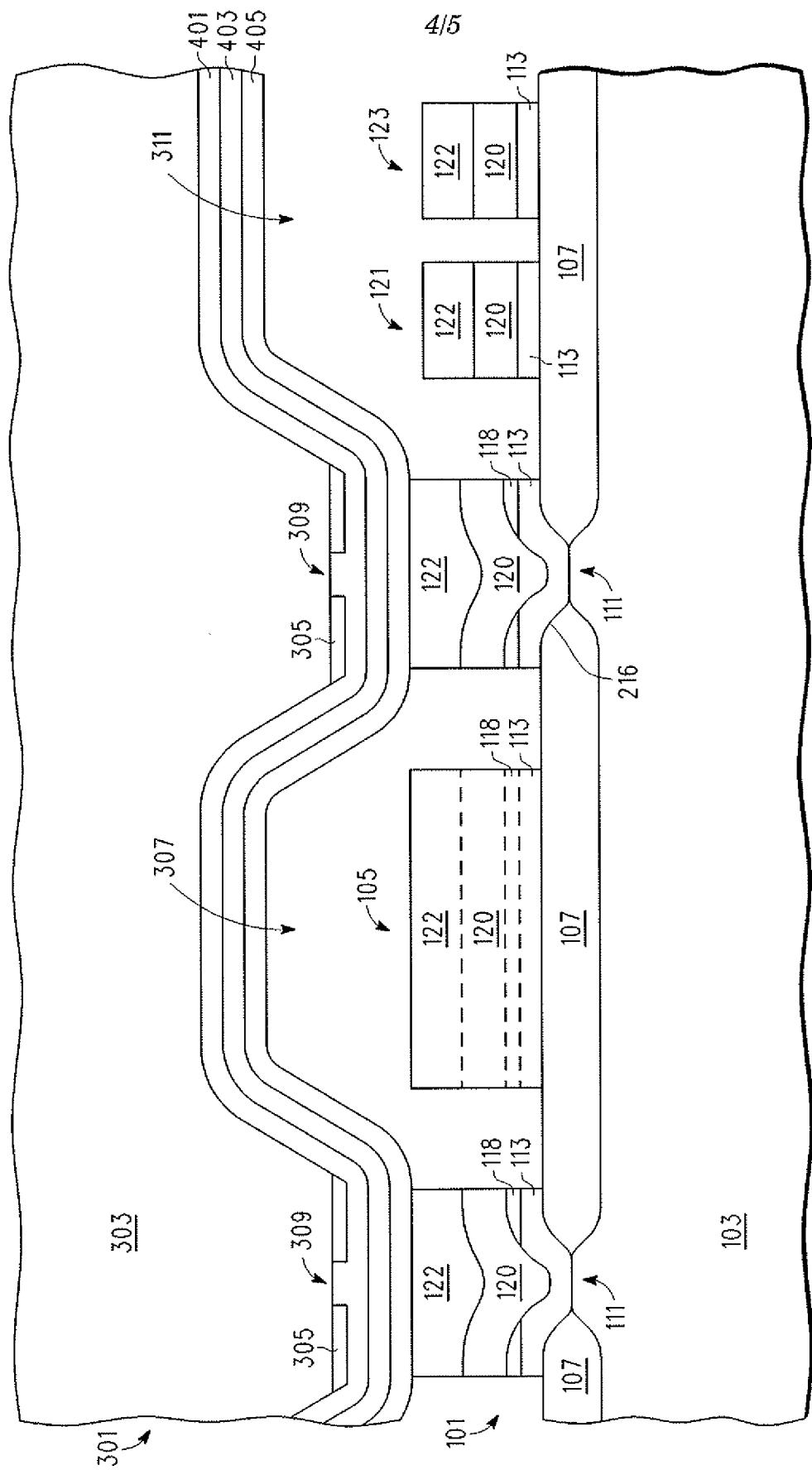


FIG. 5

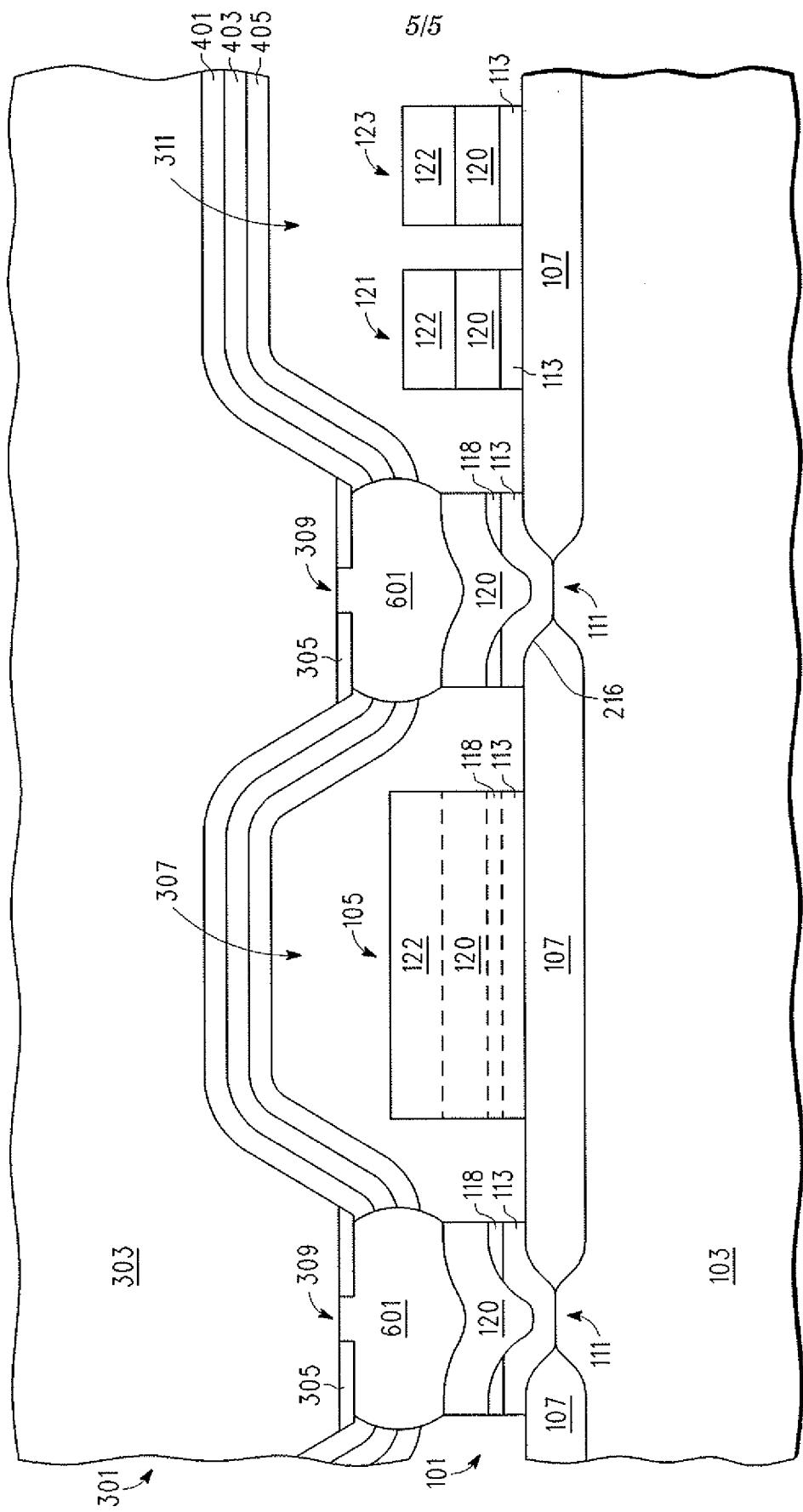


FIG. 6