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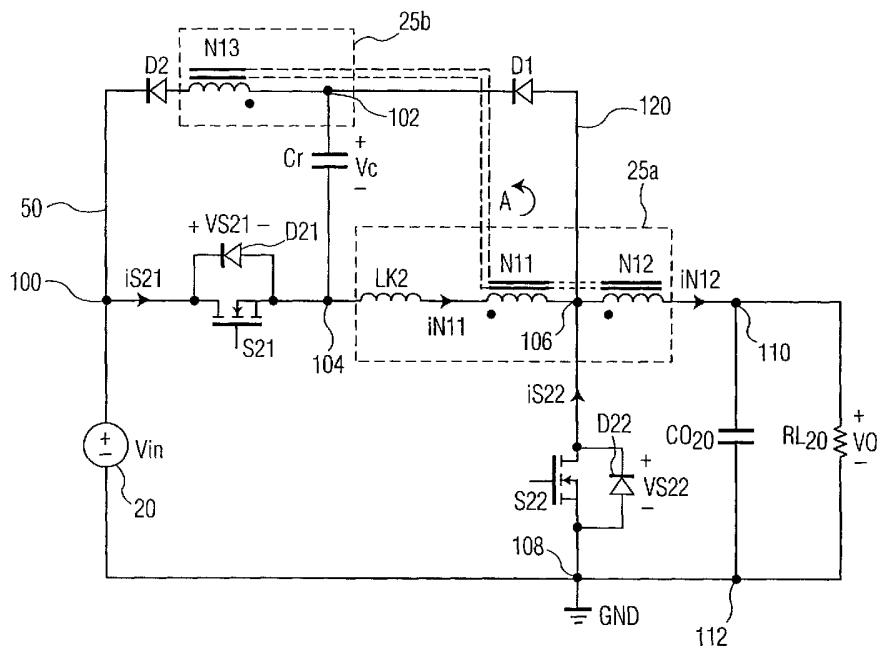
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(54) Title: TAPPED-INDUCTOR STEP-DOWN CONVERTER



(57) Abstract: A tapped-inductor step-down converter and method for clamping same with a clamping capacitor (Cr) so that MOS-FETs can be employed to improve circuit efficiency. The converter includes a tapped-inductor (25a, 25b) and clamping capacitor (Cr) uniquely arranged to eliminate resonance between the leakage energy of the leaky inductance (Lk2) and the clamping capacitor (Cr). Moreover, such arrangement provides for the recycling or recovering of the leakage energy from a leaky inductance of the tapped-inductor to further improve circuit efficiency.



WO 03/012964 A2

TAPPED-INDUCTOR STEP-DOWN CONVERTER

5 The ever-present demands for faster and more efficient data processing have prompted a significant development effort in the area of low voltage integrated chips (ICs). Currently, 3.3V ICs are gradually replacing the standard 5V ICs due to their better speed, power consumption performance and higher integration densities. However, the 3.3V IC is only a traditional stage to ICs with ever lower voltages that will not only improve the speed and reduce the power consumption of ICs but also will allow direct, single-cell battery
10 operation. It is expected that next generations of the data processing ICs will require power supply with voltages in the 1-3 V range. At the same time, since more devices are integrated on a single processor chip and the processors operate at higher frequencies, microprocessors need aggressive power management. Future generation processors' current draw will increase
15 from 13A to 50A-100A and the load range may reach 1:100. On the other hand, as the speed of the ICs increases, they are becoming more dynamic loads to their power supplies. The next generation microprocessors are expected to exhibit current slew rates of 50A/ms. Moreover, the output voltage regulation becomes much tighter from 5% to 2%. All requirements pose very serious design challenges. Voltage regulator modules (VRMs), which feed the
20 microprocessors, have to have high efficiency, fast transient response and high power density.

 A conventional synchronized buck converter, such as shown in Fig. 1, is typically used as a VRM to meet these requirements. The conventional synchronized buck converter includes two switches S1 and S2 which are turned on and off in a complementary
25 manner, output capacitor C_{O1} and load R_{L1} . The voltage gain for the conventional synchronized buck converter of Fig. 1 is given by

$$D = \frac{V_o}{V_{in}} \quad \text{Eq. (1)}$$

where D is the duty ratio or cycle of switch S1. It has been well established that the conventional buck converter has better efficiency for a duty cycle D of 0.5. For an input
 5 voltage V_{in} of 5V and an output voltage V_o of 2V, the duty cycle D is 0.4, which is good to achieve high efficiency.

Since the future VRM should provide more power to the microprocessor, the power switch has to deal with high current, which decreases efficiency. The higher the input voltage V_{in} , the lower the input current so as to reduce the conduction loss. If the input
 10 voltage V_{in} to the VRMs increases from 5V to 12V, then the current rating for the buck switch is significantly reduced, which increases efficiency. Therefore, the VRMs would need a 12V or higher input voltage V_{in} . According to Severns et al., "Modern DC-To-DC Switch Mode Power Converter Circuits," TK7868, 1984, pg. 178, the duty cycle D for the conventional synchronized buck converter is as small as .15V with 12V input. This will result
 15 in poor performances in terms of voltage regulation and transient response.

Figs. 2 and 3 illustrate a conventional tapped-inductor synchronized buck converter and the switching waveforms thereof, respectively. In operation, when switch S11 is turned on and switch S12 is turned off during time the interval T1 to T2, the voltage V_{in} - V_o is applied to the windings N1 and N2 of the tapped-inductor. The input voltage V_{in} is
 20 from a DC voltage source 2 and the output voltage V_o is across a load R_{L10} . The conventional tapped-inductor synchronized buck converter delivers power to the output. At time T2, switch S11 turns off and switch S12 turns on. The energy stored in winding N1 is transferred to winding N2 and the winding current I_{N2} flows through switch S12. The voltage gain of the conventional tapped-inductor synchronized buck converter is given by

$$\frac{V_o}{V_{in}} = \frac{D}{1 + \frac{N1}{N2} * (1 - D)} \quad \text{Eq. (2)}$$

From Eq. (2), it can be readily seen that approximately a 0.5 duty cycle (D) can be obtained to achieve high efficiency by properly choosing the turns ratio of the
 30 windings N1 and N2 of the tapped-inductor. However, the main problem is that there exists a

high voltage spike across switch S11 when switch S11 turns off because the leakage energy of leakage inductance L_k of winding N1 can not be transferred to winding N2. Instead, the leakage energy of leakage inductance L_k charges the output capacitor C_{s1} of the switch S1 (not shown) through conducting switch S12, which causes a high voltage stress across switch S11. As a result, the high voltage rating metal-oxide semiconductor field-effect transistor (MOSFET) has to be used. The MOSFET has a high on-resistance with a high voltage rating, which significantly increases the power loss and reduces the efficiency.

Fig. 3 illustrates the switching waveforms of the switches S11 and S12, currents I_{S11} and I_{S12} and the voltage stress V_{S11} and V_{S12} across switches S11 and S12, respectively.

As can be readily seen, there is a continuing need to improve the VRM performance to meet these requirements.

Broadly, the present invention contemplates a tapped-inductor step-down converter and method for clamping same so that low voltage rating MOSFETs can be used to improve the efficiency of the converter. The invention is defined by the independent claims. The dependent claims define advantageous embodiments. The converter preferably includes a tapped-inductor and a clamping capacitor which are uniquely arranged to recycle the leakage energy from a leaky inductance of the tapped-inductor and to eliminate resonance between the leakage energy of the leaky inductance and the clamping capacitor.

Fig. 1 illustrates a schematic diagram of a conventional synchronized buck converter.

Fig. 2 illustrates a schematic diagram of a conventional tapped-inductor synchronized buck converter.

Fig. 3 illustrates the switching waveforms of the conventional tapped-inductor synchronized buck converter of Fig. 2.

Fig. 4 illustrates a schematic diagram of a tapped-inductor step-down converter of the present invention.

Fig. 5 illustrates the switching waveforms of the tapped-inductor step-down converter of the embodiment of Fig. 4.

Fig. 4 illustrates an exemplary embodiment of the schematic diagram of a tapped-inductor step-down converter 10 according to the present invention which includes a clamping capacitor C_r so that low voltage rating MOSFETs can be used for the two complementarily switched switches S_{21} and S_{22} to improve the efficiency of converter 10. The converter 10 further includes a unique arrangement between a tapped-inductor 25a and 25b, having three windings N_{11} , N_{12} , and N_{13} , and the clamping capacitor C_r to recycle the leakage energy from a leaky inductance L_{k2} of the tapped-inductor 25a and 25b and to eliminate resonance between the leakage energy of the leaky inductance L_{k2} and the clamping capacitor C_r , which further improved efficiency. Additionally, such arrangement creates varying clamping voltages V_c .

The schematic diagram of the tapped-inductor step-down converter 10 converts a DC input voltage V_{in} to a DC output voltage V_o . Converter 10 will now be described in detail. The positive side of the DC voltage source 20 delivering input voltage V_{in} is coupled to the input voltage node 100. From the input voltage node 100 there are two general input paths, the first path $I_{S_{21}}$ and the second path 50. The cathode of diode D_2 of the second path 50 and the drain of the MOSFET switch S_{21} of the first path $I_{S_{21}}$ are coupled to the input voltage node 100. MOSFET switch S_{21} has a body diode D_{21} integrated therewith wherein the anode is coupled to the source and the cathode is coupled to the drain of the MOSFET switch S_{21} . The drain of the MOSFET switch S_{21} is coupled to node 104. The anode of diode D_2 is in series with the undotted terminal of winding N_{13} of the converter's storage inductor 25a and 25b, which will be described in detail below.

Referring now to the converter's storage inductor 25a and 25b, the storage inductor 25a and 25b is generally comprised of windings N_{11} , N_{12} and N_{13} wrapped by a single wire around a single magnetic core, as illustrated by the dashed lines, separated by taps 102 and 106. The number of turns in winding N_{11} and the number of turns in winding N_{12} separated by tap 106 are not necessarily the same. Moreover, the number of turns in winding N_{13} separated by tap 102 may also be different from the number of turns in either of windings N_{11} and N_{12} . By convention, the current flowing through windings N_{11} , N_{12} and N_{13} flows into the dotted terminal and out of the undotted terminal. The dotted terminal of winding N_{13} , the first terminal of the clamping capacitor C_r and the cathode of diode D_1 are coupled to tap 102. The second terminal of the clamping capacitor C_r is coupled to node 104. The second terminal of the clamping capacitor C_r and the dotted terminal of winding N_{11} via the first side of leakage inductance L_{k2} are coupled to node 104. The second side of the

leakage inductance L_{k2} is coupled to the first terminal of the winding N11. The undotted terminal of the winding N11, the dotted terminal of N12, and the anode of diode D1 are coupled to tap 106. As can be readily seen, a path 102 couples taps 102 and 106 of the storage inductor 25a and 25b together via diode D1. The operation of the storage inductor 25a and 25b will be made apparent based on the description provided with regard to the overall operation of the converter 10.

Loop A, defined by the loop from node 104, tap 106, tap 102 via diode D1 and back to node 104, is a recycling loop to recover the leakage energy from the leakage inductance L_{k2} , as will be described in more detail below. Moreover, the loop A in combination with the windings N11, N12 and N13 via taps 102 and 106 of the loop A charges the clamping capacitor C_r to a clamping voltage set forth in Eq. (3) during a first time interval when MOSFET switch S21 is in an on-state and to a clamping voltage set forth in Eq. (4) during a second time interval immediately following the first time interval to clamp the voltage stress V_{S21} across MOSFET switch S21 when it is in an off-state. Diode D2, in series with winding N3, stops the resonance between the leakage inductance L_{k2} and the clamping capacitor C_r . The resonance stops because the current through D2 is unidirectional not bi-directional.

The undotted terminal of winding N12 and the first terminal of C_{O20} are coupled to node 110. Switch S22 has a body diode D22 integrated therewith wherein the anode is coupled to the source and the cathode is coupled to the drain of MOSFET switch S22. The negative side of the DC voltage source 20 and the source of MOSFET switch S22 are coupled to node 108. Node 108 is coupled to ground GND. The second terminal of capacitor C_{O20} is coupled to node 112. Node 112 is coupled to ground GND. Load R_{L20} is coupled across nodes 110 and 112 and is parallel to the output capacitor C_{O20} .

Those skilled in the art would understand that when the switches are in the "on-state" they are conducting current therethrough and when they are in the "off-state" they are not conducting current therethrough. Furthermore, methodologies for controlling MOSFET switches so that they are conducting or non-conducting has been well established. Thus, no further discussion is necessary.

Referring also to Fig. 5, the switching waveforms of the switches S21 and S22, currents I_{S21} and I_{S22} and the voltage stress V_{S21} and V_{S22} across MOSFET switches S21 and S22, respectively, are illustrated. The operation of converter 10 will now be described in detail with respect to the switching waveforms of Fig. 5.

Assume that before T1, MOSFET switch S21 is switched to an off-state and MOSFET switch S22 is switched to an on-state. At time T1, MOSFET switch S21 is switched to an on-state and MOSFET switch S22 is switched to an off-state. The voltage Vc of clamping capacitor Cr is applied to the winding N13. The energy stored in clamping capacitor Cr is transferred to the output or load R_{L20} through the windings N11, N12 and N13 until the voltage Vc gradually changes and is finally clamped to a reflected voltage from N1 and N2, which is given by

$$V_c = \frac{N_3}{N_1 + N_2} * (V_{in} - V_o) \quad \text{Eq. (3)}$$

10

MOSFET switch S21 remains in the on-state and MOSFET switch S22 remains in the off-state for a time period or until time T2.

At time T2, MOSFET switch S21 transitions to an off-state and MOSFET switch S22 transitions to an on-state. At such time, diode D2, in the second path 50, conducts, the energy stored in winding N11 is transferred to winding N12 and the current in winding N12 flows through MOSFET switch S22. However, the leakage energy of leakage inductance Lk2 is not transferred to winding N12. Instead, diode D1, in a conducting state, in path 120 between taps 102 and 106, passes the leakage energy of leakage inductance Lk2 therethrough to the clamping capacitor Cr. Diode D1 is conducting only when switch S21 is off and S22 is on. The leakage energy charges the clamping capacitor Cr. The voltage Vc is given by

$$V_c = \frac{N_1}{N_2} * V_o \quad \text{Eq. (4)}$$

25

Moreover, the voltage stress across switch V_{S21} is the sum of the input voltage V_{in} and the voltage Vc and is expressed as

$$V_{S21} = V_{in} + \frac{N_1}{N_2} * V_o \quad \text{Eq. (5)}$$

30

In view of the foregoing, the voltage stress across switch S21, when switch S21 is in the off-state, is clamped, as best seen in Fig. 5. Thus, high voltage spikes across

switch S21 are essentially eliminated. Furthermore, the leakage energy of the leakage inductance LK2 from winding N11 is recovered when switch S21 is on and is delivered to the output or load R_{L20} instead of charging output capacitor C_{020} . Thus, the converter 10 has a higher efficiency.

5 MOSFET switch S21 remains in the off-state and MOSFET switch S22 remains in the on-state for a time period or until time T3, which ends a complementary periodic cycle. In other words, from time T3 to time T4, switch S21 is in the on-state and switch S22 is in the off-state and so on and so forth. During the complementary periodic cycle, the voltage Vc of the clamping capacitor Cr varies between equations (3) and (4).
10 Numerous modifications to and alternative embodiments of the present invention will be apparent to those skilled in the art in view of the foregoing description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention. Details of the structure may be varied substantially without departing from the invention, and the exclusive
15 use of all modifications which come within the scope of the appended claims is reserved.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The mere fact that
20 certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A tapped-inductor step-down converter comprising:
 - complementarily switched first and second switches (S21, S22);
 - a parallel combination output capacitor (C_{O20}) and load (R_{L20}); and
 - a tapped-inductor (25a, 25b) coupled between the first and second switches
- 5 (S21, S22) having a leaky inductance (L_{k2});
 - a clamping capacitor (C_r) constructed and arranged with the tapped-inductor (25a, 25b) to clamp a voltage across the first switch (S21) when the first switch (S21) is off.
2. The converter to Claim 1, wherein the tapped-inductor (25a, 25b) includes:
 - 10 - first, second and third windings wherein the first winding (N11) is tapped to the second winding (N12) at a tap, and the third winding (N13) is coupled to the first and second windings via a path having a diode (D1) coupled therealong wherein the second switch (S22) is coupled to the tap.
- 15 3. The converter according to Claim 2, further comprising:
 - a DC voltage source (20) providing an input voltage;
 - a first input path having the first switch (S21) coupled thereto; and
 - a second input path having a second diode (D2), an anode of the second diode (D2) is coupled to the DC voltage source (20) and a cathode of the second diode (D2) is
- 20 coupled in series with the undotted terminal of the third winding.
4. The converter according to Claim 2, wherein the clamping capacitor (C_r) has a first terminal coupled to the third winding (N13) and the diode (D1); and a second terminal coupled to the first switch (S21) and the first winding (N11) wherein leaky energy is
- 25 transferred to the clamping capacitor (C_r) and a voltage across the clamping capacitor (C_r) when the first switch (S21) is in an off-state, clamps the first switch (S21).
5. The converter according to Claim 1, wherein the first and second switches (S21, S22) are low voltage rating MOSFETs.

6. A tapped-inductor step-down converter comprising:
- first and second switches (S21, S22) turned on and off in a complementary manner between an on-state and an off-state;
 - 5 - an output capacitor (C_{O20});
 - a load (R_{L20}) coupled in parallel with the output capacitor (C_{O20});
 - a tapped storage inductor (25a, 25b) having first, second and third windings wherein the first winding (N11), having leaky energy, is tapped to the second winding at a tap, and the third winding (N13) is coupled to the first (N11) and second (N12) windings via
 - 10 a path having a diode (D1) coupled therealong wherein the second switch (S22) is coupled to the tap; and
 - a clamping capacitor (Cr) having one terminal coupled to the third winding (N13) and the diode (D1), and the other terminal coupled to the first switch (S21) and the first winding (N11) wherein leaky energy is transferred to the clamping capacitor (Cr) and a
 - 15 voltage across the clamping capacitor (Cr) when the first switch (S21) is in an off-state, clamps the first switch (S21).

7. The converter according to Claim 6, further comprising:
- a DC voltage source (20) providing an input voltage;
 - 20 - a first input path having the first switch (S21) coupled thereto;
 - a second input path having a second diode (D2), an anode of the second diode (D2) is coupled to the DC voltage source (20) and a cathode of the second diode (D2) is coupled in series with the undotted terminal of the third winding.

- 25 8. The converter according to Claim 7, wherein when the first switch (S21) is in the off-state, the voltage across the clamping capacitor (Cr) is given by

$$V_c = \frac{N1}{N2} * V_o$$

- 30 wherein N1 is the first winding having the leaky inductance (L_{k2}) of the tapped-inductor (25a, 25b), N2 is the second winding of the tapped-inductor (25a, 25b) and V_o is an output voltage.

9. The converter according to Claim 8, wherein the voltage stress across the first switch (S21) is the sum of a DC input voltage V_{in} and the voltage V_c and is expressed as

$$V_{s21} = V_{in} + \frac{N1}{N2} * V_o$$

5

10. The converter according to Claim 7, wherein when the second switch (S22) is in the off-state, the voltage across the clamping capacitor (Cr) charged until it reaches a reflected voltage given by

$$V_c = \frac{N3}{N1 + N2} * (V_{in} - V_o)$$

10

wherein $N1$ is the first winding of the tapped-inductor (25a, 25b), $N2$ is the second winding of the tapped-inductor (25a, 25b), $N3$ is the third winding of the tapped-inductor (25a, 25b), V_{in} is a DC input voltage and V_o is an output voltage.

1/4

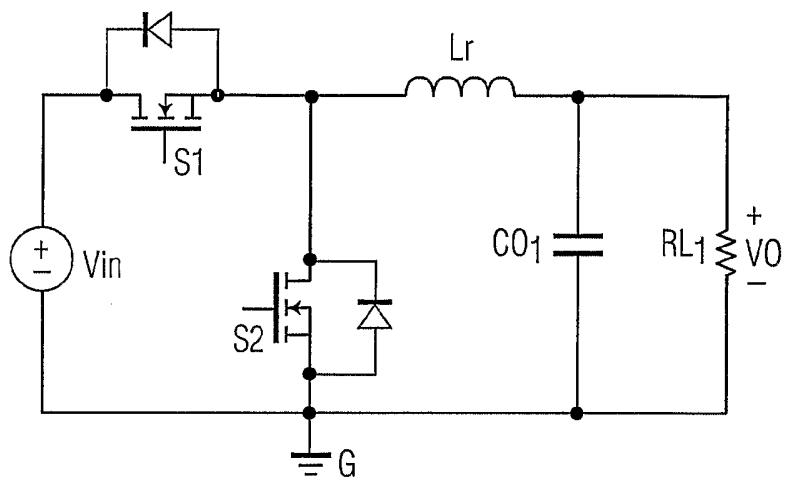


FIG. 1

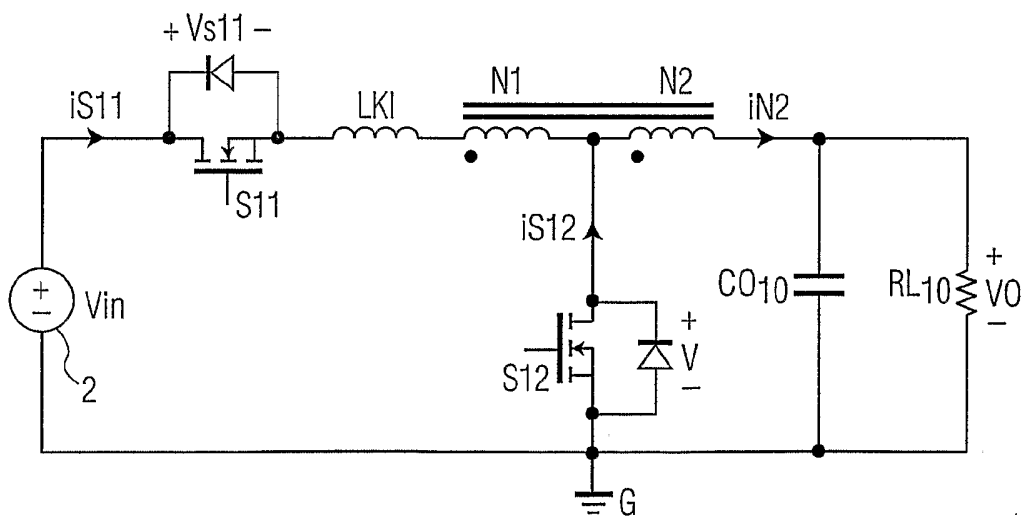


FIG. 2

2/4

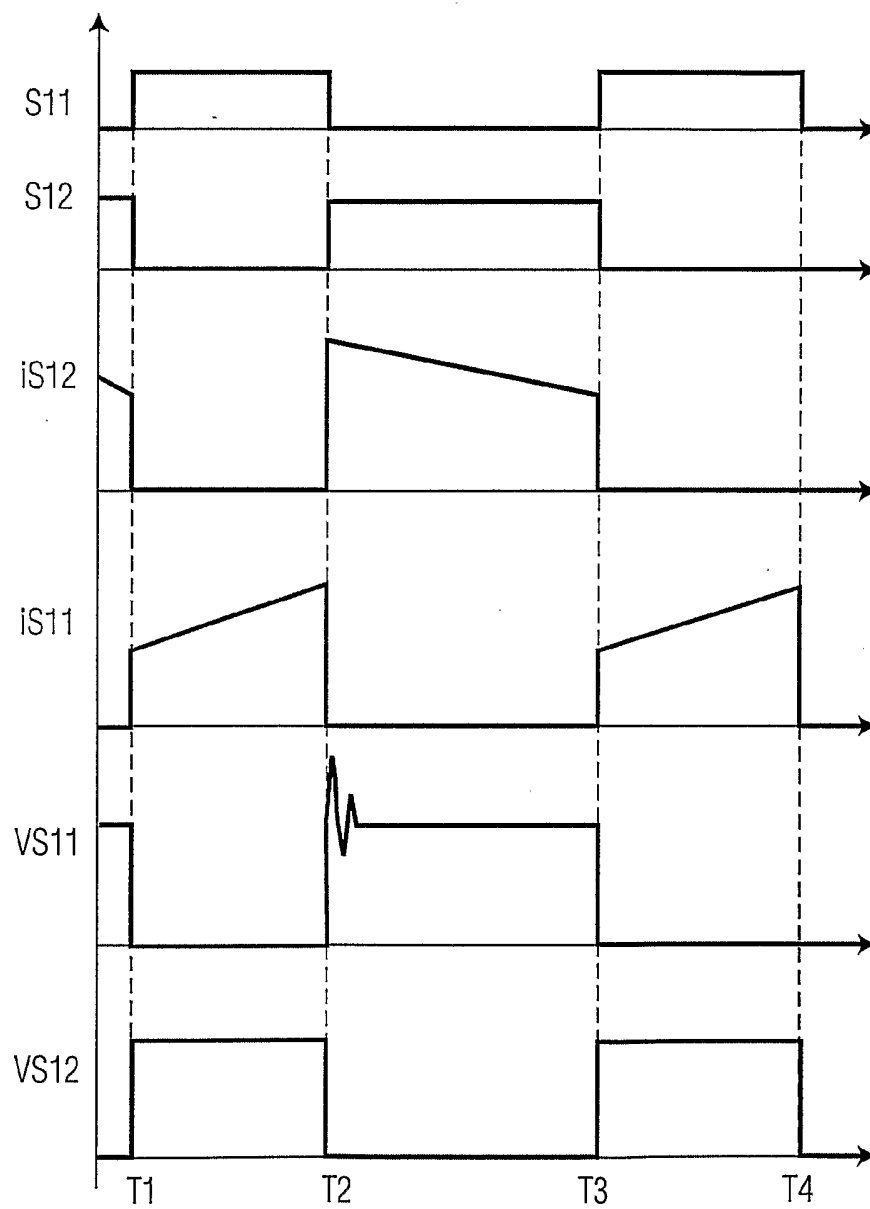


FIG. 3

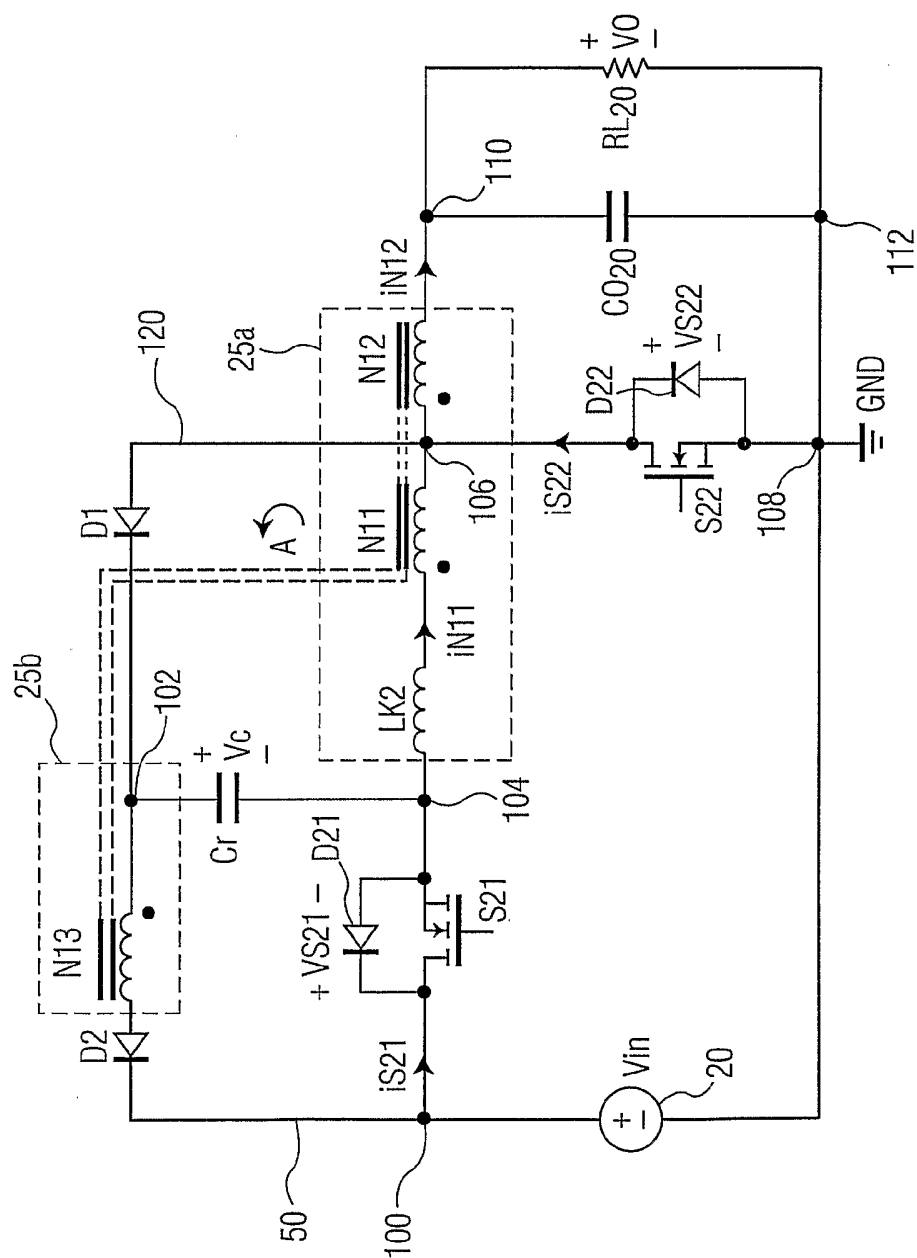


FIG. 4

4/4

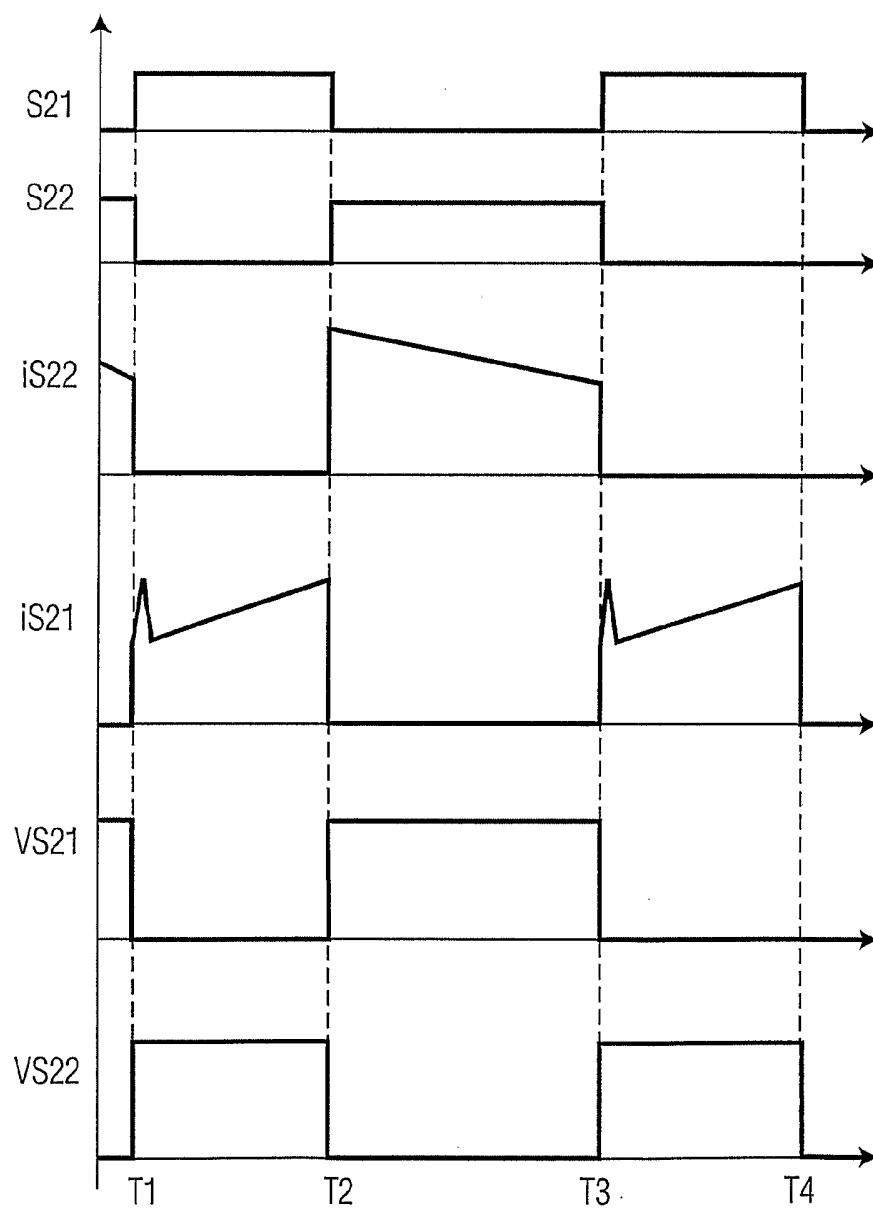


FIG. 5