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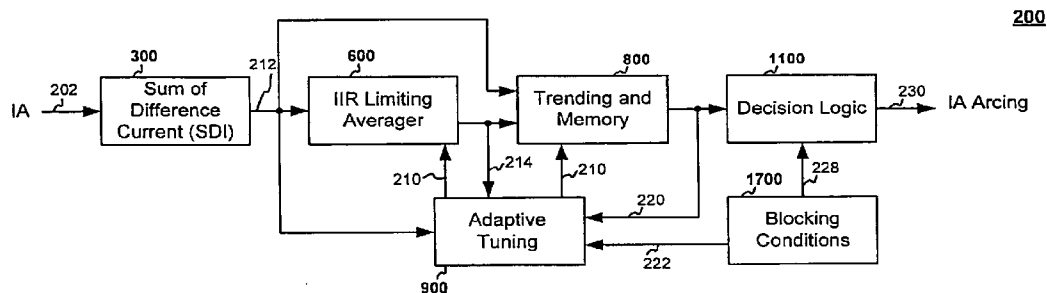
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(54) Title: SYSTEMS AND METHODS FOR DETECTING HIGH-IMPEDANCE FAULTS IN A MULTI-GROUNDED POWER DISTRIBUTION SYSTEM



(57) Abstract: The system and methods monitor odd harmonics within a power distribution system quantity using a special digital filter. A normal level of odd harmonics for the monitored quantity is established. Over predetermined time periods, the odd harmonics within the power distribution quantity are compared to the normal level, and a determination of whether a high-impedance fault is present in the monitored power distribution system is made.

**SYSTEMS AND METHODS FOR DETECTING HIGH-IMPEDANCE FAULTS IN
A MULTI-GROUNDED POWER DISTRIBUTION SYSTEM**

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation in part of application number 11/499,620, filed on August 4, 2006.

FIELD OF THE INVENTION

[0002] The present invention relates generally to detecting high-impedance faults in multi-grounded electric power distribution systems.

BACKGROUND OF THE INVENTION

[0003] High-impedance faults (HIFs) are difficult to detect on multi-grounded electrical power distribution systems. One reason for this difficulty is that many of the loads on the system are single-phase in nature. The system can therefore be quite unbalanced when a major single-phase lateral is out of service. The conventional ground fault protection has to be set above the maximum foreseeable unbalance to avoid false tripping. Conventional ground fault protection is thus not effective for HIF protection.

[0004] The second reason that HIFs are difficult to detect is that the HIF current level is typically small. For example, the HIF current level may range anywhere from about zero amperes to less than 100 amperes depending upon the ground surfaces that a power conductor contacts.

[0005] Many untraditional algorithms have been developed to detect HIF at the substation level in the power distribution system. Most of these algorithms use off-fundamental frequency components of phase or residual currents, and use complicated methods such as expert systems, neural networks, wavelets and higher-order statistics.

[0006] An algorithm that detects certain HIFs is relatively easy to design. However, it is a greater challenge to also design a secure algorithm. Electrical utilities desire to have secure HIF protection. The objective of HIF protection is not to protect the power system and apparatus from damage resulting from an HIF. Rather, the objective of implementing secure HIF protection is to remove an unsafe public condition, which may also avoid or minimize any attendant legal issues relating to the condition. When a detection device indicates the occurrence of an HIF, a utility has to make a decision based upon the circumstances. For example, it may be more dangerous to trip the electrical power to a traffic light at a busy traffic intersection or to a hospital. For such reasons, utilities cannot tolerate false alarms from HIF detection devices.

[0007] Moreover, when an HIF is detected, a number of factors or circumstances may need to be considered before a tripping decision is made. For example, it may be more dangerous to trip the power to traffic lights at a busy intersection, or to a hospital. For reasons such as these, a utility cannot normally tolerate any false HIF detection.

[0008] A general object of the present invention is to therefore provide improved systems and methods for detecting an HIF in a multi-grounded distribution system.

[0009] Another object of the present invention is to provide improved systems and methods for detecting an HIF that is secure from false detections.

[0010] A further object of the present invention is to provide improved systems and methods for detecting an HIF that may be easily incorporated into existing distribution relays and related equipment.

SUMMARY OF THE INVENTION

[0011] The present invention is directed to systems and methods for detecting a high-impedance fault in a multi-grounded electrical distribution system. The system includes a current acquisition circuit, which acquires a digital representation of at least one phase current, and a processor, which examines the digital current quantity and, based on statistics, determines whether or not a fault is present. In particular, the processor develops a long-term histogram that represents the normal level of odd harmonic current in the monitored phase. Based on this long-term histogram, the processor calculates a threshold, against which the monitored odd-harmonic current is measured. If this threshold is exceeded some number of times, a high-impedance fault is present on the monitored phase.

[0012] A method for detecting high-impedance faults is also disclosed. A current is digitally acquired, and the odd harmonic content of the current is measured. The odd harmonic content is conditioned, and a first histogram is calculated over a sufficiently long period of time to be representative of the normal level of odd harmonic current within the monitored phase. Based on the mean, standard deviation, and maximum level of the first histogram, a threshold is calculated. The measured odd harmonic current is compared against this threshold, and if the threshold is exceeded more than a calculated number of times within a window of time, a high-impedance fault is present on the monitored phase. Additionally, a second histogram may be built over a predetermined time period, and used to update the first histogram or, based on a statistical comparison with the first histogram, can be used to indicate the presence of abnormal odd harmonic current activity, potentially indicating the presence of a high-impedance fault on the monitored phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The invention, together with its objects and the advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements in the figures, and in which:

[0014] FIG. 1A is a diagram of a typical electrical distribution system illustrating placement of high-impedance fault (HIF) detection devices in various locations between a substation and end users in accordance with the present invention.

[0015] FIG. 1B is a line diagram of a portion of the electrical distribution system of FIG. 1 in which a distribution feeder includes HIF detection in a substation relay and in a recloser in accordance with the present invention.

[0016] FIG. 2 illustrates a block diagram of an HIF detection process for one of the phases of the electrical power distribution system, such as the A-phase, in accordance with the present invention.

[0017] FIG. 3 is a diagram which illustrates further details of an exemplary implementation of the Sum of Difference Current (SDI) block shown in FIG. 2 in accordance with the present invention.

[0018] FIG. 4 is a waveform illustrating the calculation of difference current and the Sum of Difference Current on a time-domain current waveform in accordance with the present invention.

[0019] FIG. 5 is a schematic diagram illustrating further details of an exemplary implementation of the infinite-impulse-response (IIR) Limiting Averager block shown in FIG. 2 in accordance with the present invention.

[0020] FIG. 6 is a schematic diagram illustrating further details of an exemplary implementation of freeze conditions for the IIR Limiting Averager implementation shown in FIG. 5 in accordance with the present invention.

[0021] FIG. 7 is a schematic diagram illustrating further details of an exemplary implementation of the Trending and Memory block shown in FIG. 2 in accordance with the present invention.

[0022] FIG. 8 is a schematic diagram illustrating further details of an exemplary implementation for the Adaptive Tuning Logic block shown in FIG. 2 in accordance with the present invention.

[0023] FIG. 9 is a schematic diagram illustrating further details of an exemplary implementation of enable conditions for the Adaptive Tuning Logic block shown in FIGS. 2 and 8 in accordance with the present invention.

[0024] FIG. 10 is a schematic diagram illustrating further details of an exemplary implementation for the Decision Logic Counters block shown in FIG. 2 in accordance with the present invention.

[0025] FIG. 11 is a diagram of the counting regions for the variable rd in FIG. 7 for the Trending and Memory block and the variable dt shown in FIG. 10 for the Decision Logic Counters in accordance with the present invention.

[0026] FIG. 12 is a diagram illustrating how the number of counts is generated as a function of the ratio, rd , in accordance with the present invention.

[0027] FIG. 13 is a schematic diagram illustrating the details of generating a clear condition for the Decision Logic block shown in FIG. 10 in accordance with the present invention.

[0028] FIG. 14 is a flowchart illustrating the methods employed in detecting an HIF in a multi-grounded distribution system in accordance with the present invention.

[0029] FIG. 15A illustrates a block diagram of an alternate embodiment of the HIF detector shown in FIG. 2 for one of the phases of the electrical power distribution system, such as for the A-phase, in accordance with the present invention.

[0030] FIG. 15B illustrates a block diagram for an enhancement portion of the alternate embodiment of the HIF detector shown in FIG. 15A in accordance with the present invention.

[0031] FIG. 15C illustrates a block diagram for a one-cycle special filter of the alternate embodiment of the HIF detector shown in FIG. 15A and for the enhancement portion shown in FIG. 15B, in accordance with the present invention.

[0032] FIG. 15D illustrates a block diagram for further details of the decision logic in the alternate embodiment of the HIF detector shown in FIG. 15A and for the enhancement portion shown in FIG. 15B, in accordance with the present invention.

[0033] FIG. 16 illustrates a block diagram of an alternate preferred embodiment of a HIF detector for one of the phases of an electrical power distribution system, in accordance with the disclosed invention.

[0034] FIG. 17 illustrates a histogram of odd-harmonic current data captured and used in accordance with the disclosed invention.

[0035] FIG. 18 illustrates a block diagram for further details of the Statistics block in the alternate preferred embodiment of the HIF detector shown in FIG. 16 in accordance with the present invention.

[0036] FIG. 19 illustrates a block diagram for further details of the Decision block in the alternate preferred embodiment of the HIF detector shown in FIG. 16 in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] It will be understood that the present invention may be embodied in other specific forms without departing from the spirit thereof. The present examples and embodiments, therefore, are to be considered in all respects as illustrative and not restrictive, and the invention is not to be limited to the details presented herein. FIG. 1A illustrates an exemplary electrical power distribution system, generally designated 100. Electrical power distribution system 100 provides electrical power, such as from a substation 114 to an end user location 110 and to a load center 120.

[0038] Figure 1A also depicts possible locations of detection devices for detection of high-impedance faults in an electric power distribution system from a substation 114 to end-users, such as at 110. For example, many of the devices in FIG. 1A constitute a high-impedance fault detection system and coordinate with each other using the fault current magnitudes, the number of arcing counts and/or communication signals. Such devices may include, for example, a fault

indicator with HIF detection 101; a pole-top recloser with HIF detection and coordination 102; a fault Indicator with HIF detection 103; a video camera 104 with communication means; an electronic fuse with HIF detection 106; a loss of voltage detection 108 with communication means; an end user location 110 which may automatically call upon loss of service; a video camera 112 with communication means; a substation 114 with wireless, power-line carrier, fiber and other communications; a sectionalizer 116 with HIF detection; an electronic fuse 118 with HIF detection; a loss of voltage detection device 126 with communication means; a signal injection device 128; a signal receiving and alarming device 130 and 132; an altimeter or laser range finder 134 with a down-conductor detection device; and/or a fault indicator 136 with loss of voltage alarm

[0039] The loss of voltage at an end user location 110 is one of the most reliable detection methods of high-impedance fault caused by downed conductors. Once a loss of voltage condition is detected, either by an end user location 110 or by a detection device 108 or 126, such as a loss of voltage detection, the condition is communicated back to an operator of the system, either by a customer call or a communication signal through a fiber, radio, wireless, power line carrier or other communication channels. The operator then sends out someone to locate the fault.

[0040] All the detection algorithms designed for a substation detection device can be fitted or simplified to fit in a device such as pole-top recloser controls 102 with HIF detection and coordination, sectionalizers 116, electronic smart fuses 106 and 118 and fault indicators 101 and 103. As the current magnitude of a high-impedance fault is small and its rich high frequency and harmonic contents attenuate from the fault location back to a substation, it is easier to detect the high-impedance fault as we move a detection device from substation close to the fault.

[0041] FIG. 1A also includes other types of devices to compliment the entire high-impedance fault detection system. A video camera 104 that has image pattern recognition program or a visual monitoring system, such as one disclosed in U.S. Patent No. 5,805,813, can be used to detect a downed

conductor and communicate the information to system operators through wireless or other communication systems. An altimeter 134 or a laser range finder can also be used to detect a dramatic position change of conductors and alarm system operators. Finally, a signal injecting and receiving system 128, 130 and 132 can be also installed in a distribution system to detect a broken conductor and provide alarms. It is much like the loss of voltage system described earlier.

[0042] FIG 1B is a subset of FIG. 1A in terms of high-impedance fault protections and distribution feeder configurations. FIG 1B shows the concept of coordination between the substation feeder relay 150 and the recloser control 156 for a high-impedance fault 160 that occurs downstream to the recloser control 156. A main feeder 152 provides electrical power from a substation 114 to a plurality of single-phase or three-phase lateral lines 164, 166 and 168. Each of lateral lines 164, 166 and 168 is protected by a fuse 154, 158 and 162, respectively.

[0043] The HIF detection techniques of the present invention can be implemented into existing intelligent electronic devices (IEDs), such as relays. The IED may include, for example, feeder relay 150 and recloser 156 shown in FIG. 1B. Preferably, the HIF techniques of the present invention are within the processing capabilities of existing IEDs such that existing IEDs may be retrofitted with the present invention.

[0044] Preferably, these HIF detection techniques include the following four elements or characteristics. (1) An informative quantity that reveals HIF signatures as much as possible and that is not affected by loads or other system operation conditions. (2) A running average of the quantity that provides a stable pre-fault reference. This average is preferably available all the times, including during an HIF condition, and does not require quick tracking of the fault quantity. (3) Adaptive tuning that learns and tunes out feeder ambient noise conditions. Preferably, the tuning is active whenever there is no HIF detected on the system. (4) An effective artificial intelligent classification or pattern recognition method to

differentiate an HIF condition from other system conditions, such as switching operations and noisy loads.

[0045] FIG. 2 shows a block diagram 200 of the HIF methods for the A-phase current. Similar processing should also be implemented for the B- and C-phase currents in a three-phase distribution system. An input quantity such as A-phase current 202 is input to a sum of difference current (SDI) 300, which calculates a quantity on which the HIF detection is based. This quantity is called SDI 212 for sum of difference current. An IIR (infinite-impulse-response) limiting averager 600 provides a stable SDI reference 214. The trending and memory 800 compares SDI with this SDI reference 214 from IIR Limiting Averager. The trending and memory block then memorizes the time and a ratio if SDI is a set-threshold above the average. These results from the trending and memory 800 are then used by the decision logic 1100 to derive a final decision of HIF occurrence on the monitored phase of the distribution system. The adaptive tuning 900 monitors the feeder background noise during normal system operations and establishes a comparison threshold 210 for the trending and memory 800. This comparison threshold 210 is also used by IIR limiting averager 600 to limit the input magnitude to the IIR limiting averager when it is too large. The Blocking Conditions block 1700 detects system conditions other than high-impedance faults and then blocks the functions such as adaptive tuning 900 and the decision logic 1100.

[0046] As identified earlier, the quantity to be used in HIF detection is important to the detection success. Since the HIF fault current magnitude, either the root mean square (RMS) value or the magnitude of the fundamental system frequency component, is much below the maximum possible load unbalance at the substation, other quantities need to be searched or evaluated for HIF detection. Each distribution feeder, such as feeder 152 in FIG. 1B, has a certain amount of harmonic energy during normal operations. This energy is normally dominated by the odd-harmonic energy. All harmonic and off-harmonic contents contain the information of arcing high-impedance faults. Because normal system operations produce little even and off-harmonic energy, the even or off-harmonic

energy generally provide better fault indications. Off-harmonics may include non-integer multiples of a fundamental frequency. Calculating even-harmonic energy requires expensive Fast Fourier Transform (FFT) operations. However, the total off-harmonic content can be simply obtained through a summation of absolute values of a differenced current with a differencing window that is one cycle of the system frequency.

[0047] In FIG. 3, the details of the SDI block 300 in FIG. 2 are shown in greater detail. Ideally, the power system frequency is tracked and the three-phase currents from a power distribution feeder, such as feeder 152, are sampled at an integer number of samples per cycle. Hereafter, a variable name without a subscript is a collective term for a variable, such as SDI, for example. When a signal value is referred to at a specific time instance, the variable name is used with a subscript. For example, SDI_k is a specific SDI value at the time instance k . The example shown in FIG. 5 uses a sampling rate of 32 samples per cycle. In FIG. 3, the subscript k refers to the present sampling time, and $k-1$ refers to the previous sampling time. $k-32$ refers to the time of 32 samples ago, which separates in time exactly one cycle from present sampling time k for a 32-sample-per-cycle sampling rate. Mathematically, the calculations of the difference current (DI) and the sum of difference current (SDI) can be expressed in the following equations,

$$DI_k = |I_k - I_{k-32}|$$

$$SDI_k = \sum_{n=0}^a DI_{k-n},$$

where a represents the number of samples desired for summation.

[0048] The SDI calculation uses two memory blocks. The first memory 304 in FIG. 3 is one-cycle long. Memory 304 saves one-cycle worth of current samples 302 and provides a one-cycle old sample in the difference calculation 306. The other memory 312 may be from two to several cycles long to save several cycles worth of the absolute values of difference currents from the difference calculation 306 and to provide all samples for the summation

calculation by summer 314. DI on line 308 is calculated at the sampling rate of the currents. However, SDI on line 316 may be calculated once every two cycles.

[0049] FIG. 4 shows the difference current and the SDI calculation on a time-domain current waveform 406. The frequency magnitude response of the one-cycle difference calculations by the SDI calculator in FIG. 3 has a magnitude response which is zero at every harmonic frequency point including the DC and the fundamental frequency. Therefore, all harmonic contents including the DC and the fundamental frequency of the current are blocked after the difference calculation of the SDI current in FIG. 3. However, the frequency components near the half harmonics are amplified by the difference calculation, that is, the gain of the frequency response is greater than one. The frequency contents of the difference current on line 316 of the SDI therefore contain only off harmonics. SDI represents a measure of the average total off-harmonic content of a current over a two-cycle window. This makes SDI a desirable quantity for use in HIF detection.

[0050] The IIR limiting averager is shown in greater detail in FIG. 5. The IIR limiting averager provides a reliable reference average, SDI_REF_k on an output line 606. A reliable reference average is important to successful HIF detection. An infinite-impulse-response (IIR) type of averaging with a fixed time constant is used because long-time memory effects can be achieved efficiently with fewer calculations and memory units. A relatively long time constant is preferably chosen to provide a stable reference during faults. For example, a one-second time constant may be used. To prevent that the reference average on output line 606 from quickly following the sporadic spikes of off-harmonic content when the SDI value is above a threshold, the input to the averager 600 is preferably limited. Alternatively, another way of stabilizing the average output in case of high input spikes is to use a variable time constant. For example, U.S. Patent No. 5,790,418 (hereby incorporated by reference) discloses a polarizing quantity memory filter.

[0051] FIG. 5 shows the details of the IIR input limiting averager 600. The averager output, SDI_REF_k , follows the general first order IIR equation,

$$SDI_REF_k = (1 - \alpha) \cdot x_{in} + \alpha \cdot SDI_REF_{k-1},$$

where α relates to the time constant and x_{in} can take two possible values according to the output of comparator 608. The input to the positive polarity of the comparator 608 is SDI_k from line 602, and the input to the negative polarity of the comparator 608 is $sd + SDI_REF_{k-1}$. Constant s can be any integer larger than one. The variable d will be introduced below with respect to the adaptive tuning and it can be treated as a constant here. The comparator output will be a logic 1 if $SDI_k > sd + SDI_REF_{k-1}$, and a logic 0 otherwise. When the comparator output is a logic 0, the switch SW is in its position 1 and x_{in} therefore equals to SDI_k . When the comparator output is a logic 1, the switch SW is in its position 2 and x_{in} therefore equals to $d + SDI_REF_{k-1}$. Putting everything together, the output of the averager 600 on line 606, SDI_REF_k , is calculated from the equation,

$$\begin{aligned} SDI_REF_k &= (1 - \alpha) \cdot SDI_k + \alpha \cdot SDI_REF_{k-1} && \text{if } SDI_k < s \cdot d + SDI_REF_{k-1} \\ &= (1 - \alpha) \cdot f \cdot d + SDI_REF_{k-1} && \text{otherwise} \end{aligned}$$

[0052] The following equation relates the time constant TC in seconds, to the α value, at a given processing rate PR in Hz,

$$\alpha = e^{-\frac{1}{PR \cdot TC}}.$$

For example, if TC is chosen to be one second, then α equals to 0.9672 when the processing rate is 30Hz, or every two cycles for the 60Hz power systems.

[0053] When conditions other than HIF occur, the freeze input on line 604 to the IIR limiting averager 600 is a logic 1 and the IIR limiting average calculation is suspended. For example, these non-HIF conditions may include large difference currents and some difference voltages.

[0054] The IIR freeze/M clear input on line 604 of the IIR limiting averager 600 in FIG. 5 may be generated as shown in FIG. 6. An N-cycle memory 712 stores current samples I_k from the monitored phase of the electrical distribution system. Absolute values of these current samples I_k on line 714 are compared to a threshold at comparator 716. Those current samples which exceed the threshold are time delayed in a timer 718, which provides the dI_DISTURB output on line 702. Similarly, an N-cycle memory 722 stores N voltage samples V_k from the monitored phase of the electrical distribution system. Absolute values of voltage samples V_k on line 724 are compared to a threshold at comparator 726. Those voltage samples which exceed the threshold are time delayed in a timer 728, which provides the dV_DISTURB output on line 704. The outputs dI_DISTURB and dV_DISTURB are then input to an OR gate 706. The outputs of OR gate 706 are stored in a table 708. Those values of current or voltage which exceeded the thresholds may then initiate a freeze of the IIR limiting averager 600 on input line 604 in FIG. 5. Otherwise, this input to the averager will clear the memory in the averager.

[0055] The trending and memory 800 of FIG. 2 is shown in greater detail in FIG. 7. Once the detection quantity SDI and its average SDI_REF are established by the sum of difference current 300 and by the IIR limiting averager 600, respectively, the HIF signatures or information can be extracted from these quantities. The purpose of the trending and memory 800 is to record unusual changes of SDI that is related to HIF on the system and to memorize these changes for the decision logic 1100. The trending and memory logic 800 thus provides information regarding how much and how often SDI exceeds SDI_REF plus a margin d.

[0056] The portion of the logic below the comparator 805 in FIG. 7 runs at the rate of every SDI update, or 30Hz when SDI is calculated every two cycles as in the prior example. The rest portion of the logic runs whenever comparator 805 outputs a logic 1. The absolute value of the difference between SDI 802 and SDI_REF 803, or dSDI 804, goes to the positive input of the comparator 805. The negative input of the comparator is connected to a variable d. The variable d

will be introduced in the Adaptive Tuning subsection, paragraphs 0058-0062 below, and can be treated as a constant here.

[0057] When dSDI is greater than d , the output of comparator 805 will be a logic 1. Otherwise the comparator output is a logic 0. A logic 1 from comparator 805 closes the switch 807, which takes a record of the time at which the switch 807 closes. The recorded time is saved in a memory block 816 which has enough units to save the maximum possible number of t_k within one second. When the comparator is operating at a rate of 30 Hz, the maximum number of t_k is also 30 and the memory should have 30 units. At the beginning of each second, in the previous set $\{t_1, t_2, \dots, t_n\}$ is not zero, then the last time value, t_n , is moved to a single memory unit 817 as t_{old} . If set $\{t_1, t_2, \dots, t_n\}$ does not have any members, then memory 817 retains its previous value as t_{old} .

[0058] A logic 1 output from the comparator 805 also enables on line 810 a ratio calculation at block 812 of dSDI to d . The calculated ratio values, rd_k , are saved in another memory 818 that has the same number of units as memory 816. The outputs on lines 820, 822 and 824 of the trending and memory logic 800 are sets of t , the old time value t_{old} , and rd , respectively, within previous one second time. The number of t and rd records within the previous one second is n , which is another output on line 820. When conditions other than HIF occur, the freeze input is a logic 1, the memories 817 and 818 are cleared and their updates are also suspended. These non-HIF conditions may include large difference current changes and smaller difference voltage changes.

[0059] During power distribution feeder normal operations, different loads come on and off, motors start and stop, capacitors and load-tap changers switch on and off. These activities all affect the sum of different current SDI and its total off-harmonic contents. Changes in these feeder operations and load characteristics may be hourly, daily, monthly or seasonal. To make the HIF detection function dependable and secure, all such feeder operations and load characteristics are better acquainted by the detection logic. The purpose of the adaptive tuning 900 in FIG. 2 is to learn or develop a margin above SDI average that SDI value may fall into during normal system operations. This margin is

denoted as variable d , which is used in both IIR limiting averager 600 and in trending and memory 800.

[0060] FIG. 8 provides further details of the adaptive tuning logic 900 of FIG. 2. In this logic, the comparator 910, timer 914 and the corresponding upper-row d update calculation run periodically, such as once every five minutes. The rest of the logic, such as comparator 912 and timer 916, runs more frequently or continuously, such as every one-second. There are two inputs on the right of FIG. 8, n on line 904 and $n5$ on line 906. n is the number of times that SDI was above its average plus the margin d within previous one second of time, as explained above with respect to the trending and memory logic 800. The value n is added up for five minutes in an accumulator 908 and its output is $n5$ on line 906, which in this example is the number of times that SDI was above its average plus the margin d within previous five minutes of time.

[0061] A first comparator 912 of the adaptive tuning logic 900, compares the value of n to a threshold p_2 . If n is greater than p_2 , the output of comparator 912 is a logic 1, otherwise, the output of comparator 912 is a logic 0. If the output of comparator 912 is a logic 1 for a consecutive period of Dpu_2 seconds, as is determined by the timer 916, the timer 916 outputs a logic 1, which enables the bottom row of block 918 to initiate an update calculation of the margin d . At the same time, the logic 1 output of timer 916 goes to an input of AND gate 917 to force its output to a logic 0. In other words, if SDI is above its average plus a margin d for more than p_2 in a second, and if the condition lasts for Dpu_2 , then the margin d is determined to be too small, and the corresponding update calculation will increase the margin d by a predetermined amount, such as in accordance with the equation

$$d_k = d_k + h_2 \cdot SDI_REF_k.$$

For example, h_2 may be a value in the range of 0 to 25 percent and the margin d may typically be increased by about five percent of the average.

[0062] A second comparator 910 of the adaptive tuning logic 900 compares the value of n_5 to a threshold p_1 . If n_5 is less than p_1 , the output of comparator 910 is a logic 1, otherwise, the output of comparator 910 is a logic 0. If the output of comparator 910 is logic 1 for a consecutive period of Dpu_1 minutes as is determined by the timer 914, the timer 914 outputs a logic 1, which enables the upper row d update calculation in the upper row of block 918. At the same time, the logic 1 output of timer 914 goes to an input of AND gate 917 to force its output to a logic 0. In other words, if SDI is not above its average plus a margin d for Dpu_1 time, then the margin d is determined to be too large, and the corresponding update calculation will decrease it by a predetermined amount, such as in accordance with the equation

$$d_k = d_k - h_1 \cdot SDI_REF_k.$$

For example, h_1 may be a value in the range of 0 to 25 percent and the margin d may be decreased by about two percent of the average.

[0063] If both outputs of timers 914 and 916 are logic 0, the AND gate 917 outputs a logic 1, which enables the middle row of block 918 to update the calculation for the margin d. In this instance, the new value for margin d may be kept the same as the prior value.

[0064] The AT Enable input 924 of FIG. 8 determines when the update for d takes place. Ideally, the tuning process should be continuous as long as there is no HIF or other faults on the system. The tuning should be also enforced within certain period of time after a breaker closure is detected and currents are detected.

[0065] FIG. 9 shows the enable conditions for the adaptive tuning logic 900 in FIG. 8. Part of the enable logic, OR1 gate 1026 and timer 1032, is also used to freeze IIR limiting averager 600, as shown in FIG. 5.

[0066] FIG. 10 shows further details of the decision logic 1100, also previously shown in FIG. 2. The trending and memory function block 800 in FIGS. 2 and 7 provides rich information regarding to "how much" and "how often"

that SDI overcomes its reference plus a learnt margin d . The information of “how much” is represented by a set of ratios, $\{rd\}$. The information of “how often” is represented by the value of n , the number of times that SDI went above the threshold within previous one second. The first block 1102 of the decision logic 1100 in FIG. 10 calculates a set of time differences, $\{dt\}$, using the set of time, $\{t\}$ and t_{old} from the trending and memory 800. The time difference can provide the time characteristic of randomness signature of the high-impedance faults. This information can be used in more sophisticated artificial intelligence methods of classification and pattern recognition, such as neural networks, expert systems or decision trees. For this invention, however, we choose to use a pair of counters 1116 and 1118, as shown in FIG. 10.

[0067] The decision logic 1100 may run at a rate of once per second. In this example, it utilizes two counters; counter 1116 for providing an HIF fault output 1120 and counter 1118 for providing an HIF alarm output 1122. For each pair of (rd, dt) in previous one-second segment, the decision of count or no-count for fault or alarm, and the number of counts are determined in the counting scheme. For example, for each one-second segment, if the number of counts for HIF fault is greater than q_1 , as is determined by comparator 1112, the comparator 1112 outputs a logic 1. Counter 1116 accumulates the number of logic 1s from comparator 1112. If three occurrences are accumulated within five one-second segments, counter 1112 outputs a logic 1 to indicate a high-impedance fault detection. The HIF alarm decision is derived in a similar way through comparator 1114 and counter 1118. Comparator 1114 may use a different detection threshold from that used by comparator 1112 as indicated at comparator inputs 1108 and 1110 in FIG. 10.

[0068] FIG. 11 shows an entire dt - rd plane 1200, which is divided into three regions: a fault count region 1202, an alarm count region 1204 and a no count region 1206. In this example, the dt axis 1208 has units of 2-cycles. For example, a value of 30 represents 30 2-cycle periods, or one second for 60Hz power systems. If $\{rd, dt\}$ pair falls in the no count region 1206, no number of counts are generated for alarm and fault in the decision logic 1100. If $\{rd, dt\}$ pair

falls in the alarm count region 1204, only counts are generated for HIF alarm. If {rd,dt} pair falls in the fault count region 1202, counts are generated for both HIF fault and alarm.

[0069] FIG. 12 shows a graphical representation of how the number of counts is generated as a function of the ratio, rd, for each {rd,dt} pair that is determined to be countable in the plane 1200 of FIG. 11. For example, if the rd value in a {rd,dt} pair is 4, and the pair falls in the fault count region 1202, then two counts are generated for this pair of {rd,dt}. Further, if the {rd,dt} pair is the only occurrence in a one-second segment, then the total of two counts is used in the operations of comparators 1112 and 1114 of the decision logic 1100. If comparator 1112 has a threshold of 3 ($q_1 = 3$) in the above example, the output of comparator 1112 will be a logic 0 and no accumulation is added to counter 1116. On the other hand, if comparator 1114 has a threshold of 1 ($q_2 = 1$), the output of comparator 1114 will be a logic 1 and one count is accumulated into counter 1118.

[0070] FIG. 13 shows the enable logic 1400 for the adaptive tuning logic 900 in FIG. 8 for a three-phase distribution system. It will be noted that the logic 1400 is similar to the enable logic 1000 in FIG. 9. In particular, OR gate 1414, timer 1420, comparator 1405, AND gate 1407 and timer 1422 in FIG. 13 are similar to corresponding elements 1028, 1034, 1029, 1030 and 1036 in FIG. 9, respectively. However, the times from the A, B and C-phases are input on lines 1408, 1410 and 1412 to block 1418 to provide for three-phase monitoring in the enable logic 1400 of FIG. 13. In contrast, the enable logic 1000 of FIG. 9 is suited for single phase monitoring.

[0071] The enable logic 1400 in FIG. 13 determines three-phase event conditions. The input {t}_A on line 1408 represents the set of time incidences that the A-phase SDI difference is above the tuned threshold within the previous second, the input {t}_B on line 1410 represents the set of time incidences that the B-phase SDI difference is above the tuned threshold within the previous second, and the input {t}_C on line 1412 represents the set of time incidences that the C-phase SDI difference is above the tuned threshold within the previous second.

Function block 1418 then determines if there are common values from the $\{t\}_A$, $\{t\}_B$ and $\{t\}_C$ inputs. If at least one common non-zero value is detected, the input on line 1423 to a timer 1424 changes state, such as to a logic 1. The output 1430 of timer 1424 then changes state for a predetermined time, such as for Ddo_6 seconds, to block the decision logic.

[0072] FIG. 14 illustrates an embodiment of a method of detecting high-impedance faults in a multi-grounded distribution system. At block 1502, the power system quantities $I_k, \dots, I_{k-32}, \dots$ are sampled. Block 1506 receives these power system quantities from block 1502 and calculates the absolute values of one-cycle difference filter, $DI_k = |I_k - I_{k-32}|$. Block 1508 receives the absolute values of one-cycle difference filter from block 1506 and calculates the sum of absolute differences, such as in accordance with the equation

$$SDI_k = \sum_{n=0}^{63} DI_{k-n}.$$

[0073] These results are supplied to the adaptive tuning and set threshold margin block 1518. Block 1510 receives the margin, d_k , from block 1518, and the sum of absolute difference from block 1508 and establishes a reference, SDI_REF_k , with an IIR limiting averager. This reference is also supplied to the adaptive tuning and set threshold margin block 1518. Block 1512 receives the margin d_k from block 1518 and the reference, SDI_REF_k , from block 1510. It then determines the trending and memory value $dSDI_k = \text{ABS}(SDI_k - SDI_REF_k)$. The ratio, $rd_k = dSDI_k / d_k$, is determined at block 1514 and this ratio is supplied to the adaptive tuning and set threshold margin block 1518 and to the decision logic at block 1516. Adaptive tuning 1518 also receives the ratio rd_k from block 1514. Blocking conditions at block 1522 are provided to the decision logic at block 1516 and to the adaptive tuning and set threshold margin block 1518. The decision logic at block 1516 then sets counters, defines fault count/no-count regions and alarm count/no-count regions. Block 1524 then receives information from decision logic block 1524 and determines if an HIF condition exists. If so, block 1526 is informed to take a safety measure. If not, the method returns to block 1502 to continue monitoring for an HIF.

[0074] FIG. 15A illustrates an alternative preferred embodiment 1600 of a system or method for determining an HIF condition, as compared to the preferred embodiment 200 shown in FIG. 2. In this embodiment, the blocks of the lower level correspond to the blocks of FIG. 2, namely: 1) the Sum of Difference Current (SDI) 1621 corresponds to the Sum of Difference Current (SDI) 300, 2) IIR Limiting Averager 1622 corresponds to IIR Limiting Averager 600, 3) Trending and Memory 1624 corresponds to Trending and Memory 800, 4) Adaptive Tuning 1626 corresponds to Adaptive Tuning 900, 5) Blocking Conditions 1630 corresponds to Blocking Conditions 1700 and 6) Decision Logic 1628 corresponds to Decision Logic 1100. In particular, an enhancement portion 1601 (see FIG. 15B) has been added to the blocks shown in FIG. 2. FIG. 15B shows the enhancement portion 1601 separately from the more detailed embodiment shown in FIG. 15A. It will be appreciated that the enhancement portion 1601 provides a separate HIF output HIF_A on line 1611, which may be combined by a gate 1632 with the output on line 1629 from the preferred embodiment 200 shown in FIG. 2. The first element in the enhancement portion 1601 is a one-cycle special filter 1602, which is shown in greater detail in FIG. 16C. The output IAs of special filter 1602 is formed by summing the outputs of two parallel filters 1612 and 1614. The first filter is a one-cycle cosine filter 1612 plus a phase adjustment and the second filter is a half-cycle differentiator 1614. Thus, power system quantities are filtered by each filter 1612 and 1614 separately and then summed by a summer to provide output IAs. Those skilled in the art can also combine two filters together and form a one-cycle FIR filter. Output IAs of special filter 1602 thus contains frequency contents of a signal around all odd harmonics in the pass band. The accumulator 1604 accumulates the absolute values of output IAs. The output ISMA of accumulator 1604 may be defined by the following equation

$$ISMA = \sum_0^{N_s} IAs_k.$$

where the accumulating time is for N_s seconds. For example, N_s may range from one cycle of samples to ten cycles of samples.

[0075] The finite impulse response (FIR) smoothing block 1606 calculates an average of the output ISMA from accumulator 1604 to smooth out the random changes of the signal content. For instance, the FIR smoothing block could average the incoming ISMA signals using the following equation:

$$ISMA_{FIR_k} = \frac{2}{N} \sum_{i=0}^{\frac{N}{2}-1} ISMA_{k-i}$$

[0076] The infinite impulse response (IIR) limiting averager 1608 may be similar in function to the previously described IIR limiting averager 600 shown in FIG. 5. The IIR limiting averager 1608 provides a long-term reference for the signal contents from the one-cycle special filter 1602. In order to make this reference stable in case of sporadic large excursions of input, the output of IIR limiting averager may be limited in accordance with the following equation

$$\begin{aligned} ISMAREF_k &= (1-\alpha) \cdot ISMA_k + \alpha \cdot ISMAREF_{k-1} && \text{if } ISMA_k < 2 \cdot ISMA_REF_{k-1} \\ &= (2-\alpha) \cdot ISMAREF_{k-1} && \text{otherwise} \end{aligned}$$

where α is a constant dependent on the power system frequency as described above. ISMAREF is the output of the IIR limiting averager 1608 and ISMA is the input to the IIR limiting averager 1608. The subscript k represents a value of a variable at the specific time instant k . The subscript $k-1$ represents a value of a variable at time instant $k-1$, which is one processing instance older than time instant k . The FIR smoothing function 1606 smoothes the signal content to a smoothed signal quantity on its output line 1616. This smoothed signal quantity on line 1616 and the ISMAREF signal on output line 1617 of the IIR limiting averager are both routed to the decision logic 1610.

[0077] FIG. 15D illustrates an exemplary embodiment of the decision logic 1610. The decision logic 1610 compares the smoothed signal quantity from FIR smoothing 1606 and the ISMAREF signal from IIR limiting averager 1608 with

corresponding adaptive thresholds 1618 and 1620. If the smoothed signal quantity is above the corresponding adaptive threshold 1618 plus the signal ISMAREF for a corresponding certain time period, as set by timer 1619, and if the output of an AND gate 1623 is a logic zero, then the decision logic 1610 outputs a logic one to signify the detection of an arcing high-impedance fault HIF on the monitored distribution feeder. As each distribution feeder carries different loads and therefore has a certain amount of ambient signal content, the thresholds 1618 and 1620 used in the decision logic are adaptive in nature and are derived in a similar manner to the previously described adaptive tuning 900 in FIG. 8. If the smoothed signal quantity on line 1616 is above the corresponding adaptive threshold 1620 plus the signal ISMAREF for a corresponding certain time period, as set by timer 1625, and if this condition is true for all A, B and C three phases, then the output of AND gate 1623 is a logic one. A logic one output from AND gate 1623 represents system three-phase conditions other than a high-impedance fault, such as a distribution capacitor bank assertion. The logic one output of AND gate 1623 clears timer 1619 and thereby disables any high-impedance fault detection.

[0078] FIG. 16 illustrates an additional alternative preferred embodiment. This embodiment builds on the embodiment of FIGs. 15A, 15B, and 15C. In particular, the Detection Signal Generation block 2001 incorporates the One-Cycle Special Filter 1602 and Accumulator (Absolute Values) 1604, which are discussed above. In addition, the FIR Smoothing block 2003 is identical to the FIR Smoothing block 1606 of FIGs. 15A and 15B; and the IIR Limiting Averager 2005 is identical to the IIR Limiting Averager 1608 of FIGs. 15A and 15B. However, the basic operating principle of the embodiment disclosed by FIG. 16 differs substantially from the operation of the earlier discussed embodiments.

[0079] The embodiment of FIG. 16 operates by determining whether the odd harmonics present in the current of a given phase have changed in a statistically significant way from a constantly updated "normal" level. The basic operation of this embodiment is the maintenance of a long-term histogram comprised of events indicating the level of odd harmonic current in the monitored

phase. A sample histogram is illustrated in FIG. 17. A histogram shows the number of times within a predetermined time period that the measured odd harmonic current falls within a particular range. By comparing the long-term histogram, which represents the normal level of odd harmonic current within the measured phase, with a shorter window of collected odd harmonic current data, a high impedance fault can be detected.

[0080] In operation, Difference block 2007 accepts the output of FIR Smoothing block 2003 and IIR Limiting Averager Block 2005. Difference block 2007 then generates a sample by sample difference of the incoming ISMAFIR and ISMAREF signals through the following formula:

$$dISMA_k = ISMAFIR_k - ISMAREF_k$$

[0081] The Statistics block 2009 builds both the long-term histogram and the short-term histogram. In addition, Statistics block 2009 also compares the short-term histogram and the long-term histogram, and based on this comparison either generates an alarm or uses the short-term histogram to update the long-term histogram. The operation of Statistics block 2007 is further detailed in FIG. 18.

[0082] Within the Statistics block 2007, the dISMA signal is used to update the HISLIMA signal, which establishes a reference level of odd harmonic current within the monitored phase. As illustrated, the HISLIMA Calculation block 2023 updates the HISLIMA signal, representing a maximum level of harmonic currents within the monitored phase current, using the following equation:

$$HISLIMA_k = \max(10 \cdot dISMA_k, HISLIMA_{k-1})$$

[0083] Where HISLIMA is limited to a range of $(0.01 - 1.0) \times INOM$, wherein INOM is a system dependent constant. HISLIMA is initialized at $0.01 \times INOM$.

[0084] The incoming dISMA signal is limited to a minimum value of 0 and a maximum value of HISLIMA in Limiter block 2021. Unit Generator block 2025 calculates which counter within the short-term histogram (as illustrated in FIG. 17) will be incremented. The counter to be incremented is determined with the following equation:

$$C_n = \text{ceil}\left(\frac{100 \cdot dISMA_k}{HISIMA_k}\right)$$

[0085] Where C_n represents the number of the counter to be incremented, within the short-term histogram (see FIG. 17). Over a predetermined time period (i.e.; an update window) the short-term histogram is updated in the Short-term Histogram Counter block 2027. At the end of each update window the statistical mean and standard deviation of the short term histogram is calculated in the Short-term Histogram Statistics Calculation block 2029, and compared with the statistical mean and standard deviation of the long term histogram in block 2039. The mean and standard deviation for the short-term histogram are calculated using the following equations:

$$mean_s = \frac{\sum_{n=1}^{100} n \cdot C_{s,n}}{\sum_{n=1}^{100} C_{s,n}}$$

$$std_s = \sqrt{\frac{C_{s,n} \cdot \sum_{n=1}^{100} (n - mean_s)^2}{\sum_{n=1}^{100} C_{s,n}}}$$

[0086] Long-term Histogram Statistics Calculation block 2033 calculates the mean and standard deviation of the long-term histogram, using the same equations as used for the short-term histogram. The statistical quantities of the short-term histogram are then compared with the statistical quantities of the long-term histogram. If both of the inequalities in the following pair of equations are satisfied, a statistically significant difference is present in the monitored phase, and the HA output is asserted.

$$mean_s > mean_L + STDALM1 \cdot std_L$$

$$std_s > STDALM2 \cdot std_L$$

[0087] Where $mean_s$ is the mean of the short-term histogram, $mean_L$ is the mean of the long-term histogram, std_s is the standard deviation of the short-term histogram, and std_L is the standard deviation of the long-term histogram, and STDALM1 and STDALM2 are calibration constants. The HA signal can give

early notification of an impending fault, but is not actually used to alert of a fault. That function is performed by the Decision Logic block 2011, described below.

[0088] If a statistically significant difference is not detected, the contents of the short-term histogram are used to update the long-term histogram, thereby ensuring that moderate changes in odd harmonic current within the monitored phase will not lead to a false HIF detection. Update block 2035 updates the long-term histogram is updated in accordance with the following equation:

$$C_{L,n,k} = (1 - \alpha) \cdot C_{S,n,k} + \alpha \cdot C_{L,n,k-1}$$

[0089] Where the subscript L refers to a counter value of the long-term histogram, the subscript S refers to a counter within the short-term histogram, the subscript n refers to a specific counter, and the subscript k refers to the present processing interval, while k-1 refers to the previous processing interval. α relates to a histogram updating time constant in the equation as defined earlier. However, while the HA output is asserted and for a predetermined time period thereafter, update of the long-term histogram is disabled by Delay block 2037.

[0090] The Decision Logic block 2011 is further detailed in FIG. 19. Comparator 2061 compares signal dISMA against a threshold derived using the following equation:

$$dISMFPUA = \frac{HISLIMA \cdot \min(mean_L + STDFPU \cdot std_L, max_L)}{100}$$

[0091] Where the maximum value in the long-term histogram, max_L , corresponds to the highest number of the counter that contains a nonzero count value.

[0092] If the comparator 2061 indicates that a particular sample of dISMA has exceeded the above threshold, a counter is incremented within the NFA Count / Comparison block 2063. The NFA Count / Comparison block 2063 accumulates an event count for a predetermined period. The event count is compared against a threshold generated using the following equations:

$$MINCNT = \text{floor}\left(\frac{100 \cdot dISMFUPA}{HISLIMA}\right)$$

$$NFA = \frac{HISWIN \cdot \sum_{n=MINCNT}^{100} c_{L,n}}{\sum_{n=1}^{100} C_{L,n}}$$

[0093] If the event count exceeds NFA, a HIF is present on the monitored phase, and the HIF output is asserted.

[0094] While the above description of the embodiment of FIG. 16 has for simplicity discussed the monitoring of its use within a monitoring a single-phase current, additional security can be added by utilizing the characteristics of a 3-phase system. For instance, harmonic activity on all phases will occur during capacitor bank switching. Even though such activity may show increased odd harmonic levels much like a HIF on one or more phases, the Decision Logic block 2011 accounts for this by comparing odd harmonic current across the phases, and disabling the HIF output when increased odd harmonic currents are detected in all three phases.

[0095] The Decision Logic block 2011 accomplishes this through the use of an additional 3-phase threshold, defined by the following equation:

$$dISM3PUA = \frac{HISLIMA \cdot \min(\text{mean}_L + STD3PU \cdot \text{std}_L, \text{max}_L)}{100}$$

[0096] This equation is very similar to the equation used to calculate dISMFPU, except that the constant STD3PU is used instead of the constant STDFPU. Generally, the constant STD3PU will be somewhat smaller than the constant STDFPU. Comparator 2065 will register when dISMA exceeds dISM3PU, and if dISMA exceeds dISM3PU for a predetermined time period pick-up timer 2067 will assert its output. The output of timer 2067 is ANDED with similar signals from other phases by AND gate 2069, and if all three phases detect higher than normal levels of odd harmonics – as determined by comparison with dISM3PU – timer 2071 will disable NFA Count / Comparison block 2063 from registering a HIF for a predetermined time.

[0097] The embodiment discussed in FIG. 16 relies on the establishment of a steady reference from the IIR Limiting Averager block 2005. For this purpose, the IIR Limiting Averager block 2005 could average the first one second worth of samples and output that as ISMAREF, and use the equations detailed above to modify ISMAREF after "steady state" operation was achieved. In addition, the long-term histogram must be established before reliable HIF detection can be achieved using the embodiment of FIG. 16. One way to accomplish this would be to monitor a particular phase for a period of time to establish the histogram before running the disclosed HIF algorithm. For instance, the long-term histogram could be built up for one day prior to enabling the fault detection algorithm to execute.

[0098] While particular embodiments of the invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made therein without departing from the invention in its broader aspects.

CLAIMS

[C1] 1. A system for detecting a high impedance fault in a multi-grounded electrical power distribution system comprising:

- i) a current acquisition circuit, said current acquisition circuit generating a digital signal reflecting a current present in said multi-grounded electrical power distribution system; and
- ii) a processor coupled to said current acquisition circuit for executing a high-impedance fault detection algorithm and generating a high-impedance fault signal indicating the absence or presence of a high-impedance fault in said multi-grounded electrical power distribution system, wherein

the processor (a) generates an odd harmonic signal from said digital signal, (b) conditions said odd harmonic signal, (c) generates a first histogram using said conditioned odd harmonic signal, (d) calculates a plurality of statistical quantities from said first histogram, (e) generates a threshold at least partially from said statistical quantities, (f) compares said conditioned odd harmonic signal to said threshold, and (g) generates said high-impedance fault signal depending on said comparison.

[C2] 2. The system of claim 1, wherein the processor generates said odd harmonic signal using a finite impulse response filter.

[C3] 3. The system of claim 2, wherein said finite impulse response filter further comprises a mathematical combination of:

- i) a half-cycle differentiator operating on said digital signal and generating a differentiated signal;
- ii) a full-cycle fundamental component filter, operating on said digital signal and generating a filtered signal;
- iii) a phase adjustor operating on said filtered signal and generating a phase adjusted filtered signal; and

- iv) a subtractor, subtracting said phase adjusted filtered signal from said differentiated signal, and outputting an odd harmonic signal.

[C4] 4. The system of claim 1, wherein the processor conditions said digital signal by generating an absolute value signal from said digital signal and summing said absolute value signal over a predetermined time period, thereby generating a summed absolute value signal.

[C5] 5. The system of claim 4, wherein the processor further conditions said digital signal by (a) applying a first filter to said digital signal, thereby generating a first filtered signal, (b) applying a second filter to said digital signal, thereby generating a second filtered signal, and (c) generating a difference signal by subtracting the second filtered signal from the first filtered signal.

[C6] 6. The system of claim 5, wherein the first filter operates by taking an average of a most recent N samples of said summed absolute value signal and the second filter operates by taking a weighted average of a present sample of said summed absolute value signal and a previous sample of said second filtered signal.

[C7] 7. The system of claim 6, wherein the second filter limits the second filter input signal based on a ratio of said present sample and said previous sample.

[C8] 8. The system of claim 1, wherein the processor further generates a second histogram, and wherein said processor updates said first histogram using said second histogram.

[C9] 9. The system of claim 8, said second histogram is gathered over a shorter time period than said first histogram.

[C10] 10. The intelligent electronic device of claim 9, wherein the processor generates said first histogram using a predetermined number of a first sequence of samples representing said conditioned odd harmonic signal.

[C11] 11. The intelligent electronic device of claim 10, wherein said processor further calculates a plurality of statistical quantities from said second histogram, and wherein said second histogram will not be used to update said

first histogram if said plurality of statistical quantities calculated from said second histogram sufficiently differ from said plurality of statistical quantities calculated from said first histogram.

[C12] 12. A method for detecting a high impedance fault within a multi-grounded power distribution system comprising the steps of:

- i) measuring a current, thereby generating a measured current signal;
- ii) generating an odd harmonic current signal from said measured current signal;
- iii) conditioning said odd harmonic signal, thereby generating a conditioned odd harmonic signal;
- iv) generating a first histogram using said conditioned odd harmonic signal;
- v) calculating a plurality of statistical quantities from said first histogram;
- vi) generating a threshold at least partially from said statistical quantities;
- vii) comparing said conditioned odd harmonic signal with said threshold; and
- viii) generating a high-impedance fault signal based on the results of said comparing step.

[C13] 13. The method of claim 12 wherein said odd harmonic signal is generated by applying an FIR filter to said measured current signal.

[C14] 14. The method of claim 12, wherein said odd harmonic signal is generated by the following steps:

- i) differentiating said measured current signal over a half-cycle, thereby generating a differentiated signal;
- ii) filtering said measured current signal, thereby generating a filtered signal;
- iii) phase adjusting said filtered signal, thereby generating a phase adjusted filtered signal; and

iv) subtracting said phase adjusted filtered signal from said differentiated signal, thereby generating an odd harmonic signal.

[C15] 15. The method of claim 12, wherein said conditioned odd harmonic signal is generated by taking an absolute value of said odd harmonic signal, thereby generating an absolute value signal, and summing said absolute value signal over a predetermined time period, thereby generating a summed absolute value signal.

[C16] 16. The method of claim 15, wherein said summed absolute value signal is filtered by a first filter, thereby generating a first filtered signal, and filtered by a second filter, thereby generating a second filtered signal, and subtracting said second filtered signal from said first filtered signal, thereby generating a difference signal.

[C17] 17. The method of claim 16, wherein said first filter averages a most recent N samples of said summed absolute value signal and wherein said second filter takes a weighted average of a present sample of said summed absolute value signal and a previous sample of said second filtered signal.

[C18] 18. The method of claim 17, wherein said second filter limits the second filter input signal based on a ratio of said present sample and said previous sample.

[C19] 19. The method of claim 12, further comprising the step of:
i) generating a second histogram; and
ii) updating said first histogram using said second histogram.

[C20] 20. The method of claim 19, wherein said second histogram is gathered over a shorter time period than said first histogram.

[C21] 21. The method of claim 20, wherein said first histogram is generated using a predetermined number of a first sequence of samples representing said conditioned odd harmonic signal.

[C22] 22. The method of claim 21, further comprising the step of calculating a plurality of statistical quantities from said second histogram, and wherein said second histogram will not be used to update said first histogram if said plurality

of statistical quantities calculated from said second histogram differ sufficiently from said plurality of statistical quantities calculated from said first histogram.

[C23] 23. A system for detecting a high impedance fault within a multi-grounded power distribution system comprising:

- i) means for measuring a current, thereby generating a measured current signal;
- ii) means for generating an odd harmonic signal from said measured current signal;
- iii) means for conditioning said odd harmonic signal, thereby generating a conditioned odd harmonic signal;
- iv) means for generating a first histogram using said conditioned odd harmonic signal;
- v) means for generating a second histogram over a predetermined time period using said conditioned odd harmonic signal; and
- vi) means for comparing said first histogram and said second histogram and generating a high impedance fault signal if there is a sufficient statistical difference between said first histogram and said second histogram.

[C24] 24. A circuit accepting a digital input signal and outputting a digital signal consisting substantially of odd harmonics of said digital input signal, the circuit comprising a processor including instructions for a digital filter.

[C25] 25. The circuit of claim 24, wherein said digital filter is a finite impulse response filter.

[C26] 26. A finite impulse response filter circuit accepting a digital input signal and outputting a digital output signal consisting substantially of odd harmonics of said digital input signal, the circuit comprising a mathematical combination of:

- i) a half-cycle differentiator operating on said digital input signal and generating a differentiated signal;
- ii) a full cycle cosine filter, operating on said digital input signal and generating a filtered signal;

- iii) a phase adjustor operating on said filtered signal and generating a phase adjusted filtered signal; and
- iv) a subtractor, subtracting said phase adjusted filtered signal from said differentiated signal, and outputting an odd harmonic signal.

[C27] 27. A method of generating a digital output signal consisting substantially of odd harmonics of a digital input signal, the method comprising the steps of:

- i) differentiating said digital input signal over a half-cycle, thereby generating a differentiated signal;
- ii) filtering said digital input signal, thereby generating a filtered signal;
- iii) phase adjusting said filtered signal, thereby generating a phase adjusted filtered signal; and
- iv) subtracting said phase adjusted filtered signal from said differentiated signal, thereby generating an odd harmonic signal.

[C28] 28. A method operating within a processor for detecting the occurrence of an event within at least one digital signal comprising the steps of:

- i) conditioning said digital signal, thereby generating a conditioned digital signal;
- ii) establishing a long-term statistical reference of said conditioned signal;
- iii) establishing a short-term statistically derived signal from said conditioned signal;
- iv) comparing said long-term statistical reference and said short-term statistically derived signal; and
- v) generating an event if there is a statistically significant difference between said long-term statistical reference and said short-term statistically derived signal.

[C29] 29. A method for disabling a high impedance fault detector within a three-phase multi-grounded power distribution system including three phase currents, the method comprising the steps of:

- i) measuring said three phase currents, thereby generating three measured current signals;
- ii) processing each of said three measured current signal, thereby generating three odd harmonic current signals;
- iii) conditioning each of said odd harmonic signals, thereby generating three conditioned odd harmonic signals;
- iv) statistically processing each of said conditioned odd harmonic signals, thereby calculating three histograms;
- v) processing each histogram, thereby calculating three pluralities of statistical quantities;
- vi) processing each plurality of statistical quantities, thereby generating three thresholds;
- vii) comparing each of said conditioned odd harmonic signal with a corresponding threshold selected from said three thresholds; and
- viii) disabling said high-impedance fault detector based on the results of said comparing step.

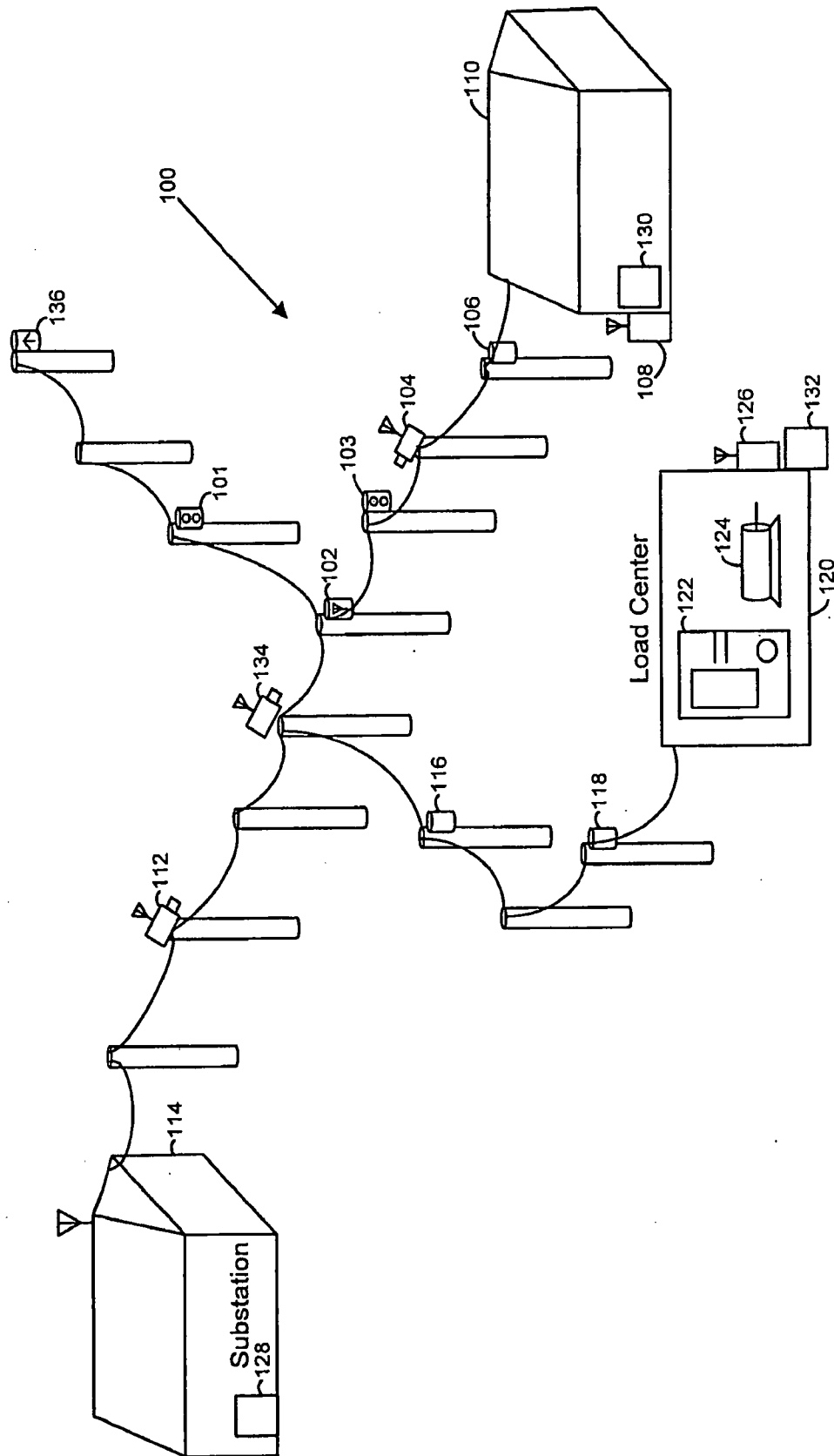
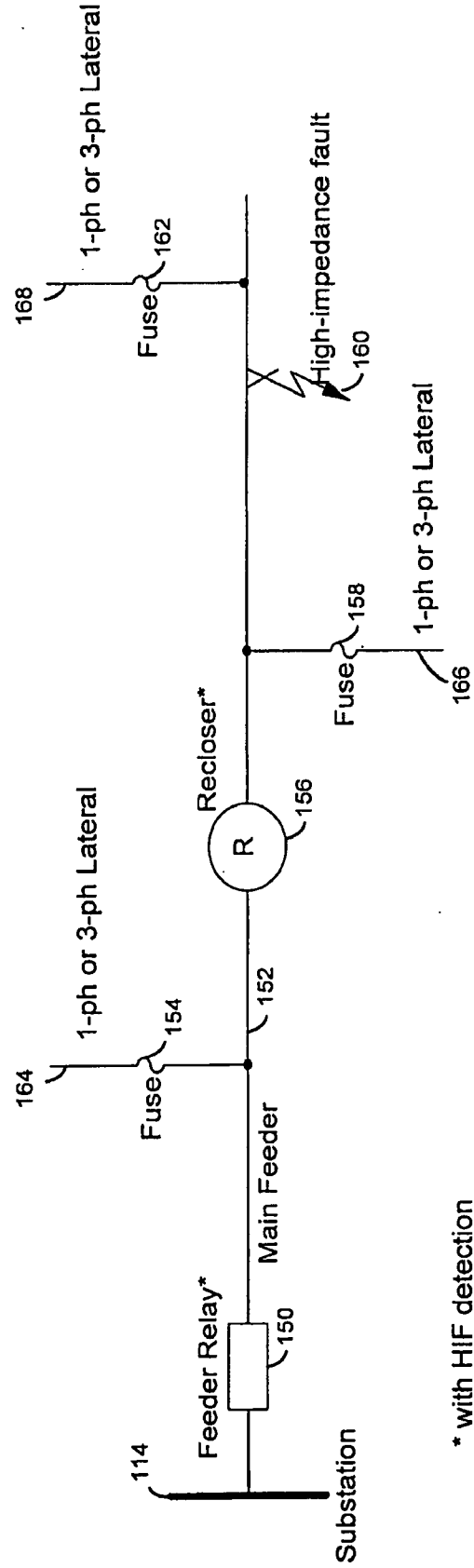


FIG. 1A



* with HIF detection

FIG. 1B

200

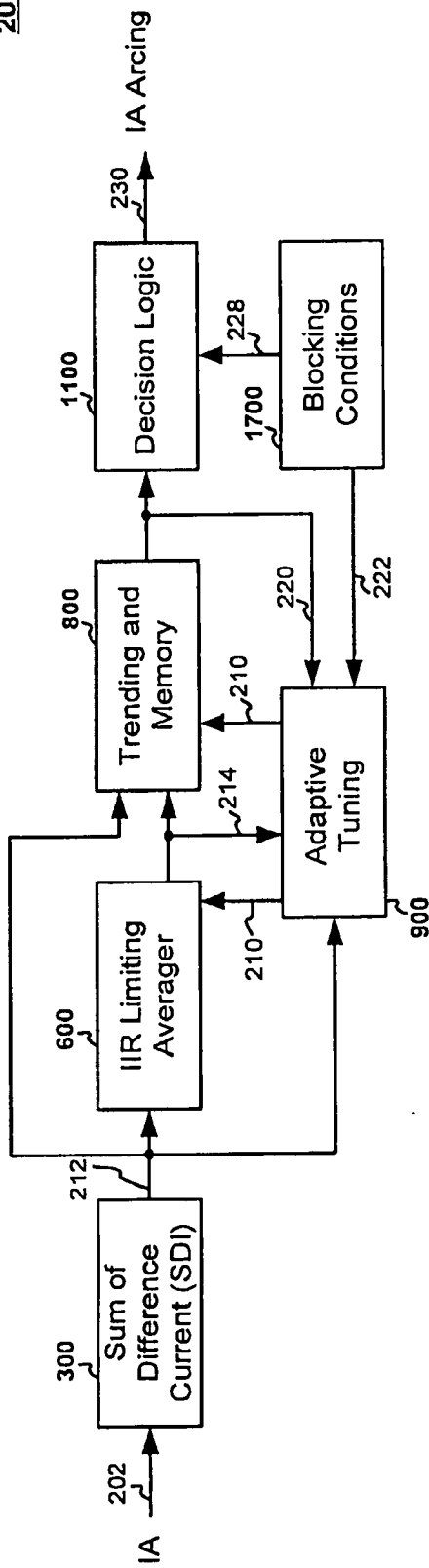


Fig. 2

300

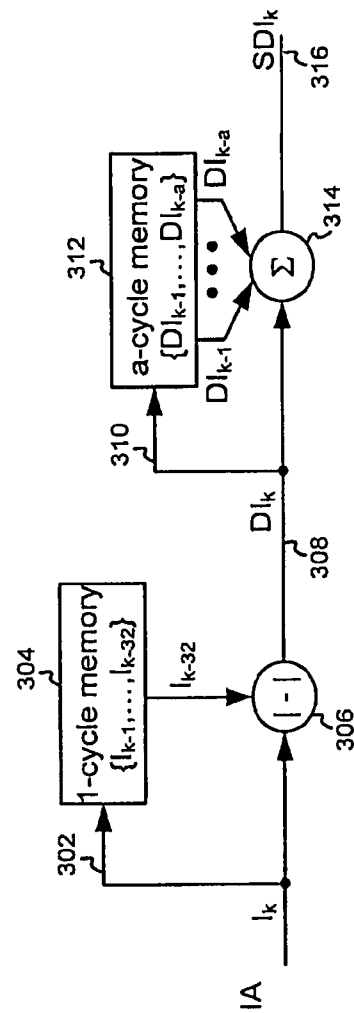


Fig. 3

400

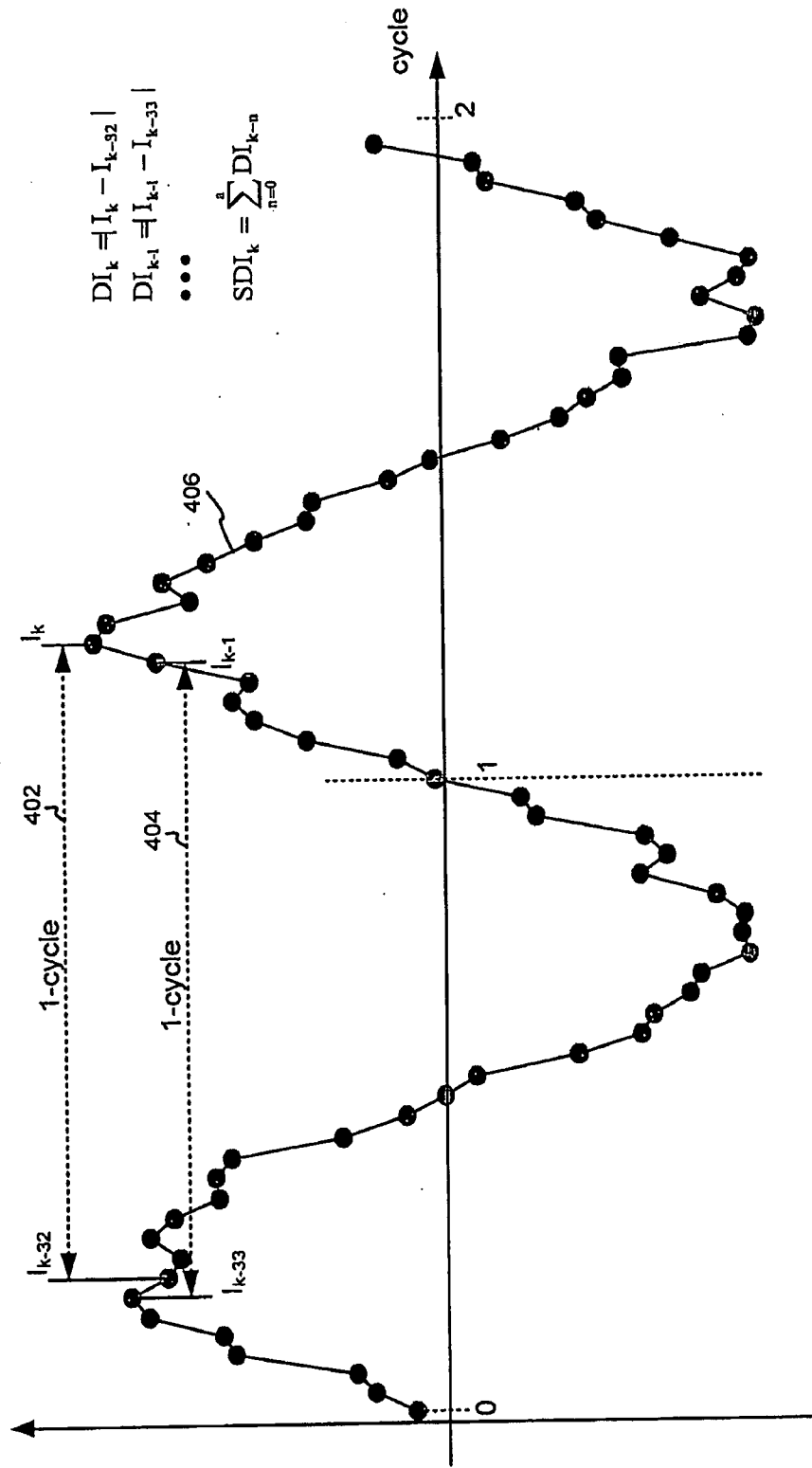


Fig. 4

600

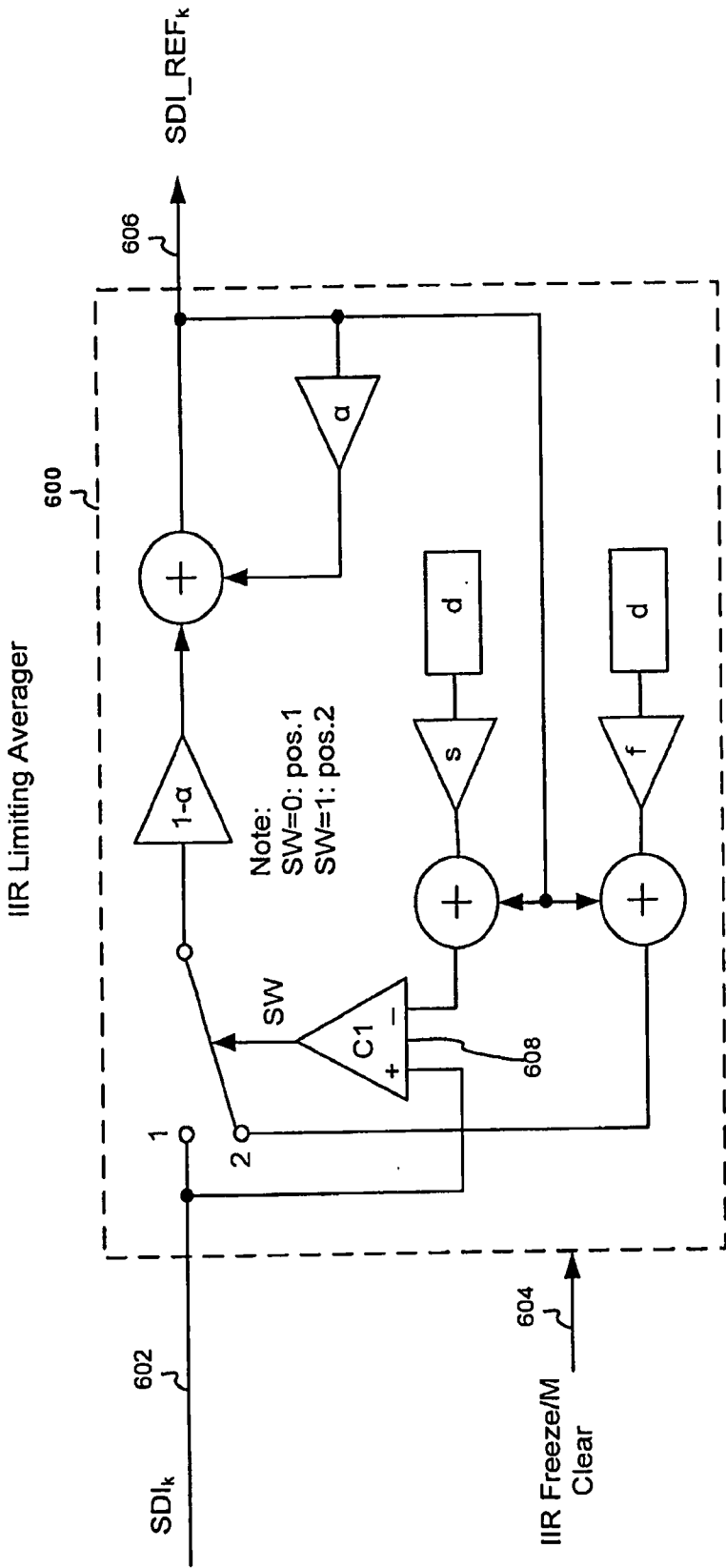


Fig. 5

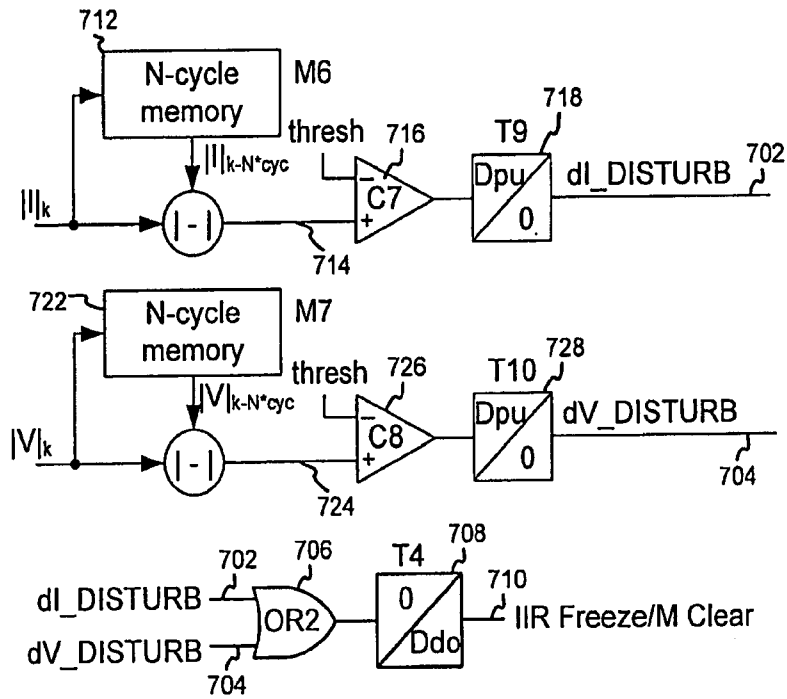


Fig. 6

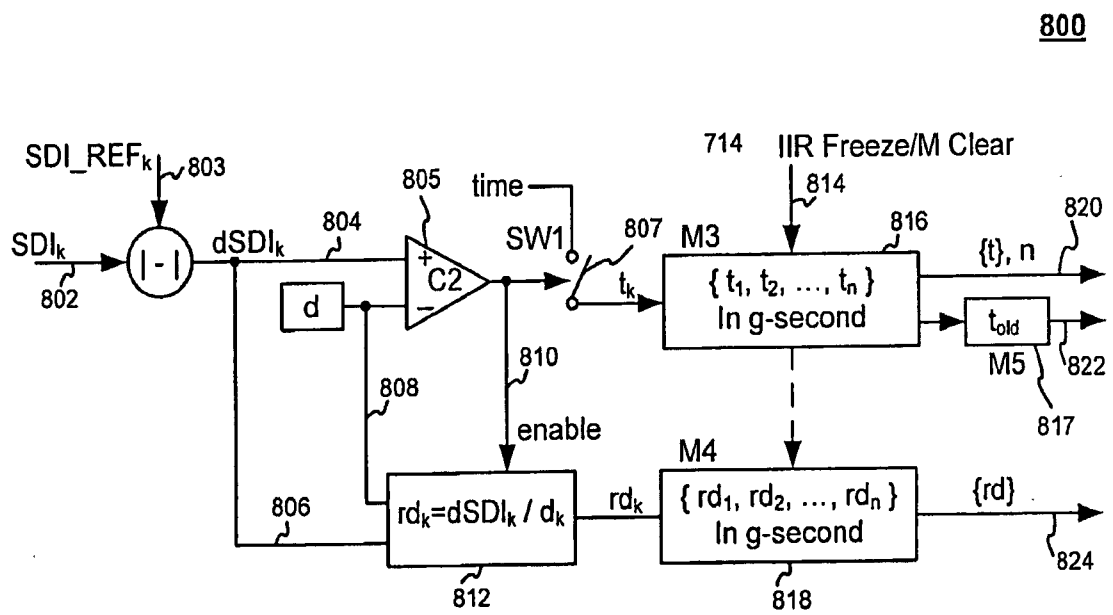
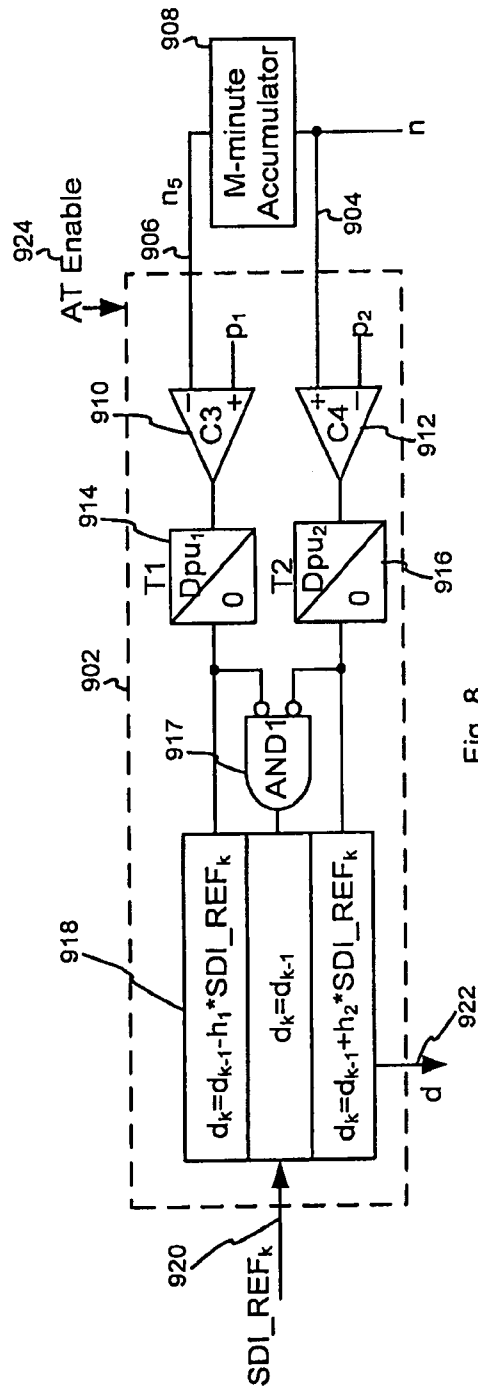
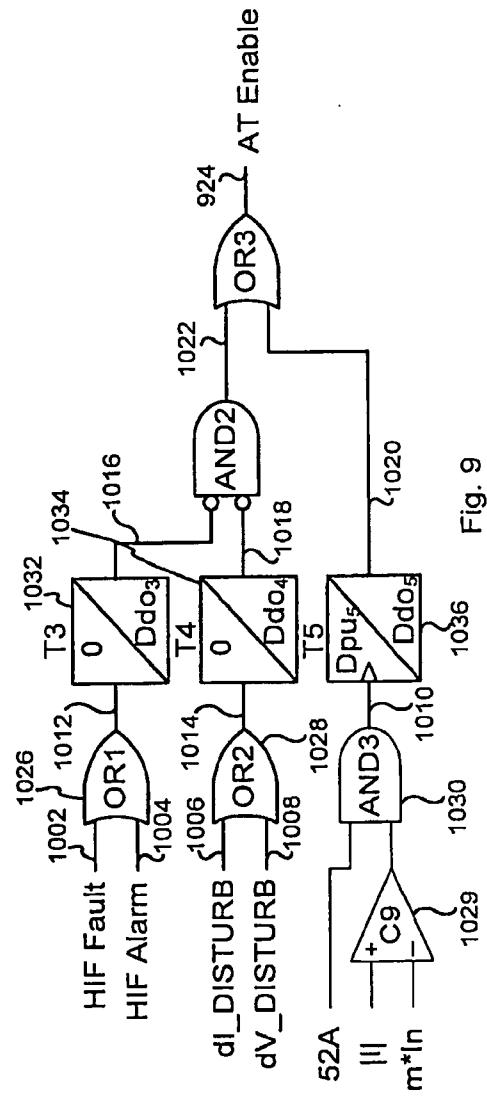


Fig 7

900



1000



1100

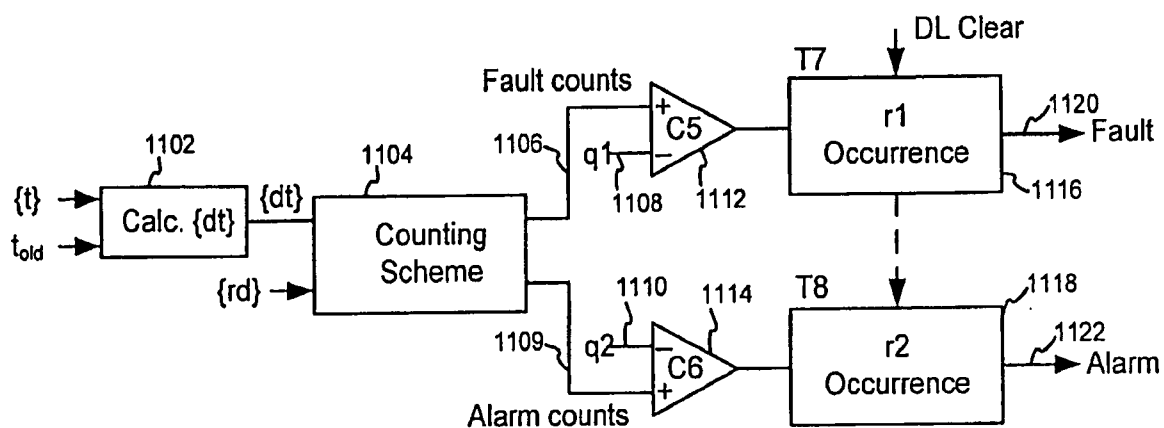


Fig. 10

1200

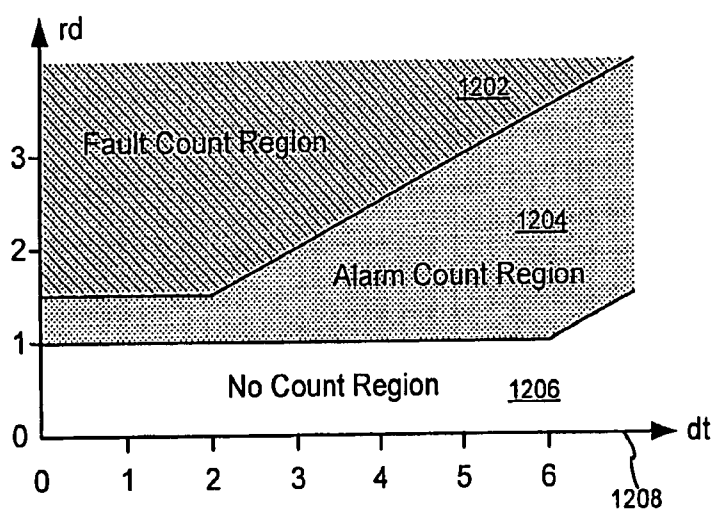


Fig. 11

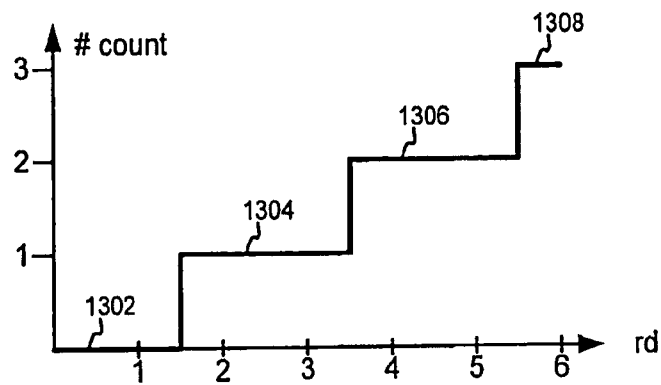
1300

Fig. 12

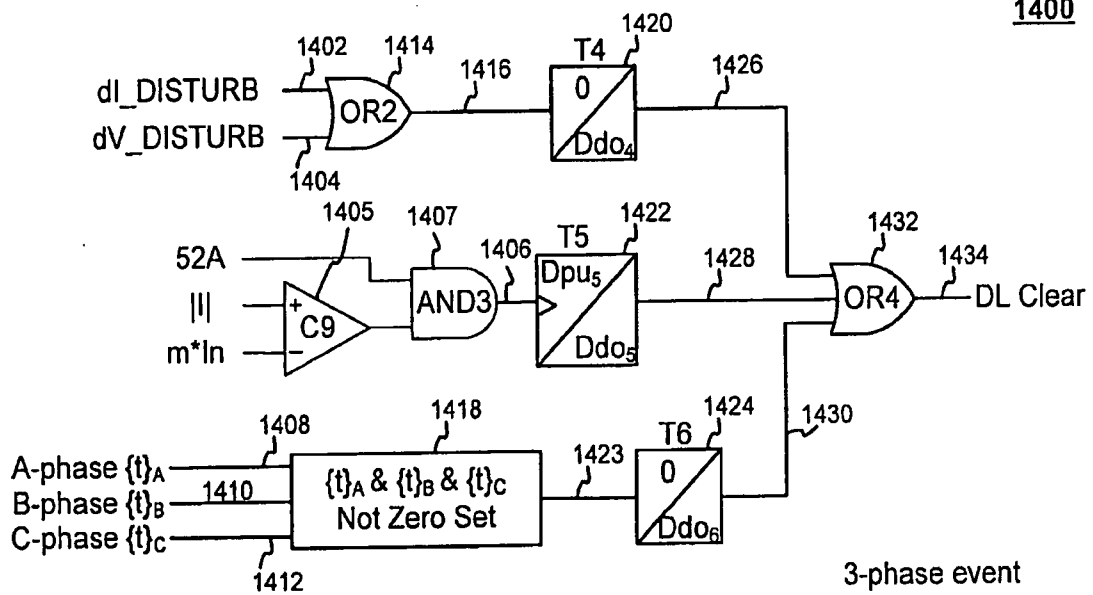
1400

Fig. 13

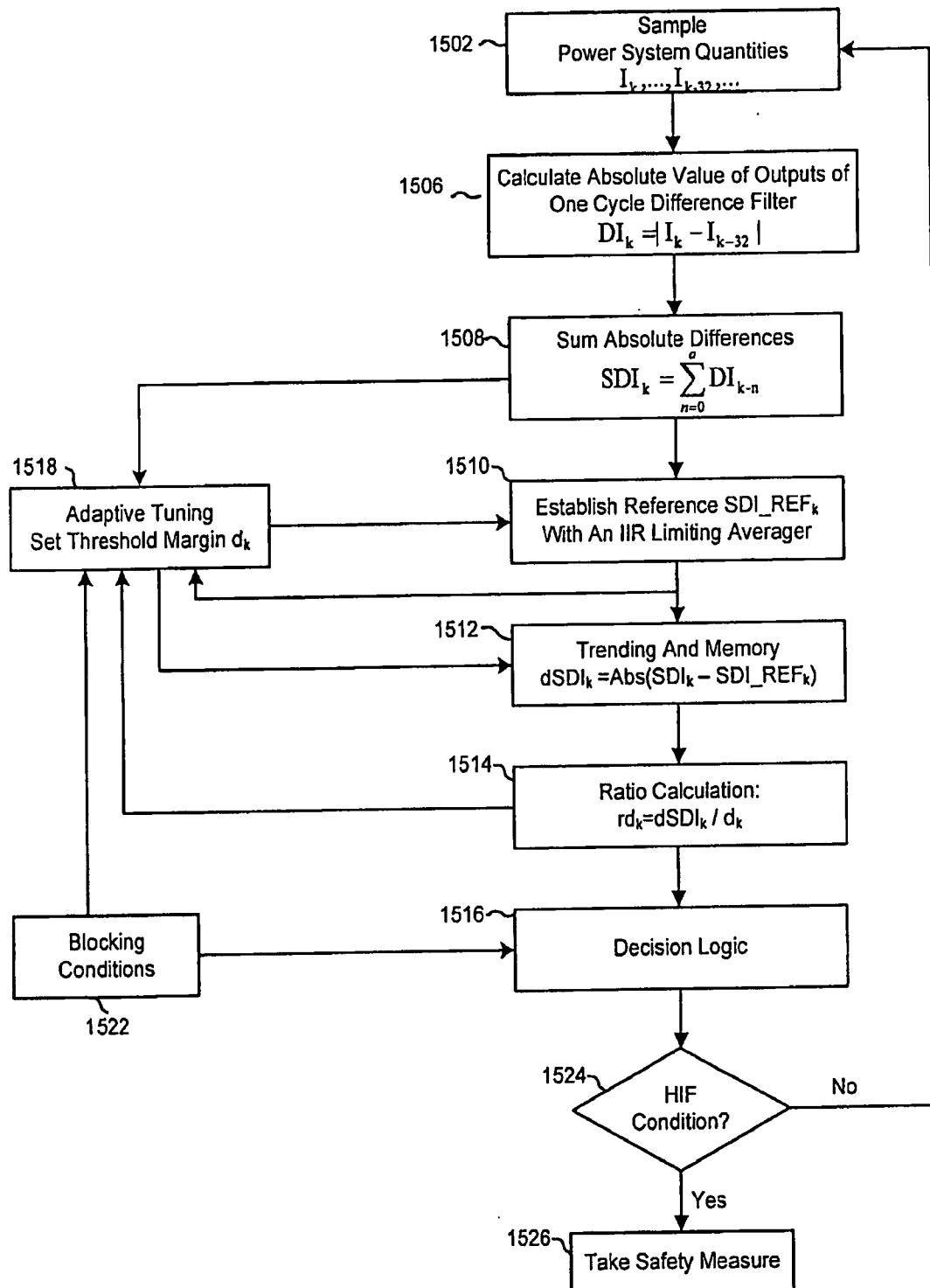
1500

FIG. 14

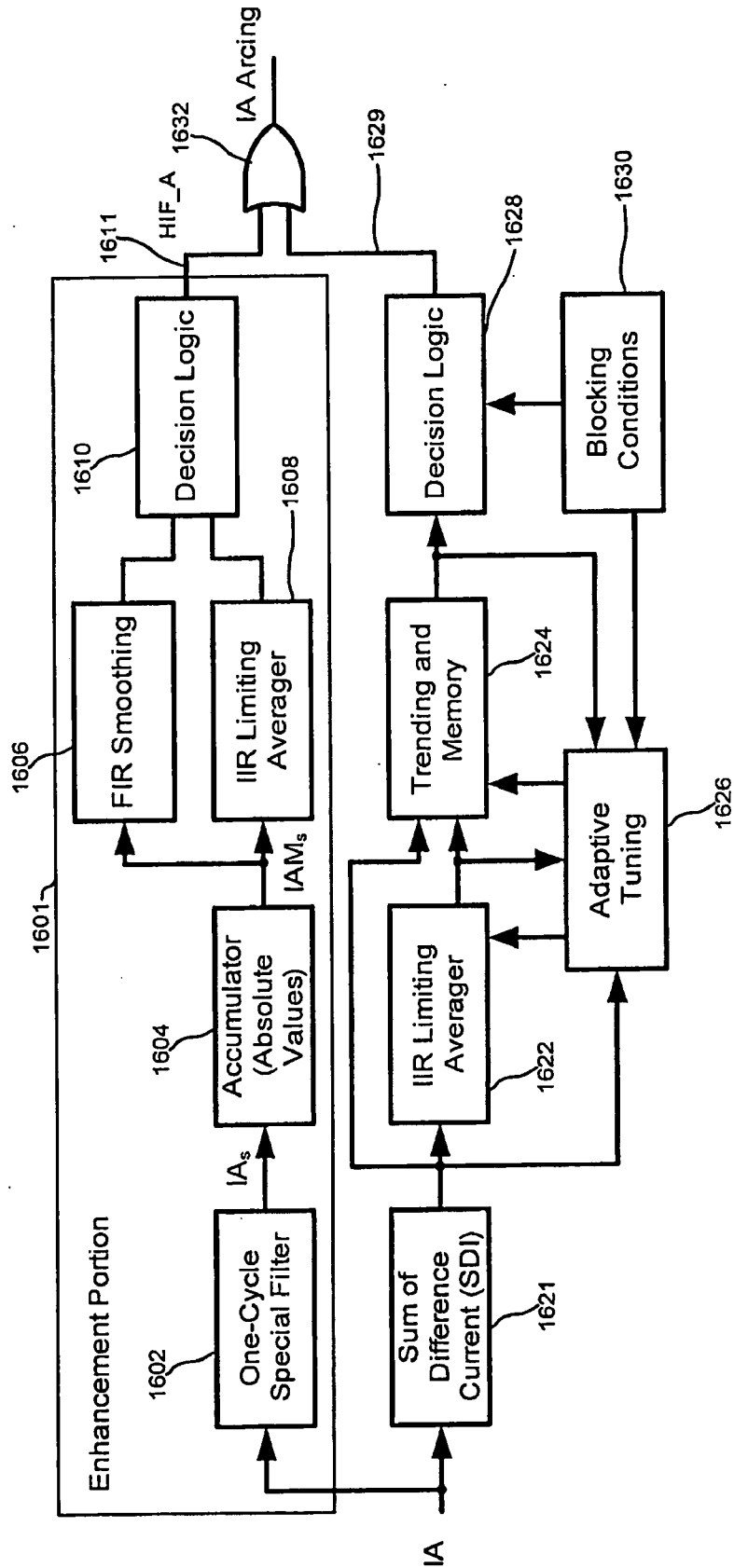
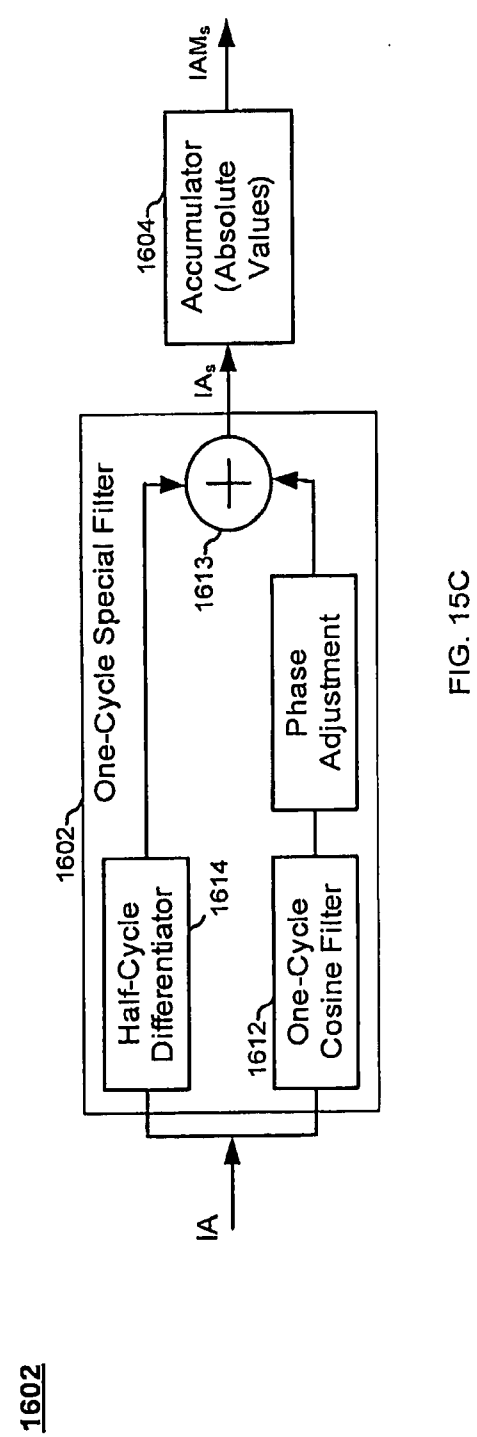
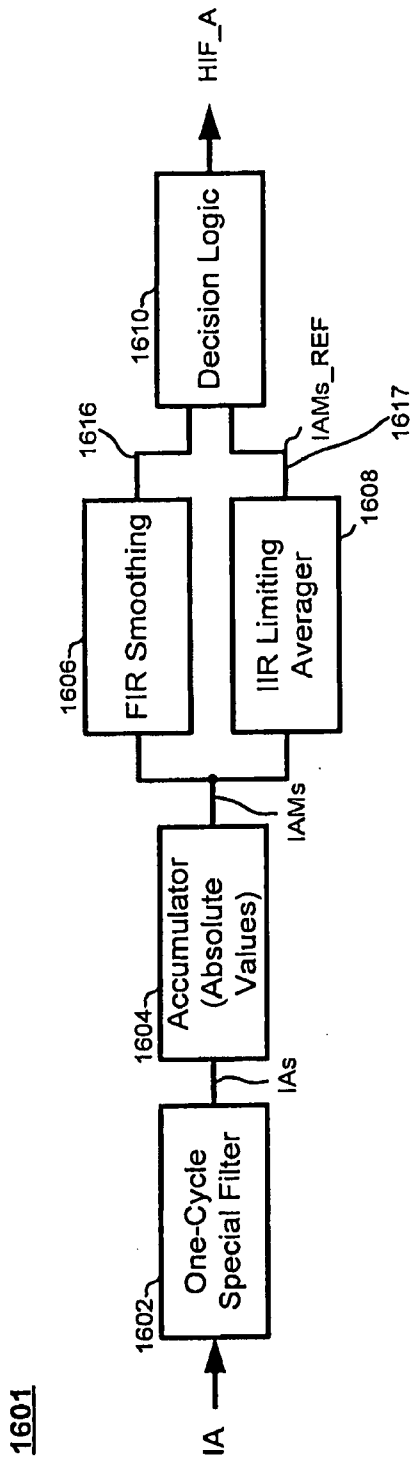
1600

FIG. 15A



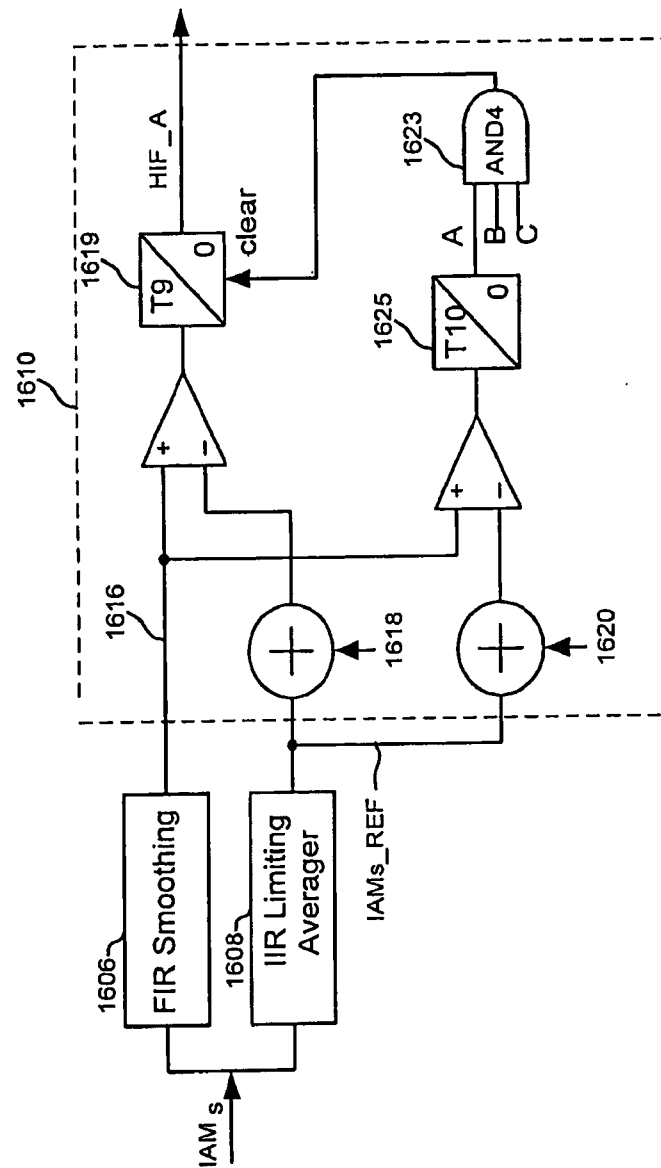


FIG. 15D

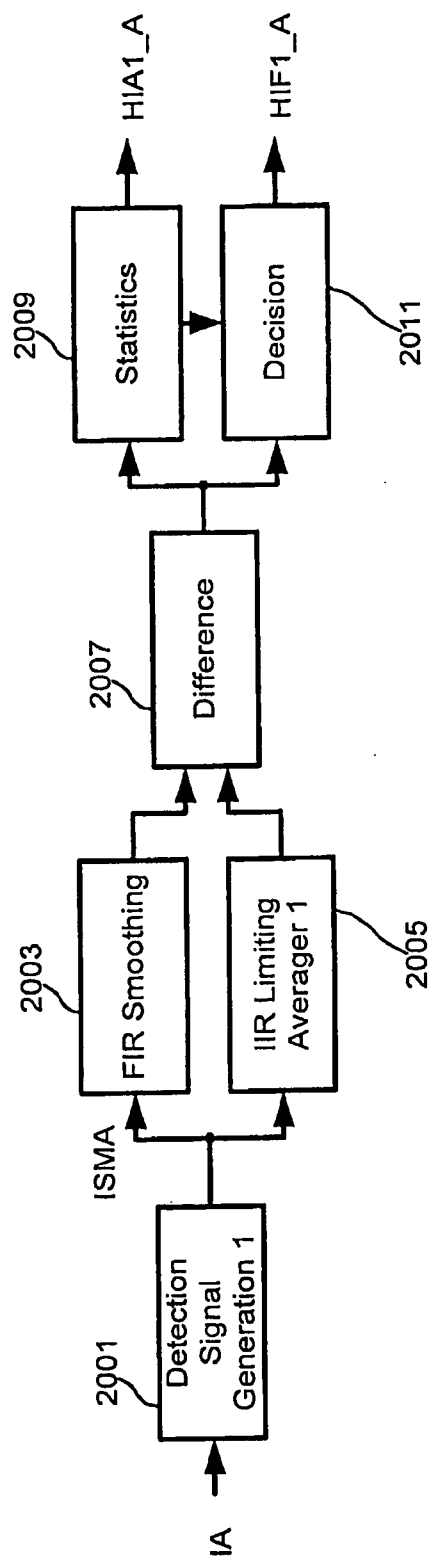


FIG. 16

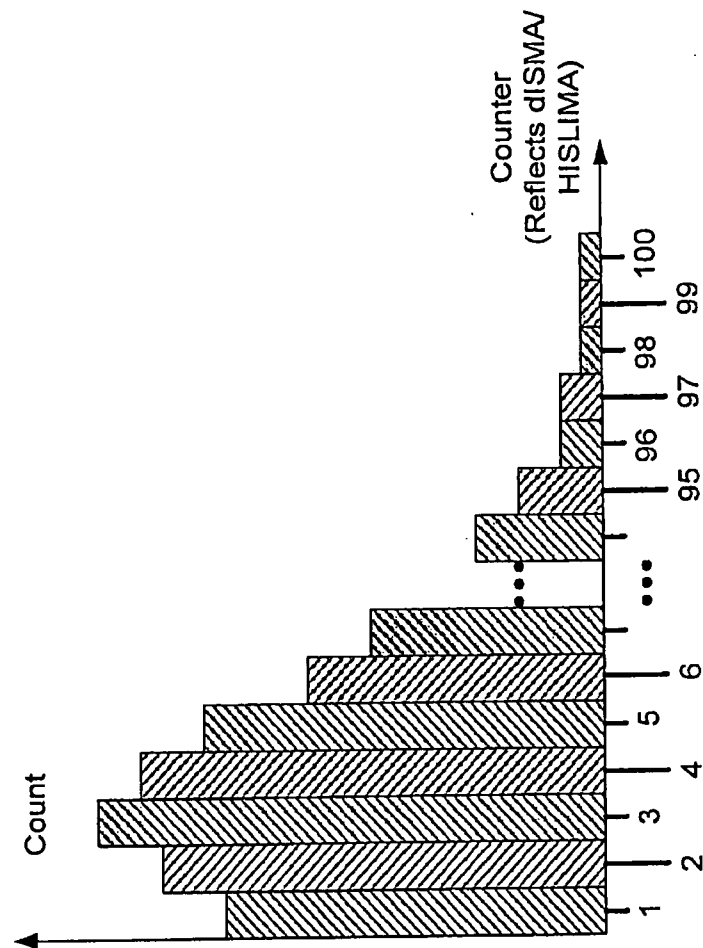


FIG. 17

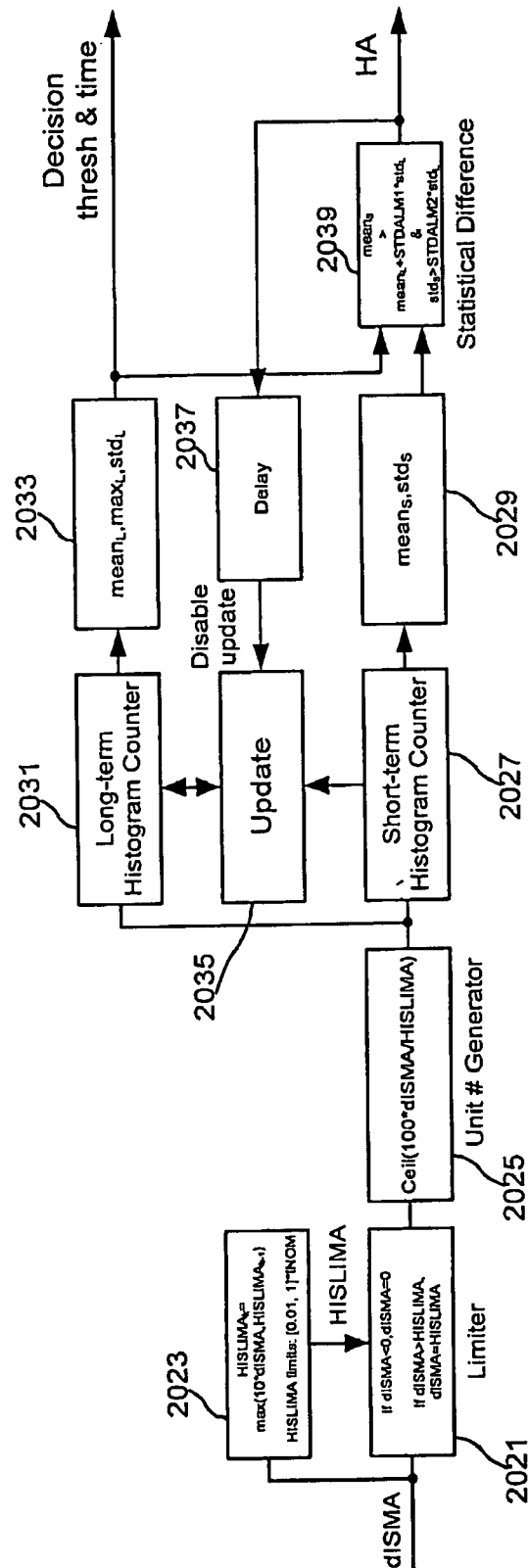


FIG. 18

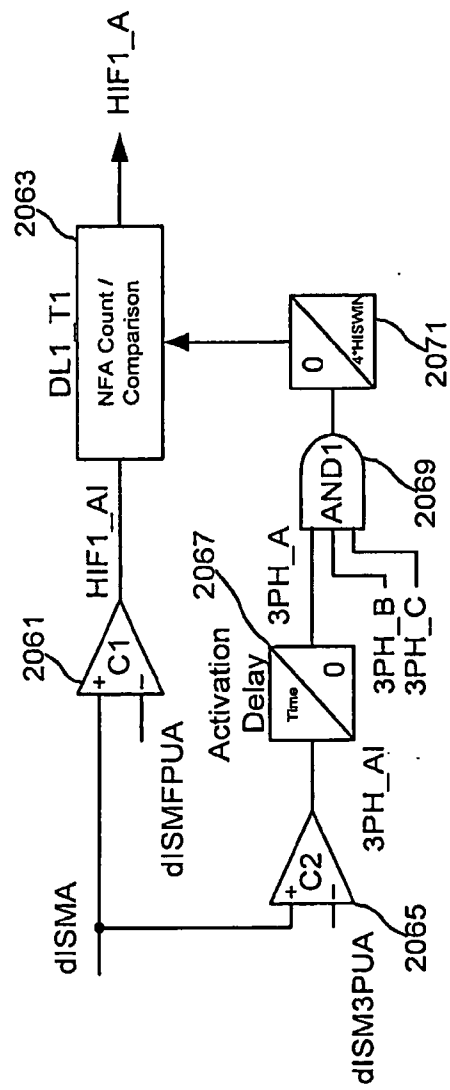


FIG. 19