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(71) Applicant (for all designated States except US): **INTERNATIONAL RECTIFIER CORPORATION** [US/US];
233 Kansas Street, El Segundo, California 90245 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **HERMAN, Thomas** [US/US]; 3113 Palm Avenue, Manhattan Beach, California 90266 (US).

(74) Agents: **SALEHI, Kourosh** et al.; Ostrolenk, Faber, Gerb & Soffen, LLP, 1180 Avenue of the Americas, New York, New York 10036 (US).

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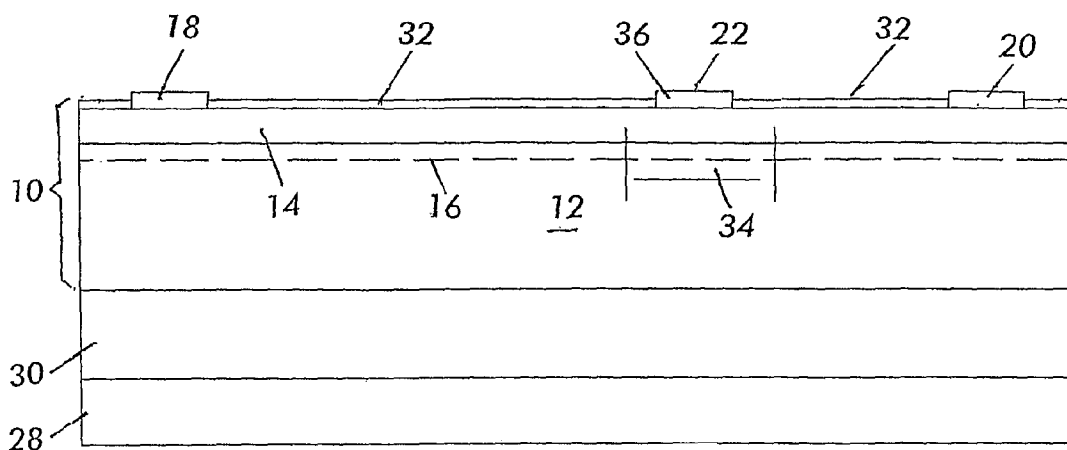
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(54) Title: **III-NITRIDE POWER SEMICONDUCTOR DEVICE**



(57) Abstract: A III-nitride power semiconductor device that includes a two dimensional electron gas having a reduced charge region under the gate thereof.

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AMENDED CLAIMS**received by the International Bureau on 01 April 2008 (01.04.2008)**

1. A power semiconductor device, comprising:
 - a III-nitride heterojunction body that includes a first III-nitride body and a second III-nitride body having a different band gap than that of said first III-nitride body;
 - a first power electrode coupled to said second III-nitride body;
 - a second power electrode coupled to said second III-nitride body;
 - a gate arrangement disposed between said first and said second power electrodes; and
 - a conductive channel that includes a two-dimensional electron gas that in a conductive state includes a reduced charge region under said gate arrangement that is less conductive than its adjacent regions, at least twice as wide as said gate arrangement, and extends beyond at least one edge of said gate arrangement.
2. The power semiconductor device of claim 1, wherein said gate arrangement includes a gate insulation body.
3. The power semiconductor device of claim 1, wherein said gate arrangement includes a schottky body.
4. The power semiconductor device of claim 1, wherein said gate arrangement is received in a recess over said reduced charge region.
5. The power semiconductor device of claim 4, wherein said recess is configured to cause said reduced charge region.
6. The power semiconductor device of claim 4, wherein said recess is wider than said gate arrangement.
7. The power semiconductor device of claim 1, further comprising at least one implanted region in said second III-nitride body under said gate arrangement configured to cause said reduced charge region.

8. The power semiconductor device of claim 1, wherein said gate arrangement does not include a field plate.

9. The power semiconductor device of claim 1, further comprising a passivation body disposed over said III-nitride heterojunction body.

10. The power semiconductor device of claim 1, wherein said first III-nitride body is comprised of a semiconductor alloy from the InAlGa_N system, and said second III-nitride body is comprised of another alloy from the InAlGa_N system.

11. The semiconductor device of claim 1, wherein said first III-nitride body is comprised of GaN and said second III-nitride body is comprised of AlGa_N.

12. The semiconductor device of claim 1, wherein said heterojunction body is disposed over a substrate.

13. The semiconductor device of claim 12, wherein said substrate is comprised of silicon.

14. The semiconductor device of claim 12, wherein said substrate is comprised of silicon carbide.

15. The semiconductor device of claim 12, wherein said substrate is comprised of sapphire.

16. The semiconductor device of claim 12, wherein said substrate is comprised of a III-nitride material.

17. The semiconductor device of claim 16, wherein said III-nitride material is GaN.

18. The semiconductor device of claim 12, further comprising a transition body disposed between said substrate and said III-nitride heterojunction body.

19. The semiconductor device of claim 18, wherein said transition body is comprised of a III-nitride material.

20. The semiconductor device of claim 19, wherein said transition body is comprised of AlN.

21. A power semiconductor device, comprising:

- a III-nitride heterojunction body that includes a first III-nitride body and a second III-nitride body having a different band gap than that of said first III-nitride body;
- a first power electrode coupled to said second III-nitride body;
- a second power electrode coupled to said second III-nitride body;
- a gate arrangement disposed between said first and said second power electrodes; and
- a conductive channel that includes a two-dimensional electron gas that in a conductive state includes a reduced charge region under said gate arrangement that is less conductive than its adjacent regions, wherein said reduced charge region extends beyond an edge of said gate arrangement toward one of said power electrodes only.

22. A power semiconductor device, comprising:

- a III-nitride heterojunction body that includes a first III-nitride body and a second III-nitride body having a different band gap than that of said first III-nitride body;
- a first power electrode coupled to said second III-nitride body;
- a second power electrode coupled to said second III-nitride body;
- a gate arrangement disposed between said first and said second power electrodes; and
- a conductive channel that includes a two-dimensional electron gas that in a conductive state includes a reduced charge region under said gate arrangement that is less conductive than its adjacent regions, wherein said reduced charge region extends farther toward one power electrode than the other power electrode.

23. A power semiconductor device, comprising:

- a III-nitride heterojunction body that includes a first III-nitride body and a second III-nitride body having a different band gap than that of said first III-nitride body;
- a first power electrode coupled to said second III-nitride body;
- a second power electrode coupled to said second III-nitride body;

a gate arrangement disposed between said first and said second power electrodes; and
a conductive channel that includes a two-dimensional electron gas that in a conductive state includes a reduced charge region under said gate arrangement that is less conductive than its adjacent regions, wherein said reduced charge region is discontinuous.