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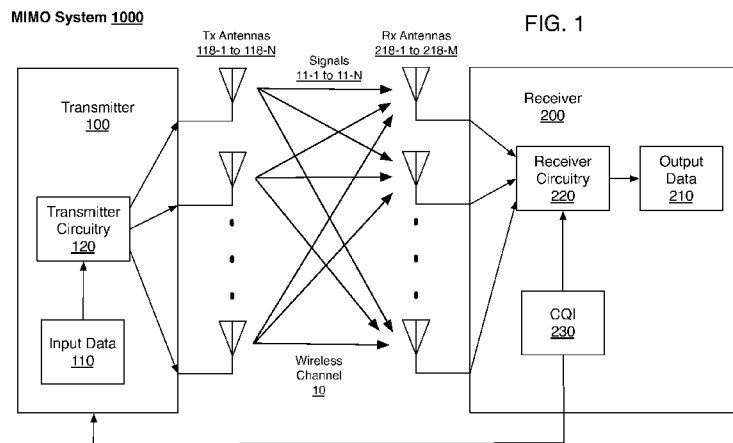
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(57) Abstract: Various embodiments are generally directed to techniques to perform MIMO detection using a dynamic search radius. An apparatus for a wireless receiver includes circuitry, a multiple-input multiple-output (MIMO) detector for execution by the circuitry to determine a plurality of estimated signals, the plurality of estimated signals corresponding to a plurality of signals transmitted through a wireless channel and received by a plurality of antennas, the MIMO detector to determine the plurality of estimated signals based on a search radius, and a search radius tuner for execution by the circuitry to dynamically modify the search radius based on a quality corresponding to the wireless channel.

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CHANNEL-ADAPTIVE CONFIGURABLE MIMO DETECTOR FOR MULTI-MODE WIRELESS SYSTEMS

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Related Applications

This application claims the benefit of United States Provisional Application Serial No. 61/883,626 filed September 27, 2013, entitled "CHANNEL-ADAPTIVE CONFIGURABLE MIMO DETECTOR FOR MULTI-MODE COMMUNICATION," which application is
10 incorporated herein by reference in its entirety.

Technical Field

Embodiments described herein generally relate to multiple-input, multiple-output (MIMO)
15 systems and particularly to MIMO detectors.

Background

Modern wireless systems, such as, for example, mobile broadband systems, may employ
20 multiple-input, multiple-output (MIMO) schemes to increase spectral efficiency and data rates. Various wireless communication standards allow MIMO schemes. For example, 802.11n provides for a 4x4 system (e.g., 4 access point antennas and 4 station antennas.) As another example, 802.11ac provides for an 8x4 system (e.g., 8 access point antennas and 4 station antennas.) Still, as another example, 3GPP LTE Advanced release 10 provides an 8x8 system
25 (e.g., 8 access point antennas and 8 station antennas.)

In general, MIMO schemes provide that a data stream is de-multiplexed into multiple streams (e.g., one for each transmit antenna) transmitted through a channel, and received by a receiver using multiple antennas. For example, a data stream may be de-multiplexed into multiple data streams. Each of these multiple data streams may be modulated using different symbols and then
30 transmitted to the receiver. As will be appreciated, the use of multiple transmit channels allows the MIMO system to increase the data rates achievable in the transmission spectrum. At the receiver, then, these transmitted data streams must be combined and the original signal estimated. MIMO systems include a MIMO detector at the receiver, which combines the transmitted data streams and estimates the original signal.

35 A variety of different techniques and algorithms for MIMO detection have been proposed. Some of the proposed techniques and algorithms provide a minimum bit error rate (e.g., Maximum Likelihood (ML) detection, Sphere Decoder (SD) detection, or the like.) However, these techniques are computationally expensive to implement and are often impractical as the number

of antennas increases. For example, ML detection complexity grows exponentially as the number of antennas grows. As such, ML detection is impractical for larger MIMO systems. SD detection has prohibitively large area and power requirements necessary for implementation. Furthermore, SD detection may not reach an optimal solution within necessary time constraints. Furthermore, while a particular MIMO detection algorithm may be suitable for transmission channels having high signal to noise ratio (SNR), the particular MIMO detection algorithms may not be suitable for transmission channels having a low SNR. Likewise, MIMO detection algorithms suitable for transmission channels having a low SNR may not be suitable for transmission channels having a high SNR.

Thus, there is a need for a MIMO detector that can support multiple standards (e.g., provide for large numbers of transmit and receive antennas) without necessitating impractical area and power requirements to implement. Additionally, there is a need for a MIMO detector that is suitable for high SNR transmission channels as well as low SNR transmission channels. Furthermore, there is a need for a MIMO detector that balances energy efficiency with bit error rate.

Brief Description of the Drawings

FIG. 1 illustrates an example of a MIMO system according to an embodiment.

FIG. 2 illustrates a portion of the MIMO system according to an embodiment.

FIG. 3 illustrates an example MIMO detector according to an embodiment.

FIG. 4 illustrates a portion of the MIMO detector according to an embodiment.

FIG. 5 illustrates a timing diagram showing time interleaving during MIMO detection according to an embodiment.

FIG. 6 illustrates an example of a logic flow for MIMO detection according to an embodiment.

FIG. 7 illustrates an embodiment of a storage medium.

FIG. 8 illustrates a device according to an embodiment.

Detailed Description

Examples are generally directed to multiple-input, multiple output (MIMO) detectors for use in MIMO systems. These MIMO detectors may be included with or implemented by receivers in

communication components (e.g., access points, mobile devices, cells, or the like) that may be configured to operate in accordance with various wireless network standards. These wireless network standards may include standards promulgated by the Institute of Electrical Engineers (IEEE). These wireless network standards may include Ethernet wireless standards (including progenies and variants) associated with the IEEE 802.11-2012. For example, some examples may be implemented for operation with the 802.11n and/or the 802.11ac Standards.

Additionally, these wireless network standards may include standards promulgated by 3rd Generation Partnership Project (3GPP). These wireless network standards may include Ethernet wireless standards (including progenies and variants) associated with the 3GPP LTE Standard.

For example, some examples may be implemented for operation with the 3GPP LTE-Advanced release 10 Standard.

According to some examples, a MIMO detector that is adaptive to varying channel conditions may be provided in a MIMO receiver. The MIMO receiver may determine a plurality of estimated signals based on a search radius, where the search radius is dynamically adjustable based on channel conditions. For example, the MIMO detector may be configured to apply a K-best sphere decoding (SD) process where K is varied based on channel conditions to provide a balance between energy efficiency (e.g., power consumption of the MIMO decoder) and bit error rate (BER). For example, the value of K may be dynamically adjusted based on a channel quality index, desired bit error rate (BER) targets, and/or a signal-to-noise (SNR) ratio of the channel.

FIG. 1 is a block diagram illustrating an example MIMO system 1000. In some examples, as shown in FIG. 1, the MIMO system 1000 includes a MIMO transmitter 100 and a MIMO receiver 200. As can be seen, the MIMO transmitter 100 and the MIMO receiver 200 each include a number of antennas. For example, the MIMO transmitter 100 includes transmit (Tx) antennas 118-1 to 118-N while the MIMO receiver 200 includes receive (Rx) antennas 218-1 to 218-M. The transmitter 100 is configured to transmit signals 11-1 to 11-N to the receiver 200 using the wireless channel 10.

It is to be appreciated, that the number of Tx antennas 118 and Rx antennas 218 may vary depending upon the implementation and/or the standard with which the system 1000 is designed to operate. Additionally, in some examples, the number of Tx antennas 118 may be the same as the number of Rx antennas 218. With some examples, the number of Tx antennas 118 may be different than the number of Rx antennas 218. Furthermore, it is to be appreciated, that although the system 1000 is described having a transmitter (e.g., the transmitter 100) and a receiver (e.g., the receiver 200), each of the transmitter and receiver may be configured to both transmit and receive signals. Said differently, although not illustrated, the transmitter 100 may include

circuitry configured to both transmit and receiver signals using the wireless channel 10.

Similarly, although not illustrated, the receiver 200 may include circuitry configured to both receive and transmit signals using the wireless channel 10.

In some examples, the transmitter 100 and/or the receiver 200 may be components in a wireless system, such as, for example, access points, base stations, cells, mobile devices, or the like. As a particularly illustrative example, the transmitter 100 may be an access point (e.g., macro cell, small cell, base station, or the like) in a mobile broadband network, such as, for example, a mobile broadband network operating in compliance with at least one or more wireless communication standards (e.g., 802.11n, 802.11ac, 3GPP LTE-Advanced release 10, or the like) while the receiver 200 may be a mobile device (e.g., smartphone, tablet, laptop, wireless access point, or the like) in the mobile broadband network.

Turning more specifically to FIG. 1, at the transmitter 100, input data 110 is processed by transmitter circuitry 120 to transmit the input data 110 to the receiver 200 using the Tx antennas 118-1 to 118-N in compliance with a MIMO scheme. More specifically, the input data 110 may be transmitted to the receiver 200 as signals 11-1 to 11-N using the wireless channel 10. It is to be appreciated that a variety of different techniques are known for transmitting data according to a MIMO scheme. In general, however, the transmitter circuitry 120 may be configured to de-multiplex the input data 110 into multiple data streams. For example, the input data 110 may be de-multiplexed into N data streams (e.g., one for each of the Tx antennas 118-1 to 118-N.) In some examples, the input data 110 may be coded (e.g., based upon a standard, or the like.) The transmitter circuitry 120 may additionally be configured to modulate the de-multiplexed data streams. For example, the de-multiplexed data streams may be modulated using different constellation sets of quadrature amplitude modulation (QAM) symbols. The transmitter circuitry 120 may additionally be configured to transmit the de-multiplexed and modulated data streams to the receiver using the Tx antennas 118-1 to 118-N.

It is important to note, that the input data 110 may represent any of a variety of types of data that may be conveyed through wireless channel 10. Furthermore, the input data 110 may be generated by the transmitter 100 or may be generated elsewhere. Furthermore, the input data 110 may be retrieved from storage (not shown,) such as, for example, a computer readable storage media.

It is to be appreciated, that the signals 11-1 to 11-N may correspond to symbols (e.g., encoded symbols, or the like). Said differently, the signals 11-1 to 11-N may each be a symbol or a stream of symbols that are transmitted from the transmitter 100 to the receiver 200. At the

receiver 200, output data 210 is determined from the signals 11-1 to 11-N by a MIMO detection process. Said differently, the signals transmitted by the transmitter 100 are estimated by the receiver 200 based on the received signals and a MIMO detection process. As will be appreciated, the signals 11-1 to 11-N may correspond to one or more symbols. During
5 transmission, the order of the symbols or the symbols themselves may be changed due to effects of the channel 10. The receiver then determines an estimate for what the original symbols and their order were. Although care is taken herein to distinguish between signals, symbols, transmitted signals, received signals, estimated signals, etc., it is to be appreciated, that the desired meaning is to be understood from the context in which each phrase is used. In some
10 instances, these phrases may be used interchangeably and sometimes may inadvertently be used interchangeably. Additionally, the reference numerals 11-1 to 11-N are used to designate the signals in the system generally and may correspond to transmitted signals, received signals, estimated signals, or the like. Examples are not limited in this context.

The signals 11-1 to 11-N are received at the Rx antennas 218-1 to 218-M and processed by the
15 receiver circuitry 220. More specifically, output data 210 may be generated by the receiver circuitry 220 from the received signals 11-1 to 11-N. In some examples, the receiver circuitry 220 may apply various baseband processing (e.g., frequency offset compensation, synchronization, equalization, or the like) to the signals 11-1 to 11-N. Additionally, the receiver circuitry 220 may apply a MIMO detection process to the signals 11-1 to 11-N. In various
20 examples, the receiver circuitry applies a K-best SD process to the signals 11-1 to 11-N. In implementing the K-best SD process, the receiver circuitry may dynamically change the value of K for the K-best SD process. For example, the value of K may be dynamically adjusted based on channel estimation feedback using a channel quality indicator (CQI) 230. When the CQI 230 indicates good channel conditions, the value of K may be reduced. When the CQI 230 indicates
25 poor channel conditions, the value of K may be increased. Additionally, the value of K may be dynamically adjusted based on the signal-to-noise (SNR) ratio of the wireless channel 10. For example, where the SNR of the wireless channel 10 is high, the value of K may be reduced. Where the SNR of the wireless channel 10 is low, the value of K may be increased. Additionally, the value of K may be dynamically adjusted based on a desired BER target. Said differently, the
30 value of K may be dynamically adjusted based on an acceptable BER. For example, for a high acceptable BER, the value of K may be reduced. For a low acceptable BER, the value of K may be increased.

It is important to note, that the CQI 230 may be generated by the receiver 200 or may be generated elsewhere in the system 1000. Furthermore, a variety of different techniques for

measuring and or quantifying channel quality are known. For example, some standards (e.g., 3GPP LTE) provide for the receiver to generate the CQI as a 4-bit value and transmit the CQI to the transmitter for the transmitter to adapt the modulation scheme based on the current channel conditions. The CQI 230 may correspond to this 4-bit value. Examples are, however, not limited in this context.

Accordingly, the system 1000 provides a MIMO receiver that may be adaptable to a variety of different wireless channel conditions and/or operable with a variety of communication standards. In particular, the receiver may provide for a reduction in the power consumed while performing MIMO detection while maintaining acceptable levels of BER across a variety of channel conditions.

FIG. 2 is a block for the receiver 200. Although the receiver 200 shown in FIG. 2 has a limited number of elements in a certain topology or configuration, it may be appreciated that the receiver 200 may include more or less elements in alternate configurations as desired for a given implementation. The receiver 200 may include a computer and/or firmware implemented apparatus having circuitry 220 arranged to execute one or more components 222-*a*. It is noted that “*a*” and “*b*” and “*c*” and similar designators as used herein are intended to be variables representing any positive integer. Thus, for example, if an implementation sets a value for $a = 4$, then a complete set of components 222-*a* may include modules 222-1, 222-2, 222-3 or 222-4. The examples are not limited in this context.

According to some examples, the receiver 200 may be included in a receiver (e.g., access point, cell, mobile device, or the like) in a MIMO system. The receiver and the MIMO system may be capable of operating in compliance with one or more wireless technologies such as those described herein. For example, a receiver as shown in FIG. 2 may be arranged or configured to wirelessly receive multiple signals using multiple antennas and detect the transmitted signals using a MIMO detector. It is noted, that although the receiver 200 is discussed in conjunction with the MIMO system of FIG. 1, the examples are not limited in this context.

In some examples, as shown in FIG. 2, receiver 200 includes the circuitry 220 (e.g., as shown in FIG. 1.) The circuitry 220 may be generally arranged to execute one or more components 222-*a*. Circuitry 220 can be any of various commercially available processors, including without limitation an AMD® Athlon®, Duron® and Opteron® processors; ARM® application, embedded and secure processors; IBM® and Motorola® DragonBall® and PowerPC® processors; IBM and Sony® Cell processors; Qualcomm® Snapdragon®; Intel® Celeron®, Core (2) Duo®, Core i3, Core i5, Core i7, Itanium®, Pentium®, Xeon®, Atom® and XScale®

processors; and similar processors. Dual microprocessors, multi-core processors, and other multi-processor architectures may also be employed as circuitry 220. According to some examples circuitry 220 may also be an application specific integrated circuit (ASIC) and components 222-a may be implemented as hardware elements of the ASIC. According to some
5 examples circuitry 220 may also be a field programmable gate array (FPGA) and components 222-a may be implemented as hardware elements of the FPGA.

According to some examples, the receiver 200 may include a baseband processor 222-1. The circuitry 220 may execute the baseband processor 222-1 to receive a plurality of signals transmitted through a wireless channel using a plurality of receiving antennas. For example, the
10 circuitry 220 may execute the baseband processor 222-1 to receive the signals 11-1 to 11-N using Rx antennas 218-1 to 218-M. With some examples, the signals 11-1 to 11-N may be encoded using different sets of symbols (e.g., ASK, APSK, FSK, PSK, QAM, 16-QAM, 64-QAM, 256-QAM, or the like). It is to be appreciated, that although not shown in this figure for simplicity, the signals 11-1 to 11-N may be processed (e.g., down converted from RF to
15 baseband, or the like) between being received by the Rx antennas 218-1 to 218-M and processed by the baseband processor 222-1.

Additionally, the circuitry 220 may execute the baseband processor 222-1 to perform one or more baseband processing operations of the received signals 11-1 to 11-N. For example, the baseband processor 222-1 may apply frequency offset compensation, synchronization, and/or
20 equalization to the received signals 11-1 to 11-N.

In some examples, the apparatus 200 may include a MIMO detector 222-2. The circuitry 220 may execute the MIMO detector 222-2 to determine a plurality of estimated signals corresponding to the plurality of received signals. Said differently, the MIMO detector 222-2 may estimate the transmitted signals 11-1 to 11-N. More specifically, the MIMO detector 222-2
25 may estimate the symbols corresponding to the signals 11-1 to 11-N. As will be appreciated, the signals 11-1 to 11-N will be subject to noise, interference, or other errors due to being transmitted through the wireless channel 10. As such, the MIMO detector 222-2 determines an estimate for these signals. In general, the MIMO detector 222-2 is configured to implement a MIMO detection process and determine the estimated signals based on a search radius, where the
30 search radius is dynamically adjusted. For example, the MIMO detector 222-2 may implement of a K-best SD process to estimate the signals 11-1 to 11-N, with the value of K being dynamically adjustable based on channel conditions (e.g., the CQI 230.)

According to some examples, the apparatus 200 may include a search radius tuner 222-3. The circuitry 220 may execute the search radius tuner 222-3 to dynamically adjust the search radius. For example, the search radius tuner 222-3 may dynamically adjust the value of K used by the MIMO detector 222-2 to estimate the transmitted signals. With some examples, the search radius

5 tuner 222-3 may determine an optimal value of K based on the CQI 230 (e.g., using a lookup table, a function, fuzzy-logic, or the like.) The search radius tuner 222-3 may then configure the MIMO detector to determine the estimated signals using the determined optimal value of K.

With some examples, the maximum search radius implementable by the MIMO detector 222-2 may be determined based on a worst-case possible channel condition estimate for the wireless

10 channel 10. Subsequently, during operation, the search radius may be dynamically adjusted between the maximum value and a minimum value (e.g., 1, or the like). In addition, the search radius tuner 222-3 may dynamically adjust the search radius based on user feedback, BER targets, or the like. Said differently, the value of K may be adjusted (e.g., increased or decreased) in order to achieve acceptable BERs or in order to improve a user experience. As such, power

15 consumption of the MIMO detector 222-2 may be balanced between achieving an acceptable level of BER and increasing energy efficiency and throughput (e.g., time to perform MIMO detection.)

According to some examples, the apparatus 200 may include a MIMO decoder 222-4. The circuitry 220 may execute the MIMO decoder 222-4 to decode the estimated signals based on the

20 encoding scheme. For example, if the transmitter 100 encoded the signals using different constellation sets of 16-QAM symbols, the MIMO decoder 222-4 may decode the estimated signals using the same constellation sets of 16-QAM symbols. Additionally the MIMO decoder 222-4 may multiplex the decoded signals to generate the output signal 210.

FIGS. 3 – 4 illustrate block diagrams of an example MIMO detector 300. With some examples, the MIMO detector 300 may be implemented as the MIMO detector 222-2 of the receiver 200

25 described above. In general, FIG. 3 illustrates the MIMO detector 300, configured to implement a K-best SD process while FIG. 4 illustrates a portion (e.g., a single stage) of the MIMO detector 300. Prior to describing the MIMO detector 300, it is worthy to note that a MIMO system with N transmit antennas and M receive antennas, operating in a symmetric X-QAM scheme, with

30 $\log_2 X$ bits per symbol may be modeled by the following equation:

$$y = Hs + v,$$

where $s = [S_1, S_2, \dots, S_N]^T$, ($S_i \in \delta$) is the N-dimensional complex information symbol vector transmitted. The set δ is the constellation set of the QAM symbols, and $y = [y_1, y_2, \dots, y_M]^T$ is

the M-dimensional complex information symbol vector received. The equivalent baseband model of the Rayleigh fading channel between the transmitter and the receiver is described by a complex valued $N \times M$ channel matrix H . The vector $v = [v_1, v_2, \dots, v_M]^T$ represents the M-dimensional complex zero-mean Gaussian noise vector with variance σ^2 .

5 Since the MIMO system is modeled using complex signals (e.g., the signals include both real and imaginary components,) a K-best SD process results in a single $2N$ -dimensional search. In some examples, the search may begin with the N^{th} layer. For each n^{th} layer, the MIMO detector 300 may derive the K best partial candidates $[s_1^{(n)}, s_2^{(n)}, \dots, s_K^{(n)}]$, where partial candidate $s_i^{(n)}$ represents the i^{th} path through the search tree from the root node to the level n , and is given by
 10 $[s_{i,1}^{(n)}, s_{i,2}^{(n)}, \dots, s_{i,N}^{(n)}]$. The error at each step is measured by the partial Euclidian distance (PED), which represents the accrued error at a given level of the search tree, for a given path through the search tree. As will be appreciated, the K candidates at level n represent the K partial candidates with the minimum PED among all the children of the K candidates of the $(n+1)^{\text{st}}$ level, wherein the distance is calculated using the following equation:

$$15 \quad PED_i^{(n)} = \sum_{j=n}^N \left[\left(y_j - \sum_{k=j}^N R_{j,k} s_{i,k}^{(n)} \right)^2 \right].$$

Where $R_{j,k}$ are components of the $N \times N$ upper triangular matrix R such that $H=QR$, where Q is an $(N+M) \times N$ orthonormal matrix.

Turning now more specifically to **FIG. 3**, the MIMO detector 300 includes a number of stages 310. As the signals 11-1 to 11- N may be complex, a separate stage 310 may be provided for the real and imaginary components of each of the received signals. For example, for a 4×4 MIMO
 20 system, 8 stages 310 may be provided, 2 for each transmitted signal (e.g., 1 for the real portion and 1 for the imaginary portion or each signal.) Accordingly, the detector 300 is shown including stages 310-1 to 310- $2N$. It is important to note, however, the stages 310 are ordered from 310- $2N$, 310- $(2N-1)$, ..., 310-2, 310-1) to indicate that the detection process begins with the N^{th} level
 25 of the search tree. For an arbitrary level of the tree (e.g., an arbitrary stage 310,) the K best nodes are collected and passed to the next stage 310 for consideration. At the end (e.g., stage 310-1) the path with the minimum overall error (e.g., minimum PED) is selected as the most likely candidate. During operation, the value of K implemented by the stages 310 may be dynamically adjusted based on channel conditions, SNR, desired BER, or the like. For example, K may be
 30 varied based on the SNR of the wireless channel 10. The MIMO detector 300 includes a controller 320 to adjust the value of K implemented in each stage 310. In general, the controller 320 may power-gate and/or clock-gate various portions of each stage (e.g., refer to FIG. 4) on or

off to dynamically adjust the value of K . The controller 320 may generate controller signal 322 which is output to the stages 310 to cause the stages 310 to implement the desired search radius (e.g., change the value of K for the K -best SD process, or the like.)

Referring now more specifically to **FIG. 4**, a MIMO detector stage 310- i is shown. The MIMO
5 detector stage 310- i may correspond to any of the stages 310-1 to 310-2 N of the MIMO detector 300 illustrated in FIG. 3. As depicted, the stage 310- i includes a branch interference (BI) cancellation unit 311- i , a sorting unit 312- i , a candidate recording unit 313- i , and a merging unit 314- i . Furthermore, the candidate recording unit 313- i includes a number of k -entry recording blocks 315-1 to 315- L , where L equals the maximum value of K . For example, where the
10 maximum value of K equals 5, L may equal 5. In some examples, the value of L may be determined based on worst-case channel condition estimates. In some examples L may be an integer multiple of the maximum value of K to provide for time interleaving (e.g., refer to FIG. 5.)

It is to be appreciated, that a variety of techniques for implementing the stages 311 to 314 are
15 known. In general, however, the BI cancellation unit 311- i calculates the interference from detected signals on the symbol candidates and mitigates the interference. Said differently, the BI cancellation unit 311- i derives the PED for each of the potential candidates at the i^{th} level of the search tree. The sorting unit 312- i sorts the potential candidates. For example, the sorting unit 312- i may sort the potential candidates based on a Schnorr-Euchner (SE) enumeration scheme
20 and the PED. The candidate recorder unit 313- i stores the K -best potential candidates that have been found so far and updates the PED for each of the candidate paths through the search tree. The merge unit 314- i selects the K -best symbol candidates for each cycle based on the PED and propagates them to the next stage.

The candidate recording unit 313- i includes a number of k -entry recording blocks 315-1 to 315-
25 L . Each of the k -entry recording blocks 315 may be configured to store the K^{th} best potential candidate (e.g., the potential candidate with the K^{th} lowest PED.) Said differently, the first k -entry recording block may store the potential candidate with the lowest PED, the second k -entry recording block may store the potential candidate with the second lowest PED, etc.

As the value of K is dynamically adjustable (e.g., by the search radius tuner 222-3 described
30 above, the recording blocks 315 are configured to be powered on and off based on the search radius (e.g., value of K , or the like.) For example, for a value of $K = 2$, all but 2 of the k -entry recording blocks 315 may be powered off to reduce the power consumption of the MIMO detector 300. The controller 320 may power-gate and/or clock-gate the k -entry recording blocks

315 on or off based on the value of K . For example, the controller 320 may generate power-gating and/or clock-gating signals as the controller signal 322, which are output to the candidate recording unit 313 to cause the candidate recording unit to shut off (or turn on) one or more k -entry recording blocks 315 based on to the search radius.

- 5 For example, where the SNR of the channel 10 is low (e.g. channel conditions are poor), more of the k -entry recording blocks 315 may be powered on in order to provide a higher value of K and reduce the BER of the estimated signals. Similarly, where the SNR of the channel 10 is high (e.g., channel conditions are good), more of the k -entry recording blocks 315 may be powered off to provide reduced power requirements of the MIMO detector while preserving the BER of
- 10 the estimated signals.

FIG. 5 illustrates a timing diagram 500, which shows the effects of time interleaving on determining the potential candidates in a stage. More specifically, FIG. 5 illustrates timing diagrams for determining and storing potential candidates in the k -entry recording blocks 315 of a candidate recording unit 313- i of a stage 310- i of the MIMO detector 300. For example, the

15 diagram 500 shows determining a first set of potential candidates 510 for a first received symbol and a second set of potential candidate 520 for a second received symbol. It is noted, that 5 potential candidates are illustrated as being determined for each symbol (e.g., 510-1 to 510-5 and 520-1 to 520-5.) FIG. 5 shows the time in cycles 501 needed to determine each of the K -best candidates for a symbol. As depicted, it takes 5 cycles 501 (e.g., cycle 1 to cycle 5 for 510-1) to

20 determine a single candidate and an additional cycle to store the candidate. It is to be appreciated, that if all k -entry recording blocks are being used (e.g., maximum search radius is 5 and 5 k -entry recording blocks are provided) then determining potential candidates would need to stall. More specifically, the stage 310- i would stall between determining the potential

25 candidate 510-5 and the potential candidate 520-1 as the k -entry recording blocks are still determining and storing potential candidates. However, as illustrated, if the number of k -entry recording blocks 315 is an integer greater than a multiple of 2 times the maximum value of the search radius, then stalling may be avoided. This may increase the throughput of the MIMO detection process and provide for detecting MIMO signals transmitted with time interleaving without necessitating stalling in each stage.

- 30 **FIG. 6** illustrates an example of a logic flow 600. The logic flow 600 may be representative of some or all of the operations executed by one or more logic, features, or devices described herein, such as the receiver 200, circuitry 220, and/or the MIMO detector 300. In particular, a receiver may implement the logic flow 600 in a MIMO system to detect MIMO signals. For

example, the baseband processor 222-1, the MIMO detector 222-2, the search radius tuner 222-3, and/or the channel decoder 222-4 may implement the logic flow 600.

In the logic flow 600, at block 602, a receiver in a MIMO system may receive a plurality of signals transmitted through a wireless channel by a plurality of antennas. For example, the receiver 200 in the MIMO system 1000 may receive the signals 11-1 to 11-N transmitted through the wireless channel 10 using the antennas 218-1 to 218-M. More specifically, the baseband processor 222-1 may receive the signals 11-1 to 11-N.

At block 604, a quality corresponding to the wireless channel may be determined. For example, the receiver 200 may determine the CQI 230.

At block 606, a search radius based on the quality may be determined. For example, the receiver 200 may determine a search radius (e.g., value of K, or the like) based on the CQI 230. More specifically, the search radius tuner 222-3 may determine the search radius based on the CQI 230.

At block 608, a plurality of estimated signals corresponding to the transmitted signals may be determined based on the search radius. For example, the receiver 200 may perform MIMO detection (e.g., using a k-best SD process with the value of K determining the search radius, or the like) to determine estimates for the signals. More particularly, the MIMO detector 222-2 may determine estimates for the signals.

FIG. 7 illustrates an embodiment of a storage medium 700. The storage medium 700 may comprise an article of manufacture. In some examples, the storage medium 700 may include any non-transitory computer readable medium or machine readable medium, such as an optical, magnetic or semiconductor storage. The storage medium 700 may store various types of computer executable instructions, such as instructions to implement logic flow 600. Examples of a computer readable or machine readable storage medium may include any tangible media capable of storing electronic data, including volatile memory or non-volatile memory, removable or non-removable memory, erasable or non-erasable memory, writeable or re-writable memory, and so forth. Examples of computer executable instructions may include any suitable type of code, such as source code, compiled code, interpreted code, executable code, static code, dynamic code, object-oriented code, visual code, and the like. The examples are not limited in this context.

FIG. 8 illustrates an embodiment of a device 2000. In some examples, device 2000 may be configured or arranged for wireless communications in a wireless MIMO system such as the MIMO system 1000 shown in FIG. 1. In some examples, the receiver 200 may be implemented

in the device 2000. For example, the device 2000 may implement the receiver 200 as apparatus 2200. Additionally, the device 2000 may implement storage medium 700 and/or a logic circuit 2600. The logic circuit 2600 may include physical circuits to perform operations described for the apparatus 2200, storage medium 700, and/or logic flow 600. As shown in FIG. 8, device
5 2000 may include a radio interface 2110, baseband circuitry 2120, and computing platform 2130, although examples are not limited to this configuration.

The device 2000 may implement some or all of the structure and/or operations for the apparatus 2200, the storage medium 700 and/or the logic circuit 2600 in a single computing entity, such as entirely within a single device. The embodiments are not limited in this context.

10 Radio interface 2110 may include a component or combination of components adapted for transmitting and/or receiving single carrier or multi-carrier modulated signals (e.g., including complementary code keying (CCK) and/or orthogonal frequency division multiplexing (OFDM) symbols and/or single carrier frequency division multiplexing (SC-FDM symbols) although the embodiments are not limited to any specific over-the-air interface or modulation scheme. Radio
15 interface 2110 may include, for example, a receiver 2112, a transmitter 2116 and/or a frequency synthesizer 2114. Radio interface 2110 may include bias controls, a crystal oscillator and antennas 2118-1 to 2118-f. In another embodiment, radio interface 2110 may use external voltage-controlled oscillators (VCOs), surface acoustic wave filters, intermediate frequency (IF) filters and/or RF filters, as desired. Due to the variety of potential RF interface designs an
20 expansive description thereof is omitted.

Baseband circuitry 2120 may communicate with radio interface 2110 to process receive and/or transmit signals and may include, an analog-to-digital converter 2122 and/or a digital-to-analog converter 2124 for use in processing receive/transmit signals (e.g., up converting, down
25 converting, filtering, sampling or the like.) Further, baseband circuitry 2120 may include a baseband or physical layer (PHY) processing circuit 2126 for PHY link layer processing of respective receive/transmit signals. Baseband circuitry 2120 may include, for example, a processing circuit 2128 for medium access control (MAC)/data link layer processing. Baseband circuitry 2120 may include a memory controller 2132 for communicating with MAC processing circuit 2128 and/or a computing platform 2130, for example, via one or more interfaces 2134.

30 In some examples, the MAC 2128 may be configured to include and/or perform the structures and/or methods described herein. Said differently, the MAC 21128 may be configured to include the MIMO detector 200 (e.g., embodied as apparatus 2200). As another example, the MAC 2128 may be configured to include the storage medium 700. As another example, the MAC 2128 may

be configured to implement logic circuit 600 (e.g., embodied as logic circuit 2600.) As another example, the MAC 2128 may access the computing platform 2130 to implement and/or perform the structure and/or methods described herein.

In some embodiments, PHY processing circuit 2126 may include a frame construction and/or detection module, in combination with additional circuitry such as a buffer memory, to construct and/or deconstruct communication frames (e.g., containing subframes). Alternatively or in addition, MAC processing circuit 2128 may share processing for certain of these functions or perform these processes independent of PHY processing circuit 2126. In some embodiments, MAC and PHY processing may be integrated into a single circuit.

10 Computing platform 2130 may provide computing functionality for device 2000. As shown, computing platform 2130 may include a processing component 2140. In addition to, or alternatively of, baseband circuitry 2120 of device 2000 may execute processing operations or logic for the apparatus 2200, storage medium 700, and logic circuit 2600 using the processing component 2130. Processing component 2140 (and/or PHY 2126 and/or MAC 2128) may
15 comprise various hardware elements, software elements, or a combination of both. Examples of hardware elements may include devices, logic devices, components, processors, microprocessors, circuits, processor circuits, circuit elements (e.g., transistors, resistors, capacitors, inductors, and so forth), integrated circuits, application specific integrated circuits (ASIC), programmable logic devices (PLD), digital signal processors (DSP), field programmable
20 gate array (FPGA), memory units, logic gates, registers, semiconductor device, chips, microchips, chip sets, and so forth. Examples of software elements may include software components, programs, applications, computer programs, application programs, system programs, software development programs, machine programs, operating system software, middleware, firmware, software modules, routines, subroutines, functions, methods, procedures,
25 software interfaces, application program interfaces (API), instruction sets, computing code, computer code, code segments, computer code segments, words, values, symbols, or any combination thereof. Determining whether an example is implemented using hardware elements and/or software elements may vary in accordance with any number of factors, such as desired computational rate, power levels, heat tolerances, processing cycle budget, input data rates,
30 output data rates, memory resources, data bus speeds and other design or performance constraints, as desired for a given example.

Computing platform 2130 may further include other platform components 2150. Other platform components 2150 include common computing elements, such as one or more processors, multi-core processors, co-processors, memory units, chipsets, controllers, peripherals, interfaces,

oscillators, timing devices, video cards, audio cards, multimedia input/output (I/O) components (e.g., digital displays), power supplies, and so forth. Examples of memory units may include without limitation various types of computer readable and machine readable storage media in the form of one or more higher speed memory units, such as read-only memory (ROM), random-
5 access memory (RAM), dynamic RAM (DRAM), Double-Data-Rate DRAM (DDRAM), synchronous DRAM (SDRAM), static RAM (SRAM), programmable ROM (PROM), erasable programmable ROM (EPROM), electrically erasable programmable ROM (EEPROM), flash memory, polymer memory such as ferroelectric polymer memory, ovonic memory, phase change or ferroelectric memory, silicon-oxide-nitride-oxide-silicon (SONOS) memory, magnetic or
10 optical cards, an array of devices such as Redundant Array of Independent Disks (RAID) drives, solid state memory devices (e.g., USB memory, solid state drives (SSD) and any other type of storage media suitable for storing information.

Computing platform 2130 may further include a network interface 2160. In some examples, network interface 2160 may include logic and/or features to support network interfaces operated
15 in compliance with one or more wireless broadband technologies such as those described in one or more standards associated with IEEE 802.11 such as IEEE 802.11u or with technical specification such as WFA Hotspot 2.0.

Device 2000 may be part of a source or destination node in a MIMO system and may be included in various types of computing devices to include, but not limited to, user equipment, a
20 computer, a personal computer (PC), a desktop computer, a laptop computer, a notebook computer, a netbook computer, a tablet computer, an ultra-book computer, a smart phone, embedded electronics, a gaming console, a server, a server array or server farm, a web server, a network server, an Internet server, a work station, a mini-computer, a main frame computer, a supercomputer, a network appliance, a web appliance, a distributed computing system,
25 multiprocessor systems, processor-based systems, wearable computing device or combination thereof. Accordingly, functions and/or specific configurations of device 2000 described herein; may be included or omitted in various embodiments of device 2000, as suitably desired. In some embodiments, device 2000 may be configured to be compatible with protocols and frequencies associated with IEEE 802.11 Standards or Specification and/or 3GPP Standards or Specifications
30 for MIMO systems, although the examples are not limited in this respect.

The components and features of device 2000 may be implemented using any combination of discrete circuitry, application specific integrated circuits (ASICs), logic gates and/or single chip architectures. Further, the features of device 2000 may be implemented using microcontrollers, programmable logic arrays and/or microprocessors or any combination of the foregoing where

suitably appropriate. It is noted that hardware, firmware and/or software elements may be collectively or individually referred to herein as “logic” or “circuit.”

It should be appreciated that the exemplary device 2000 shown in the block diagram of FIG. 8 may represent one functionally descriptive example of many potential implementations.

5 Accordingly, division, omission or inclusion of block functions depicted in the accompanying figures does not infer that the hardware components, circuits, software and/or elements for implementing these functions would be necessarily be divided, omitted, or included in embodiments.

10 Some examples may be described using the expression “in one example” or “an example” along with their derivatives. These terms mean that a particular feature, structure, or characteristic described in connection with the example is included in at least one example. The appearances of the phrase “in one example” in various places in the specification are not necessarily all referring to the same example.

15 Some examples may be described using the expression “coupled”, “connected”, or “capable of being coupled” along with their derivatives. These terms are not necessarily intended as synonyms for each other. For example, descriptions using the terms “connected” and/or “coupled” may indicate that two or more elements are in direct physical or electrical contact with each other. The term “coupled,” however, may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

20 What has been described above includes examples of the disclosed architecture. It is, of course, not possible to describe every conceivable combination of components and/or methodologies, but one of ordinary skill in the art may recognize that many further combinations and permutations are possible. Accordingly, the novel architecture is intended to embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended
25 claims. The detailed disclosure now turns to providing examples that pertain to further embodiments. The examples provided below are not intended to be limiting.

Example 1: An apparatus for a wireless receiver. The example apparatus comprising circuitry; a multiple-input multiple-output (MIMO) detector for execution by the circuitry to determine a plurality of estimated signals, the plurality of estimated signals corresponding to a plurality of
30 signals transmitted through a wireless channel and received by a plurality of antennas, the MIMO detector to determine the plurality of estimated signals based on a search radius; and a search radius tuner for execution by the circuitry to dynamically modify the search radius based on a quality corresponding to the wireless channel.

Example 2: The apparatus of example 1, the MIMO detector to determine the plurality of estimated signal based on a K-best sphere decoding (SD) process, wherein the search radius corresponds to the value of K in the K-best SD process.

5 Example 3: The apparatus of any one of examples 1 to 2, the search radius tuner to increase the search radius when the quality decreases.

Example 4: The apparatus of any one of examples 1 to 3, the search radius tuner to decrease the search radius when the quality increases.

10 Example 5: The apparatus of any one of examples 2, the MIMO detector comprising a plurality of stages, each of the stages to determine a plurality of potential candidates for estimating at least a portion of one of the received signals.

Example 6: The apparatus of example 5, each of the stages including a sorting unit for execution by the circuitry to sort the plurality of potential candidates.

15 Example 7: The apparatus of example 6, wherein the transmitted signals are encoded using a constellation set of symbols, each of the plurality of potential candidates indicating an estimate for a symbol, the symbol corresponding to the symbol with which the transmitted signal is encoded, the sorting unit to sort the plurality of potential candidates based on a partial Euclidian distance (PED) determined for the symbols of each of the plurality of potential candidates.

20 Example 8: The apparatus of example 7, each of the stages including a candidate recording unit for execution by the circuitry to store one or more of the plurality of potential candidates and update the PED corresponding to each of the one or more stored potential candidates.

Example 9: The apparatus of example 8, each of the candidate recording units including a plurality of K-entry recording blocks, each of the K-entry recording blocks to store a one of the plurality of potential candidates.

25 Example 10: The apparatus of example 9, the MIMO detector including a search radius controller to power on or off one or more of the plurality of K-entry recording blocks of each of the candidate recording units to adjust the value of K implemented by the MIMO detector.

Example 11: The apparatus of example 10, the search radius controller to power on or off one or more of the plurality of K-entry recording blocks by power-gating the K-entry recording blocks,

clock-gating the K-entry recording blocks, or power-gating and clock-gating the K-entry recording blocks.

Example 12: The apparatus of example 10, wherein the number of K-entry recording blocks of each candidate recording unit that are powered on corresponds to the value of K.

- 5 Example 13: The apparatus of any one of examples 9 to 12, wherein each of candidate recording units includes a number of K-entry recording blocks corresponding to a maximum value of K.

Example 14: The apparatus of example 13, wherein the maximum value of K is determined based on worst-case condition estimated for the wireless channel.

- 10 Example 15: The apparatus of example 13, wherein the number of K-entry recording blocks in each candidate recording unit is an integer multiple of the maximum value of K to provide for time interleaving.

Example 16: The apparatus of example 13, wherein the number of K-entry recording blocks in each candidate recording unit is 5.

- 15 Example 17: The apparatus of any one of examples 5 to 12, each of the stages including a merge unit for execution by the circuitry to identify one or more of the plurality of potential candidates as based at least in part on the PED corresponding to each of the one or more potential candidates stored in the one or more K-entry blocks.

Example 18: The apparatus of any one of of examples 5 to 12, further comprising a baseband processor for execution by the circuitry to receive the plurality of signals.

- 20 Example 19: The apparatus of example 18, the baseband processor to perform one or more baseband processing operations on the plurality of received signals.

Example 20: The apparatus of example 19, the one or more baseband processing operations selected from the group consisting of: frequency offset compensation, synchronization, and equalization.

- 25 Example 21: The apparatus of any one of examples 5 to 12, further comprising a MIMO decoder to determine an output signal from the plurality of estimated signals.

Example 22: The apparatus of example 21, the MIMO decoder to decode the plurality of estimated signals based on an encoding scheme.

Example 23: The apparatus of example 22, the encoding scheme selected from the group consisting of ASK, APSK, FSK, PSK, QAM, and 16-QAM.

Example 24: A method implemented by a receiver in a MIMO system. The method comprising receiving a plurality of signals transmitted through a wireless channel by a plurality of antennas;
5 determining a quality corresponding to the wireless channel; determining a search radius based on the quality; and determining a plurality of estimated signals corresponding to the plurality of transmitted signals based on the search radius.

Example 25: The method of example 24, determining the plurality of estimated signals comprises determining the plurality of estimated signals based on a K-best sphere decoding (SD)
10 process, wherein the search radius corresponds to the value of K in the K-best SD process.

Example 26: The method of any one of examples 24 to 25, determining a quality corresponding to the wireless channel comprises determining a signal to noise ratio (SNR) for the wireless channel.

Example 27: The method of example 26, determining a dynamic search radius based on the
15 quality comprises increasing the search radius when the SNR is low.

Example 28: The method of example 26, determining a dynamic search radius based on the quality comprises decreasing the search radius when the SNR is high.

Example 29: The method of example 25, comprising determining a plurality of potential candidates for estimating at least a portion of one of the received signals in stages, each stage
20 being associated with at least a portion of one of the plurality of received signals.

Example 30: The method of example 29, comprising sorting the plurality of potential candidates at each stage.

Example 31: The method of example 30, wherein the transmitted signals are encoded using a constellation set of symbols, each of the plurality of potential candidates indicating an estimate
25 for a symbol, the symbol corresponding to the symbol with which the transmitted signal is encoded, sorting the plurality of potential candidates based on a partial Euclidian distance (PED) determined for the symbols of each of the plurality of potential candidates at each stage.

Example 32: The method of example 31, storing one or more of the plurality of potential candidates and update the PED corresponding to each of the one or more stored potential candidates at each stage.

5 Example 33: The method of example 32, wherein the number of the plurality of potential candidates stored at each stage corresponds to the search radius.

Example 34: The method of example 33, power on or off portions of a MIMO detector circuit to store the number of plurality of potential candidates corresponding to the search radius to reduce power consumption of the MIMO detector during periods where the search radius is lowered.

10 Example 35: The method of any one of examples 24 to 25, further comprising performing one or more baseband processing operations on the plurality of received signals.

Example 36: The method of example 35, the one or more baseband processing operations selected from the group consisting of: frequency offset compensation, synchronization, and equalization.

15 Example 37: The method of any one of examples 24 to 25, further comprising a determining an output signal from the estimated plurality of signals.

Example 38: The method of example 37, determining the output signal comprising decoding the plurality of estimated signals based on an encoding scheme.

Example 39: The method of example 38, the encoding scheme selected from the group consisting of ASK, APSK, FSK, PSK, QAM, and 16-QAM.

20 Example 40: An apparatus comprising means to perform the method of any one of examples 24 to 39.

Example 41: At least one machine readable medium comprising a plurality of instructions that in response to being executed on a receiver in a multiple-input multiple-output (MIMO) communication system cause the receiver to perform the method of any one of examples 24 to
25 39.

Claims

1. An apparatus for a wireless receiver comprising:

circuitry;

5 a multiple-input multiple-output (MIMO) detector for execution by the circuitry to determine a plurality of estimated signals, the plurality of estimated signals corresponding to a plurality of signals transmitted through a wireless channel and received by a plurality of antennas, the MIMO detector to determine the plurality of estimated signals based on a search radius; and

10 a search radius tuner for execution by the circuitry to dynamically modify the search radius based on a quality corresponding to the wireless channel.

2. The apparatus of claim 1, the MIMO detector to determine the plurality of estimated signal based on a K-best sphere decoding (SD) process, wherein the search radius corresponds to the value of K in the K-best SD process.

15 3. The apparatus of any one of claims 1 to 2, the search radius tuner to increase the search radius when the quality decreases and decrease the search radius when the quality increases.

4. The apparatus of any one of claims 1 to 2, the MIMO detector comprising a plurality of stages, each of the stages to determine a plurality of potential candidates for estimating at least a portion of one of the received signals.

20 5. The apparatus of claim 4, wherein the transmitted signals are encoded using a constellation set of symbols, each of the plurality of potential candidates indicating an estimate for a symbol, the symbol corresponding to the symbol with which the transmitted signal is encoded, each of the stages including a sorting unit for execution by the circuitry to sort the plurality of potential candidates based on a partial Euclidian distance (PED) determined for the symbols of each of the plurality of potential candidates.

25 6. The apparatus of claim 5, each of the stages including a candidate recording unit for execution by the circuitry to store one or more of the plurality of potential candidates and update the PED corresponding to each of the one or more stored potential candidates, each of the candidate recording units including a plurality of K-entry recording blocks, each of the K-entry recording blocks to store a one of the plurality of potential candidates.

7. The apparatus of claim 6, the MIMO detector including a search radius controller to power on or off one or more of the plurality of K-entry recording blocks of each of the candidate recording units to adjust the value of K implemented by the MIMO detector.
8. The apparatus of claim 7, the search radius controller to power on or off one or more of the plurality of K-entry recording blocks by power-gating the K-entry recording blocks, clock-gating the K-entry recording blocks, or power-gating and clock-gating the K-entry recording blocks.
9. The apparatus of claim 8, wherein the number of K-entry recording blocks of each candidate recording unit that are powered on corresponds to the value of K.
10. The apparatus of any one of claims 6 to 9, wherein each of candidate recording units includes a number of K-entry recording blocks corresponding to a maximum value of K.
11. The apparatus of any one of claims 4 to 9, each of the stages including a merge unit for execution by the circuitry to identify one or more of the plurality of potential candidates as based at least in part on the PED corresponding to each of the one or more potential candidates stored in the one or more K-entry blocks.
12. The apparatus of any one of claims 4 to 9, further comprising a baseband processor for execution by the circuitry,
- the baseband processor to receive the plurality of signals; and
 - the baseband processor to perform one or more baseband processing operations on the plurality of received signals
13. The apparatus of any one of claims 4 to 9, further comprising a MIMO decoder to decode the plurality of estimated signals based on an encoding scheme.
14. A method implemented by a receiver in a MIMO system comprising:
- receiving a plurality of signals transmitted through a wireless channel by a plurality of antennas;
 - determining a quality corresponding to the wireless channel;
 - determining a search radius based on the quality; and

determining a plurality of estimated signals corresponding to the plurality of transmitted signals based on the search radius.

15. The method of claim 14, determining the plurality of estimated signals comprises determining the plurality of estimated signals based on a K-best sphere decoding (SD) process, wherein the search radius corresponds to the value of K in the K-best SD process.
- 5
16. The method of any one of claims 14 to 15, determining a quality corresponding to the wireless channel comprises determining a signal to noise ratio (SNR) for the wireless channel.
17. The method of claim 16, determining a dynamic search radius based on the quality comprises increasing the search radius when the SNR is low and decreasing the search radius when the SNR is high.
- 10
18. The method of claim 17, comprising determining a plurality of potential candidates for estimating at least a portion of one of the received signals in stages, each stage being associated with at least a portion of one of the plurality of received signals.
19. The method of claim 18, wherein the transmitted signals are encoded using a constellation set of symbols, each of the plurality of potential candidates indicating an estimate for a symbol, the symbol corresponding to the symbol with which the transmitted signal is encoded, the method comprising sorting the plurality of potential candidates at each stage, the sorting based on a partial Euclidian distance (PED) determined for the symbols of each of the plurality of potential candidates at each stage.
- 15
20. The method of claim 19, storing one or more of the plurality of potential candidates and update the PED corresponding to each of the one or more stored potential candidates at each stage.
- 20
21. The method of claim 20, wherein the number of the plurality of potential candidates stored at each stage corresponds to the search radius.
22. The method of claim 21, power on or off portions of a MIMO detector circuit to store the number of plurality of potential candidates corresponding to the search radius to reduce power consumption of the MIMO detector during periods where the search radius is lowered.
- 25

23. At least one machine readable medium comprising a plurality of instructions that in response to being executed on a receiver in a multiple-input multiple-output (MIMO) communication system cause the receiver to:

5 receive an indication of a plurality of signals transmitted through a wireless channel by a plurality of antennas;

determine a quality corresponding to the wireless channel;

determine a search radius based on the quality; and

10 determine a plurality of estimated signals based on a K-best sphere decoding (SD) process, wherein the search radius corresponds to the value of K in the K-best SD process, the estimated signals corresponding to the plurality of transmitted signals based on the search radius.

24. The at least one machine readable medium of claim 23, the receiver to determine a plurality of potential candidates for estimating at least a portion of one of the plurality of signals in stages, each stage being associated with at least a portion of one of the plurality of received signals.

15 25. The at least one machine readable medium of claim 23, the receiver to power on or off portions of a MIMO detector circuit to store the number of plurality of potential candidates corresponding to the search radius to reduce power consumption of the MIMO detector during periods where the search radius is lowered.

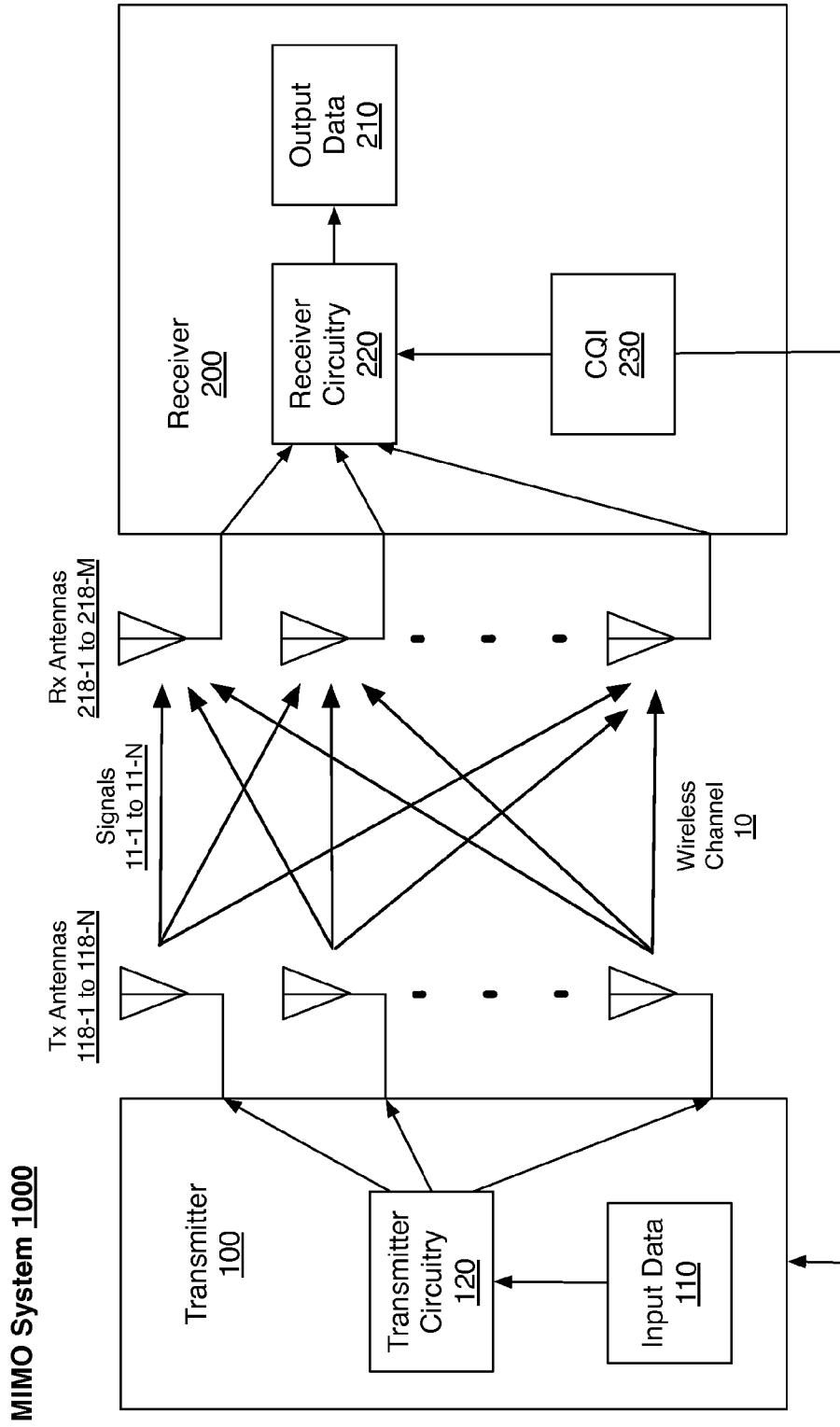


FIG. 1

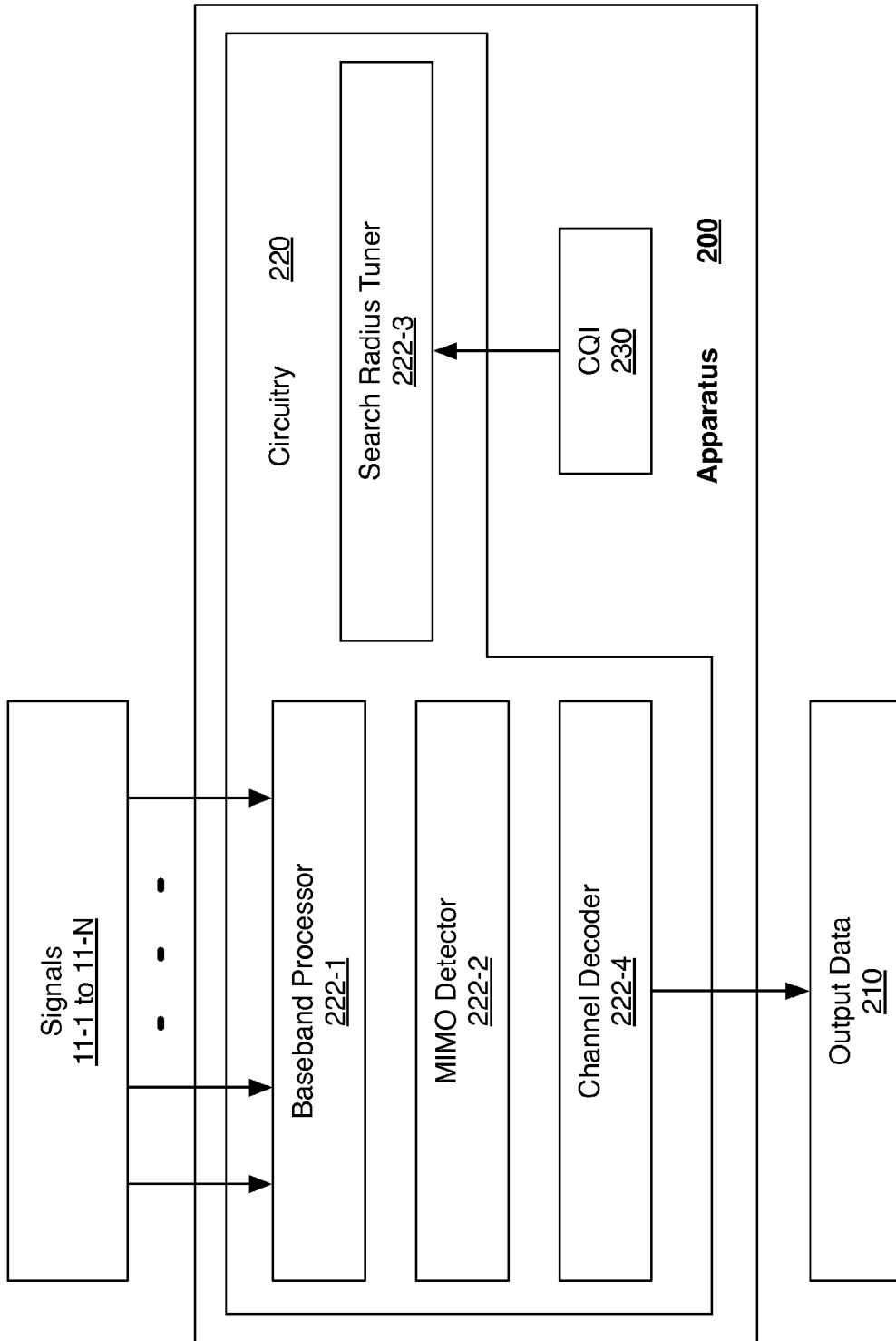


FIG. 2

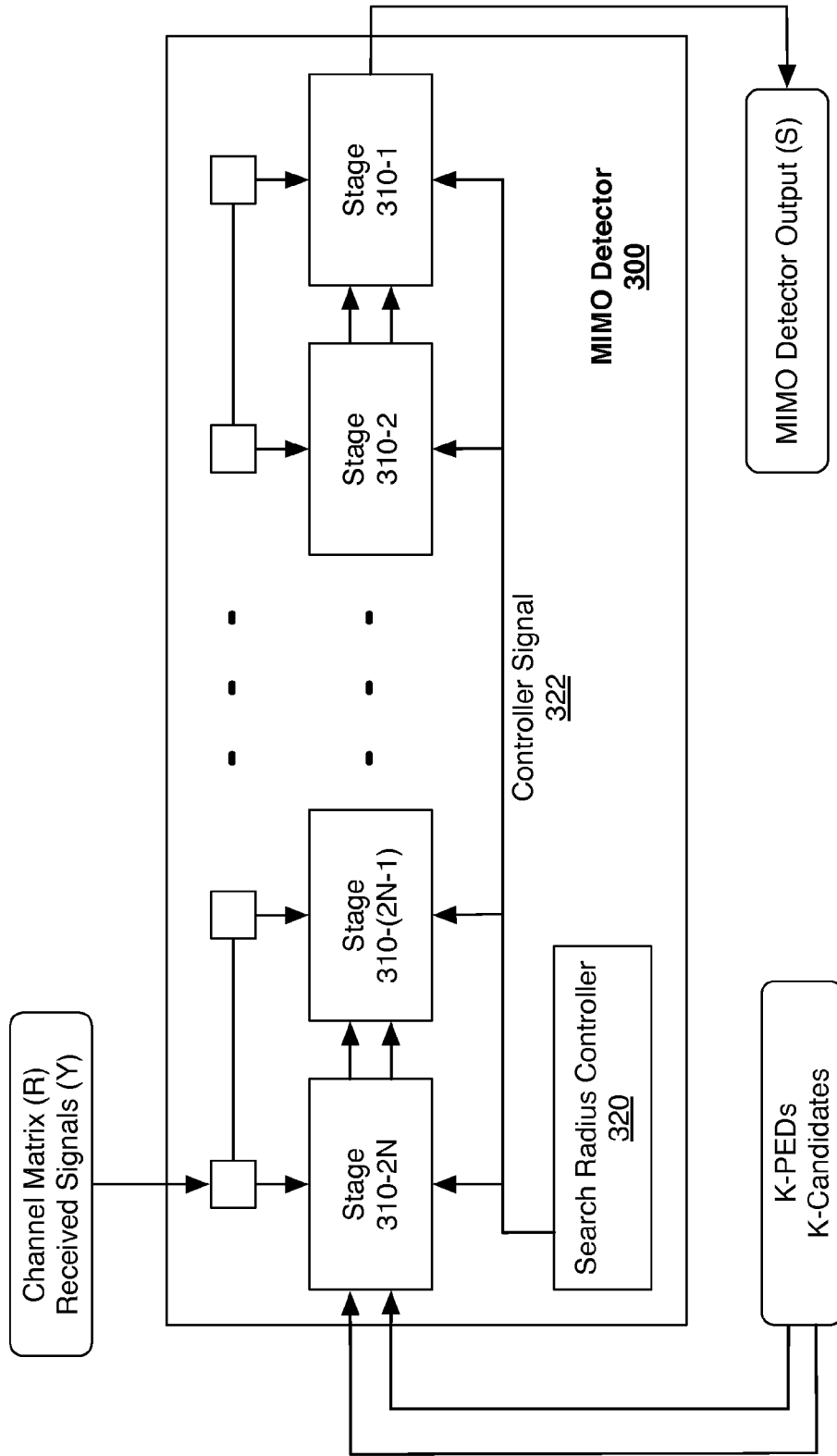


FIG. 3

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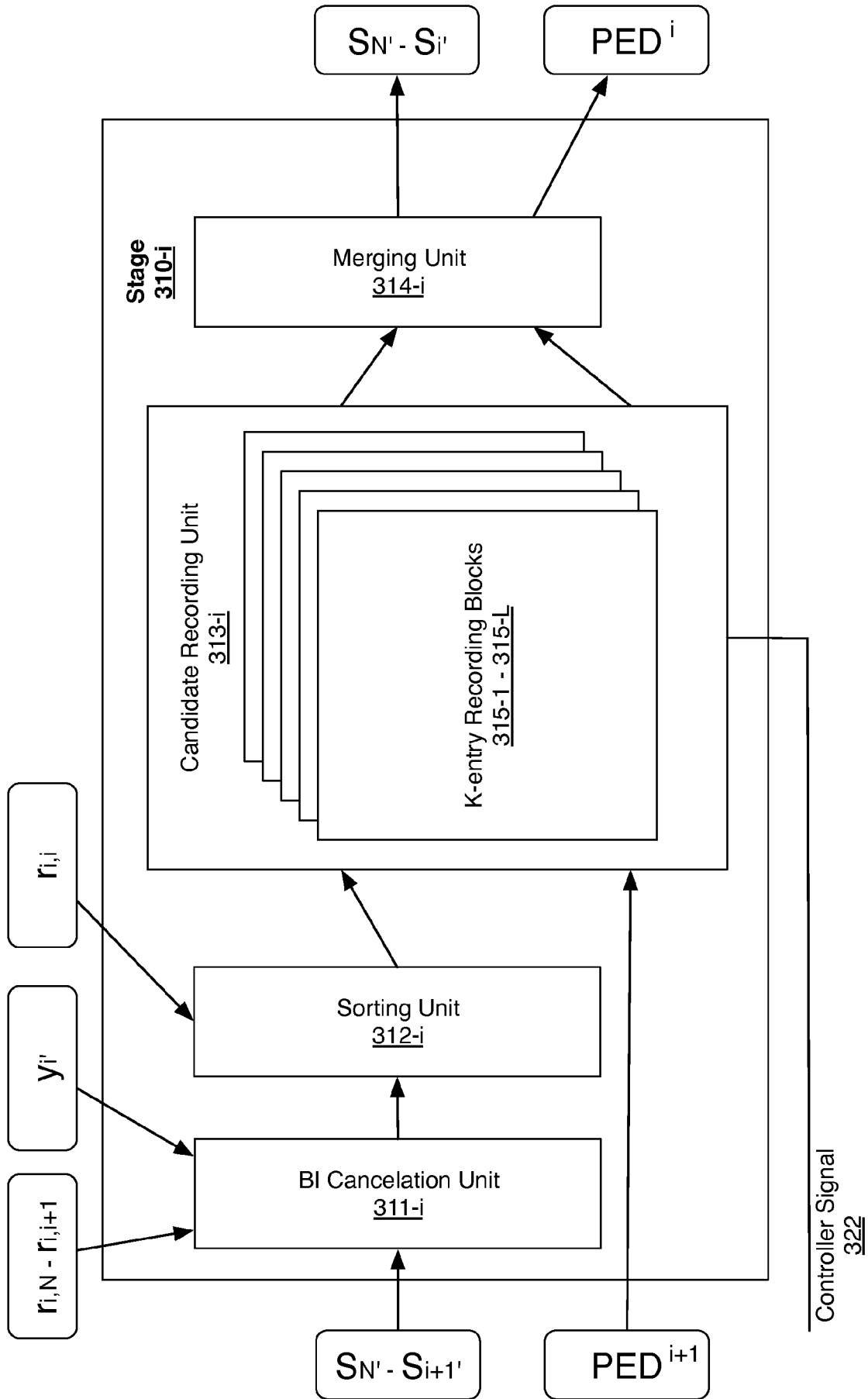


FIG. 4

500

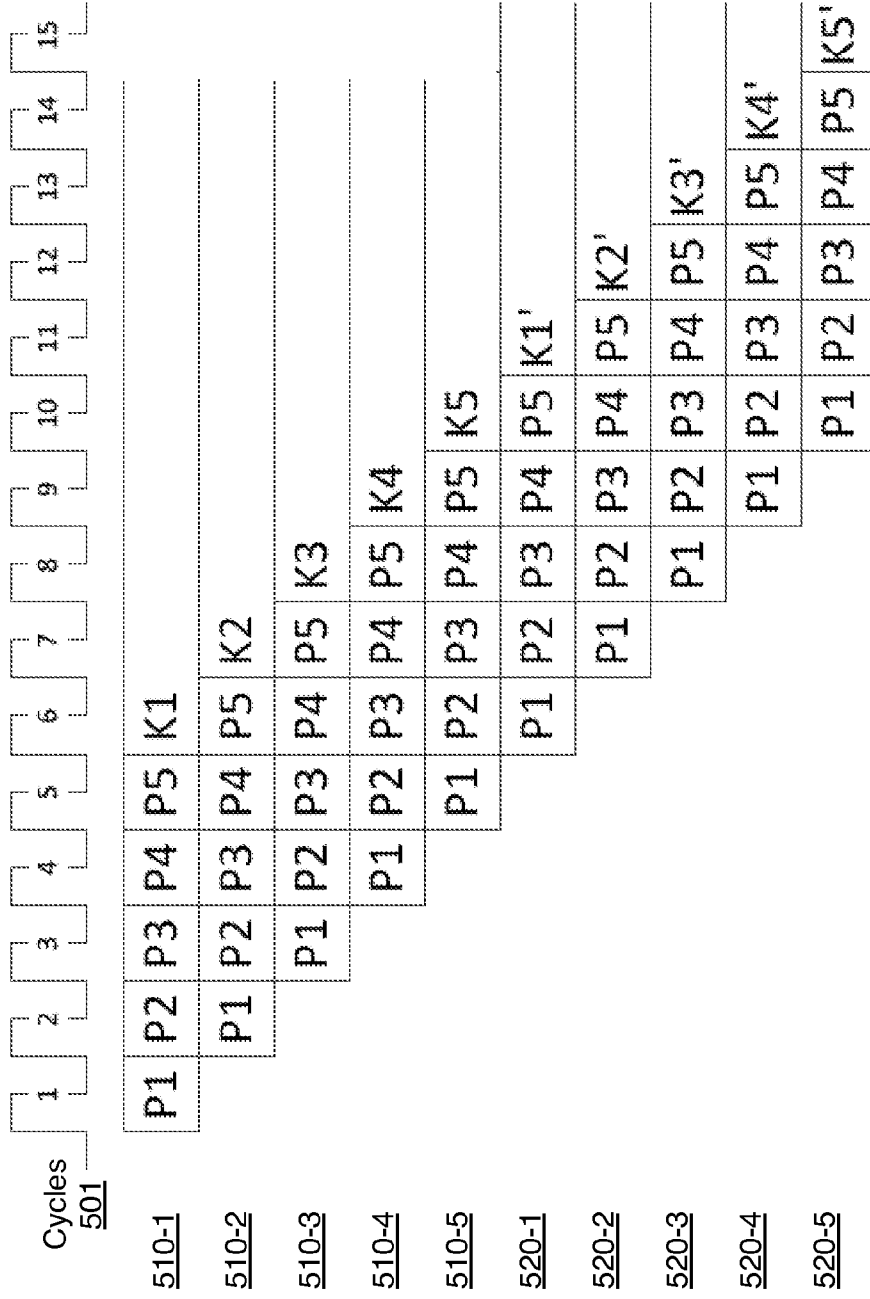


FIG. 5

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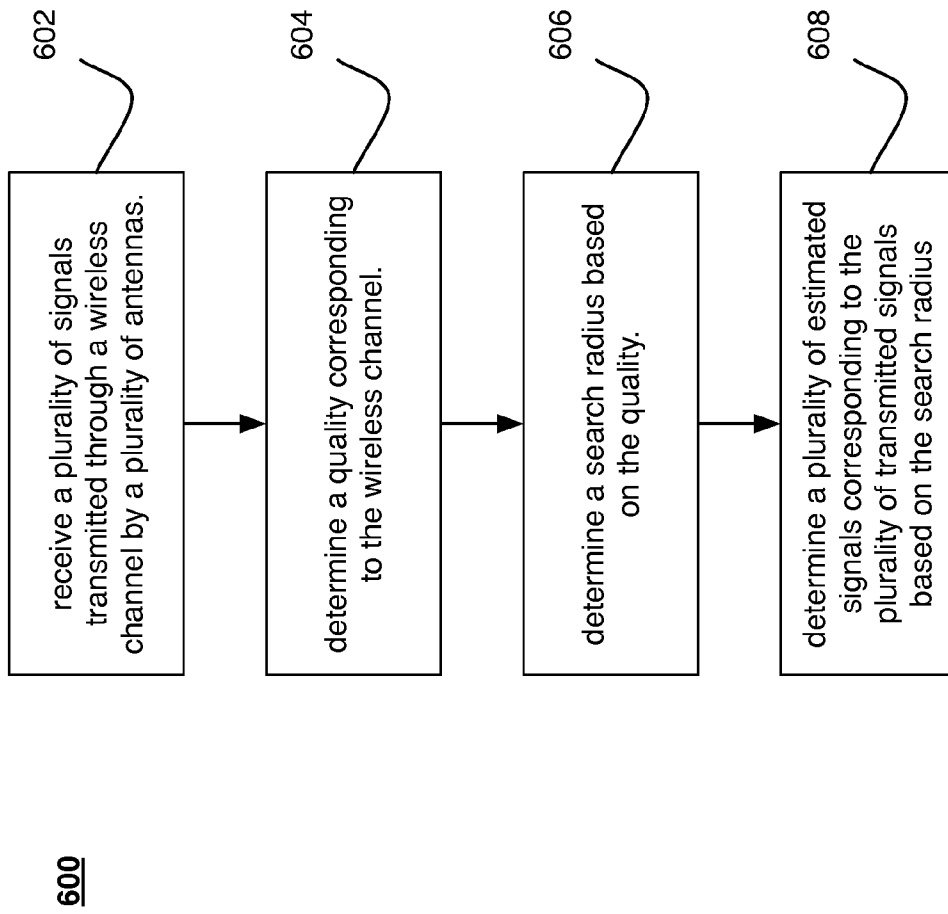


FIG. 6

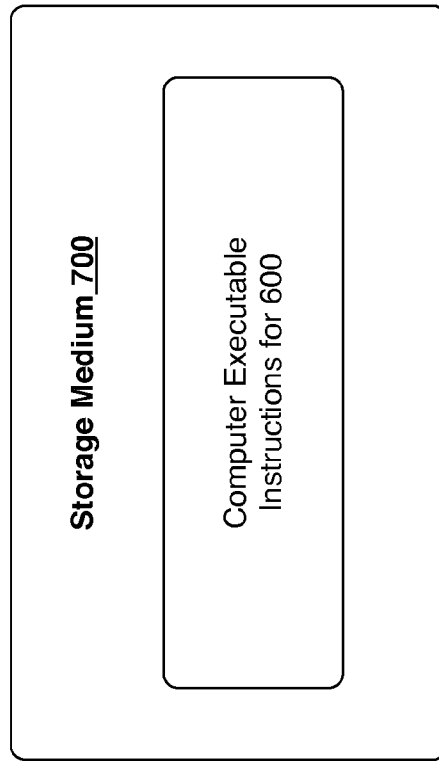


FIG. 7

Device 2000

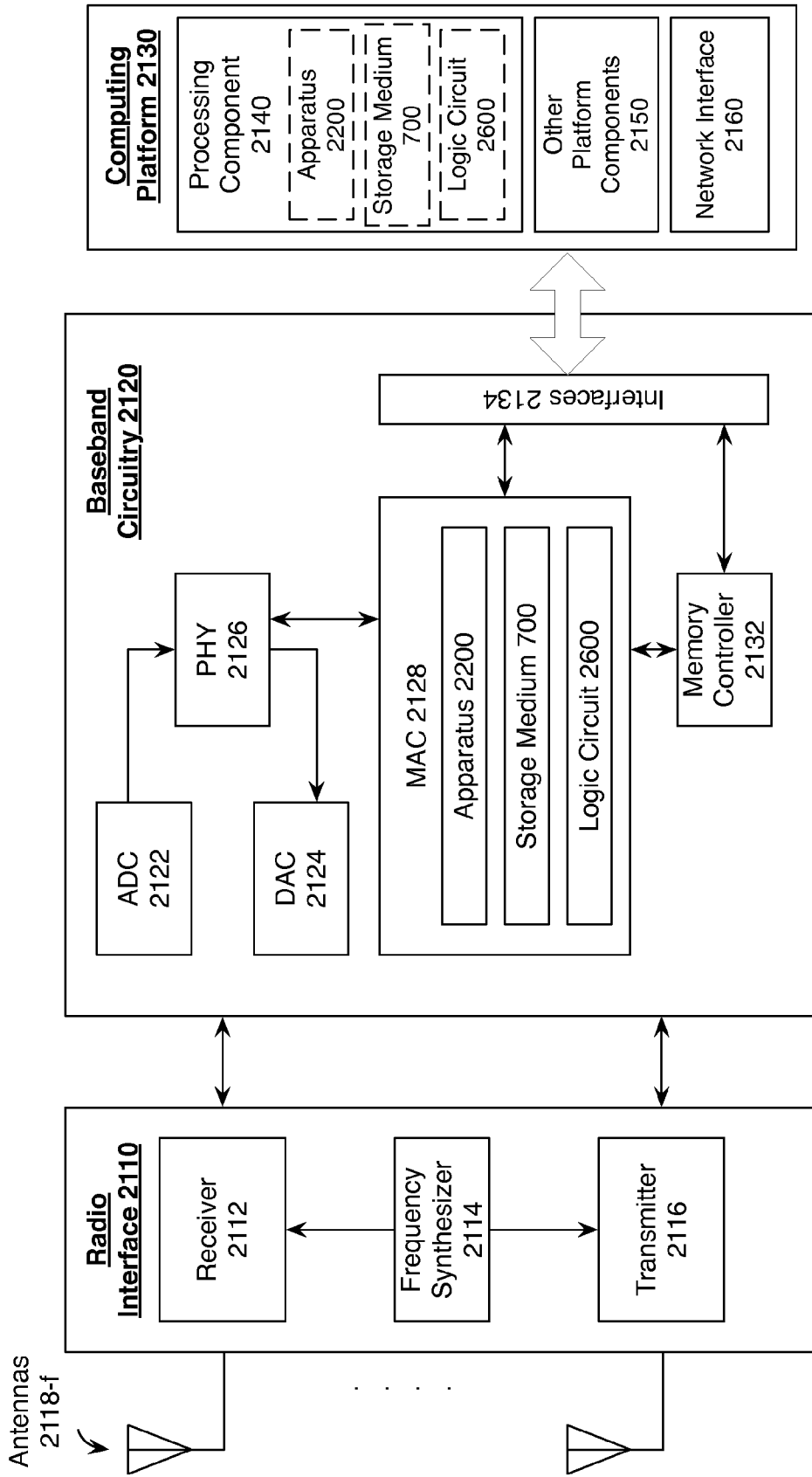


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/072239**A. CLASSIFICATION OF SUBJECT MATTER****H04B 7/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H04B 7/08; H04L 1/00; H03D 1/24; H04L 25/03; H04L 27/06; H03D 1/00Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: multiple-input multiple-output (MIMO) detector, search radius, quality, wireless channel, modify, K-best sphere decoding (SD), potential candidates, stage, sorting, partial Euclidian distance (PED), K-entry recording, power-gating, clock-gating, power on, power off, constellation set**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0286313 A1 (HOSEIN NIKOPOUR-DEILAMI et al.) 13 December 2007 See paragraphs 13, 16, 31; claims 10-15, 49; and figures 1-3.	1-4, 14-18, 23, 24
Y		5, 6, 19-21
A		7-9, 22, 25
Y	WO 2011-150428 A1 (MAXLINEAR, INC.) 1 December 2011 See paragraphs 39, 59; and figure 2.	5, 6, 19-21
A	WO 2011-153802 A1 (ZTE CORPORATION) 15 December 2011 See claims 1, 6; and figures 1-3.	1-9, 14-25
A	US 2010-0054365 A1 (SHAU-YU CHENG et al.) 4 March 2010 See paragraphs 17, 63; claims 1, 2; and figures 3-5.	1-9, 14-25
A	WO 2010-078087 A2 (QUALCOMM INCORPORATED) 8 July 2010 See paragraphs 65-68; claims 1, 4-6; and figures 9, 10.	1-9, 14-25

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

24 June 2014 (24.06.2014)

Date of mailing of the international search report

25 June 2014 (25.06.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2013/072239**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.: 10-13
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/072239

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