

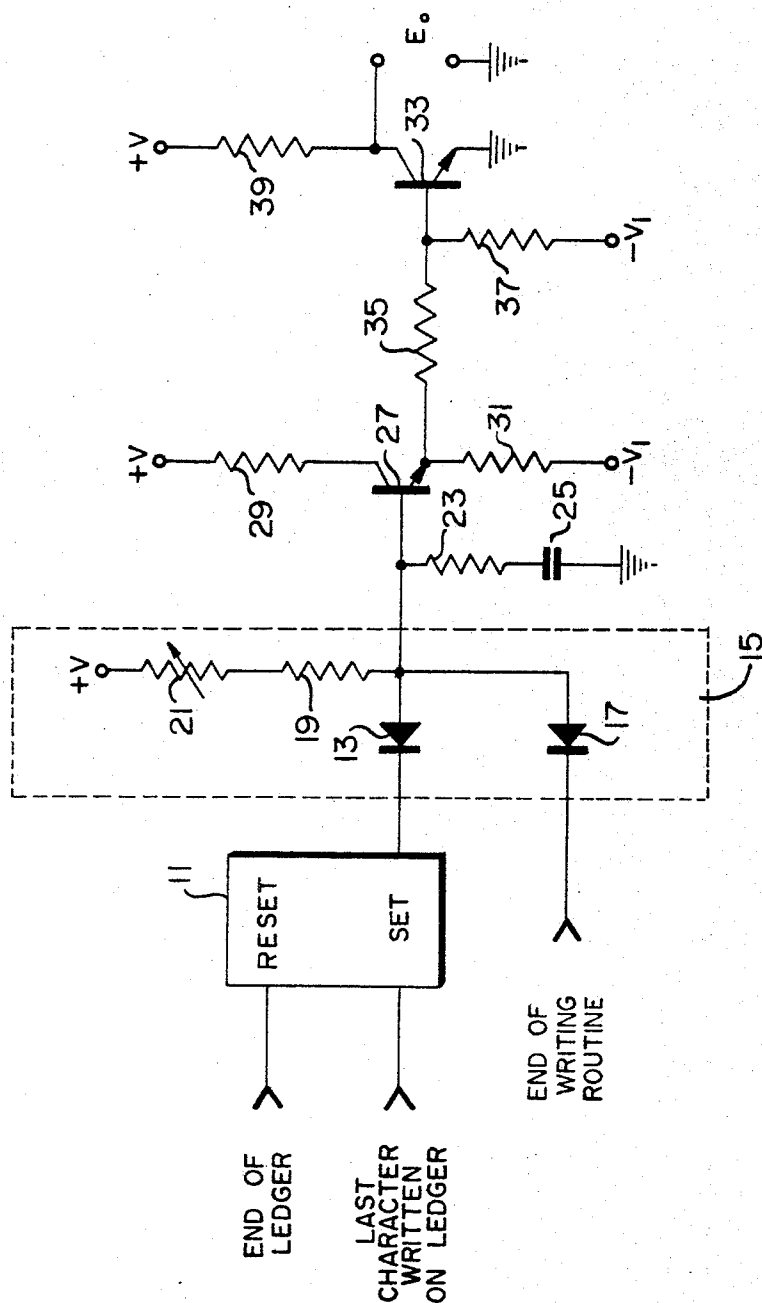
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TIME RESPONSIVE ERROR SIGNAL GENERATOR

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TIME RESPONSIVE ERROR SIGNAL GENERATOR
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1 Claim

ABSTRACT OF THE DISCLOSURE

This invention relates generally to circuits for checking the speed at which a ledger passes by a writing member of the printout portion of an accounting or data processing machine, and more particularly to timing circuits which produce an output if there is too long a time between the last character written on the ledger and the passage of the edge of the ledger, the distance between the last character and the edge of a ledger being known.

Since the advent of the computer, it has been becoming more and more the case in business that the accounting and record keeping operations, which previously had been performed by hand, are being handled with the aid of complex high speed accounting and data processing machines. It is necessary for these machines to have built-in error indicating devices to insure that the various portions of the machines are operating properly. Machines of this type operate at extremely high speeds and are able to process large numbers of documents and ledger cards very rapidly. It is therefore important that any malfunction be sensed as soon as it occurs, so that immediate steps can be taken to correct it before several documents or ledgers are improperly handled and perhaps ruined.

One such portion of the operation of the machine which must be kept at the proper level is the speed at which ledgers and documents move past the writing member of the machine. If the speed becomes too slow, the figures are likely to be crowded too close together, and, in the case of the magnetic writing heads, there is a loss of fidelity. Also, since the printout portion of a data processing machine is usually by far the slowest in operation, the entire machine must slow down, with a resulting loss of efficiency. It is relatively easy in most machines to keep track of the position on the ledger which the character is being printed, and thus the distance between the last character and the edge of the ledger is known. The speed at which the document is moving can be determined by measuring the time it takes for the edge of the document to pass by the writing member after the last character on the ledger is written. As long as the speed is above a predetermined level, the machine is operating properly. It is only when the speed falls below this minimum level that an error signal should be generated.

It is, therefore, an object of my invention to monitor the speed at which a ledger moves past the writing member of an accounting or a computing machine.

It is a further object of my invention to provide a circuit which generates a signal when the speed at which a ledger moves past the writing head falls below a specified level.

It is a further, more specific, object of my invention to generate an error signal when the speed at which a ledger moves past a writing member falls below a designated level by monitoring the time between the recording of the last character on the document and the passage of the edge of the ledger.

In carrying out these and other objects of my invention, I provide a circuit for monitoring the time between the printing of the last character on a ledger and the pas-

sage of the edge of the ledger. My circuit includes RC timing means coupled through current amplifying means to an output transistor for turning on the output transistor when the timing voltage reaches a predetermined level.

A two input AND gate clamps the timing circuit voltage below this level until signals are present at both inputs of the AND gate. A signal is generated at one input of the AND gate upon the end of the writing routine, and a signal is generated at the second input by the setting of a bistable multivibrator upon the writing of the last character on the ledger and removed by the resetting of the multivibrator upon the passage of the trailing edge of the ledger. If the speed at which the ledger is moving is above the minimum acceptable level, the multivibrator is reset by the passage of the edge of the ledger before the output transistor is triggered, thereby removing the input from the AND gate.

Various other objects, advantages, and features of my invention will become more fully apparent in the following specification with its appended claim and the accompanying drawing, in which the single figure is a schematic drawing of a checking circuit embodying my invention.

Referring now to the drawing, the output of multivibrator 11 is connected to the cathode of diode 13 of AND gate 15. The set input of the multivibrator is triggered upon the writing of the last character on the document and the reset input is triggered upon the passage of the edge of the ledger. A signal which is generated by the end of the writing routine is coupled to the cathode of diode 17 of AND gate 15. The anodes of diodes 13 and 17 are connected to the voltage source +V through resistor 19 and variable resistor 21. Timing capacitor 25 and resistor 23 are connected in series between the anodes of diodes 13 and 17 and ground. Resistors 19, 21, and 23, and capacitor 25 make up a series connected RC timing circuit. The junction of resistors 19 and 23 is connected to the base of emitter follower connected NPN transistor 27. The collector of transistor 27 is connected to voltage source +V through resistor 29 and the emitter is connected to voltage source -V₁ through resistor 31. The emitter of transistor 27 is also connected to the base of NPN transistor 33 through resistor 35. The base of transistor 33 is connected to voltage source -V₁ through resistor 37, and the collector of transistor 33 is connected to voltage source +V through resistor 39. The emitter of transistor 33 is grounded. The output signal E₀ from the circuit is taken between the collector of transistor 33 and ground.

In operation, ordinarily the voltage at the base of transistor 27 is clamped at a voltage close to ground level by diodes 13 and 17 of AND gate 15, so that the voltage at the emitter of transistor 27 is slightly below base level. Resistors 35 and 37, which are connected in series between the emitter of transistor 27 and voltage source -V₁, form a voltage divider which biases transistor 33 off.

When the end of the writing routine in the accounting machine or computer occurs, the voltage at the cathode of diode 17 of AND gate 15 becomes high. Next, the set input of multivibrator 11 is triggered when the last character is written on the ledger, thereby setting to a high state the multivibrator output which is connected to diode 13 of AND gate 15. Thus, both inputs to AND gate 15 become high, and the timing circuit voltage is no longer clamped at a low level. Capacitor 25 of the RC timing circuit commences charging from voltage source +V through resistors 19, 21, and 23. The voltage at the base of emitter follower connected transistor 27 rises at a rate determined by the time constant of the RC timing circuit, and the voltage at the emitter follows the base voltage in normal emitter follower fashion. As the volt-

age at the emitter of transistor 27 rises, the voltage at the base of transistor 33 also rises, due to the voltage divider effect of resistors 35 and 37.

If the ledger is not moving fast enough the voltage at the base of transistor 27 increases to a high enough level to forward bias the base of transistor 33, turning transistor 33 on and thereby generating an error signal which indicates that the ledger is moving too slowly. If however, the document is moving past the writing member at a high enough speed, the edge of the ledger passes by a sensing member (not shown) in time for a signal to be generated to reset multivibrator 11 before the timing circuit voltage becomes high enough to turn on transistor 33. The resetting of multivibrator 11 removes one of the input signals from AND gate 15, so that the output of the AND gate 15 becomes low again and the base of transistor 27 is clamped at a voltage below that necessary to turn on transistor 33. Timing circuit capacitor 25 discharges through diode 13 of AND gate 15, and no error signal is generated.

The input impedance to emitter follower connected transistor 27 is very high in comparison to the impedance of resistor 23 and capacitor 25, so that the shunting effect of transistor 27 has very little effect on the timing period of the RC timing circuit. Transistor 27 acts as a current amplifier which enables the timing circuit to turn transistor 33 on completely. The timing period of the circuit can be controlled by varying variable resistor 21.

An example of component values which have been found to be suitable for my circuit is listed below.

Component:	Value
Resistor 19	10K
Variable resistor 21	20K
Resistor 23	100
Capacitor 25	20
Resistor 29	100
Resistor 31	10K
Resistor 35	200
Resistor 37	47K
Resistor 39	2K

It is to be understood that this description is by way of illustration only, and, as will be obvious to one skilled

in the art, my circuit may be used in any machine handling sheets of paper where it is desired to monitor the speed of the paper. Further, it is to be understood that the word ledger, when used in the specification and claim, is intended to refer to any sheet of paper having any writing or punching operation performed on it, and is not limited to a single type of paper or operation.

I claim:

1. In a high speed system for recording characters on a sheet and having means for sensing an end of writing routine, the entry of a last character on the sheet and the passage of a trailing edge of the sheet through the recording area, a circuit for monitoring the speed of the sheet comprising:

gating means having an output during the enablement of two inputs and having a first input enabled by the sensing of the end of writing routine,

bistable means being set by the entry of the last character on the sheet and reset by the passage of the trailing edge of the sheet through the recording area, said bistable means having a set output operably connected for enabling the other input of said gating means,

a timing circuit for developing an increasing voltage during the output of said gating means, and

output means responsive to a predetermined voltage of said timing circuit for generating a signal when the speed of said sheet from the entry of said last character until the passage of the trailing edge through the recording area is less than a predetermined standard.

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