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(54) **PASSIVATION ASH/OXIDATION OF BARE COPPER**

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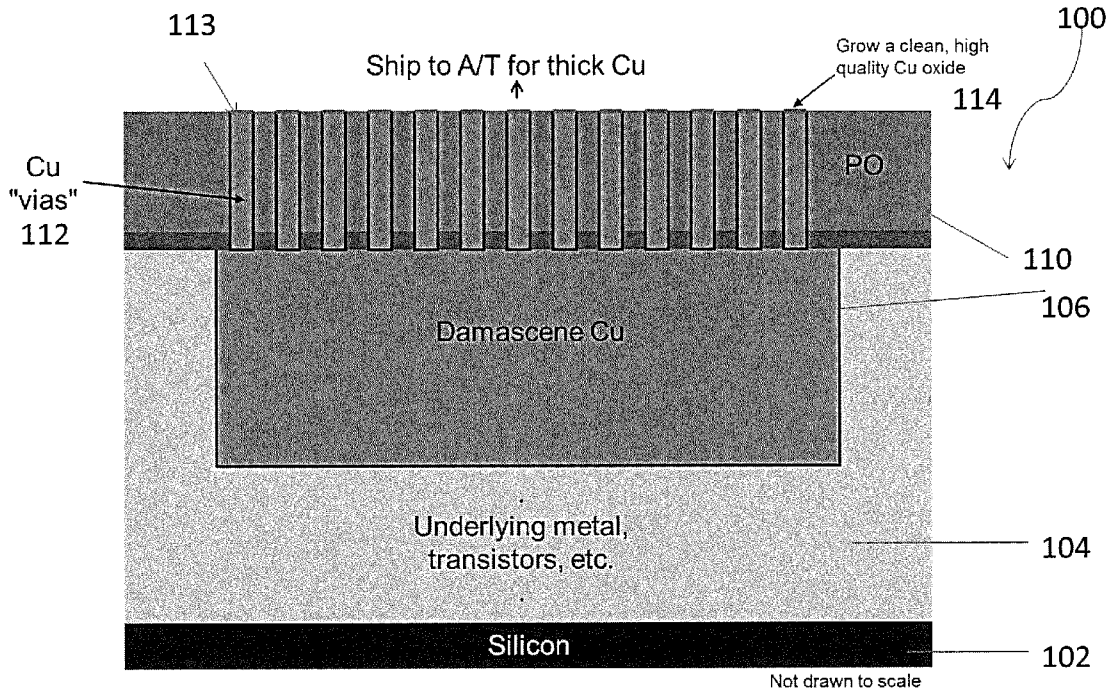
(57) **ABSTRACT**

A semiconductor wafer has a clean, high quality Cu oxide formed at the surface of exposed Cu when an extended non-fabrication process time (such as shipping to an assembly/test site or prolonged storage) is expected.



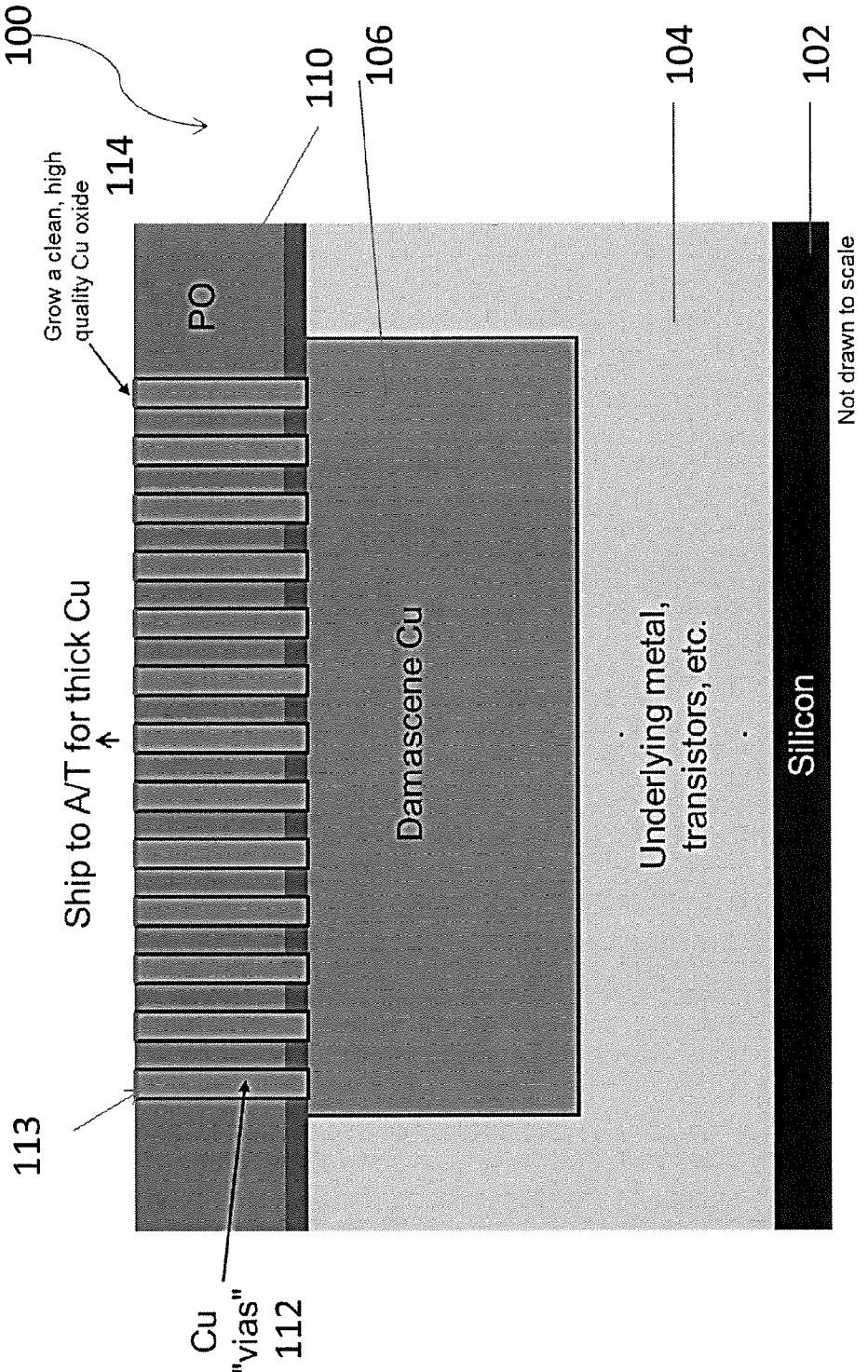

100
110
106
104
102
114
Grow a clean, high quality Cu oxide
PO
Ship to A/T for thick Cu
Damascene Cu
Underlying metal, transistors, etc.
Silicon
Not drawn to scale
113
Cu "vias" 112

FIG. 1

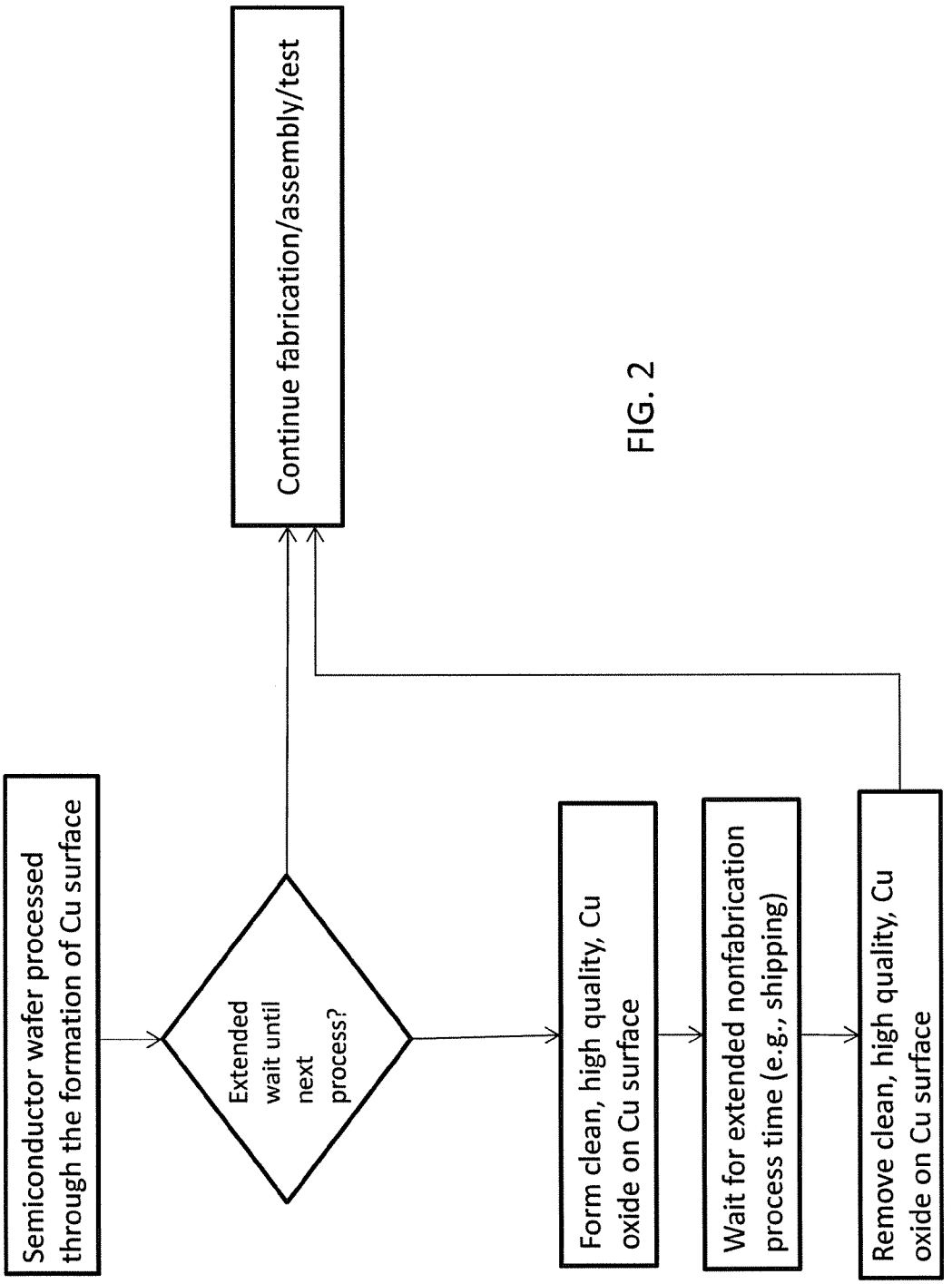

Semiconductor wafer processed through the formation of Cu surface
Extended wait until next process?
Continue fabrication/assembly/test
Form clean, high quality, Cu oxide on Cu surface
Wait for extended nonfabrication process time (e.g., shipping)
Remove clean, high quality, Cu oxide on Cu surface

FIG. 2

PASSIVATION ASH/OXIDATION OF BARE COPPER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority under U.S.C. §119(e) of U.S. Provisional Application 61/908,283 (Texas Instruments docket number TI-72691 PS, filed Nov. 25, 2013), hereby incorporated by reference.

FIELD OF THE INVENTION

[0002] The invention is generally related to the field of fabricating integrated circuits and more specifically to a passivation ash of exposed copper at a surface of an integrated circuit.

BACKGROUND OF THE INVENTION

[0003] The fabrication of integrated circuits often involves semiconductor device and interconnect fabrication on a wafer scale at one site (a semiconductor fab) and packaging of individual die at another site (assembly/test site). Conventionally, an aluminum capping layer is used as the top metal of the wafer. The surface of the aluminum capping layer remains stable when shipping the wafers from the fab to the assembly/test site.

SUMMARY OF THE INVENTION

[0004] It is desirable to ship wafers having exposed Cu on the surface to assembly/test sites. In accordance with an embodiment of the application, a semiconductor wafer has a clean, high quality Cu oxide formed at the surface of exposed Cu when an extended non-fabrication process time (such as shipping to an assembly/test site or prolonged storage) is expected.

[0005] An advantage of the invention is preventing corrosion of the exposed Cu surface.

[0006] This and other advantages will be apparent to those of ordinary skill in the art having reference to the specification in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] In the drawings:

[0008] FIG. **1** is a cross-sectional diagram of a semiconductor wafer having a clean, high quality Cu oxide according to an embodiment; and

[0009] FIG. **2** is a flow diagram of a method according to an embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0010] Integrated circuit die are fabricated on a semiconductor wafer. When Cu metallization is used, Cu is exposed at the surface at various points in the process. When Cu is exposed for extended periods of time, natural oxidation of the Cu occurs. Unfortunately, this native Cu oxide is of poor quality and is non-uniform. In addition, other contaminants can collect on the Cu surface for example from poor air quality, outgassing from shipping container plastics, etc. The non-uniform native Cu oxide and other contaminants can result in corrosion and yield loss as well as poor adhesion and poor ohmic connections in subsequent processing/assembly/test.

[0011] An embodiment will now be described in conjunction with an integrated circuit fabrication process. The embodiment may be applied to other integrated circuit fabrication processes involving Cu that may be exposed for an extended time such as Cu bond pads or Cu interconnect lines.

[0012] Referring to FIGS. **1** and **2**, an integrated circuit **100** is formed using a semiconductor wafer **102**. Transistors and other devices as well as various metal interconnect levels (shown collectively as **104**) are formed on wafer **102**. A Cu interconnect structure **106** is formed, for example using a damascene process, over the underlying structures **104**. A protective overcoat **110** is formed over the Cu **106**. Vias are formed in the protective overcoat and filled with Cu, forming Cu vias **112**. Although FIG. **1** shows Cu surface **113** as being the surface of Cu vias extending through a protective overcoat **110**, Cu surface **112** could be any Cu surface that may be exposed for an extended period of time.

[0013] If the Cu surface **113** would otherwise be exposed for an extended time (e.g., greater than 1 day), a clean, high quality Cu oxide **114** is formed on the Cu surface **113**. For example, an O_2 ash may be performed. An O_2 ash will burn off any contaminants already on the Cu surface and allow a pure Cu oxide **114** to form. The Cu oxide may be in the range of 20-100 Å thick. Cu oxide **114** differs from a natively grown oxide in that it is cleaner (contains less contaminants) and more uniform.

[0014] Cu oxide **114** protects the Cu surface **113** for the extended period of time until subsequent fabrication steps are performed (extended non-fabrication process time). For example, Cu oxide **114** may protect the Cu surface **113** during shipment from a wafer fabrication facility to an assembly/test facility. Alternatively, the extended non-fabrication process time may be a time in which the processed wafers are placed in storage.

[0015] After the extended non-fabrication process time, the Cu oxide **114** may be removed prior to further processing steps such as packaging. Cu oxide **114** may be removed using an H_2-based plasma. Sulfuric acid or citric acid cleans may also be used. Other acids with low etch rate of Cu and the surrounding dielectrics could alternatively be used. Alternatively, diluted HF could be used to remove the Cu oxide and not attack the PO too much. Further processing/assembly/test is then undertaken.

[0016] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

1. A method of fabricating an integrated circuit, comprising the steps of:

processing a semiconductor wafer through the formation of a protective overcoat at a wafer fabrication facility;

forming copper vias through the protective overcoat;

forming a copper oxide on a surface of the copper vias, wherein the cooper oxide is a clean, high quality copper oxide;

shipping the semiconductor wafer from the wafer fabrication facility to an assembly/test facility;

removing the copper oxide at the assembly/test facility; and

packaging the integrated circuit.

2. The method of claim **1**, wherein forming the copper oxide comprises a performing an O_2 ash.

3. The method of claim **2**, wherein the copper oxide is in the range of 20 ÅA-100 Å thick.

4. The method of claim **2**, wherein the step of removing the copper oxide comprises an H_2 plasma.

5. The method of claim **2**, wherein the step of removing the copper oxide comprises exposing the copper oxide to sulfuric acid.

6. The method of claim **2**, wherein the step of removing the copper oxide comprises exposing the copper oxide to citric acid.

7. A method of fabricating an integrated circuit, comprising the steps of:

processing a semiconductor wafer through the formation of at least one copper interconnect level such that the semiconductor wafer has a copper surface exposed;

forming a clean, high quality copper oxide on the copper surface;

performing no process steps on the semiconductor wafer for an extended period of time;

then, removing the copper oxide; and

then, packaging the integrated circuit.

8. The method of claim **7**, wherein forming the copper oxide comprises a performing an O_2 ash.

9. The method of claim **8**, wherein the extended period of time is greater than one day.

10. The method of claim **8**, wherein the step of performing no process steps comprises shipping the semiconductor wafer from a wafer fabrication facility to an assembly/test facility.

11. The method of claim **8**, wherein the step of performing no process steps comprises placing the semiconductor wafer in storage.

12. The method of claim **8**, wherein the step of removing the copper oxide comprises an H_2 plasma.

13. The method of claim **8**, wherein the step of removing the copper oxide comprises exposing the copper oxide to sulfuric acid.

14. The method of claim **8**, wherein the step of removing the copper oxide comprises exposing the copper oxide to citric acid.

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