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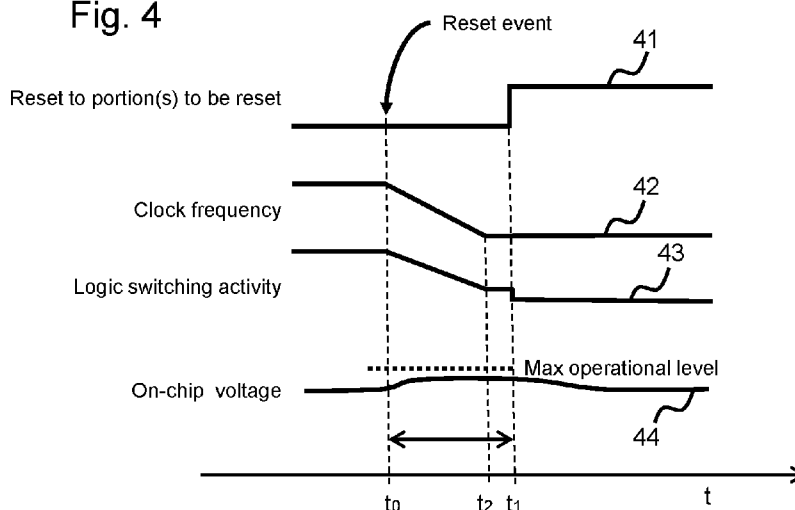
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85604 Zorneding (DE).(81) Designated States (unless otherwise indicated, for every
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BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
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(54) Title: METHOD OF RESETTING A PROCESSOR

Fig. 4



(57) Abstract: The invention relates to a method of resetting a processor, the method comprising the receiving of a reset signal indicating that one or more parts (51, 52) of said processor need to be reset, and forwarding of said reset signal to said parts (51, 52) to be reset. The forwarding of the reset signal is delayed for a period of time for at least one of the parts (51) to be reset. The clock frequency of at least one of the parts to be reset is gradually decreased during said period of time. In this way the total activity of the processor device is gradually decreased so as to avoid an on-chip voltage overshoot, which could cause a total reset of all the parts of the processor.

Title : Method of resetting a processor**Description**Field of the invention

This invention relates to a method of resetting a processor and to a processor comprising multiple processor parts. It also relates to an integrated circuit comprising such a processor.

Background of the invention

In a typical microcontroller a reset scheme will be implemented whereby on receiving of a particular event the microcontroller will be reset. In more intelligent systems this scheme may be split into separate levels of reset, some of which may require that a portion of the chip still be functional during the reset.

The limitation is that this former type of reset may cause a voltage overshoot beyond the operational range of the chip due to the sudden drop in switching activity caused by clock frequency reduction (or stopping) and large portions of the logic being held in their reset state. The follow-on result is that a more severe level of reset may be triggered by this voltage overshoot, thus eliminating the advantages of having less severe levels of reset and making it difficult for software to determine the original cause of the reset.

The phenomenon described above has already been observed on 90 nm CMOS devices, and the trend towards smaller technologies and more cores on single chips is making the problem more acute. A solution that is currently used is a very cumbersome software sequence.

Summary of the invention

The present invention provides a method of resetting a processor as described in the accompanying claims. There is also provided a processor comprising multiple processor parts and a reset controller, and an integrated circuit comprising such a processor.

Specific embodiments of the invention are set forth in the dependent claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

Further details, aspects and embodiments of the invention will be described, by way of example only, with reference to the drawings. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

Figure 1 shows a state diagram of a processor device reset sequence according to the state of the art;

Figure 2 shows graphs of a reset signal, a clock frequency, a switching activity and an on-chip voltage according to the state of the art;

Figure 3 shows a state diagram of a processor device reset sequence according to an embodiment;

Figure 4 shows graphs of an example of a reset signal, a clock frequency, a switching activity and an on-chip voltage according to an embodiment;

Figure 5 schematically shows an example of a processor according to an embodiment;

Figure 6 shows a flow chart of the method according to an embodiment;

Figure 7 shows an integrated circuit according to an embodiment.

Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. In the Figures, elements which correspond to elements already described may have the same reference numerals.

Detailed description of the preferred embodiments

Figure 1 shows a state diagram of a processor device reset sequence according to the state of the art. This typical reset sequence 11, 12, 13 is as follows. When a reset event occurs while the processor device is not in reset, the reset sequence is entered based on the reset event's severity, see RST_A, RST_B, RST_C, where in RST_A portions x, y, z are in reset, and in RST_B portions y, z are in reset, and in RST_C only portion z is in reset.

Immediately upon entering the reset sequence 11, 12, 13 the reset of the "to be reset" portion(s) of the processor device occurs, and the clock frequency is reduced or even stopped. As the reset sequence progresses, some portions of the device may be released from reset at each step, until finally the last step is exited, and the entire chip is not in reset, see state 14. If a new reset event with a higher severity occurs while the reset sequence is active, the reset sequence may return to a prior step based on the event's severity. These possible returns are indicated in Figure 1 by dashed lines.

Figure 2 shows graphs of a reset signal 21, a clock frequency 22, a switching activity 23 and an on-chip voltage 24 according to the state of the art. The example of Figure 2 may be the result of a processor device being reset by the scheme described with reference to Figure 1. As can be seen from Figure 2, due to the reset at $t=t_0$, the switching activity is immediately reduced causing a temporary voltage overshoot beyond the maximum operational level, see dotted line in Figure 2. This may result in a more severe level of reset being triggered, which is not wanted.

Figure 3 shows a state diagram of a processor device reset sequence according to an embodiment. In this example the reset sequence 31, 32, 33 is as follows. When a reset event occurs while the chip is not in reset, the new "RST_WAIT" state 35 is entered. During RST_WAIT, the portion that is to receive the delayed reset is not reset yet, but the rest is reset as per the target state RST_A, RST_B, or RST_C. Possibly an isolation between parts to be reset and parts not to be reset is activated. Furthermore a clock frequency ramp-down procedure is executed. When clock frequency ramp-down has completed, the 'usual' reset sequence 31, 32, 33 is entered at the step based on the original reset event's severity. If a new reset event occurs while in the processor

device is in "RST_WAIT" state, the reset event with the highest severity determines at which step (i.e. 31, 32 or 33) the 'usual' reset sequence is entered.

Figure 4 shows graphs of an example of a reset signal 41, a clock frequency 42, a switching activity 43 and an on-chip voltage 44 according to an embodiment. The example of Figure 4 may be the result of a processor device being reset by the scheme described with reference to Figure 3. As can be seen from Figure 4, due to the receiving of a reset signal at $t=t_0$, the clock frequency 42 is gradually reduced. On the occurrence of a reset event, the actual reset of the 'to be reset' portion of the chip is delayed until after the clock frequency 42 has been ramped down to a 'reset frequency'. During this time, the portion of the chip that is to be reset is optionally isolated from the portion of the chip that is not to be reset so that this latter portion cannot be negatively impacted by the reset. Once the clock frequency 42 has completed its ramp-down, the portion of the chip that is to be reset is actually reset, see $t=t_1$, and the reset sequence can proceed as usual. As can be seen in the example of Figure 4, the forwarding of the reset is performed later than the actual moment (i.e. at t_2) on which the frequency ramp-down has been completed. The time between t_2 and t_1 is simply the time it takes for a reset state machine to progress to the next state in which the reset is asserted. In principle, it could be immediate, too.

Figure 5 schematically shows an example of a processor 60 according to an embodiment. The processor 60 comprises multiple processor parts 51, 52, 53 and a reset controller 54. The processor parts may be processor cores of a multicore processor or any other parts of a processor, such as memory. The parts are powered by a voltage regulator 49, via power lines 50. The reset controller 54 is arranged for receiving a reset signal 55 indicating that one or more of the processor parts 51, 52 need to be reset. The reset controller 54 will forward the reset signal to the parts to be reset; in this example parts 51 and 52. In this example, the received reset signal is immediately forwarded to the first part 51, via signal line 56. The forwarding of the reset is delayed for a period of time for the second part 52, and sent via signal line 57. The third part 53 in this example will not be reset.

The processor 60 further comprises a frequency adapter 58 for gradually decreasing a clock frequency of the at least one of the parts to be reset. The frequency adapter 58 may comprise a ramp down control unit 59 arranged to control the gradually decreasing of the clock frequency, and a fractional clock divider 61 arranged to receive a control signal from said ramp down control unit 59, and to divide a clock signal received from a clock source. Figure 5 shows some further blocks representing the system clock generation. The clock generation may comprise one or more clock sources 64, 65 (e.g., crystal oscillator, internal RC oscillator, PLL). Figure 5 shows two clock sources, but it could be one or more. A multiplexer 66 is shown arranged for selecting which clock source 64, 65 is to be used as the system clock. Output of the multiplexer 66 is fed to the fractional clock divider 61 of the frequency adapter 58. It is noted that instead of using a fractional clock divider, any other mechanism to reduce the clock frequency gradually may be used.

Instead of directly resetting one or more parts, e.g. the part 51, and delaying the reset for others, e.g. the part 52, the reset controller 54 may be arranged to delay the forwarding for a period of time for all of the parts to be reset, thus the parts 51 and 52.

In the embodiment shown in Figure 5, part 53 receives its clock frequency direct from a multiplexer 66, since there is no need to ramp down the frequency for this part. It should be noted that in a more dynamic variant, the third part 53 could receive its frequency also from the frequency adapter 58, in case the third part 53 needs to be reset in some other circumstances. So the frequency adapter 58 may be arranged to ramp down the frequency for certain parts, while delivering a normal frequency (i.e. produced by the multiplexer 66) to those parts that will not be reset.

In the embodiment of Figure 5, the reset controller 54 is arranged to send an initialisation signal to the ramp down control unit 59 to initiate a frequency ramp down. Once the frequency ramp down has been completed, the ramp down control unit 59 will send a signal back to the reset controller 54 so that the delayed reset can be asserted. The delay time depends on the time it takes to ramp down the clock frequency, and this in turn may depend on an initial clock frequency, a maximum logic switching load, and voltage regulator/power supply response characteristics. In an embodiment, the forwarding of the reset signal is delayed for a predefined period of time. The predefined period of time may be defined for each of said parts to be reset.

In an embodiment the delay time may be longer for some parts than for other parts. For example, the reset controller 54 may be arranged to delay the forwarding of the reset signal in a consecutive way, wherein the forwarding of the reset signal is delayed for a first period of time for a first part and for a second period of time for a second part, wherein the first period of time is shorter than said second period of time. The forwarding of the reset signal may as well be delayed for a third part for a third period of time, where the third period of time is longer than the second period of time. In such an embodiment, a first part may for example be reset after a time $t=2\text{msec}$, a second part after $t=3\text{msec}$ and a third part after 4 msec. In this way also the total activity of the processor device is gradually decreasing to avoid an on-chip voltage overshoot.

In the embodiment shown in Figure 5, the processor further comprises a plurality of isolation units 71, 72, 73, 74 arranged to avoid signals going between different parts 51, 52, 53 of the processor. The processor may comprise an isolation controller arranged to activate the isolation units 71, 72, 73, 74. In this example the isolation controller is integrated in the reset controller 54, but the isolation controller may be a separate module in communication with the reset controller 54.

The isolation controller will send a control signal via signal lines, see dashed lines 76, to the different isolation units 71, 72, 73, 74. Once a reset signal for a specific processor part is received by the reset controller 54, an isolation control signal may be sent to those isolation units that can isolate the part to be reset from the other parts in communication with the part to be reset. This isolation will avoid that those parts not to be reset will negatively be impacted by the parts to be reset, especially during the clock frequency ramp-down time.

The frequency adapter 58 may be arranged to receive a clock signal from a clock source 65 and instructions from the reset controller 54. The frequency adapter 58 may be arranged to divide the clock frequency.

The embodiments described above allow the manipulation of the reset to a portion of the processor in conjunction with the frequency adapter 58 to prevent voltage overshoots due to sudden drop in frequency and switching activity on reset sequence entry. The solution can be implemented entirely with digital logic. An increase in availability of the processor parts is realized by preventing a less severe reset event, which would normally result in a quite short reset sequence, from resulting in a much longer reset sequence triggered by a high voltage detection.

The delay on the reset may be applied for all resets including both hardware and software reset events except a power on reset (POR) rather than only on software triggered resets. Also, the delay may be controlled by the frequency adapter operation in order to minimize impact on the voltage regulator 49 rather than, for example, the storing of data/configuration content prior to power-down.

Figure 6 shows a flow chart of the method according to an embodiment. The method 80 comprises the receiving of a reset signal indicating that one or more parts of the processor need to be reset, see step 81. The next step is a step 82 in which a clock frequency of at least one of the parts to be reset is gradually decreased during a period of time. The next step is a step 83 comprising the forwarding of the reset signal to parts to be reset.

So there is provided a method of resetting a processor, the method comprising the receiving a reset signal, see signal 55, indicating that one or more parts 51, 52 of said processor need to be reset, and forwarding of the reset signal to the parts 51, 52 to be reset, wherein the forwarding of the reset signal is delayed for a period of time for at least one of the parts 52 to be reset. A clock frequency of the at least one of the parts to be reset during this period of time is gradually decreased.

By using a combination of slow clock frequency ramp-down and delayed or staggered reset assertion in order to ensure that the logic switching activity is reduced slowly enough, the rate of change in the current drawn by that logic is small enough to be compensated by the power supply and/or voltage regulator. This prevents an overshoot of the on-chip voltage beyond the operational maximum voltage.

The forwarding of the reset signal may be delayed for the period of time for all of the parts 51, 52 to be reset. The method as described may further comprise the isolating of the parts to be reset by way of blocking processing signals from and to other parts of the processor that are not to be reset. The isolating of the parts to be reset may be done before the parts to be reset are in reset state. The one or more parts may comprise at least one processor core. The parts may also be any other type of logic or memory element.

Figure 7 shows an integrated circuit 90 according to an embodiment. The integrated circuit 90 may comprise the processor 60 according to one or more of the embodiments described above.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the scope of the invention as set forth in the appended claims. For example, the connections may be any type of connection suitable to

transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise the connections may for example be direct connections or indirect connections.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

Thus, it is to be understood that the architectures depicted herein are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In an abstract, but still definite sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements or steps than those listed in a claim. Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. A method (80) of resetting a processor, the method comprising:
 - receiving (81) a reset signal indicating that one or more parts of said processor need to be reset,
 - gradually decreasing (82) a clock frequency of said at least one of the parts to be reset;
 - forwarding (83) of said reset signal to said parts to be reset, wherein said forwarding of said reset signal is delayed for a period of time for said at least one of the parts to be reset.
2. A method according to claim 1, wherein said forwarding of said reset signal is delayed until after said clock frequency has been decreased to a reset frequency.
3. A method according to claim 1, wherein said forwarding of said reset signal is delayed for a predefined period of time.
4. A method according to claim 3, wherein said predefined period of time is defined for each of said parts to be reset.
5. A method according to claim 1, wherein said forwarding of said reset signal is delayed for said period of time for all of the parts (51, 52) to be reset.
6. A method according to any of the preceding claims, wherein said forwarding of said reset signal is delayed for a first period of time for a first part (51) and for a second period of time for a second part (52), wherein said first period of time is shorter than said second period of time.
7. A method according to claim 6, wherein said forwarding of said reset signal is delayed for a third part (53) for a third period of time, said third period of time being longer than said second period of time.
8. A method according to any of the preceding claims, said method further comprising:
 - isolating said parts to be reset by way of blocking processing signals from and to other parts of said processor that are not to be reset.
9. A method according to claim 8, wherein said isolating of said parts to be reset is done before said parts to be reset are in reset state.
10. A method according to any of the preceding claims, wherein said one or more parts comprise at least one processor core.

11. A processor (60) comprising multiple processor parts (51, 52, 53) and a reset controller (54) arranged for:

- receiving a reset signal indicating that one or more parts (51, 52) of said processor parts (51, 52) need to be reset;
- forwarding of said reset signal to said parts to be reset;
- delaying said forwarding for a period of time for at least one of the parts (51) to be reset, said processor further comprising a frequency adapter (58) for gradually decreasing a clock frequency of said at least one of the parts to be reset.

12. A processor according to claim 11, wherein said frequency adapter (58) comprises a ramp down control unit (59) arranged to control said gradually decreasing of said clock frequency, and a fractional clock divider (61) arranged to receive a control signal from said ramp down control unit, and to divide a clock signal received from a clock source.

13. A processor according to claim 11 or 12, wherein said reset controller (54) is arranged to delay the forwarding for said period of time for all of the parts (51, 52) to be reset.

14. A processor according to any of claims 11-13, wherein the said period of time is longer for some parts than for other parts.

15. A processor according to any of claims 11-14, wherein said reset controller (54) is arranged to delay said forwarding of said reset signal in a consecutive way.

16. A processor according to any of claims 11-15, wherein the frequency adapter (58) is arranged to ramp down the frequency for certain parts, while delivering a normal frequency to those parts that will not be reset.

17. A processor according to any of claims 11-16, said processor further comprising:

- a plurality of isolation units (71, 72, 73, 74) arranged to avoid signals going between different parts of said processor;
- an isolation controller (54) arranged to activate said isolation units.

18. A processor according to any of claims 11-17, wherein said frequency adapter (58) is arranged to receive a clock signal from a clock source (64, 65, 66) and instructions from said reset controller (54) and arranged to divide said clock frequency.

19. An integrated circuit comprising a processor according to any of claims 11-18.

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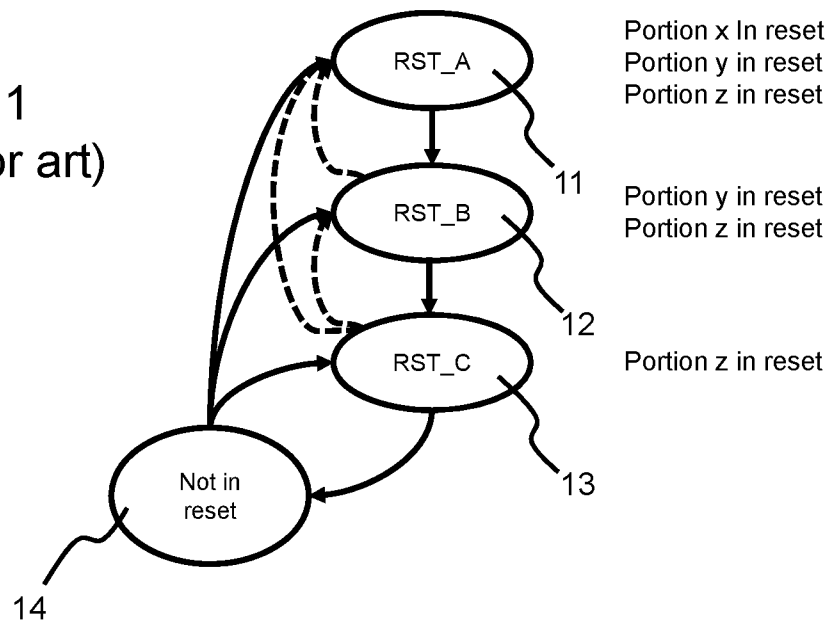
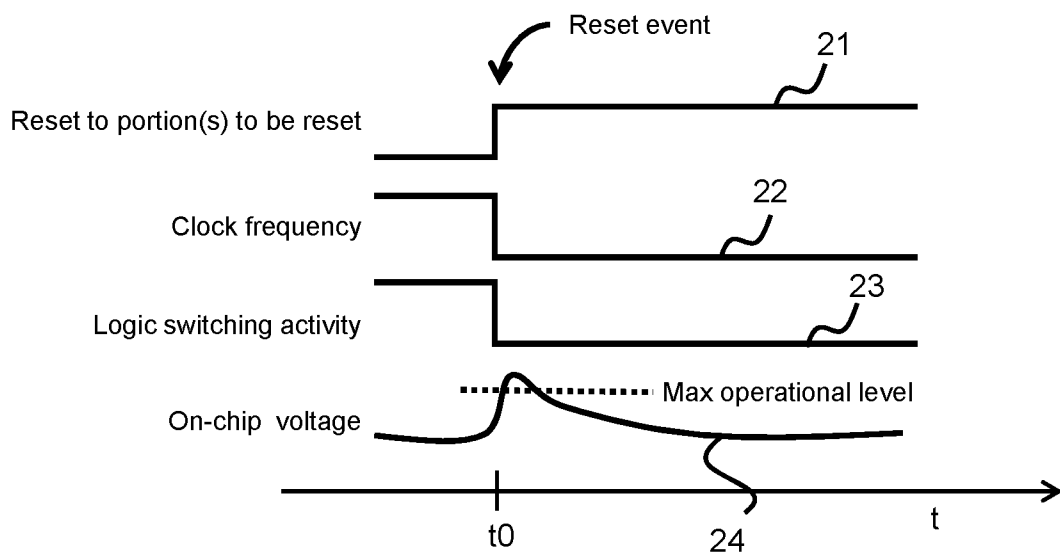
Fig. 1
(prior art)

Fig. 2 (prior art)



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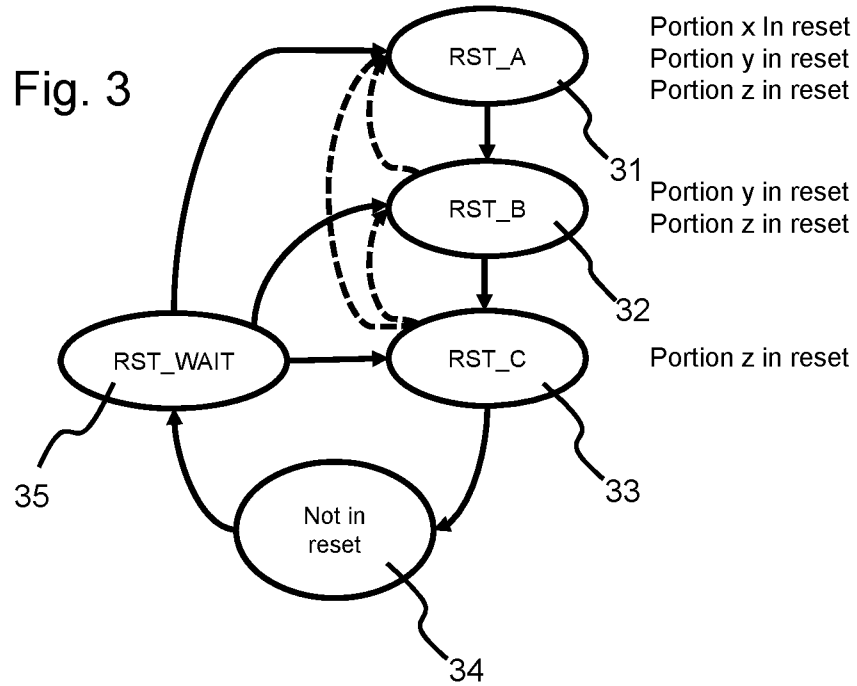
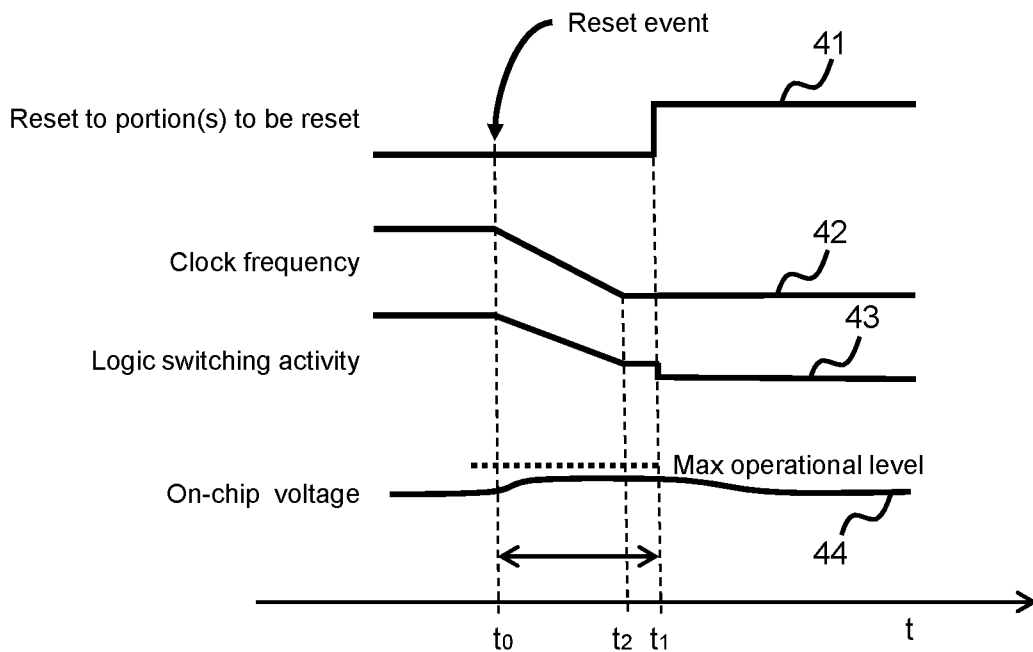
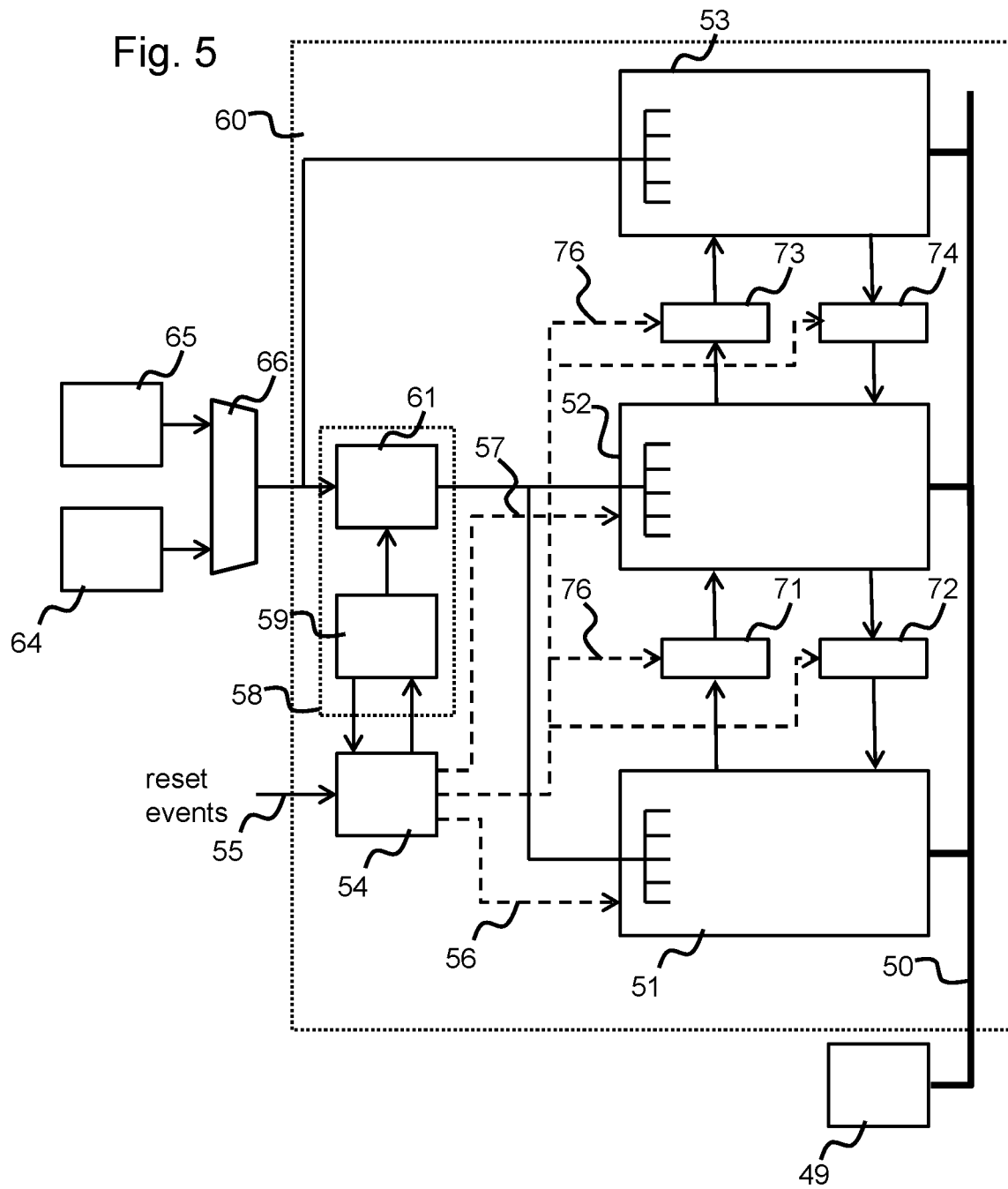


Fig. 4



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Fig. 5



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Fig. 6

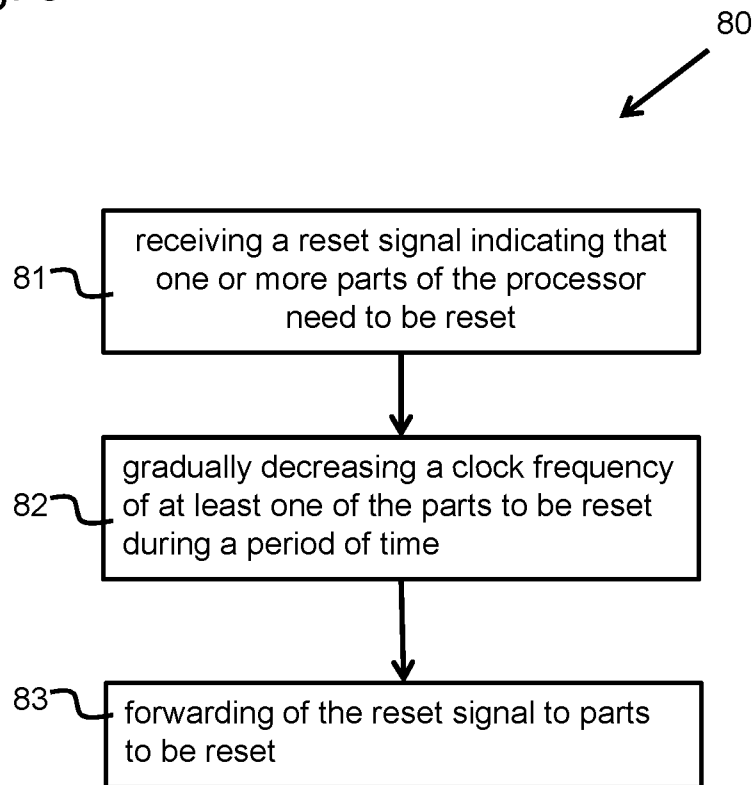
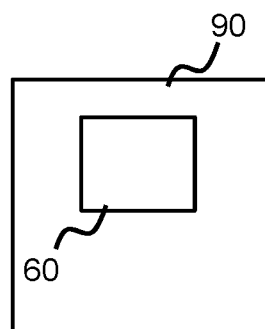


Fig. 7



INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2014/059964**A. CLASSIFICATION OF SUBJECT MATTER****G06F 1/24(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/24; H03L 7/00; G01R 23/02; G06F 1/04; G11C 11/4072; G06F 1/32; G06F 15/177; G11C 11/4076

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: reset, processor, clock frequency, delay, period

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006-0103436 A1 (TERUHIKO SAITOU) 18 May 2006 See paragraphs [0059]-[0068]; claims 1, 19; and figure 5.	1-7, 11-13
Y	JP 2000-066760 A (NEC KOFU LTD.) 03 March 2000 See abstract; paragraphs [0013]-[0019]; claims 1-2; and figures 1-2.	1-7, 11-13
A	US 2006-0112263 A1 (HSIU-MING CHU et al.) 25 May 2006 See paragraph [0016]; and figure 3.	1-7, 11-13
A	US 6118306 A (JOHN T. ORTON et al.) 12 September 2000 See abstract; column 8, line 32 - column 9, line 22; claim 1; and figure 6.	1-7, 11-13
A	KR 10-2009-0046091 A (HYNIX SEMICONDUCTOR INC.) 11 May 2009 See paragraphs [0024]-[0030]; and figure 2.	1-7, 11-13



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 August 2014 (21.08.2014)

Date of mailing of the international search report

21 August 2014 (21.08.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2014/059964

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 9
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
The claim 9 does not comply with PCT Article 6 because it is referring to unsearchable claim 8.

3. ☒ Claims Nos.: 8,10,14-19
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/IB2014/059964

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