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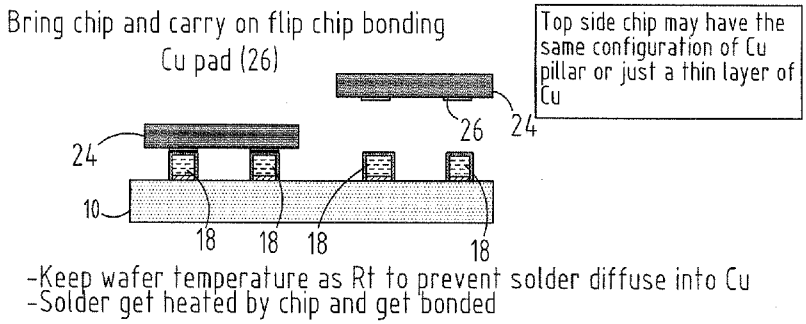


FIG. 8

(57) Abstract: A method for chip on wafer bonding is provided. The method includes the formation of a plurality of posts on at least one of a chip and a wafer, and a like plurality of contacts on the other of the chip and the wafer. After formation, a contact surface of each post is planarized, the respective planarized contact surface having a surface roughness height. A bonding material is then applied to at least one of the chip in a thickness no greater than the surface roughness height of the contact surface. The posts are then temporarily bonded to the contacts using the bonding material to stabilize a position of the chip relative to the wafer for permanent diffusion bonding of the chip to the wafer.

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Description

Title of Invention: A METHOD FOR BONDING A CHIP TO A WAFER

Technical Field

[0001] The present disclosure provides a method for bonding one or more chips to a wafer.

Background Art

[0002] Using conventional methodologies, a chip on wafer (CoW) bonding process involves the formation of copper (Cu) pillars on either the chip or the wafer, or both, before the chip is bonded to the wafer. If one of the chip and wafer does not include Cu pillars, it is instead provided with a Cu pad for bonding to the Cu pillars of the other of the chip and wafer. For simplicity, the following discussion will be limited to arrangements where there are pairs of opposing Cu pillars – i.e. the chip and wafer each have Cu pillars, with each Cu pillar of the chip aligning with a unique Cu pillar of the wafer – though the same discussion applies when bonding a Cu pillar to a Cu pad.

[0003] Each Cu pillar consists of a Cu post and a solder cap. The solder cap is typically applied using electroplating, followed by a reflow process to round the cap. During bonding, the solder caps of the chip melt and react with solder caps of the wafer to permanently fix the chip to the wafer.

[0004] The Cu pillars vary in height. This is the result of variance in the height of the Cu post and, or alternatively, the solder cap. As a consequence, thick solder caps are used, since solder deforms easily when melted, and pressure is usually applied to urge the chip against the wafer to ensure each Cu pillar meets and bonds with an opposing Cu pillar. This pressure can squeeze solder between the opposing Cu pillars. If the solder volume is large and the separation between Cu pillars (the "pitch") is small, spreading solder can bridge neighbouring Cu pillars.

[0005] Despite this, there are many reasons why thick solder caps are considered unavoidable in conventional CoW processes. Flip chip bonding – a process that can permanently bond a chip to a wafer in a single step – requires thick solder caps to ensure there is sufficient solder on each of the chip and wafer so that opposing Cu pillars can bond through formation of an intermetallic alloy between the opposing pillars.

[0006] In addition, a thick solder cap is considered useful since the solder of a Cu pillar diffuses into the Cu post at elevated temperatures. This diffusion reduces the amount of available solder for the bonding process. Also, to form a smooth solder cap using a reflow process – the smoothness being necessary to ensure proper bonding and to reduce the impact of Cu pillar height variation – a relative thick minimum thickness is usually required.

[0007] It would be useful to provide a method that avoids the need for the thick solder caps, and thereby mitigates the potential for bridging.

Summary of Invention

[0008] The present invention provides a method for chip on wafer bonding, comprising forming a plurality of posts on at least one of a chip and a wafer, and a like plurality of contacts on the other of the chip and the wafer; planarizing a contact surface of each post, the planarized contact surface having a surface roughness height; applying, to at least one of the chip and the wafer, a bonding material of a thickness no greater than the surface roughness height; temporarily bonding the posts to the contacts using the bonding material to stabilize a position of the chip relative to the wafer for permanent diffusion bonding of the chip to the wafer.

[0009] The method may further include the step of permanently bonding the chip to the wafer by diffusion of the posts and contacts into each other.

[0010] The present invention also provides an integrated chip formed using the method described above.

[0011] The term "surface roughness height", and similar, refer to the difference in height between the lowest point on a surface and the highest point on the surface. In the present case, the lowest point of a contact surface of a post on a wafer or chip is the point on that contact surface that is closest to the wafer or chip. Conversely, the highest point of a contact surface of a post on a wafer or chip is the point on that contact surface that is furthest from the wafer or chip.

[0012] The term "temporary integrated chip" refers to a chip and wafer that have been temporarily bonded in advance of being permanently bonded.

[0013] The term "temporarily bonding", "temporarily bonded", and similar, refer to a condition in which the contact surface of a post is only partially bonded to an opposing contact. In other words, across the contact surface of the post there are regions in which the post is bonded to the opposing contact and regions where it is not, such that a reliable electrical connection has not been formed.

[0014] The term "opposing contact", "opposing post", and similar, identify, for a post or contact on one of the chip and wafer, the post or contact on the other of the chip and wafer to which it will be bonded.

[0015] The term "contact surface" refers to the surface of a contact (e.g. a post) that is to be bonded to an opposing contact.

[0016] The phrase "do not oxidise", and similar, when used in the context of the oxidation of contacts or posts, means that for the time up to when the contacts or posts are bonded with opposing contacts, the contact surfaces or posts remain substantially unoxidised.

[0017] The term "low melting point metal", and similar, will be understood to mean a metal having a lower melting point than the material from which the contacts of the chip and wafer are fabricated. In embodiments described herein, the contacts are formed from Cu, aluminium (Al) or gold (Au), and the bonding material is formed from a lower melting point metal such as tin (Sn), indium (In), lead (Pb) or bismuth (Bi).

Brief Description of Drawings

[0018] Some embodiments of the present method will now be described, by way of non-limiting example only, with reference to the accompanying drawings in which:

[0019] Figure 1 is a side view of a wafer on which a Cu seed layer has been deposited;

[0020] Figure 2 is a side view of the wafer of Figure 1, with a photoresist layer in place;

[0021] Figure 3 is a side view of the wafer of Figure 2, after post deposition;

[0022] Figure 4 is a side view of the wafer of Figure 3, after planarization;

[0023] Figure 5 is a side view of the wafer of Figure 4, after removal of the photoresist layer;

[0024] Figure 6 is a side view of the wafer of Figure 5, after etching;

[0025] Figure 7 is a side view of the wafer of Figure 6, after bonding material deposition;

[0026] Figure 8 is a side view of the wafer of Figure 7, with a first chip in register with some of the posts on the wafer and a second chip being brought into register with other posts on the wafer;

[0027] Figure 9 is a side, cross-sectional view of a gang bonder with a single wafer in position on the bottom stage, ready for permanent bonding with multiple chips;

[0028] Figure 10 is a plan view of a full wafer to which a number of chips have been temporarily bonded;

[0029] Figure 11 is a side, close-up view of a bonding region between a post and pad;

[0030] Figures 12(a), 12(b) and 12(c) show progressive steps of a flip chip bonder picking up a chip, dipping it in an electroless solvent bath and then bringing the chip into register with a wafer;

[0031] Figures 13(a) and 13(b) show before and after illustrations of a chip and wafer being temporarily bonded using an electroless solvent;

[0032] Figures 14(a) and 14(b) show before and after illustrations of a chip and wafer being temporarily bonded using an electroless solvent with eutectic bonding to achieve temporary bonding of the chip to the wafer; and

[0033] Figure 15 shows a close-up view of a bonding region between a post and pad resulting from use of electroless solvent as a bonding material for temporary bonding.

Description of Embodiments

[0034] Decribed herein is one of a variety of methods for forming contacts, presently posts, on a wafer. It will be appreciated that similar teachings apply to the formation of posts

on a chip.

[0035] A method for forming posts on a wafer is shown in Figures 1 to 6. Figure 1 shows a wafer 10. An electrically conductive material seed layer 12 is deposited onto the wafer 10. The wafer 10 is formed from silicon. However, any other appropriate material may be used, such as germanium.

[0036] Deposition of the seed layer 12 is performed using physical vapour deposition (PVD). This process produces very smooth layer of electrically conductive material having a surface roughness height of around 1nm. The electrically conductive material deposited by the PVD process may be Cu, Al, Au or any other appropriate material. The present seed layer 12 is formed from Cu.

[0037] After the seed layer 12 has been deposited a photoresist 14 is laid over the seed layer 12 as shown in Figure 2. The photoresist 14 is patterned with the apertures 16 defining the positions where posts will be formed on the wafer 10.

[0038] Posts 18 are then formed on the exposed portions of the seed layer 12, through the patterned photoresist 14, as shown in Figure 3. The present posts 18 are formed using an electroplating process.

[0039] The posts 18 comprise the same electrically conductive material as the seed layer 12. Thus in the present embodiment, the posts 18 are formed from Cu. While different metals can be used for the seed layer 12 and posts 18, using the same metals is useful. This ensures the melting point of the metals is the same and reduces the likelihood of galvanic corrosion.

[0040] The posts 18 have irregular surfaces and dissimilar heights after electroplating. In prior art CoW bonding methods, this is one of the primary reasons for applying a thick layer of solder on the posts so that there is sufficient solder on each post for solder reflow to form a smooth cap.

[0041] In this manner, posts may be formed on either the chip and wafer or, in some embodiments, on both the chip and wafer.

[0042] The posts 18 then undergo planarization. The planarization process results in a highly polished or planar contact surface on each of the posts 18.

[0043] Planarization can be achieved using any process providing an appropriate low surface roughness (e.g. less than 20nm). Some relevant processes involve chemical-mechanical planarization (CMP) of the top surfaces 20 of the posts 18 using a CMP device (not shown). CMP can yield a surface roughness as low as 1nm. An different relevant process is bit grinding. Bit grinding can yield a surface roughness in the range of about 15 to 20nm. A further relevant process is dry polishing. Dry polishing can yield a surface roughness in the range of about 15 to 20nm. Whichever appropriate planarization process is adopted, it can be useful for the photoresist 14 to remain in place during planarization to reduce the likelihood of damage to the posts 18 resulting from

lateral forces (i.e. forces applied parallel to the plane of the top surface 20) applied to the posts 18 (e.g. for a CMP process, lateral force may be applied by the carrier or chuck of the CMP device). In this circumstance, the photoresist 14 provides lateral support to the posts 18 to counteract lateral forces applied during planarization. Accordingly, in the present embodiment, planarization occurs while the photoresist 14 is in place on the seed layer 12.

[0044] Planarization removes material from the posts 18 until a desired height of the posts 18 is reached. The desired height will usually be the lowest part of the top surface 20 – in other words, the part of the contact surface closest to the wafer 10 before planarization – or lower. Electroplating often results in the lowest part of the top surface 20 being within the aperture 16 of the photoresist 14 – in other words, below the exposed surface of the photoresist 14. It is therefore usually necessary to also remove part of the photoresist 14 down to the desired height of the posts 18 after planarization, as shown in Figure 4 in which the photoresist 14 and posts 18 have undergone planarization until they form a substantially continuous, planar surface 22. Thus planarization also results in uniform height of the posts 18 across the wafer. The uniformity in post height reduces the likelihood that chips will drift under applied pressure during subsequent permanent bonding.

[0045] The top surface 20 is a contact surface that, after planarization, becomes better suited to contacting an opposing contact on the chip during CoW bonding according to the methods described herein. The contact surface 20 will be substantially planar with a surface roughness height (i.e. the difference in height of the post 18 at the lowest point of the contact surface 20 when compared with the highest point of the contact surface 20) of less than 20nm.

[0046] The photoresist layer 14 is then removed, leaving behind the Cu posts 18 on the seed layer 12 as shown in Figure 5. Regions 23 of the seed layer 12 are then removed using a known process, such as chemical etching, to produce electrically isolated Cu posts 18 as shown in Figure 6.

[0047] The chip is also provided with contacts. Typically, for a plurality of posts 18 a like plurality of contacts will be provided, one contact will for each post 18. The like plurality of contacts are arranged in a mirror-image configuration to the posts 18 such that the posts 18 and contacts align upon inversion of the chip onto the wafer 10 for bonding. Also, where multiple chips are to be bonded to the same wafer, each chip will include contacts arranged in a mirror image of a subset of the posts on the wafer, as shown in Figure 8.

[0048] The contacts on the chip may be posts such as those formed on the wafer 10. Alternatively, the chip 24 may include a different types of contacts, such as pads 26, as shown in Figure 8. Where the chip 24 includes pads 26, the pads 26 may be formed by

any appropriate method such as PVD and patterning through photoresist, followed by etching. A PVD process can be useful since it provides a highly smooth surface, with a surface roughness height of around 1nm. The highly smooth surface improves the surface area for bonding and lowers the required bonding force during permanent bonding, when compared with a less smooth surface.

[0049] After formation of the posts 18, bonding material 28 is applied to the posts 18 as shown in Figure 7. The amount of bonding material is only that which is necessary to achieve a temporary CoW bond to ensure alignment of the chip and wafer during subsequent global or gang bonding.

[0050] It is desirable that the bonding material 28 be applied very shortly after planarization to reduce oxidation of the contact surfaces 20 of the posts 18 – here, "very shortly" means before oxidation of the contact surfaces 20. If the contact surfaces 20 oxidise after planarization, the contact surfaces 20 can be de-oxidised immediately before application of the bonding material 28. Removing surface oxidation lowers the bonding temperature and thereby reduces the likelihood that the bonding material will diffuse into the posts 18. For example, in order to achieve Cu-Cu diffusion bonding between oxidised contact surfaces may require a temperature of around 350 degrees Celsius, whereas those same surface may undergo Cu-Cu diffusion bonding at temperatures as low as 200 degrees Celsius when de-oxidised.

[0051] In a first embodiment, as shown in Figure 6, bonding material, presently tin (Sn) solder 28, is deposited onto the posts 18. The solder 28 is deposited using electroless electroplating, though other techniques may be used. Similarly, another low melting point metal may be used in place of Sn.

[0052] The bonding material 28 is deposited in a thickness no greater than the surface roughness height of the planarized contact surface 20. While the surface height roughness will typically be less than 20nm, even for rougher surfaces it is desirable that the bonding material thickness remain less than 1 micron. This reduces the likelihood that permanent bonding will be achieved using an intermetallic compound comprising the bonding material.

[0053] After application of the bonding material, the posts 18 are temporarily bonded to the contacts 26 using the bonding material to stabilize a position of the chip relative to the wafer10 for permanent diffusion bonding of the chip to the wafer 10. A flip chip bonder (not shown) is used for this purpose. The flip chip bonder picks up the chip 24 and positions it over the wafer 10 with the pads 26 brought into register (i.e. contact and alignment) with the posts 18. While a single chip 24 may be positioned over the wafer 10 by the flip chip bonder, the embodiment shown in Figure 8 provides two chips 24 and it will be understood that the present methodology can be applied in cases where even three or more chips 24 are temporarily bonded to the wafer 10 before being

permanently bonded to the wafer 10 in a subsequent bonding step.

[0054] The chip 24 is heated so that the solder 28 melts and tacks (i.e. temporarily bonds) the pads 26 to the posts 18 and thereby pads chip 24 to the wafer 10. The chip 24 may be heated in advance of it being brought into register with the wafer 10. However, this may result in oxidation of the Cu pads 26. It is therefore usually preferable that the chip 24 be heated once brought into register with the wafer 10.

[0055] In the present embodiment, the thickness of the Sn solder 28 is equal to or less than the surface roughness height of the contact surfaces 20. Also, heating of the chip 24 is not sufficient to melt the Cu pads 26, and the wafer 10 and Cu posts 18 are not directly heated at all, though some heat will transfer to the posts 18 from the chip. Given the pads 26 and contact surface 20 do not melt, the remaining surface roughness of the pads 26 and contact surfaces 20 will prevent them from being bonded across the full contact surfaces 20 of the posts 18. In other words, the temporary bonding of the chip to the wafer involves tacking the chip to the wafer at a number of regions across the contact surfaces 20, but not across the entirety of the contact surfaces 20.

[0056] Notably, the solder bonding material 28 is not intended to be of sufficient thickness to permanently bond the chip 24 to the wafer 10. However, Sn is still useful for temporarily bonding the chip 24 to the wafer 10 in a flip chip bonder, in advance of permanent bonding. It is therefore undesirable that the Sn solder 28 diffuse into the Cu posts 18 before temporary bonding is achieved.

[0057] To reduce diffusion of the Sn solder 28 into the Cu posts 18, the wafer 10 is maintained at a temperature lower than the melting point of the bonding material during temporary bonding – in other words, at a temperature lower than the melting point of Sn in the present example. At lower temperatures the oxidation of the contact surfaces 20 is also reduced. In the embodiment shown in Figure 8, the wafer 10 is maintained at room temperature. Thus, the solder 28 remains solid until the heated chip 24 brings it to melting temperature at which point it rapidly, temporarily bonds the chip 24 to the wafer 26. Since the solder 28 is Sn, and Sn melts quickly over around 240 degrees Celsius, temporary tacking or bonding of the chip to the wafer can be carried out in a few seconds.

[0058] Shortly after the solder 28 is melted the chip 24 ceases to be heated. The flip chip bonder may thereafter cool the chip 24 to bring the solder 28 back down below melting point. In an ideal scenario the solder 28 will melt and bond the chip 24 to the wafer 10 substantially without diffusing into either of the posts 18 or pads 26.

[0059] In this manner a temporary integrated chip 30 is formed form the chip 24 and wafer 10 to which the chip 24 is temporarily bonded.

[0060] It will be understood that bonding material can similarly be applied to the chip as well as, or alternatively to, the wafer. However, since the present embodiment intends

to provide only sufficient bonding material to temporarily bond the chip to the wafer to enable permanent bonding by diffusion of the posts and pads into each other, it is generally desirable that the bonding material be applied to only one of the chip and wafer.

[0061] Upon completion of the temporary bonding process the product of the temporary bonding process (e.g. the temporary integrated chip, or a wafer 31 to which multiple chips 33 have been temporarily bonded – see also Figure 10) is placed on a bottom stage 35 of a gang or global bonder 37, though other types of bonder may be used. The temporary integrated chip, or wafer with multiple chips, is then vacuumed (to remove volatile gases) and, subsequently, a top stage 39 presses and applies force to the chip or chips.

[0062] The top and bottom stages are then heated to a suitable temperature for permanent bonding. This heat should be sufficient to cause the Cu posts 18 to diffuse into the Cu pads 26 and vice versa, achieving permanent bonding. This temperature should be less than the melting temperature of the material (e.g. Cu) from which the posts 18 and pads 26 are formed. The temperature needed will depend on the level of oxidation of the Cu contact surfaces 20 and the pad 26. Usually, a temperature in the range of 100 degrees Celsius to 250 degrees Celsius is sufficient to achieve permanent bonding substantially by Cu-Cu diffusion.

[0063] It will be appreciated that the presence of some Sn in the bonding region will result in the creation of an intermetallic compound in the bonded region 32 during permanent bonding, as shown in Figure 11. However, in accordance with the present methods, the amount of bonding material, and the resultant amount of intermetallic compound, is insufficient for reliable, permanent CoW bonding.

[0064] Pressure may be applied during either or both of the temporary and permanent bonding steps. The pressure ensures appropriate contact between each of the posts 18 and the pads 26 to account for any variations in the height of posts 18 – these variations will be very minor due to planarization. Flip chip bonding and global wafer bonding techniques will be understood in the art. Other bonding techniques (e.g. heated air bonding) will be similarly understood as applicable to the present methods.

[0065] In a second embodiment, after regions of the Cu seed layer have been etched to complete formation of the posts, an electroless solvent is used to temporarily bond the chip to the wafer.

[0066] With reference to Figures 12(a), 12(b) and 12(c), to deposit the solvent onto the contacts 38 of a chip 40, a solvent bath or tray 50 containing electroless solvent is positioned between chip pick up and bonding in the flip chip bonder. During temporary bonding, the flip chip bonder picks up the chip 40 (see Figure 12(a)) and dips it in the electroless solvent bath 50 (see Figure 12(b)) to coat the contacts 38 (e.g. pads or

posts) with solvent 41. While the solvent is wet the chip 40 is brought into register with the wafer 42 (see Figure 12(c)). By contacting the chip 40 to the wafer 42, and ideally pressing the chip 40 to the wafer 42, solvent from the contacts 38 of the chip 40 flows onto, and coats, the contacts 44 of the wafer 42. In this manner the solvent fills between the contact surfaces 46, 48 of the contacts 38, 44.

[0067] The electroless solvent 41 reacts with the contacts, 38, 44 to form Sn between them. The process hereafter depends on the amount of electroless solvent deposited on the contacts 38. As shown in Figures 14(a) and 14(b), where a thicker layer of electroless solvent 41 is deposited (e.g. 100 nm to 1 micron thick) the amount of metal, such as Sn, formed between the contacts 38, 44 can be sufficient for temporary bonding. In other words, eutectic bonding is used to temporarily bond the chip 40 to the wafer 42. Thus permanent bonding can be achieved in a flip chip bonder, or alternatively in a gang or global bonder if desired. Where the thickness of the electroless solvent is lower (e.g. less than 100nm), as shown in Figures 13(a) and 13(b), the metal formed between the contacts 38, 44 should still be heated to forge the necessary temporary bond between the contacts 38, 44. Accordingly, for thinner layers of electroless solvent the chip 40 is brought into register with the wafer 42 using a flip chip bonder. The chip 40 is then heated, and the wafer 42 held at a lower temperature, as described above to temporarily bond the chip 40 to the wafer 42. After temporary bonding the temporary integrated chip (comprising chip 40 and wafer 42 temporarily bonded together) is moved to a global or gang bonder as described above, and permeant bonding takes place.

[0068] In both cases using electroless solvent the metal layer ultimately produced is markedly thinner than in conventional CoW bonding techniques. Similar to the thin electroplated layer of Sn of the previous embodiment, by using only a thin electroless solvent layer (e.g. less than 1 micron thick) only temporary bonding is possible using the Sn formed by the solvent react with the posts and contacts. This enables permanent bonding to result predominantly from Cu-Cu or Al-Al diffusion of the posts 18 into the contacts 32 and vice versa.

[0069] The electroless solvent layer may be 10um thick. The thickness can be adjusted by adjusting the depth of solvent in the solvent bath. To achieve a low thickness the solvent can be coated into the bath using a roller between successive chip coating steps.

[0070] It will be noted that the present methods use very little bonding material to bond the chip to the wafer. The amount of bonding material is in general only that which is necessary to temporarily bond, or tack, the chip to the wafer to ensure alignment during permanent bonding. Permanent bonding is achieved by metal-metal (e.g. Cu-Cu or Al-Al) diffusion of the posts on one of the chip and wafer into the contacts on the

other of the chip and wafer.

[0071] Due to the use of very little bonding material, there is a far lower risk of bridging between neighbouring posts when compared with conventional CoW bonding techniques. In some cases, the bonding material can be vapourised during diffusion of the chip and wafer contacts into each other. In other cases, the bonding material may be diffused into the posts or contacts (e.g. into Cu) which, in light of the minimal bonding material employed during temporary bonding, becomes practically undetectable and has negligible influence on permanent bonding – the permanent bonding in this circumstance remains substantially reliant on post/contact diffusion. This is illustrated in Figure 15, which shows the ideal scenario in which no bonding material (e.g. solder) protrudes from between the contacts after bonding. Thus the pitch (centre to centre distance between the closest posts on a chip or wafer) can be substantially reduced. For example, for a Cu post diameter in the range of 0.1 μm to 50 μm, and a post height of 0.1 μm to 50 μm, the pitch may be 0.2 μm to 100 μm. In such cases, the Sn bonding material thickness may be 0.5 nm to 100nm. As such, a post diameter of 0.1 μm may be able to achieve a pitch of 0.2 μm with a Sn thickness of 0.5 nm and, similarly, a post diameter of 50 μm may be able to achieve a pitch of 100 μm with a Sn thickness of 100 nm.

[0072] The embodiments described herein have been cast in the context of a chip being bonded to a wafer, with the wafer providing the posts and the chip providing opposing contacts. It will be appreciated that the same teachings apply to a scenario in which the chip provides the posts and the wafer provides the contacts, or in which both the chip and wafer provide posts.

Claims

[Claim 1] A method for chip on wafer bonding, comprising:
forming a plurality of posts on at least one of a chip and a wafer, and a like plurality of contacts on the other of the chip and the wafer;
planarizing a contact surface of each post, the planarized contact surface having a surface roughness height;
applying, to at least one of the chip and the wafer, a bonding material of a thickness no greater than the surface roughness height;
temporarily bonding the posts to the contacts using the bonding material to stabilize a position of the chip relative to the wafer for permanent diffusion bonding of the chip to the wafer.

[Claim 2] The method of claim 1 further comprising permanently bonding the chip to the wafer by diffusion of the posts and contacts into each other.

[Claim 3] The method of claim 1 or 2 wherein the applying step comprises applying insufficient bonding material to permanently bond the chip to the wafer through forming of an intermetallic compound.

[Claim 4] The method of any preceding claim, wherein each of the plurality of contacts comprises a pad.

[Claim 5] The method of claim 5, wherein the pads are formed by a physical vapour deposition process.

[Claim 6] The method of any one of claims 1 to 3, wherein each of the plurality of contacts comprises a post.

[Claim 7] The method of any preceding claim, further comprising the step of de-oxidising the contact surface of each post before the applying step.

[Claim 8] The method of any preceding claim, wherein bonding material is applied to one of the chip and wafer which, during the temporary bonding step, is held at a lower temperature than the other of the chip or wafer.

[Claim 9] The method of claim 8, wherein the lower temperature is a temperature at which the plurality of contacts does not oxidise.

[Claim 10] The method of claim 8 or 9, wherein the lower temperature is a temperature at which the bonding material does not diffuse into the plurality of contacts.

[Claim 11] The method of any one of claims 8 to 10, wherein the lower temperature is about room temperature.

[Claim 12] The method of any preceding claim, wherein the permanent bonding step is performed at a temperature below the melting temperature of the

bonding material.

[Claim 13] The method of any preceding claim, wherein the temporarily bonding step comprises temporarily bonding the posts to the contacts in a flip chip bonder.

[Claim 14] The method of claim 13, further comprising cooling the flip chip bonder, after the temporary bonding step, to solidify the bonding material.

[Claim 15] The method of any preceding claim, wherein the bonding material is applied using electroplating.

[Claim 16] The method of any one of claims 1 to 14, wherein the bonding material comprises a solvent applied by electroless deposition to the plurality of posts.

[Claim 17] The method of claim 16, wherein the temporary bonding step bonds the posts and contacts with the solvent reacting with the posts and contacts to form a low melting point metal.

[Claim 18] The method of any preceding claim, wherein the bonding material forms a layer having a thickness of less than 1 micron.

[Claim 19] An integrated chip formed using the method of any preceding claim.

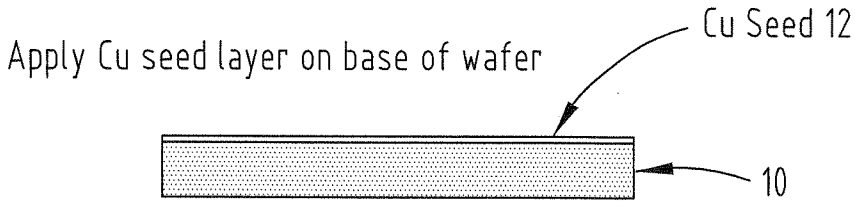


FIG. 1

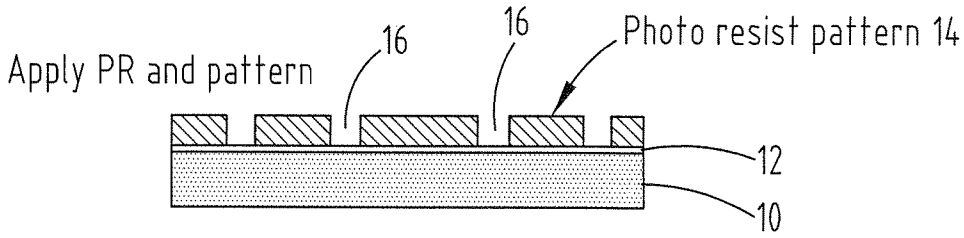


FIG. 2

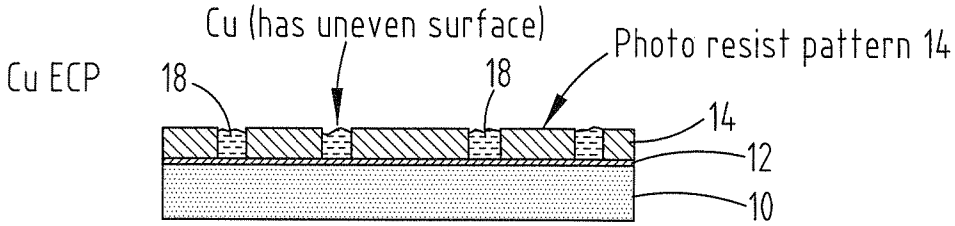


FIG. 3

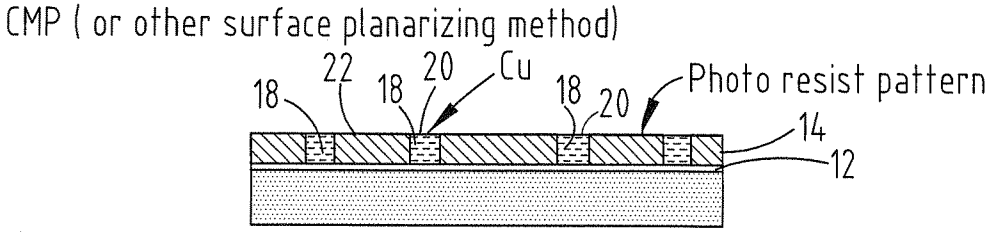


FIG. 4

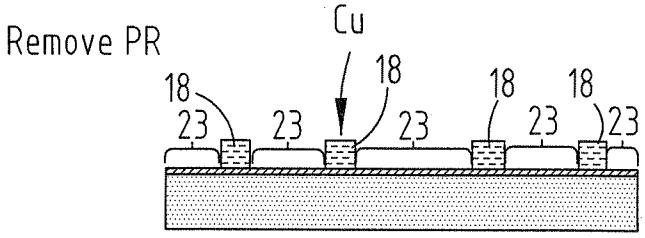


FIG. 5

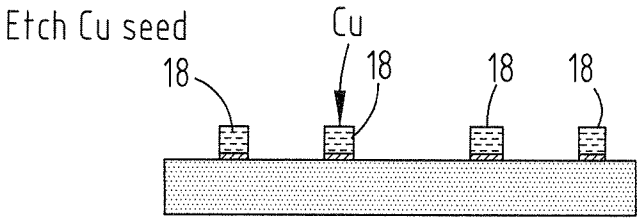


FIG. 6

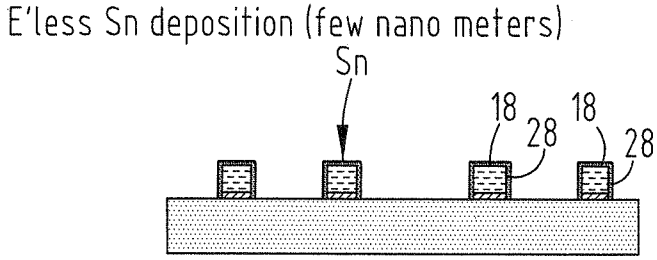


FIG. 7

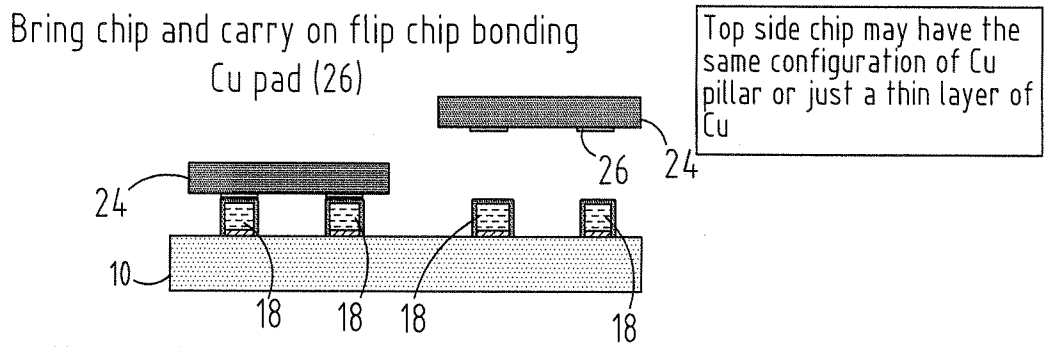


FIG. 8

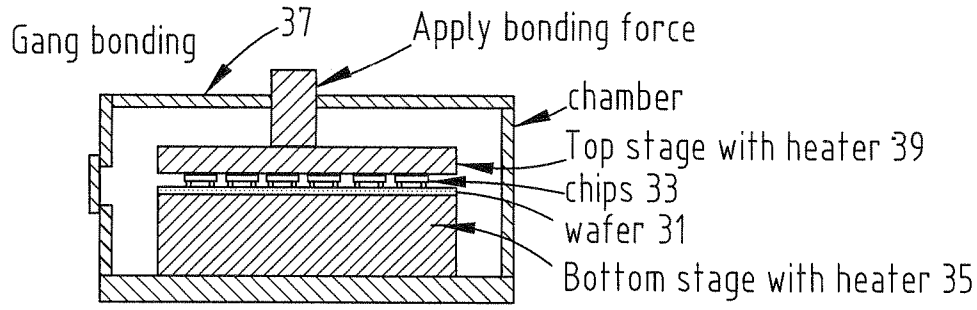


FIG. 9

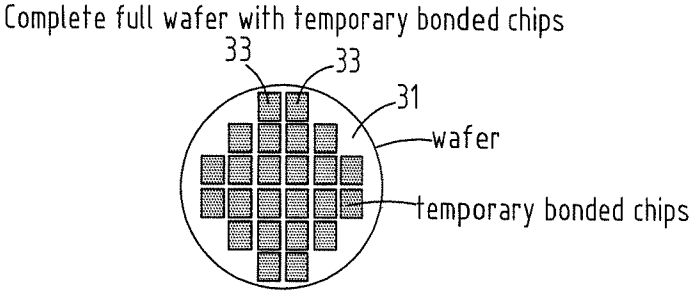


FIG. 10

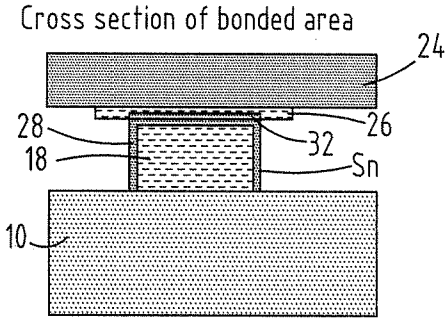


FIG. 11

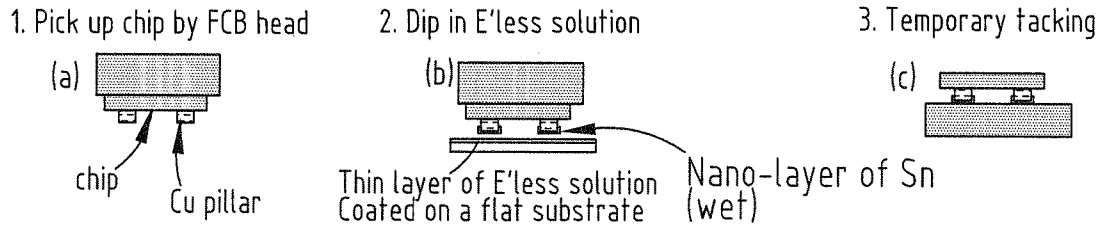


FIG. 12

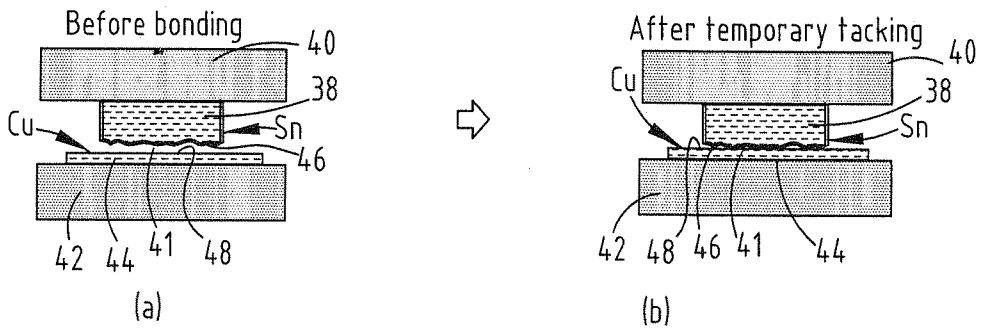


FIG. 13

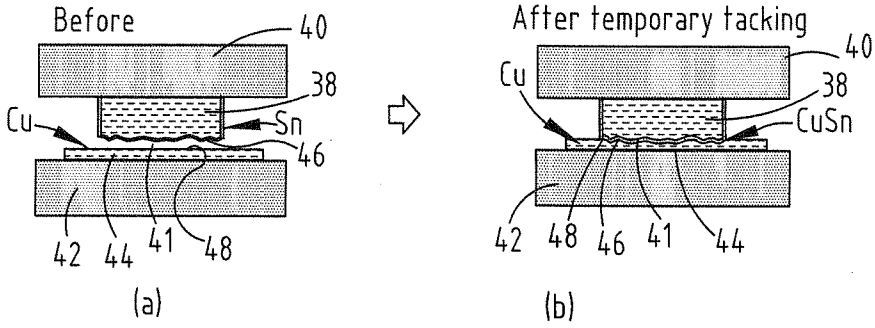


FIG. 14

- Bonding is mainly done by Cu-Cu (or Al-Al) diffusionn bonding
-Solder gets diffused into Cu
- No visible Cu-Sn intermetallic layer

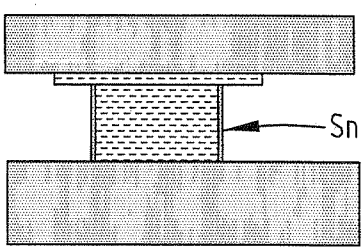


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2015/050173

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/98 (2006.01) H01L 23/13 (2006.01) H01L 23/48 (2006.01) H01L 23/52 (2006.01) H01L 25/00 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: WPI, WPIAP and EPODOC. Classification: H01L (and sub-marks in CPC and IPC). Keywords: wafer, chip, dice, die, substrate, integrated circuit; bond, glue, affix, adhere, adhesive, join; post, pillar, stanchion, protrusion, pole, column; contact, pad, electrode; temporary, intermediate, non-permanent; chip on wafer, CoW; diffusion; bond, weld, solder; planarise, smooth, polish, CMP; stack, mount, position, locate, stabilise; flip chip; AND LIKE TERMS. Database: Espacenet. Keywords: Agency for Science, Technology and Research (Applicant); Wickramanayaka (Inventor), Ling Xie (Inventor), Aw (Inventor); chip; wafer; diffusion bond; AND LIKE TERMS. Database: Auspat. Keywords: Agency for Science, Technology and Research (Applicant); Sunil Wickramanayaka (Inventor), Ling Xie (Inventor), Jerry Jie Li Aw (Inventor). Applicant and Inventor names searched in internal databases provided by IP Australia.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

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Date of the actual completion of the international search	Date of mailing of the international search report
7 September 2015	07 September 2015

Name and mailing address of the ISA/AU	**Authorised officer**
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustralia.gov.au	Richard Baker AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262832583

INTERNATIONAL SEARCH REPORT C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		International application No. **PCT/SG2015/050173**
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2014/040423 A1 (XIAMEN RATIONAL ELECTRONICS. CO., LTD.) 20 March 2014 Abstract, paragraphs 5 to 23, 38 to 55, figures 1 to 12	1-19
A	US 2009/0302469 A1 (MASUDA et al.) 10 December 2009 Abstract, paragraphs 0002, 0010 to 0012, 0037 to 0062, figures 1A to 8D	1-19
A	US 2004/0173372 A1 (SUDA) 09 September 2004 Abstract, paragraphs 0002, 0010 to 0018, 0040 to 0070, figures 1 to 19	1-19
A	US 5468655 A (GREER) 21 November 1995 Abstract, column 1 lines 17 to 19, column 2 line 40 to column 6 line 52, figures 1 to 7	1-19

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/SG2015/050173**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document/s Cited in Search Report		**Patent Family Member/s**	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**
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		CN 102915933 A	06 Feb 2013
US 2009/0302469 A1	10 December 2009	US 2009302469 A1	10 Dec 2009
		US 8637986 B2	28 Jan 2014
		JP 2009105119 A	14 May 2009
		US 2014113411 A1	24 Apr 2014
US 2004/0173372 A1	09 September 2004	US 2004173372 A1	09 Sep 2004
		US 6911606 B2	28 Jun 2005
		DE 102004010633 A1	16 Sep 2004
		JP 2004266175 A	24 Sep 2004
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		KR 100621053 B1	08 Sep 2006
US 5468655 A	21 November 1995	US 5468655 A	21 Nov 1995
		JP H08255971 A	01 Oct 1996

End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.