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(54) Title: ETCH MASK FOR HYBRID LASER SCRIBING AND PLASMA ETCH WAFER SINGULATION PROCESS

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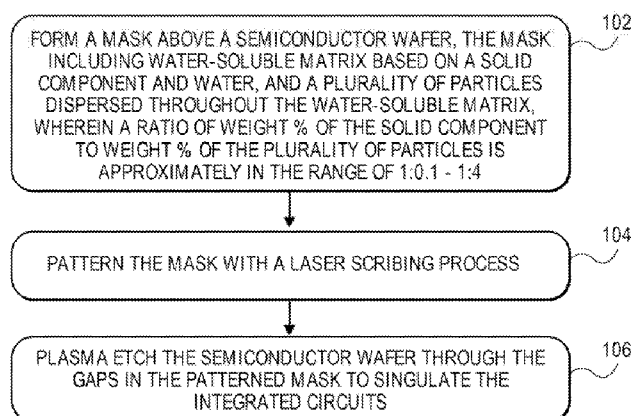


FIG. 1

(57) Abstract: Etch masks and methods of dicing semiconductor wafers are described. In an example, an etch mask for a wafer singulation process includes a water-soluble matrix based on a solid component and water. The etch mask also includes a plurality of particles dispersed throughout the water-soluble matrix. The plurality of particles has an average diameter approximately in the range of 5-100 nanometers. A ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.1 - 1:4.



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ETCH MASK FOR HYBRID LASER SCRIBING AND PLASMA ETCH WAFER SINGULATION PROCESS

BACKGROUND

1) FIELD

[0001] Embodiments of the present invention pertain to the field of semiconductor processing and, in particular, to methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

2) DESCRIPTION OF RELATED ART

[0002] In semiconductor wafer processing, integrated circuits are formed on a wafer (also referred to as a substrate) composed of silicon or other semiconductor material. In general, layers of various materials which are either semiconducting, conducting or insulating are utilized to form the integrated circuits. These materials are doped, deposited and etched using various well-known processes to form integrated circuits. Each wafer is processed to form a large number of individual regions containing integrated circuits known as dice.

[0003] Following the integrated circuit formation process, the wafer is "diced" to separate the individual die from one another for packaging or for use in an unpackaged form within larger circuits. The two main techniques that are used for wafer dicing are scribing and sawing. With scribing, a diamond tipped scribe is moved across the wafer surface along pre-formed scribe lines. These scribe lines extend along the spaces between the dice. These spaces are commonly referred to as "streets." The diamond scribe forms shallow scratches in the wafer surface along the streets. Upon the application of pressure, such as with a roller, the wafer separates along the scribe lines. The breaks in the wafer follow the crystal lattice structure of the wafer substrate. Scribing can be used for wafers that are about 10 mils (thousandths of an inch) or less in thickness. For thicker wafers, sawing is presently the preferred method for dicing.

[0004] With sawing, a diamond tipped saw rotating at high revolutions per minute contacts the wafer surface and saws the wafer along the streets. The wafer is mounted on a supporting member such as an adhesive film stretched across a film frame and the saw is repeatedly applied to both the vertical and horizontal streets. One problem with either scribing or sawing is that chips and gouges can form along the severed edges of the dice. In addition, cracks can form and propagate from the edges of the dice into the substrate and render the integrated circuit inoperative. Chipping and cracking are particularly a problem with scribing because only one side of a square or rectangular die can be scribed in the <110>direction of the crystalline

structure. Consequently, cleaving of the other side of the die results in a jagged separation line. Because of chipping and cracking, additional spacing is required between the dice on the wafer to prevent damage to the integrated circuits, e.g., the chips and cracks are maintained at a distance from the actual integrated circuits. As a result of the spacing requirements, not as many dice can be formed on a standard sized wafer and wafer real estate that could otherwise be used for circuitry is wasted. The use of a saw exacerbates the waste of real estate on a semiconductor wafer. The blade of the saw is approximate 15 microns thick. As such, to insure that cracking and other damage surrounding the cut made by the saw does not harm the integrated circuits, three to five hundred microns often must separate the circuitry of each of the dice. Furthermore, after cutting, each die requires substantial cleaning to remove particles and other contaminants that result from the sawing process.

[0005] Plasma dicing has also been used, but may have limitations as well. For example, one limitation hampering implementation of plasma dicing may be cost. A standard lithography operation for patterning resist may render implementation cost prohibitive. Another limitation possibly hampering implementation of plasma dicing is that plasma etching of commonly encountered metals (e.g., copper) in dicing along streets can create production issues or throughput limits.

SUMMARY

[0006] Embodiments of the present invention include methods of, and apparatuses for, dicing semiconductor wafers.

[0007] In an embodiment, an etch mask for a wafer singulation process includes a water-soluble matrix based on a solid component and water. The etch mask also includes a plurality of particles dispersed throughout the water-soluble matrix. The plurality of particles has an average diameter approximately in the range of 5-100 nanometers. A ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.1 – 1:4.

[0008] In another embodiment, a method of dicing a semiconductor wafer including a plurality of integrated circuits includes forming a mask above the semiconductor wafer. The mask includes a water-soluble matrix based on a solid component and water, and a plurality of particles dispersed throughout the water-soluble matrix. A ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.1 – 1:4. The method also includes patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits. The method also includes plasma etching the semiconductor wafer through the gaps in the

patterned mask to singulate the integrated circuits. The patterned mask protects the integrated circuits during the plasma etching.

[0009] In another embodiment, a method of dicing a semiconductor wafer including a plurality of integrated circuits includes forming a mask above the semiconductor wafer. The mask includes a water-soluble matrix based on a solid component and water, and a plurality of particles dispersed throughout the water-soluble matrix. The plurality of particles has an average diameter approximately in the range of 5-100 nanometers. The method also includes patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits. The method also includes plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits. The patterned mask protects the integrated circuits during the plasma etching.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a Flowchart representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention.

[0011] Figure 2A illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operations 102 of the Flowchart of Figure 1 and to operation 302 of the Flowchart of Figure 3, in accordance with an embodiment of the present invention.

[0012] Figure 2B illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation 104 of the Flowchart of Figure 1 and to operation 304 of the Flowchart of Figure 3, in accordance with an embodiment of the present invention.

[0013] Figure 2C illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation 106 of the Flowchart of Figure 1 and to operation 306 of the Flowchart of Figure 3, in accordance with an embodiment of the present invention.

[0014] Figure 3 is a Flowchart representing operations in another method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with another embodiment of the present invention.

[0015] Figure 4 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present invention.

[0016] Figures 5A-5D illustrate cross-sectional views of various operations in a method of dicing a semiconductor wafer, in accordance with an embodiment of the present invention.

[0017] Figure 6 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[0018] Figure 7 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0019] Methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon, are described. In the following description, numerous specific details are set forth, such as water soluble mask materials and treatments, laser scribing conditions, and plasma etching conditions and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known aspects, such as integrated circuit fabrication, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0020] One or more embodiments are directed particularly to using particle dispersions to improve etch selectivity in etch masks.

[0021] A hybrid wafer or substrate dicing process involving an initial laser scribe and subsequent plasma etch may be implemented for die singulation. The laser scribe process may be used to cleanly remove a mask layer, organic and inorganic dielectric layers, and device layers. The laser etch process may then be terminated upon exposure of, or partial etch of, the wafer or substrate. The plasma etch portion of the dicing process may then be employed to etch through the bulk of the wafer or substrate, such as through bulk single crystalline silicon, to yield die or chip singulation or dicing. More specifically, one or more embodiments are directed to implementing an etch-resistant mask for, e.g., dicing applications. It is to be appreciated that although many embodiments described below are associated with femto-second laser scribing, in other embodiments, laser scribing with other laser beam types may also be compatible with masking materials described herein. It is also to be appreciated that although many embodiments described below are associated with scribing streets having metallized features, in other embodiments, metal free scribing streets may also be considered.

[0022] In accordance with one or more embodiments described herein, addressing one or more of the above issues, a relatively thin, but high etch resistant mask coating is provided.

Advantages to implementing such an etch resistant mask can include one or more of (1) reducing wafer level and wafer to wafer coating thickness variation, (2) reducing a thickness requirement for the etch mask of a hybrid dicing process since less mask material is consumed in the etch portion of the process, and (3) reducing a required laser pulse energy for scribing.

[0023] To provide context, in a hybrid laser scribing and plasma etching die singulation process, a wafer is cut or sectioned along dicing streets between the die. Traditionally, dicing has been performed with a mechanical saw. Mobile devices and other technology drivers, however, may require more advanced singulation approaches to reduce cracking, delamination, and chipping defects. To facilitate such advanced processing, a water soluble polymer protective coating may be applied to the substrate. The coating and the device test layers in the street may then be removed by laser scribing, which opens up the underlying substrate material, typically Si. The exposed Si may then be plasma etched through its entire thickness to singulate the wafer into the individual dies. The protective coating may then be removed in a deionized (DI) water based cleaning operation. Water soluble protective coatings may be desirable due to environmental and ease of processing. Such a water soluble polymer coating may primarily be used as an etch mask during a plasma etching step, and also may collect any debris generated during a previous laser scribing operation. Unfortunately, most water soluble polymers, do not have high resistance to plasma etching, while polymers that have good etch resistance are typically not soluble in water. To provide further context, etch selectivity is defined as the ratio of the amount of substrate material (e.g., Si) removed to the amount of mask loss during the etch process. Water soluble polymers typically have relatively low selectivity, and it may be advantageous to enhance the selectivity of the etch mask without sacrificing water solubility.

[0024] In accordance with an embodiment of the present invention, a water soluble mask with particles therein is provided for etch selectivity for laser scribing and plasma etching wafer singulation. Embodiments may address potential needs for improved etch resistance in a water soluble dicing mask. In a specific example, a polyvinyl alcohol (PVA) matrix with silica particles dispersed therein is provided as an etch mask. More generally, in an embodiment, particle dispersions are mixed with water soluble polymers to form a composite mask. Materials such as oxides and polymers, which are not water soluble, can be incorporated into water soluble polymer mixtures as dispersions. Suitable particle dispersions may be colloidal dispersions of inorganic particles and polymers. Suitable inorganic particles may include oxide, such as silicon oxide, aluminum oxide, titanium oxide, and cerium oxide, and other particles such as calcium carbonate, barium sulfate, etc. Suitable polymer particles may include polystyrene and PTFE. It is to be appreciated that low haze is usually required for the etch mask since the mask is laser

scribed. To minimize haze, in an embodiment, particles smaller than 100 nanometers may be included in the matrix.

[0025] As such, in an aspect of the present invention, an etch-resistant mask is used for a singulation process based on a combination of a laser scribing process with a plasma etching process to dice a semiconductor wafer into singulated integrated circuits. Figure 1 is a Flowchart 100 representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention. Figure 3 is a Flowchart 300 representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention. Figures 2A-2C illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operations of Flowcharts 100 and 300, in accordance with an embodiment of the present invention.

[0026] Referring to operation 102 of Flowchart 100 or operation 302 of Flowchart 300, and corresponding Figure 2A, an etch mask 202 is formed above a semiconductor wafer or substrate 204. The etch mask 202 covers and protects integrated circuits 206 formed on the surface of semiconductor wafer 204. The etch mask 202 also covers intervening streets 207 formed between each of the integrated circuits 206.

[0027] In an embodiment, the etch mask 202 includes a water-soluble matrix based on a solid component and water. The etch mask 202 also includes a plurality of particles dispersed throughout the water-soluble matrix. In one embodiment, the plurality of particles has an average diameter approximately in the range of 5-100 nanometers. In one embodiment, a ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.1 – 1:4. In one embodiment, the plurality of particles has an average diameter approximately in the range of 5-100 nanometers, and a ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.1 – 1:4.

[0028] In one embodiment, the plurality of particles has an average diameter approximately in the range of 5-50 nanometers. It is to be appreciated that a smaller diameter may be preferable in order to mitigate or negate any potential laser light scattering or haze. In one embodiment, the ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.5 – 1:2.

[0029] In one embodiment, the plurality of particles is a plurality of particles selected from the group consisting of silica (SiO₂) particles, alumina (Al₂O₃) particles, alumina-coated silicon particles, polytetrafluoroethylene (PTFE) particles, and combinations thereof. It is to be appreciated that other oxides, such as titanium oxide, cerium oxide, zinc oxide, indium tin oxide,

zirconium oxide, and other inorganic particles such as calcium carbonate, barium sulfate, etc., may also be used as particle additives. Suitable polymer particles also include polystyrene, epoxies, etc.

[0030] In one embodiment, the water soluble matrix is a polyvinyl alcohol (PVA)-based water soluble matrix. Other water soluble matrix options include polyethylene oxide, polyethylene glycol, polyacrylic acid, polyacrylamide, polystyrene-maleic acid copolymer, hydroxyethyl cellulose, hydroxyethyl starch, etc. In one embodiment, the water-soluble matrix includes approximately 10-40 weight % of the solid component with the remainder water. In a specific embodiment, the etch mask 202 is fabricated by mixing a solution of water soluble matrix and a liquid dispersion of the particles.

[0031] In one embodiment, forming the mask 202 above the semiconductor wafer 204 includes spin-coating the mask 202 on the semiconductor wafer 204. In a specific embodiment, prior to coating, a plasma or chemical pre-treatment is performed to enable better wettability and coating of the wafer.

[0032] In one embodiment, forming the mask 202 above the semiconductor wafer 204 includes mixing the plurality of particles with the water-soluble matrix on a same tool platform used to pattern the mask with the laser scribing process (and, possibly, also the same tool used to plasma etch the wafer), e.g., by on-board mixing, including in-line mixing. In one embodiment, forming the mask 202 above the semiconductor wafer 204 includes mixing the plurality of particles with the water-soluble matrix on a same tool platform used to deposit (e.g., spin-coat) and/or ultimately clean or remove the mask, e.g., by on-board mixing, including in-line mixing. In one embodiment, forming the mask 202 above the semiconductor wafer 204 includes mixing the plurality of particles with the water-soluble matrix on a same tool platform used to pattern the mask with the laser scribing process (and, possibly, also the same tool used to plasma etch the wafer) and used to deposit (e.g., spin-coat) and/or ultimately clean or remove the mask, e.g., by on-board mixing, including in-line mixing.

[0033] In an embodiment, advantages of the above described on-board/in-line mixing may include one or more of (1) eliminating any aging effects of the mask material and remove shelf life concerns, (2) allowing for a flexible ratio of the mix which may be beneficial for (a) not having to requalify specific mixtures from suppliers, (b) accommodate different surface topology of the wafer and (c) more readily accommodate different target coating thicknesses for different applications/wafer thicknesses (e.g., thicker wafers require longer etch time), (3) improving mask quality (e.g., especially with combined with in-line de-gassing to mitigate bubble defects), and/or (4) enabling the possibility that a static mixer can provide in line mixing capability.

[0034] In an embodiment, etch mask 202 is a water soluble etch mask. In one such embodiment, as deposited, the water-soluble mask 202 is readily dissolvable in an aqueous media. For example, in one embodiment, the as deposited water-soluble mask 202 is composed of a material that is soluble in one or more of an alkaline solution, an acidic solution, or in deionized water. In a specific embodiment, the as-deposited water-soluble mask 202 has an etch or removal rate in an aqueous solution approximately in the range of 1 – 15 microns per minute and, more particularly, approximately 1.3 microns per minute.

[0035] In an embodiment, semiconductor wafer or substrate 204 is composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably be disposed. For example, in one embodiment, semiconductor wafer or substrate 204 is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing semiconductor wafer 204 includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, semiconductor wafer or substrate 204 is composed of a III-V material such as, e.g., a III-V material substrate used in the fabrication of light emitting diodes (LEDs).

[0036] In an embodiment, semiconductor wafer or substrate 204 has disposed thereon or therein, as a portion of the integrated circuits 206, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits 206. Materials making up the streets 207 may be similar to or the same as those materials used to form the integrated circuits 206. For example, streets 207 may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the streets 207 includes test devices similar to the actual devices of the integrated circuits 206.

[0037] Referring again to corresponding Figure 2A, in an optional embodiment, the etch mask 202 is baked. In an embodiment, the etch mask 202 is baked 299 to increase the etch resistance of the etch mask, providing enhanced etch resistant etch mask 203. In a specific embodiment, the etch mask 202 is baked 299 at a relatively high temperature approximately in the range of 50 to 130 degrees Celsius. Such higher temperature baking may cause crosslink of the etch mask 202 so as to significantly increase etch resistance. For example, when the etch mask 202 mask is baked at or near 130 degrees Celsius for approximately 3 minutes, the resulting enhanced etch resistant mask 203 is robust against a silicon etch process. In one

embodiment, baking is performed using a hot plate technique or a heat (light) radiation applied from the wafer front side (e.g., non-tape mounted side in the case of the use of a substrate carrier) or other suitable techniques.

[0038] Referring to operation 104 of Flowchart 100 and to operation 304 of Flowchart 300, and corresponding Figure 2B, the etch mask 202 or 203 is patterned with a laser scribing process to provide patterned mask 208 with gaps 210, exposing regions of the semiconductor wafer or substrate 204 between the integrated circuits 206. As such, the laser scribing process is used to remove the material of the streets 207 originally formed between the integrated circuits 206. In accordance with an embodiment of the present invention, patterning the etch mask 202 or 203 with the laser scribing process includes forming trenches 212 partially into the regions of the semiconductor wafer 204 between the integrated circuits 206, as depicted in Figure 2B. In accordance with an embodiment of the present invention, the plurality of particles of the etch mask 202 or 203 do not substantially interfere with a laser scribing process during the patterning of the etch mask 202 or 203 with the laser scribing process.

[0039] In an embodiment, a femtosecond-based laser is used as a source for a laser scribing process. For example, in an embodiment, a laser with a wavelength in the visible spectrum plus the ultra-violet (UV) and infra-red (IR) ranges (totaling a broadband optical spectrum) is used to provide a femtosecond-based laser, i.e., a laser with a pulse width on the order of the femtosecond (10^{-15} seconds). In one embodiment, ablation is not, or is essentially not, wavelength dependent and is thus suitable for complex films such as films of the etch mask 202 or 203, the streets 207 and, possibly, a portion of the semiconductor wafer or substrate 204.

[0040] It is to be appreciated that by using a laser beam profile with contributions from the femtosecond range, heat damage issues are mitigated or eliminated versus longer pulse widths (e.g., nanosecond processing). The elimination or mitigation of damage during laser scribing may be due to a lack of low energy recoupling or thermal equilibrium. It is also to be appreciated that laser parameter selection, such as beam profile, may be critical to developing a successful laser scribing and dicing process that minimizes chipping, microcracks and delamination in order to achieve clean laser scribe cuts. The cleaner the laser scribe cut, the smoother an etch process that may be performed for ultimate die singulation. In semiconductor device wafers, many functional layers of different material types (e.g., conductors, insulators, semiconductors) and thicknesses are typically disposed thereon. Such materials may include, but are not limited to, organic materials such as polymers, metals, or inorganic dielectrics such as silicon dioxide and silicon nitride.

[0041] A street between individual integrated circuits disposed on a wafer or substrate may include the similar or same layers as the integrated circuits themselves. For example, Figure

4 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present invention.

[0042] Referring to Figure 4, a street region 400 includes the top portion 402 of a silicon substrate, a first silicon dioxide layer 404, a first etch stop layer 406, a first low K dielectric layer 408 (e.g., having a dielectric constant of less than the dielectric constant of 4.0 for silicon dioxide), a second etch stop layer 410, a second low K dielectric layer 412, a third etch stop layer 414, an undoped silica glass (USG) layer 416, a second silicon dioxide layer 418, and an etch mask 420 (such as an etch mask described above in association with masks 202 or 203). Copper metallization 422 is disposed between the first and third etch stop layers 406 and 414 and through the second etch stop layer 410. In a specific embodiment, the first, second and third etch stop layers 406, 410 and 414 are composed of silicon nitride, while low K dielectric layers 408 and 412 are composed of a carbon-doped silicon oxide material.

[0043] Under conventional laser irradiation (such as nanosecond-based irradiation), the materials of street 400 behave quite differently in terms of optical absorption and ablation mechanisms. For example, dielectrics layers such as silicon dioxide, is essentially transparent to all commercially available laser wavelengths under normal conditions. By contrast, metals, organics (e.g., low K materials) and silicon can couple photons very easily, particularly in response to nanosecond-based irradiation. In an embodiment, a femto-second based laser scribing process is used to pattern a layer of silicon dioxide, a layer of low K material, and a layer of copper by ablating the layer of silicon dioxide prior to ablating the layer of low K material and the layer of copper.

[0044] In case that the laser beam it is a femtosecond-based laser beam, in an embodiment, suitable femtosecond-based laser processes are characterized by a high peak intensity (irradiance) that usually leads to nonlinear interactions in various materials. In one such embodiment, the femtosecond laser sources have a pulse width approximately in the range of 10 femtoseconds to 500 femtoseconds, although preferably in the range of 100 femtoseconds to 400 femtoseconds. In one embodiment, the femtosecond laser sources have a wavelength approximately in the range of 1570 nanometers to 200 nanometers, although preferably in the range of 540 nanometers to 250 nanometers. In one embodiment, the laser and corresponding optical system provide a focal spot at the work surface approximately in the range of 3 microns to 15 microns, though preferably approximately in the range of 5 microns to 10 microns or between 10 – 15 microns.

[0045] In an embodiment, the laser source has a pulse repetition rate approximately in the range of 200 kHz to 10 MHz, although preferably approximately in the range of 500kHz to 5MHz. In an embodiment, the laser source delivers pulse energy at the work surface

approximately in the range of 0.5 uJ to 100 uJ, although preferably approximately in the range of 1uJ to 5uJ. In an embodiment, the laser scribing process runs along a work piece surface at a speed approximately in the range of 500mm/sec to 5m/sec, although preferably approximately in the range of 600mm/sec to 2m/sec.

[0046] The scribing process may be run in single pass only, or in multiple passes, but, in an embodiment, preferably 1-2 passes. In one embodiment, the scribing depth in the work piece is approximately in the range of 5 microns to 50 microns deep, preferably approximately in the range of 10 microns to 20 microns deep. In an embodiment, the kerf width of the laser beam generated is approximately in the range of 2 microns to 15 microns, although in silicon wafer scribing/dicing preferably approximately in the range of 6 microns to 10 microns, measured at the device/silicon interface.

[0047] Laser parameters may be selected with benefits and advantages such as providing sufficiently high laser intensity to achieve ionization of inorganic dielectrics (e.g., silicon dioxide) and to minimize delamination and chipping caused by underlayer damage prior to direct ablation of inorganic dielectrics. Also, parameters may be selected to provide meaningful process throughput for industrial applications with precisely controlled ablation width (e.g., kerf width) and depth. In an embodiment, a line shaped profile laser beam laser scribing process is suitable to provide such advantages.

[0048] It is to be appreciated that the dicing or singulation process could be stopped after the above described laser scribing in a case that the laser scribing is used to pattern the mask as well as to scribe fully through the wafer or substrate in order to singulate the dies. Accordingly, further singulation processing would not be required in such a case. However, the following embodiments may be considered in cases where laser scribing alone is not implemented for total singulation.

[0049] In an optional embodiment, subsequent to the laser scribing process and prior to a plasma etching singulation process, an intermediate post mask-opening cleaning operation is performed. In an embodiment, the post mask-opening cleaning operation is a plasma-based cleaning process. In an example, as described below, the plasma-based cleaning process is non-reactive to the regions of the substrate 204 exposed by the gaps 210.

[0050] In accordance with one embodiment, the plasma-based cleaning process is non-reactive to exposed regions of the substrate 204 in that the exposed regions are not or only negligible etched during the cleaning process. In one such embodiment, only non-reactive gas plasma cleaning is used. For example, Ar or another non-reactive gas (or the mix) is used to perform a highly-biased plasma treatment both for mask condensation and cleaning of scribed openings. The approach may be suitable for water-soluble masks such as etch mask 202 or 203.

In another such embodiment, separate mask condensation (densification of the surface layer) and scribed trench cleaning operations are used, e.g., an Ar or non-reactive gas (or the mix) highly-biased plasma treatment for mask condensation is first performed, and then an Ar +SF₆ plasma cleaning of a laser scribed trench is performed. This embodiment may be suitable for cases where Ar-cleaning is not sufficient for trench cleaning due to too thick of a mask material.

[0051] Referring to operation 106 of Flowchart 100 or operation 306 of Flowchart 300, and corresponding Figure 2C, the semiconductor wafer 204 is etched through the gaps 210 in the patterned mask 208 to singulate the integrated circuits 206. In accordance with an embodiment of the present invention, etching the semiconductor wafer 204 includes ultimately etching entirely through semiconductor wafer 204, as depicted in Figure 2C, by etching the trenches 212 initially formed with the line shaped profile laser beam laser scribing process. In accordance with an embodiment of the present invention, plasma etching the semiconductor wafer through the gaps involves plasma etching a single crystalline silicon wafer. In that embodiment, a ratio of an etch rate of the single crystalline silicon wafer to an etch rate of the etch mask 202 or 203 is approximately in the range of 15:1 – 170:1 during the plasma etching.

[0052] In an embodiment, patterning the etch mask 202 or 203 with the laser scribing process involves forming trenches in the regions of the semiconductor wafer between the integrated circuits, and plasma etching the semiconductor wafer involves extending the trenches to form corresponding trench extensions. In one such embodiment, each of the trenches has a width, and each of the corresponding trench extensions has the width.

[0053] In an embodiment, etching the semiconductor wafer 204 includes using a plasma etching process. In one embodiment, a through-silicon via type etch process is used. For example, in a specific embodiment, the etch rate of the material of semiconductor wafer 204 is greater than 25 microns per minute. An ultra-high-density plasma source may be used for the plasma etching portion of the die singulation process. An example of a process chamber suitable to perform such a plasma etch process is the Applied Centura® Silvia™ Etch system available from Applied Materials of Sunnyvale, CA, USA. The Applied Centura® Silvia™ Etch system combines the capacitive and inductive RF coupling, which gives much more independent control of the ion density and ion energy than was possible with the capacitive coupling only, even with the improvements provided by magnetic enhancement. This combination enables effective decoupling of the ion density from ion energy, so as to achieve relatively high density plasmas without the high, potentially damaging, DC bias levels, even at very low pressures. This results in an exceptionally wide process window. However, any plasma etch chamber capable of etching silicon may be used. In an exemplary embodiment, a deep silicon etch is used to etch a single crystalline silicon substrate or wafer 204 at an etch rate greater than approximately 40% of

conventional silicon etch rates while maintaining essentially precise profile control and virtually scallop-free sidewalls. In a specific embodiment, a through-silicon via type etch process is used. The etch process is based on a plasma generated from a reactive gas, which generally a fluorine-based gas such as SF₆, C₄ F₈, CHF₃, XeF₂, or any other reactant gas capable of etching silicon at a relatively fast etch rate. In an embodiment, the etch resistant water soluble patterned mask 208 is removed after the singulation process, as depicted in Figure 2C, and as is described in greater detail below. In another embodiment, the plasma etching operation described in association with Figure 2C employs a conventional Bosch-type dep/etch/dep process to etch through the substrate 204. Generally, a Bosch-type process consists of three sub-operations: deposition, a directional bombardment etch, and isotropic chemical etch which is run through many iterations (cycles) until silicon is etched through.

[0054] In an embodiment, following the singulation process, the patterned mask 208 is removed. In an embodiment, the patterned mask 208 is removed by a hot aqueous treatment, such as a hot water treatment. In an embodiment, the patterned mask 208 is removed in a hot water treatment at a temperature approximately in the range of 40 – 100 degrees Celsius. In a specific embodiment, the patterned mask 208 is removed in a hot water treatment at a temperature approximately in the range of 80 – 90 degrees Celsius. It is to be appreciated that the hotter the temperature of the water, the less time may be needed for the hot water treatment. In accordance with an embodiment of the present invention, a plasma cleaning process can also be performed after etching to aid in the removal of the patterned mask 208.

[0055] It is to be appreciated that other circumstances may benefit from a lower water treatment temperature. For example, in the case that a wafer for dicing is supported on a dicing tape that may be impacted by a higher temperature water treatment (e.g., through loss of adhesion), a relatively lower water treatment temperature may be employed, albeit for a longer duration than a relatively higher water treatment temperature. In one such embodiment, the water treatment is between room temperature (i.e., the water is un-heated), but below a temperature of approximately 40 degrees Celsius. In a specific such embodiment, the patterned mask 208 is removed in a warm water treatment at a temperature approximately in the range of 35 – 40 degrees Celsius.

[0056] Accordingly, referring again to Flowcharts 100 and 300 and Figures 2A-2C, wafer dicing may be preformed by initial ablation to ablate through an etch mask 202 or 203, through wafer streets (including metallization), and partially into a silicon substrate. Die singulation may then be completed by subsequent through-silicon deep plasma etching. A specific example of a materials stack for dicing is described below in association with Figures 5A-5D, in accordance with an embodiment of the present invention.

[0057] Referring to Figure 5A, a materials stack for hybrid laser ablation and plasma etch dicing includes an etch mask 502, a device layer 504, and a substrate 506. The etch mask layer 502, device layer 504, and substrate 506 are disposed above a die attach film 508 which is affixed to a backing tape 510. In other embodiments, direct coupling to a standard dicing tape is used. In an embodiment, the etch mask 502 is one such as described above in association with etch mask 202 or 203. The device layer 504 includes an inorganic dielectric layer (such as silicon dioxide) disposed above one or more metal layers (such as copper layers) and one or more low K dielectric layers (such as carbon-doped oxide layers). The device layer 504 also includes streets arranged between integrated circuits, the streets including the same or similar layers to the integrated circuits. The substrate 506 is a bulk single-crystalline silicon substrate. In an embodiment, the etch mask 502 is fabricated using a thermal treatment 599, such as described above for etch mask 203.

[0058] In an embodiment, the bulk single-crystalline silicon substrate 506 is thinned from the backside prior to being affixed to the die attach film 508. The thinning may be performed by a backside grind process. In one embodiment, the bulk single-crystalline silicon substrate 506 is thinned to a thickness approximately in the range of 50 – 100 microns. It is important to note that, in an embodiment, the thinning is performed prior to a laser ablation and plasma etch dicing process. In an embodiment, the etch mask 502 has a thickness approximately in the range of 1-5 microns and the device layer 504 has a thickness approximately in the range of 2 – 3 microns. In an embodiment, the die attach film 508 (or any suitable substitute capable of bonding a thinned or thin wafer or substrate to the backing tape 510, such as dicing tapes consisting of an upper adhesive layer and a base film) has a thickness approximately in the range of 10-200 microns.

[0059] Referring to Figure 5B, the etch mask 502, the device layer 504 and a portion of the substrate 506 are patterned with a laser beam laser scribing process 512 to form trenches 514 in the substrate 506. Referring to Figure 5C, a through-silicon deep plasma etch process 516 is used to extend the trench 514 down to the die attach film 508, exposing the top portion of the die attach film 508 and singulating the silicon substrate 506. The device layer 504 is protected by the etch mask 502 during the through-silicon deep plasma etch process 516.

[0060] Referring to Figure 5D, the singulation process may further include patterning the die attach film 508, exposing the top portion of the backing tape 510 and singulating the die attach film 508. In an embodiment, the die attach film is singulated by a laser process or by an etch process. Further embodiments may include subsequently removing the singulated portions of substrate 506 (e.g., as individual integrated circuits) from the backing tape 510. In one embodiment, the singulated die attach film 508 is retained on the back sides of the singulated portions of substrate 506. In an alternative embodiment, in the case that substrate 506 is thinner

than approximately 50 microns, the laser beam laser scribing process 512 is used to completely singulate substrate 506 without the use of an additional plasma process. Embodiments may further include removing the etch mask 502 from the device layer 504. Removal of the etch mask 502 can be as described above for removal of the patterned mask 208.

[0061] A single process tool may be configured to perform many or all of the operations in a hybrid laser beam ablation and plasma etch singulation process utilizing an etch resistant water soluble mask. For example, Figure 6 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[0062] Referring to Figure 6, a process tool 600 includes a factory interface 602 (FI) having a plurality of load locks 604 coupled therewith. A cluster tool 606 is coupled with the factory interface 602. The cluster tool 606 includes one or more plasma etch chambers, such as plasma etch chamber 608. A laser scribe apparatus 610 is also coupled to the factory interface 602. The overall footprint of the process tool 600 may be, in one embodiment, approximately 3500 millimeters (3.5 meters) by approximately 3800 millimeters (3.8 meters), as depicted in Figure 6.

[0063] In an embodiment, the laser scribe apparatus 610 houses a laser assembly configured to provide a femto-second based laser beam. In an embodiment, the laser is suitable for performing a laser ablation portion of a hybrid laser and etch singulation process, such as the laser ablation processes described above. In one embodiment, a moveable stage is also included in laser scribe apparatus 610, the moveable stage configured for moving a wafer or substrate (or a carrier thereof) relative to the laser. In a specific embodiment, the laser is also moveable. The overall footprint of the laser scribe apparatus 610 may be, in one embodiment, approximately 2240 millimeters by approximately 1270 millimeters, as depicted in Figure 6.

[0064] In an embodiment, the one or more plasma etch chambers 608 is configured for etching a wafer or substrate through the gaps in a patterned mask to singulate a plurality of integrated circuits. In one such embodiment, the one or more plasma etch chambers 608 is configured to perform a deep silicon etch process. In a specific embodiment, the one or more plasma etch chambers 608 is an Applied Centura® Silvia™ Etch system, available from Applied Materials of Sunnyvale, CA, USA. The etch chamber may be specifically designed for a deep silicon etch used to create singulate integrated circuits housed on or in single crystalline silicon substrates or wafers. In an embodiment, a high-density plasma source is included in the plasma etch chamber 608 to facilitate high silicon etch rates. In an embodiment, more than one etch chamber is included in the cluster tool 606 portion of process tool 600 to enable high manufacturing throughput of the singulation or dicing process.

[0065] The factory interface 602 may be a suitable atmospheric port to interface between an outside manufacturing facility with laser scribe apparatus 610 and cluster tool 606. The factory interface 602 may include robots with arms or blades for transferring wafers (or carriers thereof) from storage units (such as front opening unified pods) into either cluster tool 606 or laser scribe apparatus 610, or both.

[0066] Cluster tool 606 may include other chambers suitable for performing functions in a method of singulation. For example, in one embodiment, a deposition and/or bake chamber 612 is included. The deposition and/or bake chamber 612 may be configured for etch mask deposition on or above a device layer of a wafer or substrate prior to laser scribing of the wafer or substrate. Such an etch mask material may be baked prior to the dicing process, as is described above. Such an etch mask material may be water soluble, as is also described above. In accordance with an embodiment of the present invention, forming an etch mask above a semiconductor wafer involves mixing a plurality of particles with a water-soluble matrix on a same tool platform used for patterning the mask with the laser scribing process. That is, although other arrangements may be suitable, in an embodiment, process tool 600 includes in-line or on-board particle and matrix mixing capability. In an embodiment, coating and cleaning modules are also integrated onto the same mainframe as the scribe and etch modules, as is described herein.

[0067] In an embodiment, referring again to Figure 6, a wet station 614 is included. The wet station may be suitable for cleaning performing a room temperature or a hot aqueous treatment for removing an etch resistant water soluble mask, as is described above, subsequent to a laser scribe and plasma etch singulation process of a substrate or wafer. In an embodiment, although not depicted, a metrology station is also included as a component of process tool 600. The cleaning chamber can include atomized mist and/or megasonics nozzle hardware that adds a physical component to the cleaning process, enhancing the dissolution rate of the mask.

[0068] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present invention. In one embodiment, the computer system is coupled with process tool 600 described in association with Figure 6. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable

transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[0069] Figure 7 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 700 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein, may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term “machine” shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[0070] The exemplary computer system 700 includes a processor 702, a main memory 704 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 706 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 718 (e.g., a data storage device), which communicate with each other via a bus 730.

[0071] Processor 702 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 702 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 702 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 702 is configured to execute the processing logic 726 for performing the operations described herein.

[0072] The computer system 700 may further include a network interface device 708. The computer system 700 also may include a video display unit 710 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 712 (e.g., a keyboard), a cursor control device 714 (e.g., a mouse), and a signal generation device 716 (e.g., a speaker).

[0073] The secondary memory 718 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 732 on which is stored one or more sets of instructions (e.g., software 722) embodying any one or more of the methodologies or functions described herein. The software 722 may also reside, completely or at least partially, within the main memory 704 and/or within the processor 702 during execution thereof by the computer system 700, the main memory 704 and the processor 702 also constituting machine-readable storage media. The software 722 may further be transmitted or received over a network 720 via the network interface device 708.

[0074] While the machine-accessible storage medium 732 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term “machine-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[0075] In accordance with an embodiment of the present invention, a machine-accessible storage medium has instructions stored thereon which cause a data processing system to perform a method of dicing a semiconductor wafer having a plurality of integrated circuits, such as a method described above.

[0076] Thus, hybrid wafer dicing approaches using a laser scribing process and plasma etch process implementing an etch-resistant mask have been disclosed.

CLAIMS

What is claimed is:

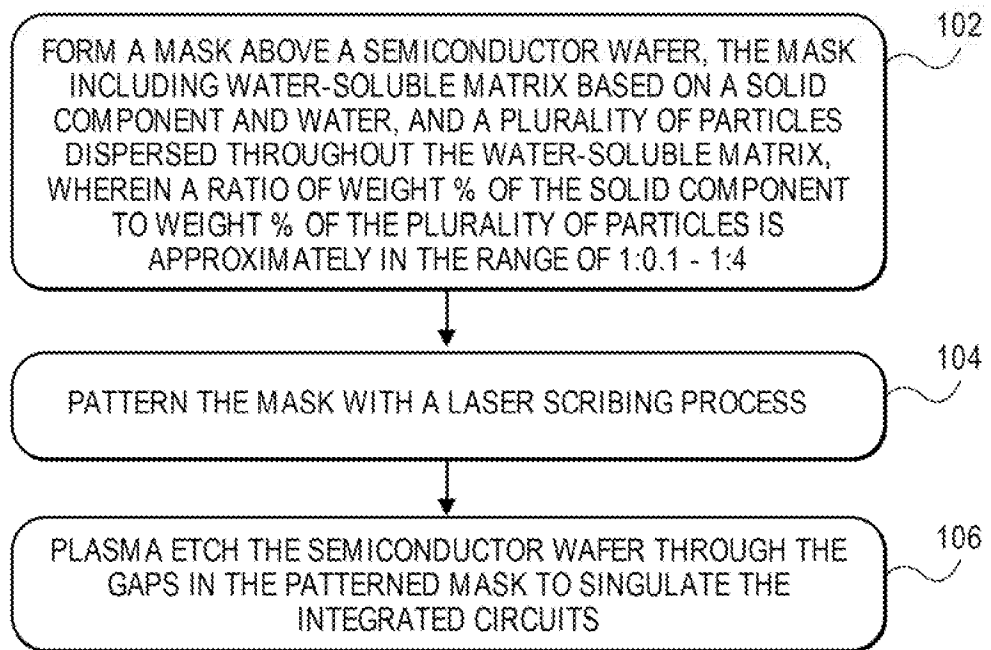
1. An etch mask for a wafer singulation process, the etch mask comprising:
a water-soluble matrix based on a solid component and water; and
a plurality of particles dispersed throughout the water-soluble matrix, the plurality of particles having an average diameter approximately in the range of 5-100 nanometers, wherein a ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.1 – 1:4.
2. The etch mask of claim 1, wherein the plurality of particles have an average diameter approximately in the range of 5-50 nanometers.
3. The etch mask of claim 1, wherein the ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.5 – 1:2.
4. The etch mask of claim 1, wherein the plurality of particles is a plurality of particles selected from the group consisting of silica (SiO₂) particles, alumina (Al₂O₃) particles, alumina-coated silicon particles, polytetrafluoroethylene (PTFE) particles, and combinations thereof.
5. The etch mask of claim 1, wherein the water soluble matrix is a water soluble matrix selected from the group consisting of a polyvinyl alcohol (PVA)-based water soluble matrix, a polyethylene oxide-based water soluble matrix, a polyethylene glycol-based water soluble matrix, and a polyacrylamide-based water soluble matrix.
6. The etch mask of claim 1, wherein the water-soluble matrix comprises approximately 10-40 weight % of the solid component with the remainder water.
7. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:
forming a mask above the semiconductor wafer, the mask comprising a water-soluble matrix based on a solid component and water, and a plurality of particles dispersed throughout the water-soluble matrix, wherein a ratio of weight % of the solid component to weight % of the plurality of particles is approximately in the range of 1:0.1 – 1:4;

patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits; and plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits, wherein the patterned mask protects the integrated circuits during the plasma etching.

8. The method of claim 7, wherein forming the mask comprises forming the mask having the plurality of particles with an average diameter approximately in the range of 5-100 nanometers.
9. The method of claim 7, wherein plasma etching the semiconductor wafer through the gaps comprises plasma etching a single crystalline silicon wafer, and wherein a ratio of an etch rate of the single crystalline silicon wafer to an etch rate of the mask is approximately in the range of 15:1 – 170:1 during the plasma etching.
10. The method of claim 7, wherein forming the mask above the semiconductor wafer comprises spin-coating the mask on the semiconductor wafer.
11. The method of claim 7, wherein the plurality of particles of the mask do not substantially interfere with the laser scribing process during the patterning of the mask with a laser scribing process.
12. The method of claim 7, further comprising:
subsequent to plasma etching the semiconductor wafer through the gaps in the patterned mask, removing the patterned mask using an aqueous solution.
13. The method of claim 7, wherein forming the mask above the semiconductor wafer comprises mixing the plurality of particles with the water-soluble matrix on a same tool platform used for patterning the mask with the laser scribing process.
14. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:
forming a mask above the semiconductor wafer, the mask comprising a water-soluble matrix based on a solid component and water, and a plurality of particles dispersed throughout the water-soluble matrix, the plurality of particles having an average diameter approximately in the range of 5-100 nanometers;

patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits; and plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits, wherein the patterned mask protects the integrated circuits during the plasma etching.

15. The method of claim 14, wherein plasma etching the semiconductor wafer through the gaps comprises plasma etching a single crystalline silicon wafer, and wherein a ratio of an etch rate of the single crystalline silicon wafer to an etch rate of the mask is approximately in the range of 15:1 – 170:1 during the plasma etching.

FLOWCHART 100**FIG. 1**

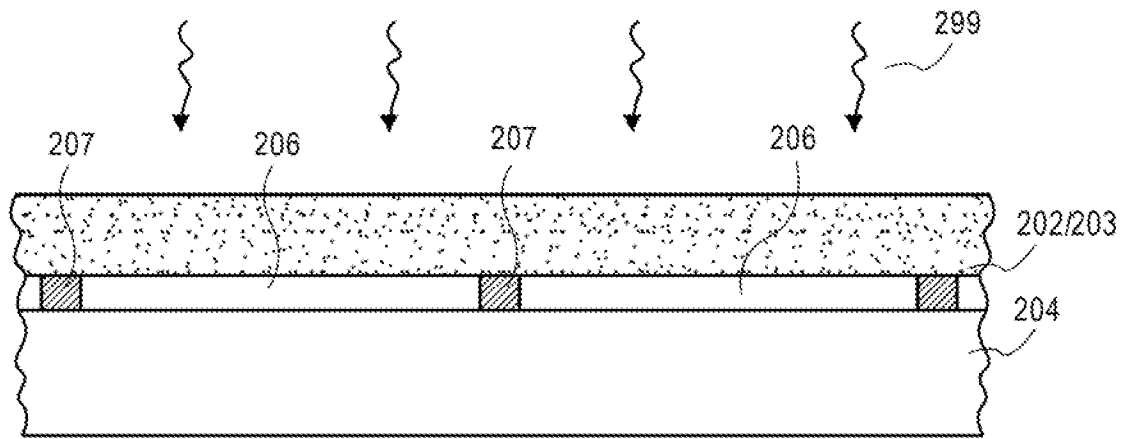


FIG. 2A

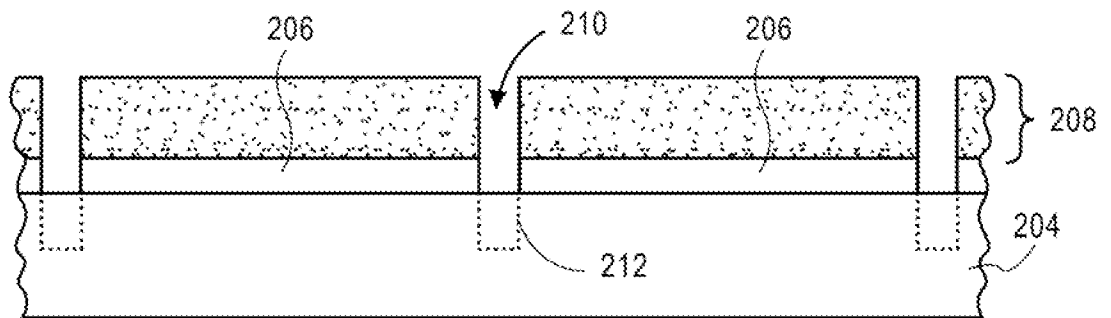


FIG. 2B

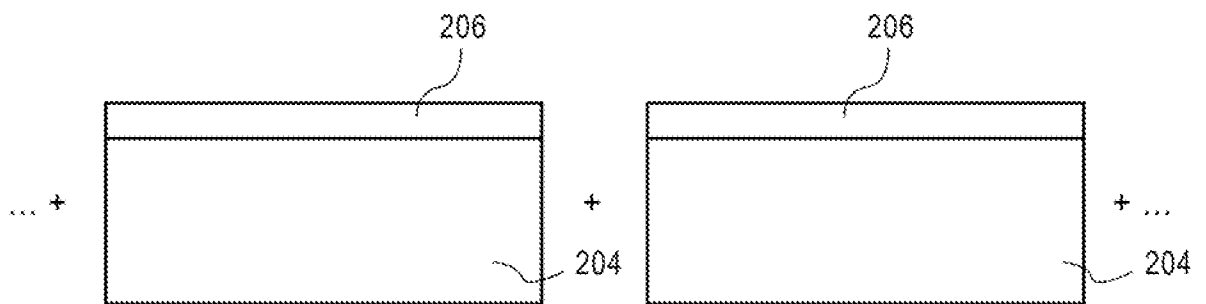
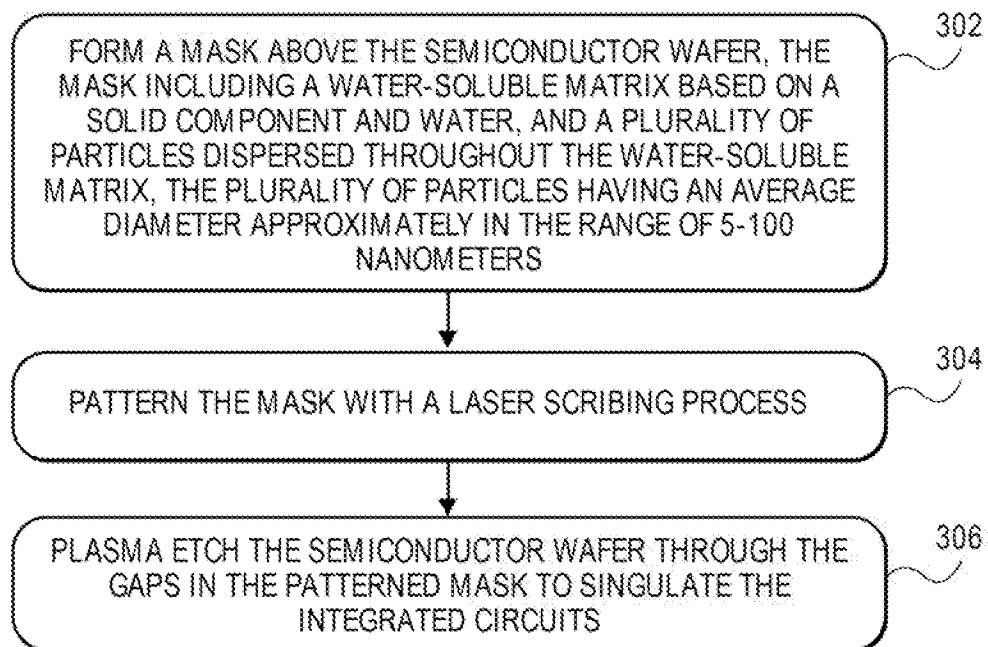


FIG. 2C

FLOWCHART 300**FIG. 3**

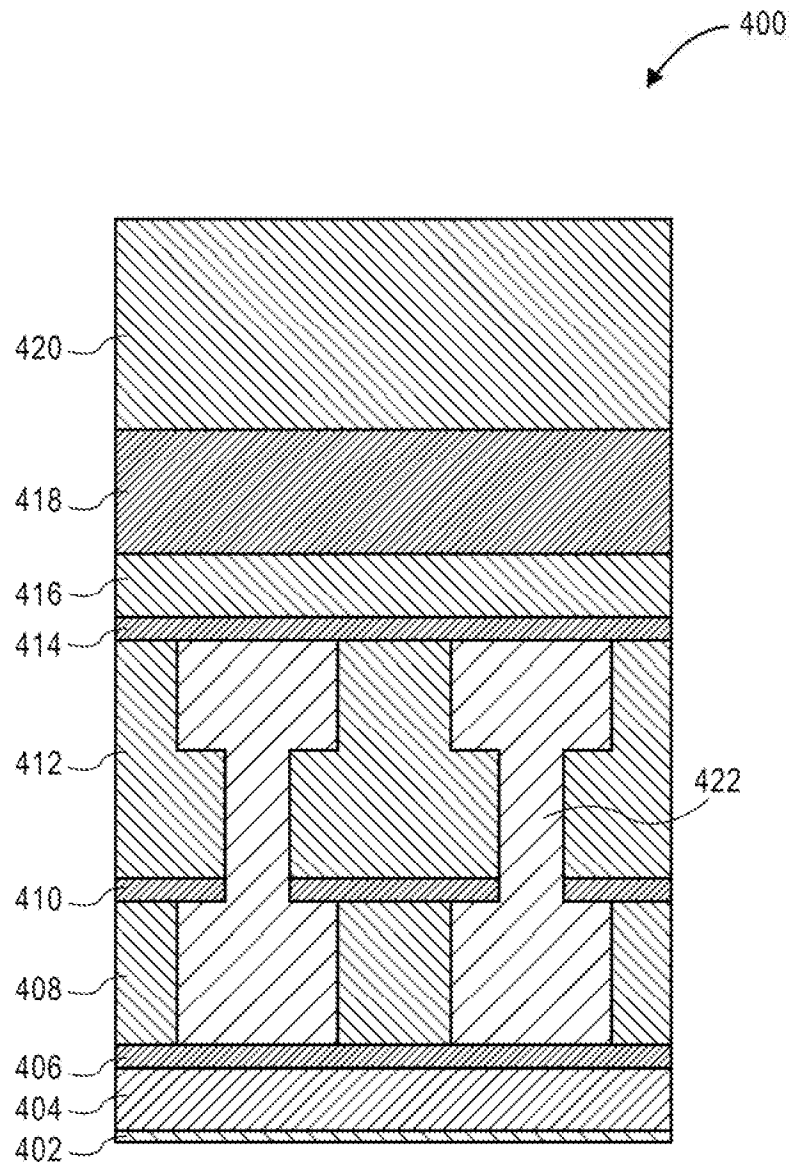
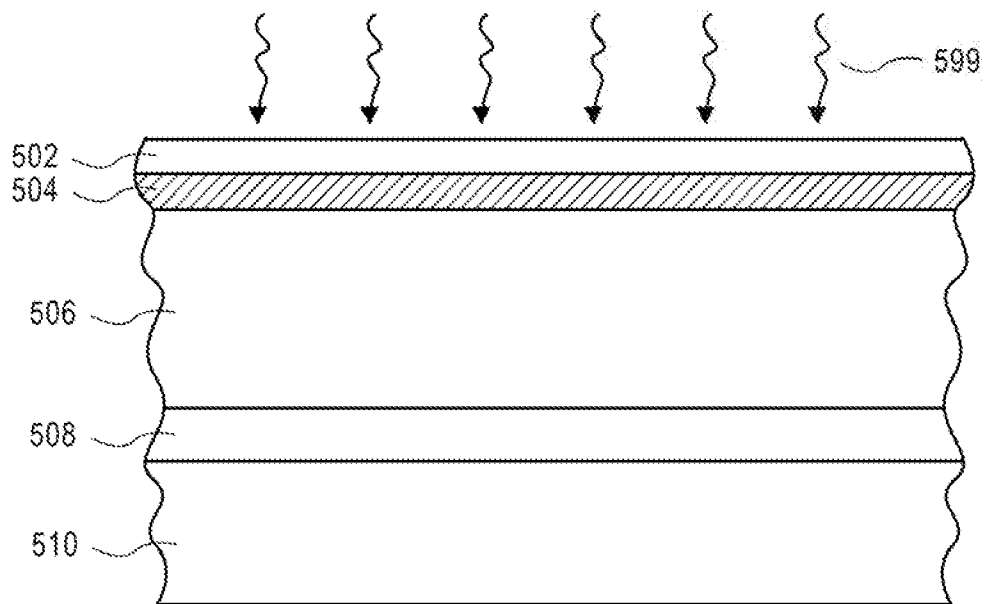
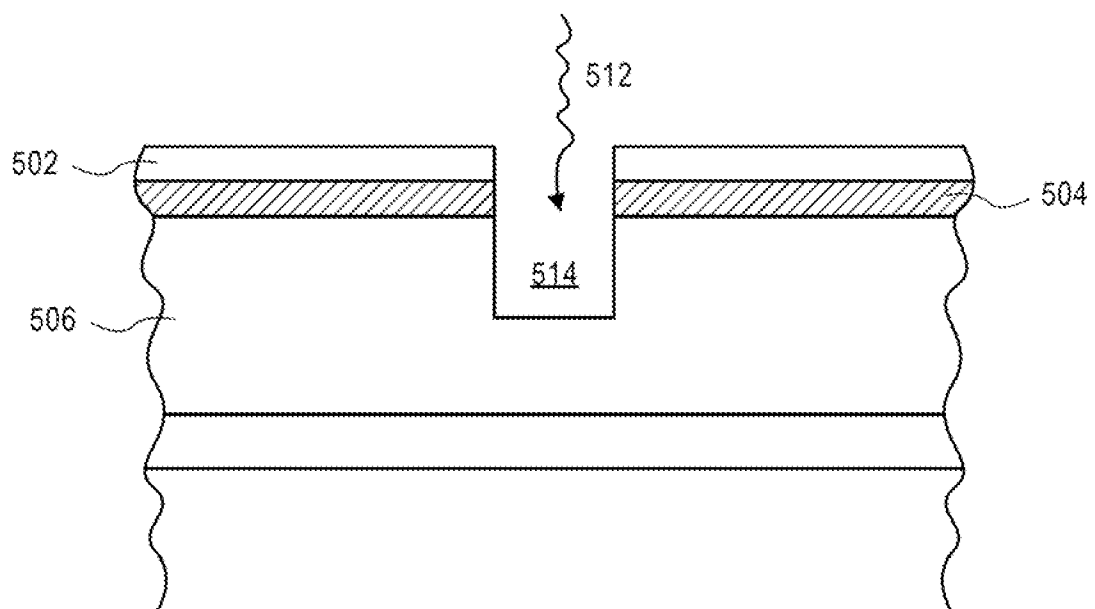


FIG. 4

**FIG. 5A****FIG. 5B**

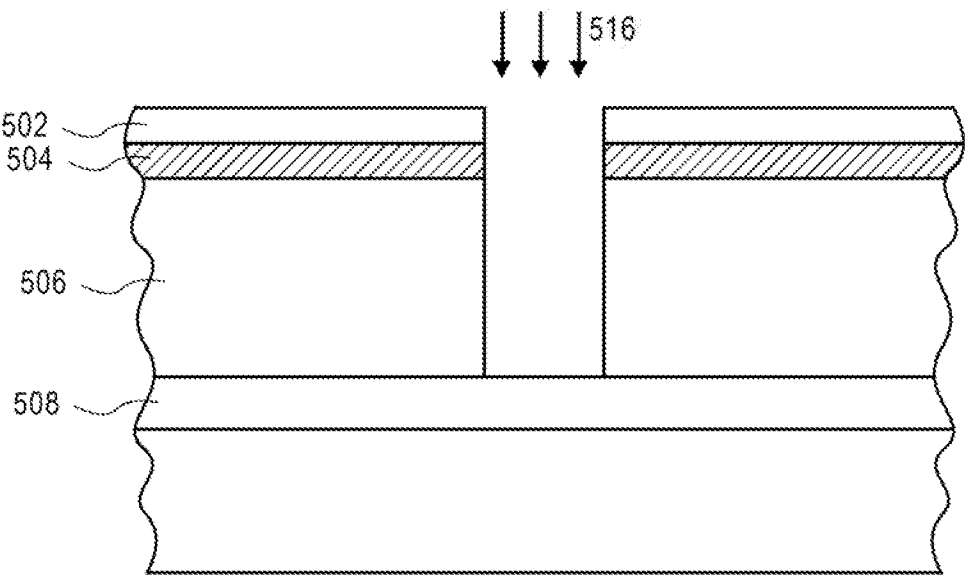


FIG. 5C

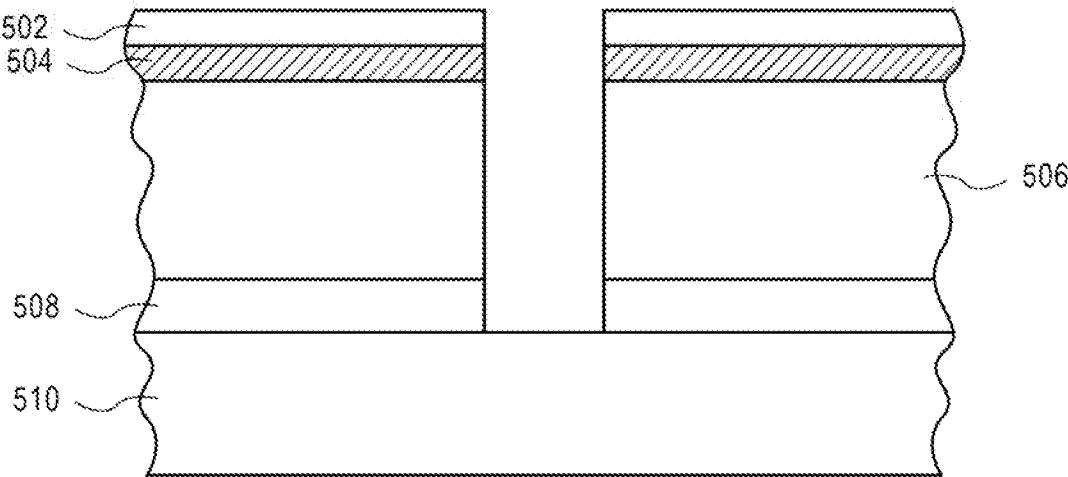


FIG. 5D

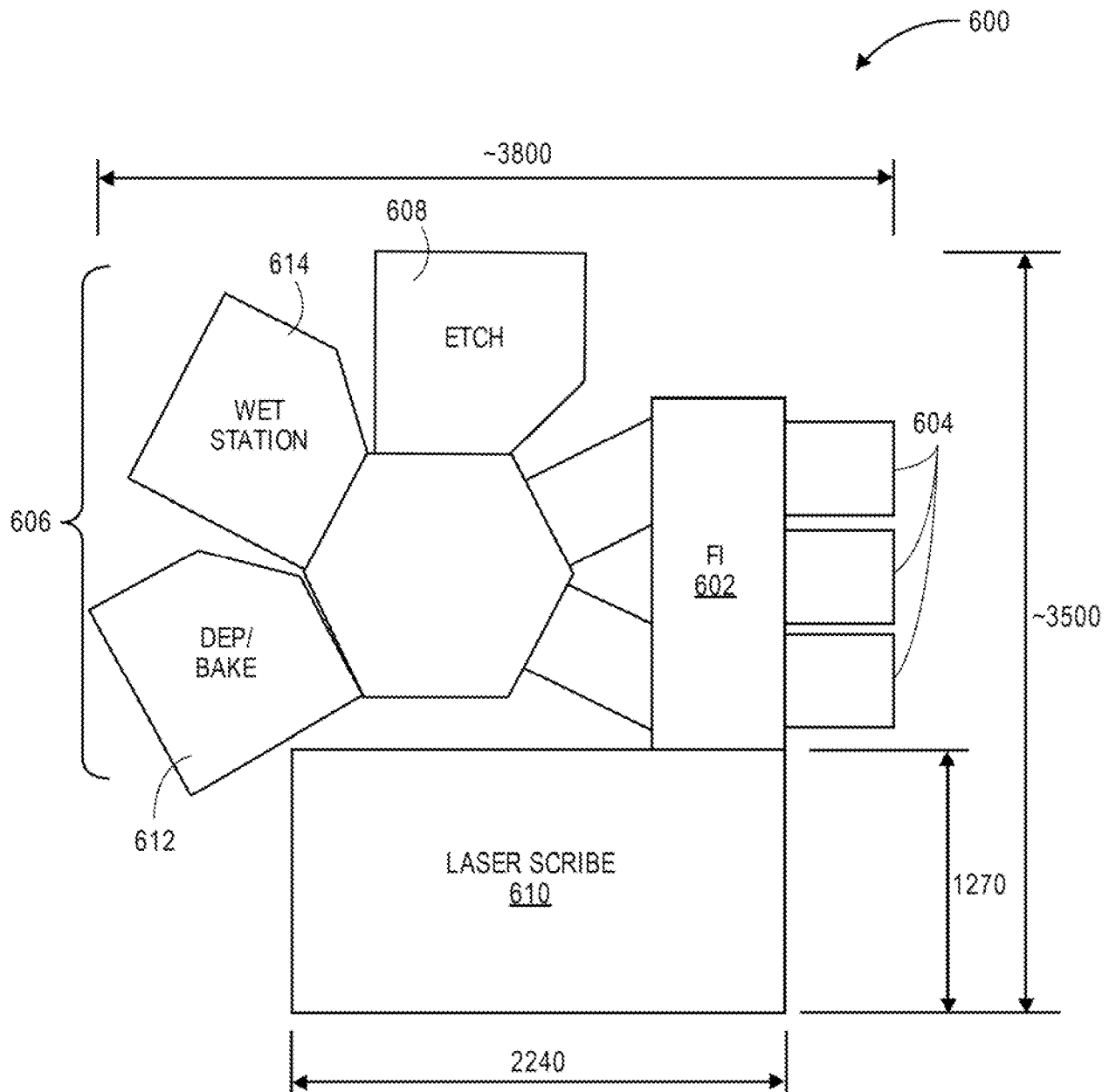
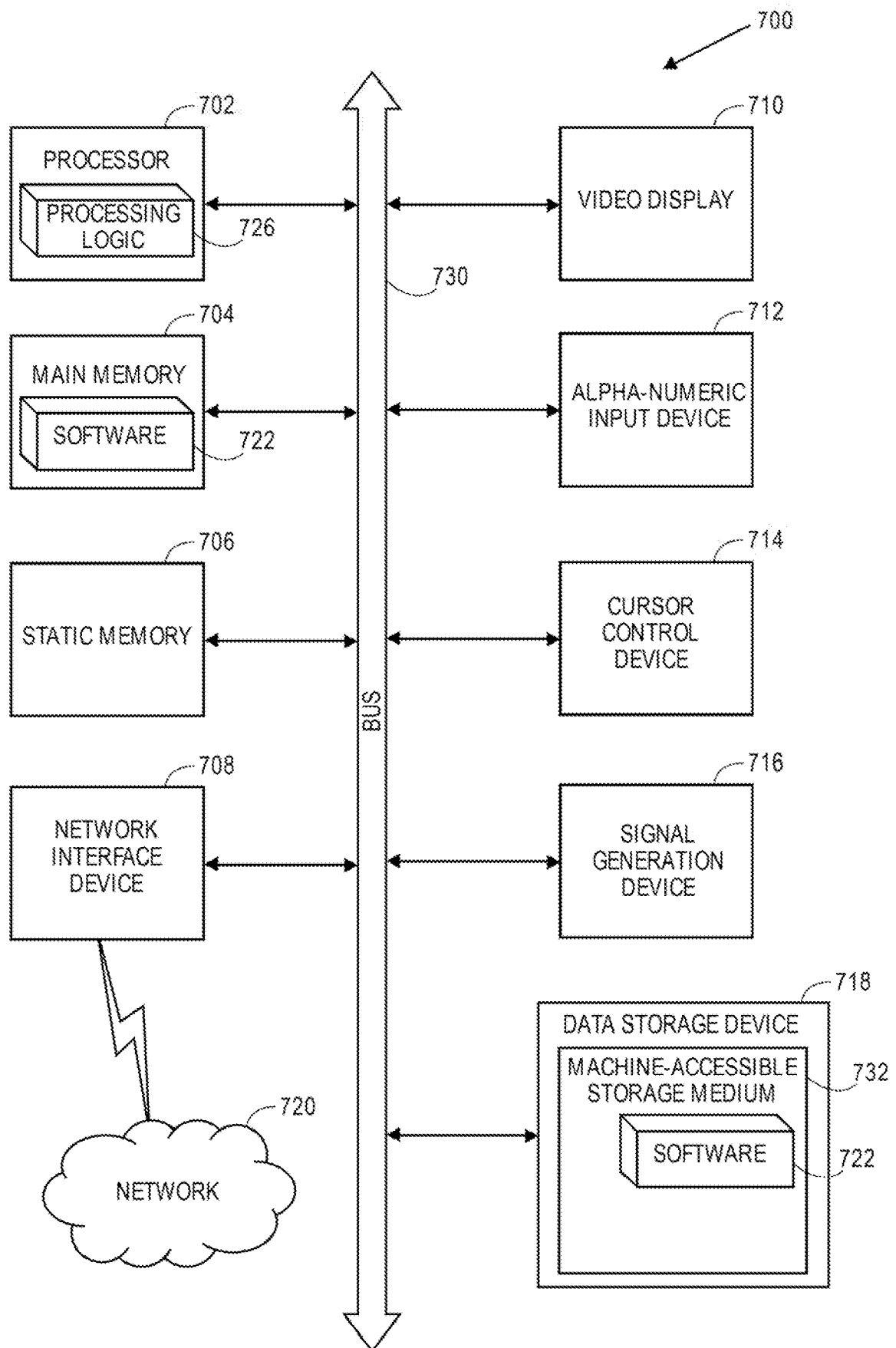


FIG. 6

**FIG. 7**

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/78(2006.01)i, H01L 21/76(2006.01)i, H01L 21/3065(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/78; H01L 21/027; H01L 21/304; H01L 21/301; H01L 21/76; H01L 21/3065

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: etch mask, singulating, water soluble, silica

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0065797 A1 (MADHAVA RAO YALAMANCHILI et al.) 06 March 2014 See paragraphs [0034]-[0036], claim 1 and figure 4A.	1-15
A	KR 10-2004-0005329 A (SAMSUNG ELECTRONICS CO., LTD.) 16 January 2004 See pages 2-3, claim 1 and figures 1-4.	1-15
A	WO 2015-116378 A1 (APPLIED MATERIALS, INC.) 06 August 2015 See paragraphs [0049]-[0053] and figure 5.	1-15
A	WO 2008-118635 A2 (MICRON TECHNOLOGY, INC.) 02 October 2008 See paragraph [0052] and figure 12A.	1-15
A	JP 2007-281526 A (MATSUSHITA ELECTRIC IND. CO., LTD.) 25 October 2007 See paragraphs [0016]-[0022] and figures 1-2.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 August 2017 (09.08.2017)

Date of mailing of the international search report

09 August 2017 (09.08.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/029958

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