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BARRIER STACKS FOR PRINTED AND/OR THIN FILM ELECTRONICS, METHODS
OF MANUFACTURING THE SAME, AND METHOD OF CONTROLLING A
THRESHOLD VOLTAGE OF A THIN FILM TRANSISTOR

CROSS REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of U.S. Provisional Patent Application No. 62/748,845, filed on October 22, 2018, incorporated herein by reference as if fully set forth herein.

FIELD OF THE INVENTION

[0002] The present invention generally relates to the field(s) of thin-film and/or printed transistors (TFTs). More specifically, embodiments of the present invention pertain to a barrier stack for thin film and/or printed electronics, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), on substrates having diffusible elements and/or species, structures adapted to control a threshold voltage (V_t) of a thin film and/or printed p-channel metal-oxide-semiconductor (PMOS) transistor, methods of manufacturing the same, and methods of controlling a V_t and/or inhibiting or preventing diffusion of a diffusible element or species in a substrate using the same.

DISCUSSION OF THE BACKGROUND

[0003] Wireless communication tags, such as RFID and/or security tags, may include labels with thin film and/or printed electronics. Such electronics may comprise an integrated circuit including a plurality of transistors (e.g., MOSFETs) and may be manufactured using printed and/or thin film doped polysilicon processing.

[0004] P-channel TFTs may have a threshold voltage (V_t) of 0 volts. When manufactured using thin film or printed processing, this V_t value may lead to high transistor off-state leakage, which impacts product performance and (where applicable) battery life. The possible causes of the high off-state leakage may include possible impurities and defects in the materials used to manufacture the TFT, dangling bonds, and possibly properties of the material used to form the source, drain and channel of the p-channel TFT. It is generally believed that the causes of off-state leakage in thin film and/or printed transistors is not circuit-related.

[0005] Unlike conventional complementary metal-oxide-semiconductor (CMOS) manufacturing processes on monolithic Si substrates, printed and thin film doped polysilicon processing may not include channel doping for V_t modulation. Thus, it can be difficult or impossible to control the V_t of certain TFTs.

[0006] FIG. 1 shows a conventional substrate with a barrier stack 100 comprising a stainless steel substrate 110, a thick AlN layer 120, an aluminosilicate insulator layer 130, and a thin AlN layer 140. The stainless steel substrate 110 provides a mechanical support for layers subsequently formed on it, but includes a number of diffusible elements or species, including iron and chromium atoms. The AlN layers 120 and 140 inhibit or prevent metal atoms from diffusing into structures (e.g., transistor channels) subsequently formed on or over the AlN layer 140.

[0007] This “Discussion of the Background” section is provided for background information only. The statements in this “Discussion of the Background” are not an admission that the subject matter disclosed in this “Discussion of the Background” section constitutes prior art to the present disclosure, and no part of this “Discussion of the Background” section may be used as an admission that any part of this application, including this “Discussion of the Background” section, constitutes prior art to the present disclosure.

SUMMARY OF THE INVENTION

[0008] In one aspect, the present invention relates to a device, comprising a substrate containing a diffusible element and/or species, a first barrier layer on the substrate, an insulator layer on the first barrier layer, a second barrier layer on the insulator layer in a first region of the substrate, and a third barrier layer on the insulator layer in a second region of the substrate and on the second barrier layer in the first region. Each of the second and third barrier layers has a thickness less than that of the first barrier layer.

[0009] In various embodiments, the substrate may comprise a metal foil. The metal foil may comprise stainless steel, aluminum, copper or titanium. In other or further embodiments, the first region is an NMOS transistor region, and the second region is a PMOS transistor region. In such embodiments, the device may further comprise a plurality of p-channel thin film transistors on the third barrier layer in the second region and a plurality of n-channel thin film transistors on the third barrier layer in the first region.

[0010] In some embodiments, the first barrier layer, the second barrier layer and the third barrier layer may independently comprise AlN, TiN, TiAlN, WN, or TiWN. In other or further embodiments, the first barrier layer may have a thickness of from 500 to 2000 Å, the second barrier layer may have a thickness of from 50 to 200 Å, and/or the third barrier layer may have a thickness of from 50 to 200 Å. In some examples, the second barrier layer and the third barrier layer have a combined thickness that is less than that of the first barrier layer.

[0011] In various embodiments, the insulator layer may comprise SiO₂, Al₂O₃, or an aluminosilicate. Any of the insulator layer materials may be doped with boron and/or phosphorus. The insulator layer may have a thickness of from 2000 to 15,000 Å. In further embodiments, the device comprises a plurality of first regions and a plurality of second regions, and the insulator layer includes a trench or recess in the second region.

[0012] In another aspect, the present invention relates to a method of manufacturing a barrier stack on a substrate, comprising forming, in sequence, a first barrier layer, an insulator layer, and a second barrier layer on a substrate containing a diffusible element and/or species, selectively removing the second barrier layer in one or more regions of the substrate, and blanket-depositing a third barrier layer in the one or more regions and on the second barrier layer in remaining region(s) of the substrate. The second barrier layer has a thickness less than that of the first barrier layer. In some embodiments, the method may further comprise forming p-channel thin film transistors in the one or more regions, and forming n-channel thin film transistors in the remaining region(s) of the substrate.

[0013] In some embodiments, selectively removing the second barrier layer in the one or more regions of the substrate may expose the insulator layer in the region(s), and blanket depositing the third barrier layer may include blanket-depositing the third barrier layer on the exposed insulator layer. In other embodiments, selectively removing the second barrier layer may include removing an amount of the second barrier layer equal to about half the thickness of the second barrier layer. In further embodiments, the second barrier layer may comprise a first thin barrier layer, an insulator layer, and a second thin barrier layer, and selectively removing the second barrier layer may include removing the insulator layer and the second thin barrier layer in the one or more regions. For example, the second barrier layer may be selectively removed using laser ablation.

[0014] In other or further embodiments, the method may further comprise partially etching the insulator layer to form a trench or recess, and forming a blocking mask in the remaining region(s) of the substrate prior to selectively removing the second barrier layer in the one or more regions. Alternatively, the method may further comprise oxidizing the second barrier layer in the one or more regions of the substrate to form an oxidized barrier layer, and selectively etching the oxidized barrier layer and the insulator layer to form the trench or recess. In further embodiments, the method may further comprise removing the blocking mask prior to blanket-depositing the third barrier layer. The blocking mask may be formed by blanket-depositing a photoresist and patterning the photoresist using photolithography.

[0015] In various embodiments, the first barrier layer, the second barrier layer, and the third barrier layer may independently comprise AlN, TiN, TiAlN, WN, or TiWN. In other or further embodiments, the substrate may comprise a metal foil, which can be selected from stainless steel, aluminum, copper or titanium. In some embodiments, the insulator layer may comprise SiO₂, Al₂O₃, or an aluminosilicate, any of which may be doped with boron and/or phosphorus.

[0016] In various embodiments, the first barrier layer, the insulator layer, and/or the second barrier layer are formed using blanket deposition. The first barrier layer may have a thickness of from 500 to 2000 Å. The insulator layer may have a thickness of from 2000 to 15,000 Å. The second barrier layer may have a thickness of from 50 to 200 Å. The third barrier layer may have a thickness of from 50 to 200 Å.

[0017] In other aspects, the present invention relates to a method of manufacturing a barrier stack, comprising forming, in sequence, a first barrier layer, an insulator layer, and a second barrier layer on a substrate containing a diffusible element and/or species, forming a blocking mask in one or more first regions of the substrate, and thinning the second barrier layer in the one or more first regions of the substrate without thinning the second barrier layer in one or more second regions of the substrate. The second barrier layer has a thickness less than that of the first barrier layer.

[0018] An ideal V_t for p-channel field effect transistors (PFETs) is about -0.5 V, since the leakage current may be lowered by orders of magnitude at an operating voltage of 0 V (V_{dd}). To solve the above problem (leakage current in PFETs at a V_t of about 0 V), altering

the thickness of the topmost AlN layer (e.g., the thin AlN layer 140 shown in FIG. 1) can modulate (i.e., increase or decrease) the amount of charge in the barrier layer stack, thus changing the electric field within the PFET channel. Using a blocking mask scheme, the thickness of the uppermost AlN layer can be varied between the NMOS transistor regions and the PMOS transistor regions to enable a reduction in the V_t of the PMOS transistors.

[0019] These and other advantages of the present invention will become readily apparent from the detailed description of various embodiments below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 shows a conventional barrier stack on a stainless steel substrate.

[0021] FIGS. 2A-E show cross-sections of intermediate and final barrier stacks, made in accordance with one or more exemplary embodiments of the present invention.

[0022] FIGS. 3A-C show cross-sections of intermediate and final barrier stacks in an exemplary method using a plasma treatment step, in accordance with one or more exemplary embodiments of the present invention.

[0023] FIGS. 4A-C show cross-sections of intermediate and final barrier stacks in an exemplary method using a deposition step, in accordance with one or more exemplary embodiments of the present invention.

[0024] FIG. 5 is a flow chart showing a method of forming a barrier stack on a substrate, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION

[0025] Reference will now be made in detail to various embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the following embodiments, it will be understood that the descriptions are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents that may be included within the spirit and scope of the invention. Furthermore, in the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be readily apparent to one skilled in the art that the present invention may be practiced without these specific details. In

other instances, well-known methods, procedures and components have not been described in detail so as not to unnecessarily obscure aspects of the present invention. Furthermore, it should be understood that the possible permutations and combinations described herein are not meant to limit the invention. Specifically, variations that are not inconsistent may be mixed and matched as desired.

[0026] For the sake of convenience and simplicity, the terms “mounting,” “affixing,” “attaching” and “securing” (and grammatical variations thereof) may be used interchangeably, as may the terms “wireless communication tag” and “wireless communication device,” the terms and the terms “fabric” and “textile,” but these terms are generally given their art-recognized meanings.

[0027] The term “length” generally refers to the largest dimension of a given 3-dimensional structure or feature. The term “width” generally refers to the second largest dimension of a given 3-dimensional structure or feature. The term “thickness” generally refers to a smallest dimension of a given 3-dimensional structure or feature. The length and the width, or the width and the thickness, may be the same in some cases (e.g., cylindrical structures such as optical fibers and certain other optical waveguides). A “major surface” refers to a surface defined by the two largest dimensions of a given structure or feature, which in the case of a structure or feature having a partially or completely circular or spherical surface, may be defined by the radius of the circle or sphere.

[0028] FIGS. 2A-C show the steps of an exemplary method of forming a substrate with a barrier stack 200. FIG. 2A shows the barrier stack 200 in an initial state. The barrier stack 200 comprises a substrate 210, a first barrier layer 220, an insulator layer 230, and a second barrier layer 240. The substrate 210 provides a mechanical support for layers subsequently formed thereon. The insulator layer 230 electrically insulates subsequently formed electrically active structures from the substrate 210 (e.g., when the substrate 210 comprises an electrically conductive material, such as stainless steel or aluminum foil). The first and second barrier layers 220 and 240 inhibit or prevent diffusible elements or species from diffusing into the subsequently formed structures.

[0029] The substrate 210 may comprise a metal foil such as stainless steel, aluminum, titanium, copper, etc. The insulator layer 230 may comprise SiO₂, Al₂O₃, or an aluminosilicate, any of which can be doped with boron and/or phosphorus. The first and

second barrier layers 220 and 240 may comprise AlN, TiN, TiAlN, WN, or TiWN. The first barrier layer 220 may be thicker than the second barrier layer 240. For example, the first barrier layer 220 may have a thickness of from 500 to 2000 Å, the insulator layer 230 may have a thickness of from 2000 to 15000 Å, and the second barrier layer 240 may have a thickness of from 50 to 200 Å. Each of the first barrier layer 220, the insulator layer 230 and the second barrier layer 240 may be formed by blanket deposition on the substrate 210 (and, optionally, additional processing, such as thermally reflowing the insulator layer 230, to make each surface smoother after the deposition step). A blocking mask 270 is formed in NMOS transistor regions 260 by blanket deposition (e.g., spin coating) and photolithographic patterning, thus exposing PMOS transistor regions 250. In an alternative embodiment, the blocking mask 270 may be selectively formed in the NMOS transistor regions 260 by printing (e.g., screen printing).

[0030] In FIG. 2B, the second barrier layer 240 and the insulator layer 230 are etched in the PMOS transistor regions 250 to form an etched barrier stack 200'. The second barrier layer 240 in the PMOS transistor regions 250 is removed, thus forming an etched and/or patterned second barrier layer 240' that remains in the NMOS transistor regions 250 and elsewhere (e.g., peripheral regions of the substrate 210). The insulator layer 230 is only partially etched or recessed, thus forming an etched insulator layer 230' and a trench or recess 235. The trench or recess 235 may have a depth of from 100 to 500 Å, or of from 5 to 50% of the thickness of the insulator layer 230. The blocking mask 270 is then stripped and/or removed (e.g., by ashing and cleaning).

[0031] In FIG. 2C, a third barrier layer 242 is blanket-deposited on the etched and unmasked barrier stack 200''. The third barrier layer 242 is blanket-deposited in the trench or recess 235 (on the upper surface of the etched insulator layer 230') and on the etched second barrier layer 240' (e.g., in the NMOS regions 260). The third barrier layer 242 may have a thickness of from 50 to 200 Å (e.g., about 75 Å). Thus, the uppermost layer of the barrier stack 200'' may include (i) the third barrier layer 242 alone in the PMOS transistor regions 250 and (ii) the combined second and third barrier layers 240' and 242 in the NMOS transistor regions 260. The combined second and third barrier layers 240' and 242 may have a thickness that is 1.2 to 5 times greater than the thickness of the third barrier layer 242 alone. The barrier stack 200'' is configured to lower the V_t of the p-channel TFTs subsequently formed in the PMOS transistor regions 250.

[0032] In an alternative embodiment, FIG. 2D shows a barrier stack 280 including a partially etched barrier layer 244 on the insulator layer 230. The blocking mask (e.g., the mask 270 shown in FIG. 2A) may be formed in the NMOS transistor regions 260 (e.g., using photolithography). The thin barrier layer 244 may have an original thickness of from, e.g., 100 to 500 Å, and the exposed portions of the thin barrier layer 244 in the PMOS transistor regions 250 may be partially etched to a depth of from 25 to 200 Å (e.g., 75 Å), or 5 to 75% (e.g., 50%) of the original thickness, thus forming the barrier stack 280. The partially etched barrier layer 244 may have a thickness of from 50 to 400 Å (e.g., 150 Å) in the PMOS transistor regions 250, and has its original thickness in the NMOS transistor regions 260. The blocking mask may then be stripped and/or removed (e.g., by ashing and cleaning). For example, the portions of the barrier layer 244 in the PMOS transistor regions 250 may have a thickness of from 25 to 200 Å (e.g., 75 Å), and the portions of the barrier layer 244 in the NMOS transistor regions 260 may have a thickness of from 50 to 400 Å (e.g., 150 Å).

[0033] In another alternative embodiment, FIG. 2E shows a barrier stack 290 comprising a trilayer. The trilayer comprises a first thin barrier layer 245, an SiO₂ or other insulator layer 247 (e.g., an etch stop layer), and a second thin barrier layer 249. The first and second thin barrier layers 245 and 249 may comprise AlN, TiN, TiAlN, WN, or TiWN. Each of the thin barrier layers 245 and 249 and the SiO₂ layer 247 may each have a thickness of from 50 to 200 Å. For example, the barrier layers 245 and 249 may each have a thickness of 75 Å and the insulator layer 247 may have a thickness of 50 Å. The exact thicknesses of the first and second thin barrier layers 245 and 249 depend on the material(s) of the first and second thin barrier layers 245 and 249 and the desired V_t and/or amount of V_t adjustment in the PMOS transistor regions 250.

[0034] The blocking mask (e.g., the mask 270 shown in FIG. 2A) may be formed in the NMOS transistor regions 260 as described herein. The portions of the second thin barrier layer 249 in the PMOS transistor regions 250 may be completely and selectively etched (e.g., removed), stopping at the insulator layer 247. The insulator layer 247 in the PMOS transistor regions 250 is then completely and selectively etched, stopping at the first thin barrier layer 245. The second thin barrier layer 249 can be selectively etched with respect to the insulator layer 247. The insulator layer 247 can then be selectively etched with respect to the first thin barrier layer 245. The selective etch chemistries for etching the second thin barrier layer 249 and the insulator layer 247 are known, but depend on the specific materials of the second thin

barrier layer 249, the insulator layer 247 and the first thin barrier layer 245. Thus, the embodiment exemplified in FIG. 2E provides a barrier stack 290 with the first thin barrier layer 245 in the PMOS transistor regions 250 and the trilayer (comprising the thin barrier layers 245 and 249 and the insulator layer 247) in the NMOS transistor regions 260.

[0035] In yet another alternative embodiment, the second barrier layer 240 (FIG. 2A) may have a thickness of from 50 to 200 Å (e.g., 75 Å) across the entire device, and the second (thin) barrier layer 240 in the PMOS transistor regions 250 may be selectively laser ablated, without laser ablating the second (thin) barrier layer 240 or using the blocking mask 270 in the NMOS transistor regions 260. For example, the laser ablation of the second barrier layer 240 in the PMOS transistor regions 250 may be conducted until it is completely removed. The third barrier layer 242 is then blanket-deposited on the insulator layer 230 in the PMOS transistor regions 250 and the remaining portion of the second barrier layer 240 in the NMOS transistor regions 260, resulting in the third barrier layer 242 alone in the PMOS transistor regions 250 and a combination of the second and third barrier layers 240 and 242 in the NMOS transistor regions 260. The third barrier layer 242 alone may have a thickness of from 50 to 200 Å (e.g., 75 Å), and the second and third barrier layers 240 and 242 together may have a combined thickness of from 100 to 400 Å (e.g., 150 Å).

[0036] FIGS. 3A-C show cross-sections of intermediate and final products in an exemplary method of forming trenches or recesses 235a-c in the barrier stack 200 using an oxygen plasma 320. The second barrier layer 240 and the insulator layer 230 are shown, and are similar or identical to the structures described with respect to the barrier stack 200 in FIG. 2A. The first barrier layer 220 and the substrate 210 (not shown) are under the insulator layer 230, as shown in FIG. 2A.

[0037] In FIG. 3A, the oxygen plasma 320 converts regions of the second barrier layer 240 exposed through a shadow mask 310 to a different material that can be selectively etched with respect to the barrier layer 240. For example, if the second barrier layer 240 comprises a metal nitride (e.g., AlN), the exposed regions of the second barrier layer 240 may be oxidized to the corresponding metal oxide (e.g., Al₂O₃). The source of the oxygen plasma 320 may include oxygen (O₂) and/or ozone (O₃) at a flow rate of from 0.01 to 1 sccm, but other gases (e.g., a nitrogen oxide, such as NO₂, NO or N₂O) may be used as well. An RF power of from 100 to 2000 W may be applied to electrodes in the plasma processing

equipment to form the plasma 320. The plasma 320 may be formed and the oxidation conducted at a temperature of from room temperature to 700 °C.

[0038] In FIG. 3B, the mask 310 is removed, and the oxidized portions 330a-c of the second barrier layer 245a-c are selectively etched (e.g., by wet etching). The etchant may include dilute and/or buffered KOH, NaOH, or ammonium hydroxide. The etching may be performed at a temperature of from room temperature to about 100 °C and for a duration of time sufficient to remove the oxidized portions 330a-c without substantially removing the second barrier layer 245a-c. Optionally, the barrier stack 200 may be overetched such that part of the insulator layer 230 is removed. For example, the insulator layer 230 may be etched to a depth of from 5% to 50% of the thickness of the insulator layer 230.

[0039] In FIG. 3C, the oxidized portions 330a-c are completely removed, and the insulator layer 230 is partially etched, to form trenches or recesses 235a-c (e.g., similar or identical to the trench or recess 235 in FIG. 2B). The trenches or recesses 235a-c may have a depth of from 100 to 500 Å, or of from 5 to 50% of the thickness of the insulator layer 230. The third barrier layer 242 may then be deposited in the trenches or recesses 235a-c and on the second barrier layer 245a-c, as shown in FIG. 2C.

[0040] FIGS. 4A-C show cross-sections of intermediate and final products in an exemplary method of forming trenches or recesses 435a-c in the barrier stack 200 using a shadow mask 410 and a selective deposition process 420. The second barrier layer 240 and the insulator layer 230 are shown, and are similar or identical to the structures described with respect to the barrier stack 200 in FIG. 2A. The first barrier layer 220 and the substrate 210 (not shown) are under the insulator layer 230, as shown in FIG. 2A.

[0041] In FIG. 4A, an ink 420 for an etching mask is deposited on regions of the second barrier layer 240 exposed through the shadow mask 410. The ink 420 may comprise a carbon-based (e.g., olefinic) resist or other polymer, and may be deposited by screen printing through the shadow mask 410. After selective deposition, the mask 410 may be removed and the ink 420 may be hardened or cured conventionally (e.g., by heat and/or radiation).

[0042] FIG. 4B shows a patterned mask 430a-c formed by the deposited and hardened or cured ink 420 for a subsequent etching step. The regions of the second barrier layer 240 that are exposed by the islands 430a-c (e.g., the regions that were covered by the shadow

mask 410 in FIG. 4A) are selectively etched. The etchant may include a wet etchant such as dilute KOH, NaOH, or ammonium hydroxide, but is not limited thereto. The etching may be performed at a temperature of from room temperature to about 100 °C and for a duration of time sufficient to remove the regions of the second barrier layer 240 that are exposed by the islands 430a-c without substantially removing the mask 430a-c. Optionally, the barrier stack 200 may be overetched such that part of the insulator layer 230 is removed.

[0043] In FIG. 4C, the regions of the second barrier layer 240 that are exposed by the islands 430a-c are completely etched, and the insulator layer 230 is partially etched, to form the trenches or recesses 235d-f (e.g., similar or identical to the trench or recess 235 in FIG. 2B). The trenches or recesses 235d-f may have a depth of from 100 to 500 Å, or of from 5 to 50% of the thickness of the insulator layer 230. The third barrier layer 242 may then be deposited in the trenches or recesses 235d-f and on the second barrier layer 245a'-c'.

[0044] FIG. 5 is a flow chart 500 showing exemplary methods of forming a barrier stack on a substrate. At 510, a barrier stack is formed on the substrate, generally by blanket deposition. The barrier stack comprises a first barrier layer, an insulator layer, and a second barrier layer as described herein. The substrate may comprise a metal foil such as stainless steel, copper, aluminum, titanium, etc. The first and second barrier layers may comprise a metal nitride such as AlN, TiN, TiAlN, WN, or TiWN, or a metal alloy such as TiW. The insulator layer may comprise SiO₂, Al₂O₃, or an aluminosilicate, any of which may be doped with boron and/or phosphorus. The second barrier layer has a thickness that is less than that of the first barrier layer.

[0045] At 520, a blocking mask is formed in NMOS transistor regions of the barrier stack. The blocking mask may be formed by blanket-depositing a photoresist and patterning the photoresist using photolithography. Alternatively, the patterned photoresist may be formed by printing (e.g., screen printing). After forming the patterned photoresist, the method may proceed in one of two alternative paths. The first path includes steps 530, 535 and 550, and the second path includes steps 540, 542, 544 and 550.

[0046] If the first path is chosen, at 530, the second barrier layer is etched, and optionally, the insulator layer is partially etched in the PMOS transistor regions to form one or more trenches or recesses. The etchant may be a wet etchant such as dilute KOH, NaOH, or ammonium hydroxide. The etch may be performed at a temperature of from room

temperature to about 100 °C and for a duration of time sufficient to remove the exposed portions of the second barrier layer. At 535, the blocking mask is removed from the NMOS transistor regions. The blocking mask may be removed by ashing and cleaning (e.g., using high temperatures and oxygen to burn or combust the mask, then removing remaining residue from the etched surface of the barrier stack).

[0047] If the second path is chosen, at 540, the regions of the second barrier layer exposed in the PMOS transistor regions of the substrate are oxidized using an oxygen plasma. For example, if the second barrier layer comprises a metal nitride (e.g., AlN), the exposed regions of the second barrier layer may be oxidized to the corresponding metal oxide (e.g., Al₂O₃). The source of the oxygen plasma may include oxygen gas (O₂) or ozone gas (O₃). The oxygen plasma may be at room temperature or heated to a temperature of up to 700 °C using electrodes having an RF power of from 100 to 2000 W. The oxygen plasma may have a flow rate of from 0.01 to 1 sccm.

[0048] At 542, the blocking mask is removed from the NMOS transistor regions. The blocking mask may be removed by ashing and cleaning (e.g., using high temperatures to combust the mask and blowing the dust off the surfaces of the barrier stack).

[0049] At 544, the oxidized portions of the second barrier layer are selectively wet etched to form one or more trenches or recesses (e.g., similar or identical to the trench or recess 235 in FIG. 2B). The etchant may include dilute KOH, NaOH, or ammonium hydroxide. The etching may be performed at room temperature or a temperature up to about 100 °C and a duration of time sufficient to remove the oxidized portions without substantially removing the second barrier layer. The trenches or recesses may have a depth of from 100 to 500 Å, or of from 5 to 50% of the thickness of the insulator layer. Alternatively, the blocking mask may be removed after the oxidized barrier layer is etched.

[0050] At 550, a third barrier layer may be deposited in the trenches or recesses formed in the PMOS transistor regions of the substrate and on the second barrier layer in the NMOS transistor regions of the substrate. The third barrier layer may be substantially similar or identical to the second barrier layer with regard to thickness and material.

CONCLUSION

[0051] The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be

exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

CLAIMS

What is claimed is:

1. A device, comprising:
 - a substrate containing a diffusible element and/or species;
 - a first barrier layer on the substrate;
 - an insulator layer on the first barrier layer;
 - a second barrier layer on the insulator layer in a first region of the substrate, the second barrier layer having a thickness less than that of the first barrier layer; and
 - a third barrier layer on the insulator layer in a second region of the substrate and on the second barrier layer in the first region, the third barrier layer having a thickness less than that of the first barrier layer.
2. The device of claim 1, wherein the first barrier layer, the second barrier layer and the third barrier layer comprise AlN, TiN, TiAlN, WN, or TiWN.
3. The device of claim 1, wherein the substrate comprises a metal foil.
4. The device of claim 1, wherein the insulator layer comprises SiO₂, Al₂O₃, or an aluminosilicate, any of which may be doped with boron and/or phosphorus.
5. The device of claim 1, wherein the insulator layer has a thickness of from 2000 to 15,000 Å, the first barrier layer has a thickness of from 500 to 2000 Å, the second barrier layer has a thickness of from 50 to 200 Å, and/or the third barrier layer has a thickness of from 50 to 200 Å.
6. The device of claim 1, further comprising a plurality of p-channel thin film transistors on the third barrier layer in the second region, and a plurality of n-channel thin film transistors on the third barrier layer in the first region.
7. The device of claim 1, wherein the second barrier layer and the third barrier layer have a combined thickness that is less than that of the first barrier layer.
8. The device of claim 1, wherein the insulator layer includes a trench or recess in the second region.
9. A method of manufacturing a barrier stack on a substrate, comprising:
 - forming, in sequence, a first barrier layer, a first insulator layer, and a second barrier layer on a substrate containing a diffusible element and/or species, wherein the second barrier layer has a thickness less than that of the first barrier layer;
 - selectively removing the second barrier layer in one or more regions of the substrate; and

blanket-depositing a third barrier layer in the one or more regions and on the second barrier layer in remaining region(s) of the substrate.

10. The method of claim 9, wherein selectively removing the second barrier layer in the one or more regions of the substrate exposes the first insulator layer in said one or more regions, and blanket depositing the third barrier layer includes blanket-depositing the third barrier layer on the insulator layer.
11. The method of claim 9, wherein the second barrier layer comprises a first thin barrier layer, a second insulator layer, and a second thin barrier layer, and selectively removing the second barrier layer in the one or more regions of the substrate includes removing the second insulator layer and the second thin barrier layer in the one or more regions of the substrate.
12. The method of claim 9, further comprising partially etching the insulator layer to form a trench or recess.
13. The method of claim 9, further comprising forming a blocking mask in the remaining region(s) of the substrate prior to selectively removing the second barrier layer in the one or more regions.
14. The method of claim 9, wherein the first barrier layer, the second barrier layer, and the third barrier layer independently comprise AlN, TiN, TiAlN, WN, or TiWN.
15. The method of claim 9, wherein the substrate comprises a metal foil.
16. The method of claim 9, wherein the insulator layer comprises an SiO₂, Al₂O₃, or an aluminosilicate, any of which may be doped with boron and/or phosphorus.
17. The method of claim 9, wherein the first barrier layer, the insulator layer, and the second barrier layer are formed using blanket deposition.
18. The method of claim 9, wherein the insulator layer has a thickness of from 2000 to 15,000 Å, the first barrier layer has a thickness of from 500 to 2000 Å, the second barrier layer has a thickness of from 50 to 200 Å, and/or the third barrier layer has a thickness of from 50 to 200 Å.
19. The method of claim 16, further comprising forming p-channel thin film transistors in the one or more regions of the substrate, and forming n-channel thin film transistors in the remaining region(s) of the substrate.
20. A method of manufacturing a barrier stack, comprising:

forming, in sequence, a first barrier layer, an insulator layer, and a second barrier layer on a substrate containing a diffusible element and/or species, wherein the second barrier layer has a thickness less than the first barrier layer;

forming a blocking mask in one or more first regions of the substrate; and

thinning the second barrier layer in the one or more first regions of the substrate without thinning the second barrier layer in one or more second regions of the substrate.

FIG. 1

100

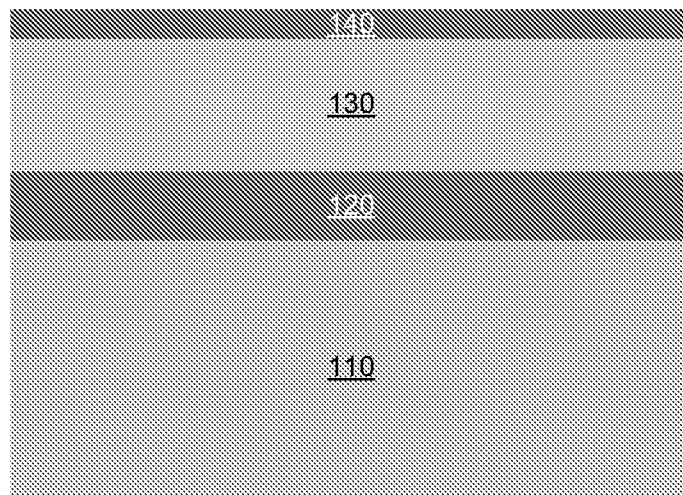



FIG. 2A

250 200 260

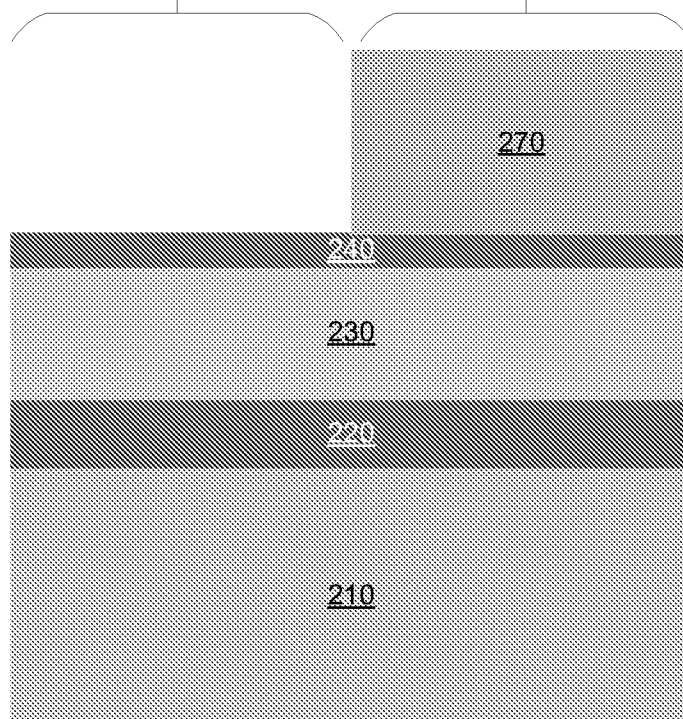



FIG. 2B

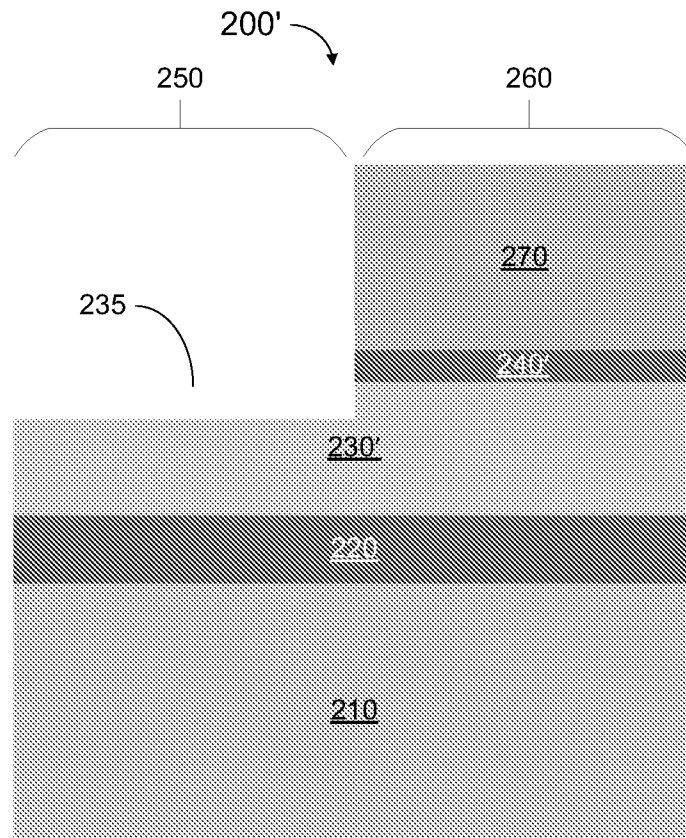


FIG. 2C

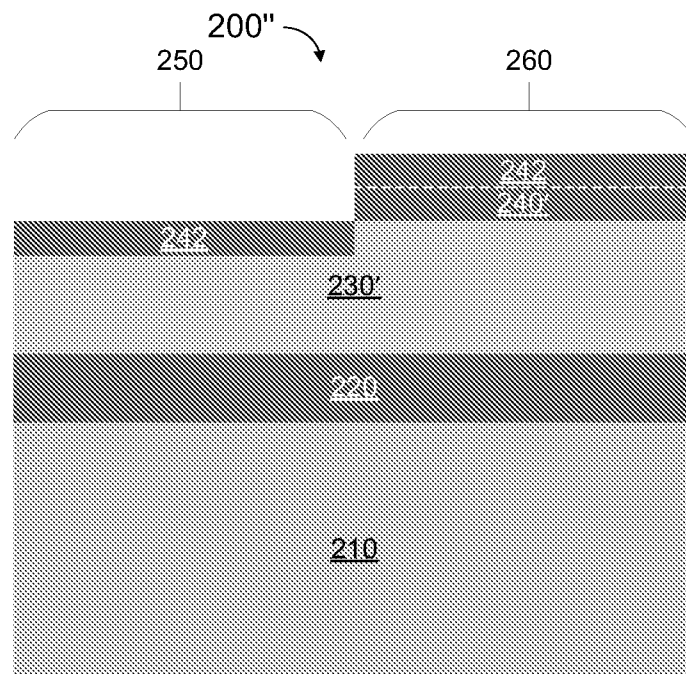


FIG. 2D

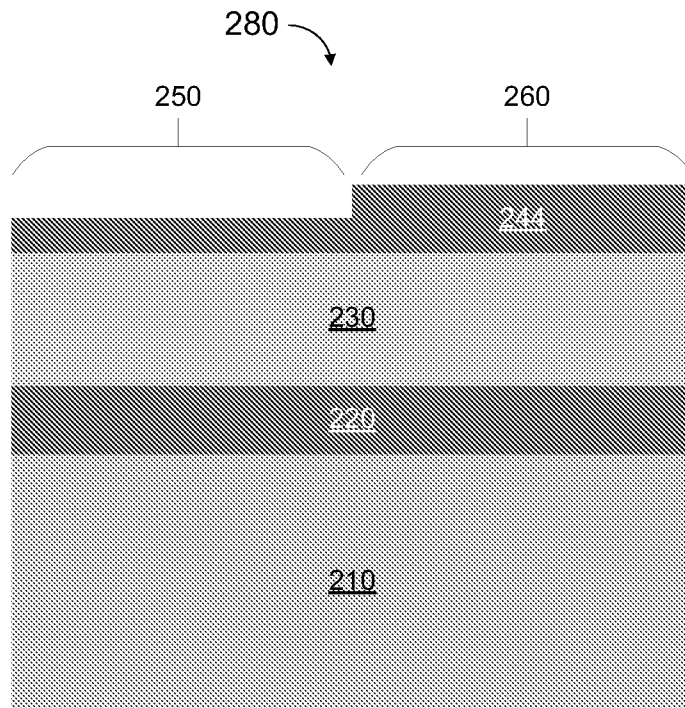


FIG. 2E

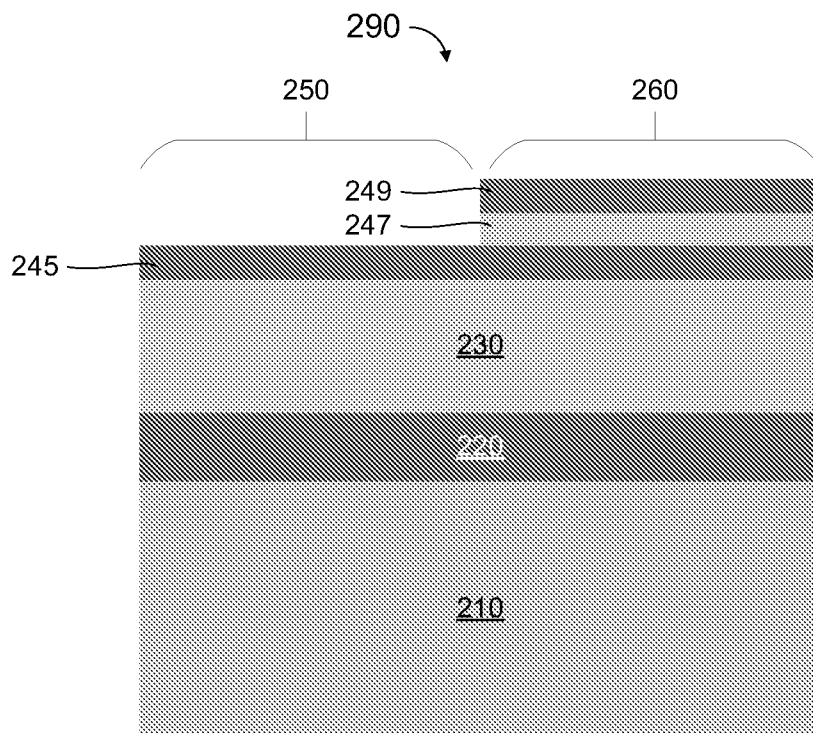


FIG. 3A

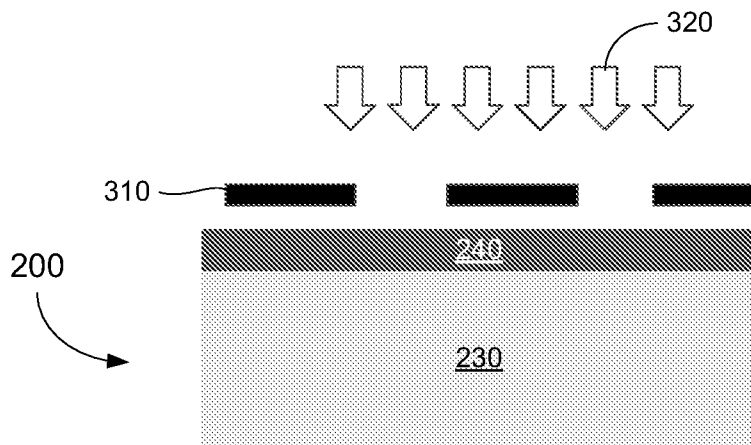


FIG. 3B

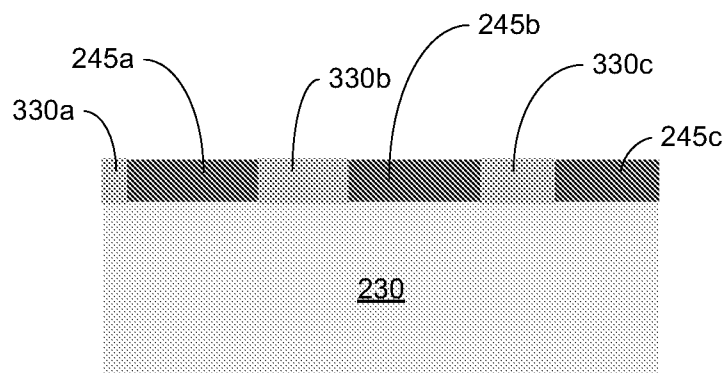


FIG. 3C

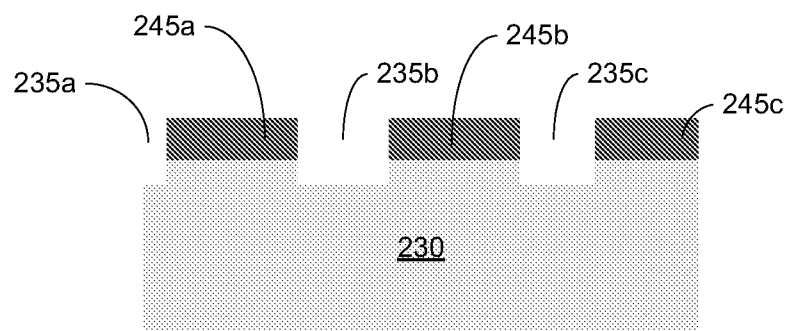


FIG. 4A

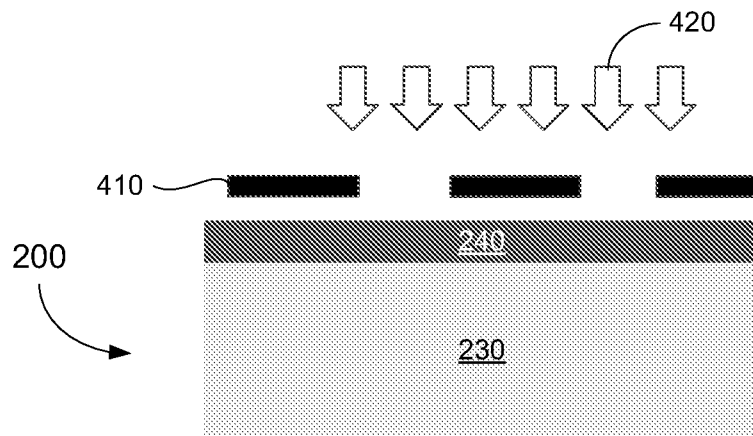


FIG. 4B

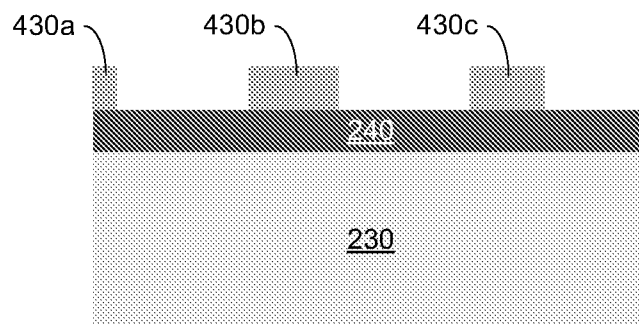


FIG. 4C

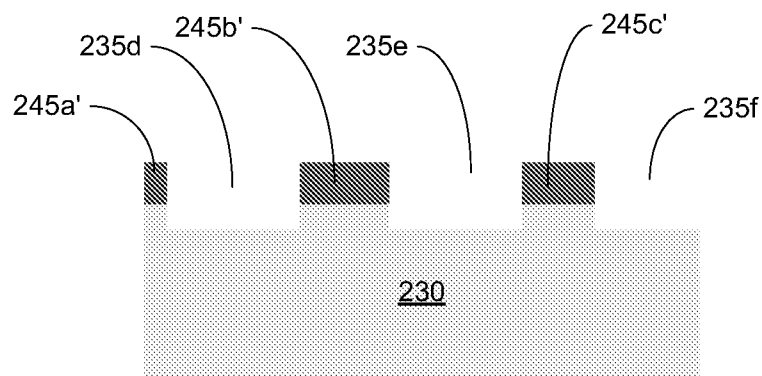
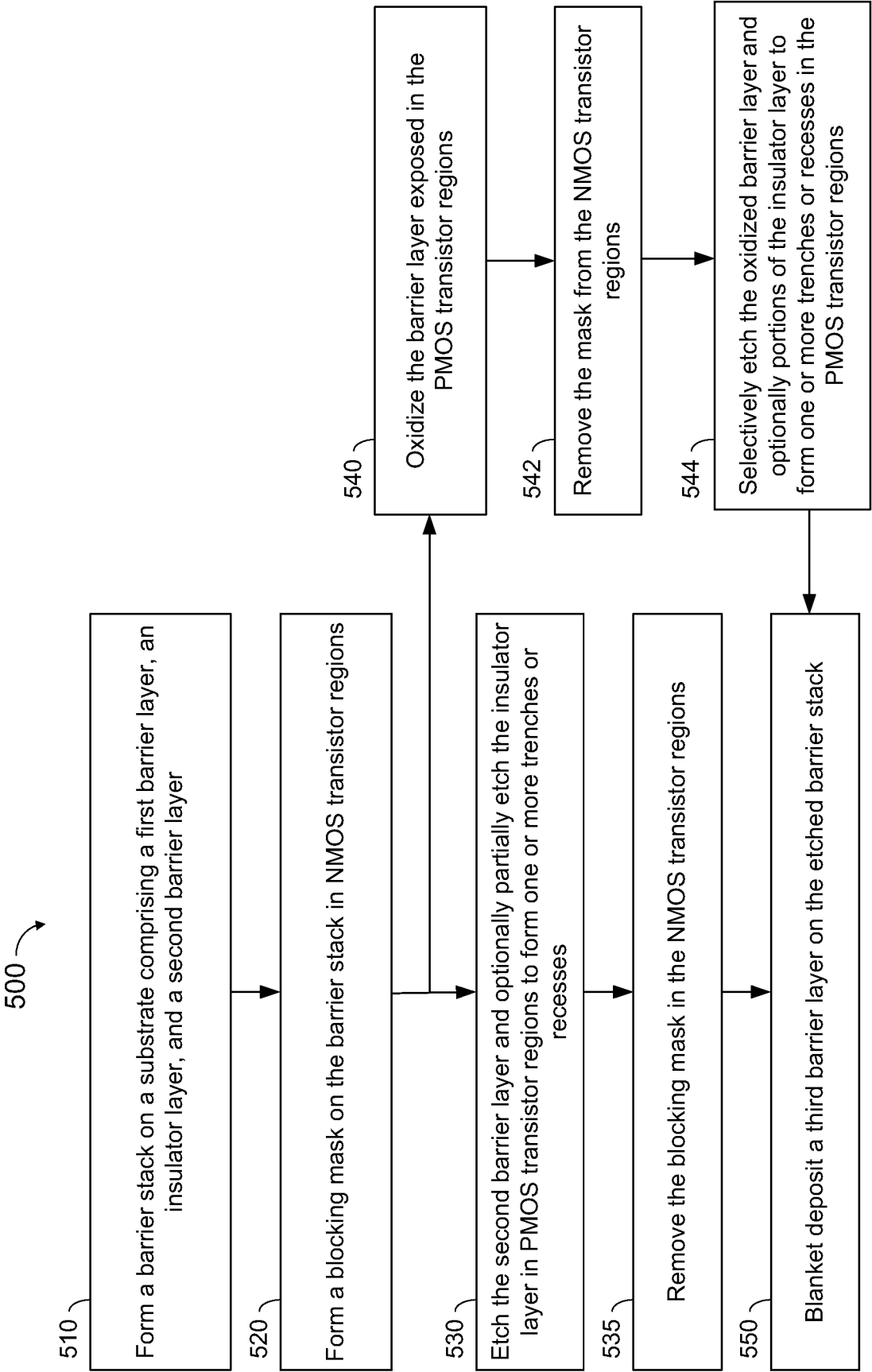


FIG. 5



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2019/057359

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/768; H01L 23/532; H01L 29/786 (2019.01)

CPC - H01L 21/76865; H01L 21/76838; H01L 21/7685; H01L 23/53223; H01L 23/53238; H01L 29/78606; H01L 2221/1078 (2019.08)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 257/751; 438/653 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7,470,992 B2 (THEI et al) 30 December 2008 (30.12.2008) entire document	1-5, 7, 8
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Y		6, 9-20
Y	US 9,299,704 B2 (SK HYNIX INC.) 29 March 2016 (29.03.2016) entire document	6, 19
Y	US 5,354,712 A (HO et al) 11 October 1994 (11.10.1994) entire document	9-20
A	US 8,963,227 B2 (LIM et al) 24 February 2015 (24.02.2015) entire document	1-20
A	KR 100383756 B1 (HYNIX SEMICONDUCTOR INC) 14 May 2003 (14.05.2003) machine translation	1-20

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

11 December 2019

Date of mailing of the international search report

09 JAN 2020

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