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10-2012-0006617 20 January 2012 (20.01.2012) KR(71) Applicant (for all designated States except US): **IN-
NOWIRELESS CO., LTD.** [KR/KR]; 201&301, First-
Building, PanGyo-Sevenventurevalley 2-development,
633, Sampyeong-dong, Bundang-gu, Seongnam-si,
Gyeonggi-do 463-400 (KR).

(72) Inventors; and

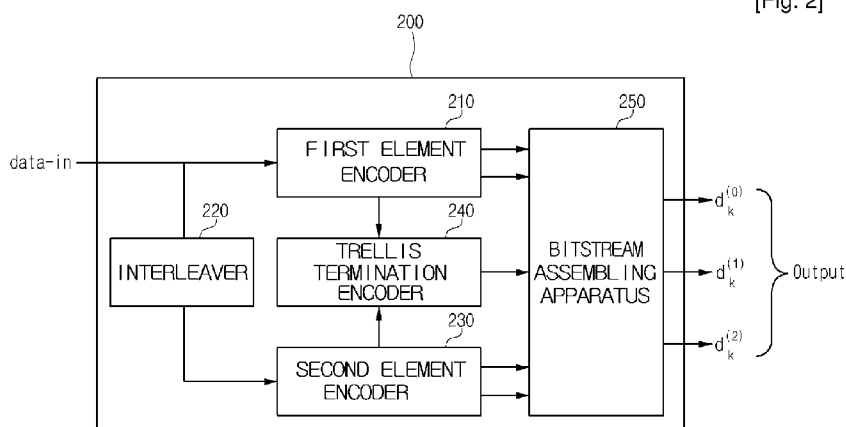
(75) Inventors/Applicants (for US only): **JOUNG, Jinsoup**
[KR/KR]; 103, Daelim Villa, 277, Gumi-dong, Bun-
dang-gu, Seongnam-si, Gyeonggi-do 463-500 (KR). **LEE,
Joohyeong** [KR/KR]; 101-801, Hyundai Hiperion, Dogok
1-dong, Gangnam-gu, Seoul 135-270 (KR). **LIM, Jongho**
[KR/KR]; 2-1005, Jangmi Apt., Jamsil 6-dong, Songpa-gu,
Seoul 138-796 (KR). **YOOK, Seungkeun** [KR/KR]; 104-
1406, Hanseong Apt., 769-1, Singil 7-dong, Yeongdeung-
po-gu, Seoul 150-057 (KR). **SHIN, Ji Hye** [KR/KR]; 106-1501, Donga Apt., Seonghyeon-dong, Gwanak-gu, Seoul
151-055 (KR).(74) Agent: **DARAE IP FIRM**; (KIPS, Yeoksam-dong), 10th
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(54) Title: TURBO ENCODER APPARATUS

[Fig. 2]



(57) Abstract: Disclosed is a turbo encoder apparatus using an improved signal processing method in order to enhance a speed of a turbo encoder used in a channel coding technology. There are effects of reducing a time spent for performing an encoding by performing the encoding in the unit of plural bits every clock cycle and performing a turbo encoding with a structure optimized for a total signal processing processor through the assembly of input forms of encoding output bitstreams in a subsequent signal processing step for encoding through the bitstream assembling apparatus.

Description

Title of Invention: TURBO ENCODER APPARATUS

Technical Field

- [1] The present invention relates to a turbo encoder apparatus, and more particularly to a turbo encoder apparatus using an improved signal processing method in order to enhance a speed of a turbo encoder used in a channel coding technology.

Background Art

- [2] In general, a channel coding such as a turbo coding is used to increase the transmission efficiency of data in a communication system.
- [3] FIG. 1 is a block diagram illustrating a construction of a conventional turbo encoder. Referring to FIG. 1, the conventional turbo encoder 100 includes an internal interleaver 110 and two 8-state element encoders 120 and 130.
- [4] The conventional turbo encoder 100 performs a channel coding by using a Parallel Concatenated Convolutional Code (PCCC).
- [5] A transfer function of the 8-state element encoders 120 and 130 is defined as follows.
- [6] $G(D) = [1, g_1(D)/g_0(D)]^{g_0(D)=1+D^2+D^3, g_1(D)=1+D+D^3}$
- [7] Initial values of shift registers used in the 8-state element encoders 120 and 130 are all 0. Outputs of the conventional turbo encoder 100 are as follows.
- [8] $d_k^{(0)} = x_k, d_k^{(1)} = z_k, d_k^{(2)} = z'_k, k=0,1,2,\dots,(K-1)$
- [9] When a code block, which should be encoded, is a 0th code block, if the number of filler bits, which should be inserted, is larger than 0 (that is, $F>0$), inputs of the conventional turbo encoder 100 are $C_k=0, k=0,\dots,(F-1)$ and outputs are

$$d_k^{(0)} = \langle \text{Null} \rangle, k=0,\dots,(F-1), d_k^{(1)} = \langle \text{Null} \rangle, k=0,\dots,(F-1).$$

- [10] An input bitstream of the conventional turbo encoder 100 is represented as $C_0, C_1, C_2, C_3, \dots, C_{k-1}$ and output bitstreams of first and second 8-state element encoders 120 and 130 are represented as $Z_0, Z_1, Z_2, Z_3, \dots, Z_{k-1}$ and $Z'_0, Z'_1, Z'_2, Z'_3, \dots, Z'_{k-1}$, respectively. Outputs of the internal interleaver 110 of the turbo encoder are represented as $C'_0, C'_1, C'_2, \dots, C'_{k-1}$, and $C'_0, C'_1, C'_2, \dots, C'_{k-1}$ become inputs of the second 8-state element

encoder 130.

- [11] When the inputs of the internal interleaver 110 of the conventional turbo encoder 100 are $C_0, C_1, C_2, \dots, C_{k-1}$ and the outputs of the internal interleaver 110 of the conventional turbo encoder 100 are $C'_0, C'_1, C'_2, \dots, C'_{k-1}$, the relation between the input and the output is as follows.

$$[12] \quad C'_i = C_{\Pi(i)}, i = 0, 1, \dots, (K-1)$$

- [13] In the above equation, an index of the input bistream and an index of the output bitstream are calculated as defined in the below equation.

$$[14] \quad \Pi(i) = (f_1 * i + f_2 * i^2) \bmod K$$

- [15] A trellis termination is performed by taking three shift register values indicating the state after all input bitstreams have been encoded as a final input bit. The final input bit is added to the back of the output bitstream after the input bitstreams have been fully encoded.

- [16] First three final bits should be used when the first 8-state element encoder 120 is terminated in a state where an operation of the second 8-state element encoder 130 is stopped. That is, a switch included in the first 8-state element encoder 120 is connected to a lower side.

- [17] Last three final bits should be used when the second 8-state element encoder 130 is terminated in a state where an operation of the first 8-state element encoder 120 is stopped. That is, a switch included in the second 8-state element encoder 130 is connected to a lower side.

- [18] Trellis termination bitstreams added to outputs are as follows.

$$[19] \quad d_k^{(0)} = x_k, d_{k+1}^{(0)} = z_{k+1}, d_{k+2}^{(0)} = x'_{k+1}, d_{k+3}^{(0)} = z'_{k+1}$$

$$[20] \quad d_k^{(1)} = z_k, d_{k+1}^{(1)} = x_{k+2}, d_{k+2}^{(1)} = z'_{k+1}, d_{k+3}^{(1)} = x'_{k+2}$$

$$[21] \quad d_k^{(2)} = x_{k+1}, d_{k+1}^{(2)} = z_{k+2}, d_{k+2}^{(2)} = x'_{k+2}, d_{k+3}^{(2)} = z'_{k+3}$$

- [22] The number of sizes (K) of input bitstreams, which can be encoded at one time, is a total of 188, and K can have values shown in the below table.

- [23] [Table 1]

- [24]

i	K_i	i	K_i	i	K_i	i	K_i
1	40	48	416	95	1120	142	3200
2	48	49	424	96	1152	143	3264
3	56	50	432	97	1184	144	3328
4	64	51	440	98	1216	145	3392
5	72	52	448	99	1248	146	3456
6	80	53	456	100	1280	147	3520
7	88	54	464	101	1312	148	3584
8	96	55	472	102	1344	149	3648
9	104	56	480	103	1376	150	3712
10	112	57	488	104	1408	151	3776
11	120	58	496	105	1440	152	3840
12	128	59	504	106	1472	153	3904
13	136	60	512	107	1504	154	3968
14	144	61	528	108	1536	155	4032
15	152	62	544	109	1568	156	4096
16	160	63	560	110	1600	157	4160
17	168	64	576	111	1632	158	4224
18	176	65	592	112	1664	159	4288
19	184	66	608	113	1696	160	4352
20	192	67	624	114	1728	161	4416
21	200	68	640	115	1760	162	4480
22	208	69	656	116	1792	163	4544
23	216	70	672	117	1824	164	4608
24	224	71	688	118	1856	165	4672
25	232	72	704	119	1888	166	4736
26	240	73	720	120	1920	167	4800
27	248	74	736	121	1952	168	4864
28	256	75	752	122	1984	169	4928
29	264	76	768	123	2016	170	4992
30	272	77	784	124	2048	171	5056
31	280	78	800	125	2112	172	5120
32	288	79	816	126	2176	173	5184
33	296	80	832	127	2240	174	5248
34	304	81	848	128	2304	175	5312
35	312	82	864	129	2368	176	5376
36	320	83	880	130	2432	177	5440
37	328	84	896	131	2496	178	5504
38	336	85	912	132	2560	179	5568
39	344	86	928	133	2624	180	5632
40	352	87	944	134	2688	181	5696
41	360	88	960	135	2752	182	5760
42	368	89	976	136	2816	183	5824
43	376	90	992	137	2880	184	5888
44	384	91	1008	138	2944	185	5952
45	392	92	1024	139	3008	186	6016
46	400	93	1056	140	3072	187	6080
47	408	94	1088	141	3136	188	6144

- [25] A maximum size (K) of the code block is 6144 bits. In this case, the time spent for generating an output bitstream by encoding an input bitstream corresponds to a 6144+3+3 clock cycle in the implementation of hardware. When the time is calculated based on a basic sampling frequency (30.72 MHz) in LTE or LTE-Advanced, the time of about 200.2 us is required and the time corresponds to one subframe of about 20%.
- [26] Further, three code blocks, which are outputs of the conventional turbo encoder 100, should be converted to a structure body in the unit of 32 bits before entering a rate

matching, which is a next signal processing step, and insufficient bits are filled with null bit.

- [27] However, the conventional turbo encoder 100 takes a long time for encoding since the conventional turbo encoder 100 performs the encoding in the unit of bits.

Disclosure of Invention

Technical Problem

- [28] An aspect of the present invention provides a turbo encoder apparatus, which is implemented to perform an encoding in the unit of plural bits and reconstructs forms of an input bitstream and an output bitstream satisfying a code block size and a trellis termination method are satisfied.

Solution to Problem

- [29] In accordance with an aspect of the present invention, there is provided a turbo encoder apparatus for receiving an input of data and outputting encoded bitstreams, the turbo encoder apparatus including a first element encoder for receiving an input of a bitstream of the data, which has a size of a designated code block and in which a padding has been implemented, in the unit of plural bits, encoding the input of the bitstream of the data, and generating a first output bitstream in the unit of plural bits; an internal interleaver for generating an interleaved input bitstream from the bitstream of the data; a second element encoder for receiving an input of the interleaved input bitstream in the unit of plural bits, encoding the input of the interleaved input bitstream, and generating a second output bitstream in the unit of plural bits; a trellis termination encoder for generating bits for trellis terminations of the first element encoder and the second element encoder; and a bitstream assembling apparatus for receiving the first output bitstream, the second output bitstream, and the bits for the trellis terminations and generating an input bitstream for a rate matching.
- [30] The first element encoder and the second element encoder may receive an input of the bitstream of the data constructed in the unit of 8 bits, and the plural bits are 8 bits.
- [31] The first element encoder may generate the first output bitstream by using the bitstream of the data and an internal state of the first element encoder, and the second element encoder may generate the second output bitstream by using the interleaved input bitstream and an internal state of the second element encoder.
- [32] The first element encoder or the second element encoder may represent null bits, which exist in the first output bitstream or the second output bitstream in equal number to a number of filler bits existing in the bitstream of the data, as "0".
- [33] The trellis termination encoder may generate the bits for the trellis termination by using an internal state when a last input bitstream for the data is input to the first element encoder or the second element encoder.

[34] The bitstream assembling apparatus may rearrange the input bitstream of the rate matching in such a manner that the rate matching can be performed in parallel.

[35] The bitstream assembling apparatus may insert as many null bits as a number determined by the size of the code block into the input bitstream of the rate matching and adds the bits for the trellis termination to the first output bitstream or the second output bitstream, wherein the null bits are inserted by changing positions of upper 4 bits and lower 4 bits in a 8 bit unit of the first output bitstream or the second output bitstream, delaying the lower 4 bits by one cycle, and making the passing the lower 4 bits pass through a cycle delay circuit according to a number of null bits, which should be added.

[36] Specific matters of other embodiments are included in the detailed description and drawings.

Advantageous Effects of Invention

[37] The present invention has an effect of reducing the time spent for performing the encoding by enabling the encoding to be performed in the unit of plural bits every clock cycle.

[38] Further, the present invention has an effect of performing a turbo encoding with a structure optimized for a total signal processing processor through the assembly of input forms of encoding output bitstreams in a subsequent signal processing step for encoding through the bitstream assembling apparatus.

[39] Furthermore, the present invention has an effect of generating bits for the trellis termination in one clock cycle.

Brief Description of Drawings

[40] The foregoing and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

[41] FIG. 1 is a block diagram illustrating a construction of the conventional turbo encoder;

[42] FIG. 2 is a block diagram illustrating a construction of a turbo encoder according to an embodiment of the present invention;

[43] FIG. 3 is a block diagram illustrating a structure of an input bitstream according to an embodiment of the present invention;

[44] FIG. 4 is a block diagram illustrating a structure of a bitstream input to a bitstream assembling apparatus according to an embodiment of the present invention;

[45] FIG. 5 is a block diagram illustrating a structure of an output bitstream of a bitstream assembling apparatus according to an embodiment of the present invention;

[46] FIG. 6 is a block diagram illustrating a construction of an element encoder circuit

according to an embodiment of the present invention;

[47] FIG. 7 is a block diagram illustrating a construction of a trellis termination encoder circuit according to an embodiment of the present invention; and

[48] FIG. 8 is a block diagram illustrating a construction of a bitstream assembling apparatus according to an embodiment of the present invention.

Mode for the Invention

[49] The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings. While the detailed description of the present invention has described certain exemplary embodiments such as a portable terminal, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. Meanwhile, the terms used herein are only for describing embodiments of the present invention and do not limit the present invention.

[50] FIG. 2 is a block diagram illustrating a construction of a turbo encoder according to an embodiment of the present invention. Referring to FIG. 2, the turbo encoder 200 according to the embodiment of the present invention includes a first element encoder 210, an internal interleaver 220, a second element encoder 230, a trellis termination encoder 240, and a bitstream assembling apparatus 250, and receives an input of data to generate and output an encoded bitstream for the input data.

[51] The first element encoder 210 has a size of a designated code block. The first element encoder 210 receives an input of a bitstream of input data in which the padding is performed, in the unit of plural bits to perform an encoding and generates a first output bitstream in the unit of plural bits.

[52] When the bitstream of the input data is $C(0, \dots, n)$, the first output bitstream becomes a bitstream $X(0, \dots, n)$ and a bitstream $Z(0, \dots, n)$.

[53] It is preferable that the first element encoder 210 includes an internal register and a state of an initial register is "000".

[54] It is preferable that the first element encoder 210 receives the bitstream of the input data in the unit of plural bits. For example, the input data may be input to the first element encoder 210 in the unit of plural bits after the input data is divided in the unit of plural bits through a means for generating the bitstream of the input data in the unit of plural bits before the input data is input to the first element encoder 210.

[55] FIG. 3 is a block diagram illustrating a structure of an input bitstream according to an embodiment of the present invention. Referring to FIG. 3, when a size of data input to the turbo encoder 200 is C , the first element encoder 210 receives an input of an input bitstream having the same number of filler bits existing in the front of the input data as

the number of F, which has no remainder when C is divided by 8. At this time, the filler bit may be "0".

- [56] That is, the size of the data bitstream input to the first element encoder 210 corresponds to a sum of the size (c) of the data input to the turbo encoder 200 and the number (F) of filler bits existing in the front of the data, and also corresponds to a value generated by multiplying the number (M_8) of input bitstreams and 8. Further, the size of the data bitstream is a maximum of 6144 and can have only a value of K_i defined in Table 1.
- [57] Referring back to FIG. 2, according to another exemplary embodiment of the present invention, the first element encoder 210 generates the first output bitstream by using the bitstream of input data and an internal state.
- [58] The internal state of the first element encoder 210 refers to a state of the internal register included in the first element encoder 210.
- [59] The first element encoder 210 operates the state of the internal register while encoding the bitstream of the input data.
- [60] It is preferable that the first element encoder 210 can generate first output bitstreams $Z(n)$, $Z(n+1)$, $Z(n+2)$, $Z(n+3)$, $Z(n+4)$, $Z(n+5)$, $Z(n+6)$, $Z(n+7)$ or $X(n)$, $X(n+1)$, $X(n+2)$, $X(n+3)$, $X(n+4)$, $X(n+5)$, $X(n+6)$, $X(n+7)$ when the bitstreams of the input data correspond to $C(n)$, $C(n+1)$, $C(n+2)$, $C(n+3)$, $C(n+4)$, $C(n+5)$, $C(n+6)$, $C(n+7)$ and the internal states of the first element encoder 210 correspond to $D_0(n)$, $D_1(n)$, $D_2(n)$. The first element encoder 210 uses an encoding method shown in FIG. 1.
- [61] $X(n) = C(n)$
- [62] $Z(n) = C(n) + D_0(n) + D_1(n)$
- [63]
- [64] $X(n+1) = C(n+1)$
- [65] $Z(n+1) = C(n+1) + D_0(n+1) + D_1(n+1)$
- [66] $= C(n+1) + C(n) + D_1(n) + D_2(n) + D_1(n+1)$
- [67] $= C(n+1) + C(n) + D_1(n) + D_2(n) + D_0(n)$
- [68]
- [69] $X(n+2) = C(n+2)$
- [70] $Z(n+2) = C(n+2) + D_0(n+2) + D_1(n+2)$
- [71] $= C(n+2) + C(n+1) + D_1(n+1) + D_2(n+1) + D_1(n+2)$
- [72] $= C(n+2) + C(n+1) + D_0(n) + D_1(n) + D_0(n+1)$
- [73] $= C(n+2) + C(n+1) + D_0(n) + D_1(n) + C(n) + D_1(n) + D_2(n)$
- [74] $= C(n+2) + C(n+1) + C(n) + D_0(n) + D_2(n)$
- [75]
- [76] $X(n+3) = C(n+3)$
- [77] $Z(n+3) = C(n+3) + D_0(n+3) + D_1(n+3)$

- [78] $= C(n+3)+C(n+2)+D_1(n+2)+D_2(n+2)+D_1(n+3)$
- [79] $= C(n+3)+C(n+2)+D_0(n+1)+D_0(n)+D_0(n+2)$
- [80] $= C(n+3)+C(n+2)+C(n)+D_1(n)+D_2(n)+D_0(n) +C(n+1)+D_1(n+1)+D_2(n+1)$
- [81] $= C(n+3)+C(n+2)+C(n+1)+C(n)+D_1(n)+D_2(n)$
- [82] $+D_0(n)+D_0(n)+D_1(n)$
- [83] $= C(n+3)+C(n+2)+C(n+1)+C(n)+D_2(n)$
- [84]
- [85] $X(n+4) = C(n+4)$
- [86] $Z(n+4) = C(n+4)+D_0(n+4)+D_1(n+4)$
- [87] $= C(n+4)+C(n+3)+D_1(n+3)+D_2(n+3)+D_1(n+4)$
- [88] $= C(n+4)+C(n+3)+D_0(n+2)+D_0(n+1)+D_0(n+3)$
- [89] $= C(n+4)+C(n+3)+C(n+1)+D_1(n+1)+D_2(n+1)+C(n)$
- [90] $+D_1(n)+D_2(n)+C(n+2)+D_1(n+2)+D_2(n+2)$
- [91] $= C(n+4)+C(n+3)+C(n+2)+C(n+1)+C(n)+D_0(n)$
- [92] $+D_1(n)+D_1(n)+D_2(n)+D_0(n+1)+D_0(n)$
- [93] $= C(n+4)+C(n+3)+C(n+2)+C(n+1)+C(n)+D_2(n)+D_0(n+1)$
- [94] $= C(n+4)+C(n+3)+C(n+2)+C(n+1)+C(n)+D_2(n)$
- [95] $+C(n)+D_1(n)+D_2(n)$
- [96] $= C(n+4)+C(n+3)+C(n+2)+C(n+1)+D_1(n)$
- [97]
- [98] $X(n+5) = C(n+5)$
- [99] $Z(n+5) = C(n+5)+D_0(n+5)+D_1(n+5)$
- [100] $= C(n+5)+C(n+4)+D_1(n+4)+D_2(n+4)+D_1(n+5)$
- [101] $= C(n+5)+C(n+4)+D_0(n+3)+D_0(n+2)+D_0(n+4)$
- [102] $= C(n+5)+C(n+4)+C(n+2)+D_1(n+2)+D_2(n+2)+C(n+1)$
- [103] $+D_1(n+1)+D_2(n+1)+C(n+3)+D_1(n+3)+D_2(n+3)$
- [104] $= C(n+5)+C(n+4)+C(n+3)+C(n+2)+C(n+1)+D_0(n+1)$
- [105] $+D_0(n)+D_0(n)+D_1(n)+D_0(n+2)+D_0(n+1)$
- [106] $= C(n+5)+C(n+4)+C(n+3)+C(n+2)+C(n+1)+D_1(n)+D_0(n+2)$
- [107] $= C(n+5)+C(n+4)+C(n+3)+C(n+2)+C(n+1)+D_1(n)$
- [108] $+C(n+1)+D_1(n+1)+D_2(n+1)$
- [109] $= C(n+5)+C(n+4)+C(n+3)+C(n+2)+D_1(n)+D_0(n)+D_1(n)$
- [110] $= C(n+5)+C(n+4)+C(n+3)+C(n+2)+D_0(n)$
- [111]
- [112] $X(n+6) = C(n+6)$
- [113] $Z(n+6) = C(n+6)+D_0(n+6)+D_1(n+6)$
- [114] $= C(n+6)+C(n+5)+D_1(n+5)+D_2(n+5)+D_0(n+5)$
- [115] $= C(n+6)+C(n+5)+D_0(n+4)+D_0(n+3)+D_0(n+5)$

- [116] $= C(n+6)+C(n+5)+C(n+3)+D_1(n+3)+D_2(n+3)+C(n+2)$
 [117] $+ D_1(n+2)+D_2(n+2)+C(n+4)+D_1(n+4)+D_2(n+4)$
 [118] $= C(n+6)+C(n+5)+C(n+4)+C(n+3)+C(n+2)+D_0(n+2)$
 [119] $+D_0(n+1)+D_0(n+1)+D_0(n)+D_0(n+3)+D_0(n+2)$
 [120] $= C(n+6)+C(n+5)+C(n+4)+C(n+3)+C(n+2)+D_0(n)+D_0(n+3)$
 [121] $= C(n+6)+C(n+5)+C(n+4)+C(n+3)+C(n+2)+D_0(n)+C(n+2)+D_1(n+2)+D_2(n+2)$
 [122] $= C(n+6)+C(n+5)+C(n+4)+C(n+3)+D_0(n)+D_0(n+1)+D_0(n)$
 [123] $= C(n+6)+C(n+5)+C(n+4)+C(n+3)+D_0(n+1)$
 [124] $= C(n+6)+C(n+5)+C(n+4)+C(n+3)+C(n)+D_1(n)+D_2(n)$
 [125]
 [126] $X(n+7) = C(n+7)$
 [127] $Z(n+7) = C(n+7)+D_0(n+7)+D_1(n+7)$
 [128] $= C(n+7)+C(n+6)+D_1(n+6)+D_2(n+6)+D_1(n+7)$
 [129] $= C(n+7)+C(n+6)+D_0(n+5)+D_0(n+4)+D_0(n+6)$
 [130] $= C(n+7)+C(n+6)+C(n+4)+D_1(n+4)+D_2(n+4)+C(n+3)$
 [131] $+D_1(n+3)+D_2(n+3)+C(n+5)+D_1(n+5)+D_2(n+5)$
 [132] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n+3)+D_0(n+3)$
 [133] $+D_0(n+2)+D_0(n+2)+D_0(n+1)+D_0(n+4)+D_0(n+3)$
 [134] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n+3)+D_0(n+1)+D_0(n+4)$
 [135] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n+3)+C(n)+D_1(n)$
 [136] $+D_2(n)+C(n+3)+D_1(n+3)+D_2(n+3)$
 [137] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n)+D_1(n)+D_2(n)+D_1(n+3)+D_2(n+3)$
 [138] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n)+D_1(n)+D_2(n)+D_0(n+2)+D_0(n+1)$
 [139] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n)+D_1(n)+D_2(n)$
 [140] $+C(n+1)+D_1(n+1)+D_2(n+1)+C(n)+D_1(n)+D_2(n)$
 [141] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n+1)+D_1(n+1)+D_2(n+1)$
 [142] $= C(n+7)+C(n+6)+C(n+5)+C(n+4)+C(n+1)+D_0(n)+D_1(n)$
 [143] Further, it is preferable that the first element encoder 210 derives $D_0(n+8)$, $D_1(n+8)$, $D_2(n+8)$, which are internal states in the case of $n+8$ according to the below equation.
 [144] $D_0(n+8) = C(n+7)+D_1(n+7)+D_2(n+7)$
 [145] $= C(n+7)+D_0(n+6)+D_0(n+5)$
 [146] $= C(n+7)+C(n+5)+D_1(n+5)+D_2(n+5)+C(n+4)+D_1(n+4)+D_2(n+4)$
 [147] $= C(n+7)+C(n+5)+C(n+4)+D_1(n+5)+D_2(n+5)+D_1(n+4)+D_2(n+4)$
 [148] $= C(n+7)+C(n+5)+C(n+4)+D_0(n+4)+D_1(n+4)+D_1(n+4)+D_0(n+2)$
 [149] $= C(n+7)+C(n+5)+C(n+4)+D_0(n+4)+D_0(n+2)$
 [150] $= C(n+7)+C(n+5)+C(n+4)+C(n+3)+D_1(n+3)+D_2(n+3)$
 [151] $+C(n+1)+D_1(n+1)+D_2(n+1)$
 [152] $= C(n+7)+C(n+5)+C(n+4)+C(n+3)+C(n+1)+D_0(n+2)+D_0(n+1)+D_0(n)+D_1(n)$

- [153] $= C(n+7)+C(n+5)+C(n+4)+C(n+3)+C(n+1)+D_0(n)$
 [154] $+D_1(n)+C(n+1)+D_1(n+1)+D_2(n+1)+C(n)+D_1(n)+D_2(n)$
 [155] $= C(n+7)+C(n+5)+C(n+4)+C(n+3)+C(n)+D_0(n)$
 [156] $+D_1(n)+D_0(n)+D_1(n)+D_1(n)+D_2(n)$
 [157] $= C(n+7)+C(n+5)+C(n+4)+C(n+3)+C(n)+D_1(n)+D_2(n)$
 [158]
 [159] $D_1(n+8) = D_0(n+7)$
 [160] $= C(n+6)+D_1(n+6)+D_2(n+6)$
 [161] $= C(n+6)+D_0(n+5)+D_0(n+4)$
 [162] $= C(n+6)+C(n+4)+D_1(n+4)+D_2(n+4)+C(n+3)+D_1(n+3)+D_2(n+3)$
 [163] $= C(n+6)+C(n+4)+C(n+3)+D_0(n+3)+D_1(n+3)+D_1(n+3)+D_0(n+1)$
 [164] $= C(n+6)+C(n+4)+C(n+3)+D_0(n+3)+D_0(n+1)$
 [165] $= C(n+6)+C(n+4)+C(n+3)+C(n+2)+D_1(n+2)+D_2(n+2)+C(n)+D_1(n)+D_2(n)$
 [166] $= C(n+6)+C(n+4)+C(n+3)+C(n+2)+C(n)+D_0(n+1)+D_0(n)+D_1(n)+D_2(n)$
 [167] $= C(n+6)+C(n+4)+C(n+3)+C(n+2)+C(n)+C(n)$
 [168] $+D_1(n)+D_2(n)+D_0(n)+D_1(n)+D_2(n)$
 [169] $= C(n+6)+C(n+4)+C(n+3)+C(n+2)+D_1(n)+D_2(n)+D_0(n)+D_1(n)+D_2(n)$
 [170] $= C(n+6)+C(n+4)+C(n+3)+C(n+2)+D_0(n)$
 [171]
 [172] $D_2(n+8) = D_0(n+6)$
 [173] $= C(n+5)+D_1(n+5)+D_2(n+5)$
 [174] $= C(n+5)+D_0(n+4)+D_0(n+3)$
 [175] $= C(n+5)+C(n+3)+D_1(n+3)+D_2(n+3)+C(n+2)+D_1(n+2)+D_2(n+2)$
 [176] $= C(n+5)+C(n+3)+C(n+2)+D_0(n+2)+D_0(n+1)+D_0(n+1)+D_0(n)$
 [177] $= C(n+5)+C(n+3)+C(n+2)+D_0(n+2)+D_0(n)$
 [178] $= C(n+5)+C(n+3)+C(n+2)+C(n+1)+D_1(n+1)+D_2(n+1)+D_0(n)$
 [179] $= C(n+5)+C(n+3)+C(n+2)+C(n+1)+D_0(n)+D_1(n)+D_0(n)$
 [180] $= C(n+5)+C(n+3)+C(n+2)+C(n+1)+D_1(n)$
 [181] The above equation may be organized as defined in the below table. “V” shown in the table refers to an Exclusive-OR operation.
 [182] [Table 2]
 [183]

	$C(n+7)$	$C(n+6)$	$C(n+5)$	$C(n+4)$	$C(n+3)$	$C(n+2)$	$C(n+1)$	$C(n)$	$D_2(n)$	$D_1(n)$	$D_0(n)$
$Z(n)$								V		V	V
$Z(n+1)$							V	V	V	V	V
$Z(n+2)$						V	V	V	V		V
$Z(n+3)$					V	V	V	V	V		V
$Z(n+4)$				V	V	V	V			V	
$Z(n+5)$			V	V	V	V					V
$Z(n+6)$		V	V	V	V			V	V	V	
$Z(n+7)$	V	V	V	V			V			V	V
$D_0(n+8)$	V		V	V	V			V	V	V	
$D_1(n+8)$		V		V	V	V					V
$D_2(n+8)$			V		V	V	V			V	

[184]

[185] FIG. 6 is a block diagram illustrating a construction of an element encoder circuit according to an embodiment of the present invention. The element encoder circuit illustrated in FIG. 6 shows an example of deriving output bitstreams $Z(n)$, $Z(n+1)$, $Z(n+2)$, $Z(n+3)$, $Z(n+4)$, $Z(n+5)$, $Z(n+6)$, $Z(n+7)$ and subsequent internal states $D_0(n+8)$, $D_1(n+8)$, $D_2(n+8)$ by using the aforementioned inputs $C(n)$, $C(n+1)$, $C(n+2)$, $C(n+3)$, $C(n+4)$, $C(n+5)$, $C(n+6)$, $C(n+7)$ and internal states $D_0(n)$, $D_1(n)$, $D_2(n)$.

[186] Referring back to FIG. 2, the first element encoder 210 receives an input of input bitstreams having the form shown in FIG. 3 and generates output bitstreams including the same number of null bits as the number of filler bits existing in the input bitstreams.

[187] According to an exemplary embodiment of the present invention, the first element encoder 210 represents the null bit as "0".

[188] There are several methods to represent the null bit, but the null bit is represented herein as "0" in order to facilitate a next step of the signal processing of the turbo encoder. Thereafter, the null bit and the "0" bit are discriminated through the number of "0" which is inserted into the input bitstream.

[189] Referring back to FIG. 2, the internal interleaver 220 receives data input to the turbo encoder 200 and generates an interleaved input bitstream.

[190] It is preferable that the internal interleaver 220 is configured to generate the interleaved input bitstream in the unit of plural bits.

[191] The second element encoder 230 receives an input of the interleaved input bitstream generated through the internal interleaver 220 in the unit of plural bits to encode the interleaved input bitstream and generates a second output bitstream in the unit of plural bits.

[192] The second element encoder 230 has the same construction as that of the first element encoder 210 but the input data bitstream and the output bitstream transmitted

to the bitstream assembling apparatus 250 are only different.

- [193] The difference of the output bistream of the second element encoder 230 from the first element encoder 210 means that the output bitstreams transmitted to the bitstream assembling apparatus 250 by the first element encoder 210 are both of operated $X(n)$ and $Z(n)$ but the output bitstream transmitted to the bitstream assembling apparatus 250 by the second element encoder 230 is only $X'(n)$ between operated $X'(n)$ and $Z'(n)$.
- [194] The trellis termination encoder 240 generates a bit for the trellis termination of the first element encoder 210 and the second element encoder 230.
- [195] According to an exemplary embodiment of the present invention, the trellis termination encoder 240 generates the bit for the trellis termination by using an internal state of the first encoder 210 or the second element encoder 230 when the last input bitstream for the input data is input to the first element encoder 210 or the second element encoder 230.
- [196] For example, when the internal states of the first element encoder 210 or the second element encoder 230 in a state where the last input bitstream for the input data is input to the first element encoder 210 or the second element encoder 230 are $D_0(n)$, $D_1(n)$, $D_2(n)$, the trellis termination encoder 240 generates $Z(n)$, $Z(n+1)$, $Z(n+2)$, $X(n)$, $X(n+1)$, $X(n+2)$ according to the below equation. A first value input to the first element encoder 210 or the second element encoder 230 is "0", so $D_0(n+1) = D_1(n+2) = 0$.
- [197] $X(n) = D_1(n) + D_2(n)$
- [198] $Z(n) = D_0(n) + D_2(n)$
- [199]
- [200] $X(n+1) = D_1(n+1) + D_2(n+1)$
- [201] $= D_0(n) + D_1(n)$
- [202] $Z(n+1) = D_0(n+1) + D_2(n+1)$
- [203] $= 0 + D_1(n)$
- [204] $= D_1(n)$
- [205]
- [206] $X(n+2) = D_1(n+2) + D_2(n+2)$
- [207] $= D_0(n+1) + D_0(n)$
- [208] $= D_0(n)$
- [209] $Z(n+2) = D_0(n+2) + D_2(n+2)$
- [210] $= 0 + D_0(n)$
- [211] $= D_0(n)$
- [212] It is preferable that bits for the trellis termination are 12 bits and the trellis termination encoder 240 can generate bits for the trellis termination during one clock cycle.

- [213] The bitstream assembling apparatus 250 receives the first output bitstream from the first element encoder 210, receives the second output bitstream from the second element encoder 230, and receives the bits for the trellis termination from the trellis termination encoder 240 to generate the input bitstream used in the rate matching.
- [214] It is preferable that the input bitstreams, which are used in the rate matching, generated by the bitstream assembling apparatus 250 are three bitstreams in the unit of bytes.
- [215] FIG. 4 is a block diagram illustrating a structure of a bitstream input to a bitstream assembling apparatus according to an embodiment of the present invention. Referring to FIG. 4, the bitstream assembling apparatus 250 receives an input of the first output bitstreams $X(n)$ and $Z(n)$ from the first element encoder, receives an input of the second output bitstream $X'(n)$ from the second element encoder 230, and receives an input of the bits for the trellis termination from the trellis termination encoder 220.
- [216] It is preferable that the bitstream assembling apparatus 250 adds four bits for the trellis termination to each of the first output bitstreams and the second output bitstream, respectively as shown in FIG. 4.
- [217] FIG. 5 is a block diagram illustrating a structure of an output bitstream of a bitstream assembling apparatus according to an embodiment of the present invention. Referring to FIG. 5, the bitstream assembling apparatus 250 connects the bits for the trellis termination to $X(0, \dots, k-1)$ and $Z(0, \dots, k-1)$ received from the first output bitstreams and $X'(0, \dots, k-1)$ received from the second output bitstream and generates a final output structure.
- [218] It is preferable that the bitstream assembling apparatus 250 divides 12 bit information generated by the trellis termination encoder 240 into three 4 bit information pieces. Further, the bitstream assembling apparatus 250 connects each of the divided 4 bits to the three final output bitstreams and adds null bits to the fronts of the output bitstreams such that the output bitstreams become structure bodies having the unit of 4 bytes.
- [219] It is preferable that the bitstream assembling apparatus 250 receives the first output bitstreams, the second output bitstream, and the bits for the trellis termination to make them become structure bodies having the unit of 32 bits and can be constructed such that they become structure bodies having the unit of 8 bits for an 8 bit unit processing.
- [220] FIG. 8 is a block diagram illustrating a construction of a bitstream assembling apparatus according to an embodiment of the present invention. Referring to FIG. 8, the bitstream assembling apparatus 250 delays lower 4 bits in the 8 bit unit by one cycle in order to construct 4 bits, which are the bits for the trellis termination, in the 8 bit unit by using the register. Further, bitstream assembling apparatus 250 detects third and fourth bits when added null bits according to a value of K are represented by a binary number and uses the detected bits as multiplexer control bits, and thus null bits,

which are 4, 12, 20, or 28 bits, are inserted.

[221] That is, the number of null bits is $32 - (K+4) \bmod 32$.

[222] It is preferable that the bitstream assembling apparatus 250 can use a delay register in the unit of 8 bits including a D-flip flop (D-type flip flop).

[223] While the detailed description of the present invention has described certain exemplary embodiments such as a portable terminal, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

[224] ** Reference Numerals

[225] 200: Turbo Encoder Apparatus 210: First Element Encoder

[226] 220: Internal Interleaver 230: Second Element Encoder

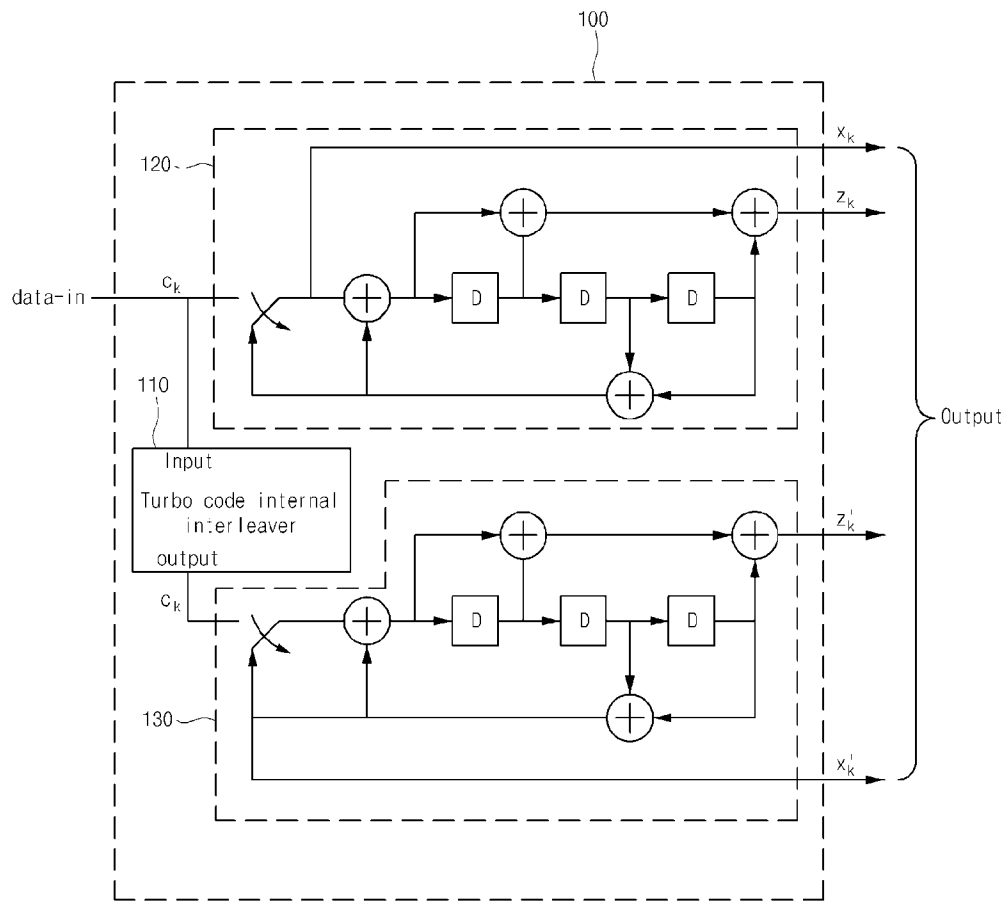
[227] 240: Trellis Termination Encoder 250: Bitstream Assembling Apparatus

Claims

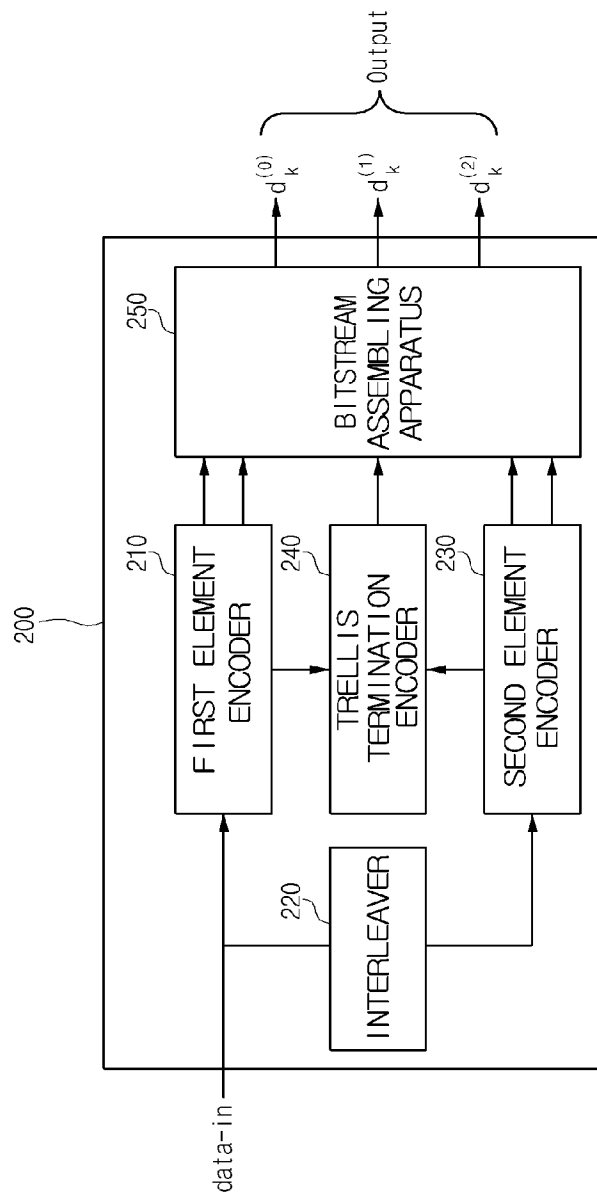
- [Claim 1] A turbo encoder apparatus for receiving an input of data and outputting encoded bitstreams, the turbo encoder apparatus comprising:
a first element encoder for receiving an input of a bitstream of the data, which has a size of a designated code block and in which a padding has been implemented, in the unit of plural bits, encoding the input of the bitstream of the data, and generating a first output bitstream in the unit of plural bits;
an internal interleaver for generating an interleaved input bitstream from the bitstream of the data;
a second element encoder for receiving an input of the interleaved input bitstream in the unit of plural bits, encoding the input of the interleaved input bitstream, and generating a second output bitstream in the unit of plural bits;
a trellis-termination-encoder for generating bits for trellis terminations of the first element encoder and the second element encoder; and
a bitstream assembler for receiving the first output bitstream, the second output bitstream, and the bits for the trellis terminations and generating an input bitstream for a rate matching.C
- [Claim 2] The turbo encoder apparatus as claimed in claim 1, wherein the first element encoder and the second element encoder receive an input of the bitstream of the data constructed in the unit of 8 bits, and the plural bits are 8 bits.
- [Claim 3] The turbo encoder apparatus as claimed in claim 2, wherein the first element encoder generates the first output bitstream by using the bitstream of the data and an internal state of the first element encoder, and the second element encoder generates the second output bitstream by using the interleaved input bitstream and an internal state of the second element encoder.
- [Claim 4] The turbo encoder apparatus as claimed in claim 2, wherein the first element encoder or the second element encoder represents null bits, which exist in the first output bitstream or the second output bitstream in equal number to a number of filler bits existing in the bitstream of the data, as "0".
- [Claim 5] The turbo encoder apparatus as claimed in claim 1, wherein the trellis termination encoder generates the bits for the trellis termination by using an internal state when a last input bitstream for the data is

- inputted to the first element encoder or the second element encoder.
- [Claim 6] The turbo encoder apparatus as claimed in claim 2, wherein the bitstream assembler rearranges the input bitstream of the rate matching so the rate matching could be performed in parallel.
- [Claim 7] The turbo encoder apparatus as claimed in claim 6, wherein the bitstream assembling apparatus inserts as many null bits as a number determined by the size of the code block into the input bitstream of the rate matching and adds the bits for the trellis termination to the first output bitstream or the second output bitstream, wherein the null bits are inserted by changing positions of upper 4 bits and lower 4 bits in a 8 bit unit of the first output bitstream or the second output bitstream, delaying the lower 4 bits by one cycle, and making the lower 4 bits pass through a cycle delay circuit according to a number of null bits, which should be added.

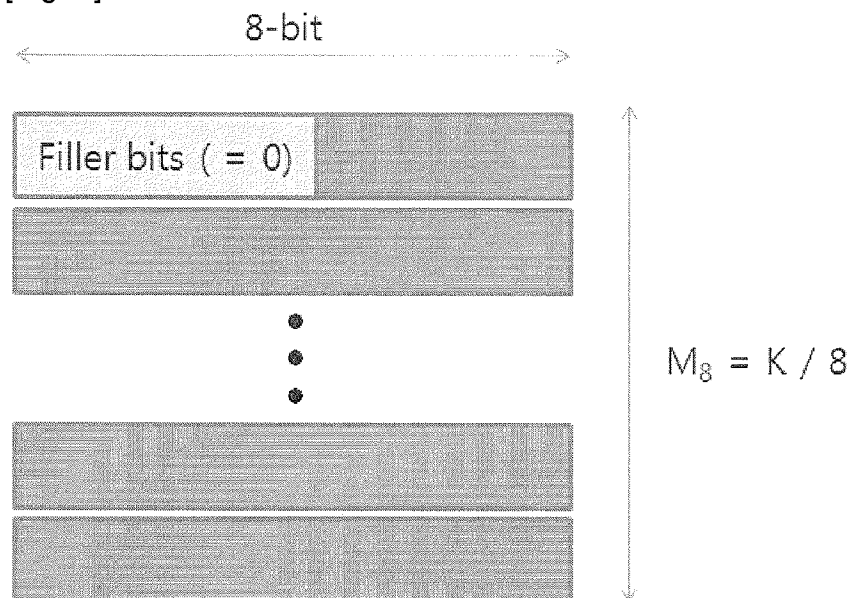
[Fig. 1]



[Fig. 2]

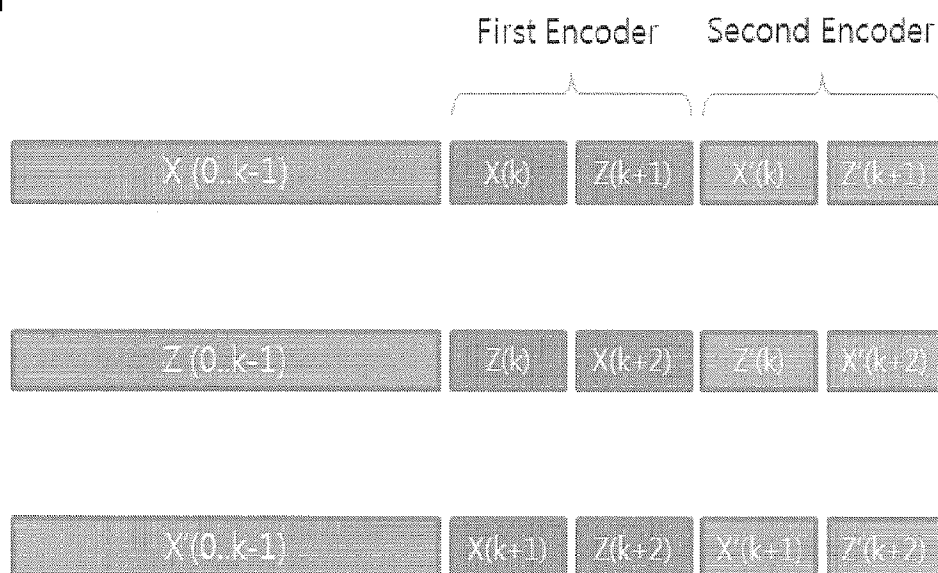


[Fig. 3]

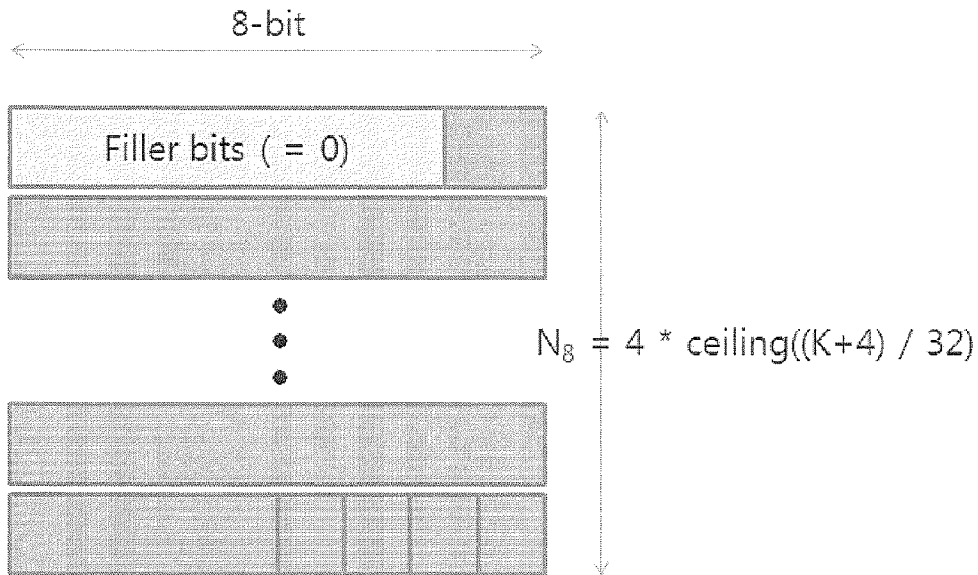


$$\text{Size} = C + F = M_8 * 8 = K$$

[Fig. 4]



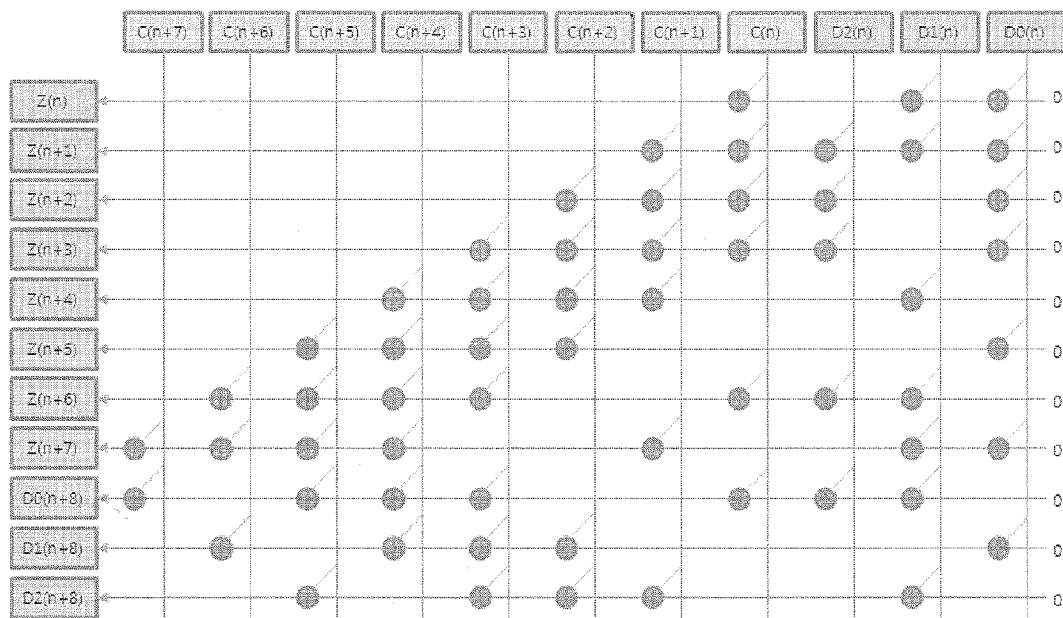
[Fig. 5]



$$\text{Size} = N_8 * 8,$$

$$F = N_8 * 8 - (K + 4)$$

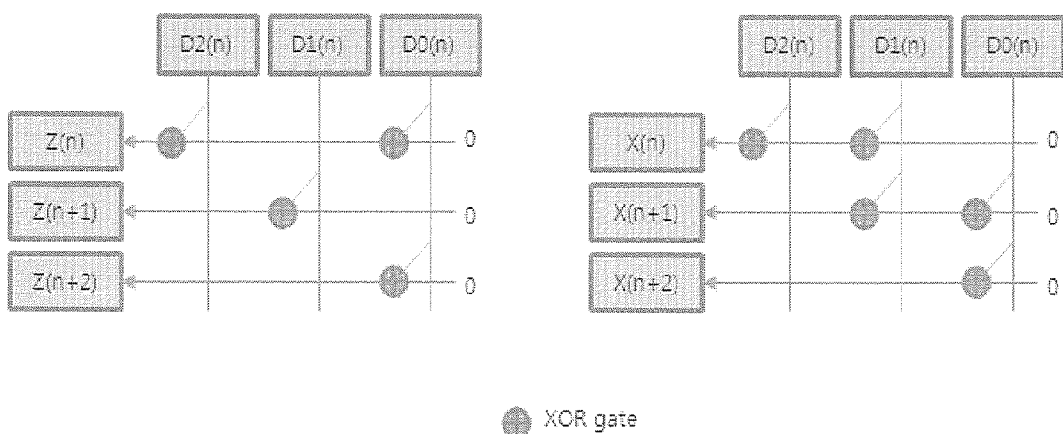
[Fig. 6]



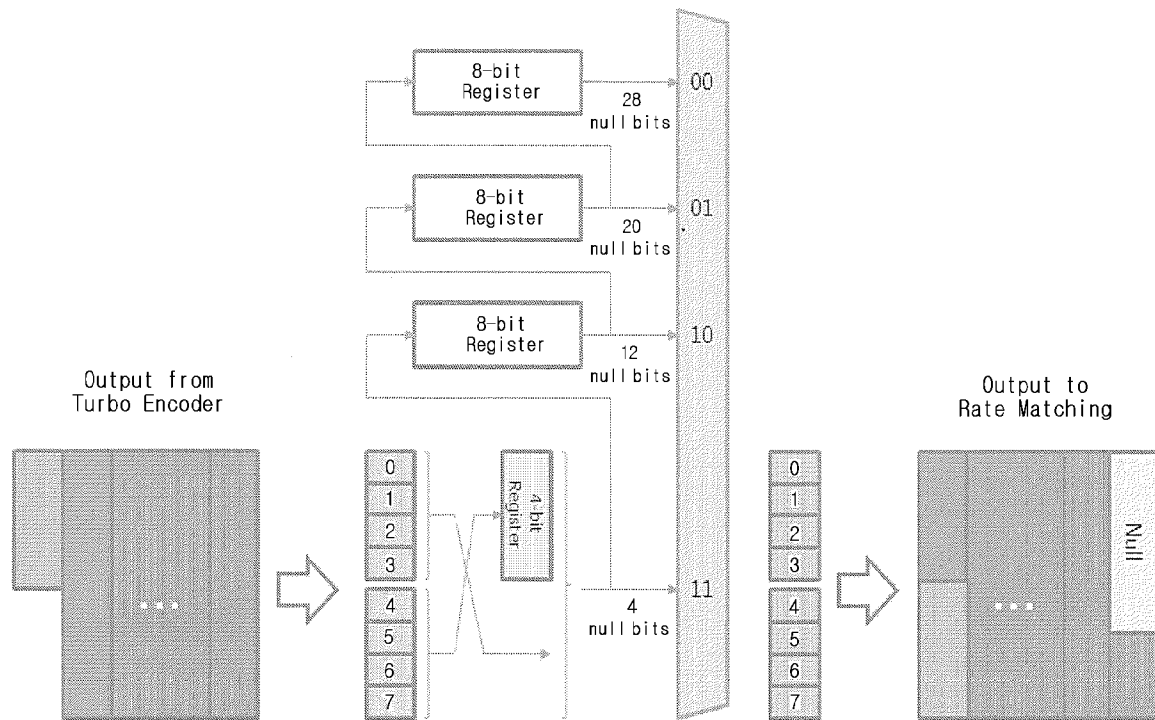
$$X(n+7..n) = C(n+7..n)$$

● XOR gate

[Fig. 7]



[Fig. 8]



A. CLASSIFICATION OF SUBJECT MATTER***H03M 13/00(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M 13/00; H04L 27/00; H03M 7/00; H04B 7/02; G06F 11/14; H04L 1/18; H03M 7/40; H04L 27/26

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: "Turbo, encoder, internal, interleaver, trellis*"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	KR 10-2009-0125080 A (SAMSUNG ELECTRONICS CO., LTD.) 03 December 2009 See the Abstract, Claim 1	1-7
A	KR 10-0319919 B1 (SAMSUNG ELECTRONICS CO., LTD.) 20 June 2002 See the Abstract, Claim 1-3	1-7
A	US 2007-0092033 A1 (JUNG-PIL YU, et al.) 26 April 2007 See the Abstract, Fig. 1,3, Claim 1	1-7
A	US 2009-0106618 A1 (LIN HUA) 23 April 2009 See the Abstract, Fig. 6, Claim 1	1-7



Further documents are listed in the continuation of Box C.



See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

24 DECEMBER 2012 (24.12.2012)

Date of mailing of the international search report

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Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan
City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Jang Seok Hwan

Telephone No. 82-42-481-8250



Information on patent family members

PCT/KR2012/001439

Form PCT/ISA/210 (patent family annex) (July 2009)

INTERNATIONAL SEARCH REPORT

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International application No.

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