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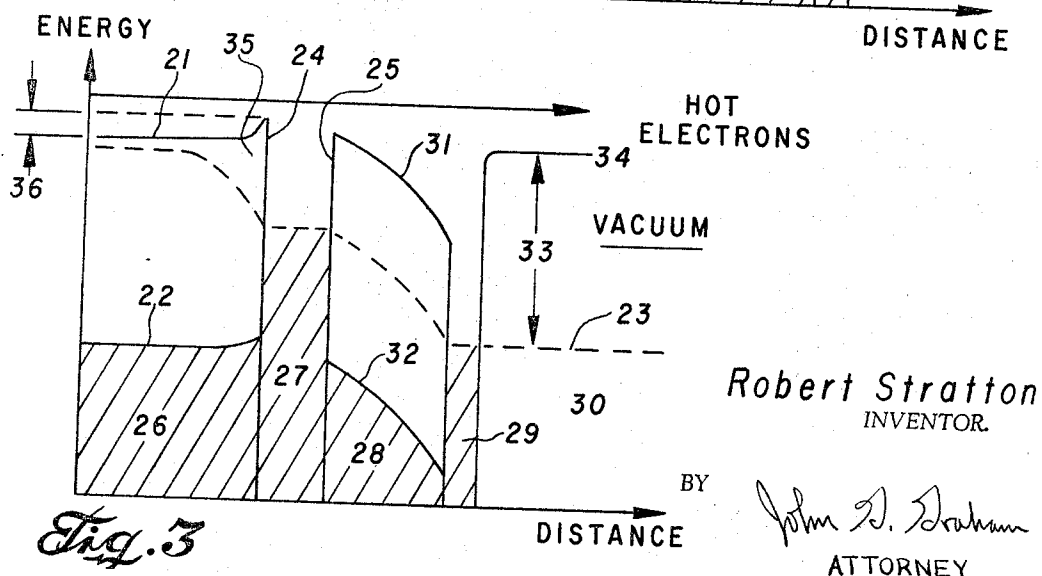
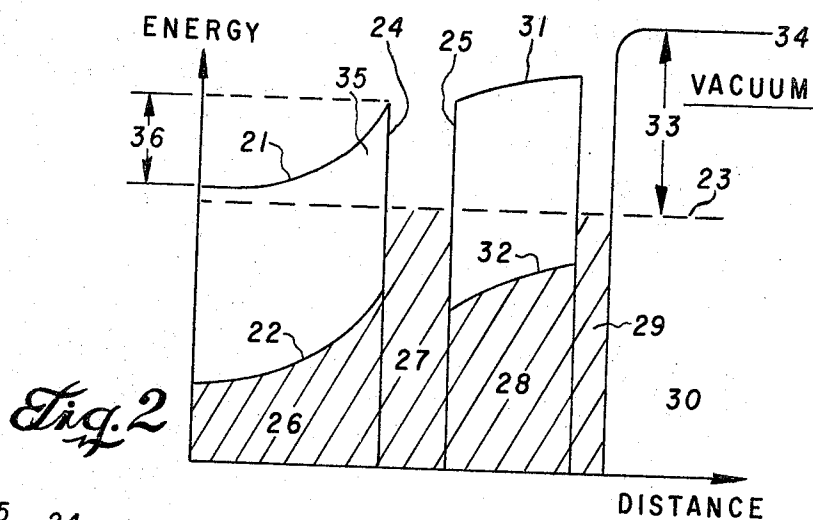
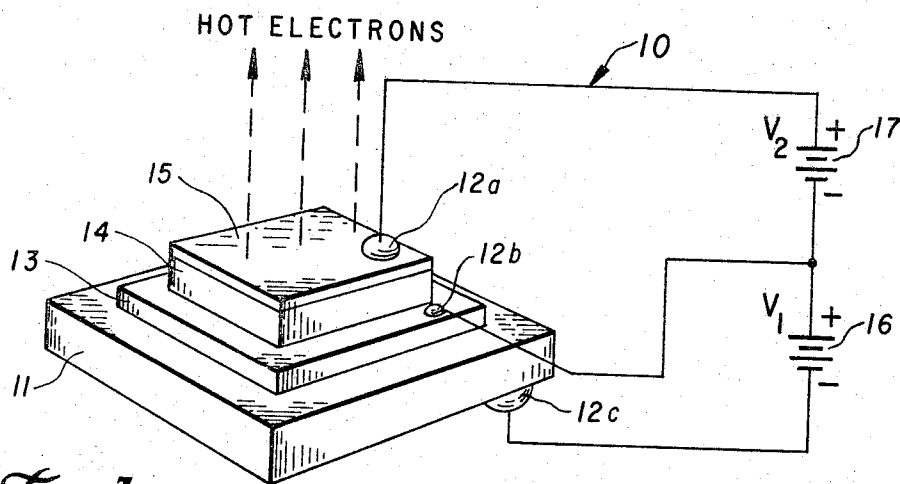
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SPACE CHARGE BARRIER HOT ELECTRON CATHODE

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2 Sheets-Sheet 1



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3,334,248 SPACE CHARGE BARRIER HOT ELECTRON CATHODE

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This invention relates to electron emitting devices, and more particularly to "cold" cathode electron emitting devices.

Research in many areas of technology is presently being carried out in search of new types of materials and structures to be used for cathode emitters. Thermionic or "hot" cathodes have been used extensively in the past to meet various requirements. Recent technological advances and developments, however, have shown that "hot" cathodes can never be completely satisfactory as electron sources. This is due to their inherent shortcomings which include limited current density, high power consumption, high temperature operation, high beam noise, and long starting time. It is desirable therefore to have "cold" cathode structures developed which eliminate these shortcomings.

In response to this demand, therefore, a number of "cold" cathode devices have been developed or are currently being researched which partially overcome the disadvantages associated with the "hot" structures.

Examples of some of these devices are the "surface-barrier diode" described by H. G. White and R. A. Logan in *Journal of Applied Physics* 34, 1990 (1963), the "graded-gap thin film Schottky barrier diode" described by D. V. Geppert and B. V. Dore in *Extended Abstract No. 13*, Electric Insulation Division, of the Spring Meeting of the Electrochemical Society, Toronto, Canada, May 1964; and the "tunnel emission cathode" which is the subject of U.S. Patent No. 3,056,073. Among other disadvantages of these devices is the fact that, in practice, all of them have very low cathode efficiencies.

Another "cold" cathode device, the "field emitter cathode," has been developed that utilizes a very high electric field which reduces the barrier height and thickness at the surface of an unheated metal or semiconductor sufficiently so that electrons can be emitted into a vacuum by quantum-mechanical tunneling through the barrier. The field emitter cathode has been shown to possess high cathode efficiency, but there are disadvantages associated with this device that severely limit its use. The emission of electrons occurs from a single point or array of points which presents a major difficulty in its operation. The emitting points change because of heating, particle bombardment, chemical reaction and evaporation, and affect both the acting field and the barrier. Since current density is a sensitive function of the applied field and the barrier height and thickness, and these factors can change unexpectedly in this device, the field emitter cathode is unstable. Another difficulty associated with this device is the very high electric field required for its operation.

With the difficulties heretofore encountered in mind, it is an object of this invention to provide a "cold" cathode emitter having a very high cathode efficiency.

It is another object to provide a "cold" cathode emitter capable of being operated at relatively low voltages and electric fields.

It is a still further object to provide the aforementioned cathode having electron emission from a large area rather than a point, thus having increased stability and higher total emission current.

In accordance with these objects and others readily apparent from the following description and appended

claims, this invention involves a unique cold cathode electron emitting device. This device, hereafter referred to as the space charge barrier hot electron cathode, is composed substantially of a very thin metal layer sandwiched between two semiconductor layers, one of which is doped with an N-type impurity, the second being either intrinsic (high resistivity) or slightly P-type. When the distribution of impurities in the N-type semiconductor is uniform, the resulting space charge barrier is the well known Schottky barrier. Another distribution will result in a space charge barrier of somewhat different form but in principle any such space charge induced barrier can be used without departing from the spirit and scope of the invention described herein. Through proper biasing the electrons in the N-type layer are emitted across this barrier through the metal and second semiconductor layer into vacuum. Since the electrons in the present invention are emitted from a relatively flat area, rather than a point, much greater control may be maintained over the current output during operation. In addition a larger total current may be expected due to the large area of emission. The cathode device of this invention also does not require high voltages to be applied for its operation. In view of the configuration which will presently be described, the space-charge barrier hot electron cathode may also be simply fabricated.

The novel features believed characteristic of this invention are set forth in the appended claims. The invention itself, however, as well as other objects and advantages thereof, may best be understood by reference to the following detailed description of illustrative embodiments, read in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a pictorial view partially in schematic form of an embodiment of the present invention showing its operation;

FIGURE 2 is an electron potential energy diagram of the device shown in FIGURE 1 under equilibrium conditions;

FIGURE 3 is an electron potential energy diagram of the device shown in FIGURE 1 under bias conditions;

FIGURE 4 is an enlarged plan view of a substrate and serves to illustrate an initial stage in one method for fabricating the present invention;

FIGURE 5 is a sectional view taken along the line 5—5 of FIGURE 4;

FIGURE 6 is an enlarged plan view similar to FIGURE 4 showing another step of the illustrative method for fabricating the present invention;

FIGURE 7 is a sectional view taken along the line 7—7 of FIGURE 6;

FIGURE 8 is an enlarged plan view showing yet another step of the illustrative method for fabricating the present invention;

FIGURE 9 is a sectional view taken on line 9—9 of FIGURE 8;

FIGURE 10 is an enlarged schematic top view of the space charge barrier hot electron cathode constructed in accordance with the present invention which also shows the final step of the illustrative method for fabricating the present invention; and,

FIGURE 11 is a sectional view taken on the line 11—11 of FIGURE 10.

Referring now to FIGURE 1, the space charge barrier hot electron cathode device 10 comprises an N-type semiconductor wafer or body 11, a very thin metal layer 13, and a thin semiconductor layer 14, preferably of intrinsic or lightly doped P-type semiconducting material. A low work function coating 15 such as cesium or barium, for example, is provided upon the surface of the semiconductor layer 14 as shown. External leads are connected to

the respective layers by means of suitable ohmic contacts 12a, 12b, and 12c to provide a means for biasing the device 10.

To understand the design considerations associated with this device, it will be particularly helpful to consider the electron potential energy diagrams of FIGURES 2 and 3 along with the device 10 shown in FIGURE 1. FIGURE 2 shows the potential energy diagram for unbiased conditions when the thin semiconductor layer 14 of device 10 is composed of lightly doped P-type semiconducting material, and FIGURE 3 is an electron potential energy diagram for the cathode device 10 suitably biased for hot electron emission. The ordinate of the graphs or diagrams represents the energy of the electron, while the abscissa corresponds to the distance across the device 10, or vertically through the device as it appears in FIGURE 1. It is to be pointed out that the graphs are not intended to be to scale. The line 24 corresponds to the edge of the space charge barrier region 35 at the intersection of the first semiconductor layer 11 and the metal layer 13, and the line 25 corresponds to the intersection of the metal layer 13 and the second semiconducting layer 14. The dotted line 23 denotes the "Fermi level" and represents the energy level which has a fifty percent probability of being filled by electrons. Lines 21 and 22 represent the bottom of the conduction band and the top of the valence band respectively of the first semiconductor layer 11, the space in between representing the energy gap characteristic of the semiconductor material. Similarly lines 31 and 32 represent the bottom of the conduction band and the top of the valence band respectively of the P-type semiconducting material 14. Regions 26, 27, 28, and 29 correspond to the layers 11, 13, 14, and 15, respectively.

Looking now at FIGURE 3 it is observed that under the influence of a forward bias across the rectifying space charge barrier region 35, electrons are emitted from the first semiconductor layer 11, represented by the region 26 on the graph, into the metal layer 13, represented by the region 27. The forward bias which tends to lower the height of the space charge barrier to a value 36 is provided by connecting the voltage source 16 shown in FIGURE 1 between these two layers. The current drawn between layers 11 and 13, represented by regions 26 and 27 respectively on the graph, increases approximately exponentially with increasing V_1 , (i.e., as voltage source 16 is increased in magnitude). However, most of the electrons contributing to the current come from energies just above the space charge barrier region 35. In the absence of V_2 (i.e., when the voltage source 17 is zero or disconnected) then most of the electrons do not have sufficient energy to surmount the work function 33 of layer 15, represented by region 29 on the graph, and the current emitted into vacuum is a very small fraction of the total current drawn between layers 11 and 13, i.e., the efficiency is low. The same problem exists when the layers 11 and 13, represented by regions 26 and 27 respectively, alone are used as a cold cathode.

The invention described herein overcomes this difficulty by the action of layers 14 and 15, represented by the regions 28 and 29 on the graphs, in conjunction with the voltage source 17.

The voltage source 17 is of sufficient magnitude and connected with the polarity shown in FIGURE 1 such that its action lowers the vacuum level, denoted by the line 34 on the graphs in FIGURES 2 and 3, to enable the electrons which travel across the metal region 27, semiconductor region 28, and metal region 29, to escape into the vacuum region 30 over the work function 33, thereby being emitted. When the space charge barrier junction is forward biased under the action of voltage source 16 as described above, the current emitted into vacuum over the work function 33 of layer 15 is initially very small. The emitted current increases with increasing V_2 (i.e., as the magnitude of voltage source 17 is in-

creased) until the emitted current obtains a saturated value. Saturation occurs when the magnitude of voltage source 17 is sufficient to bring the work function 33 of layer 15, represented by region 29 on the graph, even with or below the height of the space charge barrier 35 as shown in FIGURE 3.

The amount of saturated current emitted into the vacuum region 30 above the vacuum level 34 is thereafter determined by the magnitude of the voltage source 16. The saturated current will therefore increase until the magnitude of the voltage source 16 is sufficient to raise the bottom of the conduction band 21 in region 26 approximately even with the top of the space charge barrier 35.

Due to the influence of the thin semiconductor layer 14 and also the low work function coating 15, it is possible to emit a large number of electrons into the vacuum region 30 utilizing comparatively small bias voltages thereby making a practical and efficient cathode. For example, the voltage source 16 would be adjusted to a value of approximately 0.2 to 0.7 volt, and the voltage source 17 would be adjusted to a value of approximately 1.0 to 3.0 volts. These small voltages will avoid erratic characteristics associated with cathodes requiring operation at higher voltages.

Pursuant to the above-described conditions, and neglecting electron collisions, which lead to energy losses, there would be an extremely high emission current density and one of very low noise. This is because the spread in energies of the electrons being emitted into the vacuum would correspond to that in the semiconductor material. Since the semiconductor layer 11 is operated at the temperature of the enclosure in which the device is utilized, the noise temperature would consequently be the same.

Now in actual fact, of course, the electrons do have collisions both in the metal layer 13 and within the thin semiconductor layer 14. Considering first the metal layer 13, there are two types of collisions which are of importance: (1) electron-phonon collision which leads to a change in the direction of the electron velocity without, however, an appreciable energy loss; (2) an interaction of the "hot" electrons with the free electrons in the metal, as so-called electron-electron collision. This latter collision has been extensively studied in theory and it can be shown that on the average the electron during one of these collisions will lose approximately two thirds of its excitation energy above the Fermi level. Thus, after one of these collisions, an electron in the metal layer 13 can be ignored as far as its emission into the semiconductor region 14 is concerned. In order to overcome this difficulty, thereby increasing the efficiency of the present invention, the space charge barrier hot electron cathode, it is desirable to fabricate the metal layer 13 to a width less than or of the order of its so-called electron-electron attenuation length. There have been extensive calculations of the range of an electron in a metal which is determined by the random walk process induced by the phonon scattering mechanism and ending in the "death" of the electron when it has an electron-electron collision. It appears that metals with a strong peak in the density of states arising from electrons in the "d" shells of the atoms of the metal have very long electron-electron attenuation lengths. Typical values of attenuation lengths that have been calculated or measured experimentally are: Silver—440 A.; gold—740 A.; palladium—170 A.; and copper—50–200 A. Based on these measurements, it is advisable, although not absolutely necessary to the operation of the present invention, in order to achieve a reasonably efficient electron transfer across the metal layer 13 to have the thickness of this layer no thicker than 100 or 200 A. and preferably thinner than this provided the layer is not discontinuous and its sheet resistance not excessive.

With respect to the second semiconductor layer 14 shown in FIGURE 1, three types of electron collisions must be considered: (1) Electron-phonon collisions.

(These are of two types involving either acoustic phonons or optical phonons.) (2) Electron-electron collisions. (These are collisions of the electrons with the free electron gas in the semiconductor layer 14.) (3) Impact ionization collisions. (Here the "hot" electron in the semiconductor region 14, if it is sufficiently energetic, can interact with an electron in the valence band of the semiconductor material and excite it to the conduction band, thereby leaving both electrons at a lower energy than the initial energy of the high energy electron.) From the point of view of collisions leading to a considerable energy loss, the impact ionization collision is the most potent one. However, it can only occur if the energy of the electron exceeds the threshold for this effect. There have been many discussions in the literature as to where this threshold occurs. Certainly it must be larger than the energy gap of the semiconductor material. However, how much larger is still a matter of controversy. Some people claim that it occurs for a value which is only slightly in excess of the energy gap.

Another quantity which is the subject of considerable controversy is the mean free path an electron has to traverse before it, in fact, does excite an electron from the valence band. Some estimates for this quantity are that it would be extremely short, just a few tens of angstroms. There are other estimates which make the distance closer to a hundred angstroms.

With these difficulties in mind, a preferred embodiment of the present invention entails having the second semiconductor layer 14 as thin as possible, but thick enough to prevent large leakage currents by way of the tunnel emission process or electrical breakdown by way of the charge multiplication and subsequent avalanche breakdown. In addition, it is desirable to have the semiconductor layer 14 fabricated from material having a relatively large energy band gap. There is a limitation upon this of course, since a large energy band gap correspondingly means a large barrier height at the intersection of the metal layer 13 and the semiconductor layer 14. Depending upon the particular desired operating characteristics of the cathode of this invention, a compromise would thereby have to be effected using a material having as high a band gap as is possible while at the same time obtaining the desired barrier height. Furthermore, if the surface of the semiconductor layer 14 is supplied a low work function coating such as cesium or barium as denoted by the layer 15 of FIGURE 1, and if the bias 17 between the metal layer 13 and the semiconductor layer 14 is kept sufficiently small, the energy supplied the "hot" electrons is lowered so as to minimize the likelihood of their exciting electrons from the valence band in the semiconductor layer 14.

Similarly, in a preferred embodiment where the energy losses are to be minimized, the layer 15 should be only a few mono-layers thick. However, in a somewhat less efficient configuration, the layer 15 is thick enough to minimize the possibility of voltage drops across the layer resulting in a nonuniform distribution of voltage across the semiconductor layer 14. A thickness up to several hundred angstroms or more may therefore be required.

In accordance with the above considerations and as an important aspect of this invention, it may be desirable to fabricate the layer 14 from high resistivity intrinsic semiconductive material. With the higher resistivity material, there will be fewer charge carriers present in the layer; consequently, there will be a minimum of collisions resulting in energy losses. Alternatively, since it may be difficult to achieve the purity level associated with intrinsic semiconductive material, a lightly doped P-type semiconductive material may be used as the layer 14. Consequently the majority carriers will be holes rather than electrons, as would be the case if N-type material were used. As a result, the probability of loss of energy due to impact ionization collisions and electron-electron collisions will be greatly reduced.

With these design considerations in mind, there is now described one method for fabricating the invention, the space charge barrier hot electron cathode, shown in FIGURE 1. Upon a body of N-type semiconducting material 11, such as doped gallium arsenide, for example, there is deposited by any conventional technique, such as evaporation, the thin metal layer 13. This layer may be fabricated from a wide range of metals. As a particular example, however, gold has been found to be very favorable. The area of deposition can be controlled by masking, and the layer 13 should be as thin as possible in line with the above discussion, should be very dense, and closely bonded to the N-type semiconducting material 11.

Next a semiconductor layer 14, formed of either intrinsic or lightly doped P-type semiconductor material in accordance with the previous discussion, is formed adjacent the metal layer 13. This formation may be accomplished by any one of several techniques presently known as, for example, sputtering the layer 14 upon the metal layer 13 within an inert atmosphere. The thickness of layer 14 would depend in part, on the particular material employed for layer 14 for, as pointed out earlier, the layer 14 must be thin enough to avoid impact ionization losses (preferably a few hundred angstroms) and thick enough to avoid leakage or avalanching.

As the final steps in the manufacture of the present invention, a thin layer 15 of barium or cesium is evaporated upon the surface of the layer 14. Thereafter, in a conventional manner, ohmic contacts are attached to each of the layers as illustrated in FIGURE 1, to allow for the external bias connections.

FIGURES 4-11 show an alternative method for fabricating the space charge barrier "hot" electron cathode. FIGURE 4 is a top view of a single crystal, semi-insulating intrinsic substrate in which the crystallographic [111] plane forms the upper surface 40a, as can be seen in the sectional view of FIGURE 5. An active N-type semiconducting region 42 is formed over a predetermined area of the surface 40a of the substrate 40 either by diffusing the proper dopants into the semi-insulating substrate or by epitaxially depositing a layer of active N-type semiconducting material on the substrate. The diffusing technique is illustrated in FIGURE 7. Each of these techniques is well-known to those skilled in the art. The active semiconducting region 42 does not cover the entire semi-insulating substrate 40 and is preferably somewhat elongated so as to provide a relatively narrow area for crystal overgrowth as will presently be described. The area of the region 42 can be controlled by suitable and well-known masking techniques, and may be formed to a thickness of several mils. As can be seen in FIGURE 7, the active region 42 is preferably counterset in the substrate 40 so as to have a common upper surface, and this is more easily accomplished by diffusion of the N-type dopant into the semi-insulating substrate. However, it is to be understood that the active region 42 may also be deposited upon the surface of the substrate 40.

Next, a metallic film 44 is deposited over a major portion of the active region 42 substantially as illustrated in FIGURES 8 and 9. Again the area of deposition can be controlled by masking. It will be noted that a tab portion 42a of the active region 42 is not covered so as to provide an electrical contact for the first active semiconducting region. However, it will be noted that the metal film 44 extends out past the edges of the active region 42 except for the tab portion and covers a portion of the semi-insulating substrate 40 for insulation purposes, as will hereinafter be described in greater detail. A tab portion 44a of the metallic film 44 is also formed to provide a means for establishing electrical contact with the metal film. The metallic film 44 should be as thin as possible in line with the above discussion and should be very dense and closely bonded to the active N-type semiconductor region 42, but need not be a single crystal.

Next a semiconducting material, either intrinsic in nature or slightly doped with a P-type dopant in accordance with the previous discussion, having a crystallographic structure adapted for epitaxial growth on the substrate 40 is epitaxially deposited in the area illustrated in FIGURES 10 and 11 to produce a second semiconducting region 46. It will be noted that the active region 46 extends around the periphery of the metallic film 44 so as to be initially deposited on the single crystal semi-insulating substrate 40, yet is properly masked so as not to extend over the tab portion 42a of the first semiconductor region 42. A tab portion 46a is also provided on the semiconducting material 46 for electrical contact purposes. Since the semiconductor material 46 must be epitaxially deposited on the semi-insulating substrate 40, the two materials must have epitaxially compatible crystallographic structures.

As the epitaxial deposition process is carried out, the semiconducting material 46 forms on the single crystal substrate 40 rather than on the metal layer 44 and each nucleated layer tends to spread at a much greater rate in the [111] plane, which it will be recalled forms the surface 40a. Thus successive crystalline layers build on the substrate 40 around the periphery of the metal layer 44 until the layer is of greater thickness than the metal film 44. Then the tendency to grow in the [111] plane parallel to the surface 40a causes the semiconducting single crystal deposit to spread over the metal layer 44 and form a single crystal structure. Pursuant to the design considerations previously discussed, the growth of the semiconductor layer 46 should be controlled so that the portion of the layer 46 over the metal layer 44 will be as thin as possible.

Thereafter, in a conventional manner a very thin low work function coating such as cesium or barium may be deposited upon the upper surface of the layer 46. Electrical contacts can then be made with the device through the tabs 42a, 44a, and 46 shown in FIGURE 10.

In accordance with some particular aspects of the present invention, any semiconductor substrate having the desired electrical characteristics and the desired crystal structure can be used to practice the method of the present invention. However, GaAs in the semi-insulating or "intrinsic" form having a resistivity on the order of 10^8 ohm-cm. is preferred for the substrate 40 shown in FIGURES 4-11. The semi-insulating GaAs will provide both electrical isolation for active components deposited thereon and also a crystalline surface onto which single crystal semiconductor depositions can be made by well-known epitaxial techniques. In particular, the layer 46, shown in FIGURE 11, and corresponding to the second semiconductor layer 14 of FIGURE 1, may also be formed of GaAs material, either intrinsic or slightly P-type, which can be epitaxially deposited upon the GaAs semi-insulating substrate. A low deposition temperature for the layer 46 is necessary in order to minimize interdiffusion of the metal and semiconductor materials, and also to minimize surface migration of the atoms in the metal layer 44 and their coalescence into islands. GaAs offers a good compromise as between the temperature required for the deposition process and the desired energy band gap for efficient emission of electrons. For example, GaAs has a band gap of approximately 1.38, and requires substrate temperatures of about 750° C. for epitaxial deposition either by chemical transport, or by physical transport, such as sputtering for example.

Another advantage for fabricating the "hot electron" cathode according to the previously described method is that a wide range of metals can be used to form the thin metallic layer between the semiconducting layers. This is permitted because the metal layer may be amorphous or polycrystalline, and no particular crystal structure is required. However, the particular metal used for the metallic layer should be chosen with the following characteristics

in mind: (1) relatively long electron-electron mean free path; (2) melting point favorable for deposition techniques; (3) ease of deposition; (4) physical and chemical durability; (5) solubility in materials used for semiconductor regions adjacent to metallic layer. As a particular example, the element gold has been found to be a favorable compromise for use as the thin metallic layer.

While the fabrication of this invention has been described with reference to one specific method, it is to be understood that this description is not to be construed in a limiting sense. In particular, other methods of fabrication known in the art may be used when either of the semiconductor layers is desired to be formed of polycrystalline material.

Various modifications of the disclosed embodiments, as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. An electron emitting device comprising a first layer of semiconductor material having electrons as majority conduction carriers, a second layer of semiconductor material having holes as majority conduction carriers, a first metal layer adjacent to and intermediate the two semiconductor layers, means for providing a low work function surface on the second semiconductor layer, means for biasing the first metal layer positive with respect to the first layer of semiconductor material, and means for biasing the second layer of semiconducting material positive with respect to the first metal layer.

2. An electron emitting device comprising a first layer of semiconductor material of a first conductivity, a second layer of semiconductor material of a second conductivity, a metal layer adjacent to and intermediate the first and second semiconductor layers, metal means adjacent the second layer of semiconductor material for providing a low work function surface on said second layer of semiconductor material, means for biasing the first metal layer positive with respect to the first layer of semiconductor material, and means for biasing the second layer of semiconducting material positive with respect to the first metal layer.

3. A device comprising a first layer of semiconductor material of a first conductivity, a second layer of semiconductor material of a second conductivity, a thin metal layer interposed between the first and second layers of semiconductor material, a second metal layer overlying the second semiconductor layer, said second metal layer having a work function lower than that of said second semiconductor layer, means for biasing the layers so that electrons will travel from the first layer of semiconductor material through the remaining layers and be emitted out of the second metal layer.

4. A cold cathode device comprising a region of N-type GaAs, a thin layer of gold contiguous to a surface of the region and forming a metal-semiconductor barrier at the interface of the gold layer and the GaAs layer, a thin layer of high resistance GaAs overlying the layer of gold over said surface, metal means overlying the layer of high resistance GaAs for providing an energy barrier at the surface of such layer, means for biasing the layer of gold with a positive potential with respect to the region of N-type GaAs, and means for biasing the layer of high resistance GaAs with a positive potential with respect to the layer of gold.

5. A cold cathode device comprising a region of N-type GaAs, a thin layer of gold contiguous to a surface of the region and forming a metal-semiconductor barrier at the interface of the gold layer and the GaAs layer, a thin layer of P-type GaAs overlying the layer of gold over said surface, metal means overlying the layer of P-type GaAs for providing an energy barrier at the surface of

such layer, means for biasing the layer of gold with a positive potential with respect to the region of N-type GaAs, and means for biasing the layer of P-type GaAs with a positive potential with respect to the layer of gold.

6. The device of claim 2 wherein said metal means is a metal coating selected from the group consisting of barium and cesium.

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