PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION International Bureau



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6: WO 96/38774 (11) International Publication Number: G06F 1/32 A1 (43) International Publication Date: 5 December 1996 (05.12.96)

(21) International Application Number:

PCT/US96/02391

(22) International Filing Date:

21 February 1996 (21.02.96)

(30) Priority Data:

08/457,531

1 June 1995 (01.06.95)

US

(71) Applicant: AST RESEARCH, INC. [US/US]; 16215 Alton Parkway, Irvine, CA 92718 (US).

(72) Inventor: TANIKAWA, Roy, K.; 3611 Myrtle Street, Irvine, CA 92714 (US).

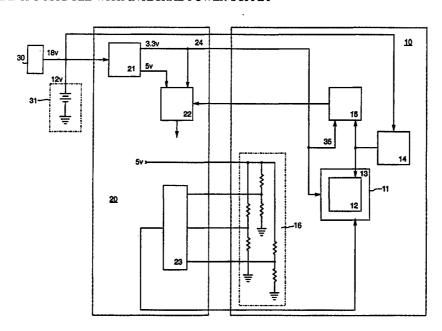
(74) Agents: FREEMAN, Corrine, M. et al.; Lyon & Lyon, First Interstate World Center, Suite 4700, 633 West Fifth Street, Los Angeles, CA 90071 (US).

(81) Designated States: AU, CA, CN, JP, KR, MX, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published

With international search report.

(54) Title: UPGRADE CPU MODULE WITH INTEGRAL POWER SUPPLY



(57) Abstract

A computer processing unit (CPU) module (10) is described. The present CPU module (10) accommodates a CPU (11) and includes a power supply (14), a power good detection circuit (15) and a clock speed selector (16), all of which are integral to the CPU module (10). The power supply (14) provides the CPU module (10) with the ability to convert power supplied to the CPU module (10) to power as needed by the CPU (11). The power good detection circuit (15) provides the CPU module (10) with the ability to notify the mother board (20) of a power supply to the CPU (11) which is below the operating voltage of the CPU (11) (e.g. a power failure or insufficient voltage). The clock speed selector (16) provides the CPU module (10) with the ability to automatically set the clock speed to that required by the CPU (11) without modification to the BIOS stored on the mother board (20) or changing components.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgystan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic	SD	Sudan
CF	Central African Republic		of Korea	SE	Sweden
CG	Congo	KR	Republic of Korea	SG	Singapore
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LR	Liberia	SZ	Swaziland
CS	Czechoslovakia	LT	Lithuania	TD	Chad
CZ	Czech Republic	LU	Luxembourg	TG	Togo
DE	Germany	LV	Latvia	TJ	Tajikistan
DK	Denmark	MC	Monaco	TT	Trinidad and Tobago
EE	Estonia	MD	Republic of Moldova	UA	Ukraine
ES	Spain	MG	Madagascar	UG	Uganda
FI	Finland	ML	Mali	US	United States of America
FR	France	MN	Mongolia	UZ	Uzbekistan
GA	Gabon	MR	Mauritania	VN	Viet Nam

1

DESCRIPTION

UPGRADE CPU MODULE WITH INTEGRAL POWER SUPPLY FIELD OF INVENTION

The present invention relates to a module (or board) for a microprocessor or computer processing unit (CPU), particularly a CPU module which accommodates a CPU and which includes a power supply, a power good detection circuit and a clock speed selector integral to the module.

10 BACKGROUND

5

15

20

25

30

1

35

In improving microprocessors (i.e. computer processing units or CPUs) manufacturers change the design to make the CPUs more efficient, faster, etc. Often with such improvements and/or new designs the operating requirements of the CPUs change (e.g. the required operating voltage, the required clock speed, etc.). For example, at one time both the central core and input/output interface (I/O) of Intel® CPUs operated at 5 volts. Then certain CPUs were upgraded and both the central core and I/O interface operated at 3.3 The central core and the I/O interface of a new Pentium $^{\scriptsize (8)}$ CPU by Intel $^{\scriptsize (8)}$ operates at 2.9 volts and 3.3 volts respectively. This trend of operating voltage changes as CPUs are upgraded is expected to continue. The trend of the central core and the I/O interface of a CPU requiring different voltages is also expected to continue.

Commonly when the CPU in a computer is upgraded the mother board of the computer must be manipulated to remove the existing CPU, to install a new CPU, and to accommodate the new CPU (e.g., reconfigure the mother board to adjust for different power and/or clock speed requirements, etc.). To facilitate the removal, installation, and accommodation of CPUs it is known to provide CPUs on an upgrade CPU module (or board) separate from the mother board whereby an old CPU can be removed by simple removal of the entire CPU module and a

2

new CPU can installed by simple installation of an upgrade CPU module.

5

10

15

20

25

30

35

To further facilitate the ability to upgrade a computer system through the installation of an upgraded CPU, upgrade CPU modules have been manufactured with integral power supplies to convert the voltage supplied by the mother board to the CPU from 5 volts to 3.3 volts as appropriate for the particular CPU (core and/or I/O interface) provided on the CPU module. The power supply provided on the CPU module can also convert the voltage supplied externally from an AC to DC wall adapter (18 volt DC output) or internally from a battery (12 volt DC) to 3.3. volt DC current as appropriate for the CPU core and/or I/O interface. Thus, a CPU module can be manufactured with a power supply to accommodate the CPU on the CPU module without having to change the power supply on the mother board.

However, such prior CPU modules (even those with integral power supplies) do not provide feedback information to the mother board (e.g. do not communicate that the power supply to the CPU is below the operating voltage of the CPU). Therefore, there can be sufficient power for the mother board to run and the mother board does not recognize if the power level has not stabilized sufficiently for the CPU to run (e.g., due to a module power supply failure). Therefore, the CPU can be stopped due to a power failure or insufficient voltage while the rest of the mother board continues to run without identifying the CPU power problem. power failure message is not communicated to the mother board prompting it to turn off the power supply and protect the rest of the mother board. This situation also can frustrate attempts to identify what is wrong with the inoperable computer.

In addition, such CPU modules (even those with integral power supplies) do not accommodate for upgrade CPUs which require a clock speed different from the

3

clock speed for which the mother board was configured for the original CPU. While the clock speed of a computer can typically manipulated by modifying the BIOS (typically stored on a chip on the mother board) or changing components, such modification requires the intervention of a knowledgeable person. It is beneficial if the clock speed can be automatically set at the speed required by the new CPU without manipulation of the BIOS or changing components. However, such a feature has not yet been provided.

Prior CPU modules have not provided adequate solutions to these problems.

5

10

15

20

25

30

35

SUMMARY OF THE INVENTION

The present invention provides a CPU module which affords solutions to the problems described above. Particularly, the present invention provides a CPU module that accommodates a CPU and includes a power supply, a power good detection circuit and a clock speed selector, all integral to the CPU module.

The power supply of the present invention provides the CPU module the ability to convert power supplied to the CPU module by the mother board or an internal or external source into the power required by the particular CPU (e.g. AC to DC and 18, 12, 5.0, or 3.3 volts to 2.9 volts).

The power good detection circuit of the present invention provides the CPU module the ability to communicate to the mother board that the supply of power is below the operating voltage of the CPU (e.g. a power failure or insufficient voltage to the CPU).

The clock speed selector of the present invention provides the CPU module the ability to automatically set the clock speed to that required by the particular CPU on the CPU module.

Accordingly it is a primary object of the present invention to provide an improved CPU module with an integral power supply.

4

It is an additional object of the present invention to provide a CPU module with an integral power good detection circuit.

It is a further object of the present invention to provide a CPU module with an integral clock speed selector.

5

10

15

20

25

30

35

Other objects and features of the present invention will become apparent from consideration of the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the CPU module of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT
As is shown in FIG. 1, the preferred embodiment of
the present invention comprises a CPU module (or board)
10 which accommodates a CPU 11 (comprising a CPU core 12
and an I/O interface 13) and which includes a CPU module
power supply 14, a CPU module power good detection
circuit 15, and a clock speed selector 16, all of which
are integral to the CPU module 10 and connectable to a
mother board 20. As is described above, arranging the
CPU 11 on a CPU module 10 provides a convenient mode of
removing a CPU from and installing a new CPU onto a
mother board.

As is also shown in FIG. 1, the mother board 20 includes a mother board power supply 21, a mother board power good detection circuit 22, and a clock 23. Although FIG. 1 shows the mother board 20 and the CPU module 10 as separate, the CPU module 10 is attachable (electrically and physically) to the mother board 20.

As is typical in the industry, the mother board 20 is supplied with power either from an external source 30 (e.g. a wall plug outlet) and/or from a battery source 31 which can be internal or external. The power is supplied to the mother board power supply 21 which then converts the power to that voltage required by the

5

components (e.g. AC to DC and 18 volts or 12 volts to 5 volts and/or 3.3 volts). The mother board power supply 21 also provides power to the mother board power good detection circuit 22 which checks the power supplied and ensures that it is within the tolerance range of the components receiving power. Typically, if the power is below operating voltage, the power good detection circuit 22 communicates this to the mother board 20 which then, typically, indicates the same and waits until the power is sufficient. In the preferred embodiment of the present invention the mother board power supply 21 also supplies power to the I/O interface 13 of the CPU module 10, for example, via line 24 in FIG. 1.

5

10

15

20

25

30

35

In the preferred embodiment of the present invention, as shown in FIG. 1, the CPU module 10 is supplied power as is the mother board 20: from either an external source 30 (e.g. a wall plug outlet) and/or a battery source 31 which can be internal or external. The power is supplied to the CPU module power supply 14 which then converts the power to that voltage required by the CPU core 12 (e.g. AC to DC and 18 volts or 12 volts to 3.3 or 2.9 volts depending on the power supplied and on the particular CPU) and provides the converted power to the CPU core 12. The CPU module power supply 14 also provides power to the CPU module power good detection circuit 15 which checks the power supplied and ensures that it is within the operating voltage level of the CPU core 12. The CPU module power good detection circuit 15 communicates if the power is not at the operating voltage level to the mother board power good detection circuit 22 which then, as is described above, typically, indicates the same to the mother board 20 and waits until it is at the proper level.

As is described above, the I/O interface 13 is supplied power by the mother board power supply 21 and

the power supplied by the mother board power supply 21 is checked by the mother board power good detection circuit 22. As is shown in FIG. 1, the preferred embodiment of the present invention includes a redundant check on this power supply to the I/O interface 13 by the CPU module power good detection circuit 15 via, for example, line 35. Although the power for the I/O interface 13 is preferably supplied from the mother board 20 as shown, CPU module 10 of the present invention can be configured such that the I/O interface 13 is supplied power by a second CPU module power supply similar to CPU module power supply 14.

The inclusion of the CPU module power good detection circuit 15 helps prevent the situation where feedback information about whether the power supply to the CPU is below the operating voltage of the CPU is not communicated to the mother board 20. Therefore, the mother board recognizes if there is insufficient power for the CPU to run (e.g., due to a module power supply failure) and is able to turn off the power supply and protect the rest of the mother board.

In general, the clock 23 on the mother board 20 provides a clock cycle for all components requiring the same, including, typically, the CPU 11. However, as is described above, the clock speed of the clock 23 (i.e. the number of clock cycles per time period) is, typically, not easily adjusted (e.g. without modifying the BIOS or changing components) and, therefore, upgrading the CPU 11 to one which requires a clock speed different from the clock speed for which the mother board clock 23 was configured is, typically, not easily accomplished. The speed of a clock such as clock 23 (which is preferably a phase locked loop rather than a crystal oscillator) is typically dependent on the voltage supplied to it.

The preferred embodiment of the present invention, as shown in FIG. 1, includes a clock speed selector 16

7

(i.e. as a voltage divider circuit). The clock speed selector 16 is preferably provided power by the mother board 20. The clock speed selector 16 uses the power supplied by the mother board to provide the selection circuit with power which when provided to the clock 23 dictates the speed at which the clock 23 must be set for the particular CPU 11 on the CPU module 10. The clock speed selector 16 enables the CPU module 10 to be manufactured with the proper clock speed selector 16 for the CPU 11 to be provided thereon. Therefore, the preferred embodiment of the present invention enables the clock speed to be automatically set at the speed required by the CPU 11 without manipulation of the BIOS or changing components.

5

10

15

20

25

30

35

Thus, the preferred embodiment of the present invention provides a CPU module 10 which solves many problems of the prior art. Specifically, the CPU module 10 accommodates a CPU 11 and includes a CPU module power supply 14, a CPU module power good detection circuit 15, and a clock speed selector 16, all of which are integral to the CPU module 10. The CPU module power supply 14 provides the CPU module 10 the ability to convert power supplied to the CPU module 10 by the mother board 20 or internal or external sources 30 and 31 into the power required by the particular CPU 11. The CPU module power good detection circuit 15 provides the CPU module 10 with the ability to communicate to the mother board 20 that the supply of power is below the operating voltage of the CPU 11 (e.g. a power failure or insufficient voltage to the CPU). The clock speed selector 16 provides the CPU module 10 the ability to automatically set the clock speed to that required by the particular CPU 11 on the CPU module 10.

Thus, the CPU module 10 of the present invention facilitates upgrading and/or replacing the CPU of a computer system since the adjustment of all variable parameters affected by such an upgrade or replacement is

8

handled by the CPU module 10 which is assembled and set by the manufacturer. This provides convenience and efficiency to anyone replacing the CPU of a computer system, particularly to end users as the end user need not modify parameters.

While a preferred embodiment of the present invention has been shown and described, various modifications may be made without departing from the scope of the present invention, and all such modifications and equivalents are intended to be covered.

5

10

WO 96/38774

9

I CLAIM:

5

10

15

20

25

30

35

- 1. A computer processing unit module comprising a computer processing unit,
- a power supply integral to the module and configured to receive power from a source external to the module, said power supply further configured to supply power to the computer processing unit, and
- a power good detection circuit integral to the module and configured to check the power supplied to the computer processing unit.
- 2. The invention of claim 1 further comprising a clock speed selector circuit integral to the module and a clock external the module wherein the clock speed selector circuit is configured to set the speed of the clock to that required by the computer processing unit.
 - 3. A computer processing unit module comprising a computer processing unit,
- a power supply integral to the module and configured to receive power from a source external to the module, said power supply further configured to supply power to the computer processing unit, and
- a clock speed selector circuit integral to the module and a clock external the module wherein the clock speed selector circuit is configured to set the speed of the clock to that required by the computer processing unit.
 - 4. A computer processing unit module comprising a computer processing unit,
- a power supply integral to the module and configured to receive power from a source external to the module, said power supply further configured to supply power to the computer processing unit,
- a power good detection circuit integral to the module and configured to check the power supplied to the computer processing unit, and
- a clock speed selector circuit integral to the module and a clock external the module wherein the clock

speed selector circuit is configured to set the speed of the clock to that required by the computer processing unit.

5. A computer processing unit module comprising a computer processing unit comprising a core and an input/output interface,

5

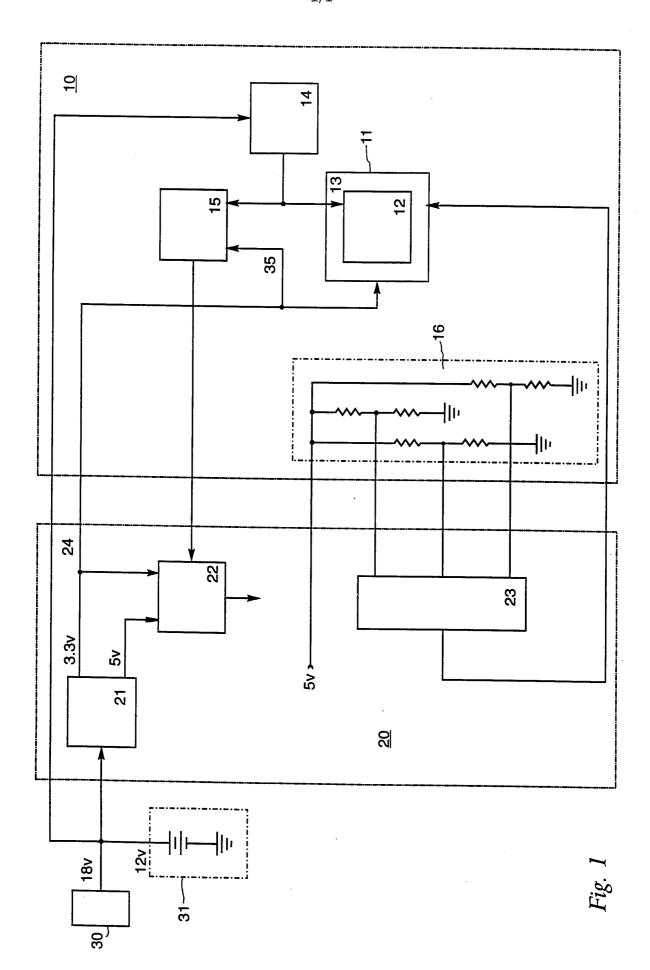
10

15

20

25

- a first power supply integral to the module and configured to receive power from a source external to the module, said first power supply further configured to supply power to the core of the computer processing unit, and
- a second power supply integral to the module and configured to receive power from a source external to the module, said second power supply further configured to supply power to the input/output interface of the computer processing unit.
- 6. The invention of claim 5 further comprising a power good detection circuit integral to the module and configured to check the power supplied to the computer processing unit.
- 7. The invention of claim 5 further comprising a clock speed selector circuit integral to the module and a clock external the module wherein the clock speed selector circuit is configured to set the speed of the clock to that required by the computer processing unit.



INTERNATIONAL SEARCH REPORT

International application No. PCT/US96/02391

A. CLASSIFICATION OF SUBJECT MATTER IPC(6): G06F 1/32 US CL: 395/750						
According to International Patent Classification (IPC) or to both national classification and IPC						
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols)						
U.S.: 395/750, 113;364/707						
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched						
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)						
C. DOCUMENTS CONSIDERED TO BE RELEVANT						
Category*	Citation of document, with indication, where ap	propriate, of the relevant passages	Relevant to claim No.			
Υ	US, A, 5,230,074 (CANOVA, JR. Figure 1 item 66.	ET AL) 20 July 1993, see	1,4,6			
Υ	US,A, 5,006,790 (BEVERLY, II ET Figure 3 item 48.	1,4,6				
Υ	US,A, 4,716,463 (STACY ET AL) 29 December 1987, see 1,4,6 Abstract					
Y,P	US, A, 5,481,697 (MATHEWS ET A	2,3,4,7				
Y	US, A, 5,142,684 (PERRY ET AL) 25 August 1992, see 2,3,4,7 Abstract					
Υ	US, A, 4,615,005 (MAEJIMA ET see Figure 2 item 21	2,3,4,7				
Further documents are listed in the continuation of Box C. See patent family annex.						
Special categories of cited documents: "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention						
	to be part of particular relevance earlier document published on or after the international filing date "X" document of particular relevance; the claimed invention cannot be					
"L" do	cument which may throw doubts on priority claim(s) or which is ed to establish the publication date of another citation or other	considered novel or cannot be conside when the document is taken alone "Y" document of particular relevance: the	•			
"O" do	ecial reason (as specified) cument referring to an oral disclosure, use, exhibition or other cans	"Y" document of particular relevance; the considered to involve an inventive combined with one or more other such being obvious to a person skilled in the	step when the document is h documents, such combination			
"P" do	cument published prior to the international filing date but later than e priority date claimed	*&" document member of the same patent				
Date of the actual completion of the international search Date of mailing of the international search report						
29 APRIL 1996 0 8 MAY 1996						
Commissio Box PCT	mailing address of the ISA/US mer of Patents and Trademarks n, D.C. 20231	Authorized officer PAUL R. MYERS	WILL			
F ' '1 N	T ₌ (702) 205 2220	The lambage Nic				