



- (51) International Patent Classification:
H01L 23/12 (2006.01)
- (21) International Application Number:
PCT/US2016/017788
- (22) International Filing Date:
12 February 2016 (12.02.2016)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
62/127,499 3 March 2015 (03.03.2015) US
- (71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).
- (72) Inventors: DUBEY, Manish; 3662 E Mead Drive, Chandler, Arizona 85249 (US). NEKKANTY, Srikant; 400 North Coronado Street, Apt. 1073, Chandler, Arizona 85224 (US). DIAS, Rajendra C.; 14230 South 14th Street, Phoenix, Arizona 85048 (US). NARDI, Patrick; 2125 North 68th Place, Scottsdale, Arizona 85257 (US).
- (74) Agents: PERDOK, Monique M. et al.; P.O. Box 2938, Minneapolis, Minnesota 55402 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: ELECTRONIC PACKAGE THAT INCLUDES MULTI-LAYER STIFFENER

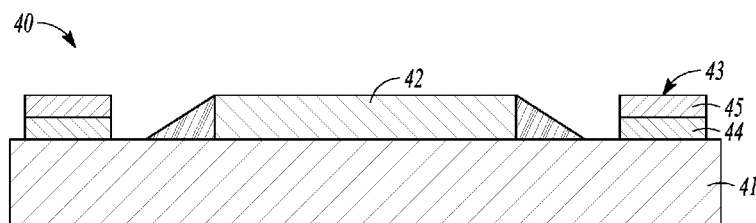


FIG. 5

(57) Abstract: An electronic package that includes a substrate and a die attached to the substrate. The electronic package further includes a stiffener that is attached to the substrate adjacent to the die. The stiffener is formed of a first layer made from one material and a second layer made from a different material.

ELECTRONIC PACKAGE THAT INCLUDES MULTI-LAYER STIFFENER

Claim of Priority

5 **[0001]** This patent application claims the benefit of U.S. Provisional Patent Application No. 62/127,499, filed March 3, 2015, entitled “ELECTRONIC PACKAGE AND METHOD OF CONNECTING A FIRST DIE TO A SUBSTRATE TO FORM AN ELECTRONIC PACKAGE”, which is incorporated by reference herein in its entirety.

10

Technical Field

[0002] Embodiments described herein generally relate to an electronic package that includes a multi-layer stiffener.

15

Background

[0003] Minimizing transistor size in order to keep up with Moore's law continually requires reducing first level interconnect (FLI) pitch and bump size. In addition, using advanced dielectrics has often resulted in utilizing low-k and extremely low-k materials in silicon.

20 **[0004]** The combination of these factors results in higher sensitivity to stress during assembly and thermo-mechanical stress. Therefore, with each new technological advancement, solutions for reducing thermo-mechanical stress become significantly more important.

[0005] The thickness of semiconductor devices has been shrinking with
25 the advent of small form factor devices such as smartphones and tablets. As a result, coreless packaging is gaining more attention for small form factor devices. The absence of a core in the substrate of electronic packages typically implies that there is relatively higher warpage for such conventional packages.

[0006] One other advancement in packaging technology has been in the
30 area of ball grid array (BGA) pitch reduction, which is often capable of obtaining smaller form factors. The combination of coreless packaging and reduced BGA pitch requires very tight peak to valley warpage control of the electronic package in order to fabricate such electronic packages using an efficient surface mount (SMT) process.

[0007] Two of the solutions that are commonly employed used to overcome the warpage problem are to use (a) molded underfill (MUF) and (b) a stiffener. The thickness of the MUF and the stiffener is driven by the thickness of the dice that form the electronic package.

- 5 [0008] These existing solutions are often able to provide sufficient process control for electronic packages where the die thickness is ~300 microns or greater. However, these existing solutions are often unable to provide sufficient process control (i.e., too much warpage) for electronic packages as the die thickness becomes smaller (e.g., gets closer to 100-200 microns).

10

Brief Description of the Drawings

- [0009] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Portions and features of some embodiments may be included in, or substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.

- 15 [0010] Figure 1 shows the changes in peak-to-valley warpage as a function of die thickness.

- 20 [0011] Figure 2 shows modeling data that demonstrates where using bimetallic material stiffeners may provide improved warpage control during SMT of thin dice.

- [0012] Figure 3 shows modeling data that demonstrates where even after reducing the width of the stiffener a bimetallic stiffener, the warpage may be less than a full width monolithic stiffener.

- [0013] Figure 4 shows that the materials for the bimetallic stiffener may be chosen to form chemical/metallurgical joints with a conductive adhesive.

- [0014] Figure 5 shows the cross-sectional view of an example electronic package.

- 30 [0015] Figure 6 shows another form of the electronic package shown in Figure 4.

- [0016] Figures 7A-7B shows example exaggerated room temperature and high temperature warpage on a bimetallic stiffener system.

Description of Embodiments

[0017] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Portions and features of some embodiments may be included in, or substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.

[0018] Orientation terminology, such as “horizontal,” as used in this application is defined with respect to a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term “vertical” refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as “on,” “side” (as in “sidewall”), “higher,” “lower,” “over,” and “under” are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

[0019] The electronic packages and methods described herein may address issues associated with maintaining warpage control on thinner dice with tighter BGA pitch. The basic principle is based on the CTE mismatch, which is what drives warpage in the first place.

[0020] The electronic packages and methods described herein use a bimetallic two-material stiffener which not only provides stiffness when the packages warps but also provides an opposing moment at higher temperatures to further reduce warpage. The opposing moment will counter the high temperature warpage of the electronic package, thereby reducing the mean warpage of the entire package.

[0021] Modeling data is presented in Figure 1 that illustrates where warpage control gets worse as stiffeners become thinner on the same electronic package. Specifically, Figure 1 shows the changes in peak-to-valley warpage as a function of die thickness. It is important to note that the thickness of the stiffener in this modeling was assumed to be the same as the die thickness.

[0022] As shown in FIG. 1, for the same package dimensions, the warpage gets worse as the dice get thinner. As an example, the target mean warpage TMW1 and the upper spec limit USL1 for 0.4 mm BGA pitch and .035 BGA pitch as shown in FIG. 1. In addition, the target mean warpage TMW1 and

upper spec limit USL1 for 0.4 mm BGA pitch is 80 and 140 μm respectively. While this is achievable for 270 μm dice as seen in Figure 1, it becomes more difficult for thinner dice.

[0023] Apart from the thickness of the die, BGA pitch reduction to 0.35 mm requires the target mean warpage TMW2 to drop down to 50 μm and the upper spec limit USL2 to drop down to 110 μm . This modeling data clearly shows that conventional stiffeners (e.g., conventional stainless steel stiffeners) do not provide the warpage control that is required for electronic packages with reduced die thickness and reduced BGA pitch.

10 [0024] The bimetallic two-material stiffener may provide warpage control on future thin die electronic packages that require tighter BGA pitch. Figure 2 shows modeling data that demonstrates where using bimetallic two-material stiffeners may provide improved warpage control during SMT of thin dice.

15 [0025] Specifically, Figure 2 shows as examples 25°C and greater than 200°C P-V the peak-to-valley warpage for (a) steel; (b) aluminum; and (c) steel/aluminum bimetallic strip and warpage. Figure 2 further shows a significant reduction in peak-to-valley warpage (~35%) when using a bimetallic two-material stiffener as compared to a monolithic stiffener.

20 [0026] As an example, a peak may equal the largest deflection in one direction and a valley may equal the largest deflection in an opposite direction. Deflection as measured may be considered the distance that the peak (or valley) is out of plane from a not deflected state of the electronic package.

[0027] The bimetallic stiffener materials and thicknesses may be selected for different die thickness such that the bimetallic two-material stiffener height does not exceed the die thickness. Therefore, the backside of the die may be exposed for thermal attachment to a substrate (e.g., to a heat sink).

[0028] As discussed above, the modeling data as shown in Figure 2 demonstrates a considerable improvement for high temperature warpage (35% better than steel and 45% better than aluminum). The room temperature warpage is also considerably better than the two monolithic stiffeners (35% better than steel and 7% better than aluminum). The modeling assumed equal

thickness (100 μm) for both of the metals in the bimetallic case for the sake of simplicity.

[0029] In some forms, further reduction in warpage may be achieved by tailoring the thickness and other material properties of the two metals. As an example, two materials may be selected with different CTE where the correct one is put on top so that the stiffener incorporates a bending moment that counters the expected warpage of the electronic package upon exposure to different temperatures. In addition, even better performance may be achieved by using multilayered metallic stiffener systems.

10 [0030] In addition to providing better warpage control for thin dice, the bimetallic two-material stiffener may also require a smaller footprint as compared to monolithic stiffeners. This smaller footprint may provide a smaller keep out zone (KOZ) for stiffeners. The smaller KOZ reduction may reduce the form factor of the electronic package without compromising warpage control of the electronic package.

[0031] Figure 3 shows the change in peak-to-valley warpage by reducing the width of the stiffener for bimetallic (e.g., aluminum & stainless steel) and monolithic (e.g., stainless steel) stiffeners. It should be noted that the peak-to-valley warpage for the narrow bimetallic two-material stiffener is still lower than the warpage for the full monolithic stiffener.

[0032] Specifically, the modeling data in Figure 3 shows that even after reducing the width of the two-material stiffener by ~50%, the delta warpage (25-260°C) of the bimetallic two-material stiffener is less than a full width monolithic stiffener. Figure 3 shows the modeling data obtained on a 170 μm thin die/stiffener. Figure 3 further illustrates that the delta warpage (25-260°C) for the narrow (650 μm on all sides) bimetallic two-material stiffener is lower than the warpage of the full (1250 μm on 2 sides and larger on other 2 sides) monolithic stiffener.

[0033] In some forms, the bimetallic two-material stiffener may be used to lower the high temperature warpage of the electronic package. Lowering the high temperature warpage of the electronic package may be achieved by joining the bimetallic sheets at higher temperature, which will produce stiffeners that are flat at the joining temperature. While joining the bimetallic sheets at higher temperature may not change the amount of warpage over a range of

temperatures, it may provide another way to control warpage depending on the electronic package design and the desired warpage requirements.

[0034] In addition, the bimetallic two-material stiffeners described herein may provide for a stiffener where the stiffener needs to be grounded to the substrate. Figure 4 shows that while it may be difficult to adhere metallic adhesive (e.g., solder) to stainless steel, the materials for the bimetallic material may be chosen to form electrical/chemical/metallurgical joints with the conductive adhesive to facilitate the stiffener conducting electricity.

[0035] In the example form shown in Figure 4, the bimetallic stiffener may provide an added benefit in situations where the stiffeners needs to be grounded to the substrate. While it is often difficult to adhere a metallic adhesive (e.g., solder) to stainless steel, the bimetallic materials may be chosen and arranged to form electrically conductive joints with the conductive adhesive.

[0036] Figure 4 is an enlarged view illustrating a portion of an example electronic package. Figure 5 illustrates the entire electronic package for the enlarged portion of the electronic package shown in Figure 4.

[0037] As shown in Figures 4 and 5, the electronic package 40 includes a substrate 41 and a die 42 (see Figure 5) attached to the substrate 41. The electronic package 40 further includes a stiffener 43 that is attached to the substrate 41 adjacent to the die 42. The stiffener 43 is formed of a first layer 44 made from one material and a second layer 45 made from a different material.

[0038] In some forms, the stiffener 43 entirely surrounds the die 42. In other forms, the stiffener 43 may partially surround the die 42. The determination to whether the stiffener 43 surrounds the entire die 42 will depend in part on the footprint design of the electronic package 40 (among other factors).

[0039] In addition, the stiffener 43 may be concentric with the die 42. The stiffener 43 may also be partially concentric with the die 42.

[0040] In some forms, stiffener 43 may have a substantial uniform cross-section. In other forms, the cross-section of the stiffener 43 may change in size. As an example, two opposing sides of the stiffener 43 may have one type of cross-section and the other two opposing sides may have another type of cross-section.

[0041] In addition, the first layer 44 may be the same size as the second layer 45. It should be noted that forms of the electronic package 43 are contemplated where the first layer 44 and the second layer 45 are different sizes.

[0042] In addition, the first layer 44 may have a different thickness than the second layer 45. In other forms, the first layer 44 may have the same thickness as the second layer 45. The relative thicknesses of the first layer 44 and the second layer 45 will depend in part on die 42 thickness, package dimensions, and the available footprint for the stiffener 43 (among other factors).

[0043] In some forms, the first layer 44 may be made of aluminum and the second layer 45 may be made of stainless steel. In another form, the first layer 44 may be made of a nickel alloy and the second material may be made of a manganese-copper-nickel alloy. It should be noted that a variety of materials are contemplated for the first layer 44 and the second layer 45. Some of the factors that determine the selection of the first layer 44 and the second layer 45 include (i) die thickness; (ii) package dimensions; (iii) package warpage; (iv) available foot-print of the stiffener 43; (v) ease of manufacturing; and/or (vi) cost (among other factors).

[0044] Figure 6 shows another example form of the electronic package 40. In the example electronic package 40 shown in Figure 6, the stiffener 43 in the electronic package 40 includes a third layer 46 that is made of a different material than the first layer 44 and the second layer 45. It should be noted that the relative size and thicknesses of the first layer 44, the second layer 45 and the third layer 46 will depend in part on many of the factors described above.

[0045] As shown in Figures 4 and 6, the electronic package 40 may further include a conductive adhesive 47 that secures the substrate 41 to the first layer 44 of the stiffener 43. First layer 44 is formed of an electrically conductive material such that the first layer 44 and the conductive adhesive 47 are electrically connected together.

[0046] In some forms, the substrate 41 of the electronic package 40 include a ground plane 48 such that the conductive adhesive 47 electrically connects the first layer 44 of the stiffener 43 to the ground plane 48.

[0047] As shown in Figures 4 and 6, an upper surface of the substrate 41 may include a solder resist 49 such that the ground plane 48 is exposed through the solder resist 49. The degree to which the ground plane 48 is exposed through

the solder resist 49 may depend in part on the type of conductive adhesive 47 and the size of the first layer 44 of the stiffener 43 (among other factors).

[0048] In some forms, additional organic and inorganic layers may be included as part of the solder resist 49. The type solder resist 49 that is included
5 in the electronic package 40 will depend in part on manufacturing considerations and the types of materials that are used for the conductive adhesive 47 and the package substrate 41 (among other factors).

[0049] In some forms, the first layer 44 may be bonded to the second layer 45 before (or after) the stiffener 43 is attached to substrate 41. As
10 examples, the first layer 44 may be bonded to the second layer 45 by laminating (e.g., rolling) the first layer 44 to the second layer 45 and/or plating the first layer 44 and the second layer 45 to the other of the first layer 44 and the second layer 45.

[0050] The stiffener 43 may be configured to oppose the bending
15 moment of the overall electronic package in order to improve the peak-to-valley warpage. The relative thickness, co-efficient of thermal expansion (CTE) and other material properties of the chosen materials for the stiffener 43 may be selected to provide the desired warpage properties, especially during SMT of thin dice. As an example, the CTE, thickness and other material properties of
20 the first material and the second material may be tailored to provide an opposing moment to the electronic package warpage, especially at high temperatures in order to improve overall peak-to-valley warpage.

[0051] WARPAGE EXAMPLE

[0052] Warpage modeling was conducted on a 20 X 20 mm coreless
25 substrate with a 270 μm thick 10 x 10 mm die. The thickness and width of the modeled stiffener was 200 μm and 2 mm respectively.

[0053] Figures 7A and 7B show the (a) room temperature and (b) high temperature warpage on a bimetallic stiffener system. The images have been exaggerated 30 times to highlight the warpage.

30 [0054] This overview is intended to provide non-limiting examples of the present subject matter—it is not intended to provide an exclusive or exhaustive explanation. The detailed description is included to provide further information about the electronic packages.

[0055] To better illustrate the electronic packages disclosed herein, a non-limiting list of examples is provided here:

[0056] Example 1 includes an electronic package. The electronic package includes a substrate and a die attached to the substrate. A stiffener
5 attached to the substrate adjacent to the die, wherein the stiffener is formed of a first layer made from one material and a second layer made from a different material.

[0057] Example 2 includes the electronic package of claim 1, wherein the stiffener surrounds the die.

10 [0058] Example 3 includes the electronic package of any one of claims 1-2, wherein the stiffener is secured to the substrate with a conductive adhesive, wherein the first layer of the stiffener engages the conductive adhesive and the first layer is formed of an electrically conductive material.

[0059] Example 4 includes the electronic package of any one of claims
15 1-3, wherein the first material has a first coefficient of thermal expansion (CTE) and the second material has a lower CTE than the first material, wherein the stiffener has a bending moment that is substantially opposite to a warpage of the electronic package when a temperature change is applied to the electronic package.

20 [0060] Example 5 includes the electronic package of any one of claims 1-4, wherein the stiffener has a substantially uniform cross-section.

[0061] Example 6 includes the electronic package of any one of claims 1-5, wherein the first layer is the same size as the second layer.

[0062] Example 7 includes the electronic package of any one of claims
25 1-6, wherein the first layer has a different thickness than the second layer.

[0063] Example 8 includes the electronic package of any one of claims 1-7, wherein the first layer is aluminum and the second layer is stainless steel.

[0064] Example 9 includes the electronic package of any one of claims
30 1-8, wherein the stiffener includes a third layer made from a different material than the first layer and the second layer.

[0065] Example 10 includes an electronic package. The electronic package includes a substrate and a die attached to the substrate. A stiffener is formed of a first layer made from a conductive material and a second layer made

from a different material, and a conductive adhesive that secures the substrate to the first layer of the stiffener.

[0066] Example 11 includes the electronic package of claim 10, wherein the stiffener surrounds the die.

5 [0067] Example 12 includes the electronic package of any one of claims 10-11, wherein the stiffener is concentric with the die.

[0068] Example 13 includes the electronic package of any one of claims 10-12, wherein the substrate includes a ground plane and the conductive adhesive electrically connects the first layer of the stiffener to the ground plane.

10 [0069] Example 14 includes the electronic package of any one of claims 10-13, wherein an upper surface of the substrate includes a solder resist and the ground plane is exposed through the solder resist.

[0070] Example 15 includes the electronic package of any one of claims 10-14, wherein the first layer is bonded to the second layer.

15 [0071] Example 16 includes the electronic package of any one of claims 10-15, wherein the stiffener has a substantially uniform cross-section, and wherein the first layer is the same size as the second layer.

[0072] Example 17 includes the electronic package of any one of claims 10-16, wherein the first layer is aluminum and the second layer is stainless steel.

20 [0073] Example 18 includes an electronic package. The electronic package includes a substrate and a die attached to the substrate. A stiffener attached to the substrate such that the stiffener surrounds the die, wherein the stiffener is formed of an aluminum layer and a second stainless steel layer made from a different material, wherein the stiffener has a substantially uniform cross-section, and wherein the aluminum layer is the same size as the stainless steel layer.

[0074] Example 19 includes the electronic package of claim 18, wherein the substrate includes a ground plane and a conductive adhesive that secures the aluminum layer of the stiffener to the ground plane such that the aluminum layer of the stiffener is electrically connected to the ground plane.

30 [0075] Example 20 includes the electronic package of any one of claims 18-19, wherein an upper surface of the substrate includes a solder resist and the ground plane is exposed through the solder resist.

[0076] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments in which the invention can be practiced. These embodiments are also referred to herein as “examples.” Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

[0077] In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of “at least one” or “one or more.” In this document, the term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In this document, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Also, in the following claims, the terms “including” and “comprising” are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

[0078] The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. Other embodiments can be used, such as by one of ordinary skill in the art upon reviewing the above description.

[0079] Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the

Detailed Description, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined with each other in various combinations or permutations. The scope of the invention should be determined with reference to the appended claims, along
5 with the full scope of equivalents to which such claims are entitled.

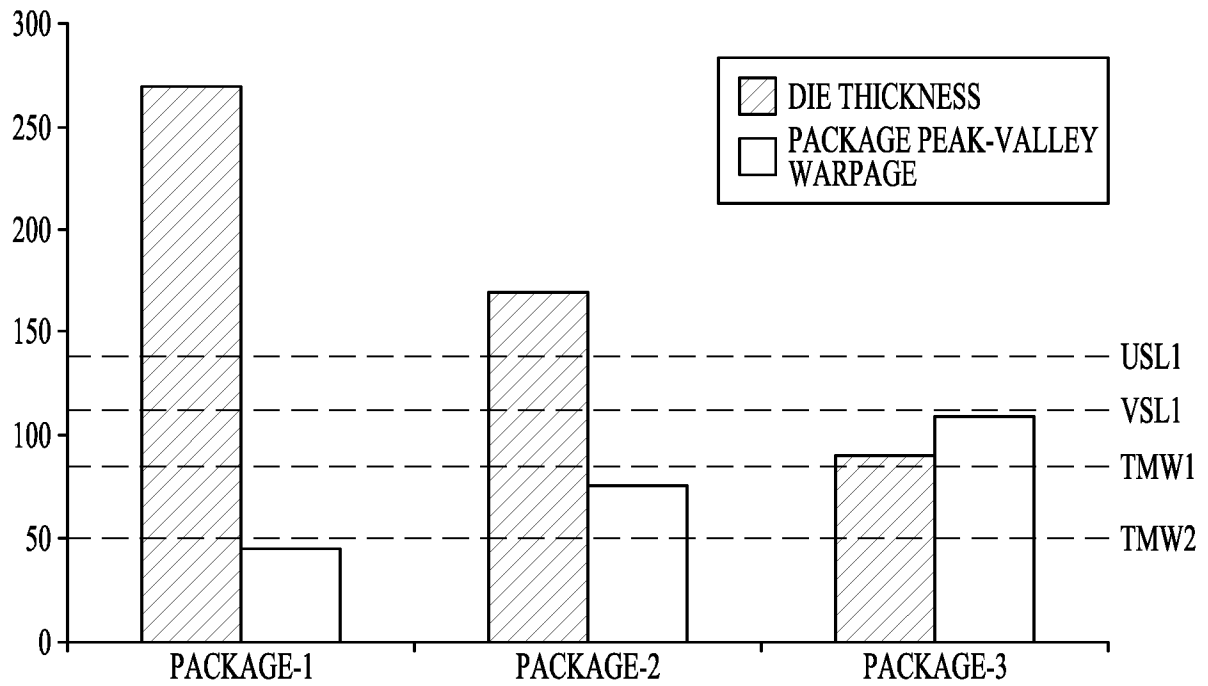
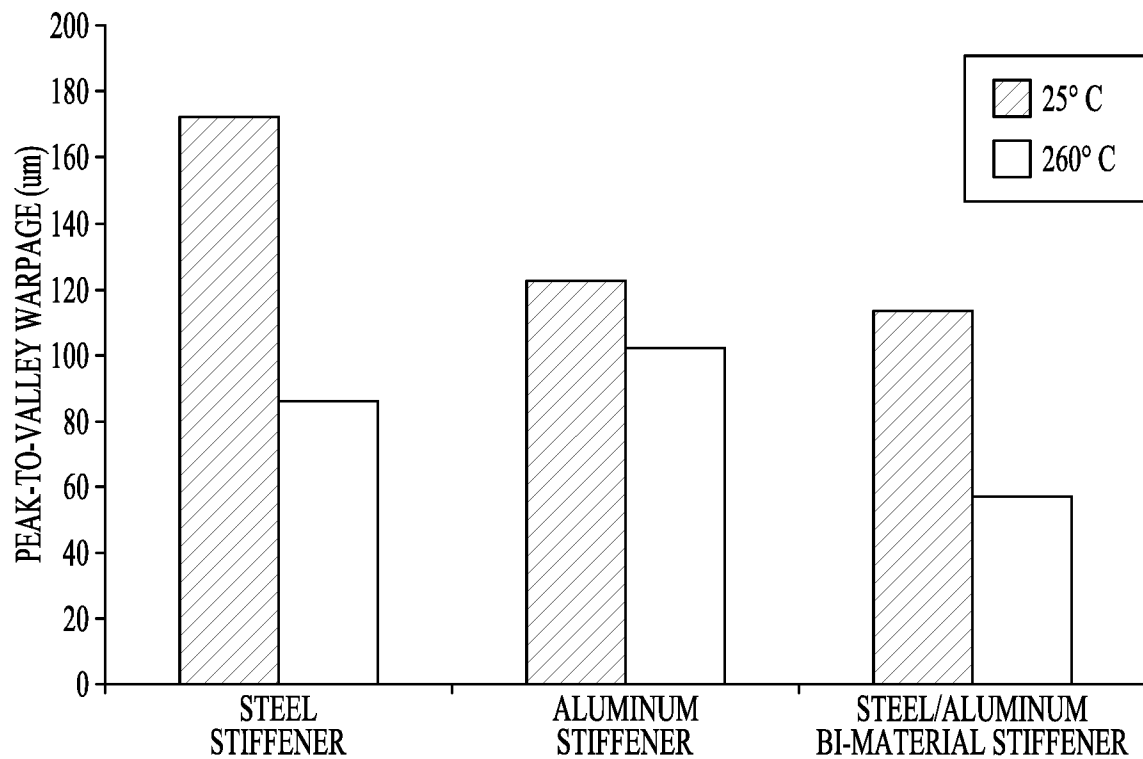
CLAIMS

1. An electronic package comprising:
a substrate;
5 a die attached to the substrate;
a stiffener attached to the substrate adjacent to the die, wherein the stiffener is formed of a first layer made from one material and a second layer made from a different material.
- 10 2. The electronic package of claim 1, wherein the stiffener surrounds the die.
3. The electronic package of claim 1, wherein the stiffener is secured to the substrate with a conductive adhesive, wherein the first layer of the stiffener
15 engages the conductive adhesive and the first layer is formed of an electrically conductive material.
4. The electronic package of claim 1, wherein the first material has a first coefficient of thermal expansion (CTE) and the second material has a lower CTE
20 than the first material, wherein the stiffener has a bending moment that is substantially opposite to a warpage of the electronic package when a temperature change is applied to the electronic package.
5. The electronic package of claim 1, wherein the stiffener has a
25 substantially uniform cross-section.
6. The electronic package of claim 1, wherein the first layer is the same size as the second layer.
- 30 7. The electronic package of claim 1, wherein the first layer has a different thickness than the second layer.
8. The electronic package of claim 1, wherein the first layer is aluminum and the second layer is stainless steel.

9. The electronic package of claim 1, wherein the stiffener includes a third layer made from a different material than the first layer and the second layer.
- 5 10. An electronic package comprising:
a substrate;
a die attached to the substrate;
a stiffener formed of a first layer made from a conductive material and a
second layer made from a different material; and
10 a conductive adhesive that secures the substrate to the first layer of the stiffener.
11. The electronic package of claim 10, wherein the stiffener surrounds the die.
- 15 12. The electronic package of claim 11, wherein the stiffener is concentric with the die.
13. The electronic package of claim 10, wherein the substrate includes a
20 ground plane and the conductive adhesive electrically connects the first layer of the stiffener to the ground plane.
14. The electronic package of claim 13, wherein an upper surface of the substrate includes a solder resist and the ground plane is exposed through the
25 solder resist.
15. The electronic package of claim 10, wherein the first layer is bonded to the second layer.
- 30 16. The electronic package of claim 10, wherein the stiffener has a substantially uniform cross-section, and wherein the first layer is the same size as the second layer.

17. The electronic package of claim 10, wherein the first layer is aluminum and the second layer is stainless steel.
18. An electronic package comprising:
- 5 a substrate;
a die attached to the substrate;
a stiffener attached to the substrate such that the stiffener surrounds the die, wherein the stiffener is formed of an aluminum layer and a second stainless steel layer made from a different material, wherein the stiffener has a
- 10 substantially uniform cross-section, and wherein the aluminum layer is the same size as the stainless steel layer.
19. The electronic package of claim 18, wherein the substrate includes a ground plane and a conductive adhesive that secures the aluminum layer of the
- 15 stiffener to the ground plane such that the aluminum layer of the stiffener is electrically connected to the ground plane.
20. The electronic package of claim 18, wherein an upper surface of the substrate includes a solder resist and the ground plane is exposed through the
- 20 solder resist.

1/4

**FIG. 1****FIG. 2**

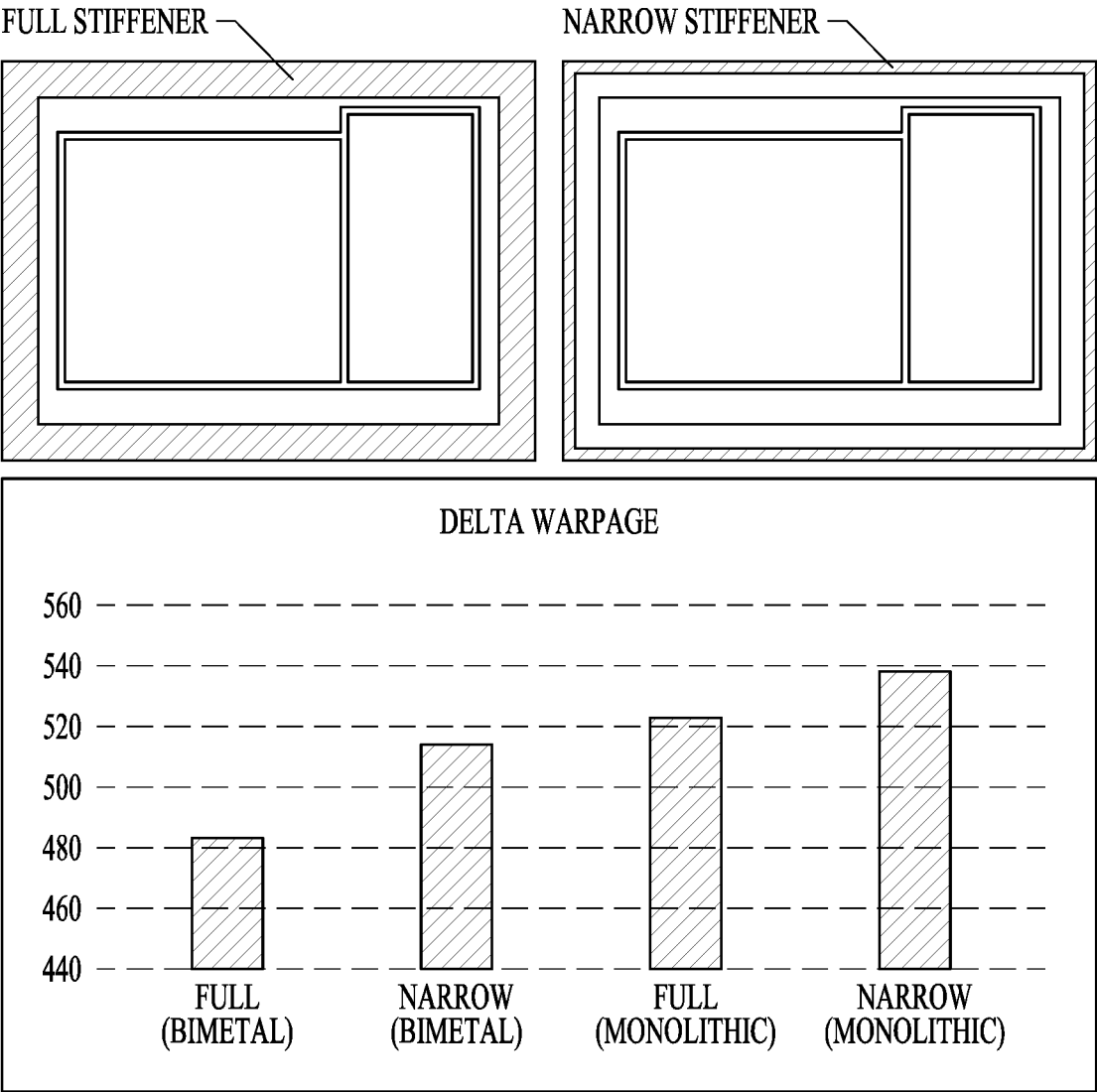


FIG. 3

3/4

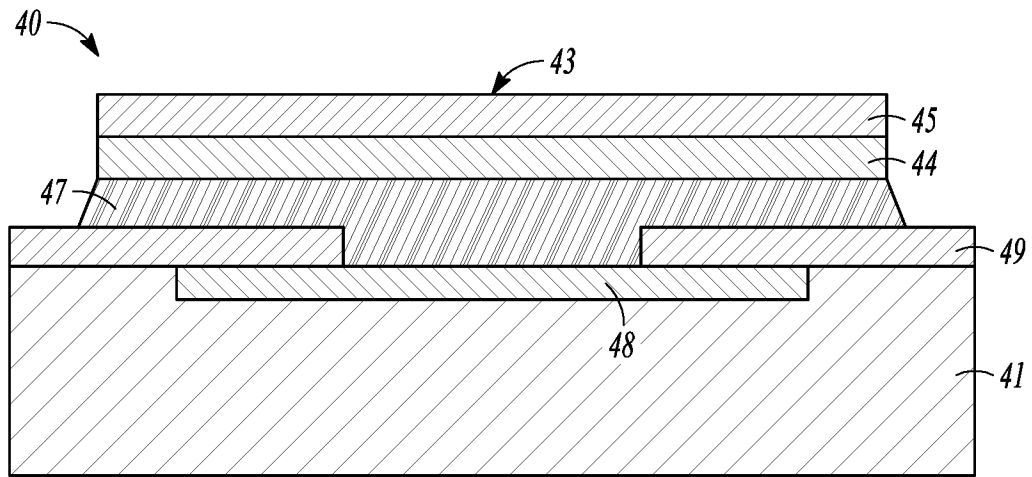


FIG. 4

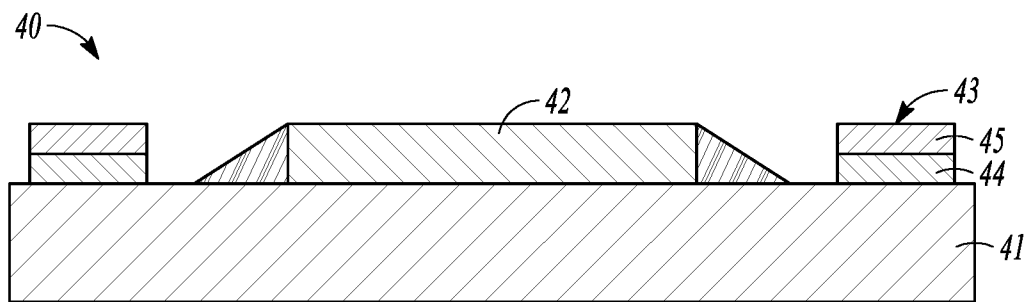


FIG. 5

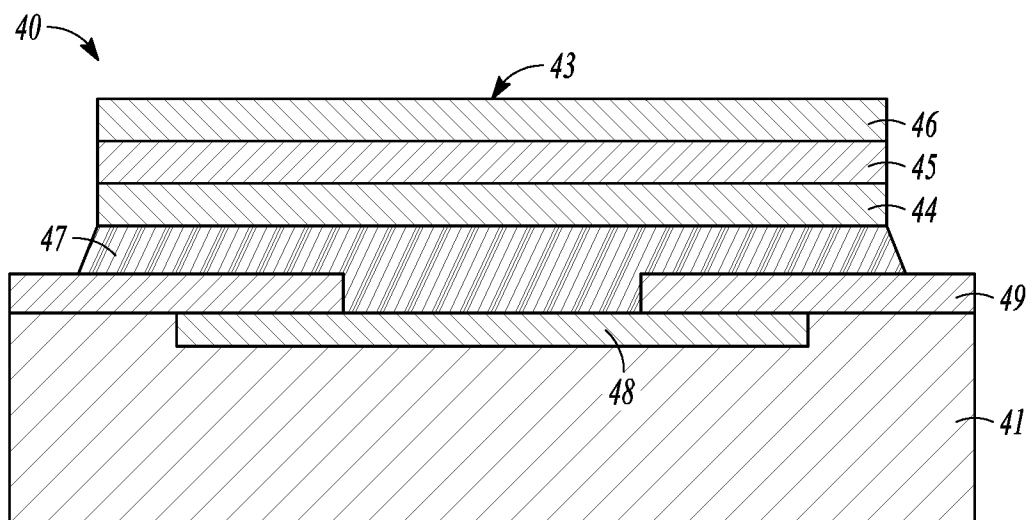


FIG. 6

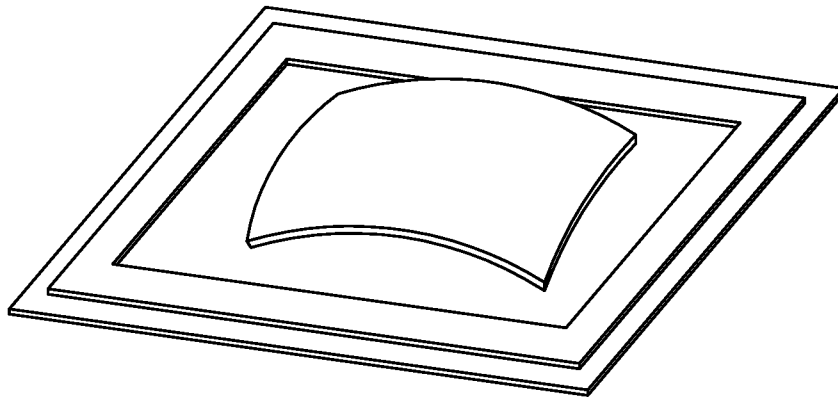


FIG. 7A

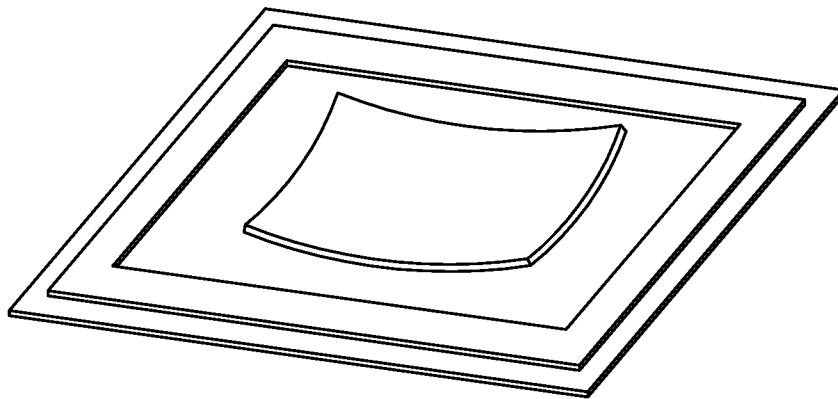


FIG. 7B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/017788**A. CLASSIFICATION OF SUBJECT MATTER****H01L 23/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/12; H01L 23/36; H01L 23/34; H01L 23/02; H01L 23/552; H01L 23/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: package, stiffener, material, aluminum

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0278647 A1 (YOSHIHIRO MORITA) 06 December 2007 See abstract, paragraphs [0025]-[0041] and figure 1.	1-2, 4-7
Y		3, 10-16
A		8-9, 17-20
Y	US 2009-0001528 A1 (HENNING BRAUNISCH et al.) 01 January 2009 See abstract, paragraphs [0008]-[0012] and figure 1.	3, 10-16
A	US 2005-0199998 A1 (CHIN-TE CHEN et al.) 15 September 2005 See abstract, paragraphs [0030]-[0032] and figures 3A-3F.	1-20
A	US 2005-0127502 A1 (DANIEL LEE et al.) 16 June 2005 See abstract, paragraphs [0008]-[0018] and figures 1-2.	1-20
A	US 2007-0145571 A1 (CHIEN-HSIUN LEE et al.) 28 June 2007 See abstract, paragraphs [0019]-[0024] and figures 3-5.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 May 2016 (30.05.2016)

Date of mailing of the international search report

30 May 2016 (30.05.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/017788

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0278647 A1	06/12/2007	CN 101124857 A CN 101124857 B JP 4500348 B2 US 7919856 B2 WO 2006-087769 A1	13/02/2008 16/11/2011 14/07/2010 05/04/2011 24/08/2006
US 2009-0001528 A1	01/01/2009	None	
US 2005-0199998 A1	15/09/2005	TW 200531232 A TW I247395 B	16/09/2005 11/01/2006
US 2005-0127502 A1	16/06/2005	US 7026711 B2	11/04/2006
US 2007-0145571 A1	28/06/2007	TW I331383 B US 8174114 B2	01/10/2010 08/05/2012