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(54) Title: HEADSET SWITCHES WITH CROSSTALK REDUCTION

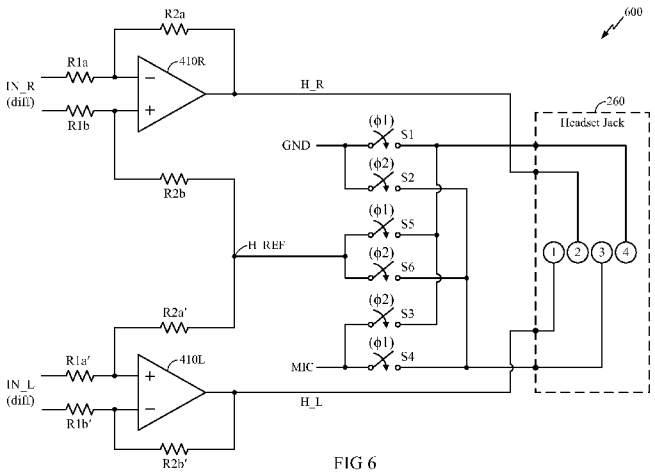

FIG 6

(57) Abstract: Techniques for utilizing a plurality of switches to reduce crosstalk in a headset jack for accommodating both European and North American type headset plugs. In an aspect, a six-switch solution is provided to selectively couple first and second terminals of the jack to a ground and a microphone terminal, and further to selectively couple a ground sensing input to the first or second terminal of the jack. The ground sensing input is provided to left and right audio channel amplifiers for driving the corresponding left and right terminals of the headset, to provide a common-mode reference level to the left and right audio channel amplifiers. In another aspect, at least four physical pins are provided to couple the switches to the ground and microphone terminals of the jack, and the connections between the ground sensing inputs and the jack may be provided adjacent to the jack for better isolation.

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HEADSET SWITCHES WITH CROSSTALK REDUCTION

RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Pat. App. No. 61/621,266, entitled "Low Crosstalk Headset Jack Microphone and Ground Line Switch," filed April 6, 2012, the contents of which are hereby incorporated by reference in their entirety.

BACKGROUND

Field

[0002] The disclosure relates to media devices, and, in particular, to techniques for reducing crosstalk caused by microphone and ground switches in an audio headset.

Background

[0003] Audio and other media devices often include a jack for receiving a media plug coupled to a peripheral device. For example, a mobile phone may include a jack for receiving a plug coupled to an audio headset with microphone, which allows a user to carry on a voice conversation over the mobile phone using the headset. Other example media devices include MP3 players, handheld gaming devices, tablets, personal computers, notebook computers, personal digital assistants, etc., while other peripheral devices include headphones, hearing-aid devices, personal computer speakers, home entertainment stereo speakers, etc.

[0004] A media device may be configured to accommodate different types of plugs, for example, a European type or a North American type. Depending on the detected plug type, a plurality of switches in the media device may be selectively enabled or disabled to couple terminals of the plug to the appropriate processing nodes in the media device. In particular implementations, certain of the switches designed to couple a plug terminal to a ground voltage may introduce significant on-resistance between the plug terminal and ground, which may undesirably lead to crosstalk between the left and right audio channels of the headphone. To reduce such crosstalk, the switches may be made larger in size. However, such a solution would undesirably consume chip and/or board area.

[0005] It would be desirable to provide simple and efficient techniques to reduce crosstalk in headset channels arising from switches for accommodating multiple media plug types.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG 1 illustrates a block diagram of a design of a wireless communication device in which the techniques of the present disclosure may be implemented.

[0007] FIG 2 illustrates an exemplary scenario wherein the techniques of the present disclosure may be applied.

[0008] FIG 3 illustrates the sequence of terminals on a plug that may generally be provided according to either a European or a North American type plug layout.

[0009] FIG 4 illustrates a prior art implementation of an electrical system, e.g., provided on a media device, for driving jack terminals 1 through 4, wherein a plurality of switches are provided to accommodate both North American and European type plugs.

[0010] FIG 5 illustrates equivalent circuits of the Φ1 and Φ2 configurations of the switches.

[0011] FIG 6 illustrates an exemplary embodiment of the present disclosure, wherein a six-switch solution is provided to reduce crosstalk in an audio system.

[0012] FIG 7 illustrates electrical connections of the system 500 according to both the Φ1 and Φ2 configurations of the switches.

[0013] FIG 8 illustrates an exemplary embodiment of the present disclosure, wherein the six switches S1-S6 are provided in discrete form.

[0014] FIG 9 illustrates an alternative exemplary embodiment of the present disclosure, wherein the six switches S1-S6 are provided on a single integrated circuit, on which the audio amplifiers are also provided.

[0015] FIG 10 illustrates an exemplary embodiment according to the present disclosure for supporting both an FM antenna and North American / European-type headset compatibility.

[0016] FIG 11 illustrates an alternative exemplary embodiment for supporting an FM antenna with North American / European-type headset compatibility, wherein the plurality of switches S1-S6 is integrated on a single chip with the codec.

[0017] FIG 12 illustrates an exemplary embodiment of a method according to the present disclosure.

DETAILED DESCRIPTION

[0018] Various aspects of the disclosure are described more fully hereinafter with reference to the accompanying drawings. This disclosure may, however, be embodied in many different forms and should not be construed as limited to any specific structure or function presented throughout this disclosure. Rather, these aspects are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art. Based on the teachings herein one skilled in the art should appreciate that the scope of the disclosure is intended to cover any aspect of the disclosure disclosed herein, whether implemented independently of or combined with any other aspect of the disclosure. For example, an apparatus may be implemented or a method may be practiced using any number of the aspects set forth herein. In addition, the scope of the disclosure is intended to cover such an apparatus or method which is practiced using other structure, functionality, or structure and functionality in addition to or other than the various aspects of the disclosure set forth herein. It should be understood that any aspect of the disclosure disclosed herein may be embodied by one or more elements of a claim.

[0019] The detailed description set forth below in connection with the appended drawings is intended as a description of exemplary aspects of the invention and is not intended to represent the only exemplary aspects in which the invention can be practiced. The term "exemplary" used throughout this description means "serving as an example, instance, or illustration," and should not necessarily be construed as preferred or advantageous over other exemplary aspects. The detailed description includes specific details for the purpose of providing a thorough understanding of the exemplary aspects of the invention. It will be apparent to those skilled in the art that the exemplary aspects of the invention may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the novelty of the exemplary aspects presented herein.

[0020] FIG 1 illustrates a block diagram of a design of a wireless communication device 100 in which the techniques of the present disclosure may be implemented. FIG 1 shows an example transceiver design. In general, the conditioning of the signals in a transmitter and a receiver may be performed by one or more stages of amplifier, filter, upconverter, downconverter, etc. These circuit blocks may be arranged differently from the configuration shown in FIG 1. Furthermore, other circuit blocks not shown in FIG 1

may also be used to condition the signals in the transmitter and receiver. Some circuit blocks in FIG 1 may also be omitted.

[0021] In the design shown in FIG 1, wireless device 100 includes a transceiver 120 and a data processor 110. The data processor 110 may include a memory (not shown) to store data and program codes. Transceiver 120 includes a transmitter 130 and a receiver 150 that support bi-directional communication. In general, wireless device 100 may include any number of transmitters and any number of receivers for any number of communication systems and frequency bands. All or a portion of transceiver 120 may be implemented on one or more analog integrated circuits (ICs), RF ICs (RFICs), mixed-signal ICs, etc.

[0022] A transmitter or a receiver may be implemented with a super-heterodyne architecture or a direct-conversion architecture. In the super-heterodyne architecture, a signal is frequency converted between radio frequency (RF) and baseband in multiple stages, e.g., from RF to an intermediate frequency (IF) in one stage, and then from IF to baseband in another stage for a receiver. In the direct-conversion architecture, a signal is frequency converted between RF and baseband in one stage. The super-heterodyne and direct-conversion architectures may use different circuit blocks and/or have different requirements. In the design shown in FIG 1, transmitter 130 and receiver 150 are implemented with the direct-conversion architecture.

[0023] In the transmit path, data processor 110 processes data to be transmitted and provides I and Q analog output signals to transmitter 130. In the exemplary embodiment shown, the data processor 110 includes digital-to-analog-converters (DAC's) 114a and 114b for converting digital signals generated by the data processor 110 into the I and Q analog output signals, e.g., I and Q output currents, for further processing.

[0024] Within transmitter 130, lowpass filters 132a and 132b filter the I and Q analog output signals, respectively, to remove undesired images caused by the prior digital-to-analog conversion. Amplifiers (Amp) 134a and 134b amplify the signals from lowpass filters 132a and 132b, respectively, and provide I and Q baseband signals. An upconverter 140 upconverts the I and Q baseband signals with I and Q transmit (TX) local oscillating (LO) signals from a TX LO signal generator 190 and provides an upconverted signal. A filter 142 filters the upconverted signal to remove undesired images caused by the frequency upconversion as well as noise in a receive frequency band. A power amplifier (PA) 144 amplifies the signal from filter 142 to obtain the

desired output power level and provides a transmit RF signal. The transmit RF signal is routed through a duplexer or switch 146 and transmitted via an antenna 148.

[0025] In the receive path, antenna 148 receives signals transmitted by base stations and provides a received RF signal, which is routed through duplexer or switch 146 and provided to a low noise amplifier (LNA) 152. The received RF signal is amplified by LNA 152 and filtered by a filter 154 to obtain a desirable RF input signal. A downconverter 160 downconverts the RF input signal with I and Q receive (RX) LO signals from an RX LO signal generator 180 and provides I and Q baseband signals. The I and Q baseband signals are amplified by amplifiers 162a and 162b and further filtered by lowpass filters 164a and 164b to obtain I and Q analog input signals, which are provided to data processor 110. In the exemplary embodiment shown, the data processor 110 includes analog-to-digital-converters (ADC's) 116a and 116b for converting the analog input signals into digital signals to be further processed by the data processor 110.

[0026] TX LO signal generator 190 generates the I and Q TX LO signals used for frequency upconversion. RX LO signal generator 180 generates the I and Q RX LO signals used for frequency downconversion. Each LO signal is a periodic signal with a particular fundamental frequency. A PLL 192 receives timing information from data processor 110 and generates a control signal used to adjust the frequency and/or phase of the TX LO signals from LO signal generator 190. Similarly, a PLL 182 receives timing information from data processor 110 and generates a control signal used to adjust the frequency and/or phase of the RX LO signals from LO signal generator 180.

[0027] The data processor 110 further includes a baseband processing module 101 configured to process RX data from the ADC's 116a, 116b, and further to process TX data to the DAC's 114a, 114b. The baseband processing module 101 is further coupled to an audio codec 102. The module 101 may transmit digital signals to the audio codec 102 for output as an analog audio signal, and may further receive digital signals from the audio codec 102 corresponding to audio input signals. The audio codec 102 may further interface with audio signals to and from a headset (not shown in FIG 1). In an exemplary embodiment, the techniques of the present disclosure may be implemented, e.g., using switches integrated on the data processor 110 with the audio codec 102, or using switches that are external to the data processor 110.

[0028] FIG 2 illustrates an exemplary scenario 200 wherein the techniques of the present disclosure may be applied. It will be appreciated that FIG 2 is shown for

illustrative purposes only, and is not meant to limit the scope of the present disclosure to the particular system shown. For example, it will be appreciated that the techniques disclosed herein may also be readily applied to audio devices other than that shown in FIG 2. Furthermore, the techniques may also be readily adapted to other types of multi-media devices, as well as to non-audio media devices, e.g., to reduce crosstalk in plugs supporting video, etc. Such alternative exemplary embodiments are contemplated to be within the scope of the present disclosure.

[0029] In FIG 2, a headset 210 includes a left (L) headphone 215, a right (R) headphone 220, and a microphone 230. These components of the headset 210 are electrically coupled to terminals of a plug 250 via conducting wires 245. The plug 250 is insertable into a jack 260 of a media device 240. Note the jack 260 need not extrude from the surface of the device 240 as suggested by FIG 2, and furthermore, the sizes of the elements shown in FIG 2 are not necessarily drawn to scale. The device 240 may be a mobile phone incorporating the circuitry shown in FIG 1. The device 240 may also be, e.g., an MP3 player, home stereo system, etc. Audio and/or other signals may be exchanged between the device 240 and the headset 210 through the plug 250 and jack 260. The plug 250 receives the audio signals from the jack 260, and routes the signals to the L and R headphones of the headset 210. The plug 250 may further couple an electrical signal with audio content generated by the microphone 230 to the jack 260, and the microphone signal may be further processed by the device 240. Note the plug 250 may include further terminals not shown, e.g., for communicating other types of signals such as control signals, video signals, etc.

[0030] The sequence of terminals on plug 250 may generally be provided according to one of several types of common standardized layouts, as shown in FIG 3. For example, according to a European type plug layout 300a, the terminals may be ordered as left audio (L), right audio (R), microphone (M), and ground (G), as enumerated from the tip of the plug to the base of the plug. On the other hand, according to a North American type plug layout 300b, the terminals may be ordered as left audio (L), right audio (R), ground (G), and microphone (M). Upon insertion into a jack, the terminals of both types of plugs may be electrically coupled to corresponding jack terminals 1, 2, 3, and 4, respectively, from tip to base, as indicated by the circled numerals in FIG 3.

[0031] To accommodate both North American and European plug types using a single jack, a device 240 may generally incorporate switching circuitry to electrically route the plug terminals to the appropriate jack terminals, depending on the type of plug inserted.

For example, a plurality of switches may be provided at the device 240 to electrically couple terminals (M) and (G) of a European type plug to terminals 3 and 4 of a jack, respectively, or alternatively, to couple terminals (G) and (M) of a North American type plug to terminals 3 and 4 of a jack, respectively. In an implementation, the device 240 may include a codec chip (not shown) on which the drivers (e.g., amplifiers) for the left (L) and right (R) audio channels may be provided, and the switching circuitry may be integrated with the codec chip, or they may be external to the codec chip.

[0032] Note the designation of certain jack terminals in FIG 3 as terminals 1, 2, 3, and 4 is for illustrative purposes only. It will be appreciated that alternative denotations of the jack terminals may readily be employed. Further note that, in this specification and the claims, the term "a first terminal" of a jack may denote, e.g., any of jack terminals 1, 2, 3, and 4 shown in FIG 3, while the term "a second terminal" of a jack may denote, e.g., any of jack terminals 1, 2, 3, and 4 distinct from the "first terminal." In general, unless otherwise noted, the use of the terms "first," "second," etc., herein is for identification purposes only, and need not imply that, e.g., a "first" element necessarily precedes a "second" element in sequence.

[0033] FIG 4 illustrates a prior art implementation of an electrical system 400, e.g., provided on a device 240, for driving jack terminals 1 through 4, wherein a plurality of switches are provided to accommodate both North American and European type plugs. In FIG 4, an amplifier 410R is configured with resistors R1a, R1b, R2a, R2b for generating a right headphone signal (H_R) for driving terminal 2 of the jack. It will be appreciated from the circuit topology shown that the H_R signal will correspond to an amplified version of a differential (diff) right-channel input signal IN_R. FIG 4 further illustrates an amplifier 410L configured with resistors R1a', R1b', R2a', R2b' for generating a left headphone signal (H_L) for driving terminal 1 of the jack. The H_L signal will also correspond to an amplified version of a differential (diff) left-channel input signal IN_L. Note the configuration of resistors in FIG 4 is shown for illustrative purposes only, and it is contemplated that alternative exemplary embodiments may incorporate other amplifier configurations for driving the left and right audio channels, e.g., amplifiers having different types of feedback or passive elements than shown in FIG 4.

[0034] In the implementation shown, resistors R2b and R2a' are coupled at a single node labeled H_REF, which is in turn coupled to the ground (GND) voltage. H_REF may also be denoted the "reference terminal" or "ground sensing input" or "ground

sensing terminal." It will be appreciated that H_REF may be understood to provide a common-mode reference to the differential amplifiers 410R and 410L. For example, to reduce common-mode ground noise that may be present at the jack ground terminal and at the board level, H_REF may be connected directly to the jack ground terminal to remove the ground noise.

[0035] In FIG 4, a plurality of switches S1, S2, S3, and S4 is further provided to alternately couple the ground (GND) and microphone (MIC) nodes of the system 400 to the appropriate terminals of the jack 260, depending on the inserted plug type. In particular, if an inserted plug type is European, then switches S1 and S4 will be closed (according to a Φ1 configuration of the switches), and switches S2 and S3 will be open. Alternatively, if the inserted plug type is North American, then switches S2 and S3 will be closed (according to a Φ2 configuration of the switches), and switches S1 and S4 will be open. In this manner, the GND and MIC nodes of the system 400 may be appropriately routed to the terminals of the jack 260 through the action of the switches S1-S4.

[0036] One disadvantage of the system 400 is that a certain degree of crosstalk may be present between the right and left audio channels H_R and H_L, due to finite on-resistance of either of the ground switches S1 or S2. In particular, as shown in FIG 5, according to either the Φ1 of Φ2 configuration of switches, there will be a resistance RG between the jack terminal and the system ground voltage, and a resistance RM between the jack terminal and the microphone node, wherein RG corresponds to the on-resistance of either switch S1 or S2, while RM corresponds to the on-resistance of either switch S3 or S4. As the H_R and H_L headset channels share a common path to ground (GND), the ground switch on-resistance RG will generate a crosstalk component between the right and left headphone channels. In particular, a component in the left audio signal H_L will be present in the right audio signal H_R, and vice versa, due to the varying voltage across the common ground switch resistance RG. For example, a 16-Ohm switch resistance can create approximately -60 dB of crosstalk when coupled with a 16-milliOhm headset. Such crosstalk undesirably degrades the signal fidelity of the left and right audio channels.

[0037] Note the amount of crosstalk in the system may be quantified as follows (Equation 1):

$$\text{Crosstalk} = \frac{RG}{RL+2\times RG};$$

wherein RL represents the resistance corresponding to the left or right audio load. Per Equation 1, the larger the ground switch resistance RG, the larger the crosstalk component will be. Thus to reduce this crosstalk component, the switches S1 and S2 may be made larger in size to reduce their turn-on resistance. However, this may undesirably consume a great deal of silicon chip area, and is not an ideal solution for integrated systems, wherein chip area is at a premium. It would thus be desirable to provide simple and efficient techniques to reduce the amount of crosstalk in an audio system.

[0038] FIG 6 illustrates an exemplary embodiment of the present disclosure, wherein a six-switch solution is provided to reduce the aforementioned crosstalk. Note certain aspects of FIG 6 are shown for illustrative purposes only, and are not meant to limit the scope of the present disclosure to the specific embodiment shown. Furthermore, certain elements may be similarly labeled in FIGs 4 and 6, and such elements may be understood as performing similar functionality, unless otherwise noted.

[0039] In FIG 6, switches S5 and S6 are provided in the audio system, in addition to the switches S1-S4. S5 and S6 are configured to always couple the ground sensing input H_REF to the ground terminal of the jack 260, regardless of whether the plug type is North American or European. In this manner, any voltage drops caused by RG may be sampled by H_REF and fed back to the audio amplifiers as common-mode ground noise. In particular, per the Φ1 configuration, corresponding to the inserted plug type being European, S5 couples H_REF to terminal 4 of the jack 260. Alternatively, per the Φ2 configuration, corresponding to the inserted plug type being North American, S6 couples H_REF to terminal 3 of the jack 260.

[0040] FIG 7 illustrates electrical connections of the system 600 according to both the Φ1 and Φ2 configurations of the switches. In particular, as shown in FIG 7, according to either the Φ1 or Φ2 configuration, the reference node H_REF is configured to sample the voltage across RG via a resistance RF, which may correspond to the on-resistance of the switch S5 or S6. As the voltage across RG is fed back to the amplifiers 410R and 410L as common-mode ground noise, it is expected that the crosstalk will be significantly reduced in the system 600 compared to the system 400.

[0041] In particular, the amount of crosstalk in the system 600 may be quantified as follows (Equation 2):

$$\text{Crosstalk} = \frac{R1 \times RF}{2 \times R2 \times (R1 + R2 + 2 \times RF)};$$

wherein it is assumed that R1 = R1a = R1a', and R2 = R2a = R2a'. In an exemplary embodiment, RF may be on the order of a few Ohms, while the resistors R1a, R2a, R1b, R2b, R1a', R2a', R1b', R2b' may all be on the order of kiloOhms. Therefore, any crosstalk contributed by RF is not expected to be significant. Furthermore, in an exemplary embodiment, any crosstalk contributed by RF can be further reduced by using integrated circuit layout techniques to match the resistances in the amplifier (410R and 410L) feedback paths to each other.

[0042] FIG 8 illustrates an exemplary embodiment of the present disclosure, wherein the six switches S1-S6 are provided in discrete form, i.e., separately from an integrated circuit housing the right channel amplifier 8200 and left channel amplifier 8300. In FIG 8, each of the switches S1-S6 is associated with two corresponding pins, corresponding to the switch terminals. For example, S1 has two pins S1.1, S1.2, while S2 has two pins S2.1, S2.2, etc. The pins may correspond to, e.g., physical pins of a discrete integrated circuit housing the corresponding switch or switches. In certain exemplary embodiments, all six of the switches S1-S6 may be provided on a single discrete integrated circuit, with twelve physical pins provided for interfacing the switches with other board-level elements. In alternative exemplary embodiments, any subset of the switches S1-S6 may be provided on single discrete integrated circuits, with a total of twelve physical pins provided across all the discrete integrated circuits housing the switches.

[0043] In FIG 8, the headset jack 260 is further shown with four physical terminals 260.1, 260.2, 260.3, and 260.4, which are electrically coupled to the corresponding terminals 1, 2, 3, and 4 of the jack 260, as earlier described hereinabove. It will be appreciated that the pins S1.2, S2.2, S3.2, S4.2, S5.2, and S6.2, representing the outputs of the switches S1-S6, may be routed to corresponding physical terminals 260.1, 260.2, 260.3, 260.4 using board trace routing 801, i.e., conductive electrical leads that are provided on a physical board on which the switches S1-S6, the jack 260, as well as an integrated circuit housing amplifiers 8200, 8300 may be provided.

[0044] In particular, note that S1.2 and S3.2 are electrically coupled, and similarly, S2.2 and S4.2 are electrically coupled. Furthermore, the output of pin S5.2 is electrically coupled to physical terminal 260.4 of the jack 260. In an exemplary embodiment, the electrical connection between S5.2 and 160.4 may be provided as close to 260.4 as possible, i.e., in close physical proximity to the jack 160. Similarly, the output of pin

S6.2 is electrically coupled to physical terminal 260.3 of the jack 260, and the electrical connection between S6.2 and 260.3 may be provided as close to 260.3 as possible.

[0045] It will be appreciated that, in this manner, the electrical connection between pin S5.2 and terminal 260.4 is effectively independent of the electrical connection between pins S1.2, S3.2 and terminal 260.4, since the two electrical connections are routed over separate conductive paths on the board. In particular, during Φ1, the parasitic routing resistance between S1.2, S3.2 and jack terminal 260.4 can be modeled as being part of the ground resistance RG, and the parasitic routing resistance between S5.2 and 260.4 can be modeled as being part of the ground sensing path resistance RF. Similarly, the electrical connection between pin S6.2 and terminal 260.3 is effectively independent of the electrical connection between pins S2.2, S4.2 and terminal 260.3. In particular, during Φ2, the parasitic routing resistance between S2.2, S4.2 and jack terminal 260.3 can be modeled as being part of the ground resistance RG, and the parasitic routing resistance between S6.2 and 260.3 can be modeled as being part of the ground sensing path resistance RF.

[0046] It will be appreciated that maintaining such independence between the ground path and the H-REF path to the jack advantageously separates any parasitic resistances due to implementing the conductive paths as physical board traces, and thus further improves the crosstalk reduction features described herein.

[0047] FIG 9 illustrates an alternative exemplary embodiment of the present disclosure, wherein the six switches S1-S6 are provided on a single integrated circuit, on which the audio amplifiers are also provided. In FIG 9, an integrated circuit 910 includes all of switches S1-S6, as well as amplifiers 410R, 410L, and associated resistances. In an exemplary embodiment, it will be appreciated that the integrated circuit 910 may include further features, e.g., audio codec functionality and other control functionality.

[0048] In FIG 9, the integrated circuit 910 includes six physical (package) pins 910.1, 910.2, 910.3, 910.4, 910.5, and 910.6 for interfacing with other board-level components. For example, these pins may be routed to physical terminals 260.1, 260.2, 260.3, 260.4 of the jack 260 using board trace routing 901. Pins 910.1 and 910.6 are used for delivery of the audio signals H_R and H_L, respectively, to physical terminals 260.2, 260.1 of the jack 260. Pins 910.2, 910.3, 910.4, 910.5 are coupled to terminals 260.4 and 260.3.

[0049] As noted hereinabove with reference to FIG 8, in an exemplary embodiment, the electrical connection between 910.3 and 260.4 may be provided as close to 260.4 as

possible, i.e., in close physical proximity to the jack 260. Similarly, the output of pin 910.4 is electrically coupled to physical terminal 260.3 of the jack 260, and the electrical connection between 910.4 and 260.3 may be provided as close to 260.3 as possible. In this manner, the aforementioned independence between the ground path and the H-REF path to the jack is advantageously maintained in the case where the switches are integrated with the codec.

[0050] FIG 10 illustrates an exemplary embodiment according to the present disclosure for supporting both an FM antenna and North American / European-type headset compatibility. Per either the Φ1 or Φ2 configuration, GND and MIC are selectively coupled to terminals 4 and 3 of the jack via ferrite beads 702, 704 and filtering capacitors 712, 714, as shown in FIG 7. In FIG 10, H_REF is further shown selectively coupled to either terminal 4 or 3 via ferrite bead 706 or 708, and filtering capacitor 716 or 718. In an exemplary embodiment, the values of the ferrite beads and filtering capacitors may be chosen to isolate GND, MIC, and H_REF from other portions of the circuitry at certain frequencies, e.g., to isolate such nodes from an FM antenna / receiver module 790 as further described hereinbelow.

[0051] In particular, the FM module 790 includes capacitors (Csmall) 792, 794 coupling nodes 3 and 4 of the jack to an inductor (Ltune) 796, a capacitor (Cmatch) 798, and another inductor (Lmatch) 799 as shown. Lmatch 799 may be coupled to FM receive processing circuitry (not shown in FIG 10) to, e.g., process an FM radio signal as received over the air via the conducting wires 245 of the headset 210. It will be appreciated that in this case, the conducting wires 245 (in particular, the wires of the headset making electrical contact with terminals 3 and 4 of the jack) may act as antenna elements to receive over-the-air FM signals. As the frequency range of such FM signals is different from the frequency range of the audio signals H_R, H_L, and MIC, the FM signals will be effectively frequency multiplexed with the audio signals over the conducting wires 245.

[0052] In the manner shown in FIG 10, the six-switch crosstalk reduction techniques of the present disclosure may advantageously be combined with techniques to receive an FM signal using the wires 245 of the headset. In particular, the ferrite beads and capacitors may be provided as filtering elements to protect the codec chip (e.g., the circuitry for processing H_R, H_L, H_REF, and MIC) from, e.g., RF inter-modulation. The filtering elements may further protect the FM processing circuitry 791 from RF spurs arising from the codec chip. It will be appreciated that one of ordinary skill in the

art may readily modify the configuration shown in FIG 10 to, e.g., add or remove filtering elements to design a filter having different characteristics, and such alternative exemplary embodiments are contemplated to be within the scope of the present disclosure.

[0053] In an exemplary embodiment, all the switches S1-S6 shown in FIG 10, along with the passive components including inductors and capacitors, may be provided externally to the codec integrated circuit. Furthermore, in alternative exemplary embodiments, the two ferrite beads 702, 704 and filtering capacitors 712, 714 may be removed to reduce the external component count, at the cost of potentially degraded crosstalk performance.

[0054] FIG 11 illustrates an alternative exemplary embodiment, wherein the plurality of switches S1-S6 is integrated on a single chip with the codec. In FIG 11, elements enclosed by the edges of the dashed box 8100 may correspond to elements found on the codec integrated circuit, while other elements not enclosed by 8100 may be provided externally to the integrated circuit. In FIG 11, a plurality of pins 822, 824 is provided to couple the outputs of switches S5 and S6 from the integrated circuit to the corresponding passive elements and terminals of the jack, independently of the pins 826, 828 dedicated to the other switches S1 through S4. It will be appreciated that by providing the pins 826, 828 separately from pins 822, 824, the H_REF node will not share the same off-chip routing path with the codec system ground node, thereby advantageously reducing any further crosstalk associated with having these nodes share the same off-chip routing path. It will be appreciated that the parasitic resistance from any external inductor (or beads) can be treated as part of the RG and RF in the equivalent circuit, and thus Equation (2) also applies in this case.

[0055] As described earlier hereinabove with reference to FIG 10, the ferrite beads 802, 804 and filtering capacitors 812, 814 may also be made optional in certain exemplary embodiments.

[0056] FIG 12 illustrates an exemplary embodiment of a method according to the present disclosure. Note FIG 12 is described for illustrative purposes only, and is not meant to limit the scope of the present disclosure to any particular method described herein.

[0057] In FIG 12, at block 1210, a first terminal of a jack is selectively coupled to a ground connection using a first ground switch.

[0058] At block 1220, a second terminal of the jack is selectively coupled to the ground connection using the second ground switch.

[0059] At block 1230, the first terminal of the jack is selectively coupled to a microphone node using a first microphone switch.

[0060] At block 1240, the second terminal of the jack is selectively coupled to the microphone node using a second microphone switch.

[0061] At block 1250, the first terminal of the jack is selectively coupled to a ground sensing input using a first ground sensing switch.

[0062] At block 1260, the second terminal of the jack is selectively coupled to the ground sensing input using a second ground sensing switch. In an exemplary embodiment, the switches are selectively coupled depending on whether the jack is detected to be of a North American or a European type.

[0063] In this specification and in the claims, it will be understood that when an element is referred to as being "connected to" or "coupled to" another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected to" or "directly coupled to" another element, there are no intervening elements present. Furthermore, when an element is referred to as being "electrically coupled" to another element, it denotes that a path of low resistance, or an electrical short circuit, is present between such elements, while when an element is referred to as being simply "coupled" to another element, there may or may not be a path of low resistance between such elements.

[0064] Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0065] Those of skill in the art would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the exemplary aspects disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether

such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the exemplary aspects of the invention.

[0066] The various illustrative logical blocks, modules, and circuits described in connection with the exemplary aspects disclosed herein may be implemented or performed with a general purpose processor, a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0067] The steps of a method or algorithm described in connection with the exemplary aspects disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

[0068] In one or more exemplary aspects, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that

facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-Ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0069] The previous description of the disclosed exemplary aspects is provided to enable any person skilled in the art to make or use the invention. Various modifications to these exemplary aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other exemplary aspects without departing from the spirit or scope of the invention. Thus, the present disclosure is not intended to be limited to the exemplary aspects shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

1. An apparatus comprising:

a first ground switch configured to selectively couple a first terminal of a jack to a ground connection;

a second ground switch configured to selectively couple a second terminal of the jack to the ground connection;

a first microphone switch configured to selectively couple the first terminal of the jack to a microphone node;

a second microphone switch configured to selectively couple the second terminal of the jack to the microphone node;

a first ground sensing switch configured to selectively couple the first terminal of the jack to a ground sensing input; and

a second ground sensing switch configured to selectively couple the second terminal of the jack to the ground sensing input; wherein the switches are configured depending on whether the jack is detected to be of a North American or a European type.

2. The apparatus of claim 1, wherein the six switches are provided on a single integrated circuit, the integrated circuit comprising:

a first physical pin coupled to the output of the first ground switch and the output of the first microphone switch;

a second physical pin coupled to the output of the second ground switch and the output of the second microphone switch;

a third physical pin coupled to the output of the first ground sensing switch; and

a fourth physical pin coupled to the output of the second ground sensing switch.

3. The apparatus of claim 2, further comprising a board for housing the switches, pins, and jack, wherein the fifth physical pin is electrically coupled to the first terminal of the jack at a point adjacent to the jack, and the sixth physical pin is electrically coupled to the second terminal of the jack at a point adjacent to the jack.

4. The apparatus of claim 2, wherein the single integrated circuit further comprises an audio codec.

5. The apparatus of claim 1, wherein the six switches are provided separately from an integrated circuit housing the audio codec, the apparatus further comprising:

a first physical pin coupled to the output of the first ground switch;

a second physical pin coupled to the output of the first microphone switch;

a third physical pin coupled to the output of the second ground switch;

a fourth physical pin coupled to the output of the second microphone switch;

a fifth physical pin coupled to the output of the first ground sensing switch; and

a sixth physical pin coupled to the output of the second ground sensing switch;

wherein the first and second physical pins are electrically coupled to each other, and the third and fourth physical pins are electrically coupled to each other.

6. The apparatus of claim 5, further comprising a board for housing the switches, pins, and jack, wherein the fifth physical pin is electrically coupled to the first terminal of the jack at a point adjacent to the jack, and the sixth physical pin is electrically coupled to the second terminal of the jack at a point adjacent to the jack.

7. The apparatus of claim 1, further comprising left and right audio channel amplifiers each comprising:

a differential amplifier having positive and negative inputs and an output;

a first resistor (R1a or R1b') coupled to the negative input;

a second resistor (R1b or R1a') coupled to the positive input;

a third resistor (R2a or R2b') coupling the output to the negative input; and

a fourth resistor (R2a' or R2b) coupling the positive input to the ground sensing input.

8. The apparatus of claim 7, wherein:

the first ground sensing switch is coupled to the first terminal of the jack via a first inductor, and a first capacitor further couples the connection between the first inductor and the first ground sensing switch to ground; and

the second ground sensing switch is coupled to the second terminal of the jack via a second inductor, and a second capacitor further couples the connection between the second inductor and the second ground sensing switch to ground.

9. The apparatus of claim 8, wherein the plurality of switches is integrated on a single chip, the single chip further comprising the circuitry for the left and right audio channel amplifiers.

10. The apparatus of claim 8, wherein the left and right audio channel amplifiers are provided on an integrated circuit, and the plurality of switches is provided separately from the integrated circuit.

11. The apparatus of claim 8, wherein the first and second inductors comprise ferrite beads.

12. The apparatus of claim 8, further comprising FM radio processing circuitry coupled to the first and second terminals of the jack.

13. An apparatus comprising:

a first ground switch configured to selectively couple a first terminal of a jack to a ground connection;

a second ground switch configured to selectively couple a second terminal of the jack to the ground connection;

a first microphone switch configured to selectively couple the first terminal of the jack to a microphone node;

a second microphone switch configured to selectively couple the second terminal of the jack to the microphone node; and

means for selectively coupling either the first or second terminal of the jack to a ground sensing input based on whether the jack is detected to be of a North American or a European type.

14. The apparatus of claim 13, the means for selectively coupling comprising:

a first inductor coupling a first ground sensing switch to the first terminal of the jack; and

a second inductor coupling a second ground sensing switch to the second terminal of the jack.

15. The apparatus of claim 13, further comprising means for driving left and right audio terminals of the jack.

16. The apparatus of claim 13, wherein the switches and means for selectively coupling are provided on a single integrated circuit, the integrated circuit further comprising:

means for coupling the output of the first ground switch and the output of the first microphone switch; and

means for coupling the output of the second ground switch and the output of the second microphone switch.

17. The apparatus of claim 16, further comprising a board for housing the switches, means for selectively coupling, and means for coupling.

18. A method comprising:

selectively coupling a first terminal of a jack to a ground connection using a first ground switch;

selectively coupling a second terminal of the jack to the ground connection using the second ground switch;

selectively coupling the first terminal of the jack to a microphone connection using a first microphone switch;

selectively coupling the second terminal of the jack to the microphone node using a second microphone switch;

selectively coupling the first terminal of the jack to a ground sensing input using a first ground sensing switch; and

selectively coupling the second terminal of the jack to the ground sensing input using a second ground sensing switch; wherein the switches are selectively coupled depending on whether the jack is detected to be of a North American or a European type.

19. The method of claim 18, further comprising:

coupling the first ground sensing switch to the first terminal of the jack using a first inductor;

coupling the connection between the first inductor and the first ground sensing switch to ground using a first capacitor;

coupling the second ground sensing switch to the second terminal of the jack using a second inductor; and

coupling the connection between the second inductor and the second ground sensing switch to ground.

20. The method of claim 18, wherein the plurality of switches is integrated on a single chip, the single chip further comprising the circuitry for the left and right audio channel amplifiers.

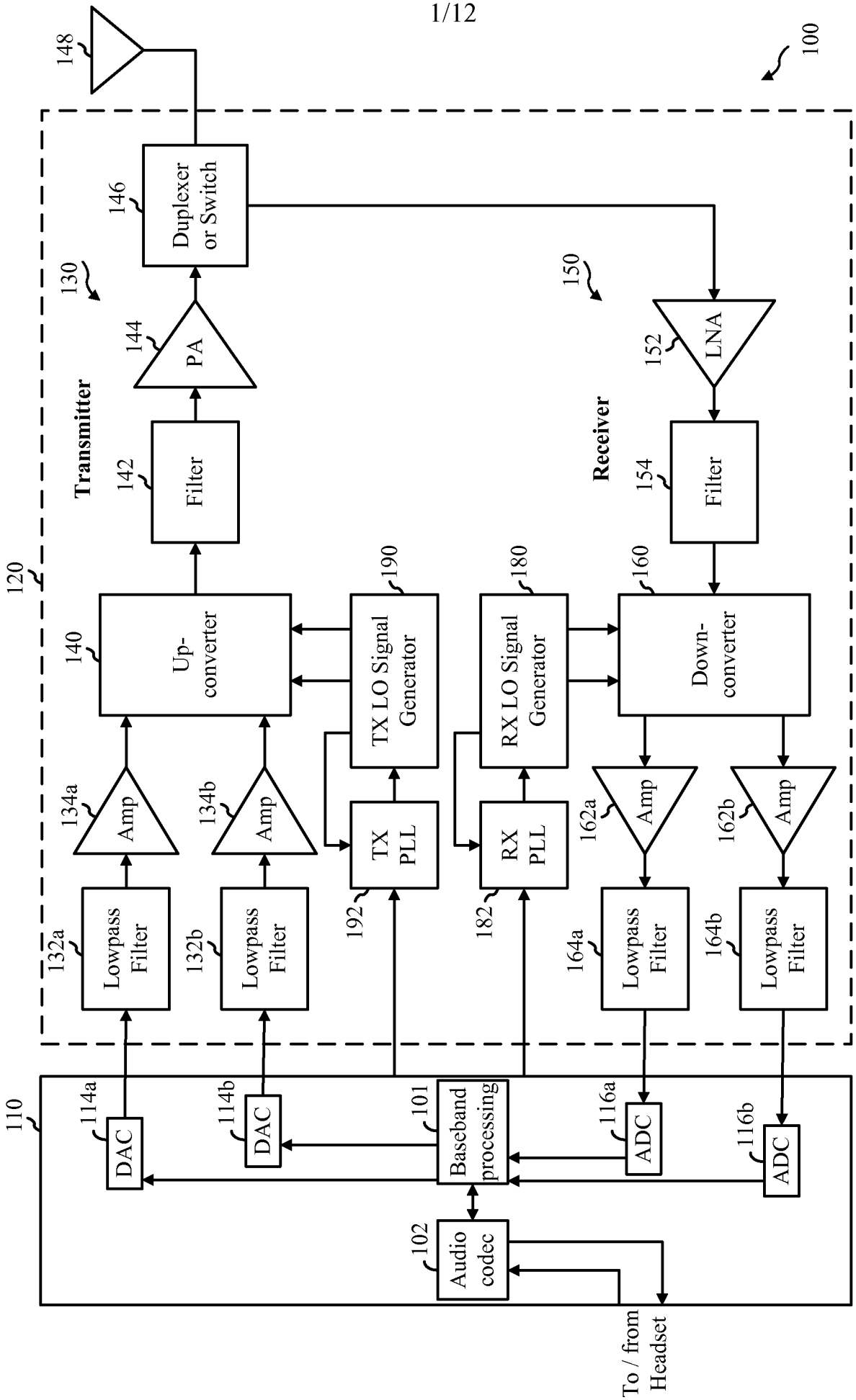

100
148
146
Duplexer or Switch
130
Transmitter
144
PA
142
Filter
150
Receiver
152
LNA
154
Filter
120
140
Up-converter
190
TX LO Signal Generator
180
RX LO Signal Generator
160
Down-converter
134a
Amp
134b
Amp
162a
Amp
162b
Amp
132a
Lowpass Filter
132b
Lowpass Filter
164a
Lowpass Filter
164b
Lowpass Filter
192
TX PLL
182
RX PLL
110
114a
DAC
114b
DAC
101
Baseband processing
116a
ADC
116b
ADC
102
Audio codec
To / from Headset

FIG 1

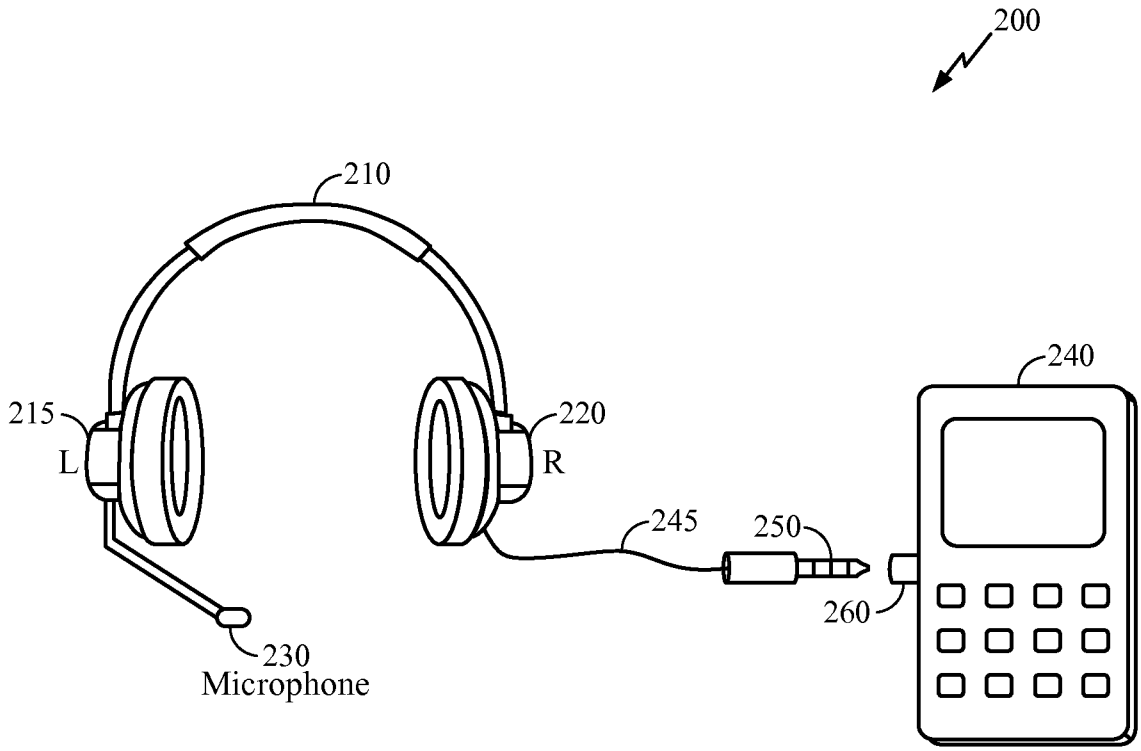
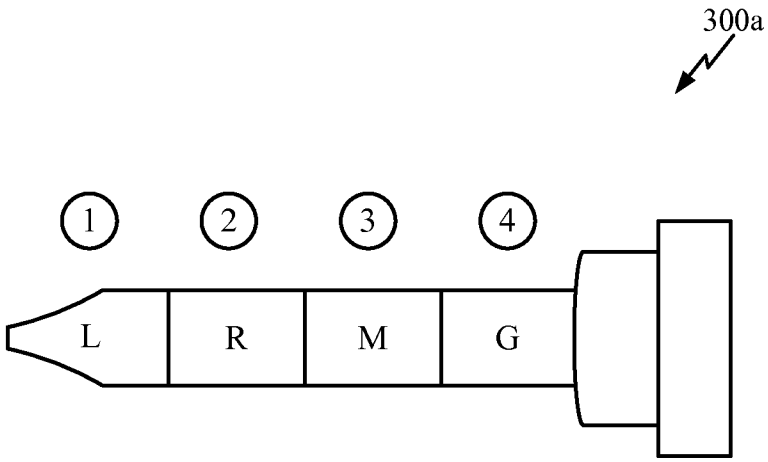
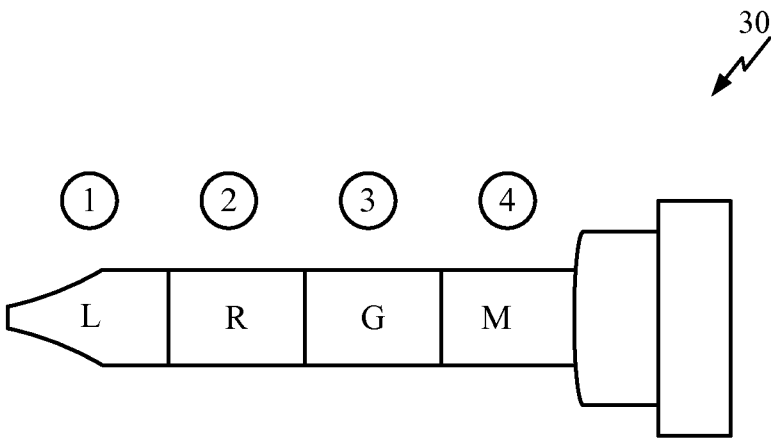


FIG 2



European
(ϕ1)



North American
(ϕ2)

FIG 3

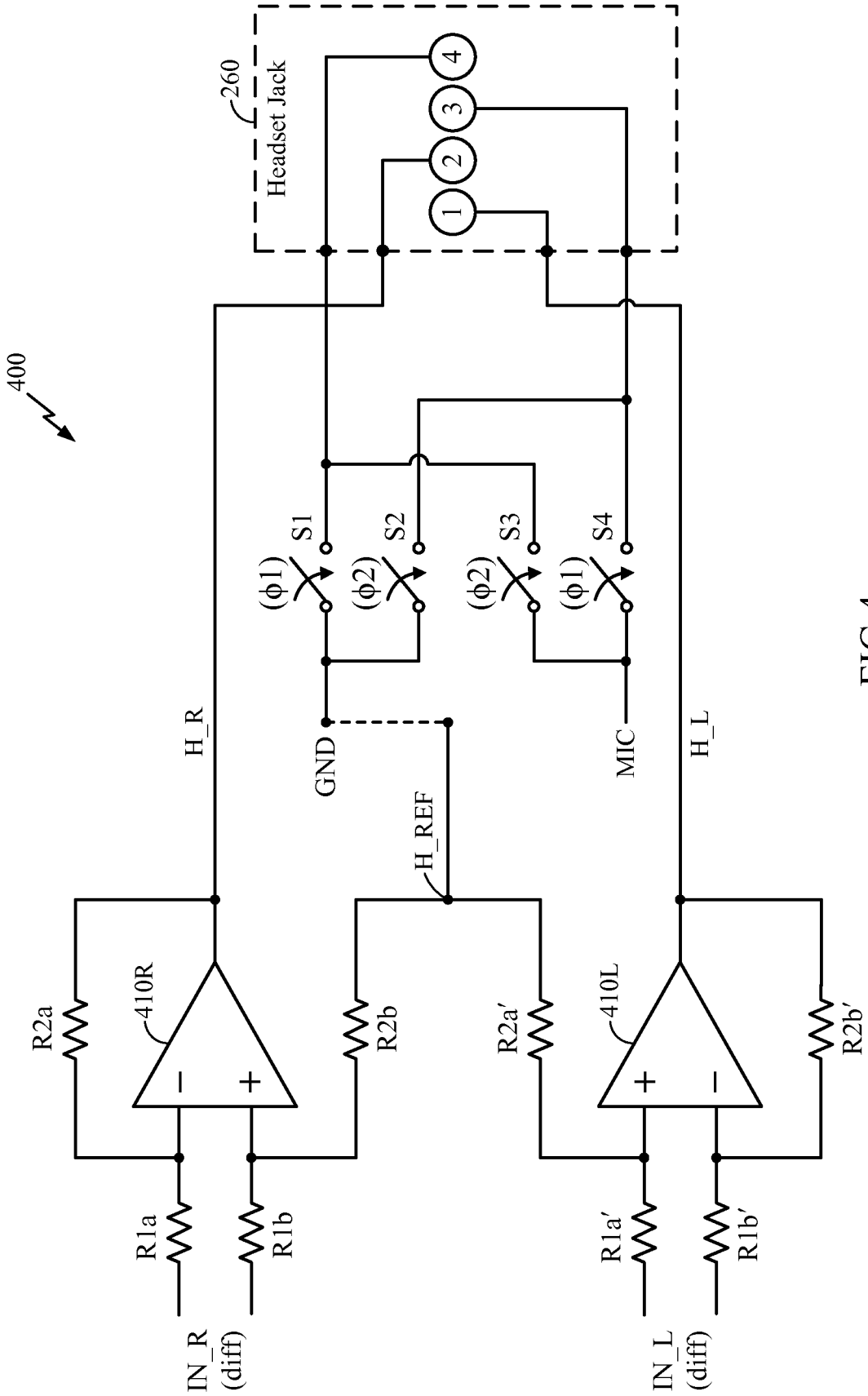

400
260
Headset Jack
1
2
3
4
S1
S2
S3
S4
(ϕ1)
(ϕ2)
(ϕ2)
(ϕ1)
H_R
GND
H_REF
MIC
H_L
R2a
410R
R2b
R2a′
410L
R2b′
R1a
R1b
R1a′
R1b′
IN_R
(diff)
IN_L
(diff)

FIG 4

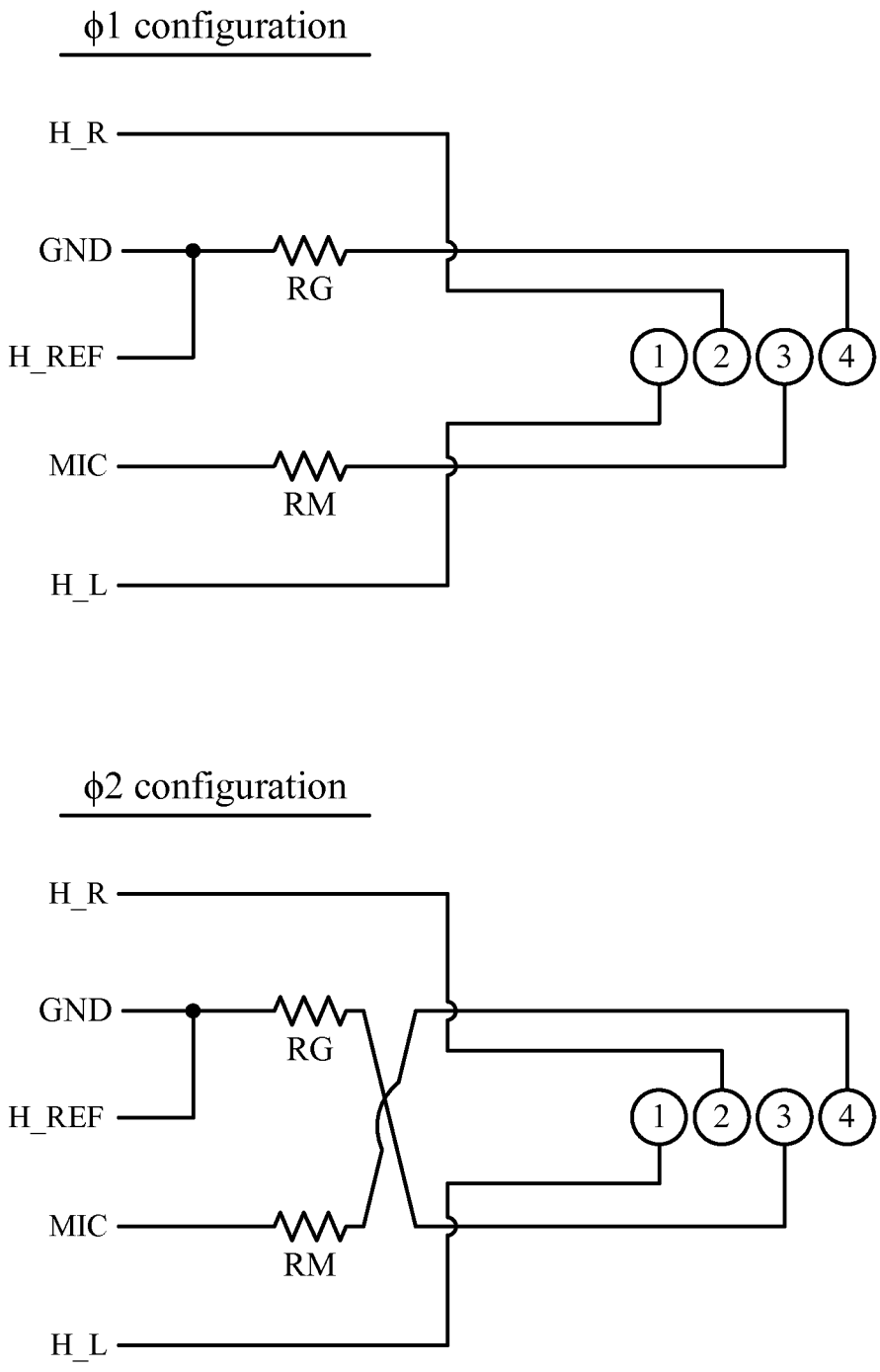

ϕ1 configuration
H_R
GND
RG
H_REF
1
2
3
4
MIC
RM
H_L
ϕ2 configuration
H_R
GND
RG
H_REF
1
2
3
4
MIC
RM
H_L

FIG 5

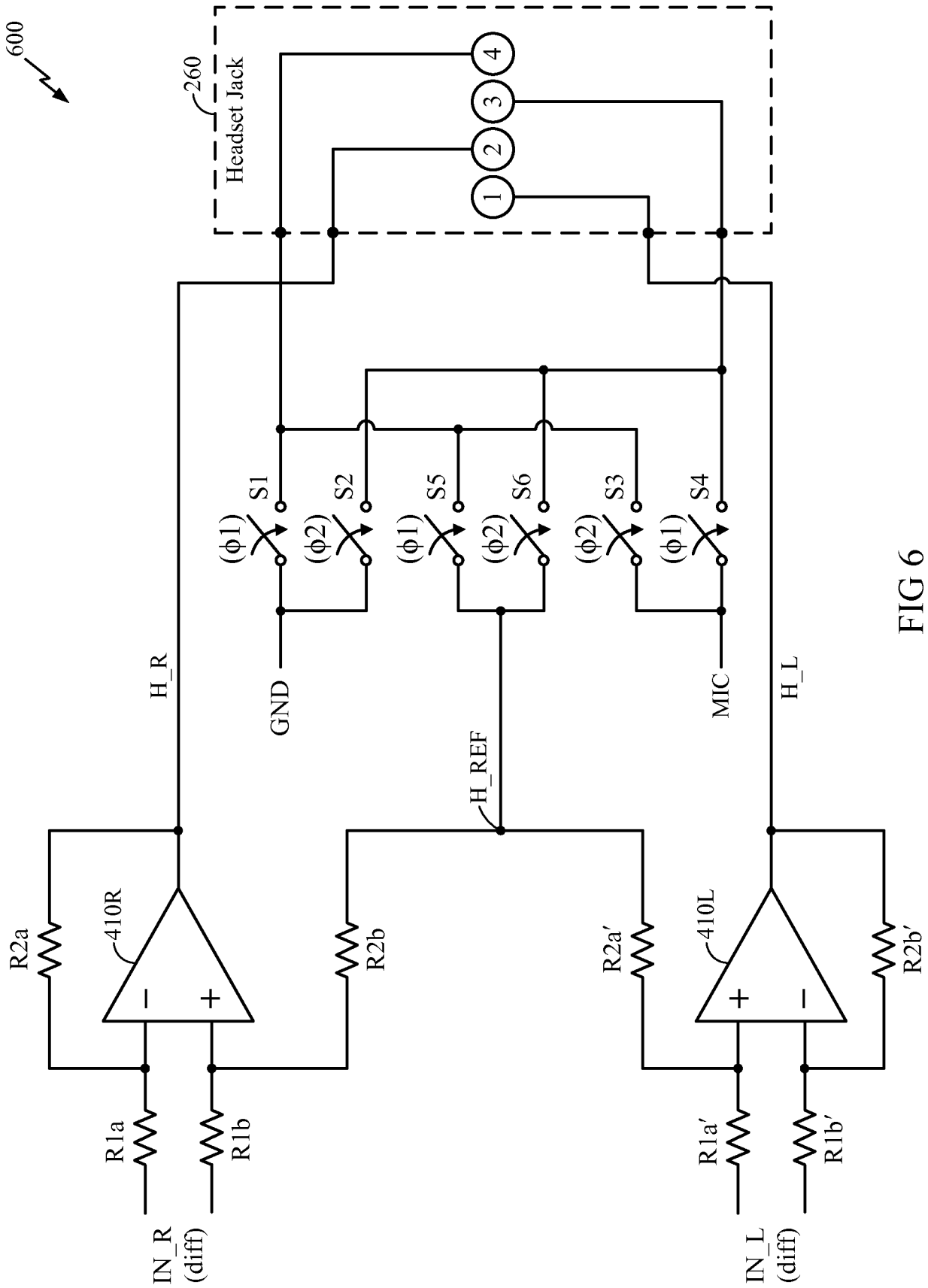

600
260
Headset Jack
4
3
2
1
S1
S2
S5
S6
S3
S4
(ϕ1)
(ϕ2)
(ϕ1)
(ϕ2)
(ϕ2)
(ϕ1)
GND
MIC
H_R
H_REF
H_L
R2a
410R
R2b
R2a′
410L
R2b′
R1a
R1b
R1a′
R1b′
IN_R
(diff)
IN_L
(diff)

FIG 6

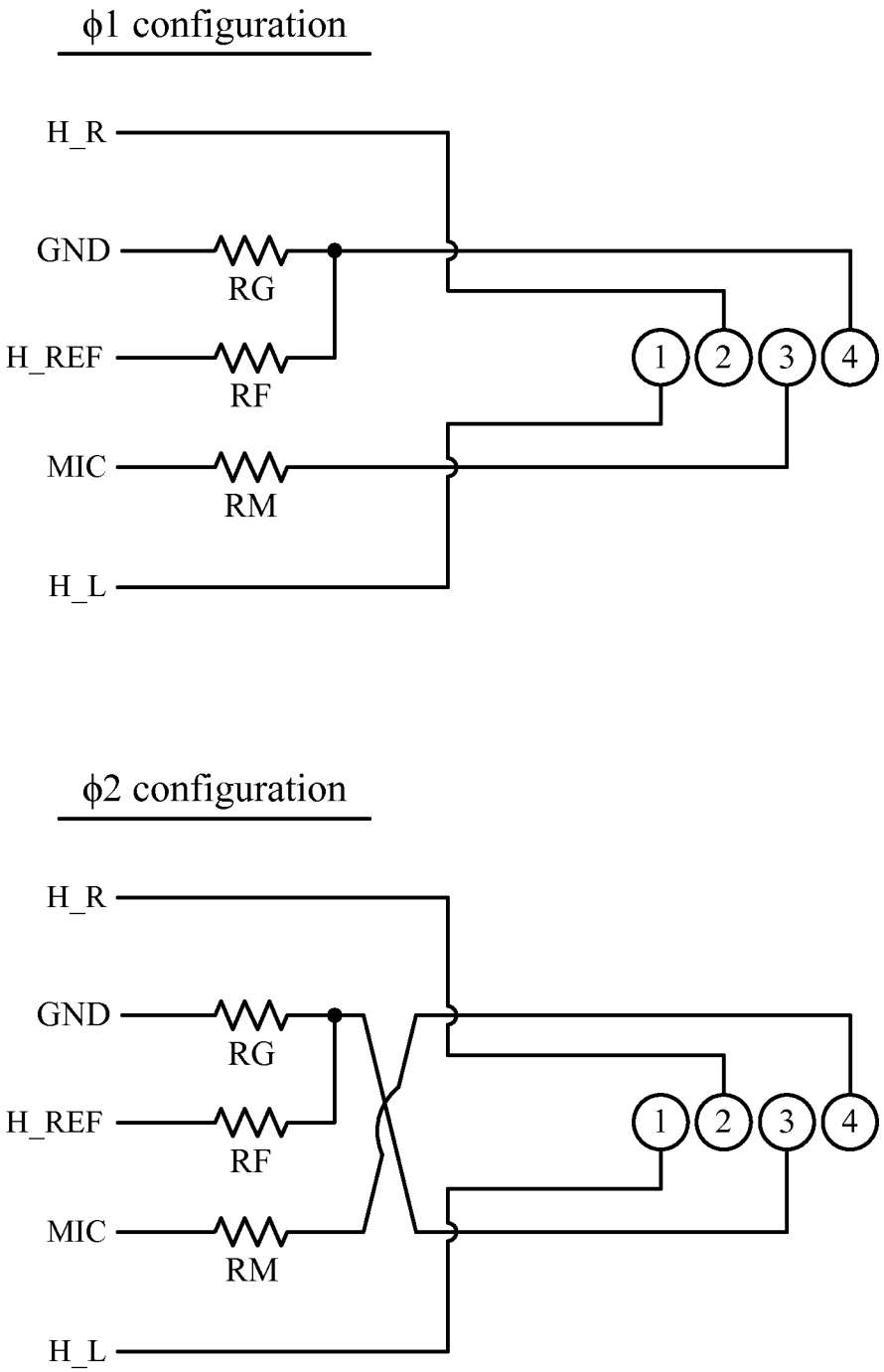

ϕ1 configuration
H_R
GND
RG
H_REF
RF
MIC
RM
H_L
1
2
3
4
ϕ2 configuration
H_R
GND
RG
H_REF
RF
MIC
RM
H_L
1
2
3
4

FIG 7

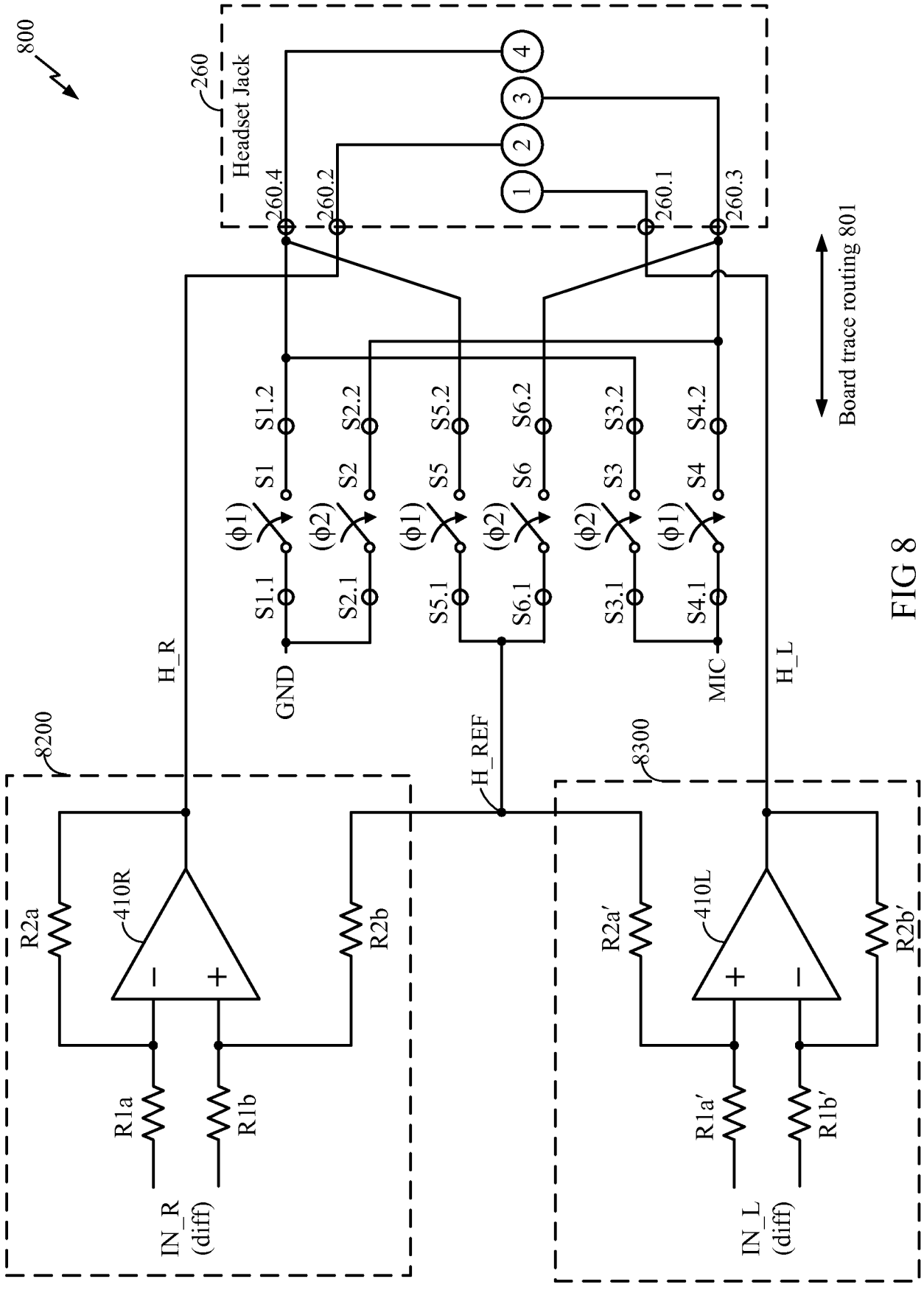

800
260
Headset Jack
260.4
260.2
260.1
260.3
1
2
3
4
Board trace routing 801
S1.2
S2.2
S5.2
S6.2
S3.2
S4.2
S1
S2
S5
S6
S3
S4
(ϕ1)
(ϕ2)
S1.1
S2.1
S5.1
S6.1
S3.1
S4.1
GND
MIC
H_R
H_L
H_REF
8200
8300
R2a
410R
R2b
R1a
R1b
IN_R
(diff)
R2a′
410L
R2b′
R1a′
R1b′
IN_L
(diff)

FIG 8

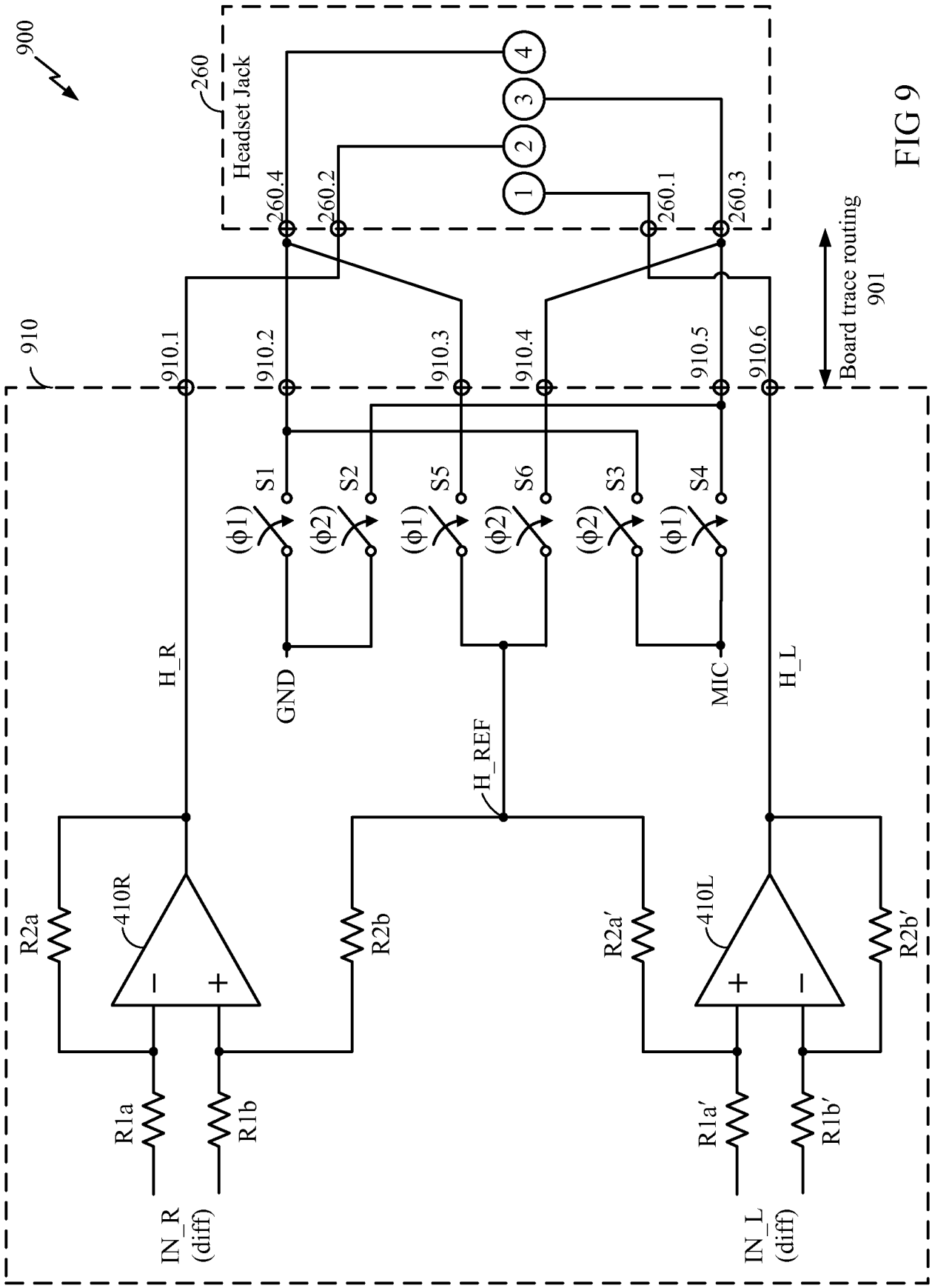

900
260
Headset Jack
260.4
260.2
260.1
260.3
1
2
3
4
910
910.1
910.2
910.3
910.4
910.5
910.6
Board trace routing
901
S1
S2
S5
S6
S3
S4
(ϕ1)
(ϕ2)
H_R
H_L
GND
MIC
H_REF
R2a
R2b
R2a′
R2b′
410R
410L
R1a
R1b
R1a′
R1b′
IN_R
(diff)
IN_L
(diff)

FIG 9

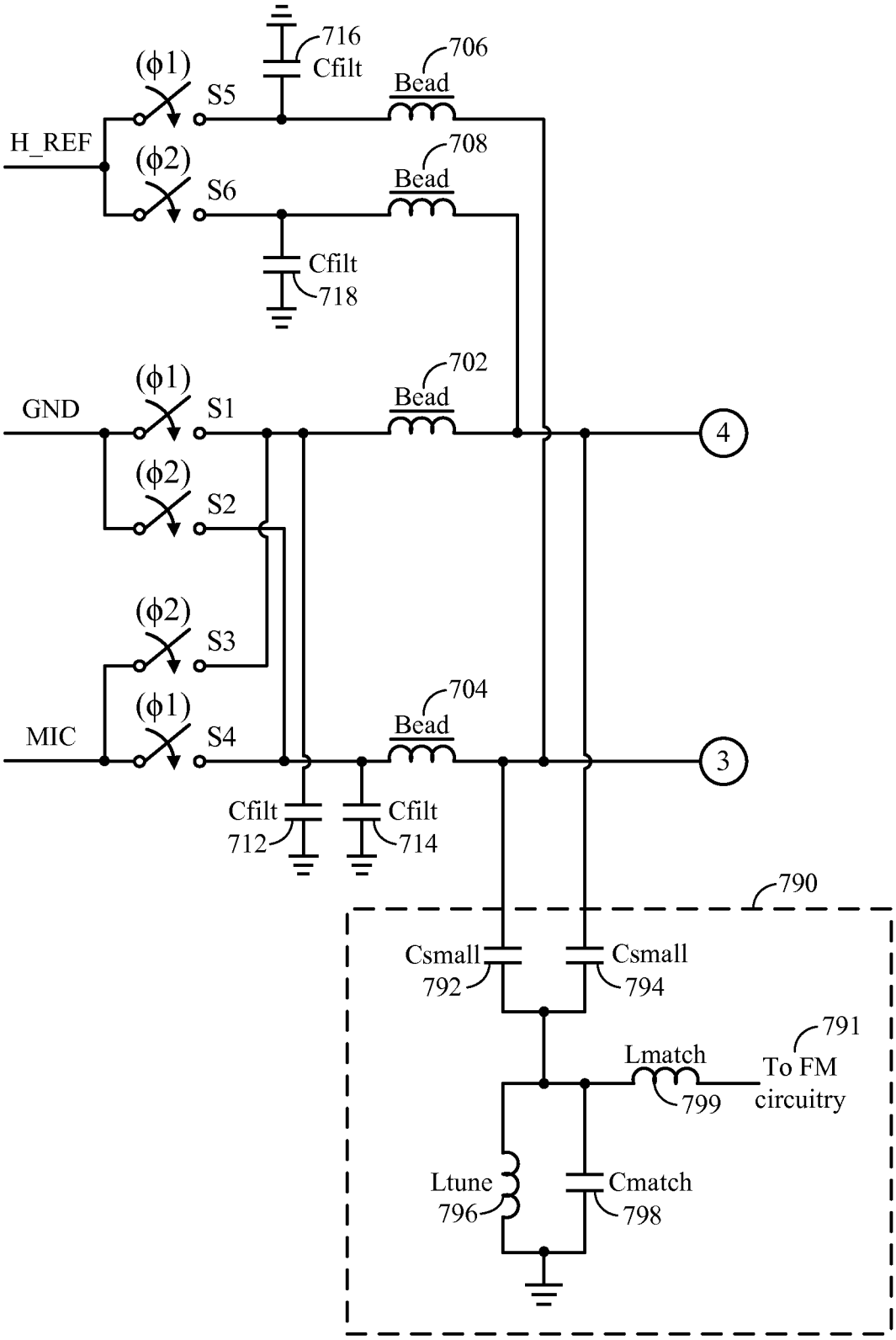

716
Cfilt
706
Bead
(ϕ1)
S5
H_REF
(ϕ2)
S6
708
Bead
Cfilt
718
GND
(ϕ1)
S1
702
Bead
4
(ϕ2)
S2
(ϕ2)
S3
MIC
(ϕ1)
S4
704
Bead
3
Cfilt
712
Cfilt
714
790
Csmall
792
Csmall
794
791
Lmatch
To FM
circuitry
799
Ltune
796
Cmatch
798

FIG 10

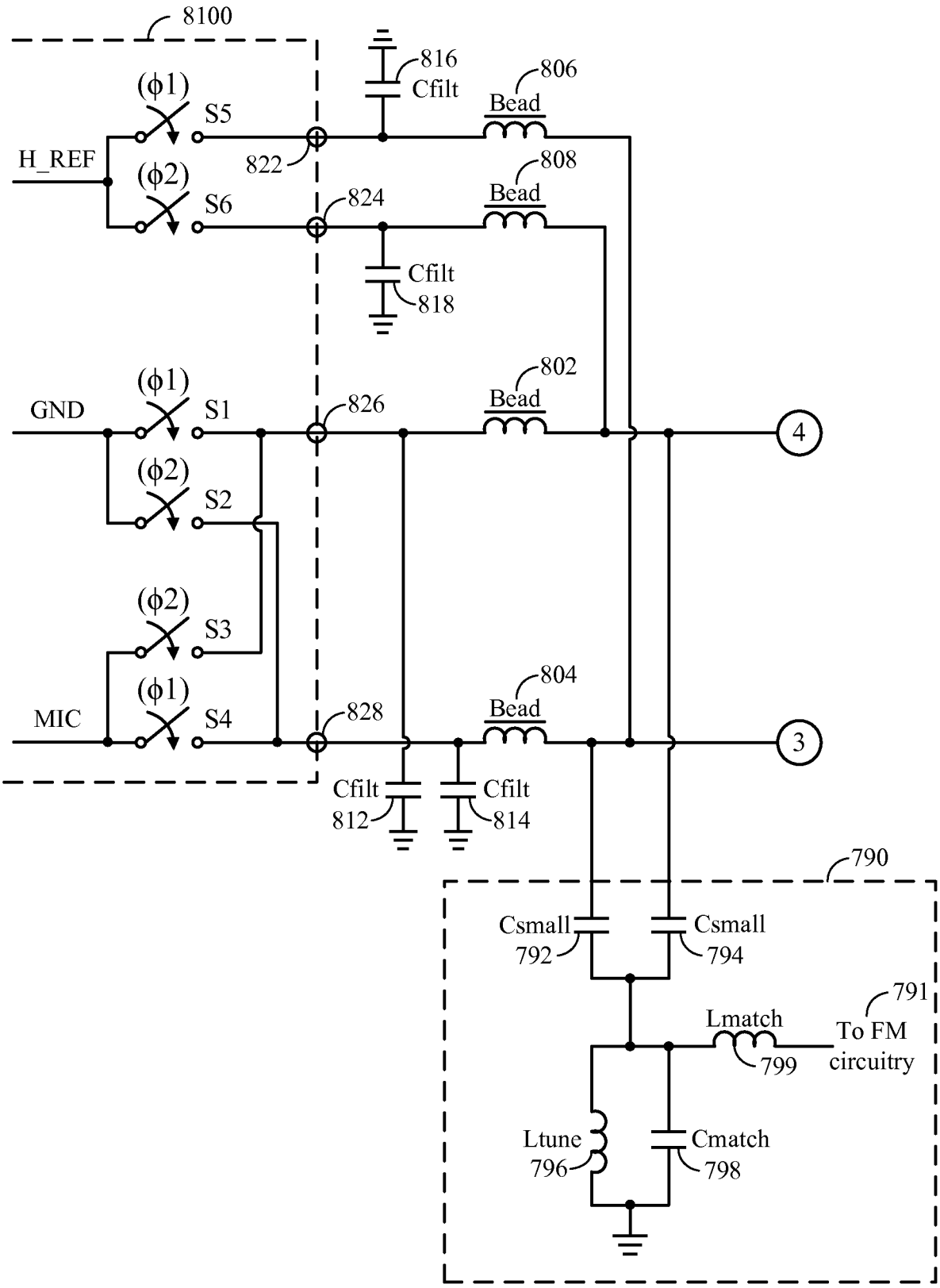

8100
816
Cfilt
806
Bead
(ϕ1)
S5
H_REF
822
(ϕ2)
S6
824
808
Bead
Cfilt
818
802
Bead
(ϕ1)
GND
S1
826
4
(ϕ2)
S2
(ϕ2)
S3
804
Bead
(ϕ1)
MIC
S4
828
3
Cfilt
812
Cfilt
814
790
Csmall
792
Csmall
794
791
Lmatch
To FM
circuitry
799
Ltune
796
Cmatch
798

FIG 11

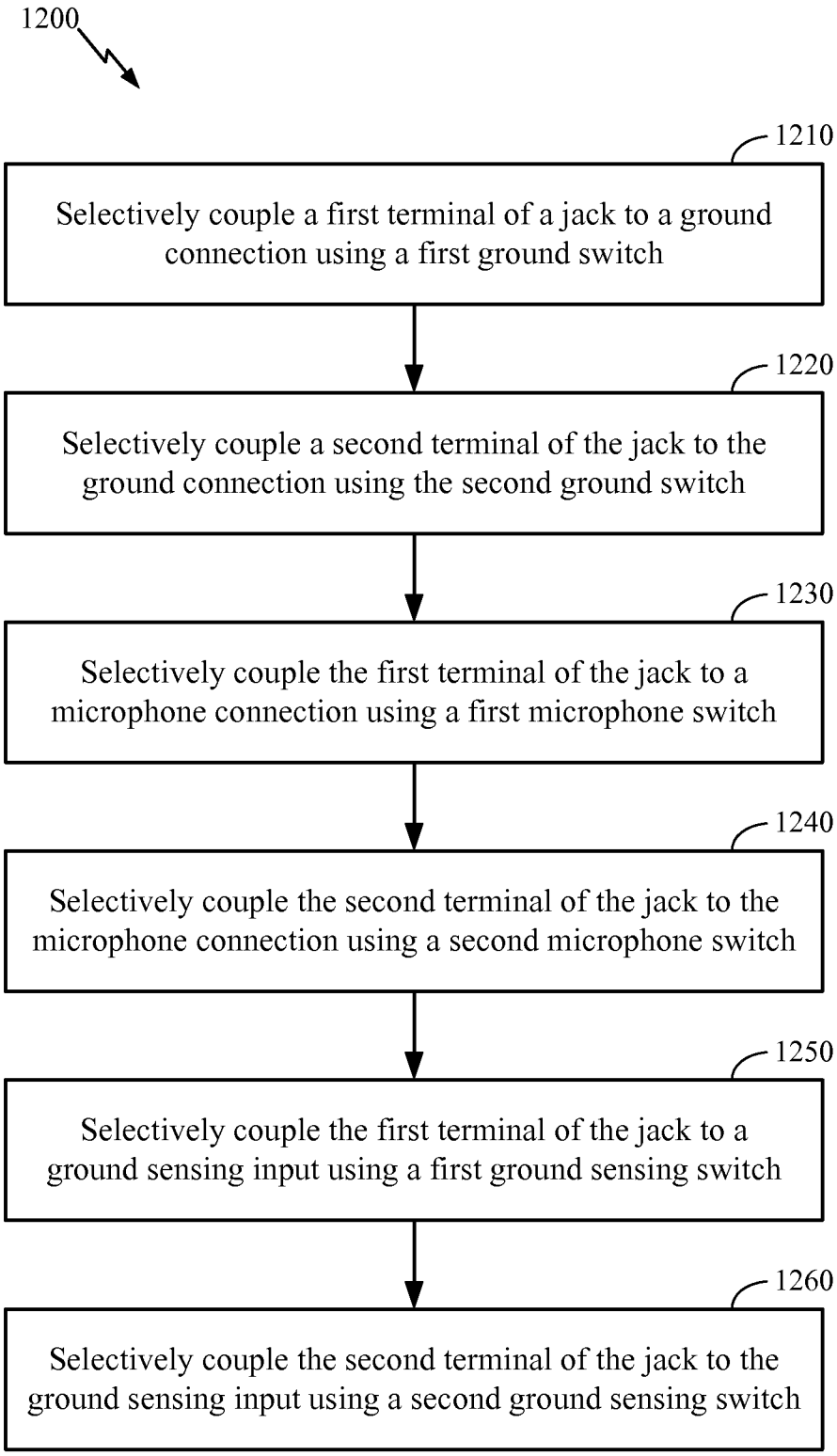

1200
1210
Selectively couple a first terminal of a jack to a ground connection using a first ground switch
1220
Selectively couple a second terminal of the jack to the ground connection using the second ground switch
1230
Selectively couple the first terminal of the jack to a microphone connection using a first microphone switch
1240
Selectively couple the second terminal of the jack to the microphone connection using a second microphone switch
1250
Selectively couple the first terminal of the jack to a ground sensing input using a first ground sensing switch
1260
Selectively couple the second terminal of the jack to the ground sensing input using a second ground sensing switch

FIG 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/035522

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04R1/10 H04R5/04
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04R H04M H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/215183 A1 (HANSSON MAGNUS [CA] ET AL) 26 August 2010 (2010-08-26) the whole document	1-20
A	WO 2011/079720 A1 (HUAWEI DEVICE CO LTD [CN]; YU CHENGDONG [CN]; WEI KONGGANG [CN]; LIU H) 7 July 2011 (2011-07-07) the whole document & US 2012/263313 A1 (YU CHENGDONG [CN] ET AL) 18 October 2012 (2012-10-18)	1-20
A	US 6 856 046 B1 (SCARLETT SHAWN W [US] ET AL) 15 February 2005 (2005-02-15) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 May 2013	31/05/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kunze, Holger

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/035522

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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