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(54) **Title:** METHOD OF ENHANCING ETCHING SELECTIVITY USING A PULSED PLASMA

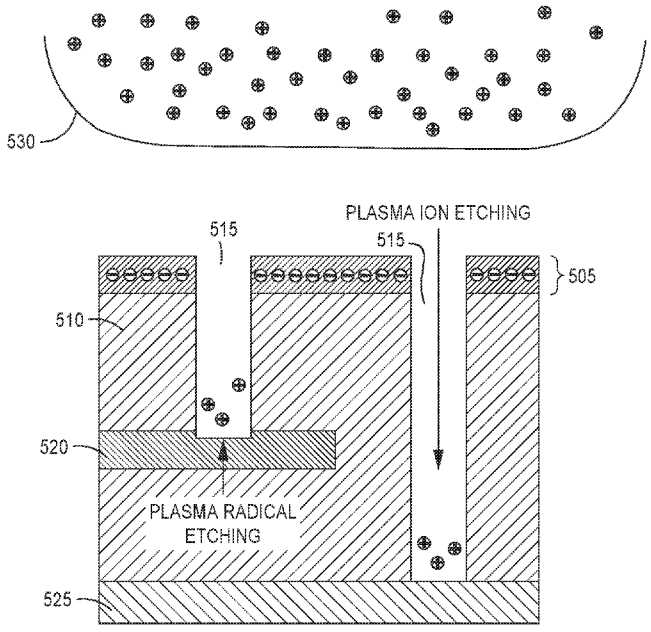


FIG. 7

(57) **Abstract:** Embodiments of this disclosure include a method of processing a substrate that includes etching a first dielectric material formed on a substrate that is disposed on a substrate supporting surface of a substrate support assembly disposed within a processing region of a plasma processing chamber The etching process may include delivering a process gas to the processing region, wherein the process gas comprises a first fluorocarbon containing gas and a first process gas, delivering, by use of a radio frequency generator, a radio frequency signal to a first electrode to form a plasma in the processing region, and establishing, by use of a first pulsed-voltage waveform generator, a first pulsed voltage waveform at a biasing electrode disposed within the substrate support assembly. The first pulsed voltage waveform comprises a series of repeating pulsed waveform cycles that each include a first portion that occurs during a first time interval, a second portion that occurs during a second time interval, and a peak-to-peak voltage. The pulsed voltage waveform

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Is substantially constant during at least a portion of the second time interval.

METHOD OF ENHANCING ETCHING SELECTIVITY USING A PULSED PLASMA

BACKGROUND

Field

[0001] Embodiments described herein generally relate to semiconductor device manufacturing hardware and processes, and more specifically to an apparatus and methods of processing a substrate in a plasma processing chamber.

Description of the Related Art

[0002] Reliably producing high aspect ratio features is one of the key technology challenges for the next generation of very large scale integration (VLSI) and ultra large scale integration (ULSI) of semiconductor devices. One method of forming high aspect ratio features uses a plasma assisted etching process, such as a reactive ion etch (RIE) plasma process, to form high aspect ratio openings in a material layer, such as a dielectric layer, of a substrate. In a typical RIE plasma process, a plasma is formed in an RIE processing chamber and ions from the plasma are accelerated towards a surface of a substrate to form openings in a material layer disposed beneath a mask layer formed on the surface of the substrate.

[0003] A typical Reactive Ion Etch (RIE) plasma processing chamber includes a radio frequency (RF) bias generator, which supplies an RF voltage to a "power electrode" (e.g., a biasing electrode), such as a metal plate positioned adjacent to an "electrostatic chuck" (ESC) assembly, more commonly referred to as the "cathode". The power electrode can be capacitively coupled to the plasma of a processing system through a thick layer of dielectric material (e.g., ceramic material), which is a part of the ESC assembly. In a capacitively coupled gas discharge, the plasma is created by using a radio frequency (RF) generator that is coupled to an RF electrode through an RF matching network ("RF match") that tunes the apparent load to 50Ω to minimize the reflected power and maximize the power delivery efficiency. The application of RF voltage to the power electrode causes an electron-repelling plasma sheath (also referred to as the "cathode sheath") to form over a processing surface of a substrate that is positioned on a substrate

supporting surface of the ESC assembly during processing. The non-linear, diode-like nature of the plasma sheath results in rectification of the applied RF field, such that a direct-current (DC) voltage drop, or "self-bias", appears between the substrate and the plasma, making the substrate potential negative with respect to the plasma potential. This voltage drop determines the average energy of the plasma ions accelerated towards the substrate, and thus etch anisotropy. More specifically, ion directionality, the feature profile, and etch selectivity to the mask and the stop-layer are controlled by the Ion Energy Distribution Function (IEDF). In plasmas with RF bias, the IEDF typically has two non-discrete peaks, one at a low energy and one at a high energy, and an ion population that has a range of energies that extend between the two peaks. The presence of the ion population in-between the two peaks of the IEDF is reflective of the fact that the voltage drop between the substrate and the plasma oscillates at the RF bias frequency. When a lower frequency RF bias generator is used to achieve higher self-bias voltages, the difference in energy between these two peaks can be significant; and because the etch profile due to the ions at low energy peak is more isotropic, this could potentially lead to bowing of the etched feature walls. Compared to the high-energy ions, the low-energy ions are less effective at reaching the corners at the bottom of the etched feature (e.g., due to the charging effect), but cause less sputtering of the mask material. This is important in high aspect ratio etch applications, such as hard-mask opening or dielectric mold etch. As feature sizes continue to diminish and the aspect ratio increases, while feature profile control requirements become more stringent, it becomes more desirable to have a well-controlled IEDF at the substrate surface during processing.

[0004] Other conventional plasma processes and processing chamber designs have also found that delivering multiple different RF frequencies to one or more of the electrodes in a plasma processing chamber can be used to control various plasma properties, such as plasma density, ion energy, and/or plasma chemistry. However, it has been found that the delivery of multiple conventional sinusoidal waveforms from two or more RF sources, which are each configured to provide different RF frequencies, is unable to adequately or desirably control the sheath properties and can lead to undesirable arcing problems. Moreover, due to direct or capacitive coupling between the RF sources during processing, each RF source may induce an RF current that is provided

to the output of the other connected RF source(s) (e.g., often referred to as the "cross-talk"), resulting in the power being diverted away from the intended load (plasma), as well as possibly causing damage to each of the RF sources.

[0005] Recently, high density storage devices have been developed that include a three-dimensional (3D) stacked memory structure. For example, a 3D NAND stacked memory device can be formed from an array of alternating vertical stacks of dielectric materials and electrically conductive layers (e.g., tungsten containing layers). Memory openings are formed and extend vertically through the dielectric material containing layers in the alternating stack to expose portions of the conductive layers, and thus have varying depths within the alternating stack structure. The memory openings are eventually filled with a conductive material to form a connection with the exposed portion of each conductive layer in each layer of the alternating stack. The electrically conductive layers within the alternating stack can function as word lines of a 3D NAND stacked memory device, and bit lines overlying an array of memory stack structures can be connected to drain-side ends of the semiconductor channels. However, it is desirable when forming the memory openings, which extend to different depths within the alternating stack, in a single etching step without over etching portions of the layers of the alternating stack at the shallowest depths versus the layers formed at the deepest depths. Therefore, there is a need for an etch process that can selectivity etch the dielectric portions of the alternating stack and stop on the conductive layers, such that all of the memory openings can be formed to all of the layers within alternating stack without over-etching the exposed portions of the various conductive features during the etching process.

[0006] Accordingly, there is a need in the art for novel, robust and reliable plasma processing and biasing methods that enable maintaining a nearly constant sheath voltage, and thus create a desirable and repeatable IEDF at the surface of the substrate to enable a precise control over the shape of IEDF and, in some cases, the etch profile of the features formed in the surface of the substrate. There is also a need for a system, device(s) and methods that solve the problems described above.

SUMMARY

[0007] The present disclosure generally includes a method of processing a substrate in a plasma processing chamber that includes etching a first dielectric material formed on a substrate that is disposed on a substrate supporting surface of a substrate support assembly disposed within a processing region of the plasma processing chamber. The process of etching the first dielectric material includes delivering a process gas to the processing region of the plasma processing chamber, wherein the process gas comprises a first fluorocarbon containing gas and a first process gas, delivering, by use of a radio frequency generator, a radio frequency signal to a first electrode disposed within the plasma processing chamber to form a plasma in the processing region, and establishing, by use of a first pulsed-voltage waveform generator, a first pulsed voltage waveform at a biasing electrode disposed within the substrate support assembly, wherein the first pulsed voltage waveform comprises a series of repeating pulsed waveform cycles. Each pulsed waveform cycle includes a first portion that occurs during a first time interval and a second portion that occurs during a second time interval, wherein the second time interval is larger than the first time interval, and a peak-to-peak voltage. The pulsed voltage waveform is substantially constant during at least a portion of the second time interval.

[0008] Embodiments of the present disclosure may further provide a method of processing a substrate in a plasma processing chamber that includes etching a first dielectric material formed on a substrate that is disposed on a substrate supporting surface of a substrate support assembly disposed within a processing region of the plasma processing chamber. The process of etching the first dielectric material includes delivering a process gas to the processing region of the plasma processing chamber, wherein the process gas comprises a first fluorocarbon containing gas and a first process gas. The first fluorocarbon-containing gas comprises at least one of C_4F_6 or C_3F_6, and the first process gas comprises at least one of N_2, Kr, and O_2. The process of etching the first dielectric material also includes delivering, by use of a radio frequency generator, a radio frequency signal to a first electrode disposed within the plasma processing chamber to form a plasma in the processing region, and establishing, by use of a first

pulsed-voltage waveform generator, a first pulsed voltage waveform at a biasing electrode disposed within the substrate support assembly, wherein the first pulsed voltage waveform comprises a series of repeating pulsed waveform cycles. Each pulsed waveform cycle includes a first portion that occurs during a first time interval and a second portion that occurs during a second time interval, wherein the second time interval is larger than the first time interval, and a peak-to-peak voltage. The first time interval can be between about 200 ns and about 400 ns, and the first time interval can be less than about 20% of a cycle of the series of repeating cycles. The pulsed voltage waveform within each pulsed waveform cycle can have a peak-to-peak voltage that is between about 5 kV and 20 kV. The pulsed voltage waveform is substantially constant during at least a portion of the second time interval.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, and may admit to other equally effective embodiments.

[0010] Figure 1 is a schematic cross-sectional view of a processing chamber configured to practice methods described herein, according to one embodiment.

[0011] Figure 2 is a simplified schematic diagram of a biasing scheme that can be used with the process chamber illustrated in Figure 1, according to one embodiment.

[0012] Figure 3A is a functionally equivalent circuit diagram of a negative pulse biasing scheme that can be performed in the process chamber illustrated in Figure 1, according to one embodiment.

[0013] Figure 3B is a functionally equivalent circuit diagram of a positive pulse biasing scheme that can be performed in the process chamber illustrated in Figure 1, according to one embodiment.

[0014] Figure 4A illustrates an example of a negative pulsed voltage (PV) waveform established at the biasing electrode, according to one embodiment.

[0015] Figure 4B illustrates an example of a shaped pulsed voltage (PV) waveform established at the biasing electrode, according to one embodiment.

[0016] Figure 4C illustrates an example of a positive pulsed voltage (PV) waveform established at the biasing electrode, according to one embodiment.

[0017] Figure 4D illustrates a comparison of a negative pulsed voltage (PV) waveform and a positive pulsed voltage (PV) waveform established at a substrate during processing, according to one embodiment.

[0018] Figure 5 illustrates a diagram of a substrate with etched trenches reaching to various conductive layers of the substrate, according to one embodiment.

[0019] Figures 6A-6C illustrate a diagram of the plasma etching process on a substrate, according to one embodiment.

[0020] Figure 7 illustrates a diagram of the plasma etching process on a substrate, according to one embodiment.

[0021] Figure 8 illustrates example sheath thickness during the plasma etching process, according to one embodiment.

[0022] Figure 9 illustrates example operations of the plasma etching process, according to one embodiment.

[0023] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0024] Embodiments of the disclosure provided herein include an apparatus and method for the plasma processing of a substrate in a processing chamber. More specifically, embodiments of this disclosure describe a process for enhancing selectivity of etching dielectric layers relative to one or more inorganic substances using a pulsed plasma ion etching process. Embodiments of the present disclosure involve an apparatus that is configured to provide a radio frequency (RF) generated RF waveform from an RF generator to one or more electrodes within a processing chamber and a pulsed-voltage (PV) waveform delivered from one or more pulsed-voltage (PV) generators to the one or more electrodes within the processing chamber.

[0025] In general, the generated RF waveform is configured to establish and maintain a plasma within the processing chamber, and the delivered PV waveform(s) are configured to control the sheath voltage across the surface of a substrate during portions of the plasma process and thus create a desirable ion energy distribution function (IEDF) at the surface of the substrate during one or more plasma processing steps performed within the processing chamber. The plasma process(es) disclosed herein can be used to control the interaction of the plasma with a surface of a substrate during processing. In some configurations, the plasma process(es) disclosed herein are used to control the profile of features formed in the surface of the substrate during processing. In some embodiments, the pulsed voltage waveform is established by a PV generator that is electrically coupled to a biasing electrode disposed within a substrate support assembly disposed within a plasma processing chamber.

[0026] Generally, semiconductor device fabrication processes can include logic and memory fabrication processes, such as the fabrication of flash memory. As devices shrink, structures for fabricating efficient and multiple memory cells are used to maximize density of memory cells in a memory device. Three-dimension (3D) NAND technology addresses challenges with two-dimensional (2D) NAND technology and stacking memory cells vertically in layers.

[0027] Plasma etching processes involved in the fabrication of 3D NAND devices are becoming increasingly challenging. Specifically, the staircase contact etch in 3D NAND technology provides access to cells at the bottom of the NAND stack thereby allowing the deposition of conductive material (e.g., tungsten) to form word-lines that allow access to the cell control gates from the outside peripheral circuitry. Staircase contact etching creates challenges for etching, especially for high aspect ratio features ranging in aspect from 20:1 to 40:1. Etching through high aspect ratio conductive layers intensifies the demands on the etching process, which must be capable of forming openings in layers that are striation free, distortion free, and free of line bending, faceting, and feature clogging. Other than these demands, the priority of the staircase contact etch application is combining simultaneous multi-level etching at aspect ratios ranging from 20:1 to more than 40:1 with high selectively to assure that there is negligible loss of the underlying conductive contact materials.

[0028] Accordingly, pulse voltage technology can enable methods of precisely controlling the plasma ion density and ion energy during plasma processing. It is believed that the precise control of the plasma ion density and ion energy, in combination with the use of a desirable dry etch chemistries, can be used to cause an increase in etch selectivity and improve etch process result. Moreover, by use of one or more of the methods described herein, etch selectivity and improved etch process results can be further achieved by the controlled formation of a fluorocarbon-based polymer layer on the exposed conductive materials surfaces during the etching process.

[0029] Figure 1 is a schematic cross-sectional view of a processing chamber configured to practice methods described herein. During some semiconductor plasma processes, ions are purposely accelerated towards the substrate by the voltage drop in an electron-repelling sheath that forms over the substrate placed on top of a substrate-support assembly 136 (Figure 1). While not intending to be limiting as to the scope of the disclosure provided herein, the substrate support assembly 136 is often referred to herein as the “cathode assembly” or “cathode”. In some embodiments, the substrate support assembly 136 includes a substrate support 105 and a support base 107. The

substrate support 105 can include an electrostatic chuck (ESC) assembly that is configured to chuck (e.g., retain) a substrate on a substrate receiving surface 105A.

[0030] In some embodiments of the disclosure provided herein, a processing chamber is configured to provide a capacitively coupled gas discharge, such that a plasma is created by use of an RF generator assembly that includes an RF generator that is coupled to an RF electrode through an RF matching network ("RF match"). The RF matching network is configured to tune the apparent load to 50Ω to minimize the reflected power and maximize the power delivery efficiency. In some embodiments, the RF electrode includes a metal plate that is positioned parallel to the plasma-facing surface of the substrate.

[0031] Additionally, during the plasma processing methods disclosed herein, an ion-accelerating cathode sheath is generally formed during plasma processing by use of a pulsed-voltage (PV) generator that is configured to establish a pulsed-voltage waveform at one or more biasing electrodes 104 (Figure 1) disposed within the substrate support assembly 136. In some embodiments, the one or more biasing electrodes 104 include a chucking electrode that is separated from the substrate by a thin layer of a dielectric material formed within the substrate support assembly 136 (e.g., electrostatic chuck (ESC) assembly) and optionally an edge control electrode that is disposed within or below an edge ring 114 that surrounds a substrate 103 when the substrate 103 is disposed on the substrate supporting surface 105A of the substrate support assembly 136. As will be discussed further below, this PV waveform can be configured to cause a nearly constant sheath voltage (e.g., a difference between the plasma potential and the substrate potential) to be formed for a sizable portion of the PV waveform's pulse period, which corresponds to a single (narrow) peak containing ion energy distribution function (IEDF) of the ions reaching the substrate during this part of the pulse period, which is also referred to herein as the "ion-current phase".

Plasma Processing Chamber Hardware Examples

[0032] Figure 1 is a schematic cross-sectional view of a processing chamber 100, in which a complex load 130 (Figures 3A-3B) is formed during plasma processing. Figures

3A-3B are each examples of a simplified electrical circuit 140 of a pulsed voltage and RF biasing scheme that can be performed using the components found in processing chamber 100. The processing chamber 100 is configured to practice one or more of the biasing schemes proposed herein, according to one or more embodiments. In one embodiment, the processing chamber is a plasma processing chamber, such as a reactive ion etch (RIE) plasma chamber. In some other embodiments, the processing chamber is a plasma-enhanced deposition chamber, for example a plasma-enhanced chemical vapor deposition (PECVD) chamber, a plasma enhanced physical vapor deposition (PEPVD) chamber, or a plasma-enhanced atomic layer deposition (PEALD) chamber. In some other embodiments, the processing chamber is a plasma treatment chamber, or a plasma based ion implant chamber, for example a plasma doping (PLAD) chamber. In some embodiments, the plasma source is a capacitively coupled plasma (CCP) source, which includes an electrode (e.g., chamber lid 123) disposed in the processing volume facing the substrate support assembly 136. As illustrated in Figure 1, an opposing electrode, such as the chamber lid 123, which is positioned opposite to the substrate support assembly 136, is electrically coupled to ground. However, in other alternate embodiments, the opposing electrode is electrically coupled to an RF generator. In yet other embodiments, the processing chamber may alternately, or additionally, include an inductively coupled plasma (ICP) source electrically coupled to a radio frequency (RF) power supply.

[0033] The processing chamber 100 also includes a chamber body 113 that includes the chamber lid 123, one or more sidewalls 122, and a chamber base 124, which define a processing volume 129. The one or more sidewalls 122 and chamber base 124 generally include materials that are sized and shaped to form the structural support for the elements of the processing chamber 100, and are configured to withstand the pressures and added energy applied to them while a plasma 101 is generated within a vacuum environment maintained in the processing volume 129 of the processing chamber 100 during processing. In one example, the one or more sidewalls 122 and chamber base 124 are formed from a metal, such as aluminum, an aluminum alloy, or a stainless steel. A gas inlet 128 disposed through the chamber lid 123 is used to provide one or more processing gases to the processing volume 129 from a processing gas

source 119 that is in fluid communication therewith. A substrate 103 is loaded into, and removed from, the processing volume 129 through an opening (not shown) in one of the one or more sidewalls 122, which is sealed with a slit valve (not shown) during plasma processing of the substrate 103. Herein, the substrate 103 is transferred to and from a substrate receiving surface 105A of an ESC substrate support 105 using a lift pin system (not shown).

[0034] In some embodiments, an RF generator assembly 160 is configured to deliver RF power to the support base 107 disposed proximate to the ESC substrate support 105, and within the substrate support assembly 136. The RF power delivered to the support base 107 is configured to ignite and maintain a processing plasma 101 formed by use of processing gases disposed within the processing volume 129. In some embodiments, the support base 107 is an RF electrode that is electrically coupled to an RF generator 118 via an RF matching circuit 161 and a first filter assembly 162, which are both disposed within the RF generator assembly 160. In some embodiments, the plasma generator assembly 160 and RF generator 118 are used to ignite and maintain a processing plasma 101 using the processing gases disposed in the processing volume 129 and fields generated by the RF power provided to the support base 107 by the RF generator 118. The processing volume 129 is fluidly coupled to one or more dedicated vacuum pumps, through a vacuum outlet 120, which maintain the processing volume 129 at sub-atmospheric pressure conditions and evacuate processing and/or other gases, therefrom. A substrate support assembly 136, disposed in the processing volume 129, is disposed on a support shaft 138 that is grounded and extends through the chamber base 124. However, in some embodiments, the RF generator assembly 160 is configured to deliver RF power to the biasing electrode 104 disposed in the substrate support 105 versus the support base 107.

[0035] The substrate support assembly 136, as briefly discussed above, generally includes a substrate support 105 (e.g., ESC substrate support) and support base 107. In some embodiments, the substrate support assembly 136 can additionally include an insulator plate 111 and a ground plate 112, as is discussed further below. The substrate support 105 is thermally coupled to and disposed on the support base 107. In some

embodiments, the support base 107 is configured to regulate the temperature of the substrate support 105, and the substrate 103 disposed on the substrate support 105, during substrate processing. In some embodiments, the support base 107 includes one or more cooling channels (not shown) disposed therein that are fluidly coupled to, and in fluid communication with, a coolant source (not shown), such as a refrigerant source or water source having a relatively high electrical resistance. In some embodiments, the substrate support 105 includes a heater (not shown), such as a resistive heating element embedded in the dielectric material thereof. Herein, the support base 107 is formed of a corrosion resistant thermally conductive material, such as a corrosion resistant metal, for example aluminum, an aluminum alloy, or stainless steel and is coupled to the substrate support with an adhesive or by mechanical means.

[0036] The support base 107 is electrically isolated from the chamber base 124 by the insulator plate 111, and the ground plate 112 is interposed between the insulator plate 111 and the chamber base 124. In some embodiments, the processing chamber 100 further includes a quartz pipe 110, or collar, that at least partially circumscribes portions of the substrate support assembly 136 to prevent corrosion of the ESC substrate support 105 and, or, the support base 107 from contact with corrosive processing gases or plasma, cleaning gases or plasma, or byproducts thereof. Typically, the quartz pipe 110, the insulator plate 111, and the ground plate 112 are circumscribed by a liner 108. Herein, a plasma screen 109 approximately coplanar with the substrate receiving surface of the ESC substrate support 105 prevents plasma from forming in a volume between the liner 108 and the one or more sidewalls 122.

[0037] The substrate support 105 is typically formed of a dielectric material, such as a bulk sintered ceramic material, such as a corrosion resistant metal oxide or metal nitride material, for example aluminum oxide (Al_2O_3), aluminum nitride (AlN), titanium oxide (TiO), titanium nitride (TiN), yttrium oxide (Y_2O_3), mixtures thereof, or combinations thereof. In embodiments herein, the substrate support 105 further includes a biasing electrode 104 embedded in the dielectric material thereof. In one configuration, the biasing electrode 104 is a chucking pole used to secure (chuck) the substrate 103 to a substrate receiving surface 105A of the substrate support 105, also referred to herein as

an ESC substrate support, and to bias the substrate 103 with respect to the processing plasma 101 using one or more of the pulsed-voltage biasing schemes described herein. Typically, the biasing electrode 104 is formed of one or more electrically conductive parts, such as one or more metal meshes, foils, plates, or combinations thereof. In some embodiments, the biasing electrode 104 is electrically coupled to a bias compensation module 116, which provides a chucking voltage thereto, such as static DC voltage between about -5000 V and about 5000 V, using an electrical conductor, such as the coaxial transmission line 106 (e.g., a coaxial cable). As will be discussed further below, the high voltage module 116 includes bias compensation circuit elements 116A (Figures 3A-3B), a DC power supply 155, and a blocking capacitor 153. A bias compensation module blocking capacitor, which is also referred to herein as the blocking capacitor 153, is disposed between the output of a pulsed-voltage waveform generator (PVWG) 150 and the biasing electrode 104.

[0038] The biasing electrode 104 is spaced apart from the substrate receiving surface 105A of the substrate support 105, and thus from the substrate 103, by a layer of dielectric material of the substrate support 105. Depending on the type of electrostatic chucking method utilized within the substrate support 105 to retain a substrate 103 during processing, such as a coulombic ESC or a Johnsen-Rahbek ESC, the effective circuit elements used to model the electrical coupling of the biasing electrode 104 to the plasma 101 will vary. In general, a parallel plate like structure is formed by the biasing electrode 104 and the layer of the dielectric material that can typically have an effective capacitance C_E of between about 5 nF and about 50 nF. Typically, the layer of dielectric material (e.g., aluminum nitride (AlN), aluminum oxide (Al_2O_3), etc.) has a thickness between about 0.1 mm and about 1 mm, such as between about 0.1 mm and about 0.5 mm, for example about 0.3 mm. Herein, the biasing electrode 104 is electrically coupled to the output of the PVWG 150 using the external conductor, such as the transmission line 106, which is disposed within the support shaft 138. In some embodiments, the dielectric material and layer thickness can be selected so that the chuck capacitance C_{ESC} of the layer of dielectric material is between about 5 nF and about 50 nF, such as between about 7 and about 10 nF, for example.

[0039] In a more complex model of the Johnsen-Rahbek ESC the circuit model includes the combination of the ESC dielectric material chuck capacitance C_{ESC}, ESC dielectric material resistance R_{CER}, gap capacitance C_{abt}, substrate capacitance C_{sub}, and substrate resistance R_{sub} as shown. The gap capacitances C_{abt} will generally account for gas containing spaces above and below a substrate that is positioned on the substrate support 105. It is expected that the gap capacitance C_{abt} has a capacitance in the same range as the chuck capacitance C_{ESC}.

[0040] In some applications, since the substrate 103 is typically made out of a thin layer of a semiconductor material and/or dielectric material, the substrate 103 can be considered to be electrically a part of the ESC dielectric layer disposed between the biasing electrode 104 and the substrate receiving surface 105A. Thus, in some applications, the chuck capacitance C_{ESC} is approximated by the combined series capacitance of the ESC and the substrate (i.e., substrate capacitance C_{sub}). However, in the coulombic chuck case, since the substrate capacitance C_{sub} is typically very large (>10nF), or the substrate may be conductive (infinite capacitance), the series capacitance is determined primarily by the capacitance C_{ESC}. In this case, the effective capacitance C_E is effectively equal to the chuck capacitance C_{ESC}. In the case of a "Johnsen-Rahbek ESC", the ESC dielectric layer is "leaky", in that it is not a perfect insulator and has some conductivity, since, for example, the dielectric material may be a doped aluminum nitride (AlN) having a permittivity (ε) of about 9. However, the effective capacitance of a Johnsen-Rahbek ESC should be similar to a coulombic chuck. In one example, the volume resistivity of the dielectric layer within a Johnsen-Rahbek ESC is less than about 10^{12} ohms-cm (Ω-cm), or less than about 10^{10} Ω-cm, or even in a range between 10^{8} Ω-cm and 10^{12} Ω-cm.

[0041] The substrate support assembly 136 further includes an edge control electrode 115 that is positioned below the edge ring 114 and surrounds the biasing electrode 104 so that when biased, due to its position relative to the substrate 103, it can affect or alter a portion of the generated plasma 101 that is at or outside of the edge of the substrate 103. The edge control electrode 115 can be biased by use of a PVWG 150 that is different from the PVWG 150 that is used to bias the biasing electrode 104. In one

configuration, a first PV waveform generator 150 of a first PV source assembly 196 is configured to bias the biasing electrode 104, and a second PV waveform generator 150 of a second PV source assembly 197 is configured to bias the edge control electrode 115. In one embodiment, the edge control electrode 115 is positioned within a region of the substrate support 105, as shown in Figure 1. In general, for processing chambers 100 that are configured to process circular substrates, the edge control electrode 115 is annular in shape, is made from a conductive material and configured to surround at least a portion of the biasing electrode 104, as shown in Figure 1. In some embodiments, as illustrated in Figure 1, the edge control electrode 115 includes a conductive mesh, foil or plate that is disposed a similar distance (i.e., Z-direction) from the surface 105A of the substrate support 105 as the biasing electrode 104. Alternately, in some other embodiments, the edge control electrode 115 includes a conductive mesh, foil or plate that is positioned on or within a region of the quartz pipe 110 (not shown), which surrounds at least a portion of the biasing electrode 104 and/or the substrate support 105. In some other embodiments, the edge control electrode 115 is positioned within or is coupled to the edge ring 114, which is disposed adjacent to the substrate support 105. In this configuration, the edge ring 114 is formed from a semiconductor or dielectric material (e.g., AlN, Al_2O_3, etc.).

[0042] Referring to Figure 1, the support base 107 is spaced apart from the biasing electrode 104 by a portion of dielectric material. The portion of dielectric material in some configurations is the dielectric material used to form the substrate support 105, and extends from the backside of the substrate support 105 to the biasing electrode 104. The portion of dielectric material of the substrate support 105 has a support base capacitance C_{CL} that is in series with the ESC capacitance C_E, as schematically illustrated in Figures 3A and 3B. In some embodiments, the thickness of the portion of the dielectric material disposed between the support base 107 and the biasing electrode 104 is greater than the thickness of the dielectric material disposed between the biasing electrode 104 and the substrate 103, wherein the dielectric materials are the same material and/or form part of the substrate support 105. In one example, the portion of a dielectric material of the substrate support 105 (e.g., Al_2O_3 or AlN) disposed between support base 107 and the

biasing electrode 104 is greater than 1 mm thick, such as between about 1.5 mm and about 20 mm thick.

[0043] Generally, a low pressure formed in the processing volume 129 of the processing chamber 100 results in poor thermal conduction between surfaces of hardware components disposed therein, such as between the dielectric material of the substrate support 105 and the substrate 103 disposed on the substrate receiving surface thereof, which reduces the substrate support's effectiveness in heating or cooling the substrate 103. Therefore, in some processes, a thermally conductive inert heat transfer gas, typically helium, is introduced into a volume (not shown) disposed between a non-device side surface of the substrate 103 and the substrate receiving surface 105A of the substrate support 105 to improve the heat transfer therebetween. The heat transfer gas, provided by a heat transfer gas source (not shown), flows to the backside volume through a gas communication path (not shown) disposed through the support base 107 and further disposed through the substrate support 105.

[0044] The processing chamber 100 further includes a controller 126, which is also referred to herein as a processing chamber controller. The controller 126 herein includes a central processing unit (CPU) 133, a memory 134, and support circuits 135. The controller 126 is used to control the process sequence used to process the substrate 103 including the substrate biasing methods described herein. The CPU 133 is a general-purpose computer processor configured for use in an industrial setting for controlling processing chamber and sub-processors related thereto. The memory 134 described herein, which is generally non-volatile memory, may include random access memory, read only memory, floppy or hard disk drive, or other suitable forms of digital storage, local or remote. The support circuits 135 are conventionally coupled to the CPU 133 and comprise cache, clock circuits, input/output subsystems, power supplies, and the like, and combinations thereof. Software instructions (program) and data can be coded and stored within the memory 134 for instructing a processor within the CPU 133. A software program (or computer instructions) readable by CPU 133 in the controller 126 determines which tasks are performable by the components in the processing chamber 100. Preferably, the program, which is readable by CPU 133 in the controller 126, includes

code, which, when executed by the processor (CPU 133), performs tasks relating to the monitoring and execution of the electrode biasing scheme described herein. The program will include instructions that are used to control the various hardware and electrical components within the processing chamber 100 to perform the various process tasks and various process sequences used to implement the electrode biasing scheme described herein.

[0045] During processing, the PV generators 314 within the PV waveform generators 150 of the first PV source assembly 196 and the second PV source assembly 197 establishes a pulsed voltage waveform on a load (e.g., the complex load 130) disposed with the processing chamber 100. While not intending to be limiting as to the disclosure provided herein, and to simplify the discussion, the components within the second PV source assembly 197, which are used to bias the edge control electrode 115, are not schematically shown in Figures 3A-3B. The overall control of the delivery of the PV waveform from each of the PV waveform generators 150 is controlled by use of signals provided from the controller 126. In one embodiment, as illustrated in Figure 3A, the PV waveform generator 150A is configured to maintain a predetermined, substantially constant positive voltage across its output (i.e., to ground) during regularly recurring time intervals of a predetermined length, by repeatedly closing and opening its internal switch S_1 at a predetermined rate. Alternately, in one embodiment, as illustrated in Figure 3B, a PV waveform generator 150B maintains a predetermined, substantially constant negative voltage across its output (i.e., to ground) during regularly recurring time intervals of a predetermined length, by repeatedly closing and opening its internal switch S_1 at a predetermined rate. In Figures 3A-3B, the PV waveform generator 150A, 150B is reduced to a minimal combination of the components that are important for understanding of its role in establishing a desired pulsed voltage waveform at the biasing electrode 104. Each PV waveform generator 150 will include a PV generator 314 (e.g., DC power supply) and one or more electrical components, such as high repetition rate switches, capacitors (not shown), inductors (not shown), fly back diodes (not shown), power transistors (not shown) and/or resistors (not shown), that are configured to provide a PV waveform to an output 350, as schematically illustrated in Figures 3A-3B. An actual PV waveform generator 150, which can be configured as a nanosecond pulse generator,

may include any number of internal components and may be based on a more complex electrical circuit than what is illustrated in Figures 3A-3B. The schematic diagrams of Figures 3A-3B each provide only a functionally equivalent representation of the components of the PV waveform generator 150 and its electrical circuitry, in as much as is required to explain the fundamental principle of its operation, its interaction with the plasma in the processing volume, and its role in establishing a pulsed voltage waveform, such as the input pulsed voltage waveform at the biasing electrode 104. As can be inferred from a schematic diagram shown in Figures 3A-3B, when the switch S_1 moves from the open (Off) to the closed (On) position, it connects the output of the PV waveform generator 150 to its PV generator 314 that produces a substantially constant output voltage. The PV waveform generator 150 may be primarily used as a charge injector (current source), and not as a constant voltage source; therefore it is not necessary to impose stringent requirements on the stability of the output voltage, in that it can vary in time even when the switch remains in the closed (On) position. Further, in some configurations, the PV generator 314 is fundamentally a sourcing, but not a sinking supply, in that it only passes a current in one direction (e.g., the output can charge, but not discharge a capacitor). Additionally, when the switch S_1 remains in the open (Off) position, the voltage (V_0), across the output of the PV waveform generator 150 is not controlled by the PV generator 314 and is instead determined by the interaction of its internal components with other circuit elements.

[0046] A current-return output stage 314A has one end connected to ground, and another end connected to a connection point (i.e., one side of a generator coupling assembly (not shown)) at the output of the PV waveform generator 150. The current-return output stage 314A can include the following elements: a resistor, a resistor and an inductor connected in series, a switch S_2, and/or a more complex combination of electrical elements, including parallel capacitors, which permits a positive current flow towards the ground.

[0047] Transmission line 131, which forms part of the PV transmission line 157 (Figures 1), electrically connects the output 350 of the PV waveform generator 150 to the second filter assembly 151. While the discussion below primarily discusses the PV

transmission line 157 of the first PV source assembly 196, which is used to couple a PV waveform generator 150 to the biasing electrode 104, the PV transmission line 158 of the second PV source assembly 197, which couples a PV waveform generator 150 to the edge control electrode 115, will include the same or similar components. Therefore, in general, the output 350 of the PV waveform generator 150 is the end, where the output of the PV pulse generator 314 is connected through the internal electrical conductor to the output 350 and to the current-return output stage 314A. The transmission line 131 connects a generator coupling assembly 181, which is positioned at the output 350 of the PV waveform generator 150, to the second filter assembly 151. The electrical conductor(s) within the various parts of the PV transmission line 157, 158 may include: (a) a coaxial transmission line (e.g., coaxial line 106), which may include a flexible coaxial cable that is connected in series with a rigid coaxial transmission line, (b) an insulated high-voltage corona-resistant hookup wire, (c) a bare wire, (d) a metal rod, (e) an electrical connector, or (f) any combination of electrical elements in (a) – (e). The external conductor portion (e.g., first electrical conductor) of the PV transmission line 157, such as the portion of PV transmission line 157 within the support shaft 138 and the biasing electrode 104, will have some combined stray capacitance C_{stray} (Figures 3A-3B) to ground. While not shown in the figures, the external conductor portion (e.g., second electrical conductor) of the PV transmission line 158 and the edge control electrode 115 will also have some combined stray capacitance C_{stray} to ground. The internal electrical conductor of the PV waveform generator 150 may include the same basic elements as the external electrical conductor. In most practical applications, the transmission line 131 will include a line inductance 159 which can include a portion that is created by the internal components of the PV waveform generator 150 (i.e., left side of the generator output coupling assembly 181 (Figures 3A-3B)) and/or a portion that is created by the external line/cables (i.e., right side of the generator output coupling assembly 181) that connect the PV waveform generator 150 to the second filter assembly 151.

[0048] Referring back to Figure 1, the processing chamber 100 includes a chamber lid 123 that is grounded. In this configuration, which is generally different from conventional plasma processing chamber designs, the RF power is instead delivered through the substrate support. Thus, by coupling the RF generator 118 to the support

base 107, the entire body of the ESC, which is functionally part of the cathode assembly, enables the top electrode to be grounded and allows the current-return area to be maximized. For plasma processes that utilize RF power delivery and PV waveform delivery, maximizing the grounded surface area within the plasma processing chamber, and hence the current-return area, minimizes the plasma potential jump during the ESC-recharging/sheath-collapse phase of the PV waveform cycle generated by the output of the PV waveform generator 150, which are discussed further below. Thus, the apparatus and methods provided herein will minimize the power losses to chamber walls and improves the plasma processing efficiency. The RF power and PV pulsed waveform delivery methods described herein also provides certain process benefits as they impact and allow for an improved control of the plasma properties and radical production. However, as noted above, there is a strong capacitive coupling between the support base 107 and the biasing electrode 104 through the ESC ceramic layer as well as between the RF transmission line 167 and PV transmission line 157, so when both types of power are delivered through the substrate support assembly 136 (i.e., cathode assembly), each generator will induce the current through the other, resulting in the power being diverted away from the intended (plasma) load as well as a possible damage to both generators.

[0049] In another alternate chamber lid 123 configuration, which can be used with one or more of the other embodiments disclosed herein, the chamber lid 123 (i.e., opposing electrode) is electrically isolated from the one or more sidewalls 122 and is electrically coupled to an RF generator 118 through a plasma generator assembly 160. In this configuration, the chamber lid 123 can be driven by a RF generator 118 to ignite and maintain a processing plasma 101 within the processing volume 129. In one example, a RF generator 118 is configured to provide an RF signal at an RF frequency greater than about 300 kHz to the chamber lid 123, such as between about 300 kHz and 60 MHz, or even a frequency in range from about 2 MHz to about 40 MHz.

Plasma Processing Biasing Schemes and Processes

[0050] Figure 2 is a simplified schematic diagram of a biasing scheme that can be used with the process chamber illustrated in Figure 1. As shown in Figure 2, the RF

generator 118 and PV waveform generators 150 are configured to deliver an RF waveform and pulsed-voltage waveforms, respectively, to one or more electrodes disposed within the chamber body 113 of the processing chamber 100. In one embodiment, the RF generator 118 and PV waveform generators 150 are configured to simultaneously deliver an RF waveform and pulsed-voltage waveform(s) to one or more electrodes disposed within the substrate support assembly 136. In one non-limiting example, as discussed above, the RF generator 118 and a PV waveform generator 150 are configured to deliver an RF waveform and pulsed-voltage waveform to the support base 107 and biasing electrode 104, respectively, which are both disposed in the substrate support assembly 136. In another example, the RF generator 118, a first PV waveform generator 150 and a second PV waveform generator 150 are configured to deliver an RF waveform, a first pulsed-voltage waveform and a second pulsed-voltage waveform to the support base 107, the biasing electrode 104 and the edge control electrode 115, respectively, which are all disposed in the substrate support assembly 136.

[0051] As illustrated in Figure 2, the RF generator 118 is configured to provide a sinusoidal RF waveform to the one or more electrodes disposed in the chamber body 113 by delivering the RF signal, which includes the sinusoidal RF waveform 601 (Figures 6A-6G), through the plasma generator assembly 160, which includes the RF matching circuit 161 and the first filter assembly 162. Additionally, each of the PV waveform generators 150 are configured to provide a PV waveform, which typically includes a series of voltage pulses (e.g., nanosecond voltage pulses), to the one or more electrodes disposed in the chamber body 113 by establishing a PV waveform 401 (Figures 4A, 5A), 441 (Figure 5B), or 431 (Figure 5C) at the biasing electrode 104 through the second filter assembly 151. The components within the bias compensation module 116 can be optionally positioned between each PV waveform generator 150 and the second filter assembly 151.

[0052] As briefly discussed above, Figures 3A-3B are each examples of a functionally equivalent, simplified electrical circuit 140 of the pulsed voltage and RF biasing scheme proposed herein, which also includes a representation of the plasma in the process

volume. Figure 3A depicts a simplified electrical circuit 140 of a pulsed voltage and RF biasing scheme that utilizes a PV waveform generator 150, within the first PV source assembly 196, that is configured to provide a positive voltage during a portion of the process of establishing the PV waveform at the biasing electrode 104, such as PV waveform 431 (Figure 4C). Figure 3B depicts a simplified electrical circuit 140 of a pulsed voltage and RF biasing scheme that utilizes a PV waveform generator 150, within the first PV source assembly 196, that is configured to provide a negative voltage during a portion of the process of establishing the PV waveform at the biasing electrode 104, such as PV waveform 401 (Figure 4A). These circuits illustrate a simplified model of the interaction of a pulsed-voltage waveform generator 150 of the first PV source assembly 196 and RF generator 118 within the processing chamber 100, and generally illustrate the basic elements used during operation of the process chamber 100. For clarity purposes, the following definitions are used throughout this disclosure: (1) unless a reference is specified, all potentials are referenced to ground; (2) the voltage at any physical point (like a substrate or a biasing electrode) is likewise defined as the potential of this point with respect to ground (zero potential point); (3) the cathode sheath is implied to be an electron-repelling, ion-accelerating sheath that corresponds to a negative substrate potential with respect to plasma; (4) the sheath voltage (also referred to sometimes as "sheath voltage drop"), V_{sh}, is defined as the absolute value of the potential difference between the plasma and the adjacent surface (e.g. of the substrate or the chamber wall); and (5) the substrate potential is the potential at the substrate surface facing the plasma.

[0053] The complex load 130 illustrated in Figures 3A-3B is shown as a standard electrical plasma model that represents the processing plasma 101 as three series elements. The first element being an electron-repelling cathode sheath (which we sometimes also refer to as the "plasma sheath" or just the "sheath") adjacent to the substrate 103. The cathode sheath is represented in Figures 3A-3B by a conventional three-part circuit element comprising: (a) the diode D_{SH}, which when open represents the sheath collapse, (b) the current source I_i, representing the ion current flowing to the substrate in the presence of the sheath, and (c) the capacitor C_{SH} (e.g., ~100-300 pF), which represents the sheath for the main portion of the biasing cycle (i.e., ion current

phase of the PV waveform), during which the ion acceleration and the etching occur. The second element being a bulk plasma, which is represented by a single resistor R_{plasma} (e.g., resistor 146 = ~ 5 – 10 Ohms). The third element being an electron-repelling wall sheath forming at the chamber walls. The wall sheath is likewise represented in Figure 3 by a three-part circuit element comprising: (a) the diode D_{wall}, (b) the current source I_{iwall} representing the ion current to the wall, and (c) the capacitor C_{wall} (e.g., ~5 – 10 nF), which represents the wall sheath primarily during the ESC recharging phase of the PV waveform (described later in the text). The interior surface of the grounded metal walls can also be considered to be coated with a thin layer of a dielectric material, which is represented in Figure 3 by a large capacitor C_{coat} (e.g., ~300-1000nF).

[0054] As illustrated in Figure 3A-3B, the RF generator 118 is configured to provide an RF signal to the support base 107, and eventually the complex load 130, by delivering the generated RF power through the first filter assembly 162, the RF matching circuit 161, line inductance L_{Line}, support base capacitance C_{CL}, and effective capacitance C_E. In one embodiment, the RF matching circuit 161 includes a series inductance element L_{SER}, and an adjustable series capacitance element C_{SER} and an adjustable shunt capacitance element C_{Shunt} that can be controlled by input from the controller 126. In some embodiments, the RF matching circuit 161 may alternately be formed by use of other circuit element configurations, such as L network, pi network, or transmatch circuits, for example. As noted above, the RF matching circuit 161 is generally configured to tune the apparent load to 50Ω to minimize the reflected power generated by the delivery of the RF signal from the RF generator 118 and maximize its power delivery efficiency. In some embodiments, the RF matching circuit 161 is optional, and in these cases other RF signal matching techniques may be used (e.g., variable frequency tuning) during a plasma processing of a substrate to avoid the inefficient delivering RF power to the complex load 130.

[0055] The first filter assembly 162 includes one or more electrical elements that are configured to substantially prevent a current generated by the output of the PV waveform generator 150 from flowing through the RF transmission line 167 and damaging the RF generator 118. The first filter assembly 162 acts as a high impedance (e.g., high Z) to

the PV signal generated from the PV pulse generator 314 within the PV waveform generator 150, and thus inhibits the flow of current to the RF generator 118. In one embodiment, the first filter assembly 162 includes a blocking capacitor C_{BC}, which is disposed between the RF matching circuit 161 and the RF generator 118. In this configuration, the RF matching element 161 is configured to compensate for the capacitance of the blocking capacitor C_{BC} as it tunes the load apparent to the RF generator 118. In one example, to prevent a nanosecond PV waveform (e.g., pulse period 10-100 ns) provided from the PV waveform generator 150 from damaging the RF generator 118 the first filter assembly 162 includes a 38-40 pF capacitor. In another example, the first filter assembly 162 includes a blocking capacitor C_{BC} that has a capacitance that is less than 38 pF.

[0056] In some embodiments, as shown in Figures 1-3B, each of the PV waveform generators 150 are configured to provide a pulsed voltage waveform signal to the biasing electrode 104, and eventually the complex load 130, by delivering the generated pulsed voltage waveforms through the blocking capacitor 153 of the high-voltage module 116 and second filter assembly 151, high-voltage line inductance L_{HV}, and effective capacitance C_E. In this case, the system optionally includes a bias compensation module 116 used for chucking, such as "electrically clamping", the substrate to the substrate receiving surface of the ESC substrate support. Chucking the substrate allows filling a gap between the substrate receiving surface and the non-device side surface of the substrate with helium gas (He), which is done in order to provide good thermal contact between the two and allow substrate temperature control by regulating the temperature of the ESC substrate support. Combining a DC chucking voltage produced by the bias compensation module 116 with the pulsed voltage produced by the PV waveform generator 150 at a biasing electrode 104 will result in an additional voltage offset of the pulsed voltage waveform equal to the DC chucking voltage. The additional voltage offset can be added or subtracted from the offset ΔV illustrated in Figures 4A-4B. The effect of the bias compensation module 116 on the operation of the PV pulse generator 314 of the PV waveform generator 150 can be made negligible by selecting appropriately large blocking capacitor 153 and blocking resistor 154. The blocking resistor 154 schematically illustrates a resistor positioned within the components connecting the bias compensation

module 116 to a point within the transmission line 131. The value of blocking capacitor 153 is selected such that while blocking only the bias compensation module DC voltage, it does not present any load to the pulsed bias generator's pulsed voltage output. In one example, the capacitance of blocking capacitor C_{BC} is about 38 pF and the capacitance of the blocking capacitor 153 is about 40 nF. This blocking resistor 154 is typically sized to be large enough to efficiently minimize the current through it. For example, a resistance of ≥1 MOhm is used to make a 400 kHz current from the PV waveform generator 150 into the bias compensation module 116 negligible. In one example, the blocking resistor has a resistance of more than about 500 kOhm. The resultant average induced current of the order of 0.5 – 1 mA is indeed much smaller than a typical limitation for bias compensation module power supplies, which is about 5 mA DC current.

[0057] The second filter assembly 151 includes one or more electrical elements that are configured to prevent a current generated by the output of the RF generator 118 from flowing through PV transmission line 157 and damaging the PV pulse generator 314 of the PV waveform generator 150. As discussed above, the PV transmission line 157 is an assembly that includes the coaxial transmission line 106 and transmission line 131. In one embodiment, the second filter assembly 151 includes a filter capacitor 151A, which has a capacitance C_{FC}, and a filter inductor 151B, which has an inductance L_{FL}, that are connected in parallel, and are disposed in the transmission line 157 between the PV pulse generator 314 and the biasing electrode 104. In some configurations, the second filter assembly 151 is disposed between the blocking capacitor 153 of the bias compensation module 116 and the biasing electrode 104. The second filter assembly 151 acts as a high impedance (e.g., high Z) to the RF signal generated from the RF generator 118, and thus inhibits the flow of current to the PV pulse generator 314. In general, the second filter assembly 151 is configured to block the RF signal, and any associated harmonics from making their way to the PV pulse generator 314. In some embodiments, the RF signal generated by the RF generator is configured to deliver an RF frequency greater than 400 kHz, such an RF frequency ≥1 MHz, or ≥2 MHz, or ≥13.56 MHz, or ≥40 MHz. In one example, to prevent RF power provided from the RF generator 118 at a frequency of 40 MHz from damaging the PV pulse generator 314 the second

filter assembly 151 includes a filter capacitor 151A that has a capacitance of about 51 pF and a filter inductor 151B that has an inductance of about 311 nH.

Pulse Waveform Examples

[0058] As noted above, embodiments of the disclosure provide novel substrate biasing methods that enable the maintaining of a nearly constant sheath voltage during processing, and thus creating a desired IEDF at the surface of the substrate, while also providing the ability to separately control aspects of the plasma formed in the processing volume of the plasma processing chamber by use of one or more RF source assemblies. In some embodiments, by use of the novel substrate biasing apparatus and methods disclosed herein, a single-peak (mono-energetic) IEDF can be formed at the surface of the substrate during processing. In other embodiments, a two-peak (bi-energetic) IEDF is formed at the surface of the substrate during processing by use of one or more of the novel substrate biasing apparatus and methods disclosed herein.

[0059] As is discussed further below in relation to Figures 4A-4C, the novel substrate biasing methods, which enable the maintaining of a nearly constant sheath voltage during plasma processing, include the delivery of a series of pulses and/or bursts of pulses during a plasma processing sequence performed on a substrate during a plasma process performed in the plasma processing chamber. Embodiments of the disclosure provided herein include the delivery of pulses that have a desired PV waveform, which each include multiple different phases. As is discussed further below, each PV waveform includes at least one phase of the multiple phases that are controlled by the delivery of a voltage signal, or in some cases a constant current signal, provided from the PV waveform generator 150. Generally, for discussion purposes, each pulse of a PV waveform can be segmented into two main regions, which include a first region 405 and a second region 406, as illustrated in Figures 4A-4C. In general, each PV waveform will include an amplitude (V_{out}), offset (e.g., ΔV), a pulse period (T_P), and a pulse repetition frequency ($f_P = 1/T_P$).

[0060] In some embodiments, the PV waveform is separately established at the biasing electrode 104 and edge control electrode 115 by use of the PV waveform

generator 150 of a first PV source assembly 196 and the PV waveform generator 150 of a second PV source assembly 197, respectively. Figure 4A illustrates a negative-pulse biasing scheme type of pulsed voltage waveform in which the PV waveform generators 150 are configured to control the generation of a series 550 of multiphase negative pulse waveforms 401 to establish the PV waveform at the biasing electrode 104 or edge control electrode 115. In some embodiments, the multiphase negative pulse waveforms 401 include a series of repeating cycles, such that a waveform within each cycle has a first portion that occurs during a first time interval and a second portion that occurs during a second time interval. The multiphase negative pulse waveforms 401 will also include a positive voltage that is only present during at least a portion of the first time interval, and the pulsed voltage waveform is substantially constant during at least a portion of the second time interval. An output of the PV waveform generator 150 is connected to a negative voltage supply for at least a portion of the second time interval.

[0061] Referring to Figures 4A and 4D, in one example, a substrate PV waveform 425 is a series of PV waveforms established at the substrate due to the established PV waveform formed at the biasing electrode 104 or edge control electrode 115 by a PV waveform generator 150. The substrate PV waveform 425 is established at the surface of a substrate during processing, and includes a sheath collapse and ESC recharging phase 450 (or for simplicity of discussion the sheath collapse phase 450) that extends between point 420 and point 421 of the illustrative substrate PV waveform 425, a sheath formation phase 451 that extends between point 421 and point 422, and an ion current phase 452 that extends between point 422 and back to the start at point 420 of the next sequentially established pulse voltage waveform. The plasma potential curve illustrates the local plasma potential during the delivery of the negative pulse waveforms 401 that are established at the biasing electrode 104 and/or edge control electrode 115 by use of one or more PV waveform generators 150.

[0062] In this example, during processing in the processing chamber 100, a multiphase negative pulse waveform 401 (Figure 4A) is formed when a PV waveform generator 150 supplies and controls the delivery of a negative voltage during two of the phases of the established multiphase negative pulse waveform 401, such as the portions

of the PV waveform that trend in a negative direction and/or are maintained at a negative voltage level (e.g., ion current phase). For example, these negative voltage-containing portions of the negative pulse waveform 401 would, by analogy, relate to the sheath formation phase 451 and the ion current phase 452 for the substrate PV waveform 425. In this case, for a multiphase negative pulse waveform 401, the delivery of a negative voltage from a PV waveform generator 150 occurs during the second phase 406, which extends from or between the point 411 (i.e., peak of multiphase negative pulse waveform 401) and the start of the sheath collapse phase 450 of the substrate PV waveform that coincides with point 413. In some embodiments, during the ion current phase 452, which coincides with the portion of the established multiphase negative pulse waveform 401 that is between points 412 and 413, the PV waveform generator 150 is configured to provide a constant negative voltage (e.g., V_{OUT}). Due to, for example, the ion current (I_i) depositing positive charge on the substrate surface during the ion current phase 452, the voltage at the substrate surface will increase over time, as seen by the positive slope of the line between points 422 and 420. The voltage increase over time at the substrate surface will reduce the sheath voltage and result in a spread of the ion energy. Therefore, it is desirable to control and set at least the PV waveform frequency ($1/T_{PD}$, where T_{PD} is PV waveform period (Figure 5A)) to minimize the effects of the reduction in the sheath voltage and spread of the ion energy.

[0063] By delivering and controlling the PV waveforms provided to the biasing electrode 104 during plasma processing, a desirable ion energy distribution function (IEDF) can be formed, such as a nearly monoenergetic IEDF. The generation and control of the characteristics of the PV waveforms (e.g., peak-to-peak voltage, duty cycle, frequency, etc.) allows for the precise control of the plasma ion density and generated ion energies, and also results in a more controllable fluorinated carbon (C_xF_y) based polymer deposition on a conductive material (e.g., W) surface found at the bottom of an etched feature. The formation of the polymer deposition on the conductive material surface will improve the etch selectivity of the dry etch chemistry to the conductive material versus an intervening etched dielectric material.

[0064] Figure 4B illustrates a shaped-pulse biasing scheme type of PV waveform in which the PV waveform generator 150 is configured to control the generation of a series 551 of multiphase shaped pulse waveforms 441 that are established at the biasing electrode 104 and/or edge control electrode 115. In some embodiments, the multiphase shaped pulse waveform 441 is formed by a PV waveform generator 150 that is configured to supply a positive voltage during one or more phases of a voltage pulse (e.g., first region 405) and a negative voltage during one or more phases of the voltage pulse (e.g., second region 406) by use of one or more internal switches and DC power supplies.

[0065] In some embodiments, as illustrated in Figure 4C, the PV waveform generator 150 is configured to provide a series 552 of multiphase positive pulse waveforms 431 to the biasing electrode 104 and edge control electrode 115. Each positive pulse in the positive pulse waveform 431 can include multiple phases, such as a sheath collapse phase, ESC recharging phase, a sheath formation phase and an ion current phase. In this example, the first region 405 generally includes the sheath collapse phase and ESC recharging phase. The second region 406 generally includes the sheath formation phase and the ion current phase. In some embodiments, the multiphase positive pulse waveforms 431 includes a series of repeating cycles, such that a waveform within each cycle has a first portion that occurs during a first time interval and a second portion that occurs during a second time interval. The multiphase positive pulse waveforms 431 will also include a positive voltage that is only present during at least a portion of the first time interval, and the multiphase positive pulse waveforms 431 is substantially constant during at least a portion of the second time interval. An output of the PV waveform generator 150 is connected to a positive voltage supply for at least a portion of a first time interval.

[0066] The various pulse voltage waveforms 401, 441 and 431 illustrated in Figures 4A, 4B and 4C, respectively, are representative of pulse voltage waveforms that are provided to the input of the bias compensation module 116, and thus may differ from the pulse voltage waveforms that are established at the biasing electrode 104 and edge control electrode 115. The DC offset ΔV found in each PV waveform is dependent on various properties of the PV waveform generator 150 configuration used to establish the PV waveform.

[0067] In some embodiments, a series of bursts of at least one or more types of pulse voltage waveforms 401, 441, and/or 431 are established at the biasing electrode 104 and/or edge control electrode 115 and established at the substrate surface. In one example, a plurality of pulses within each burst include a series of negative pulse waveforms 401 that are established at the biasing electrode 104 and/or edge control electrode 115. In one example, each of the bursts of pulse voltage waveforms include pulses that have a waveform that has a consistent pulsed voltage shape (e.g., constant voltage magnitude is provided during a portion of each PV waveform 401), a burst delivery length T_{ON} that may vary from one burst to another over time, and a burst rest length T_{OFF} that may also varying length over time. The burst rest length T_{OFF} is formed by halting the delivery of the PV waveforms provided during the burst delivery length T_{ON} time for a period of time. The duty cycle of the bursts, which is the ratio of the length of time the plurality of pulses are delivered during the burst (i.e., burst delivery length T_{ON}) divided by the duration of a burst period (i.e., $T_{BD} = T_{ON} + T_{OFF}$), may be constant or be varied over time. One will appreciate that in other processing methods, the plurality of pulses could include negative pulse waveforms 401, shaped pulse waveforms 441 or positive pulse waveforms 431, or combinations thereof.

Example Selectivity of Etching of Silicon Dioxide

[0068] As mentioned previously, plasma etching processes involved in the fabrication of 3D NAND devices are becoming increasingly challenging. Specifically, the staircase contact etch in 3D NAND technology provides access to cells at the bottom of the NAND stack thereby allowing the formed conductive material layers (e.g., tungsten containing layers) buried in the NAND stack to form portions of word-lines that allow access to the cell control gates from the outside peripheral circuitry.

[0069] Figure 5 illustrates the results of a staircase contact etch process performed on a substrate, according to certain embodiments described herein. According to one embodiment, the substrate 500 includes a mask layer 505 and a multilayer stack 501 that includes a plurality of conductive layers 520 and a plurality of intervening dielectric material layers disposed therebetween. The plurality of intervening dielectric material

layers and dielectric material disposed adjacent to portions of the conductive layers 520 are collectively described and referred to herein as a dielectric material 510. The mask layer 505 includes a pre-etching pattern that is formed based on customer specifications by use of lithography and mask etch process. The patterned mask layer 505 guides the formation of the features, such as trenches 515, formed during the plasma etching process (as illustrated in Figure 6A). The multilayer stack 501 includes multiple conductive layers 520, and the conductive layers 520 formed a staggered arrangement so that each of the trenches 515 formed during the plasma etching process described herein reaches each of the conductive layers 520 that are positioned at different depths (Z-direction) within the multilayer stack 501. As illustrated in Figure 5, each of the trenches 515 formed during the plasma etching process, due to pattern formed in the mask layer 505 have a different depth and contact a different conductive layer 520. Each of the trenches 515 formed during the plasma etching process also do not extend through the corresponding conductive layer 520.

[0070] In some embodiments, the conductive layers 520 disposed in the dielectric material 510 of the multilayer stack 501 may be composed of tungsten, platinum, titanium, ruthenium, silicon, molybdenum, cobalt and hafnium.

[0071] Figures 6A-6C each illustrate a portion of a multilayer stack 501 during different phases of a plasma etching process used to form the trenches 515 in a staircase contact structure within a portion of a substrate, according to certain embodiments described herein. Figure 6A illustrates the substrate with a patterned mask layer 505 formed prior to the plasma etching process used to form trenches 515, which for discussion purposes is referred to herein as a time T_0. The pre-etching of the mask layer 505 demarcates where the etching is intended to occur within the dielectric layer 510 during the subsequent plasma etching process.

[0072] Figure 6B illustrates the substrate 500 during the plasma etching process when the plasma process has contacted a conductive layer 520 of the substrate 500. In this example, as shown in Figure 6B, the plasma etching process has formed two trenches in the dielectric layer 510 due to pattern formed in the mask layer 505. During the plasma

etching process, the plasma (e.g., plasma 530 of Figure 7) formed in the plasma processing chamber interacts with the dielectric material 510 through the patterned mask layer 505, and after a period of time forms the trenches 515 within the dielectric material 510. Because of the composition of the mask layer 505 and the composition of the plasma chemistry, used during the etching process, are selected such that minimal etching will occur during processing, the plasma does not etch the mask layer 505 and only etches the dielectric material 510 exposed through the patterned mask layer 505. Each of the trenches 515 have the same depth at this point in time, which for discussion purposes is referred to herein as a time T_1, during the plasma etching process. In some embodiments, the plasma etching process operates in the manner described above.

[0073] Figure 6C illustrates the substrate 500 at the completion of the plasma etching process, which for discussion purposes is referred to herein as a time T_2. The plasma etching process continues to etch into the dielectric material 510 within the trenches 515, which were demarcated by the patterned mask layer 505. Because of the composition of the conductive layer 520 and the need for certain compositions of the plasma chemistry to perform the etch process, the conductive layer 520 will experience some undesirable etching while the plasma etching process continues on after the conductive layer 520 is first exposed at time T_1 (as illustrated in Figure 6C). The rate of etching into the conductive layer 520 is much smaller than the rate of etching into the dielectric material 510. Accordingly, the plasma etching process etches into the dielectric material 510 to form trenches in the dielectric material 510 until the plasma 530 reaches one or more conductive layers 520 within the multilayer stack 501 or the base layer 525 of the substrate 500. When the plasma 530 reaches one or more conductive layers 520 or the base layer 525 of the substrate 500, the rate of etching decreases while the rate of etching through the dielectric material 510 stays the same until another conductive layer or the base layer 525 of the substrate 500 is reached.

[0074] As mentioned above, the plasma etching process etches into the dielectric material 510 to form trenches in the dielectric material 510 until the plasma 530 reaches one or more conductive layers 520. When the plasma 530 etches through the dielectric material 510 and reaches a conductive layer 520, due to the use of a desirable dry etch

chemistry during the plasma etching process, the rate of etching decreases or is inhibited due to a selectivity of the etch chemistry composition to the materials in the conductive layer 520 to the dielectric material 510. As discussed further below, the dry etch chemistry, or process gas, can include a fluorocarbon-containing gas (e.g., C_xF_y) and an additional non-fluorocarbon-containing process gas. The interface formed at the surface of the conductive layer 520 may be composed of a polymer material that is formed by the exposure of the dry etch chemistry to the conductive layer material found at the bottom of the etched feature. For example, if the one or more conductive layers 520 is made from tungsten (W), then the plasma etching process forms a polymer material on the surface of the tungsten material, and thus protects the otherwise exposed surface. In some examples, the interface formed is a fluorocarbon-based polymer deposited on the surface of the one or more conductive layers 520 for better protection against plasma radical etching. The interface may be formed on each of the one or more conductive layers 520 that are disposed at different depths within the substrate as the dry etching plasma process progresses. The formation of one or more interfaces on the one or more conductive layers helps with the etching selectivity. That is, the plasma etching process involves selectively etching the dielectric material 510 and avoids etching into the one or more conductive layers 520 by forming an interface on the etched surface of the one or more conductive layers 520. In some examples, the formation of the interface(s) on the one or more conductive layers 520 facilitates etching selectivity of the substrate, such that the plasma 530 (as illustrated in Figure 7) selectively etches into the dielectric material 510 of the substrate 500 and not into the one or more conductive layers 520 or other underlying materials layers.

[0075] Figure 7 illustrates the enhanced etching selectivity of the plasma etching process, according to one example. During the ESC recharging phase of a PV waveform (e.g., a portion of positive jump within a PV pulse (FIG. 4D)), the sheath thickness of the plasma 530 decreases and the substrate 500 will undergo plasma radical etching, or etching that is primarily caused by radicals versus ions which tends to be more isotropic. During plasma radical etching, fluorocarbon radicals are deposited into the trenches 515 of the substrate 500, and thus the plasma radicals are advantageously used to form a polymer deposition on the surface of the one or more conductive layers 520. Once the

ESC recharging phase ends, the sheath of the plasma 530 forms and during the ion current phase (FIG. 4D), the substrate 500 undergoes plasma ion etching, or etching that is primarily caused by ions versus radicals which tends to be more anisotropic.

[0076] Figure 8 includes a curve 801 that illustrates a graph of the sheath thickness during the plasma etching process, according to one embodiment. The sheath thickness varies as the PV waveform 401, which is illustrated in Figure 4D, varies as a function of time. Specifically, during the ESC recharging phase 450, the sheath thickness decreases and the substrate may undergo plasma radical etching, or etching primarily caused by radicals versus ions which tends to be more isotropic. Once the ESC recharging phase 450 ends, the sheath forms during the sheath formation phase 451, and during the ion current phase 452 the substrate undergoes plasma ion etching, or etching that is primarily caused by ions versus radicals which tends to be more anisotropic. During the ion current phase 452, the thickness of the sheath may decrease in line with the increase of wafer voltage during the ion current phase 452.

[0077] Figure 9 is a flow diagram illustrating example operations 900 for processing a substrate in a plasma processing chamber, in accordance with certain embodiments of the present disclosure. The operations 900 may be performed, for example, in a plasma processing chamber (e.g., such as the plasma processing chamber 100 in Figure 1).

[0078] The operations 900 may begin, at operation 905, by positioning substrate, which includes a patterned mask layer and a first dielectric material formed thereon, on a substrate supporting surface of a substrate support assembly disposed within a processing region of the plasma processing chamber. Operation 905 generally includes the operations performed in operations 910-920, which can be performed in any order, but will generally be performed simultaneously for most of the time that operation 905 is performed.

[0079] At operation 910, the plasma etching process involves delivering a dry etch chemistry into the processing region of the plasma processing chamber. The dry etch chemistry may include a first fluorocarbon-containing gas (e.g., C_xF_y such as C_4F_6, C_3F_6, etc.) and a first process gas. Delivering the dry etch chemistry into the processing region

of the plasma processing chamber involves delivering two or more gases selected from including, but are not limited to, N_2 gas at a first flow rate, krypton (Kr) gas at a second flowrate, C_4F_6 gas at a third flowrate, C_3F_6 gas at a fourth flowrate, and O_2 gas at a fifth flowrate. The plasma etching process will also include controlling the chamber pressure, substrate support temperature, roof temperatures, and support helium (He) pressure. The first flowrate of N_2 may range between 5 sccm to 1000 sccm. The second flow rate of Kr may range between 5 sccm to 1000 sccm. The third flow rate of C_4F_6 may range between 5 sccm to 1000 sccm. The fourth flow rate of C_3F_6 may range between 5 sccm to 1000 sccm. The fifth flow rate of O_2 may range between 5 sccm to 1000 sccm. The plasma etching process will also include controlling the chamber pressure within a range between 1 mTorr to 500 mTorr. The plasma etching process will also include controlling the substrate support temperature within a range of between -80 to 500°C. The plasma etching process will also include controlling the roof temperature within a range between 10°C to 500°C. The plasma etching process may also include controlling the He pressure within a range between 0-100Torr. In one example, the plasma etching process includes delivering a process gas that has a composition formed by creating a C_4F_6 gas flowrate to C_3F_6 gas flowrate ratio of about 4, a C_4F_6 gas flowrate to O_2 gas flowrate ratio of about 2, a C_4F_6 gas flowrate to N_2 gas flowrate ratio of about 1.1, and a C_4F_6 gas flowrate to Kr gas flowrate ratio of about 0.7 at a chamber pressure of between about 1 mTorr and 40 mTorr.

[0080] At operation 915, the plasma etching process involves delivering, by use of a radio frequency generator, a radio frequency signal to a first electrode disposed within the plasma processing chamber to form a plasma in the processing region. Delivering the radio frequency signal to the first electrode disposed within the plasma processing chamber to form a plasma involves parameters including, but are not limited to: source power and frequency. The RF source power may range between 500W to 5000W at a frequency of >400 kHz, such as 2 MHz, or 13.56 MHz, or 40 MHz, or 60 MHz.

[0081] At operation 920, the plasma etching process involves establishing, by use of a first pulsed-voltage waveform generator, a first pulsed voltage waveform at a biasing electrode within the substrate support assembly. The first pulsed voltage waveform may

involve a series of repeating pulsed waveform cycles. Each pulsed waveform cycle includes a first portion that occurs during first time interval (810 in FIG 8) and a second portion that occurs during a second time interval (811 in FIG 8), and the second time interval is larger than the first time interval. Each pulsed waveform cycle also includes a peak-to-peak voltage. The pulsed voltage waveform output from the first pulsed-voltage waveform generator is substantially constant during at least a portion of the second time interval. The first time interval of each pulsed waveform cycle may include the sheath collapse phase, the ESC recharging phase, and the sheath formation phase. The second time interval of each pulsed waveform cycle may include the ion current phase. In some examples, the plasma etching process involves plasma radical etching during the first time interval, and plasma ion etching during the second time interval. The plasma etches through dielectric material via plasma ion etching during the second time interval of each pulsed waveform, and the plasma etches into the one or more conductive layers via plasma radical etching during the first time interval of each pulsed waveform.

[0082] Delivering the pulsed-voltage waveform to the biasing electrode 104 disposed within the plasma processing chamber involves delivering a pulsed voltage waveform having parameters including, but are not limited to: PVT bias power, duty cycle, pulse frequency, peak-to-peak voltage and flow ratio control (FRC). The bias power may range between 500W to 500,000W. The duty cycle may range between 0 to 100%, such as between about 1 and 99%, or even between 5% and 20% for a PV waveform generator 150 that is configured to provide a positive output voltage during the generation of the positive pulse waveforms 431, or a duty cycle of between 50% and 98% for a PV waveform generator 150 that is configured to provide a negative output voltage during the generation of the negative pulse waveforms 401. The pulse frequency may range between 1 to 1000 kHz, such as between about 10 kHz and about 500 kHz, or between about 50 kHz and 400 kHz, or even between about 50 kHz and 200 kHz. The FRC may range between 0 to 100% for all the FRC channel. The peak-to-peak voltage of each of the PV waveforms, generated by the PV waveform generator 150, within a series of PV waveforms is between 0.5 kV and 20 kV, such as between about 2 kV and 20 kV, or between about 5 kV and 9 kV, or between about 5 kV and 8 kV. It has been found that higher peak-to-peak voltages increase the feature etch-rate, and also, surprisingly,

improve the selectivity to etching tungsten using the dry etch chemistries, described in operation 910 and the other processing parameters disclosed herein, such as in operations 915 and 920.

[0083] The operations 900 may be completed for a desired period of time, or until a desired endpoint is sensed within the plasma processing chamber, so that an etching process can be performed through one or more layers of a multilayer stack, such as the process(es) discussed above in relation to Figures 5-6C. In some embodiments, one or more of the software algorithms within the controller 126 are used to monitor, control and/or implement the processes performed within operation 900.

[0084] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method of processing a substrate in a plasma processing chamber, comprising:

etching a first dielectric material formed on a substrate that is disposed on a substrate supporting surface of a substrate support assembly disposed within a processing region of the plasma processing chamber, wherein etching the first dielectric material comprises:

delivering a process gas to the processing region of the plasma processing chamber, wherein the process gas comprises a first fluorocarbon containing gas and a first process gas;

delivering, by use of a radio frequency generator, a radio frequency signal to a first electrode disposed within the plasma processing chamber to form a plasma in the processing region; and

establishing, by use of a first pulsed-voltage waveform generator, a first pulsed voltage waveform at a biasing electrode disposed within the substrate support assembly, wherein the first pulsed voltage waveform comprises a series of repeating pulsed waveform cycles, wherein

each pulsed waveform cycle comprises:

a first portion that occurs during a first time interval and a second portion that occurs during a second time interval, wherein the second time interval is larger than the first time interval; and

a peak-to-peak voltage; and

the pulsed voltage waveform is substantially constant during at least a portion of the second time interval.

2. The method of claim 1, wherein first time interval is between about 200 ns and about 400 ns.

3. The method of claim 1, wherein the first time interval is less than about 20% of a cycle of the series of repeating cycles.

4. The method of claim 3, wherein the pulsed voltage waveform within each pulsed waveform cycle has a peak-to-peak voltage that is between about 5 kV and 20 kV.

5. The method of claim 1, wherein the process gas comprises a second fluorocarbon containing gas and a second process gas.

6. The method of claim 1 wherein the first fluorocarbon-containing gas comprises at least one of C_4F_6 or C_3F_6, and the first process gas comprises at least one of N_2, Kr, and O_2.

7. The method of claim 1, further comprising:

disposing a mask on the substrate comprising one or more conductive layers;

providing the substrate with the mask and the one or more conductive layers within the plasma processing chamber; and

etching the first dielectric material based on a plurality of parameters.

8. The method of claim 7, wherein the one or more conductive layers comprises at least one of tungsten, platinum, titanium, ruthenium, and silicon.

9. The method of claim 7, wherein the one or more conductive layers comprises at least one of molybdenum, cobalt and hafnium.

10. The method of claim 7, wherein etching the first dielectric material comprises:

etching a first trench through the first dielectric material, the first trench extending to a first conductive layer of the one or more conductive layers; and

etching a second trench through the first dielectric material past a depth of the first trench, the second trench extending to a second conductive layer of the one or more conductive layers.

11. The method of claim 10, wherein etching the first dielectric material comprises:

etching a third trench through the first dielectric material past a depth of the second trench until the third trench reaches a base layer of the substrate.

12. The method of claim 10, wherein the first trench does not pass through the first conductive layer and the second trench does not pass through the second conductive layer.

13. The method of claim 10, wherein etching the first trench through the dielectric comprises etching the second trench to a depth matching the depth of the first trench.

14. The method of claim 1, wherein etching the first dielectric material comprises etching one or more trenches through the first dielectric material, wherein a depth of each of the one or more trenches is different and each of the one or more trenches contacts a different conductive layer of the one or more conductive layers.

15. The method of claim 14, wherein each of the one or more trenches does not pass through any of the one or more conductive layers.

16. The method of claim 14, wherein etching the first dielectric material comprises forming an interface between one or more trenches and a conductive layer of the one or more conductive layers.

17. The method of claim 16, wherein ends of each of the one or more conductive layers are displaced from each other to form a staircase.

18. The method of claim 1, wherein

the delivering of the process gas to the processing region of the plasma processing chamber forms a chamber pressure between 1 mTorr and 500 mTorr, wherein delivering the process gas comprises flowing the first fluorocarbon containing gas at a first flow rate and the first process gas at a second flow rate; and

the pulsed voltage waveform that is established at the biasing electrode disposed comprises a duty cycle that is between 1 and 99%.

19. The method of claim 18, wherein the first fluorocarbon-containing gas comprises at least one of C_4F_6 or C_3F_6, and the first process gas comprises at least one of N_2, Kr, and O_2.

20. The method of claim 19, wherein

the series of repeating pulsed waveform cycles are provided at a pulse frequency between about 300 and 500 kHz, and

the etching the first dielectric further comprises maintaining a temperature of the substrate support surface in a ranges between -80°C to 500°C.

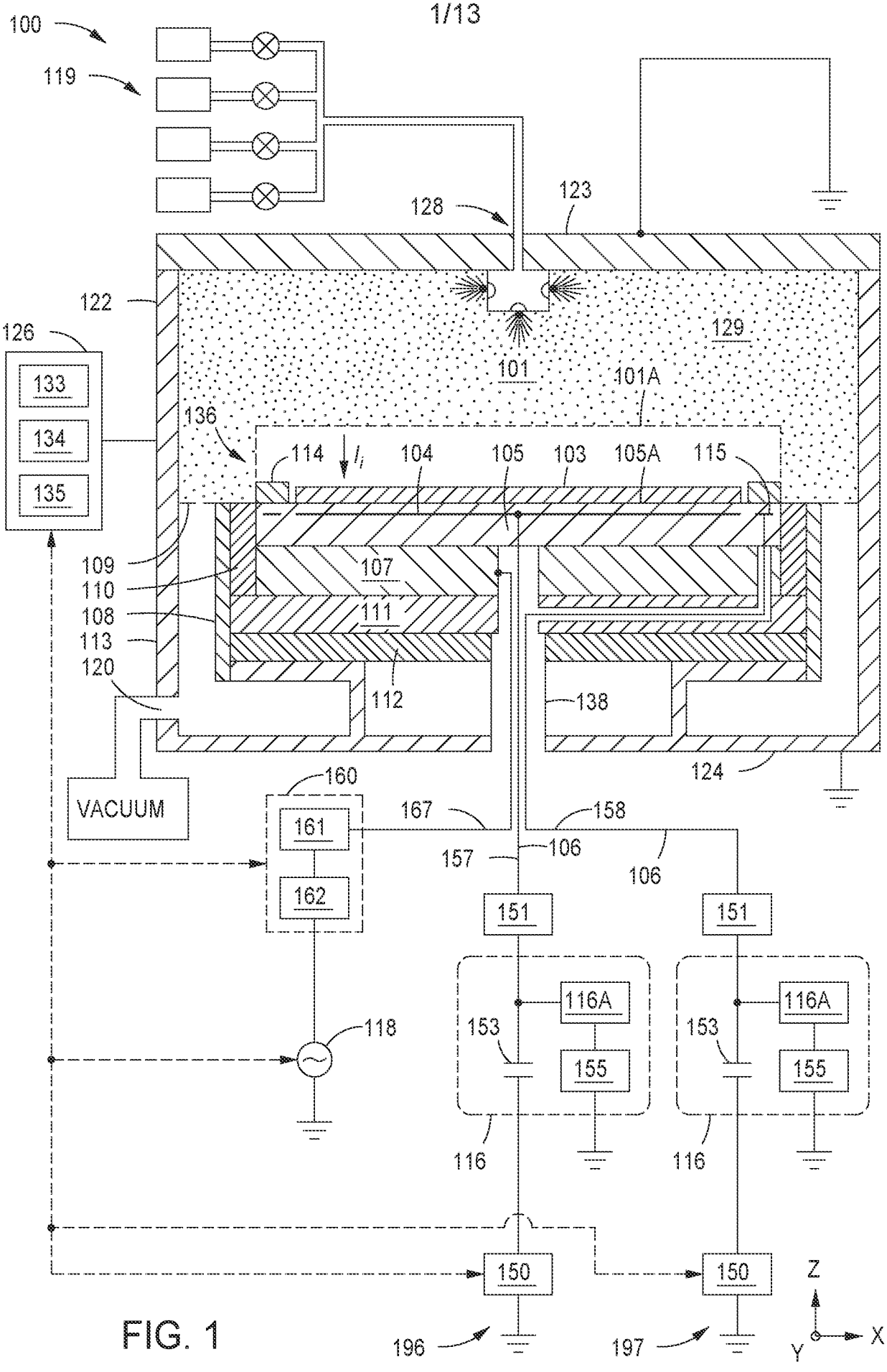

100
119
128
123
122
126
129
101
101A
133
134
135
136
114
I_i
104
105
103
105A
115
109
110
108
113
120
107
111
112
138
124
VACUUM
160
161
162
167
158
157
106
106
151
151
116A
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153
153
155
155
118
116
116
150
150
196
197
Z
X
Y

FIG. 1

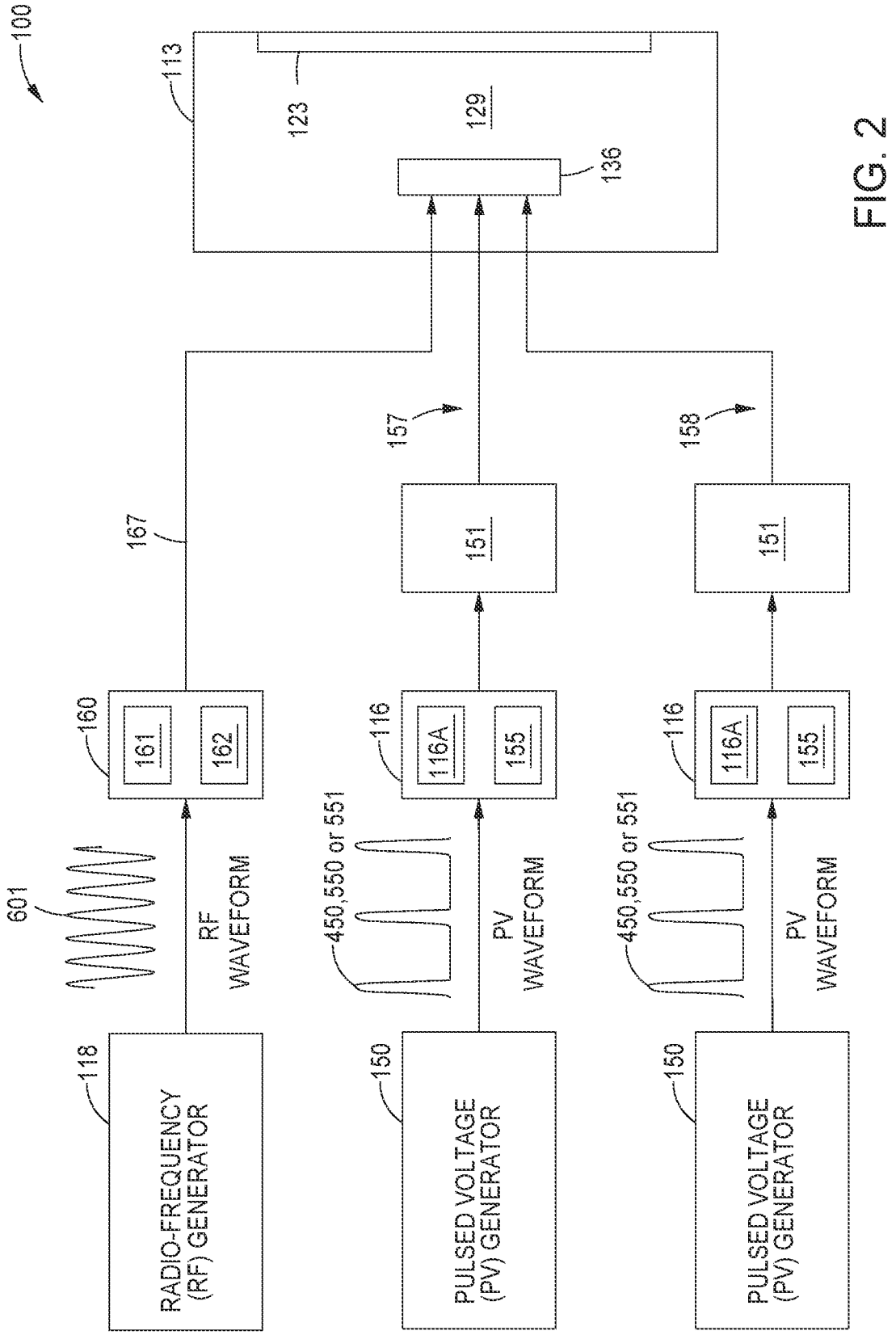

100
113
123
129
136
157
158
167
151
151
160
161
162
116
116A
155
116
116A
155
601
RF WAVEFORM
450,550 or 551
PV WAVEFORM
450,550 or 551
PV WAVEFORM
118
RADIO-FREQUENCY (RF) GENERATOR
150
PULSED VOLTAGE (PV) GENERATOR
150
PULSED VOLTAGE (PV) GENERATOR

FIG. 2

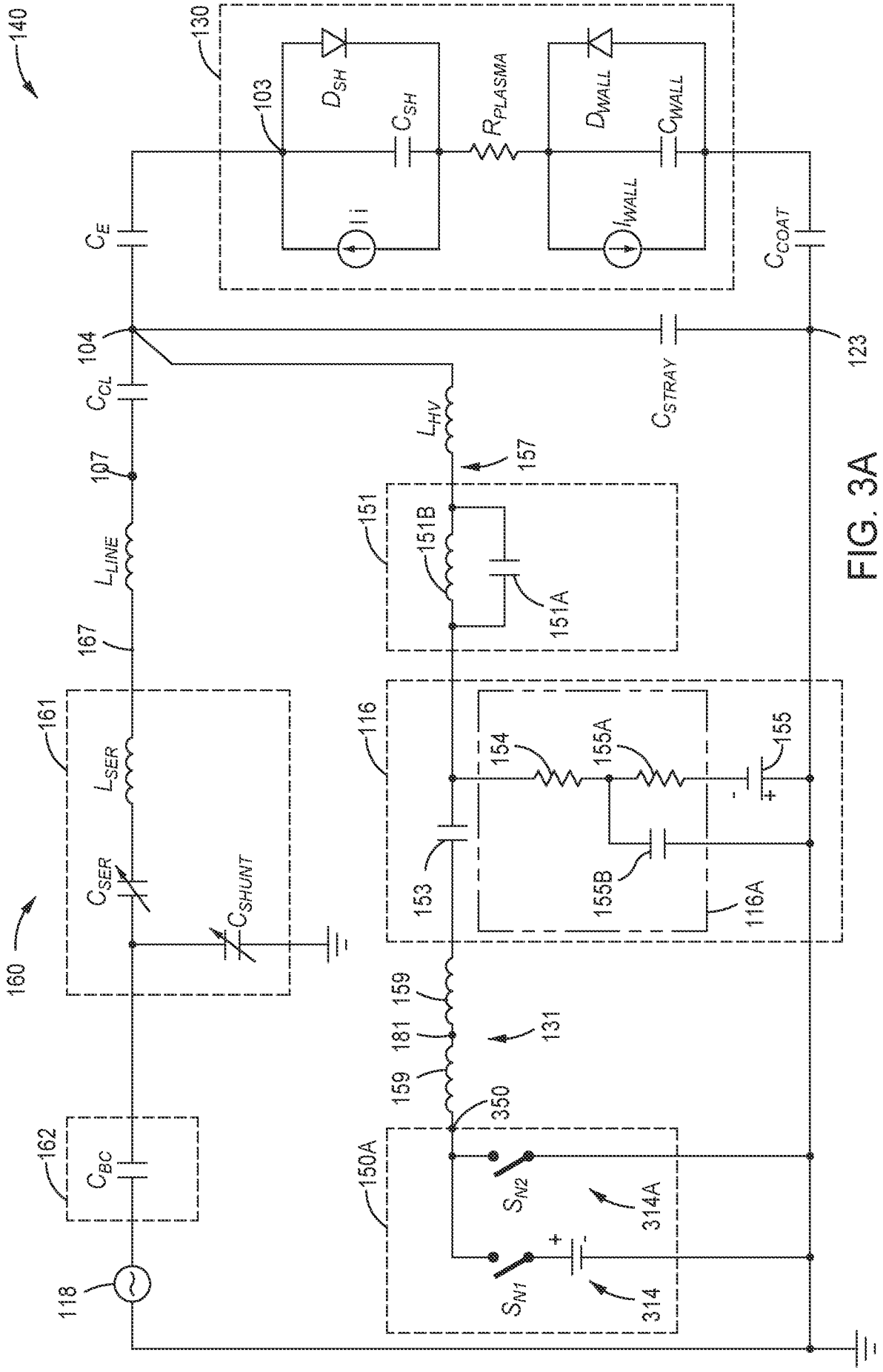

140
130
103
D_{SH}
C_{SH}
R_{PLASMA}
D_{WALL}
C_{WALL}
I_i
I_{WALL}
C_E
C_{COAT}
104
123
C_{CL}
C_{STRAY}
107
L_{HV}
157
151
151B
151A
L_{LINE}
167
116
154
155A
155
153
155B
116A
161
L_{SER}
C_{SER}
C_{SHUNT}
160
159
181
131
159
350
150A
162
C_{BC}
S_{N2}
314A
118
S_{N1}
314

FIG. 3A

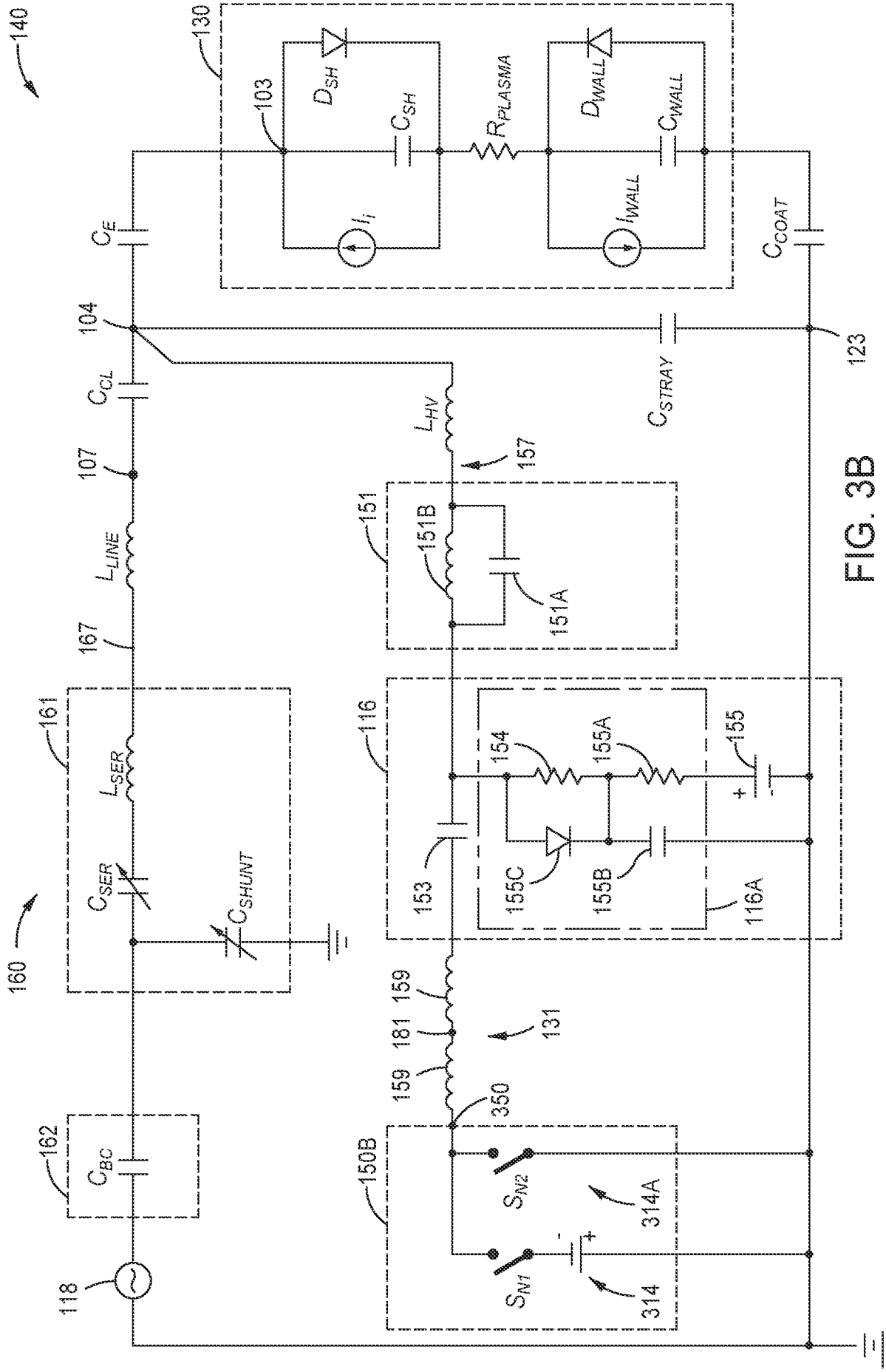

140
130
103
D_{SH}
C_{SH}
I_i
R_{PLASMA}
D_{WALL}
C_{WALL}
I_{WALL}
C_{COAT}
C_E
104
123
C_{STRAY}
C_{CL}
107
L_{LINE}
167
L_{HV}
157
151
151B
151A
161
L_{SER}
C_{SER}
C_{SHUNT}
116
154
155A
155
153
155C
155B
116A
160
159
181
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159
350
162
C_{BC}
150B
S_{N2}
314A
118
S_{N1}
314

FIG. 3B

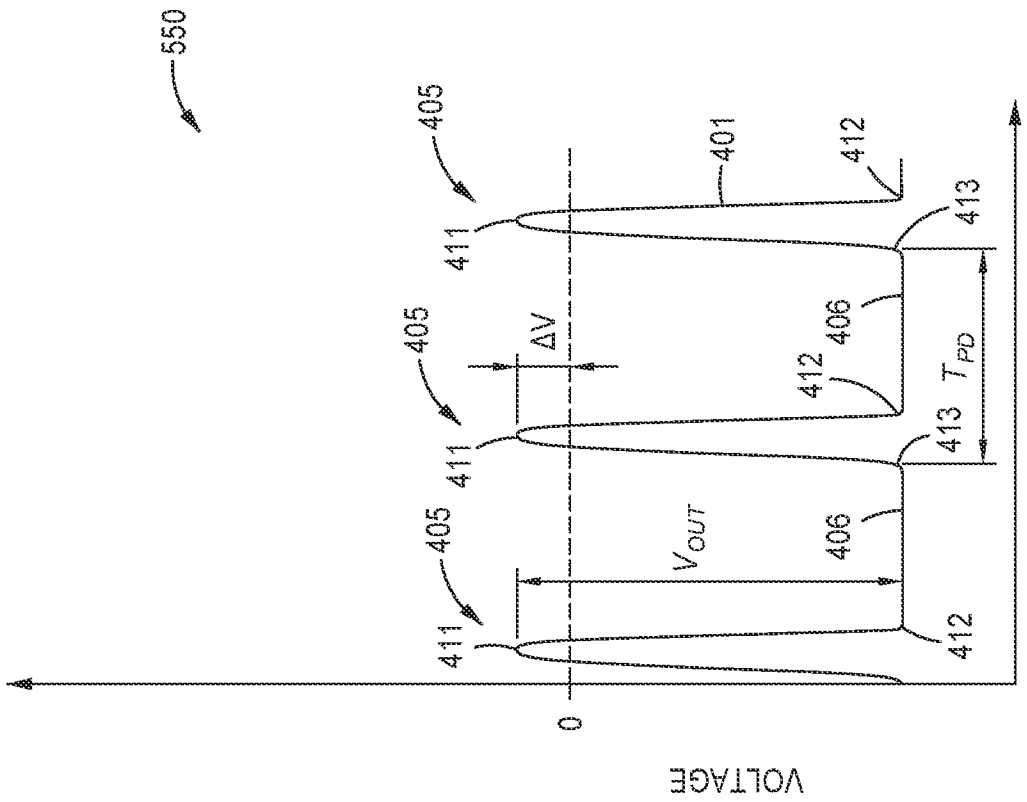


FIG. 4A

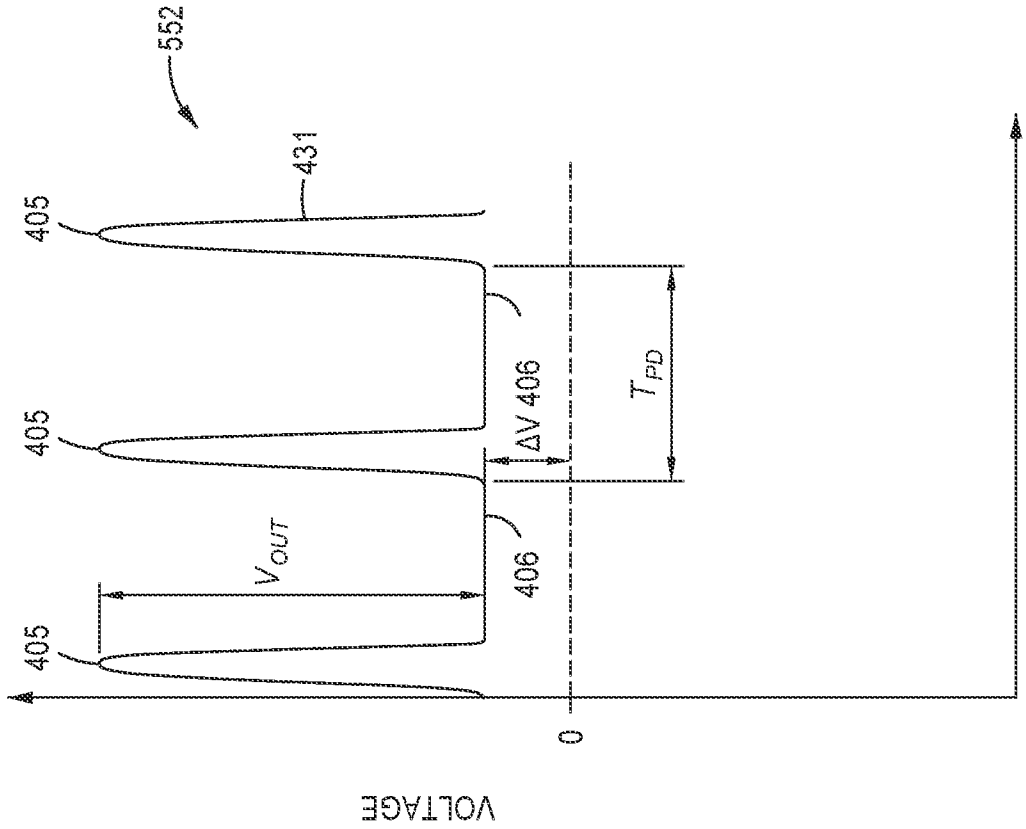

552
431
405
405
405
V_{OUT}
406
ΔV 406
T_{PD}
0
VOLTAGE
TIME

FIG. 4C

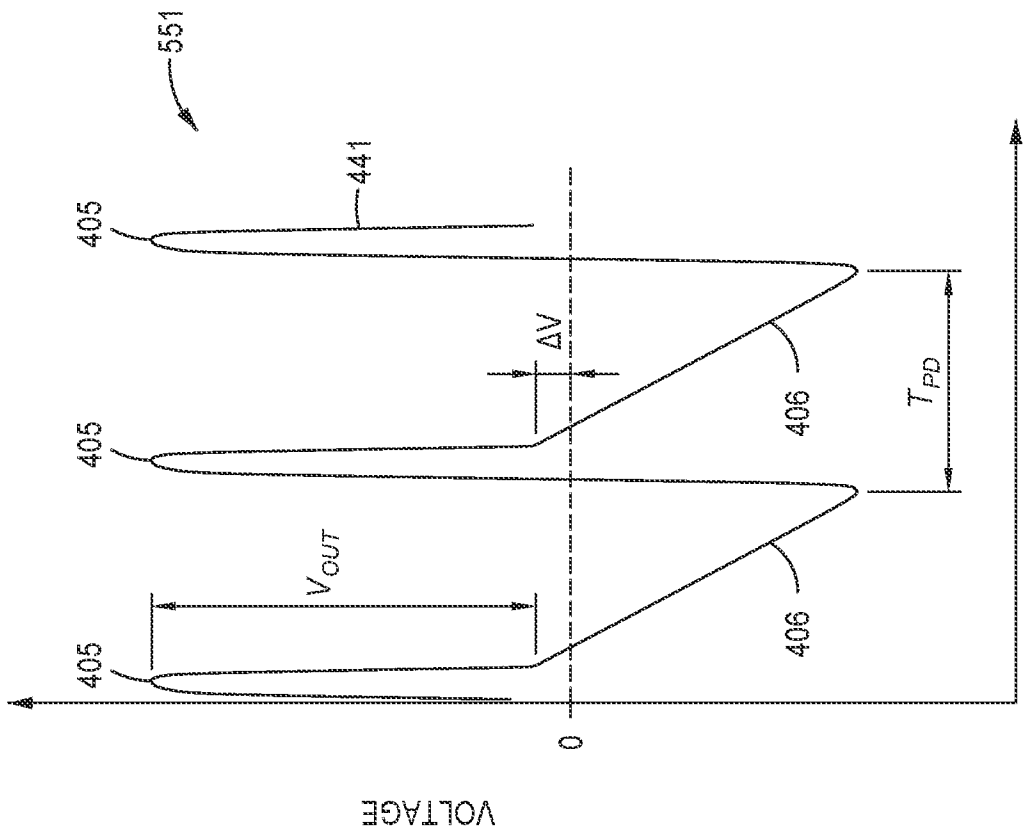

551
441
405
405
405
V_{OUT}
ΔV
406
406
T_{PD}
0
VOLTAGE
TIME

FIG. 4B

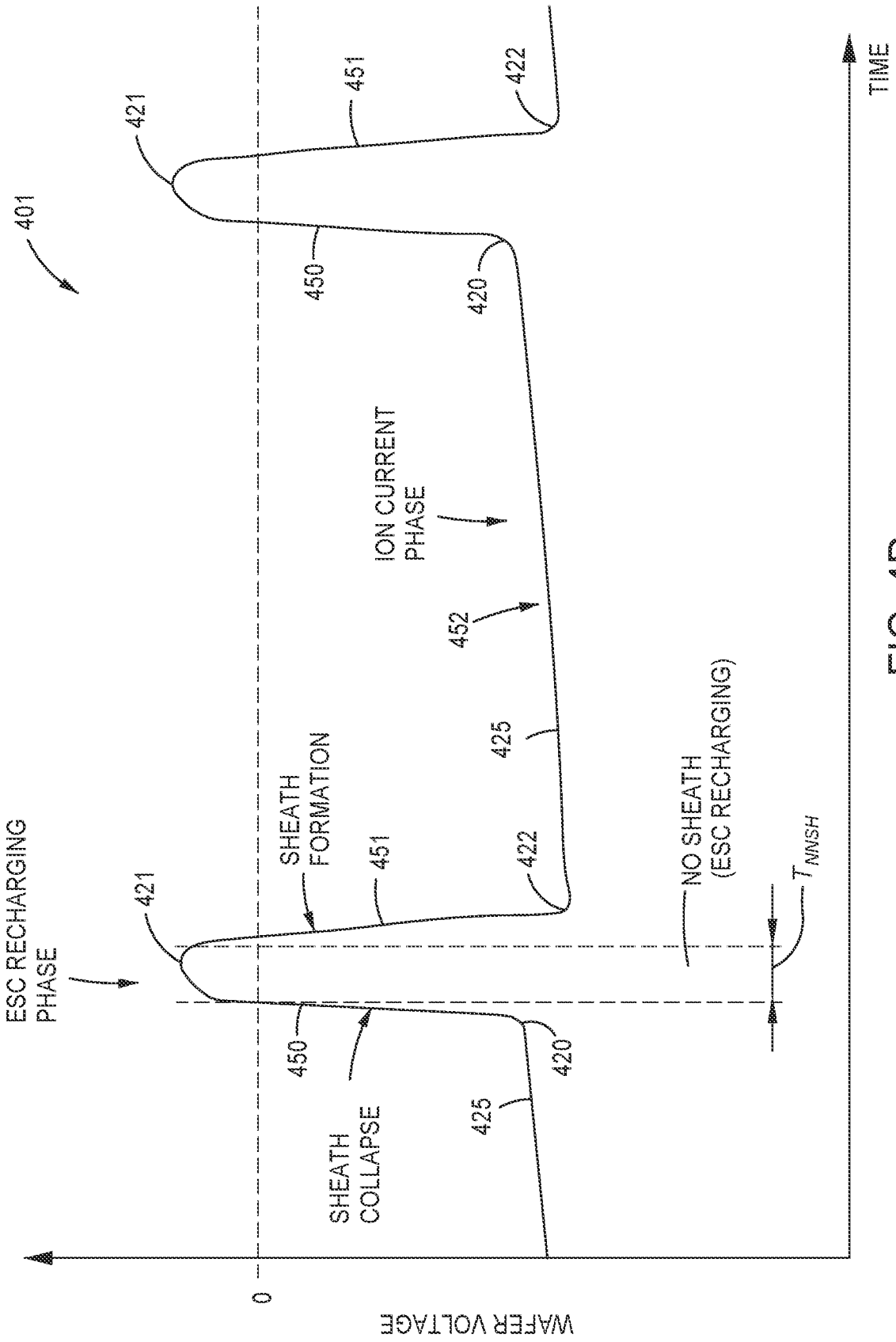

401
421
451
422
450
420
ION CURRENT PHASE
452
425
SHEATH FORMATION
451
422
NO SHEATH (ESC RECHARGING)
T_{NNSH}
ESC RECHARGING PHASE
421
450
420
SHEATH COLLAPSE
425
0
WAFER VOLTAGE
TIME

FIG. 4D

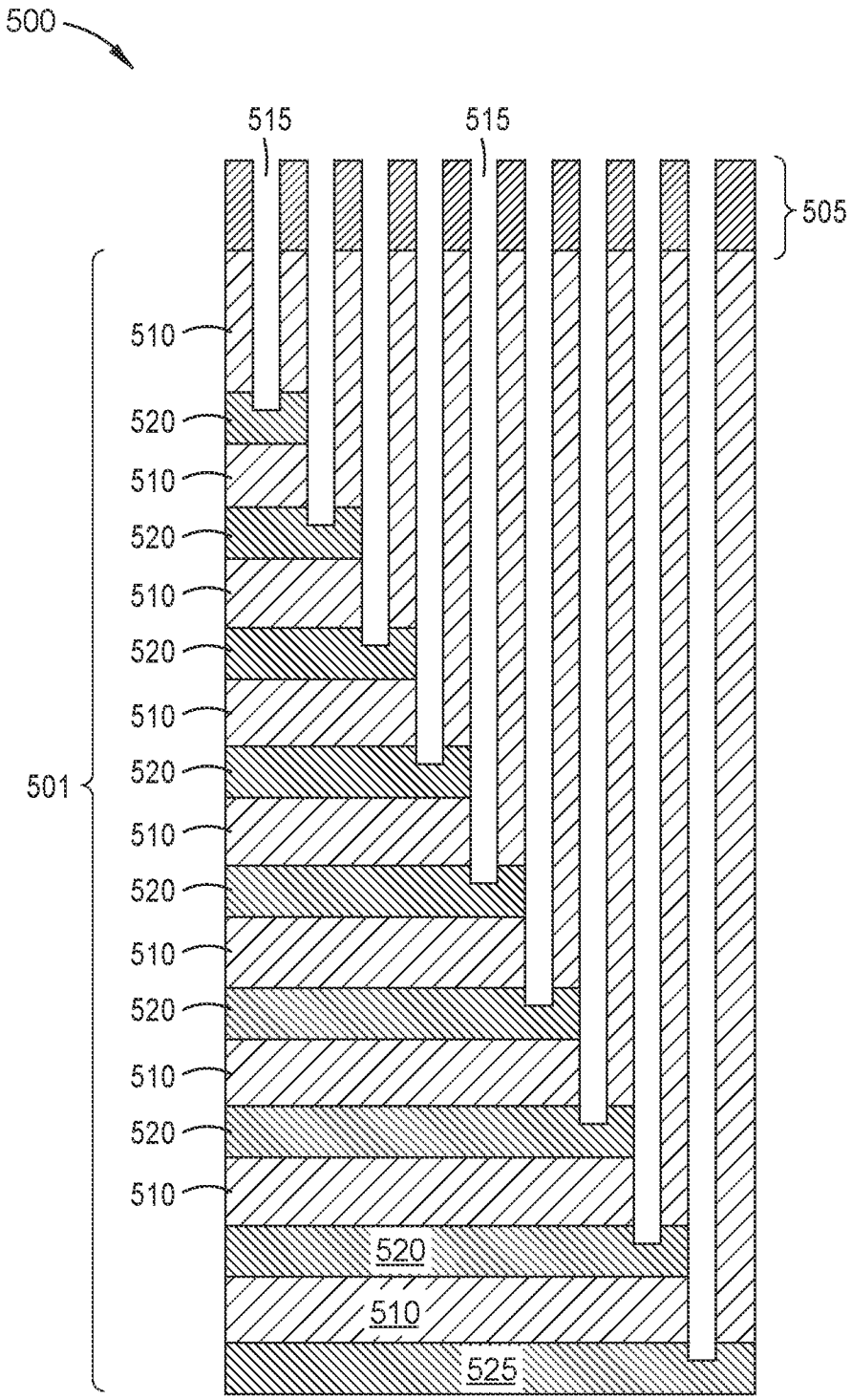

500
515
515
505
510
520
510
520
510
520
510
520
510
520
510
520
510
520
510
520
510
520
510
520
510
501
520
510
525

FIG. 5

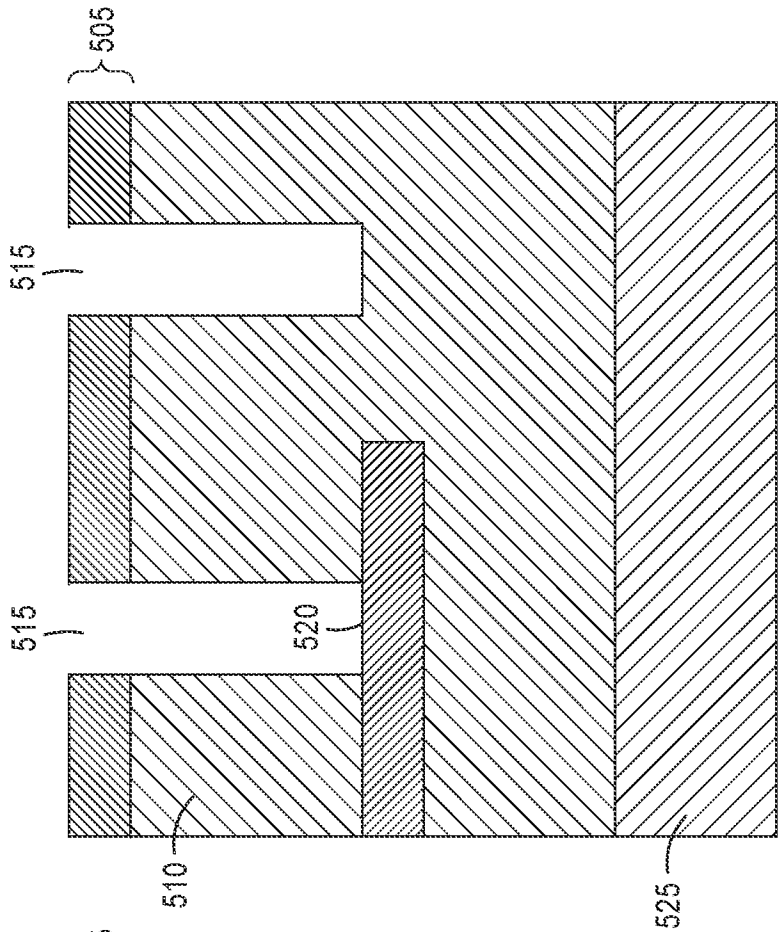


FIG. 6B

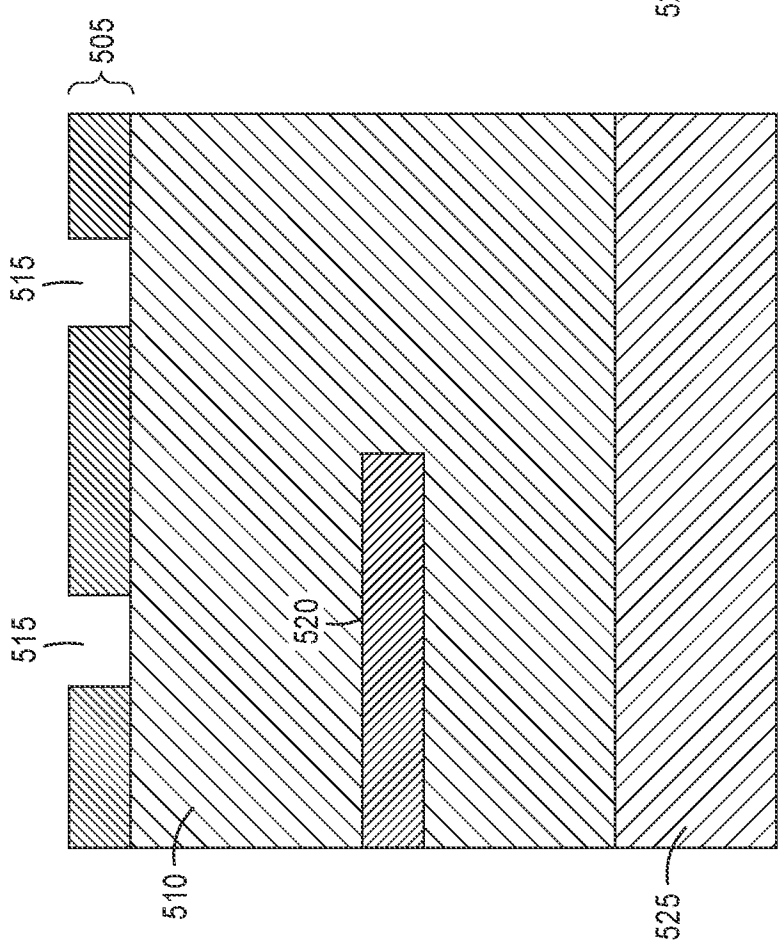


FIG. 6A

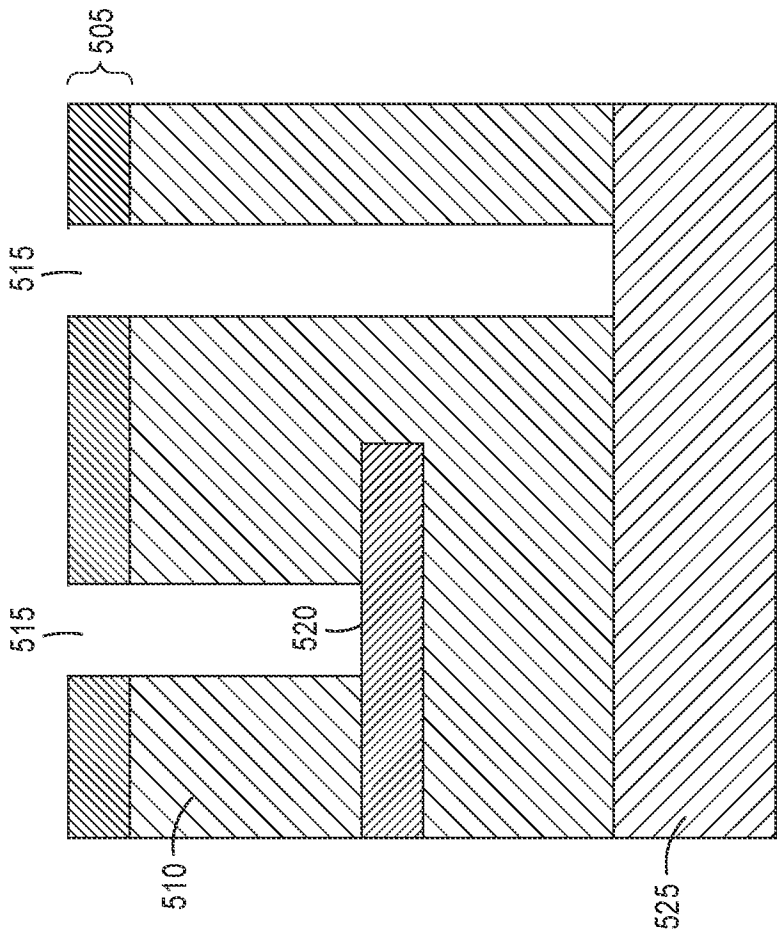


FIG. 6C

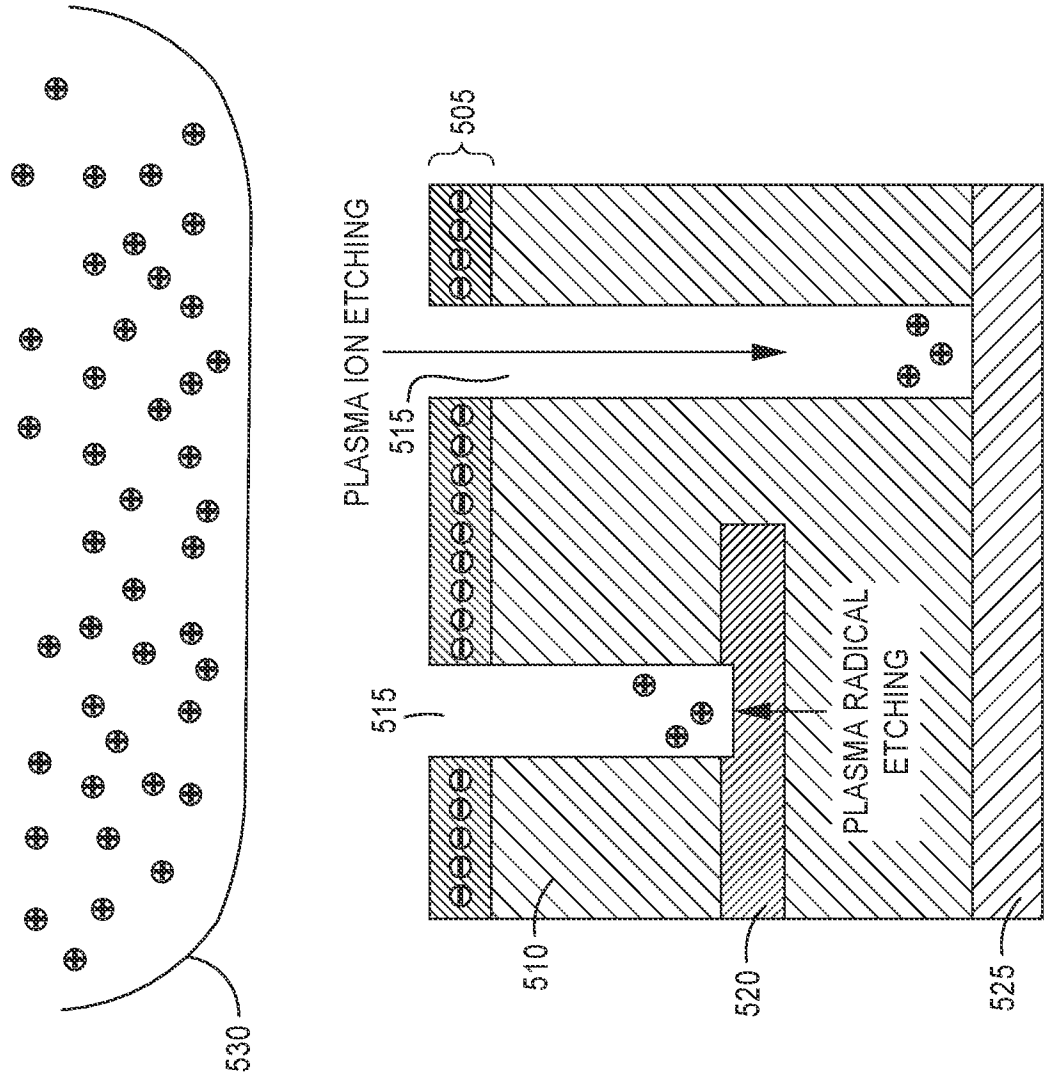

530
PLASMA ION ETCHING
505
515
515
PLASMA RADICAL ETCHING
510
520
525

FIG. 7

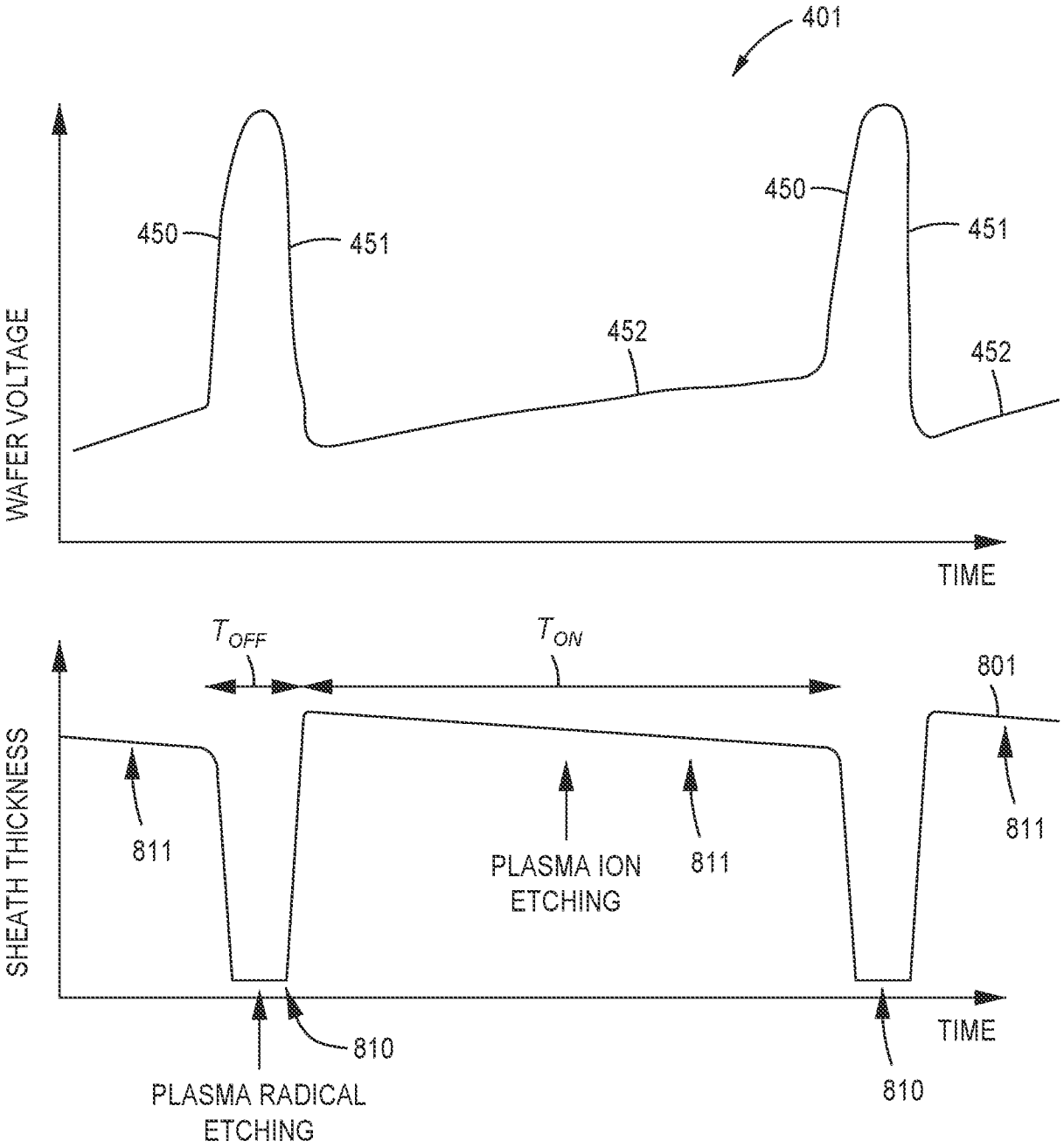

401
WAFER VOLTAGE
450
451
452
450
451
452
TIME
T_{OFF}
T_{ON}
801
SHEATH THICKNESS
811
PLASMA ION ETCHING
811
811
TIME
810
PLASMA RADICAL ETCHING
810

FIG. 8

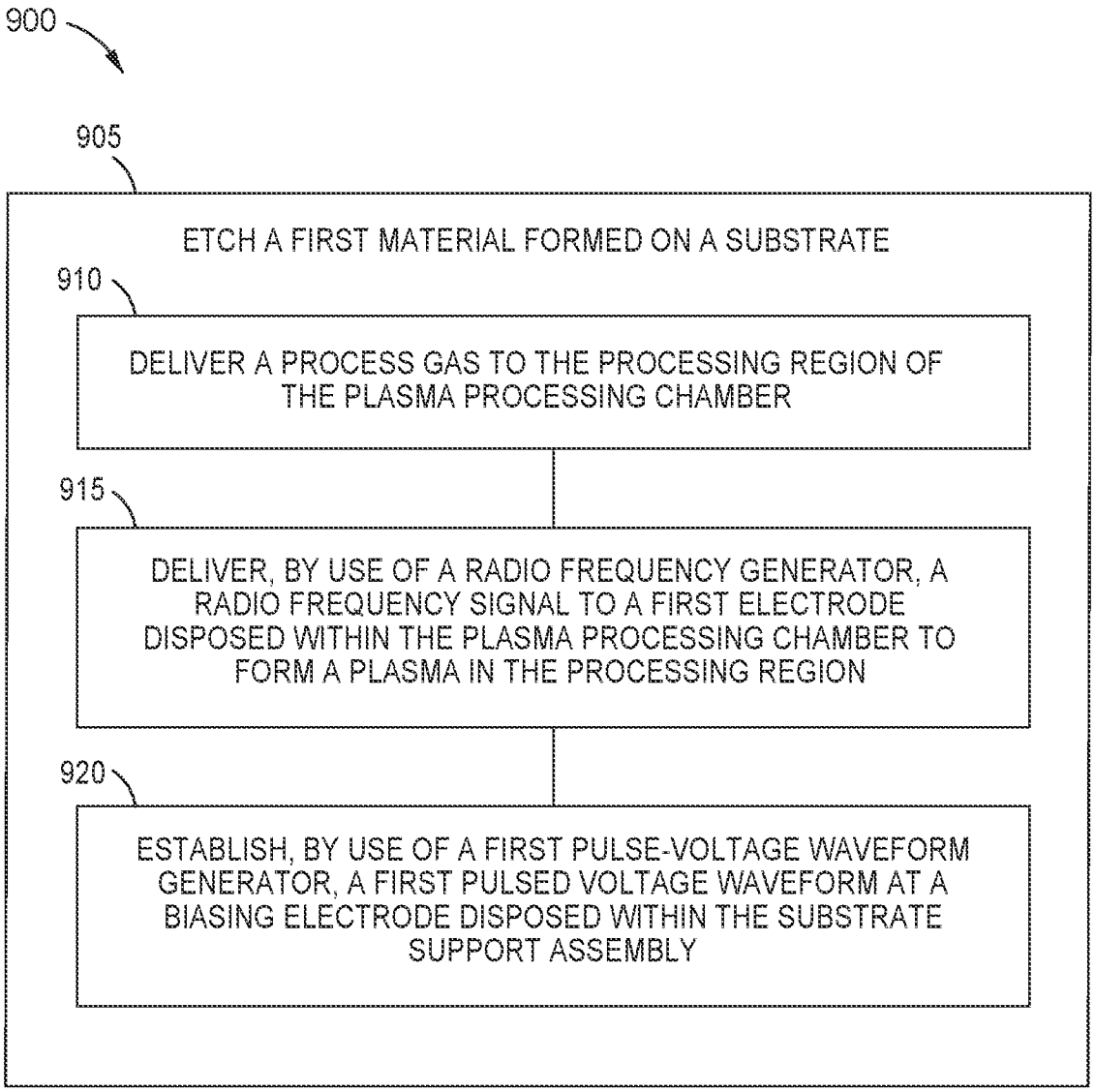

900
905
ETCH A FIRST MATERIAL FORMED ON A SUBSTRATE
910
DELIVER A PROCESS GAS TO THE PROCESSING REGION OF THE PLASMA PROCESSING CHAMBER
915
DELIVER, BY USE OF A RADIO FREQUENCY GENERATOR, A RADIO FREQUENCY SIGNAL TO A FIRST ELECTRODE DISPOSED WITHIN THE PLASMA PROCESSING CHAMBER TO FORM A PLASMA IN THE PROCESSING REGION
920
ESTABLISH, BY USE OF A FIRST PULSE-VOLTAGE WAVEFORM GENERATOR, A FIRST PULSED VOLTAGE WAVEFORM AT A BIASING ELECTRODE DISPOSED WITHIN THE SUBSTRATE SUPPORT ASSEMBLY

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/020957

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/311(2006.01)i; **H01J 37/32**(2006.01)i; **H01L 27/11524**(2017.01)i; **H01L 27/1157**(2017.01)i; **H01L 27/11556**(2017.01)i; **H01L 27/11582**(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/311(2006.01); H01J 37/32(2006.01); H01L 27/115(2006.01); H01L 27/11524(2017.01); H01L 27/11565(2017.01); H01L 27/11582(2017.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: plasma processing chamber, substrate, radio frequency signal, pulsed-voltage waveform, pulsed waveform cycle

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2015-0221478 A1 (TOKYO ELECTRON LIMITED) 06 August 2015 (2015-08-06) See paragraphs [0058]-[0077] and figures 1-3.	1-20
Y	US 2020-0234923 A1 (APPLIED MATERIALS, INC.) 23 July 2020 (2020-07-23) See paragraphs [0100]-[0101], claim 1 and figures 8A, 9A.	1-20
Y	CN 111512439 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 07 August 2020 (2020-08-07) See paragraphs [0028], [0037], [0045], [0047] and figures 2, 6, 8.	7-17
A	US 2017-0278864 A1 (SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORPORATION) 28 September 2017 (2017-09-28) See paragraphs [0041]-[0096] and figures 7-16.	1-20
A	US 2020-0075627 A1 (SAMSUNG ELECTRONICS CO., LTD.) 05 March 2020 (2020-03-05) See paragraphs [0041]-[0065] and figures 2F-2N.	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 July 2022	**11 July 2022**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**PARK, HYE LYUN**
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2022/020957

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