

- [54] **APPARATUS FOR STORING SEQUENCES OF MUSICAL NOTES**
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- [22] **Filed:** Feb. 19, 1974
- [21] **Appl. No.:** 443,292
- [52] **U.S. Cl.** 84/1.01; 84/1.03; 84/115; 84/445; 84/462
- [51] **Int. Cl.** G10h 1/00; G10f 5/00
- [58] **Field of Search** 84/1.01-1.03, 84/1.28, 115, 445, 461, 462, DIG. 29

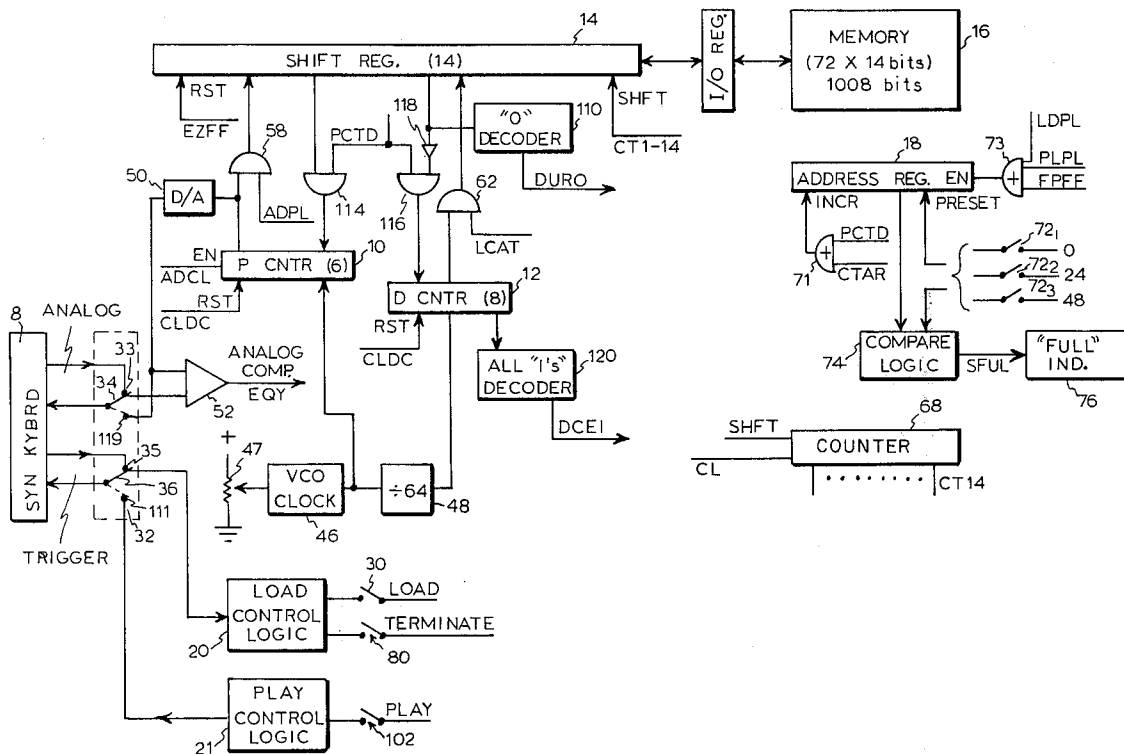
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[57] **ABSTRACT**

A sequencing apparatus responsive to electric signals produced by playing an electronic music synthesizer keyboard for storing melodic and rhythmic information. The sequencer develops digital codes representing the durations between successive notes, and in addition converts the analog signals representing the pitch of a note into digital form. The sequencer, operating in a LOAD MODE, stores the digital data for subsequent playback during a PLAY MODE. Upon command, the digital pitch information is reconverted to analog form and returned to the electronic synthesizer at a selectable speed above or below the tempo of the melody originally played on the synthesizer keyboard.

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14 Claims, 7 Drawing Figures



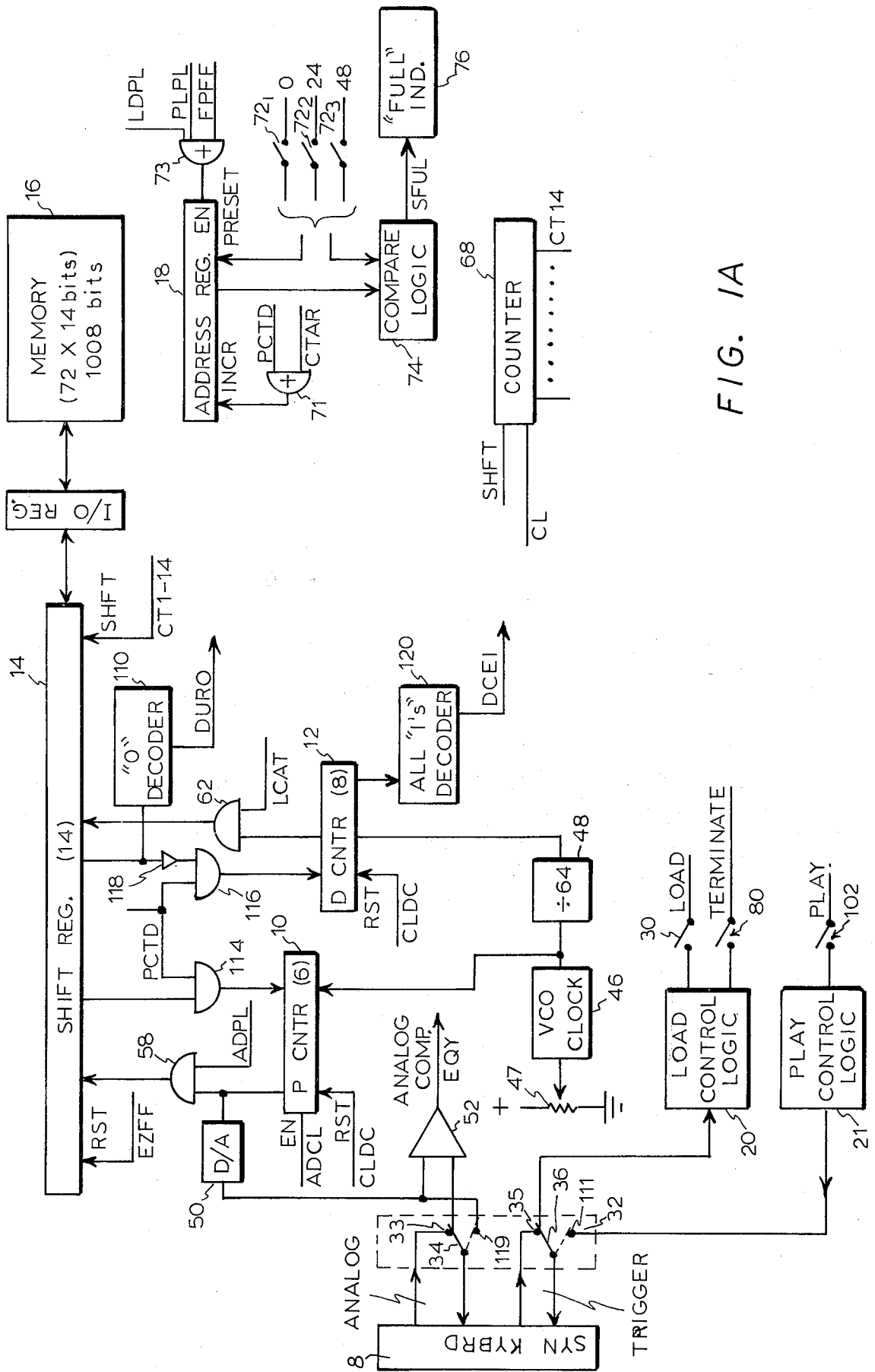


FIG. 1A

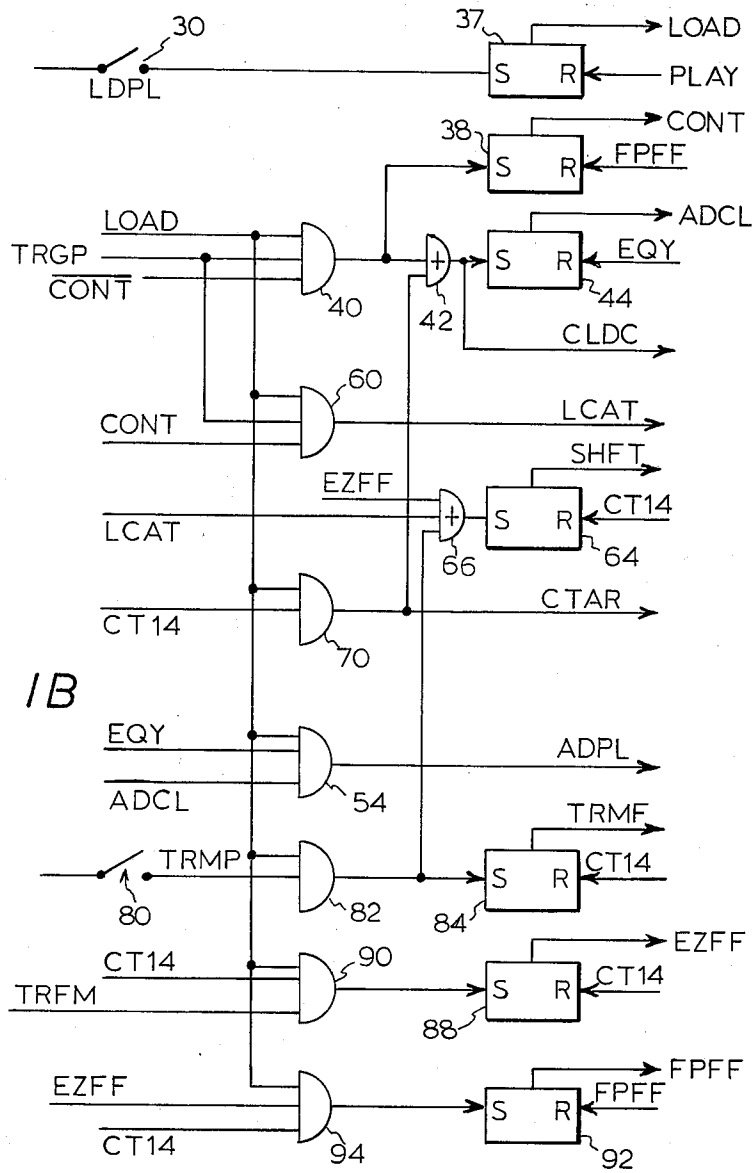


FIG. 1B

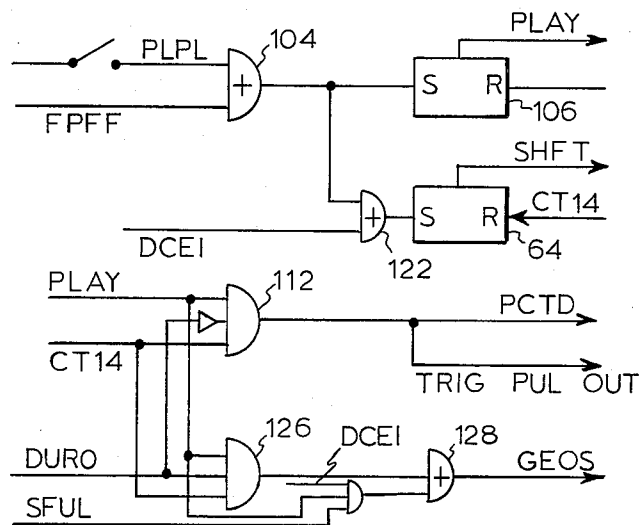


FIG. 1C

LOAD MODE TIMING DIAGRAM

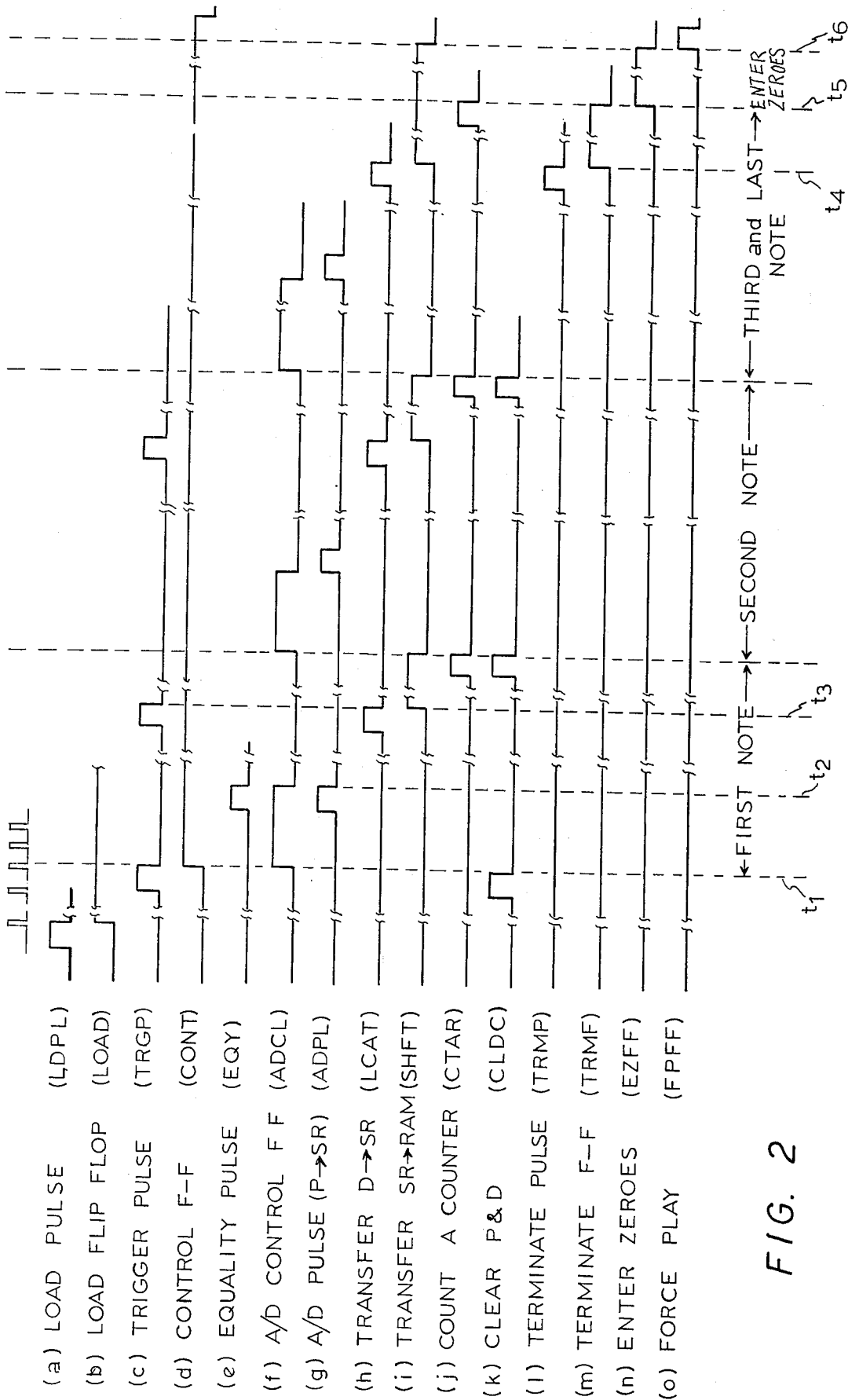


FIG. 2

EXAMPLE OF 3-NOTE SEQUENCE

PLAY MODE TIMING DIAGRAM

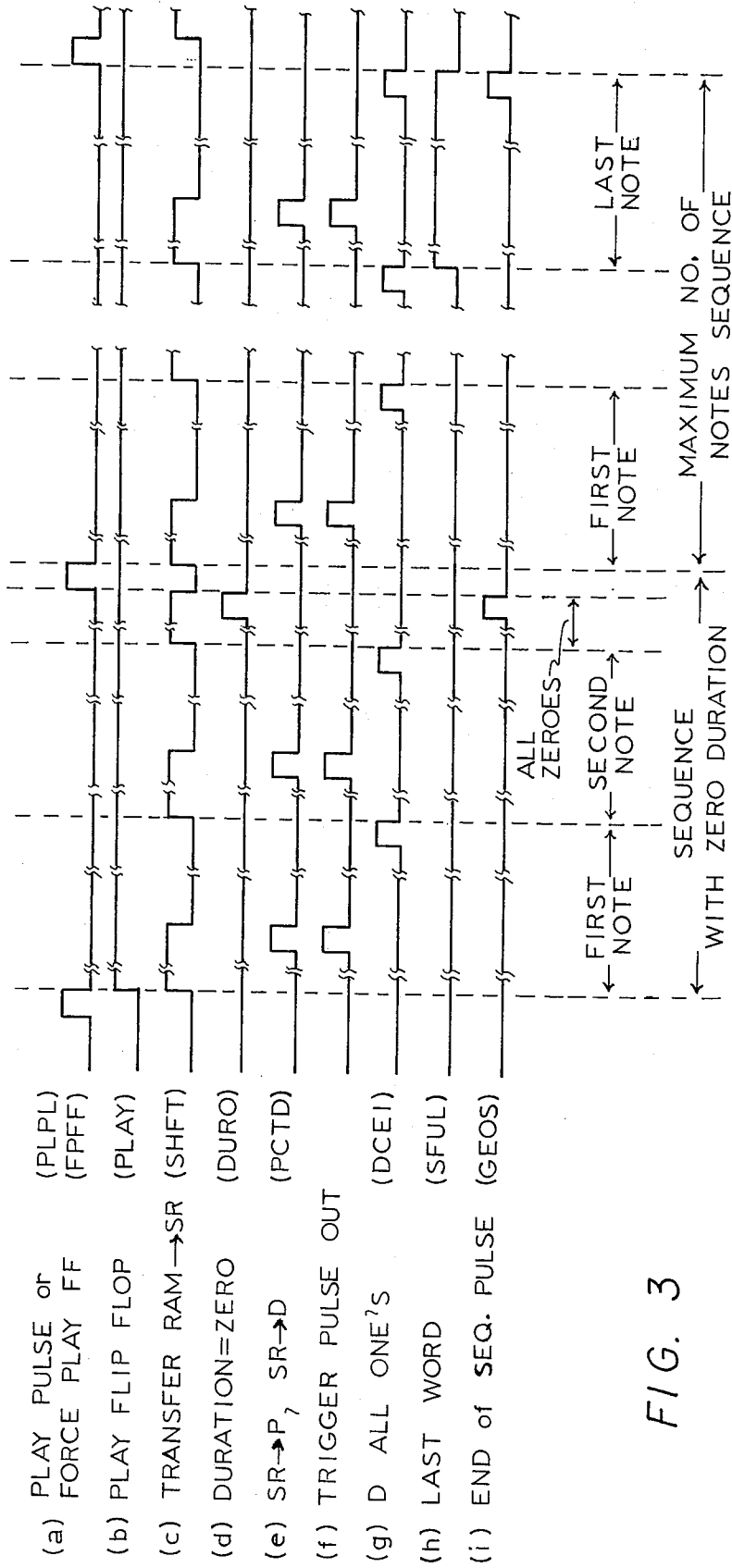


FIG. 3

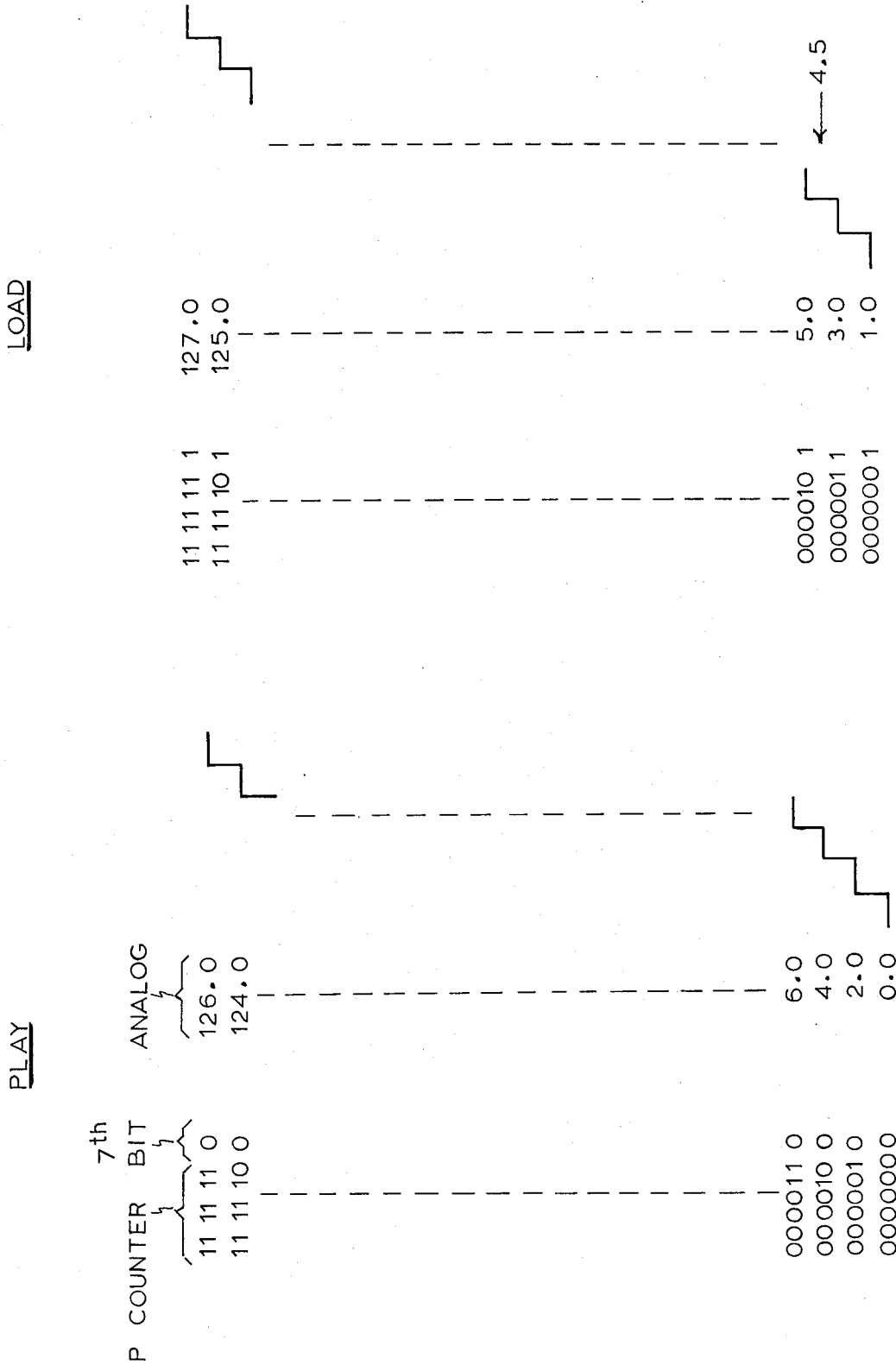


FIG. 4

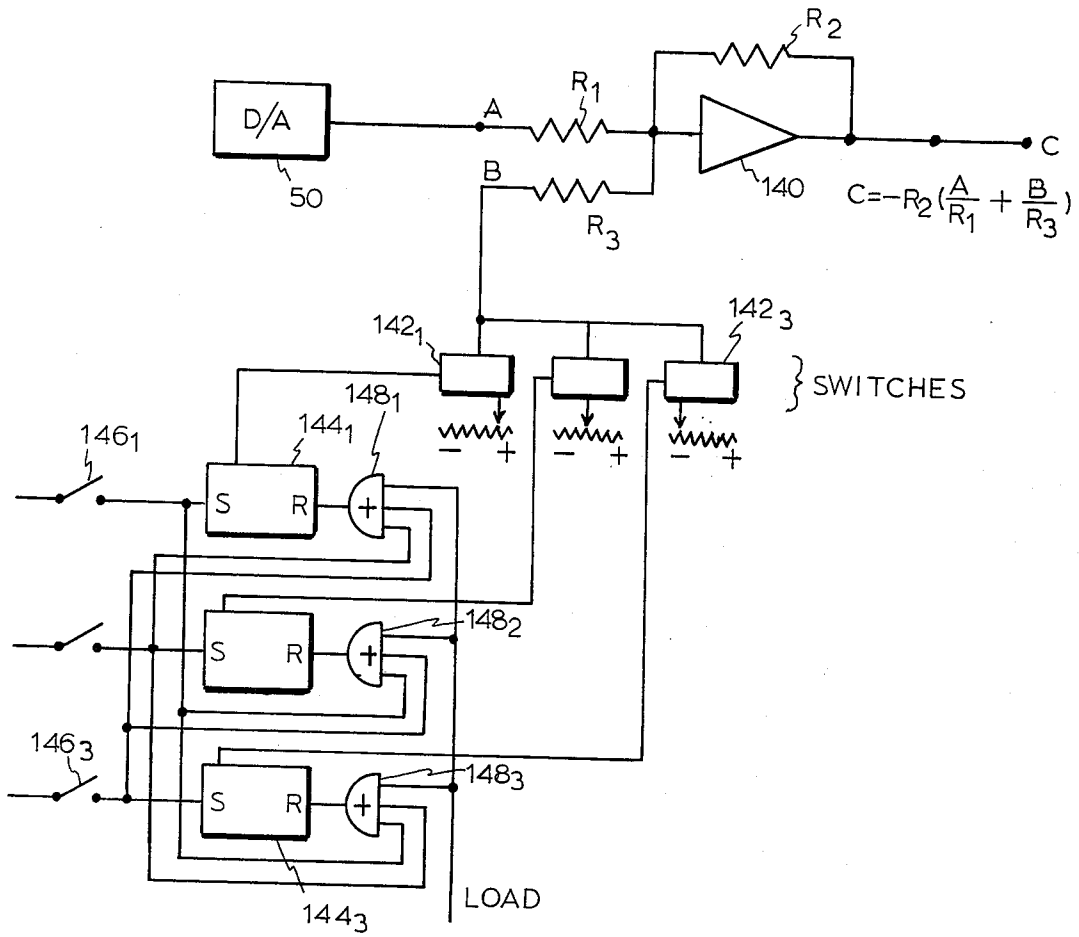


FIG. 5

APPARATUS FOR STORING SEQUENCES OF MUSICAL NOTES

BACKGROUND OF THE INVENTION

The present invention relates to a digital sequencer primarily intended for use in conjunction with an electronic music synthesizer.

Commercially available electronic music synthesizers are frequently used by professional musicians to assist them in performing, arranging and composing. Typically, these synthesizers include keyboards, which when played by the musician, produce trigger pulses and discrete analog (DC) voltages representative of pitch. The DC voltages are applied to electronic circuitry including a voltage controlled oscillator whose output is applied through gating circuitry, controlled by the trigger pulses, to drive some type of audio transducer.

Attempts have been made in the prior art to provide an apparatus (known as a "sequencer") capable of simply and inexpensively both remembering a sequence of notes loaded therein and of accessing that sequence to drive the synthesizer tone generator. Perhaps the most widely used sequencer is one comprised of a bank of potentiometers each including a manually operable dial for establishing a certain DC voltage. In order to load this sequencer, the musician would manually set each potentiometer. Thereafter, the bank of potentiometers is scanned to sequentially read out the DC voltages to drive the voltage controlled oscillator to produce melody. The sequencer, of course, enables the musician to repeatedly listen to the melody and to make changes by varying the potentiometer dials.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a sequencer for use with an electronic music synthesizer which allows a sequence of notes to be loaded and stored while a melody is being played on the synthesizer keyboard.

In accordance with the invention, a sequencer is provided which, in the LOAD MODE, stores digital information with respect to each note played on the synthesizer keyboard. The digital information stored with respect to each note is representative of both the pitch of the note and the time duration between trigger pulses of adjacent notes.

In a preferred embodiment of the invention, the sequencer includes means for converting the DC analog voltage developed by the synthesizer into a multi-bit code representative of pitch and means for counting locally generated clock pulses between trigger pulses to develop a multi-bit code representative of time duration. The pitch and time duration codes are stored as separate fields of a single digital word or note.

In the PLAY MODE, the stored notes are read out sequentially with the pitch field being converted back to analog form and with the duration field being used to generate trigger pulses for application to the synthesizer.

In accordance with one feature of the invention, means are provided for enabling a user to vary the tempo of a melody as it is played back through a synthesizer during the PLAY MODE.

In accordance with a further feature of the invention, means are provided for enabling a user to transpose,

that is change the key of a melody as it is played back through a synthesizer during the PLAY MODE.

In accordance with a still further feature of the invention, means are provided for compensating for noise which could be superimposed on an input voltage level by offsetting the digital-analog conversion characteristics between the PLAY and LOAD modes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic block diagram of a sequencer in accordance with the present invention;

FIG. 1B is a schematic block diagram illustrating the logic within the LOAD control logic block of FIG. 1A;

FIG. 1C is a schematic block diagram illustrating the logic within the PLAY control logic block of FIG. 1A;

FIG. 2 is a timing diagram depicting the time relationship between signals generated during the LOAD MODE;

FIG. 3 is a timing diagram depicting the time relationship between signals generated during the PLAY MODE;

FIG. 4 is a diagram depicting the voltage levels produced by the digital to analog converter during the PLAY and LOAD modes of operation; and

FIG. 5 is a block schematic diagram illustrating the circuitry for enabling notes to be transposed to a different key.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Prior to referring to the preferred embodiment of the invention illustrated in the drawing, the operation of a sequencer in accordance with the invention will be explained. The sequencer functions to store representations of the pitch of each of a sequence of musical notes and the time duration between adjacent notes. A sequencer in accordance with the present invention is intended to respond to electrical signals provided by an electronic music synthesizer representative of a note played. With respect to each note in a sequence played on the synthesizer keyboard 8 (FIG. 1A) the synthesizer provides a trigger pulse and a discrete analog voltage representative of pitch. The sequencer stores a multibit digital word for each note played on the synthesizer keyboard. The digital word is comprised of a first multibit field containing pitch information and a second multibit field containing information representing the time duration between adjacent trigger pulses. In the exemplary embodiment to be discussed herein, the first field is comprised of six bits thus enabling sixty-four different pitch levels to be represented. The second field is comprised of eight bits enabling two hundred fifty-six different durations to be defined.

The sequencer operates in either a LOAD MODE or a PLAY MODE. During the LOAD MODE, the discrete DC voltage levels provided by the synthesizer are converted from analog to digital form and stored in a digital memory along with a digital representation of the length of time between trigger pulses. During the PLAY MODE, the digital memory is accessed at a rate determined by the previously stored duration between trigger pulses. The accessed pitch information is reconverted to analog form and supplied to the synthesizer along with trigger pulses generated by the sequencer.

Attention is now called to FIG. 1A which illustrates the sequencer as including a six bit P counter 10 which functions to accumulate a digital representation of the

analog voltage provided by the synthesizer and an eight bit D counter 12 which accumulates a digital representation of the time duration between adjacent notes. The P counter operates by counting pulses sequentially provided by a pulse source. A digital-to-analog converter 50 responds to the increasing count in the P counter to produce a staircase waveform which is compared with the analog voltage provided by the synthesizer. When equality is recognized, the contents of the P counter, constituting the digital equivalent of the analog voltage are transferred to the shift register 14 for subsequent storage in memory 16. The D counter operates by counting the number of pulses generated between trigger pulses.

The six-bit pitch information developed by the P counter 10 and the eight-bit duration information developed by the D counter 12 are subsequently loaded into the fourteen-bit shift register 14. Subsequently, a sequence of fourteen clock pulses is provided to shift the fourteen-bit digital word in the shift register 14 into the digital memory 16. The memory 16 can constitute any one of several types of well known digital memories such as semi-conductor, magnetic core, tape, disc, or drum. Regardless of the particular type of memory employed, it will be assumed herein to be comprised of seventy-two word locations each comprised of fourteen bits. Thus, the memory 16 must have a capacity of at least 1,008 bits. An address register 18 is provided to identify the particular one of the seventy-two locations into which the 14-bit note from the shift register 14 is to be loaded (or accessed during the PLAY MODE).

The timing and control of the digital apparatus of FIG. 1A is controlled primarily by a LOAD control logic means 20 during the LOAD MODE and by a PLAY control logic means 21 during the PLAY MODE. The details of LOAD and PLAY control logic means are respectively illustrated in FIGS. 1B and 1C.

In order to now gain a detailed understanding of the implementation and operations of the apparatus of FIG. 1A, attention is directed to the LOAD control logic of FIG. 1B and the LOAD MODE timing diagram of FIG. 2.

The sequencer of FIG. 1A includes a manual load switch 30 available to the operator which produces the LOAD PULSE (LDPL) shown in line a of FIG. 2. Generation of the load pulse switches switch 32 to the load position illustrated in solid line FIG. 1A. The switch 32 preferably comprises an electronic or electromechanical double pole-double throw switch operable in either a LOAD position (solid line) or a PLAY position (dotted line). The switch includes a fixed sequencer analog input contact 33 coupled to the analog output of the synthesizer. Movable contact 34, tied to the analog input of the synthesizer, engages sequencer input contact 33 when in the LOAD position and the sequencer analog output contact 119 in the PLAY position. Similarly, sequencer trigger pulse input contacts 35 is tied to the synthesizer trigger pulse output. Movable contact 36 engages contact 35 when in the LOAD position and sequencer trigger pulse output contact 111 when in the PLAY position.

Note that when switch 32 is in the LOAD position, the analog voltage from the synthesizer keyboard 8 (FIG. 1A) is supplied to the sequencer on contact 33 but is also still available to the synthesizer via contact 34. Similarly, the trigger pulses are supplied to the sequencer via contact 35 but are also still available to the

synthesizer via contact 36 so that the synthesizer continues to operate normally with the sequencer attached and operating in the LOAD MODE.

As shown in FIG. 1B, generation of the load pulse LDPL sets load flip-flop 37 illustrated in line b of FIG. 2. With the load flip-flop 37 set, the sequencer is now to accept incoming information from the synthesizer. Now assume that the musician plays the first note on the synthesizer. This action generates a trigger pulse (TRGP) illustrated in line c of FIG. 2. With the control (CONT) flip-flop 38 (FIG. 1B) false, the trigger pulse TRGP will, via AND gate 40, set the control flip-flop 38 as shown in line d. In addition, the output of gate 40 will, via OR gate 42, set the A/D control flip-flop 44 to cause the output thereof ADCL to go true as represented in line f. The output of OR gate 42 will also produce signal CLDC, line k of FIG. 2, which clears the P counter 10 and D counter 12.

The signal ADCL going true at time t_1 , shown in FIG. 2, enables P counter 10. Thus, P counter 10 and D counter 12 start counting clock pulses originating in clock pulse source 46, which may, for example, comprise a voltage controlled oscillator (VCO) whose frequency is determined by the voltage on the slide of potentiometer 47.

P counter 10 directly counts the pulses supplied by clock pulse source 46. Inasmuch as it is necessary for the P counter to be able to count up to sixty four counts (i.e., to define anyone of sixty four different pitches or notes) during the shortest duration between successive notes (i.e., one count of the D counter), the output of pulse source 46 is passed through a divide by sixty four circuit 48 prior to application to D counter 12. The output of the P counter is applied to the input of a digital-to-analog converter 50. The analog output of converter 50 is applied to one input of an analog comparator 52. The second input to the analog comparator is derived from the synthesizer via switch contact 33.

It should be appreciated that as the P counter counts, the converter 50 will produce a staircase voltage at its output. When the output of the converter 50 equals the discrete analog voltage level provided by the synthesizer through switch contact 33, the analog comparator 52 will provide an equality signal EQY which will reset flip-flop (ADCL) 44 as represented in FIG. 1B at time t_2 shown in line e FIG. 2. In addition, the signal EQY occurring while flip-flop 44 is true, will produce the signal ADPL via gate 54 of FIG. 1B as depicted in line g of FIG. 2. The signal ADPL functions to transfer the six-bit contents of the P counter through gate 58 (FIG. 1A) to the left most six-bit field of the shift register 14.

The D counter 12 will continue to count until the trigger pulse for the next note occurs as represented at t_3 in FIG. 2. This action will produce signal LCAT via gate 60 of FIG. 1B as represented in line h of FIG. 2. Signal LCAT functions to enable gate 62 (FIG. 1A) to transfer the eight-bit duration count from the D counter 12 to the right most eight-bit field of the shift register 14. The signal LCAT in turn sets flip-flop 64 (FIG. 1B) via gate 66 to cause logic signal SHFT to true as shown in line i of FIG. 2. Logic signal SHFT enables a 14 state counter 68 (FIG. 1A) to produce fourteen successive pulses CT 1-14 which are applied to the shift control terminal of shift register 14 to shift the fourteen-bit digital note from the shift register 14 into a word location in memory 16 designated by the contents of address register 18. When pulse CT is gener-

ated, meaning that all fourteen bits have been shifted out of the shift register 14, then the signal CTAR is generated via gate 70 (FIG. 1B). Signal CTAR functions to increment the address register 18 by one count via OR gate 71. Also, signal CLDC is generated to reset the P and D counters.

Note that the address register 18 (FIG. 1A) at the start of the LOAD mode is preset in response to the generation of the load pulse LDPL via OR gate 73 at either location 0, location 24, or location 48, depending upon which of three manual switches 72₁, 72₂, or 72₃ is set by the user. The switches 72 are provided to enable the user to selectively use the seventy-two memory locations to store a single seventy-two note sequence, a twenty-four and a forty-eight note sequence or three separate twenty-four note sequences. A comparison logic means 74 monitors the contents of the address register 18 and compares it with the setting of the switches 72. For example, if the user had depressed switch 72₁, to indicate a starting address of zero and no other switch 72, then the comparison logic 74 would generate a "full" signal SFUL when the address register 18 incremented to a count of 23. Generation of the signal SFUL actuates the full indicator 76 during the LOAD MODE. On the other hand, if the user depressed both switches 72₁ and 72₂ then the address register 18 would have been preset to zero at the beginning of the LOAD MODE operation, but the comparison logic 74 would not generate signal SFUL until the address register 18 incremented to location 47. If all three of the switches 72 were closed, this would designate that a single 72 note sequence was to be stored and the address register 18 would initially be preset to location zero and the comparison logic 74 would not actuate the "full" indicator 76 until the address register incremented to location 71.

It has been mentioned that upon the completion of 14 pulse shift sequence, at pulse CT 14, the address register 18 is incremented and the P and D counters are reset. In addition, flip-flop 44 is set via OR gate 42 to again provide the signal ADCL shown in line *f* of FIG. 2. This again enables the P counter to count clock pulses and produce the staircase waveform, via converter 50, for application to the analog comparator 52 for comparison with the analog voltage provided by the synthesizer in association with the trigger pulse occurring at time *t*₃.

It should now be appreciated that as notes are played on the synthesizer, the sequencer will continue to accumulate pitch and duration information and store fourteen bit digital notes in sequential locations of the memory 16. In most instances, the musician will store sequences shorter than twenty four notes and he will desire to terminate the LOAD MODE and listen to the stored sequence. In order to do this, the user will actuate panel switch 80 (FIG. 1A) to generate terminate pulse TRMP represented in line *l* of FIG. 2. Terminate pulse TRMP will, via gate 82, set terminate flip-flop 84 to produce a true logic level for signal TRMF at time *t*₄ shown in line *m* of FIG. 2. In addition, the output of gate 82 will produce the signal SHFT shown in line *i* via OR gate 66. This action will transfer the contents of the shift register 14 into the memory 16. At the completion of the fourteen pulse shift period when pulse CT 14 is generated, an enter zero flip-flop 88 will be enabled via gate 90, as represented in line *n* of FIG. 2 at time *t*₅. As a consequence of flip-flop EZFF being set, the flip-flop

64 is again set to again generate a fourteen count shift cycle which then shifts fourteen zeroes into the memory 16. The all zero word is used during the PLAY MODE to represent an end of sequence. After the fourteen count shift sequence has been completed at time *t*₆, a force play flip-flop 92 is set via gate 94 to switch the system out of the LOAD MODE into the PLAY MODE to enable the user to listen to the melody he has just stored.

As will be seen hereinafter, during the PLAY MODE a word with all zero duration read from memory 16 will be interpreted as an end of sequence word and cause the first word in the sequence to be read next and the sequence to be played again. In order to avoid the entering of all zero duration in any word during the LOAD mode, which might occur when two notes are played very closely together, whenever the D counter is reset by signal CLDC, it is forced to a count of one rather than a count of zero.

Attention is now called to FIG. 1C which comprises a logic block diagram of the PLAY control 21 depicted in FIG. 1A and FIG. 3 which comprises a timing diagram illustrating the time relationship between various signals occurring during the PLAY MODE.

The PLAY MODE is initiated in response to either the generation of the force play (FPFF) signal generated at the end of the LOAD MODE or in response to actuation of the panel play switch 102 illustrated in FIG. 1A. Either of these conditions will enable the output of OR gate 104 (FIG. 1C) to set the play flip-flop 106 and cause the play signal to go true as illustrated in line *b* of FIG. 3. The output of gate 104 also sets the previously mentioned shift flip-flop 64 to cause the fourteen stage binary counter 68 to provide fourteen pulses CT 1-14. During the PLAY MODE, the fourteen bits stored in the word location identified by the address register 18 are shifted into the shift register 14 (FIG. 1A) during the time interval depicted in line *c* of FIG. 3. After the 14th bit has been shifted into the shift register, i.e., in response to signal CT 14, the zero decoder 110 (FIG. 1A) determines whether the duration, i.e., the right most eight bits in the shift register 14 are zero. If the duration is not zero, then AND gate 112 (FIG. 1C) is enabled to supply a trigger pulse (line *f* FIG. 3) to the switch 32 (FIG. 1A) which is now in the PLAY position shown in dotted line. The trigger pulse is supplied to the synthesizer via contacts 111 and 36. In addition, the output of gate 112 produces signal PCTD which enables both gates 114 and 116. Gate 114 transfers the left most six bits constituting the pitch information from the shift register to the P counter. Gate 116 transfers the eight bits representing the duration information, complemented by logical inverter 118, from the shift register 14 to the D counter 12.

The output of the P counter is coupled to the digital-to-analog converter 50 which develops an analog signal which is supplied through switch contacts 119 and 34 to the synthesizer. The D counter 12, which now contains the complement of the duration between notes is allowed to count. When it reaches the all ones state, as detected by decoder 120, it provides the signal DCE1 represented in line *g* of FIG. 3. The signal DCE1 sets the shift flip-flop 64 via OR gate 122 to cause the fourteen stage counter 68 to again define fourteen shift pulses. This action again causes the next digital note of fourteen bits to be read out of the memory 16 into the shift register 14.

This sequence of reading out successive digital words from the memory 16 into the shift register 14 will continue until a word having a duration of zero is read out. When this occurs, as detected by decoder 110, AND gate 126 (FIG. 1C) will be enabled to in turn produce the end of sequence pulse GEOS via OR gate 128. The signal GEOS in turn produces the force play signal PFFF to initiate the playing of the sequence again. Thus, it should now be appreciated that a sequence of words will be accessed from the memory 16 to produce trigger pulses and analog levels which are provided to the synthesizer through the switch 32 until a word having an all zero duration is encountered. A word having an all zero duration will initiate the playing of the sequence again as a consequence of it producing the signal PFFF represented in line a of FIG. 3.

In addition to a sequence being terminated and reinitiated in response to a word having an all zero duration, termination will also occur when the maximum number of words in the sequence have been accessed from memory. That is, as each word is accessed from the memory 16, the address register 18 is incremented in response to signal PCTD via OR gate 71. When the contents of address register 18 is incremented to be equal to the highest address in the sequence, as defined by the configuration of switches 72 the compare logic 74 will generate the signal SFUL represented in line *h* of FIG. 3. More particularly, if switch 72₁ is the only switch closed, then the compare logic 74 will generate signal SFUL when the address register 18 defines location 23, i.e., the highest address in the initial twenty-four note sequence. If switches 72₂ or 72₃ are respectively closed, then the compare logic 74 will generate signal SFUL when the address register defines locations 47 and 72 respectively. In any event, when the compare logic 74 generates the signal SFUL, it indicates that the end of a sequence has been reached and as a consequence, the pulse GEOS represented in line *i* of FIG. 3, will be produced via OR gate 128, to thereafter produce the pulse shown in line a of FIG. 3 to reinitiate the sequence.

It should be recognized that during the PLAY MODE, new note information (i.e., trigger pulse and analog voltage level) is supplied to the synthesizer at a rate determined by the magnitude of the duration fields in the words read from memory 16. That is, the complement of a duration field is transferred into D counter 12 and then D counter is counted up to an all ones state by pulses provided by pulse source 46. In order to enable the melody to be played back by the synthesizer at either a faster or slower tempo, the frequency of the pulses provided by source 46 can be varied by the operator by adjustment of potentiometer 47.

It has been explained that the digital to analog converter 50 produces an analog representation of the count stored digitally in P counter 10. During the LOAD MODE, the converter 50 produces a staircase voltage wave form as the P counter counts the pulses supplied by clock pulse source 46. During the PLAY MODE, the converter 50 produces a voltage level equivalent to the digitally expressed count transferred into the P counter via gate 114. For the sequencer to operate properly, it is of course necessary that during the PLAY MODE, it return to the synthesizer the same voltage levels as were produced by the synthesizer during the LOAD MODE. In order to do this in a manner which minimizes the error rate attributable to noise,

the staircase wave form produced by the converter 50 during the LOAD MODE, is offset by one half-level from the staircase characteristic exhibited by the converter during the PLAY MODE.

In order to gain a better understanding of the foregoing, attention is called to FIG. 4 which, on the left, depicts the sixty four different voltage levels produced by the converter during the PLAY MODE. The voltage levels are represented as comprising a multiple of some unit voltage (e.g., 0.1 volts). Thus, voltage levels 0, 2, 4, 6; 8 ... 122, 124, 126 are shown which are produced by the converter 50 in response to the six bit P counter codes illustrated, the converter also responding to a seventh least significant bit which is always 0 during the PLAY MODE. These sixty four voltage levels correspond exactly to the voltage levels ideally produced by the synthesizer during the LOAD MODE. However, during the LOAD MODE, there may be small amounts of noise superimposed on the voltage supplied by the synthesizer. For example, a voltage level of 4.0 units may have a value of 4.5 units at the input to analog comparator 52. In order to assure that a 4.0 unit voltage is returned to the synthesizer, the staircase waveform produced by the converter 50 during the LOAD MODE is offset as shown in FIG. 4. This is accomplished by merely changing the state of the seventh least significant bit to 1. As a consequence, the 4.5 unit voltage supplied to the comparator 52 from switch contact 33 will produce a six bit field in the P counter for storage in memory 16 of 000010. On play-back during the PLAY MODE, this six bit order will produce the 4.0 unit voltage desired for application to the synthesizer.

Attention is now called to FIG. 5 which depicts the circuitry employed to implement the further feature of enabling a melody to be transposed as it is played back. Transposition, of course, involves changing the key of a melody or in other words shifting the pitch of all notes in the melody either up or down. In accordance with the present invention, transposition is achieved by incorporating controllable amplification means at the output of the digital to analog converter 50 to enable the voltage levels produced by the converter to be shifted in response to manually operable transpose switches on the sequencer. Since the voltage level establishes the pitch of a note played, the key of a melody can be varied by varying the voltage levels.

More particularly, as shown in FIG. 5, the output (A) of converter 50 is connected through a resistor of value R₁ to the input of operational amplifier 140, having a feedback resistor of value R₂. A variable voltage (B) is supplied to the input through a resistor of value R₃. Thus, the operational amplifier 140 will produce an output voltage C where

$$C = -R_2 \left(\frac{A}{R_1} + \frac{B}{R_3} \right)$$

Therefore, by controlling the voltage B, the voltage level C supplied to the synthesizer will be controlled.

For simplicity in explanation, it will be assumed that it is desired to be able to transpose an original melody to three different keys. In order to do this, three electronic or electromechanical switches 142₁, 142₂, 142₃ are provided for respectively applying different voltages B to the amplifier 140. The switches 142 are re-

spectively responsive to flip-flops 144₁, 144₂, 144₃, which in turn are set by manual transpose switches 146₁, 146₂, 146₃, available to the user. The switches 146 are connected to the flip-flops 144 such that actuation of a switch sets the flip-flop to which it is connected and resets the other two flip-flops 144 via OR gates 148. The transpose circuit of FIG. 5 is intended to be active only during the PLAY MODE and consequently the flip-flops 144 are all reset whenever the LOAD MODE occurs.

From the foregoing, it should now be appreciated that a sequencer apparatus has been disclosed herein capable of operating in combination with an electronic music synthesizer for storing digital representations of a sequence of notes played on the synthesizer, while the synthesizer is being played. That is, it should be recognized that as the synthesizer keyboard is played to produce a trigger pulse and a discrete analog voltage for each note, the sequencer, in accordance with the present invention, will store a six-bit digital representation of the notes pitch and an eight-bit representation of the duration occurring between adjacent trigger pulses in a sequence. After a sequence of notes has been stored in the sequencer memory in digital form, the sequencer is operable in a PLAY MODE to access the stored digital notes in the sequence in which they were loaded for reconversion to analog form for application to the synthesizer.

It should be recognized that a preferred embodiment of the invention has been described herein and that numerous changes and modifications may occur to those skilled in the art without departing from the spirit and scope of the invention.

The embodiments of the invention in which an exclusive property of privilege is claimed are defined as follows:

1. In combination with an electronic music synthesizer having a keyboard and means responsive to the playing of each key for producing a trigger pulse and an analog voltage level representative of pitch, a sequencer apparatus responsive to the playing of a sequence of keys for storing information describing the melody represented thereby, said sequencer apparatus comprising:

duration logic means responsive to each trigger pulse subsequent to the initial trigger pulse in a sequence, for providing a multibit digital code representing the time duration since the immediately preceding trigger pulse;

level logic means for providing a multibit digital code representing the level of analog voltage after each trigger pulse;

memory means comprised of a plurality of word locations each for storing a multibit word; and

means responsive to each trigger pulse provided by said duration logic means subsequent to the initial trigger pulse in a sequence for successively storing digital words in sequential locations of said memory means, each word comprised of a first digital code representative of time duration provided by said duration logic means and a second digital code representative of analog voltage level provided by said level logic means.

2. The combination of claim 1 wherein said means for storing words in sequential locations of said memory means includes addressing means for identifying a word location; and

means for incrementing said addressing means after each word is stored in said memory means.

3. The combination of claim 2 including means for reading a word from the word location identified by said addressing means;

means for incrementing said addressing means after each word is read from said memory means; and means responsive to the duration represented in a read word for controlling when the next word is read by said reading means.

4. The combination of claim 3 including means responsive to the digital code in each read word representing analog voltage level for producing an analog voltage for application to said synthesizer.

5. The combination of claim 4 wherein said means for controlling when the next word is read includes a source of timing pulses and means for counting said timing pulses; and

tempo control means for varying the rate of said timing pulses to thereby vary the rate at which said analog voltages are applied to said synthesizer.

6. The combination of claim 4 wherein said means for producing an analog voltage includes:

transpose control means for varying the level of said analog voltage.

7. The combination of claim 1 wherein said synthesizer includes analog input and output terminals and trigger pulse input and output terminals and wherein said sequencer apparatus includes analog input and output terminals and trigger pulse input and output terminals; and

switch means operable in a LOAD position to couple said synthesizer analog output terminal to both said sequencer analog input terminal and said synthesizer analog input terminal and said synthesizer trigger pulse output terminal to both said sequencer trigger pulse input terminal and said synthesizer trigger pulse input terminal and operable in a PLAY position to couple said sequencer analog and trigger pulse output terminals to said synthesizer analog and trigger pulse input terminals, respectively.

8. The combination of claim 1, wherein said means for providing a digital code representing time duration includes:

pulse source means producing a train of timing pulses;

digital counting means for counting said timing pulses; and

means responsive to each trigger pulse for resetting said digital counting means.

9. The combination of claim 1 wherein said means for providing a code representing the level of analog voltage includes:

pulse source means producing a train of pulses;

digital counting means responsive to said pulse source means for counting said pulses;

converter means responsive to said digital counting means for producing an analog signal equivalent to the count accumulated by said digital counting means; and

analog comparison means for inhibiting said digital counting means in response to said analog signal produced by said converter means being equal to said analog voltage level produced by said synthesizer.

10. Apparatus useful with a music synthesizer including (1) a keyboard and (2) means for producing a trigger pulse and an analog signal representative of pitch in response to each key actuation, said apparatus comprising:

means producing a train of timing pulses;
first means for counting said timing pulses;
means responsive to the count accumulated by said first means for producing an analog signal representative thereof;

means for comparing said analog signal representative of the accumulated count with an analog signal produced by a synthesizer to provide a match signal indicating when the compared analog signals match;

memory means for storing a plurality of counts;
means responsive to said match signal for transferring the count representative of pitch accumulated by said first means to said memory means;

second means for counting said timing pulses occurring between successive trigger pulses produced by a synthesizer to develop a count representative of the duration between successive key actuations; and

means for storing said count representative of duration in said memory means.

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11. The apparatus of claim 10 wherein said memory means includes a plurality of word location each capable of storing a pitch count and a duration count and address means for identifying each of said word locations; and

means for incrementing said address means subsequent to each storing of said counts in a word location.

12. The apparatus of claim 11 including means for reading the contents of the word location identified by said means;

means for incrementing said address means after reading the contents of a word location; and
means responsive to the duration count read from a word location for controlling when the contents of a word location is next to be read.

13. The apparatus of claim 12 including means responsive to the pitch count read from a word location for producing an analog signal representative thereof.

14. The apparatus of claim 13 wherein said means for producing said analog signal responsive to said first means and said means for producing said analog signal responsive to said pitch count define digital to analog conversion characteristics offset with respect to another.

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