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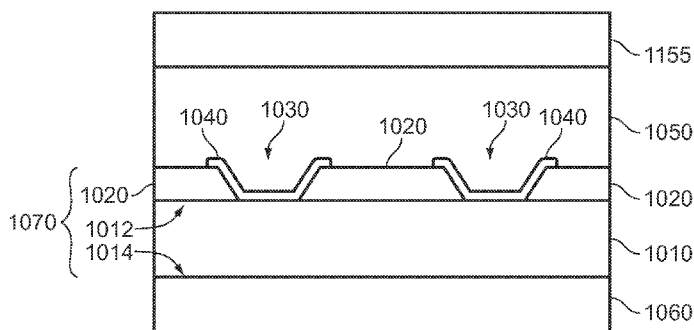
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(54) Title: DISPLAY DEVICE AND DUAL-SIDED PROCESS FOR FORMING LIGHT TURNING FEATURES AND DISPLAY ELEMENTS



(57) Abstract: This disclosure provides systems, methods and apparatus for providing illumination by using a light guide to distribute light. In an aspect, an illumination system is provided with a substrate having a first side and a second side opposite the first. The substrate can be optically transmissive and form part of the light guide for distributing light. The first side of the substrate is processed using a first processing technology. Processing the first side includes forming a light turning feature on the first side and forming a protective layer over the light turning feature. The second side is processed using a second processing technology to form display elements, while the protective layer protects the first side from damage. The first and second processing technologies can be performed using the same tool set. In addition to protecting the first side, the protective layer may function as an optical cladding and/or passivation layer.

DISPLAY DEVICE AND DUAL-SIDED PROCESS FOR FORMING LIGHT TURNING FEATURES AND DISPLAY ELEMENTS

TECHNICAL FIELD

[0001] This disclosure relates to illumination systems, including illumination systems for displays, particularly illumination systems having light guides with light turning features, and to electromechanical systems.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0002] Electromechanical systems include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components (e.g., mirrors) and electronics. Electromechanical systems can be manufactured at a variety of scales including, but not limited to, microscales and nanoscales. For example, microelectromechanical systems (MEMS) devices can include structures having sizes ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or deposited material layers, or that add layers to form electrical and electromechanical devices.

[0003] One type of electromechanical systems device is called an interferometric modulator (IMOD). As used herein, the term interferometric modulator or interferometric light modulator refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In some implementations, an interferometric modulator may include a pair of conductive plates, one or both of which may be transparent and/or reflective, wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In an implementation, one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap. The position of one plate in relation to another can change the optical interference of light incident on the interferometric modulator. Interferometric modulator devices have a wide range of

applications, and are anticipated to be used in improving existing products and creating new products, especially those with display capabilities.

[0004] Reflected ambient light is used to form images in some display devices, such as reflective displays using display elements formed by interferometric modulators. The perceived brightness of these displays depends upon the amount of light that is reflected towards a viewer. In low ambient light conditions, light from an illumination device with an artificial light source can be used to illuminate the reflective display elements, which then reflect the light towards a viewer to generate an image. To meet market demands and design criteria for display devices, including reflective and transmissive displays, new illumination devices and methods for forming them are continually being developed.

SUMMARY

[0005] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0006] One innovative aspect of the subject matter described in this disclosure can be implemented in a method of manufacturing a display device. The method includes providing a substrate having a first side and a second side opposite the first side. The method further includes processing the first side using a first processing technology. Processing the first side includes forming a plurality of light turning features on the first side of the substrate. Processing the first side further includes forming a first protective layer over the light turning features and subsequently processing the second side using a second processing technology. Processing the second side includes forming an array of display elements on the second side of the substrate. In an implementation, the first processing technology can use substantially the same tool set as the second processing technology. In an implementation, the first protective layer can be a scratch resistant layer. In an implementation, the first protective layer can be resistant to etch chemistries for forming the array of display elements.

[0007] Another innovative aspect of the subject matter described in this disclosure can be implemented in a display device. The display device includes a substrate having a first side and a second side opposite the first side. The display device further includes a

plurality of light turning features defined by indentations on the first side. The display device further includes a substantially planar first protective layer over the light turning features and substantially extending into the indentations. The display device further includes an array of display elements formed on the second side. In an implementation, the array of display elements can be formed directly in contact with the substrate. In an implementation, the substrate can constitute a light guide.

[0008] Another innovative aspect of the subject matter described in this disclosure can be implemented in a display device. The display device includes a substrate having a first side and a second side opposite the first side. The display device further includes a plurality of light turning features on the first side. The display device further includes means for protecting the light turning features and an array of display elements formed on the second side. In an implementation, the means for protecting can include an optical cladding layer. In an implementation, the means for protecting can include a passivating layer. In an implementation, the plurality of light turning features can be formed in indentations on the first side of the substrate, and the means for protecting can include a scratch-resistant layer extending into the indentations.

[0009] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device.

[0011] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display.

[0012] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1.

[0013] Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied.

[0014] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2.

[0015] Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A.

[0016] Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1.

[0017] Figures 6B–6E show examples of cross-sections of varying implementations of interferometric modulators.

[0018] Figure 7 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0019] Figures 8A–8E show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0020] Figure 9 shows an example of a cross-section of an illumination system.

[0021] Figures 10A–D show examples of cross-sectional schematic illustrations of various stages in a method of making an integrated light and display element array, according to some implementations.

[0022] Figures 11A–B show examples of cross-sectional schematic illustrations of various stages in a method of making an integrated light and display element array, according to some other implementations.

[0023] Figure 12A shows a cross-sectional schematic illustration of some implementations of the light guide of Figures 10A-11B.

[0024] Figure 12B shows a cross-sectional schematic illustration of another implementation of the light guide of Figures 10A-11B.

[0025] Figure 12C shows a cross-sectional schematic illustration of yet another implementation of the light guide of Figures 10A-11B.

[0026] Figure 13 shows an example of a flow diagram illustrating a manufacturing process for an integrated light and display element array.

[0027] Figures 14A and 14B show examples of system block diagrams illustrating a display device that includes a plurality of interferometric modulators.

[0028] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0029] The following detailed description is directed to certain implementations for the purposes of describing the innovative aspects. However, the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented in any device that is configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual, graphical or pictorial. More particularly, it is contemplated that the implementations may be implemented in or associated with a variety of electronic devices such as, but not limited to, mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, Bluetooth® devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, tablets, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (e.g., e-readers), computer monitors, auto displays (e.g., odometer display, etc.), cockpit controls and/or displays, camera view displays (e.g., display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (e.g., MEMS and non-MEMS), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of electromechanical systems devices. The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes, and electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to a person having ordinary skill in the art.

[0030] In some implementations, an illumination system is provided with a substrate having a first side and a second side opposite the first. The substrate can be optically transmissive and form part of a light guide for distributing light. The first side of the substrate can be processed using a first processing technology. In some implementations, the first processing technology can involve using a particular processing tool set (such as a first set of processing equipment or a first processing chamber). The first processing technology can be utilized for one or more first deposition and/or patterning processes, which can create one or more first structures.

[0031] The second side can be processed using a second processing technology, while the protective layer protects the first side from damage. In some implementations, the second processing technology can involve using a particular processing tool set and can include one or more second deposition and/or patterning processes. The second processing technology can create one or more structures, which can be different from the structures formed on the first side. For example, processing the second side can include forming a display element on the second side of the substrate. Note that the first and second processing technologies can utilize the same tool set (for example, the same processing equipment or process chamber).

[0032] In some implementations, processing the first side of the substrate can include forming light turning features on the first side and forming a first protective layer over the light turning features. In addition to protecting the first side, the first protective layer may function as an optical cladding and/or passivation layer. In some implementations, a second protective layer can be formed over the protective layer. Relative to the first protective layer, the second protective layer can have a higher scratch resistance and/or resistance to reaction with chemistries in the second processing technology, in some implementations.

[0033] The illumination system may be an integrated device that includes a display and a display light for illuminating the display. For example, the light turning features can be configured to turn light propagating inside the substrate so that the light exits the substrate and impinges on the display elements, thereby illuminating the display formed by the display elements. Thus, the substrate can function both as a light guide for the illumination function and as a support for the display elements during fabrication of those

display elements. In addition, in some implementations, the protective layer can protect the light turning features during the fabrication of the display elements and also act as a cladding layer to facilitate propagation of light within the light guide by total internal reflection and/or as a passivation layer.

[0034] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. For example, various implementations of the methods disclosed herein allow integrated fabrication of both display elements and light-turning features on a single substrate. In contrast, separately forming and combining the display elements with a light guide having the display elements can be costly, and the interface between the light guide and a display substrate can interfere with light transmission, reducing the brightness of the end device. For example, there may be undesirable Fresnel reflections at the interface between the light guide and the display substrate. Accordingly, an integrated device having a substrate that both supports display elements during fabrication and that can function as part of a display light can improve the brightness of the front light and reduce the fabrication cost. In addition, various implementations of the methods disclosed herein provide a substantially planar protective layer over a first side of the integrated substrate. The protective layer can help alleviate potential problems including, but not limited to: process damage to the first side from chemicals used during processing of the second side, scratch and handling damage to the first side from contact with processing surfaces and robot end-effectors during processing of the second side, contamination of front-end process systems by damaged light turning feature parts that have been removed from the first side during processing of the second side, contamination of the light turning features by particulate matter present during processing of the second side, and vacuum sensor errors during processing of the second side due to protrusions in the surface of the first side. In addition, the protective layer may also function as a cladding layer and/or passivation layer, thereby facilitating propagation of light in the display light and/or reducing corrosion in the light turning features, where the light turning features are provided with parts, such as metallic reflective layers, that are sensitive to corrosion. One or more of these potential advantages can reduce the time and/or cost of

manufacture, and increase the manufacturing yield, while also improving display performance.

[0035] An example of a suitable MEMS device, to which the described implementations may apply, is a reflective display device. Reflective display devices can incorporate interferometric modulators (IMODs) to selectively absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the optical resonant cavity and thereby affect the reflectance of the interferometric modulator. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors. The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

[0036] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state. In the bright (“relaxed,” “open” or “on”) state, the display element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark (“actuated,” “closed” or “off”) state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to black and white.

[0037] The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The movable reflective layer may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated

position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when actuated, reflecting light outside of the visible range (e.g., infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0038] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators 12. In the IMOD 12 on the left (as illustrated), a movable reflective layer 14 is illustrated in a relaxed position at a predetermined distance from an optical stack 16, which includes a partially reflective layer. The voltage V_0 applied across the IMOD 12 on the left is insufficient to cause actuation of the movable reflective layer 14. In the IMOD 12 on the right, the movable reflective layer 14 is illustrated in an actuated position near or adjacent the optical stack 16. The voltage V_{bias} applied across the IMOD 12 on the right is sufficient to maintain the movable reflective layer 14 in the actuated position.

[0039] In Figure 1, the reflective properties of pixels 12 are generally illustrated with arrows indicating light 13 incident upon the pixels 12, and light 15 reflecting from the pixel 12 on the left. Although not illustrated in detail, it will be understood by a person having ordinary skill in the art that most of the light 13 incident upon the pixels 12 will be transmitted through the transparent substrate 20, toward the optical stack 16. A portion of the light incident upon the optical stack 16 will be transmitted through the partially reflective layer of the optical stack 16, and a portion will be reflected back through the transparent substrate 20. The portion of light 13 that is transmitted through the optical stack 16 will be reflected at the movable reflective layer 14, back toward (and through) the transparent substrate 20. Interference (constructive or destructive) between the light reflected from the partially reflective layer of the optical stack 16 and the light

reflected from the movable reflective layer 14 will determine the wavelength(s) of light 15 reflected from the pixel 12.

[0040] The optical stack 16 can include a single layer or several layers. The layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer and a transparent dielectric layer. In some implementations, the optical stack 16 is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate 20. The electrode layer can be formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a combination of materials. In some implementations, the optical stack 16 can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack 16 or of other structures of the IMOD) can serve to bus signals between IMOD pixels. The optical stack 16 also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0041] In some implementations, the layer(s) of the optical stack 16 can be patterned into parallel strips, and may form row electrodes in a display device as described further below. As will be understood by one having skill in the art, the term “patterned” is used herein to refer to masking as well as etching processes. In some implementations, a highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer 14, and these strips may form column electrodes in a display device. The movable reflective layer 14 may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack 16) to form columns deposited on top of posts 18 and an intervening sacrificial material deposited between the posts 18. When the sacrificial material is etched away, a defined gap 19, or optical cavity, can be formed between the movable reflective layer 14 and the

optical stack 16. In some implementations, the spacing between posts 18 may be on the order of 1–1000 μm , while the gap 19 may be on the order of $< 10,000$ Angstroms ($\text{\AA}$).

[0042] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer 14 remains in a mechanically relaxed state, as illustrated by the pixel 12 on the left in Figure 1, with the gap 19 between the movable reflective layer 14 and optical stack 16. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer 14 can deform and move near or against the optical stack 16. A dielectric layer (not shown) within the optical stack 16 may prevent shorting and control the separation distance between the layers 14 and 16, as illustrated by the actuated pixel 12 on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as “rows” or “columns,” a person having ordinary skill in the art will readily understand that referring to one direction as a “row” and another as a “column” is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows. Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an “array”), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a “mosaic”). The terms “array” and “mosaic” may refer to either configuration. Thus, although the display is referred to as including an “array” or “mosaic,” the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

[0043] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display. The electronic device includes a processor 21 that may be configured to execute one or more software modules. In addition to executing an operating system, the processor 21 may be

configured to execute one or more software applications, including a web browser, a telephone application, an email program, or any other software application.

[0044] The processor 21 can be configured to communicate with an array driver 22. The array driver 22 can include a row driver circuit 24 and a column driver circuit 26 that provide signals to, e.g., a display array or panel 30. The cross section of the IMOD display device illustrated in Figure 1 is shown by the lines 1–1 in Figure 2. Although Figure 2 illustrates a 3x3 array of IMODs for the sake of clarity, the display array 30 may contain a very large number of IMODs, and may have a different number of IMODs in rows than in columns, and vice versa.

[0045] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1. For MEMS interferometric modulators, the row/column (i.e., common/segment) write procedure may take advantage of a hysteresis property of these devices as illustrated in Figure 3. An interferometric modulator may require, for example, about a 10-volt potential difference to cause the movable reflective layer, or mirror, to change from the relaxed state to the actuated state. When the voltage is reduced from that value, the movable reflective layer maintains its state as the voltage drops back below, e.g., 10-volts, however, the movable reflective layer does not relax completely until the voltage drops below 2-volts. Thus, a range of voltage, approximately 3 to 7-volts, as shown in Figure 3, exists where there is a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the “hysteresis window” or “stability window.” For a display array 30 having the hysteresis characteristics of Figure 3, the row/column write procedure can be designed to address one or more rows at a time, such that during the addressing of a given row, pixels in the addressed row that are to be actuated are exposed to a voltage difference of about 10-volts, and pixels that are to be relaxed are exposed to a voltage difference of near zero volts. After addressing, the pixels are exposed to a steady state or bias voltage difference of approximately 5-volts such that they remain in the previous strobing state. In this example, after being addressed, each pixel sees a potential difference within the “stability window” of about 3–7-volts. This hysteresis property feature enables the pixel design, e.g., illustrated in Figure 1, to remain stable in either an actuated or relaxed pre-existing state under the

same applied voltage conditions. Since each IMOD pixel, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be held at a steady voltage within the hysteresis window without substantially consuming or losing power. Moreover, essentially little or no current flows into the IMOD pixel if the applied voltage potential remains substantially fixed.

[0046] In some implementations, a frame of an image may be created by applying data signals in the form of “segment” voltages along the set of column electrodes, in accordance with the desired change (if any) to the state of the pixels in a given row. Each row of the array can be addressed in turn, such that the frame is written one row at a time. To write the desired data to the pixels in a first row, segment voltages corresponding to the desired state of the pixels in the first row can be applied on the column electrodes, and a first row pulse in the form of a specific “common” voltage or signal can be applied to the first row electrode. The set of segment voltages can then be changed to correspond to the desired change (if any) to the state of the pixels in the second row, and a second common voltage can be applied to the second row electrode. In some implementations, the pixels in the first row are unaffected by the change in the segment voltages applied along the column electrodes, and remain in the state they were set to during the first common voltage row pulse. This process may be repeated for the entire series of rows, or alternatively, columns, in a sequential fashion to produce the image frame. The frames can be refreshed and/or updated with new image data by continually repeating this process at some desired number of frames per second.

[0047] The combination of segment and common signals applied across each pixel (that is, the potential difference across each pixel) determines the resulting state of each pixel. Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied. As will be readily understood by one having ordinary skill in the art, the “segment” voltages can be applied to either the column electrodes or the row electrodes, and the “common” voltages can be applied to the other of the column electrodes or the row electrodes.

[0048] As illustrated in Figure 4 (as well as in the timing diagram shown in Figure 5B), when a release voltage $V_{C_{REL}}$ is applied along a common line, all interferometric modulator elements along the common line will be placed in a relaxed state, alternatively

referred to as a released or unactuated state, regardless of the voltage applied along the segment lines, i.e., high segment voltage VS_H and low segment voltage VS_L . In particular, when the release voltage VC_{REL} is applied along a common line, the potential voltage across the modulator (alternatively referred to as a pixel voltage) is within the relaxation window (see Figure 3, also referred to as a release window) both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line for that pixel.

[0049] When a hold voltage is applied on a common line, such as a high hold voltage VC_{HOLD_H} or a low hold voltage VC_{HOLD_L} , the state of the interferometric modulator will remain constant. For example, a relaxed IMOD will remain in a relaxed position, and an actuated IMOD will remain in an actuated position. The hold voltages can be selected such that the pixel voltage will remain within a stability window both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line. Thus, the segment voltage swing, i.e., the difference between the high VS_H and low segment voltage VS_L , is less than the width of either the positive or the negative stability window.

[0050] When an addressing, or actuation, voltage is applied on a common line, such as a high addressing voltage VC_{ADD_H} or a low addressing voltage VC_{ADD_L} , data can be selectively written to the modulators along that line by application of segment voltages along the respective segment lines. The segment voltages may be selected such that actuation is dependent upon the segment voltage applied. When an addressing voltage is applied along a common line, application of one segment voltage will result in a pixel voltage within a stability window, causing the pixel to remain unactuated. In contrast, application of the other segment voltage will result in a pixel voltage beyond the stability window, resulting in actuation of the pixel. The particular segment voltage which causes actuation can vary depending upon which addressing voltage is used. In some implementations, when the high addressing voltage VC_{ADD_H} is applied along the common line, application of the high segment voltage VS_H can cause a modulator to remain in its current position, while application of the low segment voltage VS_L can cause actuation of the modulator. As a corollary, the effect of the segment voltages can be the opposite when a low addressing voltage VC_{ADD_L} is applied, with high segment

voltage VS_H causing actuation of the modulator, and low segment voltage VS_L having no effect (i.e., remaining stable) on the state of the modulator.

[0051] In some implementations, hold voltages, address voltages, and segment voltages may be used which always produce the same polarity potential difference across the modulators. In some other implementations, signals can be used which alternate the polarity of the potential difference of the modulators. Alternation of the polarity across the modulators (that is, alternation of the polarity of write procedures) may reduce or inhibit charge accumulation which could occur after repeated write operations of a single polarity.

[0052] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2. Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A. The signals can be applied to the, e.g., 3x3 array of Figure 2, which will ultimately result in the line time 60e display arrangement illustrated in Figure 5A. The actuated modulators in Figure 5A are in a dark-state, i.e., where a substantial portion of the reflected light is outside of the visible spectrum so as to result in a dark appearance to, e.g., a viewer. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, but the write procedure illustrated in the timing diagram of Figure 5B presumes that each modulator has been released and resides in an unactuated state before the first line time 60a.

[0053] During the first line time 60a: a release voltage 70 is applied on common line 1; the voltage applied on common line 2 begins at a high hold voltage 72 and moves to a release voltage 70; and a low hold voltage 76 is applied along common line 3. Thus, the modulators (common 1, segment 1), (1,2) and (1,3) along common line 1 remain in a relaxed, or unactuated, state for the duration of the first line time 60a, the modulators (2,1), (2,2) and (2,3) along common line 2 will move to a relaxed state, and the modulators (3,1), (3,2) and (3,3) along common line 3 will remain in their previous state. With reference to Figure 4, the segment voltages applied along segment lines 1, 2 and 3 will have no effect on the state of the interferometric modulators, as none of common lines 1, 2 or 3 are being exposed to voltage levels causing actuation during line time 60a (i.e., VC_{REL} – relax and VC_{HOLD_L} – stable).

[0054] During the second line time 60b, the voltage on common line 1 moves to a high hold voltage 72, and all modulators along common line 1 remain in a relaxed state regardless of the segment voltage applied because no addressing, or actuation, voltage was applied on the common line 1. The modulators along common line 2 remain in a relaxed state due to the application of the release voltage 70, and the modulators (3,1), (3,2) and (3,3) along common line 3 will relax when the voltage along common line 3 moves to a release voltage 70.

[0055] During the third line time 60c, common line 1 is addressed by applying a high address voltage 74 on common line 1. Because a low segment voltage 64 is applied along segment lines 1 and 2 during the application of this address voltage, the pixel voltage across modulators (1,1) and (1,2) is greater than the high end of the positive stability window (i.e., the voltage differential exceeded a predefined threshold) of the modulators, and the modulators (1,1) and (1,2) are actuated. Conversely, because a high segment voltage 62 is applied along segment line 3, the pixel voltage across modulator (1,3) is less than that of modulators (1,1) and (1,2), and remains within the positive stability window of the modulator; modulator (1,3) thus remains relaxed. Also during line time 60c, the voltage along common line 2 decreases to a low hold voltage 76, and the voltage along common line 3 remains at a release voltage 70, leaving the modulators along common lines 2 and 3 in a relaxed position.

[0056] During the fourth line time 60d, the voltage on common line 1 returns to a high hold voltage 72, leaving the modulators along common line 1 in their respective addressed states. The voltage on common line 2 is decreased to a low address voltage 78. Because a high segment voltage 62 is applied along segment line 2, the pixel voltage across modulator (2,2) is below the lower end of the negative stability window of the modulator, causing the modulator (2,2) to actuate. Conversely, because a low segment voltage 64 is applied along segment lines 1 and 3, the modulators (2,1) and (2,3) remain in a relaxed position. The voltage on common line 3 increases to a high hold voltage 72, leaving the modulators along common line 3 in a relaxed state.

[0057] Finally, during the fifth line time 60e, the voltage on common line 1 remains at high hold voltage 72, and the voltage on common line 2 remains at a low hold voltage 76, leaving the modulators along common lines 1 and 2 in their respective addressed

states. The voltage on common line 3 increases to a high address voltage 74 to address the modulators along common line 3. As a low segment voltage 64 is applied on segment lines 2 and 3, the modulators (3,2) and (3,3) actuate, while the high segment voltage 62 applied along segment line 1 causes modulator (3,1) to remain in a relaxed position. Thus, at the end of the fifth line time 60e, the 3x3 pixel array is in the state shown in Figure 5A, and will remain in that state as long as the hold voltages are applied along the common lines, regardless of variations in the segment voltage which may occur when modulators along other common lines (not shown) are being addressed.

[0058] In the timing diagram of Figure 5B, a given write procedure (i.e., line times 60a–60e) can include the use of either high hold and address voltages, or low hold and address voltages. Once the write procedure has been completed for a given common line (and the common voltage is set to the hold voltage having the same polarity as the actuation voltage), the pixel voltage remains within a given stability window, and does not pass through the relaxation window until a release voltage is applied on that common line. Furthermore, as each modulator is released as part of the write procedure prior to addressing the modulator, the actuation time of a modulator, rather than the release time, may determine the necessary line time. Specifically, in implementations in which the release time of a modulator is greater than the actuation time, the release voltage may be applied for longer than a single line time, as depicted in Figure 5B. In some other implementations, voltages applied along common lines or segment lines may vary to account for variations in the actuation and release voltages of different modulators, such as modulators of different colors.

[0059] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 6A–6E show examples of cross-sections of varying implementations of interferometric modulators, including the movable reflective layer 14 and its supporting structures. Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1, where a strip of metal material, i.e., the movable reflective layer 14 is deposited on supports 18 extending orthogonally from the substrate 20. In Figure 6B, the movable reflective layer 14 of each IMOD is generally square or rectangular in shape and attached to supports at or near the corners, on tethers 32. In Figure 6C, the movable

reflective layer 14 is generally square or rectangular in shape and suspended from a deformable layer 34, which may include a flexible metal. The deformable layer 34 can connect, directly or indirectly, to the substrate 20 around the perimeter of the movable reflective layer 14. These connections are herein referred to as support posts. The implementation shown in Figure 6C has additional benefits deriving from the decoupling of the optical functions of the movable reflective layer 14 from its mechanical functions, which are carried out by the deformable layer 34. This decoupling allows the structural design and materials used for the reflective layer 14 and those used for the deformable layer 34 to be optimized independently of one another.

[0060] Figure 6D shows another example of an IMOD, where the movable reflective layer 14 includes a reflective sub-layer 14a. The movable reflective layer 14 rests on a support structure, such as support posts 18. The support posts 18 provide separation of the movable reflective layer 14 from the lower stationary electrode (i.e., part of the optical stack 16 in the illustrated IMOD) so that a gap 19 is formed between the movable reflective layer 14 and the optical stack 16, for example when the movable reflective layer 14 is in a relaxed position. The movable reflective layer 14 also can include a conductive layer 14c, which may be configured to serve as an electrode, and a support layer 14b. In this example, the conductive layer 14c is disposed on one side of the support layer 14b, distal from the substrate 20, and the reflective sub-layer 14a is disposed on the other side of the support layer 14b, proximal to the substrate 20. In some implementations, the reflective sub-layer 14a can be conductive and can be disposed between the support layer 14b and the optical stack 16. The support layer 14b can include one or more layers of a dielectric material, for example, silicon oxynitride (SiON) or silicon dioxide (SiO₂). In some implementations, the support layer 14b can be a stack of layers, such as, for example, a SiO₂/SiON/SiO₂ tri-layer stack. Either or both of the reflective sub-layer 14a and the conductive layer 14c can include, e.g., an aluminum (Al) alloy with about 0.5% copper (Cu), or another reflective metallic material. Employing conductive layers 14a, 14c above and below the dielectric support layer 14b can balance stresses and provide enhanced conduction. In some implementations, the reflective sub-layer 14a and the conductive layer 14c can be formed of different materials for a variety

of design purposes, such as achieving specific stress profiles within the movable reflective layer 14.

[0061] As illustrated in Figure 6D, some implementations also can include a black mask structure 23. The black mask structure 23 can be formed in optically inactive regions (e.g., between pixels or under posts 18) to absorb ambient or stray light. The black mask structure 23 also can improve the optical properties of a display device by inhibiting light from being reflected from or transmitted through inactive portions of the display, thereby increasing the contrast ratio. Additionally, the black mask structure 23 can be conductive and be configured to function as an electrical bussing layer. In some implementations, the row electrodes can be connected to the black mask structure 23 to reduce the resistance of the connected row electrode. The black mask structure 23 can be formed using a variety of methods, including deposition and patterning techniques. The black mask structure 23 can include one or more layers. For example, in some implementations, the black mask structure 23 includes a molybdenum-chromium (MoCr) layer that serves as an optical absorber, a layer, and an aluminum alloy that serves as a reflector and a bussing layer, with a thickness in the range of about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively. The one or more layers can be patterned using a variety of techniques, including photolithography and dry etching, including, for example, carbon tetrafluoride (CF₄) and/or oxygen (O₂) for the MoCr and SiO₂ layers and chlorine (Cl₂) and/or boron trichloride (BCl₃) for the aluminum alloy layer. In some implementations, the black mask 23 can be an etalon or interferometric stack structure. In such interferometric stack black mask structures 23, the conductive absorbers can be used to transmit or bus signals between lower, stationary electrodes in the optical stack 16 of each row or column. In some implementations, a spacer layer 35 can serve to generally electrically isolate the absorber layer 16a from the conductive layers in the black mask 23.

[0062] Figure 6E shows another example of an IMOD, where the movable reflective layer 14 is self supporting. In contrast with Figure 6D, the implementation of Figure 6E does not include support posts 18. Instead, the movable reflective layer 14 contacts the underlying optical stack 16 at multiple locations, and the curvature of the movable reflective layer 14 provides sufficient support that the movable reflective layer 14 returns

to the unactuated position of Figure 6E when the voltage across the interferometric modulator is insufficient to cause actuation. The optical stack 16, which may contain a plurality of several different layers, is shown here for clarity including an optical absorber 16a, and a dielectric 16b. In some implementations, the optical absorber 16a may serve both as a fixed electrode and as a partially reflective layer.

[0063] In implementations such as those shown in Figures 6A–6E, the IMODs function as direct-view devices, in which images are viewed from the front side of the transparent substrate 20, i.e., the side opposite to that upon which the modulator is arranged. In these implementations, the back portions of the device (that is, any portion of the display device behind the movable reflective layer 14, including, for example, the deformable layer 34 illustrated in Figure 6C) can be configured and operated upon without impacting or negatively affecting the image quality of the display device, because the reflective layer 14 optically shields those portions of the device. For example, in some implementations a bus structure (not illustrated) can be included behind the movable reflective layer 14 which provides the ability to separate the optical properties of the modulator from the electromechanical properties of the modulator, such as voltage addressing and the movements that result from such addressing. Additionally, the implementations of Figures 6A–6E can simplify processing, such as, e.g., patterning.

[0064] Figure 7 shows an example of a flow diagram illustrating a manufacturing process 80 for an interferometric modulator, and Figures 8A–8E show examples of cross-sectional schematic illustrations of corresponding stages of such a manufacturing process 80. In some implementations, the manufacturing process 80 can be implemented to manufacture, e.g., interferometric modulators of the general type illustrated in Figures 1 and 6, in addition to other blocks not shown in Figure 7. With reference to Figures 1, 6 and 7, the process 80 begins at block 82 with the formation of the optical stack 16 over the substrate 20. Figure 8A illustrates such an optical stack 16 formed over the substrate 20. The substrate 20 may be a transparent substrate such as glass or plastic, it may be flexible or relatively stiff and unbending, and may have been subjected to prior preparation processes, e.g., cleaning, to facilitate efficient formation of the optical stack 16. As discussed above, the optical stack 16 can be electrically conductive, partially transparent and partially reflective and may be fabricated, for example, by depositing one

or more layers having the desired properties onto the transparent substrate 20. In Figure 8A, the optical stack 16 includes a multilayer structure having sub-layers 16a and 16b, although more or fewer sub-layers may be included in some other implementations. In some implementations, one of the sub-layers 16a, 16b can be configured with both optically absorptive and conductive properties, such as the combined conductor/absorber sub-layer 16a. Additionally, one or more of the sub-layers 16a, 16b can be patterned into parallel strips, and may form row electrodes in a display device. Such patterning can be performed by a masking and etching process or another suitable process known in the art. In some implementations, one of the sub-layers 16a, 16b can be an insulating or dielectric layer, such as sub-layer 16b that is deposited over one or more metal layers (e.g., one or more reflective and/or conductive layers). In addition, the optical stack 16 can be patterned into individual and parallel strips that form the rows of the display.

[0065] The process 80 continues at block 84 with the formation of a sacrificial layer 25 over the optical stack 16. The sacrificial layer 25 is later removed (e.g., at block 90) to form the cavity 19 and thus the sacrificial layer 25 is not shown in the resulting interferometric modulators 12 illustrated in Figure 1. Figure 8B illustrates a partially fabricated device including a sacrificial layer 25 formed over the optical stack 16. The formation of the sacrificial layer 25 over the optical stack 16 may include deposition of a xenon difluoride (XeF_2)-etchable material such as molybdenum (Mo) or amorphous silicon (a-Si), in a thickness selected to provide, after subsequent removal, a gap or cavity 19 (see also Figures 1 and 8E) having a desired design size. Deposition of the sacrificial material may be carried out using deposition techniques such as physical vapor deposition (PVD, e.g., sputtering), plasma-enhanced chemical vapor deposition (PECVD), thermal chemical vapor deposition (thermal CVD), or spin-coating.

[0066] The process 80 continues at block 86 with the formation of a support structure e.g., a post 18 as illustrated in Figures 1, 6 and 8C. The formation of the post 18 may include patterning the sacrificial layer 25 to form a support structure aperture, then depositing a material (e.g., a polymer or an inorganic material, e.g., silicon oxide) into the aperture to form the post 18, using a deposition method such as PVD, PECVD, thermal CVD, or spin-coating. In some implementations, the support structure aperture formed in the sacrificial layer can extend through both the sacrificial layer 25 and the optical stack

16 to the underlying substrate 20, so that the lower end of the post 18 contacts the substrate 20 as illustrated in Figure 6A. Alternatively, as depicted in Figure 8C, the aperture formed in the sacrificial layer 25 can extend through the sacrificial layer 25, but not through the optical stack 16. For example, Figure 8E illustrates the lower ends of the support posts 18 in contact with an upper surface of the optical stack 16. The post 18, or other support structures, may be formed by depositing a layer of support structure material over the sacrificial layer 25 and patterning portions of the support structure material located away from apertures in the sacrificial layer 25. The support structures may be located within the apertures, as illustrated in Figure 8C, but also can, at least partially, extend over a portion of the sacrificial layer 25. As noted above, the patterning of the sacrificial layer 25 and/or the support posts 18 can be performed by a patterning and etching process, but also may be performed by alternative etching methods.

[0067] The process 80 continues at block 88 with the formation of a movable reflective layer or membrane such as the movable reflective layer 14 illustrated in Figures 1, 6 and 8D. The movable reflective layer 14 may be formed by employing one or more depositions, e.g., reflective layer (e.g., aluminum, aluminum alloy) deposition, along with one or more patterning, masking, and/or etching operations. The movable reflective layer 14 can be electrically conductive, and referred to as an electrically conductive layer. In some implementations, the movable reflective layer 14 may include a plurality of sub-layers 14a, 14b, 14c as shown in Figure 8D. In some implementations, one or more of the sub-layers, such as sub-layers 14a, 14c, may include highly reflective sub-layers selected for their optical properties, and another sub-layer 14b may include a mechanical sub-layer selected for its mechanical properties. Since the sacrificial layer 25 is still present in the partially fabricated interferometric modulator formed at block 88, the movable reflective layer 14 is typically not movable at this stage. A partially fabricated IMOD that contains a sacrificial layer 25 may also be referred to herein as an “unreleased” IMOD. As described above in connection with Figure 1, the movable reflective layer 14 can be patterned into individual and parallel strips that form the columns of the display.

[0068] The process 80 continues at block 90 with the formation of a cavity, e.g., cavity 19 as illustrated in Figures 1, 6 and 8E. The cavity 19 may be formed by exposing

the sacrificial material 25 (deposited at block 84) to an etchant. For example, an etchable sacrificial material such as Mo or amorphous Si may be removed by dry chemical etching, e.g., by exposing the sacrificial layer 25 to a gaseous or vaporous etchant, such as vapors derived from solid XeF_2 for a period of time that is effective to remove the desired amount of material, typically selectively removed relative to the structures surrounding the cavity 19. Other etching methods, e.g. wet etching and/or plasma etching, also may be used. Since the sacrificial layer 25 is removed during block 90, the movable reflective layer 14 is typically movable after this stage. After removal of the sacrificial material 25, the resulting fully or partially fabricated IMOD may be referred to herein as a “released” IMOD.

[0069] Figure 9 shows an example of a cross-section of an illumination system. A light guide 1070 receives light from a light source 130. A plurality of light turning features 1030 in the light guide 1070 are configured to redirect light (e.g., light ray 150) from the light source 130 back towards an underlying array 1060 of display elements. The array 1060 of display elements can include reflective display elements that reflect the redirected light forward towards a viewer 170. In some implementations, the reflective display elements can include IMODs (such as the IMODs 12 shown in Figure 1). In some other implementations, the display elements can be transmissive and light can propagate through the array 1060 to a viewer (not shown) on a side of the array 1060 opposite the light guide 1070.

[0070] With continued reference to Figure 9, the light guide 1070 may be a substantially planar optical device coupled to, and parallel to, the array 1060 of display elements such that incident light passes through a thickness the light guide 1070 to the array 1060 of display elements, and light reflected from the array 1060 of display elements also passes back through the thickness of the light guide 1070 to the viewer 170, in implementations where the display elements are reflective.

[0071] The light source 130 may include any suitable light source, for example, an incandescent bulb, a edge bar, a light emitting diode (“LED”), a fluorescent lamp, an LED light bar, an array of LEDs, and/or another light source. In certain implementations, light from the light source 130 is injected into the light guide 1070 such that a portion of the light propagates in a direction across at least a portion of the light guide 1070 at a

low-graze angle relative to the surface of the light guide 1070 aligned with the array 1060 of display elements such that the light is reflected within the light guide 1070 by total internal reflection (“TIR”) off of the light guide’s first and second sides 1012 and 1014, respectively. In some implementations, optical cladding layers (not shown) having a lower refractive index (for example, 0.05 or 0.1 lower) than the light guide 1070 may be disposed at the first side 1012 and/or second side 1014 to facilitate TIR off those sides. In some implementations, the light source 130 injecting light into the light guide 1070 includes a light bar. Light entering the light bar from a light generating device (e.g., a LED) may propagate along some or all of the length of the bar and exit out of a surface or edge of the light bar over a portion or all of the length of the light bar. Light exiting the light bar may enter an edge of the light guide 1070, and then propagate within the light guide 1070.

[0072] The light turning features 1030 in the light guide 1070 redirect the light towards display elements in the array 1060 of display elements at an angle sufficient such that at least some of the light passes out of the light guide 1070 to the array 1060 of display elements. The redirected light passing out the light guide 1070 may be considered to be extracted out of the light guide 1070. The light turning features 1030 may include one or more layers of different materials (for example, described herein with respect to Figure 12A) referred in the aggregate as coating layers 1040. The coating layers 1040 can be configured to increase reflectivity of the turning feature 1030, for example, by including a reflective metal layer.

[0073] In some implementations, the light turning features 1030 are formed in the light guide 1070, and the IMODs (such as the IMODs 12 shown in Figure 1) are separately fabricated using the light guide 1070 as a substrate to support the display elements of the array 1060 during fabrication of those display elements. The light turning features 1030 can be formed in the light guide 1070 using a first processing technology, which can involve deposition and/or patterning, and the IMODs can be formed in the array 1060 of display elements using a second processing technology, which can also involve deposition and patterning. Both technologies may use the same tool set in some implementations.

[0074] In various implementations, a protective layer can protect the light turning features 1030 during subsequent processing, such as when using the second processing technology. In some implementations, the protective layer can be removed at the end of the fabrication process. In some implementations, the protective layer can remain at the end of the fabrication process as a protective, passivation, and/or cladding layer, as discussed herein. The protective layer can be made thick enough to protect the light turning features 1030 on a first side 1012 from chemical and/or mechanical damage during processing of the second side 1014. For example, the protective layer can be a scratch resistant and/or passivation layer. The passivation layer can reduce moisture absorption and chemical damage to underlying features. The passivation layer may provide a moisture or gas barrier to protect moisture-sensitive underlying features, such as metal-containing light turning features that may be present in the light guide 1070. Thus, corrosion or other undesired changes to the light turning features 1030 may be mitigated or avoided. In some implementations, the protective layer can also be planarized. Planarization of the protective layer can provide compatibility with processing equipment designed for use with substrates having flat substrate backsides.

[0075] Figures 10A–D show examples of cross-sectional schematic illustrations of various stages in a method of making an integrated light and display element array, according to some implementations. The method can provide both light turning features and display elements on opposite sides of a single substrate. Moreover, the method illustrated in Figures 10A–D may prepare surfaces of the light turning features for additional processing, for example, by providing a substantially planar top surface that facilitates integration (for example, attachment) with other structures.

[0076] Referring to Figure 10A, a partially formed display device including a substrate 1010, a light turning film 1020, one or more light turning features formed in indentations 1030, and a coating layer 1040 are provided. The substrate 1010 has first side 1012 and second side 1014, and the light turning film 1020 is disposed on the first side 1012. Both the turning film 1020 and substrate 1010 may be formed of a substantially optically transmissive material that allows light to propagate along the lengths thereof. For example, the turning film 1020 and substrate 1010 may each include one or more of the following materials: acrylics, acrylate copolymers, UV-curable resins,

polycarbonates, cycloolefin polymers, polymers, organic materials, inorganic materials, silicates, alumina, sapphire, glasses, polyethylene terephthalate ("PET"), polyethylene terephthalate glycol ("PET-G"), silicon oxy-nitride, and/or other optically transparent materials. For mechanical and chemical stability, the material forming the turning film 1020 may have a low moisture absorption, thermal and chemical resistance to materials and temperatures used in later processing, and limited or substantially no out-gassing. In some implementations, the light turning film 1020 can be a layer of SiON.

[0077] In some implementations, the light turning film 1020 is selectively patternable and has sufficient structural integrity to support the formation of the light turning features 1030 with angled sidewalls. While shown in isolation for ease of illustration and description, a plurality of light turning features 1030 may be distributed across the light turning film 1020. In the illustrated implementation, the light turning features 1030 in the light turning film 1020 extend all the way through the light turning film 1020 to the substrate 1010. In another implementation, the light turning features 1030 may not extend all the way through the light turning film 1020, and may not reach the substrate 1010. In another implementation, the light turning features 1030 may be formed directly in the substrate 1010 without providing a separate light turning film 1020. For example, the substrate 1010 may be patterned and etched to define recesses on the surface 1012 to form light turning features on the substrate 1010 directly.

[0078] Referring still to Figure 10A, the coating layer 1040 can be deposited over the light turning film 1020. The deposition may be a conformal blanket deposition, such as a chemical vapor deposition (CVD) or physical vapor deposition (PVD). The coating 1040 can be reflective, thereby facilitating the turning of light by the light turning features 1030. For example, the coating 1040 can be a reflective metal layer. In some implementations, the coatings 1040 can include a stack of two or more sequentially deposited constituent layers (such as, for example, the layers 1242, 1244, and 1246 described below with respect to Figure 12A). In an implementation, the light turning features 1030 can be between about 3 μm to about 10 μm in width. In an implementation, the light turning features 1030 can include sidewalls at angles of about 43° to about 47°.

[0079] Referring now to Figure 10B, a protective layer 1050 is formed over the light turning film 1020 and the coating layer 1040 on the first side 1012 of the substrate 1010. In various implementations, the protective layer 1050 can be chemically stable, thermally stable, and/or mechanically strong. The protective layer 1050 can protect the light turning features 1030 from mechanical abrasion, chemical attack, and/or extreme temperatures during processing of the second side 1014. In an implementation, the protective layer 1050 can be selected of a material and thickness sufficient to protect underlying layers from temperatures greater than 350° C which may occur, for example, during subsequent CVD processing. As another example, the protective layer 1050 can be selected of a material and thickness sufficient to protect underlying layers from etchants used during processing of the display elements on second side 1014. Examples of such etchants include a buffered oxide etch (BOE), a phosphoric acid stripper, tetramethylammonium hydroxide (TMAH), etc. In some implementations, the passivation layer has a moisture transmission coefficient of about 1g/m²/day or less, about 0.01g/m²/day or less, or about 0.0001g/m²/day or less, to protect underlying materials from corrosion. In some implementations, the moisture absorption per weight of the passivation layer is less than about 0.5%. In other words, the passivation layer may absorb less than about 0.5 g of moisture for every 100 g of passivation layer material. In some implementations, the passivation layer may have a low diffusion coefficient.

[0080] In some implementations, the protective layer 1050 can be formed using, for example, a material that forms a substantially planar surface as-deposited, or a material that can be made to have a substantially planar surface by subsequent processing after deposition. For example, the protective layer 1050 can be formed by spin coating a planarization polymer. The planarization polymer can be a high-temperature, low-refractive index polymer. Examples of planarization polymers include the organic polymers sold under the trademark AGC-ALX543™ by Asahi Glass Co. of Chiyoda-ku, Tokyo, Japan; AGC-ALX2000™ by Asahi Glass Co. of Chiyoda-ku, Tokyo, Japan, and/or HD-4100™ by HP Microsystems of Parlin, NJ. As another example, the protective layer 1050 can be formed by spin coating a spin-on glass material, including a patternable spin-on glass material. In various implementations, the protective layer 1050

can include a spin-on glass material such as the material sold under the trademark Accuglass T-12™ by Honeywell International, Inc. of Morristown, NJ, 512B™ by Honeywell International, Inc. of Morristown, NJ, PTS-R™ by Honeywell International, Inc. of Morristown, NJ, PTS-T™ by Honeywell International, Inc. of Morristown, NJ, and/or TOK-Trial 009™ by Tokyo Ohka Kogyo Co., Ltd. of Nakahara-ku, Kawasaki-shi, Kanagawa Prefecture, Japan. In various implementations, the protective layer 1050 can include a photo-patternable spin-on glass material such as the material sold under the trademark TOK-OLiM-iF™ by Tokyo Ohka Kogyo Co., Ltd. of Nakahara-ku, Kawasaki-shi, Kanagawa Prefecture, Japan. In some implementations, the protective layer 1050 can include AZLExp™j sold by AZ Electronic Materials (Japan) Co. LTD., of 3330 Chihama Kakegawa-city, Shiznoka Japan. The planarization layer fills the light turning features 1030 and provides a substantially planar top surface.

[0081] In some implementations, the protective layer 1050 is a thick coating of SiO₂. In various implementations, the protective layer 1050 can be about 1000 Å to about 3 μm thick. The SiO₂ can be formed using a plasma CVD process. In another implementation, the SiO₂ can be formed using a sputtering process. The protective layer 1050 fills in the light turning features 1030, and may include one or more surface protrusions 1052. The surface protrusions 1052 can be caused by, for example, protrusions in the topology of the underlying substrate 1010 which is propagated through to the top of the protective layer 1050.

[0082] Referring now to Figure 10C, in some implementations (for example, where the protective layer 1050 does not form a planar surface as deposited), the protective layer 1050 can be planarized. For example, the protective layer 1050 may be planarized in implementations where the protective layer 1050 includes a material causing the surface protrusions 1052 after formation. In an implementation, the planarization can be accomplished using a chemical mechanical polishing (CMP) process. In some implementations, between about 1.5 μm and about 3.0 μm of the protective layer 1050 deposited is removed during subsequent planarization. In some implementations, the protective layer can be planarized to have a substantially planar surface having a mean absolute deviation (MAD) of less than about 15 Å or less than about 7 Å. In

implementations, where the protective layer 1050 includes a material that forms a substantially planar surface as-deposited, the planarization process can be omitted.

[0083] In some implementations, the protective layer 1050 includes a material with a refractive index substantially matched to the substrate 1010 and/or the turning film 1020. For example, the indices of refraction of the protective layer 1050 and the turning film 1020 may be within about 0.03, or about 0.02 of one another. In some implementations, the substrate 1010 and the light turning film 1020 may form a light guide 1070. Further, the protective layer 1050 may form some part of the light guide 1070 and may support TIR at an upper surface of the protective layer 1050. In some other implementations, the protective layer 1050 can include a material having a refractive index lower than the light turning film 1020 and sufficient to support TIR at the interface between the protective layer 1050 and the light turning film 1020. For example, the refractive index of the protective layer 1050 can be less than the refractive index of the light turning film 1020 by more than about 0.05, about 0.08, or about 0.1. Thus, the protective layer 1050 can function as a cladding layer. Additionally or alternatively, in some implementations, the protective layer 1050 can be a passivation layer formed of a material sufficient to protect one or more underlying layers from oxidation.

[0084] Referring now to Figure 10D, an array 1060 of display elements is formed on the second side 1014 of the substrate 1010. In some implementations, the array 1060 can be formed on the second side 1014 of the substrate 1010 by flipping the substrate 1010. In some implementations, the array 1060 can include a plurality of IMODs (such as the IMODs 12 shown in Figure 1). The array 1060 can be formed using the same or substantially similar processing equipment, or tool set, used for forming the light turning features 1030 described above with respect to Figures 10A-C. In some implementations, the array 1060 can be formed using the process described above with respect to Figures 6-8, with the substrate 1010 taking the place of the substrate 20 in those figures. In some other implementations, a cladding layer (for example, a layer of SiO₂) may be formed on the second side 1014 and then the display elements of the array 1060 are fabricated directly on, or contacting, the cladding layer.

[0085] Referring still to Figure 10D, together, the substrate 1010 and the light turning film 1020 can form a light guide 1070. In various implementations, the substrate 1010

and the light turning film 1020 can be formed of the same material or different materials with substantially similar refractive indices, thereby allowing light to propagate back and forth between the layers and laterally across the light guide 1070. In some implementations, the refractive indices of the light turning film 1020 and the substrate 1010 are within about 0.05, about 0.03, or about 0.02 of each other.

[0086] Referring now to Figures 11A-B, in some other implementations, a plurality of protective layers may be provided. Figures 11A-B show examples of cross-sectional schematic illustrations of various stages in a method of making an integrated light and display element array, according to some other implementations. In some implementations, the protective layer 1050 is a first protective layer over which one or more additional protective layers may be deposited. In some implementations, the protective layer 1050 can include a first protective material that forms a planar surface, as it is deposited. For example, the first protective layer may be formed of a spin-on-glass (SOG) or a high-temperature, low-refractive index polymer coating. The first protective layer can be covered with a second protective layer, which can be harder and/or more resistant to chemical interaction or mechanical abrasion than the first protective layer. The illustrated method can provide a protective layer without a planarizing process, such as CMP. In some other implementations, CMP may be employed.

[0087] Referring to Figure 11A, the substrate 1010, the light turning film 1020, one or more light turning features 1030, the coating layer 1040, the first protective layer 1050, and a second protective layer 1155 are provided. The substrate 1010 has first and second sides 1012 and 1014, and the light turning film 1020 is provided on the first side 1012. The first protective layer 1050 is formed over the light turning film 1020 and the coating layer 1040 on the first side 1012 of the substrate. As discussed above with respect to Figures 10A-10D, the first protective layer 1050 can be formed using, for example, a material that forms a substantially planar surface as-deposited, or a material that can be made to have a substantially planar surface by subsequent processing after deposition. For example, the first protective layer 1050 can be formed by spin coating a planarization polymer or spin-on glass material, including a patternable spin-on glass material. In an implementation, the first protective layer 1050 fills the light turning features 1030 and provides a substantially planar top surface.

[0088] Referring still to Figure 11A, the second protective layer 1155 is formed over the first protective layer 1050. In some implementations, the second protective layer 1155 can include a material that is stronger, harder, more scratch-resistant, and/or has higher resistance to chemicals to which it will be exposed than the first protective layer 1050, and may provide additional protection to the first protective layer 1050 and other underlying layers 1020 and 1040 during subsequent back-side processing. In some implementations, the first protective layer 1050 may not be strong enough to withstand processing of the second side 1014 of the substrate 1010. Other potential uses of the second protective layer 1155 include reducing or preventing moisture absorption and outgassing during processing of the second side 1014 of the substrate 1010. In various implementations, the second protective layer 1155 can be between about 0.1 μm and about 3 μm thick.

[0089] In some implementations, the second protective layer 1155 can include one of SiON, SiO₂, silicon nitride (SiN_x), or combinations thereof. The second protective layer 1155 can be formed using a plasma CVD process. In another implementation, the second protective layer 1155 can be formed using a sputtering process. The second protective layer 1155 may not include the surface protrusions 1052 described above with respect to Figure 10B, due to the substantially planar surface of the first protective layer 1050.

[0090] Referring now to Figure 11B, the array 1060 is formed on the second side 1014 of the substrate 1010. The array 1060 may be formed as described herein, for example, with respect to Figure 10D.

[0091] Figure 12A shows a cross-sectional schematic illustration of some implementations of the light guide 1070 of Figures 10A – 11B. In the illustrated implementation, the coating layer 1040 can be formed of three constituent layers 1242, 1244, and 1246, which may form a “black mask,” as described below. In certain implementations, the coating layer 1040 of the turning features 1030 (Figure 9) may be configured as an interferometric stack having: a reflective layer 1242 that re-directs or reflects light propagating within the light guide 100, an optically transmissive spacer layer 1244, and a partially reflective layer 1246 overlying the spacer layer 1244. The

spacer layer 1244 is disposed between the reflective layer 1242 and the partially reflective layer 1246 and defines an optical resonant cavity by its thickness.

[0092] The interferometric stack can be configured to give the coatings 1040 a dark appearance, as seen by the viewer 170 (Figure 9), and may therefore be referred to as a “black mask,” in some implementations. For example, light can be reflected off of each of the reflective layer 1242 and partially reflective layer 1246, with the thickness of the spacer 1244 selected such that the reflected light interferes destructively so that the coatings 1040 appear black or dark as seen from above by the viewer 170.

[0093] The reflective layer 1242 may, for example, include a metal layer, for example, aluminum (Al), nickel (Ni), silver (Ag), molybdenum (Mo), gold (Au), and chromium (Cr). The reflective layer 1242 can be between about 100 Å and about 700 Å thick. In one implementation, the reflective layer 1242 is about 300 Å thick. The spacer layer 1244 can include various optically transmissive materials, for example, air, silicon oxy-nitride (SiO_xN), silicon dioxide (SiO₂), aluminum oxide (Al₂O₃), titanium dioxide (TiO₂), magnesium fluoride (MgF₂), chromium (III) oxide (Cr₃O₂), silicon nitride (Si₃N₄), transparent conductive oxides (TCOs), indium tin oxide (ITO), and zinc oxide (ZnO). In some implementations, the spacer layer 1244 is between about 500 Å and about 1500 Å thick. In one implementation, the spacer layer 1244 is about 800 Å thick. The partially reflective layer 1246 can include various materials, for example, molybdenum (Mo), titanium (Ti), tungsten (W), chromium (Cr), etc., as well as alloys, for example, MoCr. The partially reflective 1246 can be between about 20 and about 300 Å thick in some implementations. In one implementation, the partially reflective layer 1246 is about 80 Å thick. In some implementations, the reflective layer 1242, the spacer layer 1244, and the partially reflective layer 1246 can include an Al film, a SiO₂ film, and a MoCr film, respectively.

[0094] Figure 12B shows a cross-sectional schematic illustration of another implementation of the light guide 1070 of Figures 10A – 11B. In some implementations, the coating layer 1040 can include an opening 1280. Because the sides 1290 of the light turning feature 1030 are principally used to redirect light to the array 1060 of display elements (Figure 9), in some implementations, the coating layer 1040 may be provided with an opening 1280 through which light can travel. The opening 1280 can facilitate the

propagation of ambient light to the array 1060 of display elements and/or the propagation of reflected light to the viewer 170. The opening 1280 may be formed by providing a patterned mask over the coating layer 1040, and etching the coating layer 1040 to define the opening 1280.

[0095] Figure 12C shows a cross-sectional schematic illustration of yet another implementation of the light guide of Figures 10A – 11B. In some implementations, the light turning feature 1030 may not include the coating layer 1040 (Figure 12A). Rather, the light turning feature 1030 redirects light by total internal reflection off of its surfaces. In such implementations, a relatively low refractive index material, such as the material of a cladding layer (such as, for example, SiO₂), can fill the indentation forming the light turning feature 1030, thereby facilitating total internal reflection at the surfaces of the light turning feature 1030.

[0096] Figure 13 shows an example of a flow diagram illustrating a manufacturing process 1300 for an integrated light and display element array. Various stages of the manufacturing process 1300 are illustrated and described above with respect to Figures 10A – 11B. In some implementations, the manufacturing process 1300 can be implemented to manufacture, for example, the integrated light and display element array of the general type illustrated in Figure 9. Although the blocks of the process 1300 are described herein with respect to Figures 9 and 10A-D, a person having ordinary skill in the art will appreciate that the process 1300 can be applied to other structures. For example, the process 1300 can also be applied to the structure of Figures 11A-B. Moreover, the blocks of the process 1300 can be performed in any order, blocks can be omitted or modified, and/or additional blocks added within the scope of this disclosure.

[0097] The manufacturing process 1300 begins at block 1310 with the provision of the substrate 1010 (Figure 10). The substrate 1010 has a first side and a second side opposite the first. The process 1300 continues at block 1320 with the processing of the first side using a first processing technology. In some implementations, a plurality of light turning features 1030 is formed in the substrate 1010. The protective layer 1050 is formed over the substrate 1010 and the light turning features 1030. The light guide 1070 can include the protective layer 1050, the light turning features 1030, and the substrate 1010. As discussed above, light turning features 1030 can be formed in the light turning

film 1020 or directly in the substrate 1010. In some implementations, the light guide 1070 can be the light guide 1070 (Figure 9). The light guide 1070 can be configured to propagate light along the length of the light guide 1070 by total internal reflection.

[0098] In some implementations, a coating layer 1040 can be formed in the light turning features 1030. In some implementations, the coating layer 1040 can be configured to increase reflectivity of the ultimately-formed turning feature and/or function as a black mask from the viewer side to improve contrast of the array 1060 of display elements as observed by the viewer 170 (Figure 9). In some implementations, a planarization layer 1035 is further deposited over the coating layer 1040. Then the process 1300 transitions to block 1330.

[0099] At block 1330, the second side of the substrate 1010 can be processed using a second processing technology. In some implementations, the second processing technology can be the same as, or substantially similar to, the first processing technology. In some implementations, processing of the second side of the substrate 1010 can include forming the array 1060 on the second side of the substrate 1010. In some implementations, the array 1060 can be formed on the second side of the substrate 1010 by flipping the substrate 1010. In some implementations, the array 1060 can be formed using the process described above with respect to Figures 6-8. In some implementations, the first protective layer 1050 can be cured and further baked before each processing operation for the second side of the substrate 1010. In some implementations, the block 1320 can be performed before the block 1330. In some other implementations, blocks 1320 and 1330 can overlap in time.

[0100] Figures 14A and 14B show examples of system block diagrams illustrating a display device 40 that includes a plurality of interferometric modulators. The display device 40 can be, for example, a cellular or mobile telephone. However, the same components of the display device 40 or slight variations thereof are also illustrative of various types of display devices such as televisions, e-readers and portable media players.

[0101] The display device 40 includes a housing 41, a display 30, an antenna 43, a speaker 45, an input device 48, and a microphone 46. The housing 41 can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing 41 may be made from any of a variety of

materials, including, but not limited to: plastic, metal, glass, rubber, and ceramic, or a combination thereof. The housing 41 can include removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0102] The display 30 may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display 30 also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display 30 can include an interferometric modulator display, as described herein.

[0103] The components of the display device 40 are schematically illustrated in Figure 14B. The display device 40 includes a housing 41 and can include additional components at least partially enclosed therein. For example, the display device 40 includes a network interface 27 that includes an antenna 43 which is coupled to a transceiver 47. The transceiver 47 is connected to a processor 21, which is connected to conditioning hardware 52. The conditioning hardware 52 may be configured to condition a signal (e.g., filter a signal). The conditioning hardware 52 is connected to a speaker 45 and a microphone 46. The processor 21 is also connected to an input device 48 and a driver controller 29. The driver controller 29 is coupled to a frame buffer 28, and to an array driver 22, which in turn is coupled to a display array 30. A power supply 50 can provide power to all components as required by the particular display device 40 design.

[0104] The network interface 27 includes the antenna 43 and the transceiver 47 so that the display device 40 can communicate with one or more devices over a network. The network interface 27 also may have some processing capabilities to relieve, e.g., data processing requirements of the processor 21. The antenna 43 can transmit and receive signals. In some implementations, the antenna 43 transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g or n. In some other implementations, the antenna 43 transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna 43 is designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM),

GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G or 4G technology. The transceiver 47 can pre-process the signals received from the antenna 43 so that they may be received by and further manipulated by the processor 21. The transceiver 47 also can process signals received from the processor 21 so that they may be transmitted from the display device 40 via the antenna 43.

[0105] In some implementations, the transceiver 47 can be replaced by a receiver. In addition, the network interface 27 can be replaced by an image source, which can store or generate image data to be sent to the processor 21. The processor 21 can control the overall operation of the display device 40. The processor 21 receives data, such as compressed image data from the network interface 27 or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor 21 can send the processed data to the driver controller 29 or to the frame buffer 28 for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation, and gray-scale level.

[0106] The processor 21 can include a microcontroller, CPU, or logic unit to control operation of the display device 40. The conditioning hardware 52 may include amplifiers and filters for transmitting signals to the speaker 45, and for receiving signals from the microphone 46. The conditioning hardware 52 may be discrete components within the display device 40, or may be incorporated within the processor 21 or other components.

[0107] The driver controller 29 can take the raw image data generated by the processor 21 either directly from the processor 21 or from the frame buffer 28 and can re-format the raw image data appropriately for high speed transmission to the array driver 22. In some implementations, the driver controller 29 can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for

scanning across the display array 30. Then the driver controller 29 sends the formatted information to the array driver 22. Although a driver controller 29, such as an LCD controller, is often associated with the system processor 21 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor 21 as hardware, embedded in the processor 21 as software, or fully integrated in hardware with the array driver 22.

[0108] The array driver 22 can receive the formatted information from the driver controller 29 and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

[0109] In some implementations, the driver controller 29, the array driver 22, and the display array 30 are appropriate for any of the types of displays described herein. For example, the driver controller 29 can be a conventional display controller or a bi-stable display controller (e.g., an IMOD controller). Additionally, the array driver 22 can be a conventional driver or a bi-stable display driver (e.g., an IMOD display driver). Moreover, the display array 30 can be a conventional display array or a bi-stable display array (e.g., a display including an array of IMODs). In some implementations, the driver controller 29 can be integrated with the array driver 22. Such an implementation is common in highly integrated systems such as cellular phones, watches and other small-area displays.

[0110] In some implementations, the input device 48 can be configured to allow, e.g., a user to control the operation of the display device 40. The input device 48 can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, or a pressure- or heat-sensitive membrane. The microphone 46 can be configured as an input device for the display device 40. In some implementations, voice commands through the microphone 46 can be used for controlling operations of the display device 40.

[0111] The power supply 50 can include a variety of energy storage devices as are well known in the art. For example, the power supply 50 can be a rechargeable battery, such as a nickel-cadmium battery or a lithium-ion battery. The power supply 50 also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or

solar-cell paint. The power supply 50 also can be configured to receive power from a wall outlet.

[0112] In some implementations, control programmability resides in the driver controller 29 which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver 22. The above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0113] The various illustrative logics, logical blocks, modules, circuits and algorithm steps described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0114] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function.

[0115] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the

structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[0116] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein. The word “exemplary” is used exclusively herein to mean “serving as an example, instance, or illustration.” Any implementation described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other implementations. Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the IMOD as implemented.

[0117] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0118] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict

one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

CLAIMS

What is claimed is:

1. A method of manufacturing a display device, the method comprising:
providing a substrate having a first side and a second side opposite the first side;
processing the first side using a first processing technology, wherein processing the first side includes:
forming a plurality of light turning features on the first side of the substrate, and
forming a first protective layer over the light turning features; and
subsequently processing the second side using a second processing technology, wherein processing the second side includes:
forming an array of display elements on the second side of the substrate.
2. The method of claim 1, wherein the first processing technology uses substantially the same tool set as the second processing technology.
3. The method of claim 1, wherein the first protective layer is a scratch resistant layer.
4. The method of claim 1, wherein the first protective layer is resistant to etch chemistries for forming the array of display elements.
5. The method of claim 1, further comprising:
planarizing the first protective layer by chemical mechanical polishing the first protective layer.
6. The method of claim 1, wherein the first protective layer includes silicon dioxide (SiO₂).

7. The method of claim 1, wherein the first protective layer is formed of a self-planarizing material.

8. The method of claim 7, wherein the self-planarizing material is a spin-on-glass (SOG) material.

9. The method of claim 1, further comprising forming a second protective layer over the first protective layer.

10. The method of claim 9, wherein the second protective layer is harder than the first protective layer.

11. The method of claim 1, wherein forming the array of display elements includes forming a plurality of interferometric modulators by performing deposition and patterning.

12. A display device comprising:
a substrate having a first side and a second side opposite the first side;
a plurality of light turning features defined by indentations on the first side;
a substantially planar first protective layer over the light turning features and substantially extending into the indentations; and
an array of display elements formed on the second side.

13. The device of claim 12, wherein the array of display elements are formed directly in contact with the substrate.

14. The device of claim 12, wherein the substrate constitutes a light guide.

15. The device of claim 14, wherein the light guide includes a light turning film on the first side of the substrate, wherein the indentations are formed in the light turning film.

16. The device of claim 12, wherein the first protective layer includes an optical cladding layer.

17. The device of claim 12, wherein the first protective layer includes a passivation layer.

18. The device of claim 17, wherein the light turning features include a reflective layer in each of the indentations and underlying the first protective layer, wherein the passivation layer prevents corrosion of the reflective layer.

19. The device of claim 18, wherein the reflective layer is part of a black mask, the black mask including:

- the reflective layer;
- a partially reflective layer; and
- a spacer layer separating the reflective layer from the partially reflective layer.

20. The device of claim 12, wherein the first protective layer includes silicon dioxide (SiO_2).

21. The display device of claim 12, wherein the first protective layer is formed of a self-planarizing material.

22. The device of claim 21, wherein the self-planarizing material is a spin-on-glass (SOG).

23. The display device of claim 21, further comprising a second protective layer over the first protective layer, wherein the second protective layer is harder than the first protective layer.

24. The device of claim 23, wherein the second protective layer includes at least one of silicon dioxide (SiO_2), silicon oxynitride (SiON), and silicon nitride (SiN_x).

25. The device of claim 12, wherein the array of display elements include reflective display elements.

26. The device of claim 25, wherein the reflective display elements are interferometric modulators (IMODs).

27. The device of claim 12, wherein the display elements form a display, the device further comprising:

a processor that is configured to communicate with the display, the processor being configured to process image data; and
a memory device that is configured to communicate with the processor.

28. The device of claim 27, further comprising:
a driver circuit configured to send at least one signal to the display; and
a controller configured to send at least a portion of the image data to the driver circuit.

29. The device of claim 27, further comprising:
an image source module configured to send the image data to the processor.

30. The device of claim 29, wherein the image source module includes at least one of a receiver, transceiver, and transmitter.

31. The device of claim 27, further comprising:
an input device configured to receive input data and to communicate the input data to the processor.

32. A display device comprising:
a substrate having a first side and a second side opposite the first side;
a plurality of light turning features on the first side;
means for protecting the light turning features; and
an array of display elements formed on the second side.

33. The device of claim 32, wherein the means for protecting includes an optical cladding layer.

34. The device of claim 32, wherein the means for protecting includes a passivating layer.

35. The device of claim 32, wherein the plurality of light turning features are formed in indentations on the first side of the substrate, wherein the means for protecting includes a scratch-resistant layer extending into the indentations.

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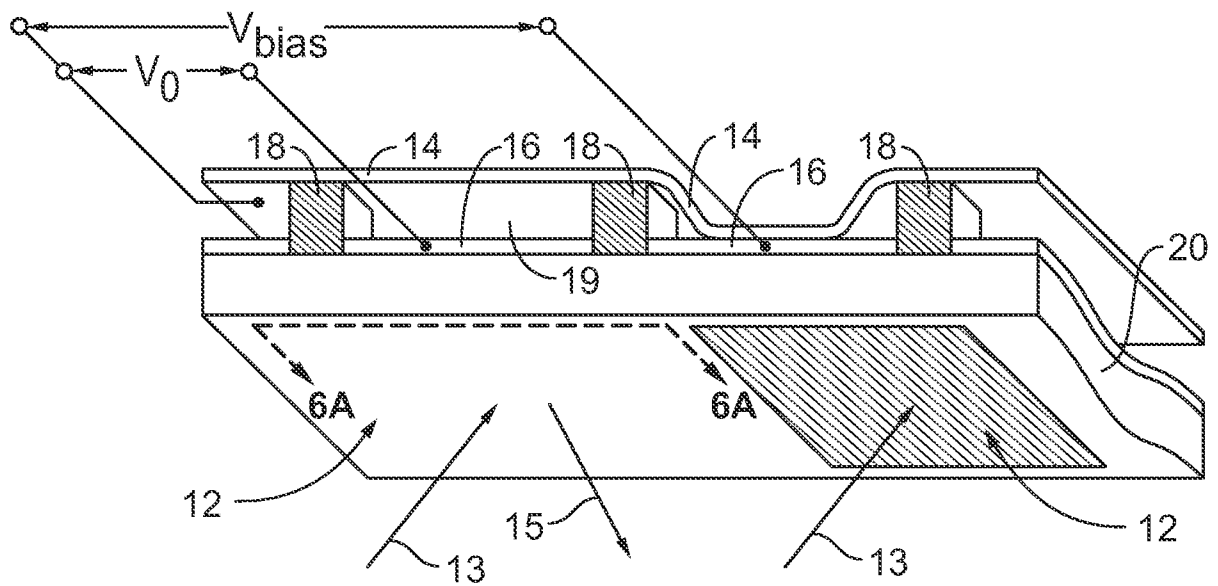


Figure 1

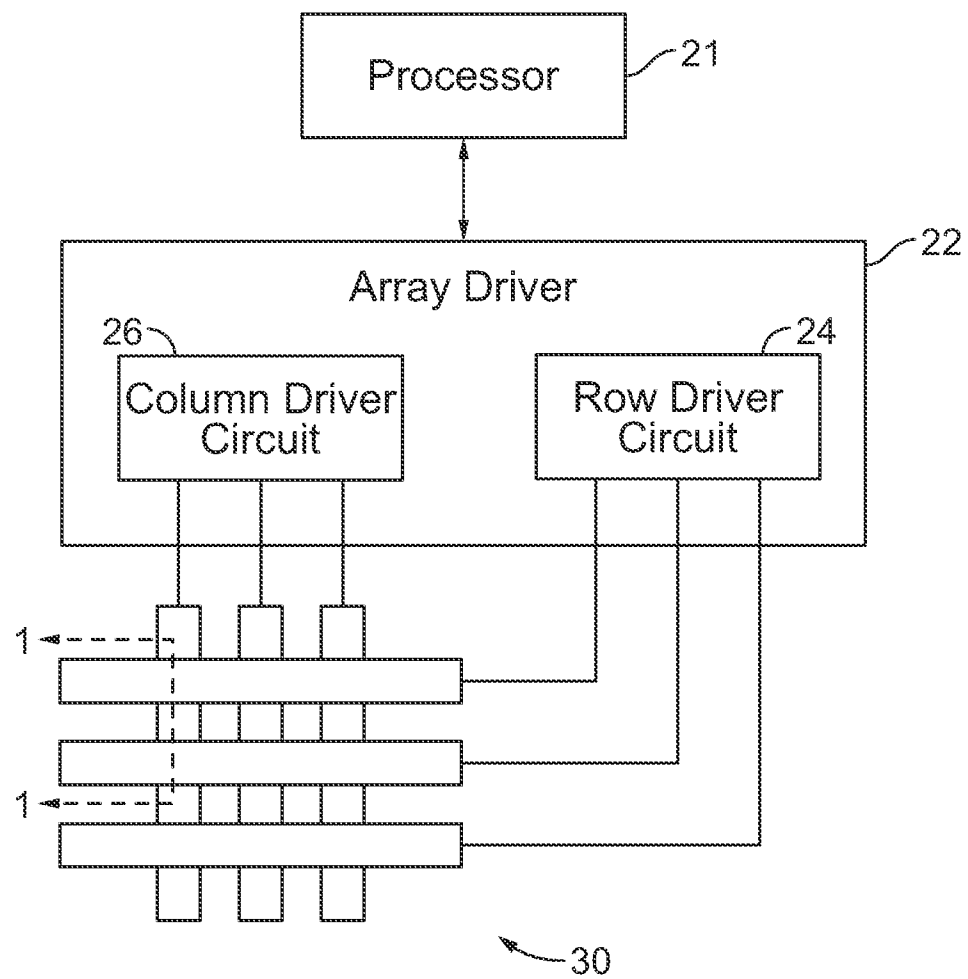


Figure 2

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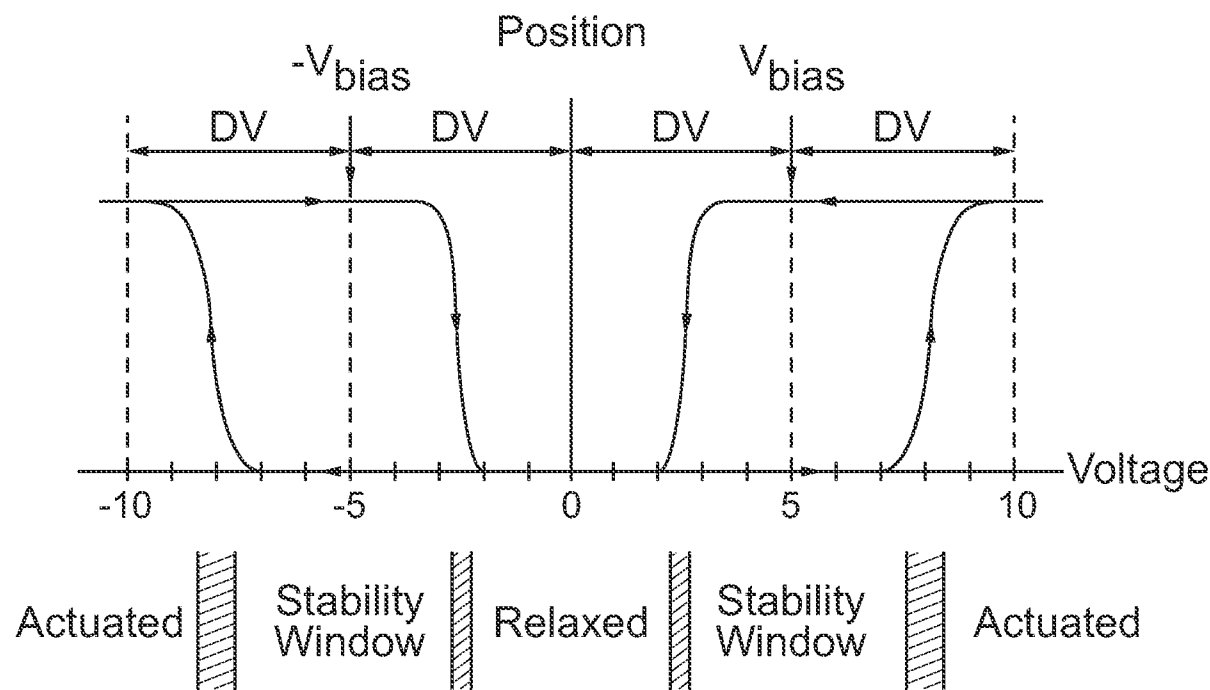
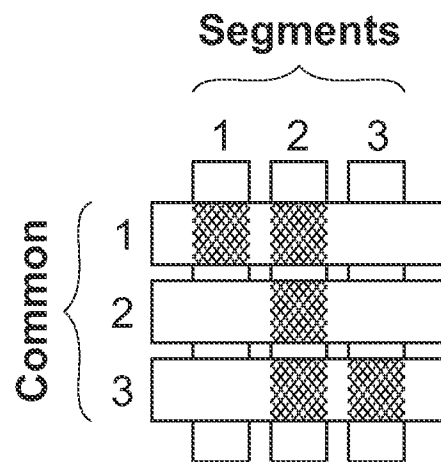
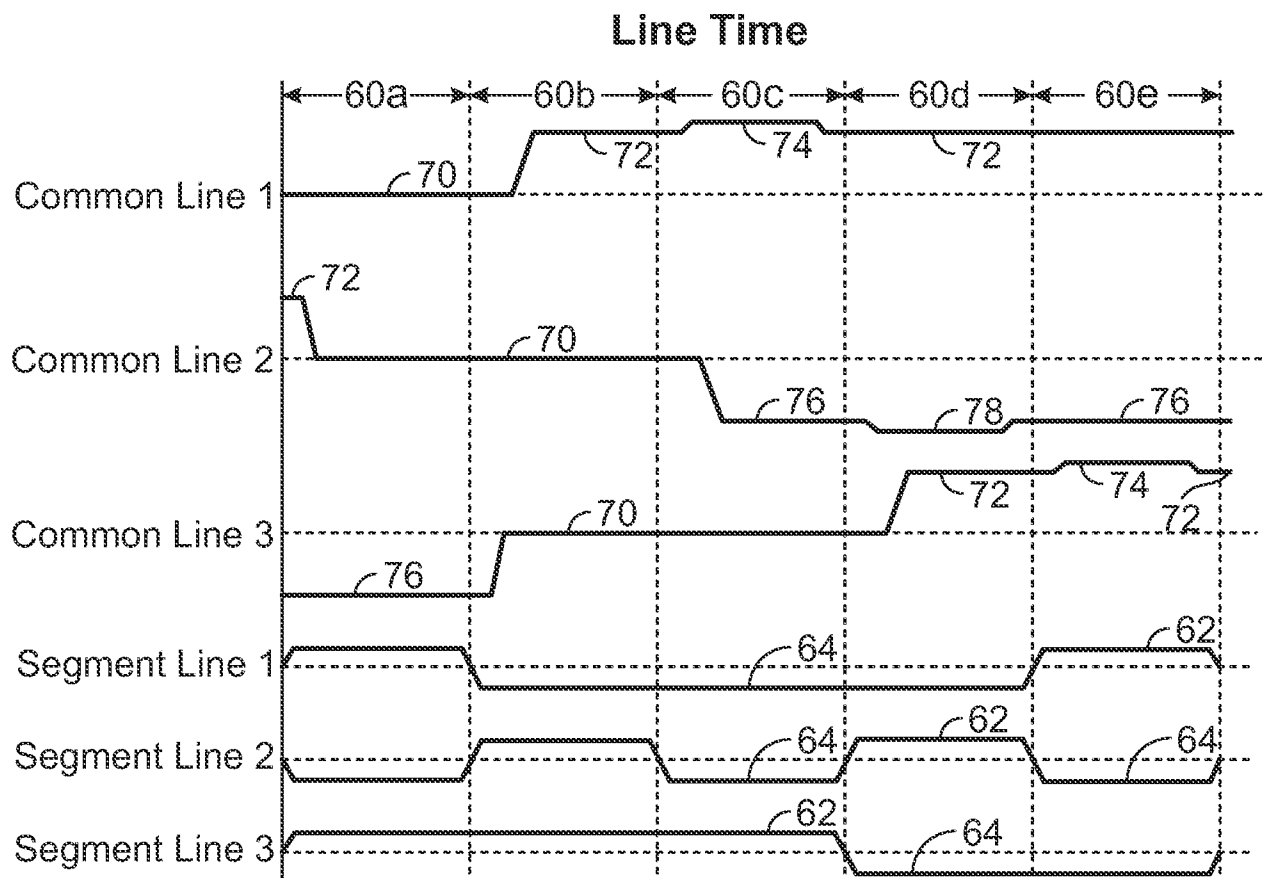


Figure 3

Common Voltages						
Segment Voltages		V_{CADD_H}	V_{CHOLD_H}	V_{CREL}	V_{CHOLD_L}	V_{CADD_L}
	V_{S_H}	Stable	Stable	Relax	Stable	Actuate
	V_{S_L}	Actuate	Stable	Relax	Stable	Stable

Figure 4

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**Figure 5A****Figure 5B**

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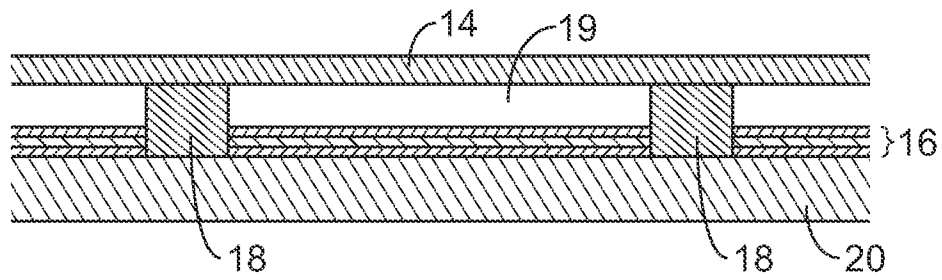


Figure 6A

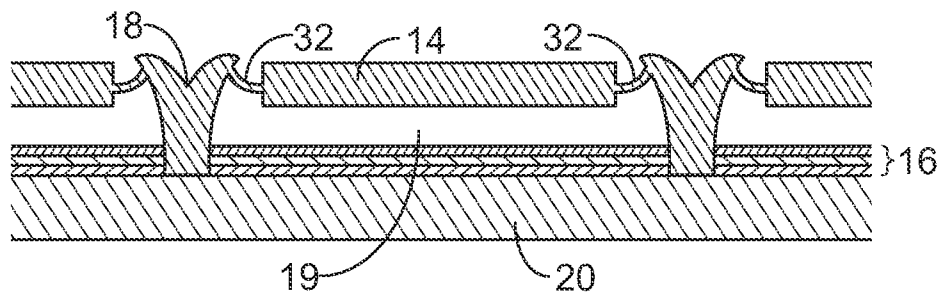


Figure 6B

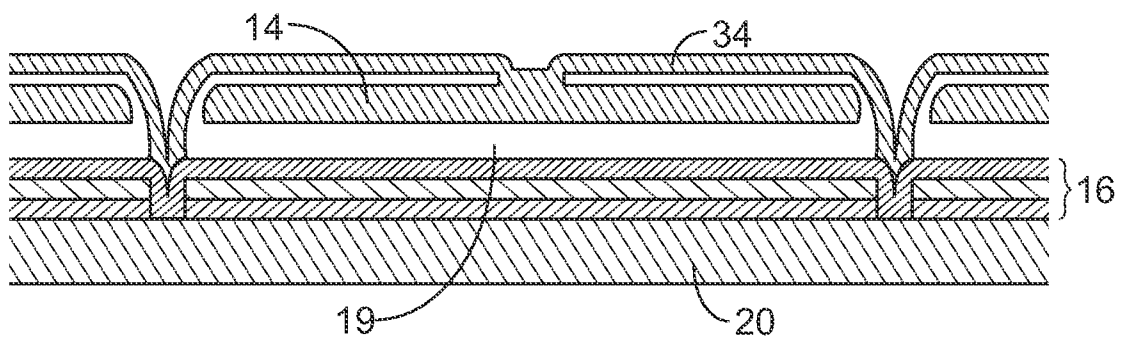


Figure 6C

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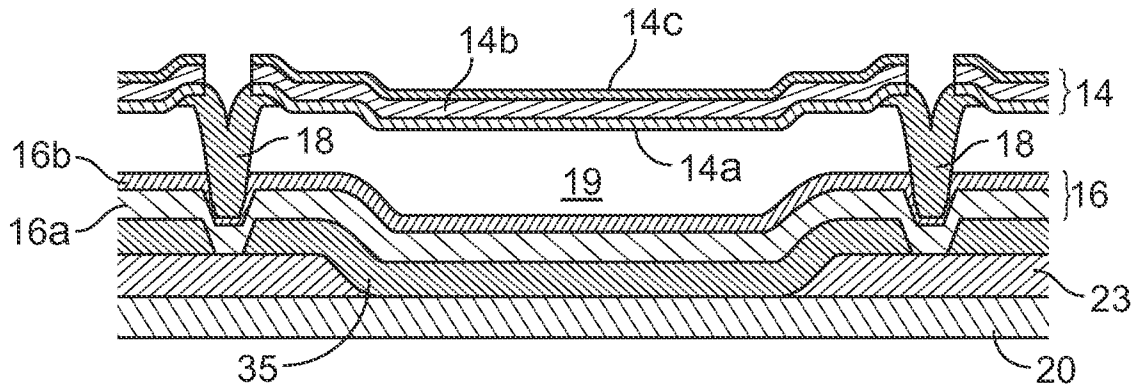


Figure 6D

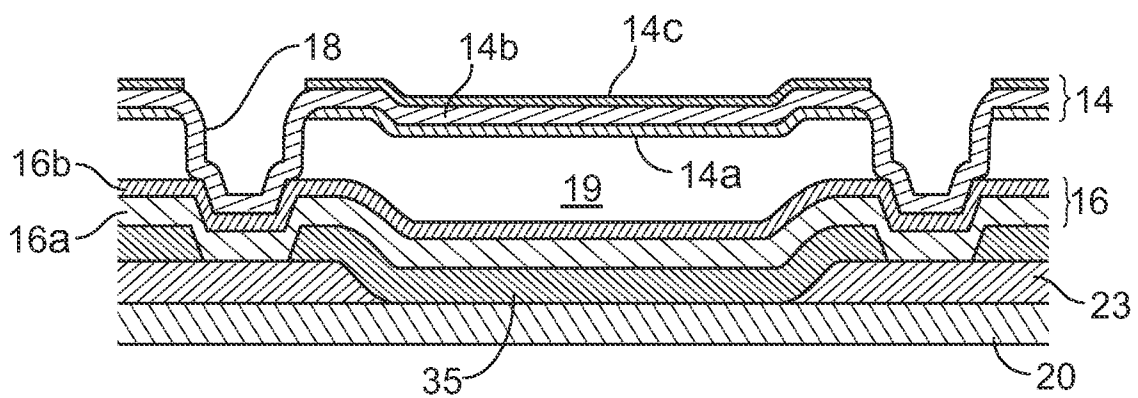


Figure 6E

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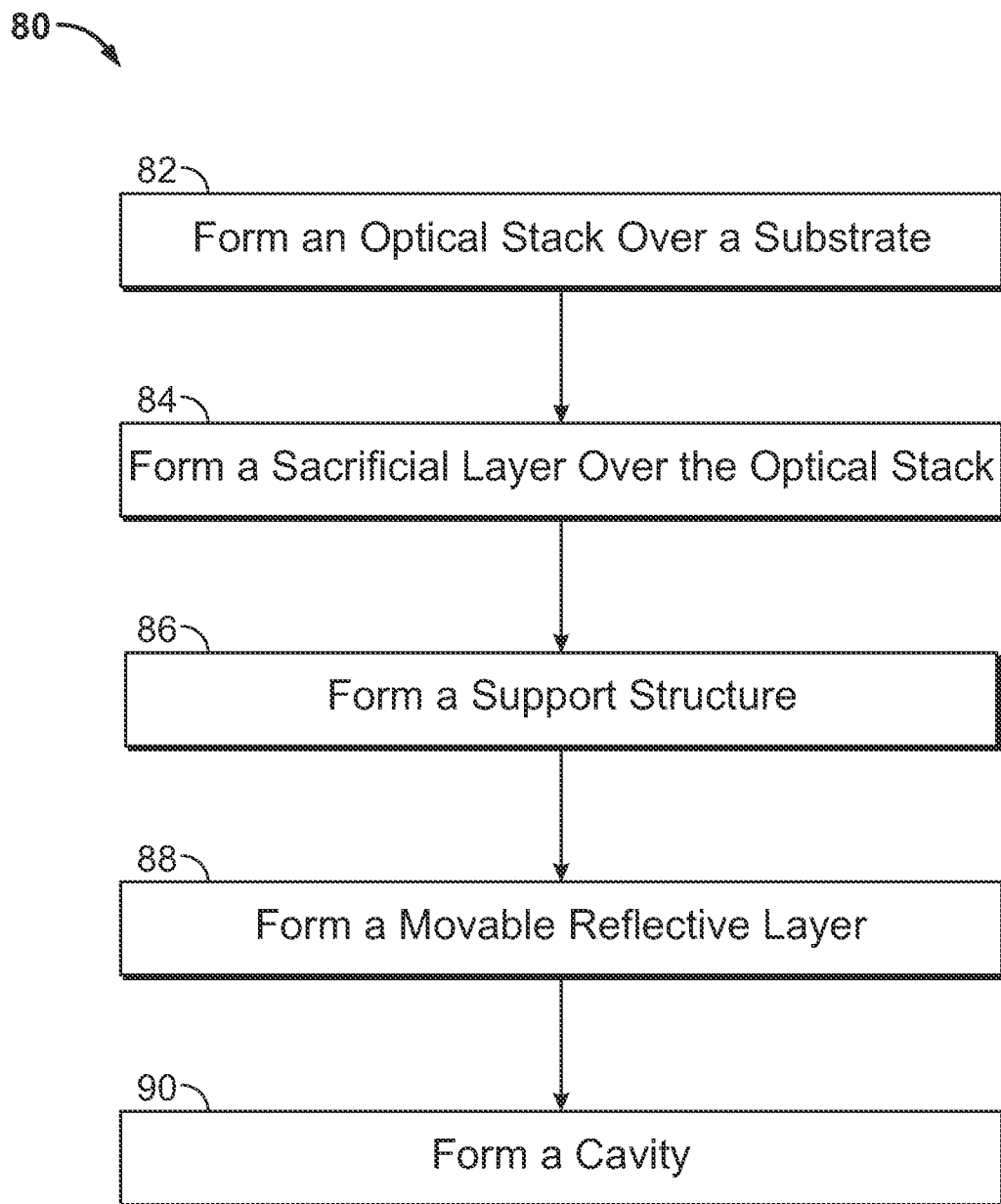


Figure 7

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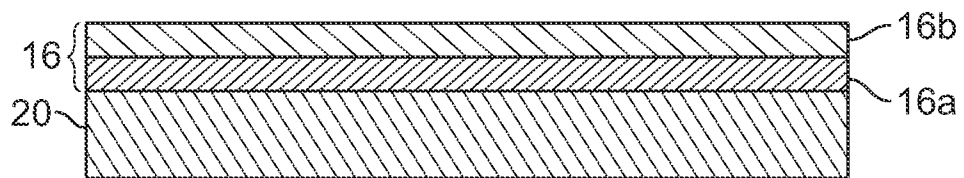


Figure 8A

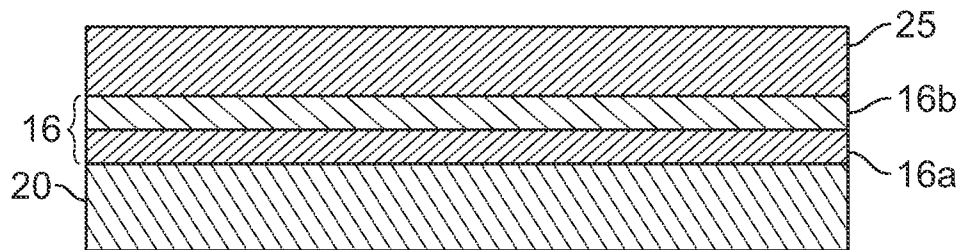


Figure 8B

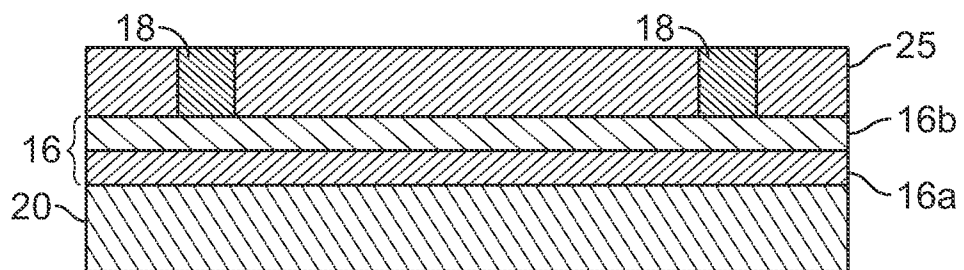


Figure 8C

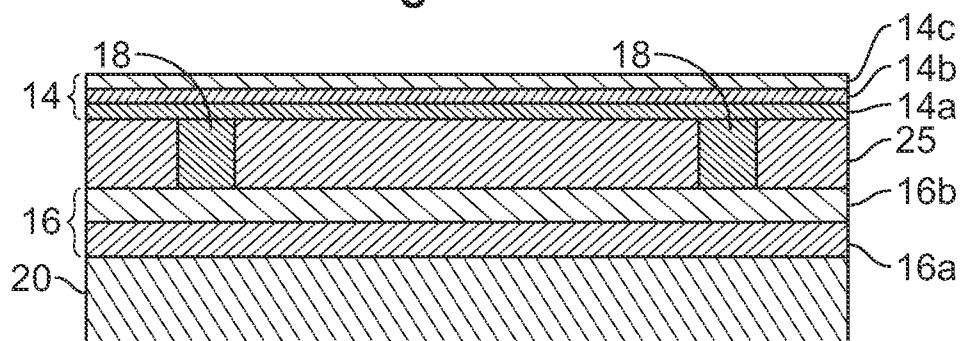


Figure 8D

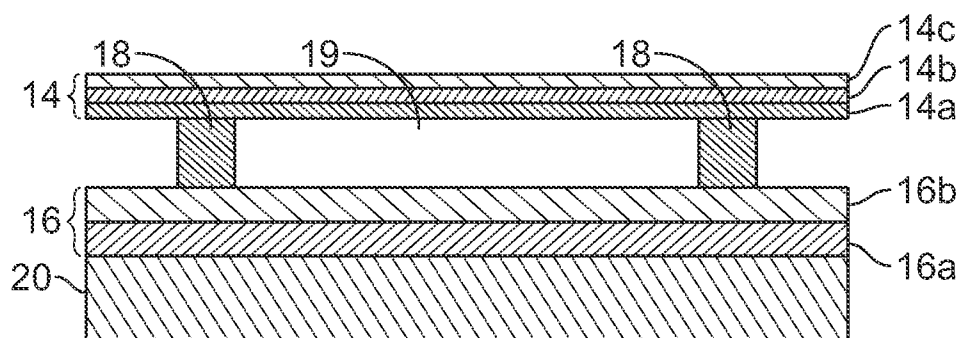


Figure 8E

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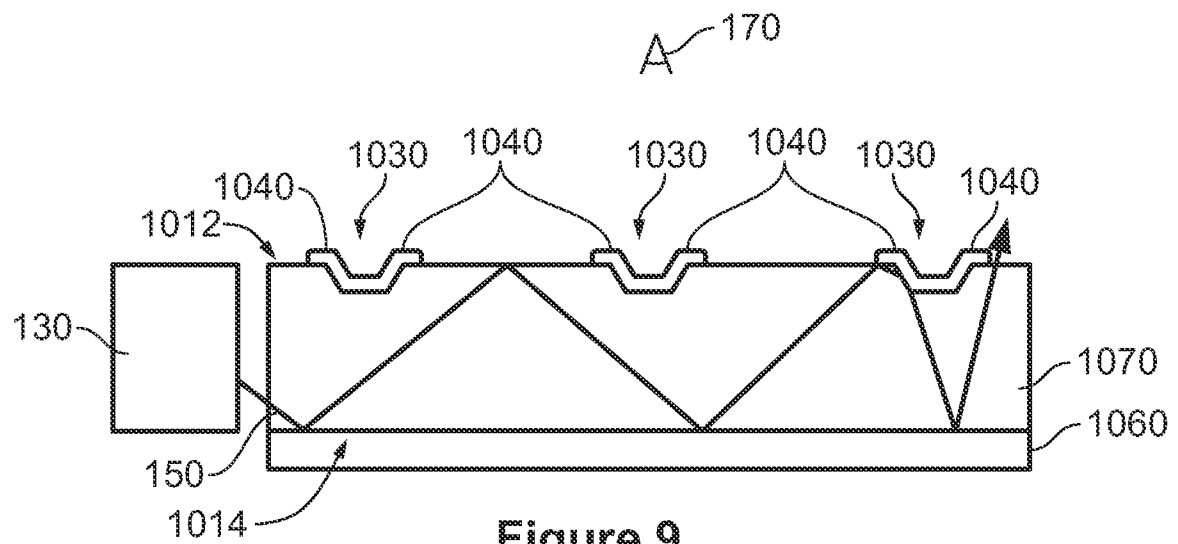


Figure 9

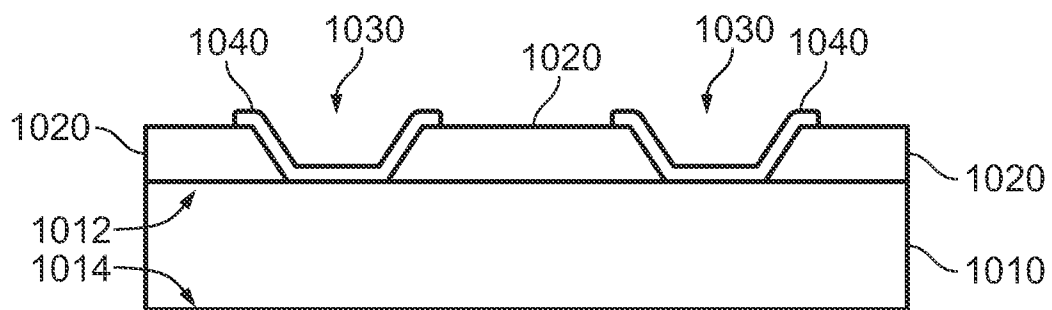


Figure 10A

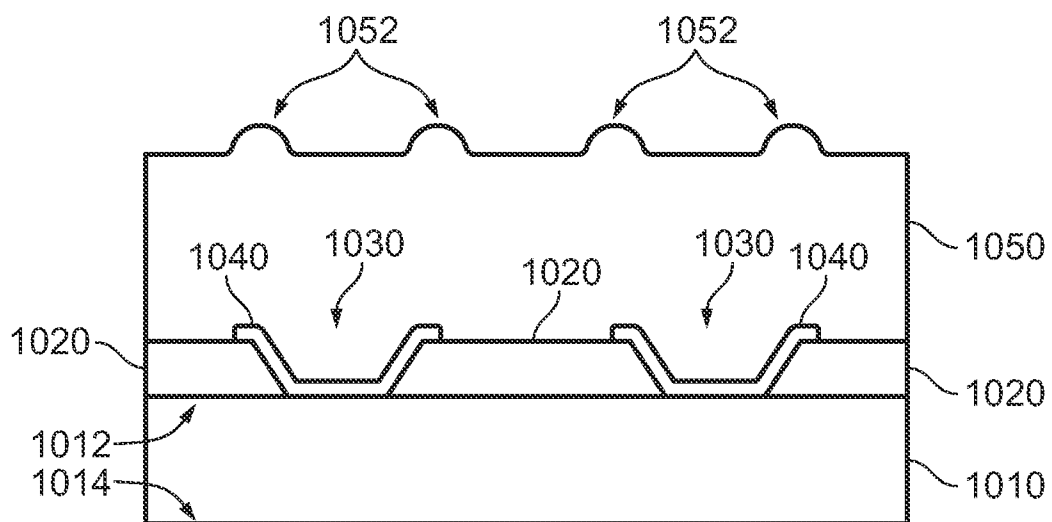


Figure 10B

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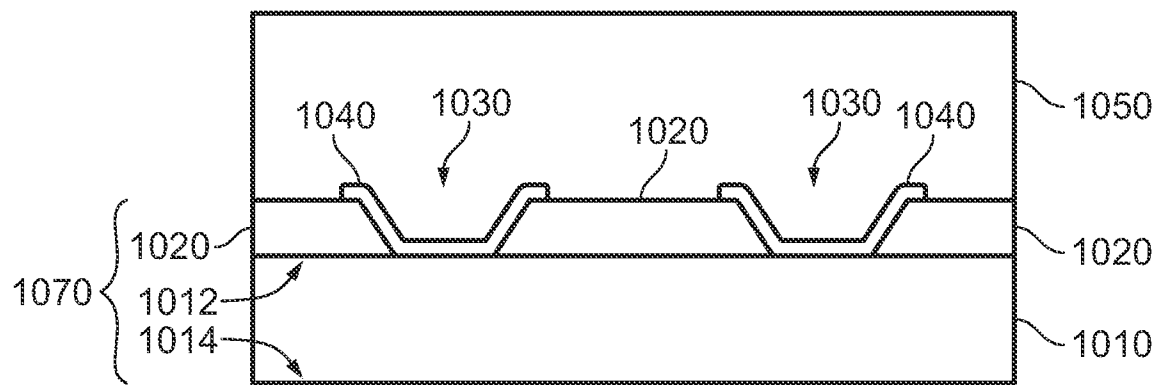


Figure 10C

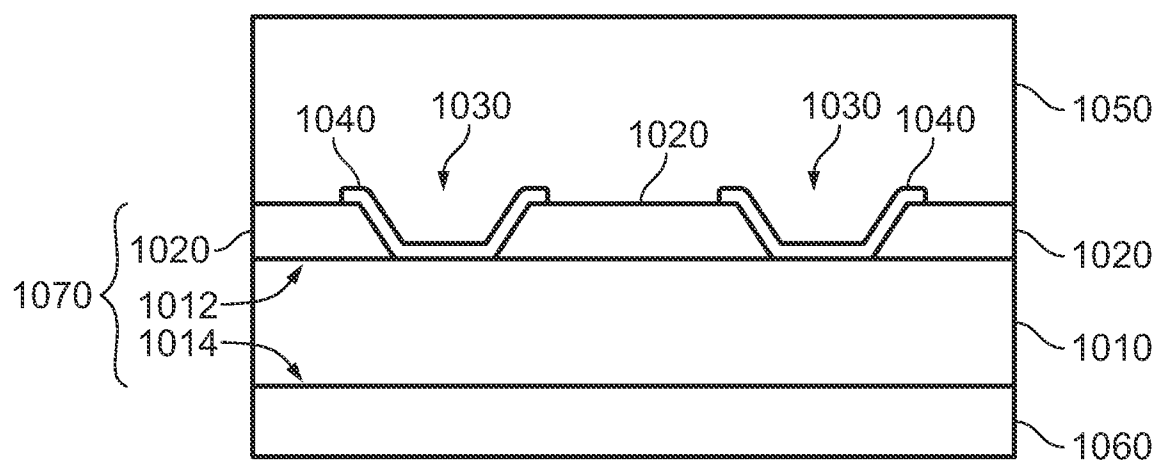


Figure 10D

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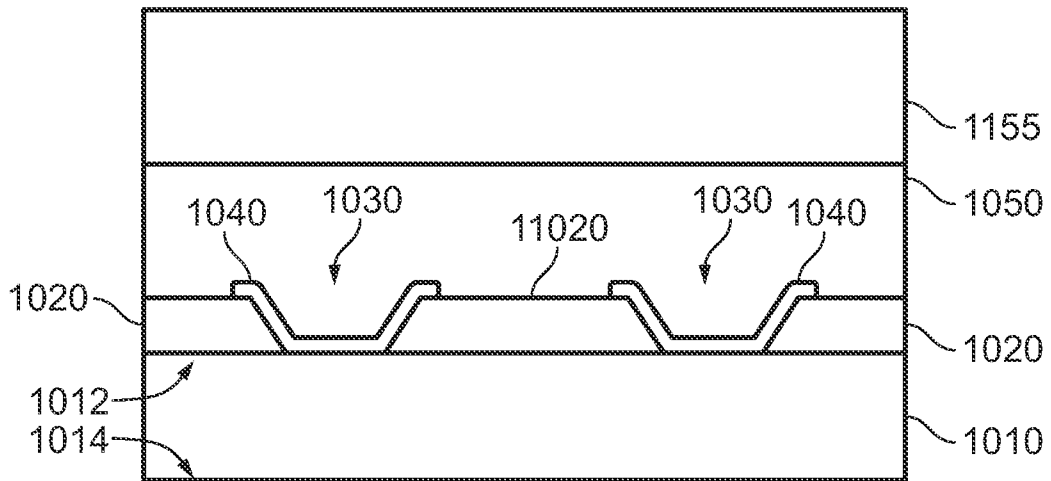


Figure 11A

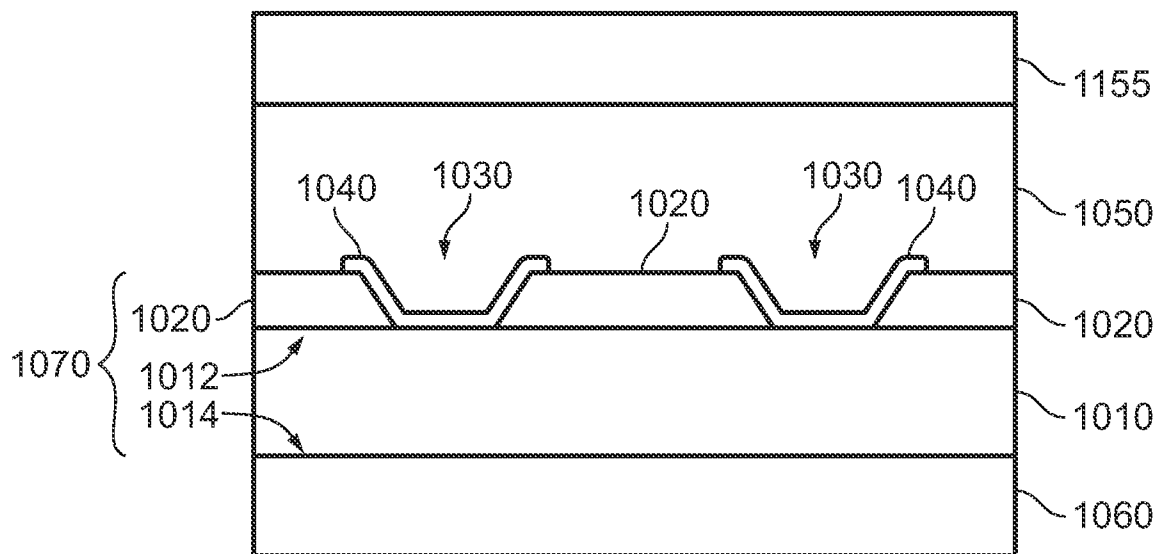


Figure 11B

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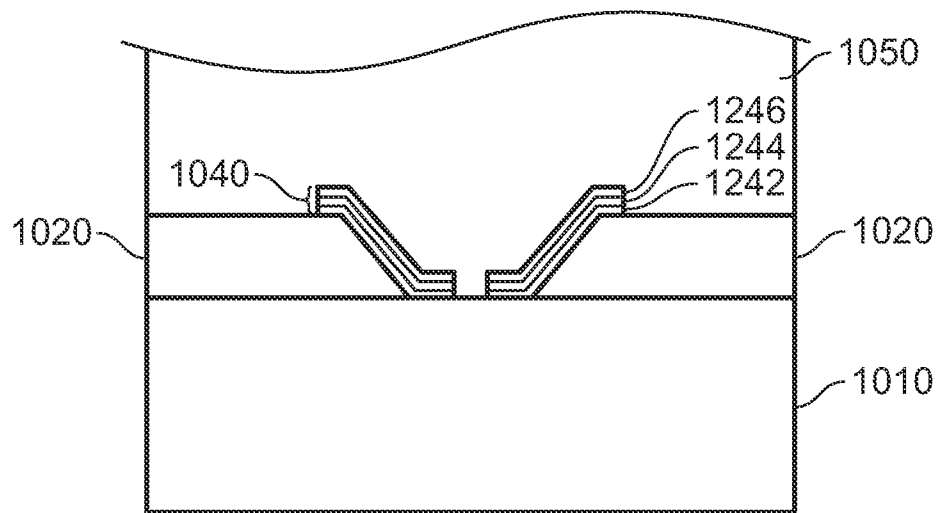


Figure 12A

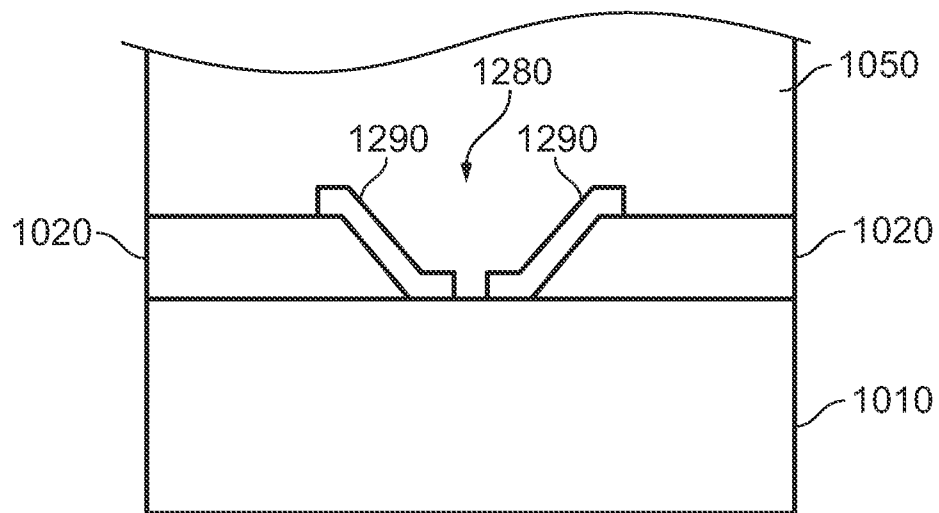


Figure 12B

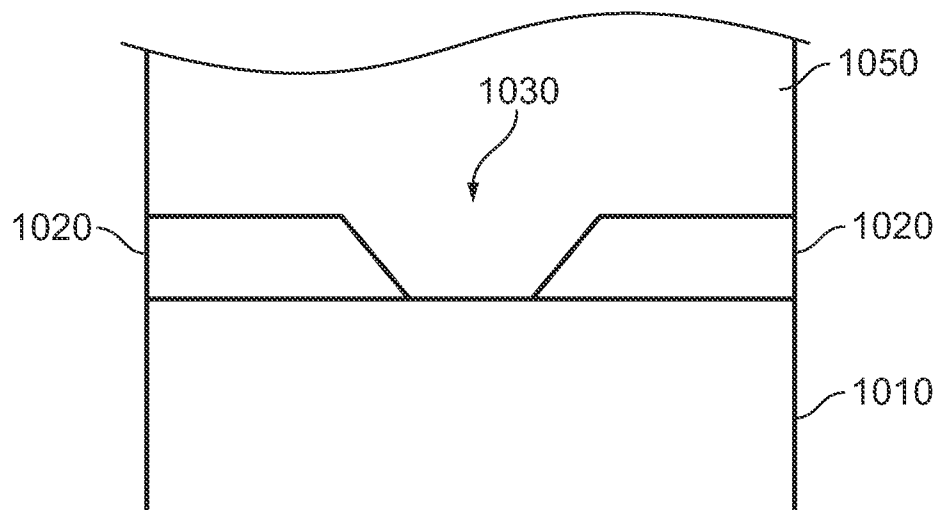
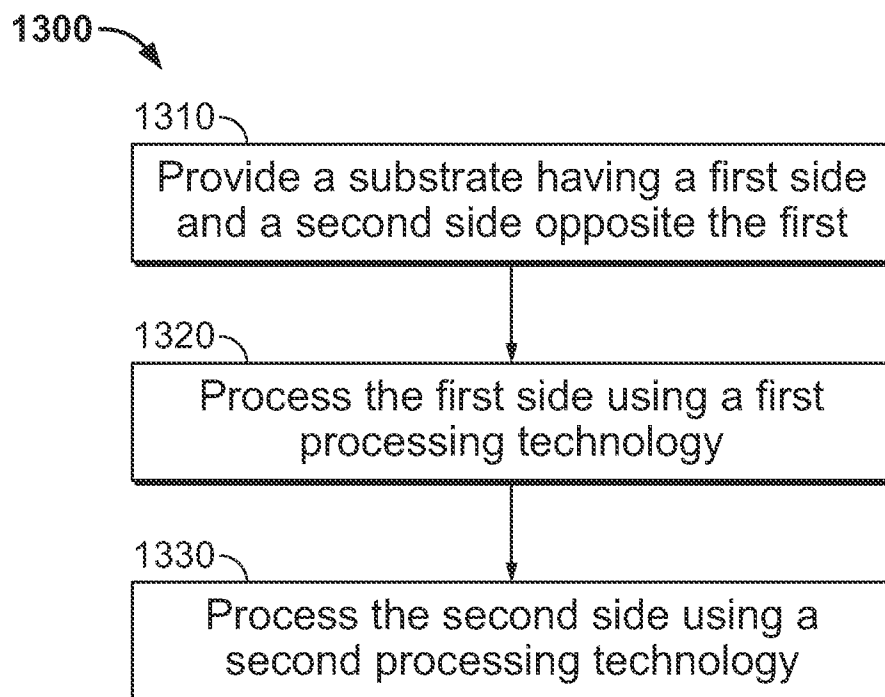


Figure 12C

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**Figure 13**

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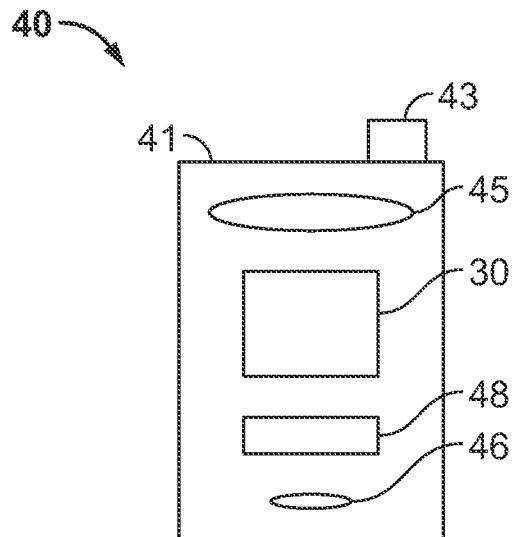


Figure 14A

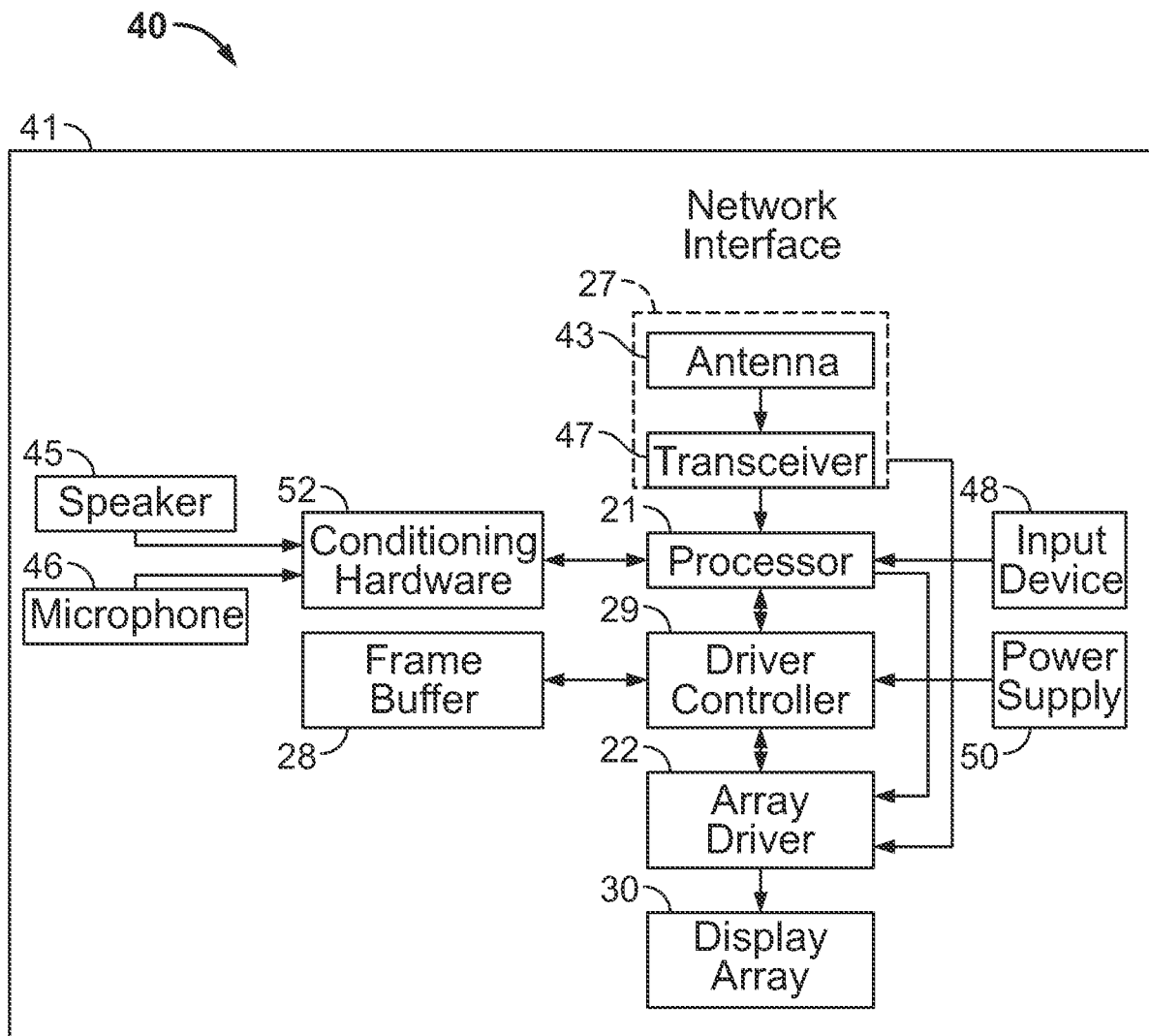


Figure 14B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/065191

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B26/00 G02B6/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/302218 A1 (BITA ION [US] ET AL) 2 December 2010 (2010-12-02) paragraphs [0111] - [0118], [0146]; figures 8,21H -----	1-35
X	US 2009/296193 A1 (BITA ION [US] ET AL) 3 December 2009 (2009-12-03) paragraph [0080]; figure 9a -----	1,12,32
A	US 2005/024890 A1 (YAMAMOTO KOICHI [JP] ET AL) 3 February 2005 (2005-02-03) claim 17 -----	1
X	EP 2 068 180 A1 (QUALCOMM MEMS TECHNOLOGIES INC [US]) 10 June 2009 (2009-06-10) -----	12,32
A	paragraphs [0060] - [0079]; figure 8 -----	1-11

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Further documents are listed in the continuation of Box C.

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See patent family annex.

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Date of the actual completion of the international search

31 January 2013

Date of mailing of the international search report

08/02/2013

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Authorized officer

Hambach, Dirk

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2012/065191

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