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(57) Abstract:

POWER MANAGENT SYSTEM FOR PSEUDO-ENVELOPE AND AVERAGE POWER TRACKING

Related Applications

[0001] The present application claims priority to U.S. Provisional Patent Application No. 61/482,702, filed May 5, 2011.

[0002] The present application claims priority to U.S. Provisional Patent Application No. 61/484,613, filed May 10, 2011.

[0003] The present application claims priority to U.S. Provisional Patent Application No. 61/508,202, filed July 15, 2011.

[0004] The present application claims priority to U.S. Provisional Patent Application No. 61/530,625, filed September 2, 2011.

[0005] The present application claims priority to U.S. Provisional Patent Application No. 61/544,051, filed October 06, 2011.

[0006] The present application claims priority to U.S. Provisional Patent Application No. 61/551,605, filed October 26, 2011.

[0007] The present application claims priority to U.S. Provisional Patent Application No. 61/565,138, filed November 30, 2011.

[0008] The present application claims priority to U.S. Provisional Patent Application No. 61/576,520, filed December 16, 2011.

[0009] The present application claims priority to and is a continuation-in-part of U.S. Patent Application No. 13/218,400, filed August 25, 2011, entitled "BOOST CHARGE-PUMP WITH FRACTIONAL RATIO AND OFFSET LOOP FOR SUPPLY MODULATION," which claims priority to U.S. Provisional Patent Application No. 61/376,877, filed August 25, 2010. U.S. Patent Application No. 13/218,400, filed August 25, 2011, is a continuation-in-part of U.S. Patent Application No. 13/089,917, filed April 19, 2011, which claims priority to U.S. Provisional Patent Application No. 61/325,659, filed April 19, 2010.

[0010] The present application claims priority to and is a continuation-in-part of international application No. PCT/US11/49243, filed August 25, 2011, entitled "BOOST CHARGE-PUMP WITH FRACTIONAL RATIO AND OFFSET LOOP

FOR SUPPLY MODULATION," which claims priority to U.S. Provisional Patent Application No. 61/376,877, filed August 25, 2010.

[0011] The present application claims priority to and is a continuation-in-part of international application No. PCT/US11/54106, filed September 29, 2011, entitled "SINGLE µC-BUCKBOOST CONVERTER WITH MULTIPLE REGULATED SUPPLY OUTPUTS," which claims priority to U.S. Provisional Patent Application No. 61/387,600, filed September 29, 2010.

[0012] The present application claims priority to and is a continuation-in-part of U.S. Patent Application No. 13/316,229, filed December 9, 2011, entitled "PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM WITH HIGH FREQUENCY RIPPLE CURRENT" which claims priority to U.S. Provisional Patent Application No. 61/421,348, filed December 9, 2010; U.S. Provisional Patent Application No. 61/421,475, filed December 9, 2010, and U.S. Provisional Patent Application No. 61/469,276, filed March 30, 2011. U.S. Patent Application No. 13/316,229, filed December 9, 2011 is a continuation-in-part of U.S. Patent Application No. 13/089,917, filed April 19, 2011, entitled “PSEUDO-ENVELOPE FOLLOWING POWER MANAGEMENT SYSTEM,” which claims priority to U.S. Provisional Patent Application No. 61/325,659, filed April 19, 2010. U.S. Patent Application No. 13/316,229, filed December 9, 2011 is a continuation-in-part of U.S. Patent Application No. 13/218,400, filed August 25, 2011, entitled “BOOST CHARGE-PUMP WITH FRACTIONAL RATIO AND OFFSET LOOP FOR SUPPLY MODULATION,” which claims priority to U.S. Provisional Patent Application No. 61/376,877, filed August 25, 2010. U.S. Patent Application No. 13/218,400, filed August 25, 2011, is a continuation-in-part of U.S. Patent Application No. 13/089,917, filed April 19, 2011, which claims priority to U.S. Provisional Patent Application No. 61/325,659, filed April 19, 2010.

[0013] The present application claims priority to and is a continuation-in-part of international application No. PCT/US11/64255, filed December 8, 2011, entitled "PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM WITH HIGH FREQUENCY RIPPLE CURRENT," which claims priority to U.S. Provisional Patent Application No. 61/421,348, filed December 9, 2010; U.S.

Provisional Patent Application No. 61/421,475, filed December 9, 2010, and U.S. Provisional Patent Application No. 61/469,276, filed March 30, 2011. U.S. Patent Application No. 13/316,229, filed December 9, 2011 is a continuation-in-part of U.S. Patent Application No. 13/089,917, filed April 19, 2011, entitled "PSEUDO-ENVELOPE FOLLOWING POWER MANAGEMENT SYSTEM," which claims priority to U.S. Provisional Patent Application No. 61/325,659, filed April 19, 2010. U.S. Patent Application No. 13/316,229, filed December 9, 2011 is a continuation-in-part of U.S. Patent Application No. 13/218,400, filed August 25, 2011, entitled "BOOST CHARGE-PUMP WITH FRACTIONAL RATIO AND OFFSET LOOP FOR SUPPLY MODULATION," which claims priority to U.S. Provisional Patent Application No. 61/376,877, filed August 25, 2010. U.S. Patent Application No. 13/218,400, is a continuation-in-part of U.S. Patent Application No. 13/089,917, filed April 19, 2011, which claims priority to U.S. Provisional Patent Application No. 61/325,659, filed April 19, 2010.

[0014] The present application claims priority to and is a continuation-in-part of U.S. Patent Application No. 13/367,973, filed February 7, 2012, entitled "GROUP DELAY CALIBRATION METHOD FOR POWER AMPLIFIER ENVELOPE TRACKING," which claims priority to U.S. Provisional Patent Application No. 61/440,089, filed February 7, 2011, and which is also filed as international application No. PCT/US12/24124.

[0015] The present application claims priority to and is a continuation-in-part of U.S. Patent Application No. 13/423,649, filed March 19, 2012, entitled "APPARATUSES AND METHODS FOR RATE CONVERSION AND FRACTIONAL DELAY CALCULATION USING A COEFFICIENT LOOK UP TABLE;" which claims priority to U.S. Provisional Patent Application No. 61/454,141, filed March 18, 2011, and U.S. Provisional Patent Application No. 61/454,226, filed March 18, 2011; and which is a continuation-in-part of U.S. Patent Application No. 13/367,973, filed February 7, 2012.

[0016] The present application claims priority to and is a continuation-in-part of U.S. Patent Application No. 13/363,888, filed February 1, 2012, entitled "FAST ENVELOPE SYSTEM CALIBRATION;" which is also filed as international

application No. PCT/US12/23495, on February 1, 2012; and which both claim priority to U.S. Provisional Patent Application No. 61/438,755, filed February 2, 2011.

[0017] All of the applications listed above are hereby incorporated herein by reference in their entireties.

Field of the Disclosure

[0018] The embodiments described herein relate to a power management system for delivering current to a linear radio frequency power amplifier. More particularly, the embodiments relate to the use of a pseudo-envelope tracker in a power management system of mobile communications equipment.

Background

[0019] Next-generation mobile devices are morphing from voice-centric telephones to message and multimedia-based "smart" phones that offer attractive new features. As an example, smart phones offer robust multimedia features such as web-browsing, audio and video playback and streaming, email access and a rich gaming environment. But even as manufacturers race to deliver ever more feature rich mobile devices, the challenge of powering them looms large.

[0020] In particular, the impressive growth of high bandwidth applications for radio-frequency (RF) hand-held devices has led to increased demand for efficient power saving techniques to increase battery life. Because the radio frequency power amplifier of the mobile device consumes a large percentage of the overall power budget of the mobile device, various power management systems have been proposed to increase the overall power efficiency of the radio frequency power amplifier.

[0021] As an example, some power managements systems may use a V_{RAMP} power control voltage to control the voltage presented on a power amplifier collector of a linear radio frequency power amplifier. As another example, other power management schemes may use a buck converter power supply and a

class AB amplifier in tandem to provide power to the linear radio frequency power amplifier.

[0022] Even so, there remains a need to further improve the power efficiency of mobile devices to provide extended battery life. As a result, there is a need to improve the power management system of mobile devices.

Summary

[0023] Embodiments disclosed in the detailed description relate to a pseudo-envelope follower power management system including a parallel amplifier and a switch mode power supply converter cooperatively coupled to generate a power supply voltage at a power supply output coupled to a linear radio frequency power amplifier. The parallel amplifier output is in communication with the power amplifier supply output. The parallel amplifier governs operation of the switch mode power supply converter and regulates the power amplifier supply voltage base on a V_{RAMP} signal. The parallel amplifier circuit includes an linear regular to provide an output current to regulate the power supply output when the parallel amplifier and switcher mode power supply converter are disabled in a low power modulation mode.

[0024] Embodiments disclosed in the detailed description relate to a pseudo-envelope follower power management system including a parallel amplifier and a switch mode power supply converter cooperatively coupled to generate a power supply voltage at a power supply output coupled to a linear radio frequency power amplifier. The parallel amplifier output is in communication with the power amplifier supply output. The parallel amplifier governs operation of the switch mode power supply converter and regulates the modulated power supply voltage base on a V_{RAMP} signal. The parallel amplifier circuit includes a linear regular to provide an output current to regulate the power supply output when the parallel amplifier and switcher mode power supply converter are disabled in a low power modulation mode.

[0025] As another embodiment, the open loop assist current circuit may generate an open loop assist current based on a target voltage for a power

amplifier supply voltage, (V_{RAMP}), and an estimate of a switching voltage generated by a switch mode power supply to reduce a parallel amplifier output current generated by a parallel amplifier configured to regulate a power amplifier supply voltage at the power amplifier supply output. The estimate of the switching voltage generated by the switch mode power supply may be either a scaled switching voltage or an switching voltage output estimate. An estimate of a load current of an RF power amplifier is generated based on a difference between the V_{RAMP} signal and a minimum power amplifier turn on a voltage parameter. An estimate of a bypass capacitor current is generated based on a product of an estimated bypass capacitor capacitance parameter and a derivative of a V_{RAMP} signal. An estimate of a power inductor current is generated based on an estimated power inductor inductance parameter, the estimate of the switching voltage, and the V_{RAMP} signal. An estimated power inductor voltage is calculated by subtracting the V_{RAMP} signal from the estimate of the switching voltage. The estimated power inductor voltage is integrated and scaled by a reciprocal of the estimated power inductor inductance parameter to generate the estimate of the power inductor current. A summing circuit subtracts the estimate of a bypass capacitor current and the estimate of a power inductor current from the estimate of a load current of an RF power amplifier to generate an estimate of an open loop assist current. A controlled current source generates an open loop assist current based on the estimate of an open loop assist current. The open loop assist current is provided and /or applied to a power amplifier supply output.

[0026] As another embodiment, examples of circuits, systems, and methods are described for an open loop assist circuit to generate an open loop assist current that assists a parallel amplifier circuit to regulate a radio frequency power amplifier supply voltage. The radio frequency power amplifier supply voltage may be a modulated power supply voltage that substantially tracks an envelope of a radio frequency signal to be generated by a radio frequency power amplifier. The open loop assist current may be generated based on an indication of a switching voltage generated by a switch mode power supply and a target voltage

for a power amplifier supply voltage. The target voltage may be a V_{RAMP} signal. The indication of a switching voltage may be an estimate of a future value of the switching voltage that is temporally related to an output current by the parallel amplifier based on the target voltage.

[0027] A parallel amplifier output impedance compensation circuit is configured to generate a compensated V_{RAMP} signal based on an estimate of a parallel amplifier output current provided by a parallel amplifier to regulate a power amplifier output voltage at a power amplifier supply output, an estimate of a bypass capacitor current provided by a bypass capacitor coupled between the power amplifier supply output and ground, and a V_{RAMP} signal. As an example, the parallel amplifier output impedance compensation circuit generates an estimate of a bypass capacitor current provided by a bypass capacitor coupled between a power amplifier supply output and ground based on a derivative of a V_{RAMP} signal used to set a target voltage for a power amplifier supply voltage and an estimate of a capacitance of the bypass capacitor. The estimate of the bypass capacitor current is combined with an estimate of a parallel amplifier output current provided by a parallel amplifier to regulate a power amplifier output voltage at the power amplifier supply output to create a dynamic current. The derivative of the dynamic current is scaled by a parallel amplifier inductance estimate parameter generating a power amplifier supply ripple voltage estimate. A V_{RAMP} signal is filtered by a frequency pre-distortion circuit to generate a peaked V_{RAMP} signal in order to compensate for a roll off of a modulation frequency response of the parallel amplifier.

[0028] As another embodiment, a system and method provides a compensated V_{RAMP} signal to a parallel amplifier to compensate for the non-ideal output impedance of the parallel amplifier, where the parallel amplifier regulates a power amplifier supply voltage. The compensated V_{RAMP} signal is generated based on a peaked V_{RAMP} signal and a power amplifier supply ripple voltage estimate. The power amplifier supply ripple voltage estimate is generated based on a product of an inductive characteristic of the parallel amplifier output impedance and a derivative of a dynamic current, where the dynamic current is

the sum of a parallel amplifier output current estimate and a bypass capacitor current estimate. The bypass capacitor is coupled between the power amplifier supply output and ground. A V_{RAMP} signal is filtered to generate the peaked V_{RAMP} signal to compensate for a roll off of a modulation frequency response of the parallel amplifier.

[0029] As another embodiment, a system and method for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output is provided. An offset voltage control circuit controls an offset voltage across a coupling circuit that is between the power amplifier supply output and the parallel amplifier circuit output. A summing circuit subtracts a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal. An integrator circuit integrates the offset voltage error signal to generate an offset voltage feedback signal, which is provided to a switch mode power supply converter to regulate the offset voltage across the coupling circuit. The integrator circuit may be an integrator with zero compensation. The offset voltage control circuit may be configured to pre-charge the coupling circuit for a pre-determined time period prior to a data transmission.

[0030] As another embodiment, a system and method for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output is provided. An offset voltage control circuit controls an offset voltage across a coupling circuit that is between the power amplifier supply output and the parallel amplifier circuit output. A summing circuit subtracts a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal. An error gain circuit scales the offset voltage error signal by an error gain value to generate an offset voltage feedback signal, which is provided to a switch mode power supply converter to regulate the offset voltage across the coupling circuit. The offset voltage control circuit may be configured to pre-charge the coupling circuit for a pre-determined time period prior to a data transmission.

[0031] As another embodiment, a system and method for automatically pre-charging an offset voltage across a coupling device coupled between a power amplifier supply output and a parallel amplifier circuit output is provided. A summing circuit generates an offset voltage error signal based on an offset voltage and a target offset voltage. An integrator having a normal mode of operation and a pre-charge mode of operation generates an offset voltage feedback signal based on the offset voltage error signal, which is provided to a switch mode power supply converter to regulate the offset voltage. Prior to commencement of a data transmission, a control circuit determines whether to operate the integrator in either the pre-charge mode of operation for a pre-determined time period or the normal mode of operation based on a magnitude of the offset voltage error signal. When the V_{RAMP} signal is not modulated, the integrator may operate in the pre-charge mode of operation.

[0032] As another embodiment, a pseudo-envelope follower power management system includes a feedback delay compensation circuit that generates a feedback delay compensation signal based on the slope of a V_{RAMP} signal to provide an early indication of a change in a target voltage of the power amplifier supply voltage. A switcher control circuit of a switch mode power supply converter uses the feedback delay compensation signal to compensate for a delay in generation of a feedback signal by a parallel amplifier circuit that regulates the power amplifier supply voltage. The switcher control circuit generates a feedback delay compensated feedback signal based on the feedback signal and the feedback delay compensation signal. The switcher control circuit governs generation of a switching voltage based on the feedback delay compensated feedback signal. A time constant of a high pass filter is adjusted to set the aggressiveness of the feedback delay compensation circuit.

[0033] As another embodiment, the parallel amplifier output impedance compensation circuit generates a compensated V_{RAMP} signal based on a combination of a pre-distorted V_{RAMP} signal and a difference between the V_{RAMP} signal and a switching voltage output estimate, where the switching voltage output estimate may be temporally aligned with the V_{RAMP} signal by

programmable delay circuitry. The parallel amplifier uses the compensated V_{RAMP} signal to regulate a power amplifier supply voltage.

[0034] The switch mode power supply converter generates a switching voltage output estimate. The parallel amplifier output impedance compensation circuit generates an expected difference signal based on a difference between a V_{RAMP} signal and the switching voltage output estimate. The parallel amplifier output impedance compensation circuit high pass filters and scales the expected difference signal to generate a high frequency ripple compensation signal based on a band of operation in which a communication device is assigned to operate. A pre-distortion filter circuit filters a V_{RAMP} signal to generate a pre-filtered V_{RAMP} signal in order to equalize a frequency response between a power amplifier supply output and an input configured to receive the V_{RAMP} signal based on a wideband modulation associated with a mode of operation of a communication device. The parallel amplifier output impedance compensation circuit combines the pre-filtered V_{RAMP} signal and the high frequency ripple compensation signal to generate a compensated V_{RAMP} signal.

[0035] As another embodiment, a system and method for compensating for the non-ideal output impedance of a parallel amplifier in a pseudo-envelope follower power management system generates a compensated V_{RAMP} signal. The parallel amplifier regulates a power amplifier supply voltage based on the compensated V_{RAMP} signal. A difference between a V_{RAMP} signal and an estimated switching voltage signal generated by a switch mode power supply converter are high pass filtered and scaled with a scaling factor to generate an estimated high frequency ripple signal. A pre-distortion filter generates a pre-distorted V_{RAMP} signal that is combined with the estimated high frequency ripple signal to form the compensated V_{RAMP} signal. The frequency response of the pre-distortion filter is adjusted to equalize a frequency response of the pseudo-envelope follower power management system. The scaling factor may be generated based on a band of operation a communication device is assigned to use in a communication network.

[0036] As another embodiment, an operational amplifier includes a first push-pull output stage, a second push-pull output stage having a first programmable transconductance, and a third push-pull output stage having a second programmable transconductance. The first push-pull output stage generates an operational amplifier output current. The second push-pull output stage includes a first array of mirrored transistor elements arranged to generate an output load current based on the operational amplifier output current. The second push-pull output stage transconductance is programmed by selectively controlling the operational state of mirrored transistor elements in the first array of mirrored transistor elements. The third push-pull output stage includes a second array of mirrored transistor elements arranged to generate a sensed output current that is fractionally related to the output load current by a sense scaling factor. The operational amplifier further includes an operational amplifier output isolation circuit to provide a feedback signal based an operational amplifier output current.

[0037] As another embodiment, a system and method for minimizing jitter of a programmable delay of a programmable delay circuit is provided. The programmable delay is provided by controlling a charge and discharge time of a variable capacitor. A first transistor charges the variable capacitor with a first bias current to provide a charging delay period. A second transistor charges the variable capacitor with a first bias current to provide a discharging delay period. To prevent jitter due to random charge building up on the source of the first transistor and the second transistor while they are in a non-conducting mode, a third transistor pulls the source of the first transistor to a first known voltage while the first transistor is off. A fourth transistor pulls the source of the second transistor to a second known voltage while the second transistor is off.

[0038] As another embodiment, a method and system for delaying a digital signal by a programmable delay period that is substantially insensitive to variations of a supply voltage is provided. A programmable delay circuit delays the digital signal by a programmable delay period. The programmable delay circuit delays the digital signal by controlling the propagation delay of the digital signal through a variable delay circuit. The propagation delay is created by

charging and discharging a variable capacitor with a capacitor current that is proportional to the supply voltage of the programmable delay circuit. An output buffer changes a logic state of an output buffer output based on a voltage developed on the variable capacitor and input logic threshold voltages of the output buffer. The sensitivity of the input logic threshold voltages to the supply voltage is substantially offset by the sensitive of the capacitor current to the supply voltage.

[0039] As another embodiment, a system and method for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output is provided. An offset voltage control circuit controls an offset voltage across a coupling circuit that is between the power amplifier supply output and the parallel amplifier circuit output. A summing circuit subtracts a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal. An integrator circuit integrates the offset voltage error signal to generate an offset voltage feedback signal, which is provided to a switch mode power supply converter to regulate the offset voltage across the coupling circuit. The integrator circuit may be an integrator with zero compensation. The offset voltage control circuit may be configured to pre-charge the coupling circuit for a pre-determined time period prior to a data transmission.

[0040] As another embodiment, an operational amplifier includes a first push-pull output stage, a second push-pull output stage having a first programmable transconductance, and a third push-pull output stage having a second programmable transconductance. The first push-pull output stage generates an operational amplifier output current. The second push-pull output stage includes a first array of mirrored transistor elements arranged to generate an output load current based on the operational amplifier output current. The second push-pull output stage transconductance is programmed by selectively controlling the operational state of mirrored transistor elements in the first array of mirrored transistor elements. The third push-pull output stage includes a second array of mirrored transistor elements arranged to generate a sensed output current that is

fractionally related to the output load current by a sense scaling factor. The operational amplifier further includes an operational amplifier output isolation circuit to provide a feedback signal based an operational amplifier output current.

[0041] As another embodiment, a rechargeable parallel amplifier includes a charge storage capacitor having a charge storage capacitor voltage, a NFET transistor configured to charge the charge storage capacitor as a function of the parallel amplifier output voltage, the charge storage capacitor voltage, and the minimum NFET headroom voltage to generate a parallel amplifier output current, and a first PFET transistor configured to discharge the charge storage capacitor function of the parallel amplifier output voltage, the charge storage capacitor voltage, and the minimum PFET headroom voltage to generate the parallel amplifier output current.

[0042] As another embodiment, a parallel amplifier includes a parallel amplifier output, a charge storage capacitor, a first PFET transistor and a first NFET transistor. The first NFET transistor charges the charge storage capacitor from the parallel amplifier output voltage when a sum of the parallel amplifier supply voltage plus a NFET headroom voltage is greater than the charge storage voltage of the charge storage capacitor to generate a parallel amplifier output current. The first PFET transistor discharges the charge storage capacitor when a sum of the parallel amplifier output voltage and a PFET headroom voltage is less than a charge storage voltage of the charge storage capacitor to generate the parallel amplifier output current.

[0043] As another embodiment, a rechargeable parallel amplifier includes an output stage having a first transistor configured to charge a charge storage capacitor from a power amplifier output supply as a function of a power amplifier supply voltage, a charge storage capacitor voltage of the charge storage capacitor, and the minimum PFET headroom voltage and a second transistor configured to generate a parallel amplifier output current from the charge storage capacitor as a function of the parallel amplifier output voltage, the charge storage capacitor voltage, and a minimum PFET headroom voltage.

[0044] As another embodiment, the parallel amplifier is configured to regulate a power amplifier supply voltage. The parallel amplifier includes a parallel amplifier output, a charge storage capacitor, a first PFET transistor and a first NFET transistor. The first NFET charges the charge storage capacitor from the power amplifier supply output when the power amplifier supply voltage is at least greater than a sum of the minimum NFET headroom voltage and a charge storage capacitor voltage of the charge storage capacitor. The first PFET discharges a charge storage capacitor when a sum of the parallel amplifier output voltage and a PFET headroom voltage is less than the charge storage voltage of the charge storage capacitor to generate a parallel amplifier output current. In addition, parallel amplifier includes a second PFET, a second NFET, an output control circuit, and a front end circuit having a first amplifier and a second amplifier.

[0045] As another embodiment, a bias reference and mirror circuit configured to generate a bias reference current that tracks a change in a propagation delay between a switcher control circuit and a switching voltage output of a switch mode power supply converter as a function of temperature such that the programmable delay period substantially tracks a change in propagation delay between a switcher control circuit and a switching supply voltage output of a switching mode power supply converter. As another embodiment, thee programmable delay circuit is configured to maintain time alignment between the switching voltage at the switching voltage output of the switching power supply converter and the predicted / future value provided to an open loop high frequency ripple compensation circuit. A bias reference and mirror circuit configured to generate a bias reference current that tracks a change in a propagation delay between a switcher control circuit and a switching voltage output of a switch mode power supply converter as a function of temperature, voltage, and/or a combination thereof. There are two approaches.

[0046] As another embodiment, a voltage reference circuit that sets a reference voltage may include a compensation current source that adjust a current through a current setting resistor of a voltage divider circuit with respect

to temperature, supply voltage, or a combination thereof. The reference voltage controls a bias reference current generated across a resistor, which is mirrored to create a first bias current and a second bias current. A variable capacitor is charged and discharged with the figure bias current and the second bias current, respectively, to delay propagation of an input signal through the programmable delay circuit.

[0047] As another embodiment, the voltage reference circuit is a voltage divider circuit and sets a reference voltage across the current setting resistor in the bias reference and mirror circuit. A compensation current source is coupled to the current mirror circuit to sink a portion of the reference bias current as a function of temperature, supply voltage, and/or a combination thereof.

[0048] As another embodiment, the compensation current source is configured to adjust the first bias current and the second bias current such that the propagation delay through the programmable delay circuit changes to track the change in propagation delay between a switch control circuit and a switching voltage output of a switch mode power supply converter as a function of temperature and a function of a supply voltage. In some embodiments, the compensation current source may be configured to also take into consideration a change in the propagation delay between the output of the output buffer and the application of the high frequency ripple compensation current generated by the open loop high frequency ripple compensation circuit

[0049] A first embodiment of pseudo-envelope follower power management system with high frequency ripple compensation includes a switch mode power supply converter and an open loop high frequency ripple compensation assist circuit. For example, the switch mode power supply converter may be configured to operate as a buck converter. As another example, the switch mode power supply converter may be configured to operate as a multi-level charge pump buck converter. The switch mode power supply may generate a switching output voltage and a switching voltage output estimate. The switching voltage output estimate may provide an early indication of a future voltage level of the switching output voltage. For example, in some embodiments, the switch mode power

supply converter may also include programmable delay circuitry, a switcher control circuit, and a buffer scalar. The switcher control circuit may generate a digital switching voltage output signal that represents a state of the switcher control circuit used to control generation of the switching output voltage by the switch mode power supply converter. The programmable delay circuitry may receive the digital switching voltage output signal, and delay the digital switching voltage output signal by a programmable delay period to generate a delayed digital switching voltage output signal. The buffer scalar is configured to receive the delayed digital switching voltage output signal, and generate the switching voltage output estimate based on the delayed digital switching voltage output signal and a buffer scalar.

[0050] The open loop high frequency ripple compensation assist circuit is configured to receive the switching voltage output estimate and a V_{RAMP} signal. Based on the based on the switching voltage output estimate and the V_{RAMP} signal, the open loop high frequency ripple compensation assist circuit generates a high frequency ripple compensation current. The open loop high frequency ripple compensation assist circuit applies the high frequency ripple compensation current to a power amplifier supply output to reduce high frequency ripple current at the power amplifier supply output. The power amplifier supply output is configured to power a linear radio frequency power amplifier. The high frequency ripple compensation current is generated in a frequency band located substantially near a transmit to receive duplex offset for a band of operation in a communication network, where the frequency band of the high frequency ripple compensation current has a bandwidth substantially equal to a bandwidth of a receiver channel frequency band for the band of operation.

[0051] In some embodiments, the switch mode power supply converter further includes a programmable delay circuitry configured to delay generation of the switching voltage output estimate by a programmable delay period. The programmable delay period may be configured to temporally align the switching voltage output estimate and the V_{RAMP} signal to position a notch in a ripple rejection response of the power amplifier supply output near the transmit to

receive duplex offset for the band of operation. In addition, the open loop high frequency ripple compensation assist circuit may generate a scaled high frequency ripple compensation current estimate based on the high frequency ripple compensation current, which can be used as part of a feedback signal to the switch mode power supply converter. As an example, the switch mode power supply converter may receive a feedback signal, wherein the feedback signal is based on the scaled high frequency ripple compensation current estimate, where the switch mode power supply converter adjusts the switching output voltage based on the feedback signal. In some embodiments, the pseudo-envelope follower power management system with high frequency ripple compensation further includes a parallel amplifier. The parallel amplifier receives the V_{RAMP} signal and a power amplifier supply voltage from the power amplifier supply output. Based on a difference between the V_{RAMP} signal and the power amplifier supply voltage, the parallel amplifier generates a parallel amplifier output current. The parallel amplifier applies the parallel amplifier output current to the power amplifier supply output to control the power amplifier supply voltage. In addition, the parallel amplifier may generate a scaled parallel amplifier output current estimate based on the parallel amplifier output current. The scaled parallel amplifier output current estimate may be combined with the scaled high frequency ripple compensation current estimate to create the feedback signal provided to the switch mode power supply converter.

[0052] Some embodiments of open loop high frequency ripple compensation assist circuit may include a filter network having a first node and a second node, a feedback network having a first node and a second node, and an operational amplifier including a non-inverting input, an inverting input, and an operational amplifier output. The first node of the filter network may be configured to receive the switching voltage output estimate. The second node of the filter network may be in communication with the inverting input of the operational amplifier. The first node of the feedback network may be in communication with the second node of the filter network and the inverting input of the operational amplifier. In addition, the second node of the feedback network may be in communication with the

operational amplifier output. The operational amplifier may be configured to generate the high frequency ripple compensation current. The operational amplifier may also be configured to generate a scaled high frequency ripple compensation current estimate as a function of the high frequency ripple compensation current. The operational amplifier may include a first push-pull output stage in communication with the operational amplifier output, where the first push-pull output stage generates an operational amplifier output current. A bias capacitor having a bias capacitance and a bias resistor may be arranged in series between the operational amplifier output and a reference voltage. For example, the reference voltage may be ground. The first push-pull output stage may have a first stage transconductance. The bias capacitance may be configured such that the first stage transconductance of the first push-pull output stage is substantially equal to a transconductance of the bias resistor in a frequency band located substantially near a transmit to receive duplex offset for a band of operation in a communication network. The open loop high frequency ripple compensation assist circuit may also include an operational amplifier output isolation circuit including a high impedance input in communication with the operational amplifier output and an isolated feedback node in communication with the second node of the feedback network. The operational amplifier may also include a second push-pull output stage configured to generate the high frequency ripple compensation current, where the high frequency ripple compensation current is mirrored to the operational amplifier output current. The second push-pull output stage may include a programmable second output stage transconductance. The programmable second output stage transconductance second output stage transconductance may be a substantially linear function of a programmable transconductance parameter. The open loop high frequency ripple compensation assist circuit may adjust a magnitude of the high frequency ripple compensation current based on the programmable second output stage transconductance. The operational amplifier may also include a third push-pull output stage configured to generate the scaled high frequency ripple

compensation current estimate as a function of the high frequency ripple compensation current based on a sense scaling factor.

[0053] The filter network may be associated with a first corner frequency of a filter response of the open loop ripple compensation assist circuit. The feedback network may be associated with a second corner frequency of the frequency response of the open loop ripple compensation assist circuit. In some cases, the first corner frequency has a programmable range between 3MHz and 11.5MHz and the second corner frequency has a programmable range between 3MHz and 11.5MHz. In other cases, the first corner frequency is substantially equal to 6 MHz, and the second corner frequency is substantially equal to 6 MHz.

[0054] Another example embodiment includes a method for reducing high frequency ripple currents at a power amplifier supply output. The method may include a first step of generating a switching output voltage and a switching voltage output estimate with a switch mode power supply converter, where the switching voltage output estimate provides an early indication of a future voltage level of the switching output voltage. The method may include the step of receiving the switching voltage output estimate and a V_{RAMP} signal at an open loop high frequency ripple compensation assist circuit. The method may include the step of generating a high frequency ripple compensation current based on the switching voltage output estimate and the V_{RAMP} signal. The method may include the step of applying the high frequency ripple compensation current to a power amplifier supply output to reduce high frequency ripple current at the power amplifier supply output. In some embodiments the generation of the high frequency ripple compensation current based on the switching voltage output estimate and the V_{RAMP} signal may include generating the high frequency ripple compensation current within in a frequency band located substantially near a transmit to receive duplex offset for a band of operation in a communication network. In addition, the frequency band of the high frequency ripple compensation current may have a bandwidth substantially equal to a bandwidth of a receiver channel frequency band for the band of operation. In some

embodiments, generation of the switching voltage output estimate may include delaying generation of the switching voltage output estimate by a programmable delay period to temporally align the switching voltage output estimate and the V_{RAMP} signal to position a notch in a ripple rejection response of the power amplifier supply output near the transmit to receive duplex offset for the band of operation. In addition, the method may further include a step for generating a scaled high frequency ripple compensation current estimate based on the high frequency ripple compensation current. Based on the scaled high frequency ripple compensation current estimate, the method may form a feedback signal, which is provided to the switch mode power supply converter. The switch mode power supply converter may adjust the switching output voltage based on the feedback signal. In some embodiments, the switch mode power supply converter is configured to be a buck converter. Alternatively, in other embodiments, the switch mode power supply converter is configured to be a multi-level charge pump buck converter.

[0055] One example embodiment of the pseudo-envelope follower power management system may include a switch mode power supply converter and a parallel amplifier cooperatively coupled to provide a linear radio frequency power amplifier supply to a linear radio frequency power amplifier. The pseudo-envelope follower power management system may include a charge pump configured to power the parallel amplifier. The charge pump may generate a plurality of output voltage levels. The charge pump may be either a boost charge pump or a boost/buck charge pump. The pseudo-envelope follower power management system may include an offset voltage control circuit configured to provide feedback to the switch mode power supply converter to regulate an offset voltage developed across a coupling device that couples the output of the parallel amplifier to the linear radio frequency power amplifier supply.

[0056] Another example embodiment of a power management system for a linear radio frequency power amplifier includes a switch mode power supply converter and a parallel amplifier operatively coupled to generate a linear radio frequency power amplifier supply output for a linear radio frequency power

amplifier of a radio frequency device. The switch mode power supply converter may be configured to generate a plurality of switching voltage levels on a switching voltage output. The switching voltage output of the switch mode power supply converter may be coupled via a power inductor to the linear radio frequency power amplifier supply output. A bypass capacitor may be coupled between the linear radio frequency power amplifier supply output and ground such that the power inductor and bypass capacitor form a low pass filter for the switch mode power supply converter. The parallel amplifier may include a parallel amplifier output coupled, via a coupling device, to the linear radio frequency power amplifier supply output. As an example, the coupling device may be a coupling capacitor. The power management system may further include a charge pump configured to provide a charge pump parallel amplifier power supply output. The charge pump may include a first flying capacitor, a second flying capacitor, a plurality of switches operably coupled to form the charge pump parallel amplifier power supply output. The charge pump may be configured to selectively generate various output voltage levels, derived from a supply voltage, on the charge pump parallel amplifier power supply output. In addition, the charge pump parallel amplifier power supply output may be configured to provide an operational power supply voltage to the parallel amplifier.

[0057] Another example embodiment of a pseudo-envelope follower power management system may include a multi-level charge pump buck converter and a parallel amplifier configured to operate in tandem to generate a power amplifier supply voltage output for a linear radio frequency power amplifier. The multi-level charge pump buck converter may include a supply input configured to receive a direct current (DC) voltage, and a switching voltage output. The switching voltage output is coupled to the power amplifier supply voltage output by a power inductor, where the power inductor couples to a bypass capacitor to form an output filter for the switching voltage output of the multi-level charge pump buck converter. For example, the direct current (DC) voltage may be a battery voltage. The parallel amplifier may include a supply input configured to

receive the direct current (DC) voltage, an amplifier output, a first control input configured to receive a V_{RAMP} signal, and a second control input configured to receive the power amplifier supply voltage. The amplifier output may be coupled to the power amplifier supply voltage by a coupling circuit. In some embodiments of the pseudo-envelope follower system, the coupling circuit may be an offset capacitor. In other embodiments of the pseudo-envelope follower system, the coupling circuit may be a wire trace such that the offset voltage between the amplifier output and the power amplifier supply voltage is zero volts.

[0058] In addition, the multi-level charge pump buck converter may generate a feed forward control signal configured to provide an indication of the output state of the switching voltage output to the parallel amplifier. In some embodiments, the switching voltage output is provided as the feed forward control signal. In other embodiments, the feed forward control signal is generated by a switcher control circuit and provides an indication of the switching voltage output based on the state of the switcher control circuit. The parallel amplifier may include a parallel amplifier output current estimate signal that provides an estimate of the output current of the parallel amplifier. In some embodiments of the pseudo-envelope follower system, the parallel amplifier may also generate a threshold offset signal. The threshold offset signal may be configured to estimate the magnitude of the offset voltage appearing across the coupling circuit.

[0059] The multi-level buck converter may include a supply input configured to receive a direct current (DC) voltage, a switching voltage output coupled to a power inductor, a switcher control circuit, a multi-level charge pump circuit having a control input, a charge pump supply input configured to receive the DC voltage, a series switch having a first switch terminal, a second switch terminal, and a series control terminal and a shunt switch having a first switch terminal, a second switch terminal, and a shunt control terminal. The first terminal of the series switch may be coupled to the supply input of the multi-level buck converter. The second terminal of the series switch may be coupled to the first terminal of the series switch to form a switching voltage output. The second terminal of the

series switch may be coupled to ground. The boost charge pump circuit may include a charge pump control input, a charge pump supply input coupled to the supply input of the multi-level buck converter, and a charge pump output coupled to the supply input of the multi-level buck converter. The boost charge pump includes a plurality of switches and two flying capacitors that provide for three modes of operation. In a charging mode of operation, the flying capacitors are coupled in series between the charge pump supply input and ground, and the flying capacitors are switchably disconnected from the charge pump output. In a first boost mode of operation, the flying capacitors are arranged in parallel between the charge pump output and the charge pump supply input to generate a 3/2 x the DC voltage output at the charge pump output. In a second boost mode of operation, the flying capacitors are arranged in series between the charge pump output and the charge pump supply input to generate a 2 x the DC voltage output at the charge pump output. The multi-level buck converter may include four modes of operation. In a first mode of operation, the series switch is open, the boost charge pump is in the charging mode of operation, and the shunt switch is closed to generate zero volts at the switching voltage output. In a second mode of operation, the series switch is closed, the boost charge pump is in the charging mode of operation, and the shunt switch is open to generate the DC voltage output at the switching voltage output. In a third mode of operation, both the series switch and the shunt switch are open and the boost charge pump is in the first boost mode of operation to generate a 3/2 x the DC voltage output at the switching mode output. In a fourth mode of operation, both the series switch and the shunt switch are open and the boost charge pump is in the second boost mode of operation to generate a 2 x the DC voltage output at the switching mode output.

[0060] Those skilled in the art will appreciate the scope of the disclosure and realize additional aspects thereof after reading the following detailed description in association with the accompanying drawings.

Brief Description of the Drawings

[0061] The accompanying drawings incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0062] Figure 1A depicts an embodiment of a pseudo-envelope follower power management system for managing power supplied to a linear radio frequency power amplifier.

[0063] Figure 1B depicts an embodiment of a pseudo-envelope follower power management system for managing power supplied to a linear radio frequency power amplifier.

[0064] Figure 2A depicts an embodiment of the pseudo-envelope follower power management system of Figure 1A in further detail.

[0065] Figure 2B depicts an embodiment of the pseudo-envelope follower power management system of Figure 1B in further detail.

[0066] Figure 3A depicts an embodiment of a portion of a multi-level charge pump buck converter.

[0067] Figure 3B depicts another embodiment of a portion of a multi-level charge pump buck converter.

[0068] Figure 3C depicts another embodiment of a portion of a multi-level charge pump buck converter.

[0069] Figure 3D depicts another embodiment of a portion of a multi-level charge pump buck converter.

[0070] Figure 3E depicts another embodiment of a portion of a buck converter.

[0071] Figure 3F depicts another embodiment of a portion of a buck converter.

[0072] Figure 3G depicts another embodiment of a portion of a buck converter.

[0073] Figure 3H depicts another embodiment of a portion of a buck converter.

[0074] Figure 3I depicts an embodiment of a switcher control circuit for a multi-level charge pump buck converter having feedback compensation.

[0075] Figure 3J depicts an embodiment of a switcher control circuit for a multi-level charge pump buck converter having feedback compensation.

[0076] Figure 3K depicts an embodiment of a switcher control circuit for a multi-level charge pump buck converter having feedback compensation.

[0077] Figure 3L depicts an embodiment of a switcher control circuit for a multi-level charge pump buck converter having feedback compensation.

[0078] Figure 3M depicts an embodiment of a switcher control circuit for a buck converter having feedback compensation.

[0079] Figure 3N depicts an embodiment of a switcher control circuit for a buck converter having feedback compensation.

[0080] Figure 3P depicts an embodiment of a switcher control circuit for a buck converter having feedback compensation.

[0081] Figure 3Q depicts an embodiment of a switcher control circuit for a buck converter having feedback compensation.

[0082] Figure 3R depicts an embodiment of a switcher control circuit for a multi-level charge pump buck converter having feedback compensation.

[0083] Figure 4A depicts an embodiment of a threshold detector and control circuit of a switcher control circuit of a multi-level charge pump buck converter.

[0084] Figure 4B depicts another embodiment of a threshold detector and control circuit of a switcher control circuit of a multi-level charge pump buck converter.

[0085] Figure 4C depicts another embodiment of a threshold detector and control circuit of a switcher control circuit of a multi-level charge pump buck converter.

[0086] Figure 4D depicts another embodiment of a threshold detector and control circuit of a switcher control circuit of a multi-level charge pump buck converter.

[0087] Figure 4E depicts an embodiment of a threshold detector and control circuit of a buck converter.

[0088] Figure 4F depicts another embodiment of a threshold detector and control circuit of a buck converter.

[0089] Figure 4G depicts another embodiment of a threshold detector and control circuit of a buck converter.

[0090] Figure 4H depicts another embodiment of a threshold detector and control circuit of a buck converter.

[0091] Figure 4I depicts an embodiment of a threshold detector and control circuit of a multi-level charge pump buck converter that includes feedback compensation.

[0092] Figure 4J depicts an embodiment of a threshold detector and control circuit of a multi-level charge pump buck converter that includes feedback compensation.

[0093] Figure 4K depicts another embodiment of a threshold detector and control circuit of a multi-level charge pump buck converter that includes feedback compensation.

[0094] Figure 4L depicts another embodiment of a threshold detector and control circuit of a multi-level charge pump buck converter that includes feedback compensation.

[0095] Figure 4M depicts an embodiment of a threshold detector and control circuit of a buck converter that includes feedback compensation.

[0096] Figure 4N depicts another embodiment of a threshold detector and control circuit of a buck converter that includes feedback compensation.

[0097] Figure 4P depicts another embodiment of a threshold detector and control circuit of a buck converter that includes feedback compensation.

[0098] Figure 4Q depicts another embodiment of a threshold detector and control circuit of a buck converter that includes feedback compensation.

[0099] Figure 4R depicts another embodiment of a threshold detector and control circuit of a multi-level charge pump buck converter that includes feedback compensation.

[00100] Figure 4S depicts an embodiment of a threshold detector for envelope and average power tracking modes of operation.

[00101] Figure 5A depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4A.

[00102] Figure 5B depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4B.

[00103] Figure 5C depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4C.

[00104] Figure 5D depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4D.

[00105] Figure 5E depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4E.

[00106] Figure 5F depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4F.

[00107] Figure 5G depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4G.

[00108] Figure 5H depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4H.

[00109] Figure 5L depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4L

[00110] Figure 5Q depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4Q.

[00111] Figure 5R depicts an embodiment of a first state machine of the threshold detector and control circuit of Figure 4R.

[00112] Figure 5S depicts an embodiment of an average power tracking mode of operation of the threshold detector and control circuit of Figure 4D.

[00113] Figure 6A depicts an embodiment of a second state machine of the threshold detector and control circuit of Figure 4A.

[00114] Figure 6B depicts an embodiment of a second state machine of the threshold detector and control circuit of Figure 4B.

[00115] Figure 6C depicts an embodiment of a second state machine of the threshold detector and control circuit of Figure 4C.

[00116] Figure 6D depicts an embodiment of a second state machine of the threshold detector and control circuit of Figure 4D.

[00117] Figure 6L depicts an embodiment of a second state machine of the threshold detector and control circuit of Figure 4L.

[00118] Figure 6R depicts an embodiment of a second state machine of the threshold detector and control circuit of Figure 4R.

[00119] Figure 7A depicts one embodiment of a multi-level charge pump circuit of a pseudo-envelope follower power management system.

[00120] Figure 7B depicts another embodiment of a multi-level charge pump circuit of a pseudo-envelope follower power management system.

[00121] Figure 7C depicts still another embodiment of a multi-level charge pump circuit of a pseudo-envelope follower power management system.

[00122] Figure 7D depicts an additional embodiment of the multi-level charge pump circuit configured to provide a

[00123] Figure 8 depicts one embodiment of a V_{OFFSET} loop circuitry of a parallel amplifier circuit of a pseudo-envelope follower power management system.

[00124] Figure 9A depicts an embodiment of the open loop assist circuit of a parallel amplifier circuit of a pseudo-envelope follower power management system.

[00125] Figure 9B depicts an embodiment of the open loop assist circuit of a parallel amplifier circuit of a pseudo-envelope follower power management system.

[00126] Figure 10 depicts an embodiment of a parallel amplifier output impedance compensation circuit of a parallel amplifier circuit of a pseudo-envelope follower power management system.

[00127] Figure 11A depicts one embodiment of the indication of the switching voltage output generated by a multi-level charge pump buck converter in a pseudo-envelope follower power management system.

[00128] Figure 11B depicts another embodiment of the indication of the switching voltage output generated by a multi-level charge pump buck converter in a pseudo-envelope follower power management system.

[00129] Figure 11C depicts another embodiment of the indication of the switching voltage output generated by a multi-level charge pump buck converter in a pseudo-envelope follower power management system.

[00130] Figure 11D depicts another embodiment of the indication of the switching voltage output generated by a multi-level charge pump buck converter in a pseudo-envelope follower power management system.

[00131] Figure 11E depicts another embodiment of the indication of the switching voltage output generated by a multi-level charge pump buck converter in a pseudo-envelope follower power management system.

[00132] Figure 11F depicts another embodiment of the indication of the switching voltage output generated by a multi-level charge pump buck converter in a pseudo-envelope follower power management system

[00133] Figure 12A depicts one embodiment of a parallel amplifier used in a pseudo-envelope follower power management system.

[00134] Figure 12B depicts one embodiment of a rechargeable parallel amplifier used in a pseudo-envelope follower power management system.

[00135] Figure 12C depicts another embodiment of a rechargeable parallel amplifier used in a pseudo-envelope follower power management system.

[00136] Figure 12D depicts one embodiment of a parallel amplifier used in a pseudo-envelope follower power management system.

[00137] Figure 12E depicts another embodiment of a rechargeable parallel amplifier used in a pseudo-envelope follower power management system.

[00138] Figure 12F depicts another embodiment of a rechargeable parallel amplifier used in a pseudo-envelope follower power management system.

[00139] Figure 13 depicts an embodiment of a pseudo-envelope follower power management system including a buck converter and a parallel amplifier circuit having an open loop assist circuit and a parallel amplifier circuit.

[00140] Figure 14 depicts another embodiment of a pseudo-envelope follower power management system including a multi-level charge pump buck converter and a parallel amplifier circuit having both an open loop assist circuit and a parallel amplifier circuit.

[00141] Figure 15 depicts another embodiment of a pseudo-envelope follower power management system including a multi-level charge pump buck converter and a parallel amplifier circuit having a parallel amplifier circuit and a V_{OFFSET} loop circuit.

[00142] Figure 16 depicts another embodiment of a pseudo-envelope follower power management system including a multi-level charge pump buck converter and a parallel amplifier circuit having a parallel amplifier, a V_{OFFSET} loop circuit, an open loop assist circuit and a parallel amplifier output impedance compensation circuit.

[00143] Figure 17A depicts another embodiment of pseudo-envelope follower power management system including a buck converter and a parallel amplifier circuit having a rechargeable parallel amplifier circuit.

[00144] Figure 17B depicts another embodiment of a pseudo-envelope follower power management system including a buck converter and a parallel amplifier circuit having a parallel amplifier circuit.

[00145] Figure 18A depicts an embodiment of a pseudo-envelope follower power management system having a multi-level charge pump buck converter and a µC charge pump circuit configured to provide a parallel amplifier power supply to a parallel amplifier circuit.

[00146] Figure 18B depicts another embodiment of a pseudo-envelope follower power management system having a multi-level charge pump buck converter and a µC charge pump circuit configured to provide a parallel amplifier power supply to a parallel amplifier circuit.

[00147] Figure 18C depicts an embodiment of a pseudo-envelope follower power management system having a buck converter and a µC charge pump circuit configured to provide a parallel amplifier power supply to a parallel amplifier circuit.

[00148] Figure 18D depicts another embodiment of a pseudo-envelope follower power management system having a buck converter and a μC charge pump circuit configured to provide a parallel amplifier power supply to a parallel amplifier circuit.

[00149] Figure 19A depicts an embodiment of a μC charge pump circuit configured to provide a parallel amplifier power supply to a parallel amplifier circuit of a pseudo-envelope follower power management system.

[00150] Figure 19B depicts another embodiment of a μC charge pump circuit configured to provide a parallel amplifier power supply to a parallel amplifier circuit of a pseudo-envelope follower power management system, where the μC charge pump circuit includes both buck and boost modes of operation.

[00151] Figures 20A-C depict functionally equivalent circuit topologies of the μC charge pump circuit of Figure 19A for different modes of operation of the μC charge pump circuit.

[00152] Figure 21 depicts a method for configuring a μC charge pump circuit to provide a supply voltage to a parallel amplifier prior to commencement of a data transmission by a linear radio frequency power amplifier.

[00153] Figure 22 depicts a method for pre-charging a V_{OFFSET} loop circuit prior to commencement of a data transmission by a linear radio frequency power amplifier.

[00154] Figure 23A depicts an embodiment of a pseudo-envelope follower power management system including a multi-level charge pump buck converter and an embodiment of a parallel amplifier circuit that includes an open loop ripple compensation assist circuit.

[00155] Figure 23B depicts an embodiment of a pseudo-envelope follower power management system including a buck converter and an embodiment of a parallel amplifier circuit that includes an open loop ripple compensation assist circuit.

[00156] Figure 23C depicts an embodiment of a pseudo-envelope follower power management system including a multi-level charge pump buck converter

and an embodiment of a parallel amplifier circuit that includes an open loop ripple compensation assist circuit in combination with an open loop assist circuit.

[00157] Figure 23D depicts an embodiment of a pseudo-envelope follower power management system including a buck converter and an embodiment of a parallel amplifier circuit that includes an open loop ripple compensation assist circuit in combination with an open loop assist circuit.

[00158] Figure 24 depicts an embodiment of the open loop ripple compensation assist circuit and corresponding programmable delay circuitry of the pseudo-envelope follower power management systems depicted in Figures 23A-23D.

[00159] Figure 25 depicts three example ripple rejection response curves for an embodiment of the pseudo-envelope follower power management system, where each example ripple rejection response curve corresponds to a different programmable delay.

[00160] Figure 26 further depicts an embodiment of the high pass circuitry depicted in Figure 25.

[00161] Figure 27A depicts an embodiment of the open loop ripple compensation assist circuit of Figures 23A-23D.

[00162] Figure 27B that depicts an alternative embodiment of the open loop ripple compensation assist circuit of Figures 23A-23D.

[00163] Figure 28A depicts example ripple rejection response curves for an example pseudo-envelope follower power management system having an operational amplifier isolation circuit.

[00164] Figure 28B depicts example ripple rejection response curves for an example pseudo-envelope follower power management system not having an operational amplifier isolation circuit.

[00165] Figure 29A depicts an embodiment of the programmable delay circuitry depicted in Figure 24.

[00166] Figure 29B depicts another example embodiment of the programmable delay circuitry depicted in Figure 24.

[00167] Figure 30A depicts another example embodiment of the programmable delay circuitry depicted in Figure 24.

[00168] Figure 30B depicts another example embodiment of the programmable delay circuitry depicted in Figure 24.

[00169] Figure 30C depicts another example embodiment of the programmable delay circuitry depicted in Figure 24.

[00170] Figure 31A depicts an example embodiment of the operational amplifier of the embodiment of an operational amplifier circuitry depicted in Figure 27A.

[00171] Figure 31B depicts an example embodiment of the operational amplifier depicted in Figurer 27B, where the operational amplifier output isolation circuit is not present.

[00172] Figure 32A depicts an example embodiment of an operational amplifier push-pull output stage circuit configured to generage a high frequency ripple compensation current (I_{COR}).

[00173] Figure 32B depicts an example embodiment of an operational amplifier configured to generate a scaled high frequency ripple compensation current estimate (I_{COR_SENSE}) as a function of the high frequency ripple compensation current (I_{COR}).

[00174] Figure 32C depicts an example embodiment of the Gm bias circuit and operational amplifier isolation circuit of the embodiment of the operational amplifier circuitry.

[00175] Figure 32D depicts an example embodiment of the Gm bias circuit of the operational amplifier.

[00176] Figure 33 depicts a graphical representation of the programmable transconductance (Gm) output current function of an example embodiment of the operational amplifier controlled I_{COR} current circuit.

[00177] Figure 34A depicts an embodiment of a parallel amplifier output impedance compensation circuit including a digital V_{RAMP} pre-distortion filter circuit.

[00178] Figure 34B depicts an alternative embodiment of a parallel amplifier output impedance compensation circuit.

[00179] Figure 34C depicts another embodiment of a parallel amplifier output impedance compensation circuit including an analog V_{RAMP} pre-distortion filter circuit.

[00180] Figure 34D depicts an alternative embodiment of a parallel amplifier output impedance compensation circuit.

[00181] Figure 34E depicts an alternative embodiment of a parallel amplifier output impedance compensation circuit.

[00182] Figure 35 depicts embodiments of the digital V_{RAMP} pre-distortion filter and a V_{RAMP} digital-to-analog (D/A) circuit.

[00183] Figure 36 depicts an example embodiment of a variable delay capacitor.

[00184] Figure 37 depicts an example graph of the total delay time provided by the programmable delay circuit depicted in Figures 30A-C as a function of the binary weighted programmable capacitor array.

[00185] Figure 38A depicts an example embodiment of a pseudo-envelope follower power management system that includes a feedback delay compensation circuit in combination with a multi-level charge pump buck converter.

[00186] Figure 38B depicts an example embodiment of a pseudo-envelope follower power management system that includes a feedback delay compensation circuit in combination with a buck converter.

[00187] Figure 39A depicts a block diagram of an embodiment of the feedback delay compensation circuit of Figure 38A and Figure 38B.

[00188] Figure 39B depicts another embodiment of the feedback delay compensation circuit of Figure 38A and Figure 38B.

[00189] Figure 40A depicts an embodiment of a pseudo-envelope tracking modulated power supply system depicted in Figures 40B-C.

[00190] Figure 40B depicts an embodiment of a switch mode power supply controller of the power management systems depicted in Figures 40A, Figures 40C-E and Figures 46A-B and Figures 46E-H.

[00191] Figure 40C depicts an embodiment of a parallel amplifier circuit of a power management system.

[00192] Figure 40D depicts an embodiment of a parallel amplifier circuit of a power management system.

[00193] Figure 40E depicts an embodiment of a parallel amplifier circuit of a power management system.

[00194] Figure 41 depicts an equivalent circuit of the pseudo-envelope follower power management system configured to operate in a low power modulation mode.

[00195] Figure 42 depicts the pseudo-envelop follower power management system configured to operate in the low power modulation mode.

[00196] Figures 43A-B depict a method for configuring a power management system to operate in a high power modulation mode.

[00197] Figure 44A-B depict a method for configuring a power management system to operate in a medium power modulation mode.

[00198] Figure 45 depicts a method for configuring a power management system to operate in a low power modulation mode.

[00199] Figure 46A depicts an embodiment of a system for generating a pseudo-envelope and average power tracking modulated power supply voltage, depicted in Figure 40B and Figure 46B.

[00200] Figure 46B depicts an embodiment of a parallel amplifier circuit to generate a pseudo-envelope an average power tracking modulated power supply, depicted in Figure 40B and Figure 46C.

[00201] Figure 46C depicts an embodiment of a parallel amplifier adapted to provide a modulation mode feedback signal.

[00202] Figure 46D depicts an embodiment of an offset voltage loop circuit adapted to regulate a switch mode power supply converter operating in various average power tracking modulation modes of operation.

[00203] Figure 40E depicts an embodiment of a parallel amplifier circuit of a power management system.

[00204] Figure 40F depicts an embodiment of a parallel amplifier circuit of a power management system.

[00205] Figure 40G depicts an embodiment of a parallel amplifier circuit of a power management system.

[00206] Figure 40H depicts an embodiment of a parallel amplifier circuit of a power management system.

[00207] Figure 47 depicts an embodiment of a method for determining a power level modulation mode in which to operate a power management system prior to commencement of a data transmission.

[00208] Figure 48A-B depict an embodiment of a method for configuring a power management system to operate in a high power modulation mode during a data transmission.

[00209] Figure 49A-B depict an embodiment of a method for configuring a power management system to operate in a medium power modulation mode during a data transmission.

[00210] Figure 50A-B depict an embodiment of a method for configuring a power management system to operate in a medium power average power tracking modulation mode during a data transmission.

[00211] Figure 51 depicts an embodiment a low power average power tracking modulation mode during a data transmission.

[00212] Figues 52A-D depict embodiments of a parallel amplifier having a segmented output stage, where each segment receives a different supply voltage. Figures 53A-B repectively depict embodiments of a charge pump having two outputs and three outputs.

[00213] Figure 54 depicts a number of iso-gain contours in relationship to two dynamic ranges of drive level for the modulated fradio frequency input signal.

[00214] Figure 55 depicts an embodiment of an envelope tracking modulated power supply with power control loop compensation system.

[00215] Figure 56 depicts an embodiment of a digital baseband circuir of the envelope tracking modulated power supply with power control loop compensation system.

[00216] Figure 57A depicts a noise corruption model for a digital baseband circuit during calibration of a number of iso-gain contours of the radio frequency power amplifier.

[00217] Figures 58A-D depict a method for compensating generation of a modulated power supply voltage in response to a change in a drive level of a modulated radio frequency input signal provided to a radio frequency power amplifier inorder to maintain a linear gain.

[00218] Figure 59 depicts an embodiment of an average frequency control system.

[00219] Figure 61 depicts a timing diagram associated with controlling the switching frequency of a switch mode power supply converter with the average frequency control sytem of Figures 59.

[00220] Figure 62 depicts a depicts an embodiment of a power supply selection system.

[00221] Figure 63 depicts an embodiments of a supply switching circuit 3100.

Detailed Description

The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the disclosure and illustrate the best mode of practicing the disclosure. Upon reading the following description in light of the accompanying drawings, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[00222] Embodiments disclosed in the detailed description relate to a pseudo-envelope follower power management system including a parallel amplifier and a switch mode power supply converter cooperatively coupled to generate a power supply voltage at a power supply output coupled to a linear radio frequency power amplifier. The parallel amplifier output is in communication with the power

amplifier supply output. The parallel amplifier governs operation of the switch mode power supply converter and regulates the power amplifier supply voltage base on a V_{RAMP} signal. The parallel amplifier circuit includes an linear regular to provide an output current to regulate the power supply output when the parallel amplifier and switcher mode power supply converter are disabled in a low power modulation mode.

[00223] Embodiments disclosed in the detailed description relate to a pseudo-envelope follower power management system including a parallel amplifier and a switch mode power supply converter cooperatively coupled to generate a power supply voltage at a power supply output coupled to a linear radio frequency power amplifier. The parallel amplifier output is in communication with the power amplifier supply output. The parallel amplifier governs operation of the switch mode power supply converter and regulates the modulated power supply voltage base on a V_{RAMP} signal. The parallel amplifier circuit includes a linear regular to provide an output current to regulate the power supply output when the parallel amplifier and switcher mode power supply converter are disabled in a low power modulation mode.

[00224] As another embodiment, the open loop assist current circuit may generate an open loop assist current based on a target voltage for a power amplifier supply voltage, (V_{RAMP}), and an estimate of a switching voltage generated by a switch mode power supply to reduce a parallel amplifier output current generated by a parallel amplifier configured to regulate a power amplifier supply voltage at the power amplifier supply output. The estimate of the switching voltage generated by the switch mode power supply may be either a scaled switching voltage or an switching voltage output estimate. An estimate of a load current of an RF power amplifier is generated based on a difference between the V_{RAMP} signal and a minimum power amplifier turn on a voltage parameter. An estimate of a bypass capacitor current is generated based on a product of an estimated bypass capacitor capacitance parameter and a derivative of a V_{RAMP} signal. An estimate of a power inductor current is generated based on an estimated power inductor inductance parameter, the

estimate of the switching voltage, and the V_{RAMP} signal. An estimated power inductor voltage is calculated by subtracting the V_{RAMP} signal from the estimate of the switching voltage. The estimated power inductor voltage is integrated and scaled by a reciprocal of the estimated power inductor inductance parameter to generate the estimate of the power inductor current. A summing circuit subtracts the estimate of a bypass capacitor current and the estimate of a power inductor current from the estimate of a load current of an RF power amplifier to generate an estimate of an open loop assist current. A controlled current source generates an open loop assist current based on the estimate of an open loop assist current. The open loop assist current is provided and /or applied to a power amplifier supply output.

[00225] As another embodiment, examples of circuits, systems, and methods are described for an open loop assist circuit to generate an open loop assist current that assists a parallel amplifier circuit to regulate a radio frequency power amplifier supply voltage. The radio frequency power amplifier supply voltage may be a modulated power supply voltage that substantially tracks an envelope of a radio frequency signal to be generated by a radio frequency power amplifier. The open loop assist current may be generated based on an indication of a switching voltage generated by a switch mode power supply and a target voltage for a power amplifier supply voltage. The target voltage may be a V_{RAMP} signal. The indication of a switching voltage may be an estimate of a future value of the switching voltage that is temporally related to an output current by the parallel amplifier based on the target voltage.

[00226] A parallel amplifier output impedance compensation circuit is configured to generate a compensated V_{RAMP} signal based on an estimate of a parallel amplifier output current provided by a parallel amplifier to regulate a power amplifier output voltage at a power amplifier supply output, an estimate of a bypass capacitor current provided by a bypass capacitor coupled between the power amplifier supply output and ground, and a V_{RAMP} signal. As an example, the parallel amplifier output impedance compensation circuit generates an estimate of a bypass capacitor current provided by a bypass capacitor coupled

between a power amplifier supply output and ground based on a derivative of a V_{RAMP} signal used to set a target voltage for a power amplifier supply voltage and an estimate of a capacitance of the bypass capacitor. The estimate of the bypass capacitor current is combined with an estimate of a parallel amplifier output current provided by a parallel amplifier to regulate a power amplifier output voltage at the power amplifier supply output to create a dynamic current. The derivative of the dynamic current is scaled by a parallel amplifier inductance estimate parameter generating a power amplifier supply ripple voltage estimate. A V_{RAMP} signal is filtered by a frequency pre-distortion circuit to generate a peaked V_{RAMP} signal in order to compensate for a roll off of a modulation frequency response of the parallel amplifier.

[00227] As another embodiment, a system and method provides a compensated V_{RAMP} signal to a parallel amplifier to compensate for the non-ideal output impedance of the parallel amplifier, where the parallel amplifier regulates a power amplifier supply voltage. The compensated V_{RAMP} signal is generated based on a peaked V_{RAMP} signal and a power amplifier supply ripple voltage estimate. The power amplifier supply ripple voltage estimate is generated based on a product of an inductive characteristic of the parallel amplifier output impedance and a derivative of a dynamic current, where the dynamic current is the sum of a parallel amplifier output current estimate and a bypass capacitor current estimate. The bypass capacitor is coupled between the power amplifier supply output and ground. A V_{RAMP} signal is filtered to generate the peaked V_{RAMP} signal to compensate for a roll off of a modulation frequency response of the parallel amplifier.

[00228] As another embodiment, a system and method for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output is provided. An offset voltage control circuit controls an offset voltage across a coupling circuit that is between the power amplifier supply output and the parallel amplifier circuit output. A summing circuit subtracts a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal.

An integrator circuit integrates the offset voltage error signal to generate an offset voltage feedback signal, which is provided to a switch mode power supply converter to regulate the offset voltage across the coupling circuit. The integrator circuit may be an integrator with zero compensation. The offset voltage control circuit may be configured to pre-charge the coupling circuit for a pre-determined time period prior to a data transmission.

[00229] As another embodiment, a system and method for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output is provided. An offset voltage control circuit controls an offset voltage across a coupling circuit that is between the power amplifier supply output and the parallel amplifier circuit output. A summing circuit subtracts a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal. An error gain circuit scales the offset voltage error signal by an error gain value to generate an offset voltage feedback signal, which is provided to a switch mode power supply converter to regulate the offset voltage across the coupling circuit. The offset voltage control circuit may be configured to pre-charge the coupling circuit for a pre-determined time period prior to a data transmission.

[00230] As another embodiment, a system and method for automatically pre-charging an offset voltage across a coupling device coupled between a power amplifier supply output and a parallel amplifier circuit output is provided. A summing circuit generates an offset voltage error signal based on an offset voltage and a target offset voltage. An integrator having a normal mode of operation and a pre-charge mode of operation generates an offset voltage feedback signal based on the offset voltage error signal, which is provided to a switch mode power supply converter to regulate the offset voltage. Prior to commencement of a data transmission, a control circuit determines whether to operate the integrator in either the pre-charge mode of operation for a pre-determined time period or the normal mode of operation based on a magnitude of the offset voltage error signal. When the V_{RAMP} signal is not modulated, the integrator may operate in the pre-charge mode of operation.

[00231] As another embodiment, a pseudo-envelope follower power management system includes a feedback delay compensation circuit that generates a feedback delay compensation signal based on the slope of a V_{RAMP} signal to provide an early indication of a change in a target voltage of the power amplifier supply voltage. A switcher control circuit of a switch mode power supply converter uses the feedback delay compensation signal to compensate for a delay in generation of a feedback signal by a parallel amplifier circuit that regulates the power amplifier supply voltage. The switcher control circuit generates a feedback delay compensated feedback signal based on the feedback signal and the feedback delay compensation signal. The switcher control circuit governs generation of a switching voltage based on the feedback delay compensated feedback signal. A time constant of a high pass filter is adjusted to set the aggressiveness of the feedback delay compensation circuit.

[00232] As another embodiment, the parallel amplifier output impedance compensation circuit generates a compensated V_{RAMP} signal based on a combination of a pre-distorted V_{RAMP} signal and a difference between the V_{RAMP} signal and a switching voltage output estimate, where the switching voltage output estimate may be temporally aligned with the V_{RAMP} signal by programmable delay circuitry. The parallel amplifier uses the compensated V_{RAMP} signal to regulate a power amplifier supply voltage.

[00233] The switch mode power supply converter generates a switching voltage output estimate. The parallel amplifier output impedance compensation circuit generates an expected difference signal based on a difference between a V_{RAMP} signal and the switching voltage output estimate. The parallel amplifier output impedance compensation circuit high pass filters and scales the expected difference signal to generate a high frequency ripple compensation signal based on a band of operation in which a communication device is assigned to operate. A pre-distortion filter circuit filters a V_{RAMP} signal to generate a pre-filtered V_{RAMP} signal in order to equalize a frequency response between a power amplifier supply output and an input configured to receive the V_{RAMP} signal based on a wideband modulation associated with a mode of operation of a communication

device. The parallel amplifier output impedance compensation circuit combines the pre-filtered V_{RAMP} signal and the high frequency ripple compensation signal to generate a compensated V_{RAMP} signal.

[00234] As another embodiment, a system and method for compensating for the non-ideal output impedance of a parallel amplifier in a pseudo-envelope follower power management system generates a compensated V_{RAMP} signal. The parallel amplifier regulates a power amplifier supply voltage based on the compensated V_{RAMP} signal. A difference between a V_{RAMP} signal and an estimated switching voltage signal generated by a switch mode power supply converter are high pass filtered and scaled with a scaling factor to generate an estimated high frequency ripple signal. A pre-distortion filter generates a pre-distorted V_{RAMP} signal that is combined with the estimated high frequency ripple signal to form the compensated V_{RAMP} signal. The frequency response of the pre-distortion filter is adjusted to equalize a frequency response of the pseudo-envelope follower power management system. The scaling factor may be generated based on a band of operation a communication device is assigned to use in a communication network.

[00235] As another embodiment, an operational amplifier includes a first push-pull output stage, a second push-pull output stage having a first programmable transconductance, and a third push-pull output stage having a second programmable transconductance. The first push-pull output stage generates an operational amplifier output current. The second push-pull output stage includes a first array of mirrored transistor elements arranged to generate an output load current based on the operational amplifier output current. The second push-pull output stage transconductance is programmed by selectively controlling the operational state of mirrored transistor elements in the first array of mirrored transistor elements. The third push-pull output stage includes a second array of mirrored transistor elements arranged to generate a sensed output current that is fractionally related to the output load current by a sense scaling factor. The operational amplifier further includes an operational amplifier output isolation circuit to provide a feedback signal based an operational amplifier output current.

[00236] As another embodiment, a system and method for minimizing jitter of a programmable delay of a programmable delay circuit is provided. The programmable delay is provided by controlling a charge and discharge time of a variable capacitor. A first transistor charges the variable capacitor with a first bias current to provide a charging delay period. A second transistor charges the variable capacitor with a first bias current to provide a discharging delay period. To prevent jitter due to random charge building up on the source of the first transistor and the second transistor while they are in a non-conducting mode, a third transistor pulls the source of the first transistor to a first known voltage while the first transistor is off. A fourth transistor pulls the source of the second transistor to a second known voltage while the second transistor is off.

[00237] As another embodiment, a method and system for delaying a digital signal by a programmable delay period that is substantially insensitive to variations of a supply voltage is provided. A programmable delay circuit delays the digital signal by a programmable delay period. The programmable delay circuit delays the digital signal by controlling the propagation delay of the digital signal through a variable delay circuit. The propagation delay is created by charging and discharging a variable capacitor with a capacitor current that is proportional to the supply voltage of the programmable delay circuit. An output buffer changes a logic state of an output buffer output based on a voltage developed on the variable capacitor and input logic threshold voltages of the output buffer. The sensitivity of the input logic threshold voltages to the supply voltage is substantially offset by the sensitive of the capacitor current to the supply voltage.

[00238] As another embodiment, a system and method for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output is provided. An offset voltage control circuit controls an offset voltage across a coupling circuit that is between the power amplifier supply output and the parallel amplifier circuit output. A summing circuit subtracts a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal.

An integrator circuit integrates the offset voltage error signal to generate an offset voltage feedback signal, which is provided to a switch mode power supply converter to regulate the offset voltage across the coupling circuit. The integrator circuit may be an integrator with zero compensation. The offset voltage control circuit may be configured to pre-charge the coupling circuit for a pre-determined time period prior to a data transmission.

[00239] As another embodiment, an operational amplifier includes a first push-pull output stage, a second push-pull output stage having a first programmable transconductance, and a third push-pull output stage having a second programmable transconductance. The first push-pull output stage generates an operational amplifier output current. The second push-pull output stage includes a first array of mirrored transistor elements arranged to generate an output load current based on the operational amplifier output current. The second push-pull output stage transconductance is programmed by selectively controlling the operational state of mirrored transistor elements in the first array of mirrored transistor elements. The third push-pull output stage includes a second array of mirrored transistor elements arranged to generate a sensed output current that is fractionally related to the output load current by a sense scaling factor. The operational amplifier further includes an operational amplifier output isolation circuit to provide a feedback signal based an operational amplifier output current.

[00240] As another embodiment, a rechargeable parallel amplifier includes a charge storage capacitor having a charge storage capacitor voltage, a NFET transistor configured to charge the charge storage capacitor as a function of the parallel amplifier output voltage, the charge storage capacitor voltage, and the minimum NFET headroom voltage to generate a parallel amplifier output current, and a first PFET transistor configured to discharge the charge storage capacitor function of the parallel amplifier output voltage, the charge storage capacitor voltage, and the minimum PFET headroom voltage to generate the parallel amplifier output current.

[00241] As another embodiment, a parallel amplifier includes a parallel amplifier output, a charge storage capacitor, a first PFET transistor and a first

NFET transistor. The first NFET transistor charges the charge storage capacitor from the parallel amplifier output voltage when a sum of the parallel amplifier supply voltage plus a NFET headroom voltage is greater than the charge storage voltage of the charge storage capacitor to generate a parallel amplifier output current. The first PFET transistor discharges the charge storage capacitor when a sum of the parallel amplifier output voltage and a PFET headroom voltage is less than a charge storage voltage of the charge storage capacitor to generate the parallel amplifier output current.

[00242] As another embodiment, a rechargeable parallel amplifier includes an output stage having a first transistor configured to charge a charge storage capacitor from a power amplifier output supply as a function of a power amplifier supply voltage, a charge storage capacitor voltage of the charge storage capacitor, and the minimum PFET headroom voltage and a second transistor configured to generate a parallel amplifier output current from the charge storage capacitor as a function of the parallel amplifier output voltage, the charge storage capacitor voltage, and a minimum PFET headroom voltage.

[00243] As another embodiment, the parallel amplifier is configured to regulate a power amplifier supply voltage. The parallel amplifier includes a parallel amplifier output, a charge storage capacitor, a first PFET transistor and a first NFET transistor. The first NFET charges the charge storage capacitor from the power amplifier supply output when the power amplifier supply voltage is at least greater than a sum of the minimum NFET headroom voltage and a charge storage capacitor voltage of the charge storage capacitor. The first PFET discharges a charge storage capacitor when a sum of the parallel amplifier output voltage and a PFET headroom voltage is less than the charge storage voltage of the charge storage capacitor to generate a parallel amplifier output current. In addition, parallel amplifier includes a second PFET, a second NFET, an output control circuit, and a front end circuit having a first amplifier and a second amplifier.

[00244] As another embodiment, a bias reference and mirror circuit configured to generate a bias reference current that tracks a change in a propagation delay

between a switcher control circuit and a switching voltage output of a switch mode power supply converter as a function of temperature such that the programmable delay period substantially tracks a change in propagation delay between a switcher control circuit and a switching supply voltage output of a switching mode power supply converter. As another embodiment, thee programmable delay circuit is configured to maintain time alignment between the switching voltage at the switching voltage output of the switching power supply converter and the predicted / future value provided to an open loop high frequency ripple compensation circuit. A bias reference and mirror circuit configured to generate a bias reference current that tracks a change in a propagation delay between a switcher control circuit and a switching voltage output of a switch mode power supply converter as a function of temperature, voltage, and/or a combination thereof. There are two approaches.

[00245] As another embodiment, a voltage reference circuit that sets a reference voltage may include a compensation current source that adjust a current through a current setting resistor of a voltage divider circuit with respect to temperature, supply voltage, or a combination thereof. The reference voltage controls a bias reference current generated across a resistor, which is mirrored to create a first bias current and a second bias current. A variable capacitor is charged and discharged with the figure bias current and the second bias current, respectively, to delay propagation of an input signal through the programmable delay circuit.

[00246] As another embodiment, the voltage reference circuit is a voltage divider circuit and sets a reference voltage across the current setting resistor in the bias reference and mirror circuit. A compensation current source is coupled to the current mirror circuit to sink a portion of the reference bias current as a function of temperature, supply voltage, and/or a combination thereof.

[00247] As another embodiment, the compensation current source is configured to adjust the first bias current and the second bias current such that the propagation delay through the programmable delay circuit changes to track the change in propagation delay between a switch control circuit and a switching

voltage output of a switch mode power supply converter as a function of temperature and a function of a supply voltage. In some embodiments, the compensation current source may be configured to also take into consideration a change in the propagation delay between the output of the output buffer and the application of the high frequency ripple compensation current generated by the open loop high frequency ripple compensation circuit

[00248] Embodiments disclosed herein relate to a pseudo-envelope follower power management system including a parallel amplifier and a switch mode power supply converter cooperatively coupled to generate a power supply voltage at a power supply output coupled to a linear radio frequency power amplifier. The parallel amplifier output is in communication with the power amplifier supply output. The parallel amplifier governs operation of the switch mode power supply converter and regulates the power amplifier supply voltage base on a V_{RAMP} signal. The parallel amplifier circuit includes an open loop high frequency compensation assist circuit that generates a high frequency ripple compensation current based on an estimate of the high frequency ripple currents contained in a ripple current of the power inductor. The high frequency ripple compensation current is injected into the parallel amplifier circuit output to cancel out high frequency ripple currents at the power amplifier supply output.

[00249] A first embodiment of the pseudo-envelope follower power management system with high frequency ripple compensation includes a switch mode power supply converter and an open loop high frequency ripple compensation assist circuit. For example, the switch mode power supply converter may be configured to operate as a buck converter. As another example, the switch mode power supply converter may be configured to operate as a multi-level charge pump buck converter. The switch mode power supply may generate a switching output voltage and a switching voltage output estimate. The switching voltage output estimate may provide an early indication of a future voltage level of the switching output voltage. For example, in some embodiments, the switch mode power supply converter may also include programmable delay circuitry, a switcher control circuit, and a buffer scalar. The

switcher control circuit may generate a digital switching voltage output signal that represents a state of the switcher control circuit used to control generation of the switching output voltage by the switch mode power supply converter. The programmable delay circuitry may receive the digital switching voltage output signal, and delay the digital switching voltage output signal by a programmable delay period to generate a delayed digital switching voltage output signal. The buffer scalar is configured to receive the delayed digital switching voltage output signal, and generate the switching voltage output estimate based on the delayed digital switching voltage output signal and a buffer scalar.

[00250] The open loop high frequency ripple compensation assist circuit is configured to receive the switching voltage output estimate and a V_{RAMP} signal. Based on the switching voltage output estimate and the V_{RAMP} signal, the open loop high frequency ripple compensation assist circuit generates a high frequency ripple compensation current. The open loop high frequency ripple compensation assist circuit applies the high frequency ripple compensation current to a power amplifier supply output to reduce high frequency ripple current at the power amplifier supply output. The power amplifier supply output is configured to power a linear radio frequency power amplifier. The high frequency ripple compensation current is generated in a frequency band located substantially near a transmit to receive duplex offset for a band of operation in a communication network, where the frequency band of the high frequency ripple compensation current has a bandwidth substantially equal to a bandwidth of a receiver channel frequency band for the band of operation.

[00251] In some embodiments, the switch mode power supply converter further includes programmable delay circuitry configured to delay generation of the switching voltage output estimate by a programmable delay period. The programmable delay period may be configured to temporally align the switching voltage output estimate and the V_{RAMP} signal to position a notch in a ripple rejection response of the power amplifier supply output near the transmit to receive duplex offset for the band of operation. In addition, the open loop high frequency ripple compensation assist circuit may generate a scaled high

frequency ripple compensation current estimate based on the high frequency ripple compensation current, which can be used as part of a feedback signal to the switch mode power supply converter. As an example, the switch mode power supply converter may receive a feedback signal, wherein the feedback signal is based on the scaled high frequency ripple compensation current estimate, where the switch mode power supply converter adjusts the switching output voltage based on the feedback signal. In some embodiments, the pseudo-envelope follower power management system with high frequency ripple compensation further includes a parallel amplifier. The parallel amplifier receives the V_{RAMP} signal and a power amplifier supply voltage from the power amplifier supply output. Based on a difference between the V_{RAMP} signal and the power amplifier supply voltage, the parallel amplifier generates a parallel amplifier output current. The parallel amplifier applies the parallel amplifier output current to the power amplifier supply output to control the power amplifier supply voltage. In addition, the parallel amplifier may generate a scaled parallel amplifier output current estimate based on the parallel amplifier output current. The scaled parallel amplifier output current estimate may be combined with the scaled high frequency ripple compensation current estimate to create the feedback signal provided to the switch mode power supply converter.

[00252] Some embodiments of the open loop high frequency ripple compensation assist circuit may include a filter network having a first node and a second node, a feedback network having a first node and a second node, and an operational amplifier including a non-inverting input, an inverting input, and an operational amplifier output. The first node of the filter network may be configured to receive the switching voltage output estimate. The second node of the filter network may be in communication with the inverting input of the operational amplifier. The first node of the feedback network may be in communication with the second node of the filter network and the inverting input of the operational amplifier. In addition, the second node of the feedback network may be in communication with the operational amplifier output. The operational amplifier may be configured to generate the high frequency ripple

compensation current. The operational amplifier may also be configured to generate a scaled high frequency ripple compensation current estimate as a function of the high frequency ripple compensation current. The operational amplifier may include a first push-pull output stage in communication with the operational amplifier output, where the first push-pull output stage generates an operational amplifier output current. A bias capacitor having a bias capacitance and a bias resistor may be arranged in series between the operational amplifier output and a reference voltage. For example, the reference voltage may be ground. The first push-pull output stage may have a first stage transconductance. The bias capacitance may be configured such that the first stage transconductance of the first push-pull output stage is substantially equal to a transconductance of the bias resistor in a frequency band located substantially near a transmit to receive duplex offset for a band of operation in a communication network. The open loop high frequency ripple compensation assist circuit may also include an operational amplifier output isolation circuit including a high impedance input in communication with the operational amplifier output and an isolated feedback node in communication with the second node of the feedback network. The operational amplifier may also include a second push-pull output stage configured to generate the high frequency ripple compensation current, where the high frequency ripple compensation current is mirrored to the operational amplifier output current. The second push-pull output stage may include a programmable second output stage transconductance. The programmable second output stage transconductance second output stage transconductance may be a substantially linear function of a programmable transconductance parameter. The open loop high frequency ripple compensation assist circuit may adjust a magnitude of the high frequency ripple compensation current based on the programmable second output stage transconductance. The operational amplifier may also include a third push-pull output stage configured to generate the scaled high frequency ripple compensation current estimate as a function of the high frequency ripple compensation current based on a sense scaling factor.

[00253] The filter network may be associated with a first corner frequency of a filter response of the open loop high frequency ripple compensation assist circuit. The feedback network may be associated with a second corner frequency of the frequency response of the open loop high frequency ripple compensation assist circuit. In some cases, the first corner frequency has a programmable range between 3MHz and 11.5MHz and the second corner frequency has a programmable range between 3MHz and 11.5MHz. In other cases, the first corner frequency is substantially equal to 6 MHz, and the second corner frequency is substantially equal to 6 MHz.

[00254] Another example embodiment includes a method for reducing high frequency ripple currents at a power amplifier supply output. The method may include a first step of generating a switching output voltage and a switching voltage output estimate with a switch mode power supply converter, where the switching voltage output estimate provides an early indication of a future voltage level of the switching output voltage. The method may include the step of receiving the switching voltage output estimate and a V_{RAMP} signal at an open loop high frequency ripple compensation assist circuit. The method may include the step of generating a high frequency ripple compensation current based on the switching voltage output estimate and the V_{RAMP} signal. The method may include the step of applying the high frequency ripple compensation current to a power amplifier supply output to reduce high frequency ripple currents at the power amplifier supply output. In some embodiments, the generation of the high frequency ripple compensation current based on the switching voltage output estimate and the V_{RAMP} signal may include generating the high frequency ripple compensation current within in a frequency band located substantially near a transmit to receive duplex offset for a band of operation in a communication network. In addition, the frequency band of the high frequency ripple compensation current may have a bandwidth substantially equal to a bandwidth of a receiver channel frequency band for the band of operation. In some embodiments, generation of the switching voltage output estimate may include delaying generation of the switching voltage output estimate by a programmable

delay period to temporally align the switching voltage output estimate and the V_{RAMP} signal to position a notch in a ripple rejection response of the power amplifier supply output near the transmit to receive duplex offset for the band of operation. In addition, the method may further include a step for generating a scaled high frequency ripple compensation current estimate based on the high frequency ripple compensation current. Based on the scaled high frequency ripple compensation current estimate, the method may form a feedback signal, which is provided to the switch mode power supply converter. The switch mode power supply converter may adjust the switching output voltage based on the feedback signal. In some embodiments, the switch mode power supply converter is configured to be a buck converter. Alternatively, in other embodiments, the switch mode power supply converter is configured to be a multi-level charge pump buck converter.

[00255] Embodiments disclosed herein further relate to a pseudo-envelope follower power management system used to manage the power delivered to a linear radio frequency power amplifier. One example embodiment of the pseudo-envelope follower power management system may include a switch mode power supply converter and a parallel amplifier cooperatively coupled to provide a linear radio frequency power amplifier supply to a linear radio frequency power amplifier. The pseudo-envelope follower power management system may include a charge pump configured to power the parallel amplifier. The charge pump may generate a plurality of output voltage levels. The charge pump may be either a boost charge pump or a boost/buck charge pump. The pseudo-envelope follower power management system may include an offset voltage control circuit configured to provide feedback to the switch mode power supply converter to regulate an offset voltage developed across a coupling device that couples the output of the parallel amplifier to the linear radio frequency power amplifier supply.

[00256] Another example embodiment of a power management system for a linear radio frequency power amplifier includes a switch mode power supply converter and a parallel amplifier operatively coupled to generate a linear radio

frequency power amplifier supply output for a linear radio frequency power amplifier of a radio frequency device. The switch mode power supply converter may be configured to generate a plurality of switching voltage levels on a switching voltage output. The switching voltage output of the switch mode power supply converter may be coupled via a power inductor to the linear radio frequency power amplifier supply output. A bypass capacitor may be coupled between the linear radio frequency power amplifier supply output and ground such that the power inductor and bypass capacitor form a low pass filter for the switch mode power supply converter. The parallel amplifier may include a parallel amplifier output coupled, via a coupling device, to the linear radio frequency power amplifier supply output. As an example, the coupling device may be a coupling capacitor. The power management system may further include a charge pump configured to provide a charge pump parallel amplifier power supply output. The charge pump may include a first flying capacitor, a second flying capacitor, a plurality of switches operably coupled to form the charge pump parallel amplifier power supply output. The charge pump may be configured to selectively generate various output voltage levels, derived from a supply voltage, on the charge pump parallel amplifier power supply output. In addition, the charge pump parallel amplifier power supply output may be configured to provide an operational power supply voltage to the parallel amplifier.

[00257] Another example embodiment of a pseudo-envelope follower power management system may include a multi-level charge pump buck converter and a parallel amplifier configured to operate in tandem to generate a power amplifier supply voltage output for a linear radio frequency power amplifier. The multi-level charge pump buck converter may include a supply input configured to receive a direct current (DC) voltage, and a switching voltage output. The switching voltage output is coupled to the power amplifier supply voltage output by a power inductor, where the power inductor couples to a bypass capacitor to form an output filter for the switching voltage output of the multi-level charge pump buck converter. The parallel amplifier may include a supply input

configured to receive the direct current (DC) voltage, an amplifier output, a first control input configured to receive a V_{RAMP} signal, and a second control input configured to receive the power amplifier supply voltage. The amplifier output may be coupled to the power amplifier supply voltage by a coupling circuit. In some embodiments of the pseudo-envelope follower system, the coupling circuit may be an offset capacitor. In other embodiments of the pseudo-envelope follower system, the coupling circuit may be a wire trace such that the offset voltage between the amplifier output and the power amplifier supply voltage is zero volts.

[00258] In addition, the multi-level charge pump buck converter may generate a feed forward control signal configured to provide an indication of the output state of the switching voltage output to the parallel amplifier. In some embodiments, the switching voltage output is provided as the feed forward control signal. In other embodiments, the feed forward control signal is generated by a switcher control circuit and provides an indication of the switching voltage output based on the state of the switcher control circuit. The parallel amplifier may include a parallel amplifier output current estimate signal that provides an estimate of the output current of the parallel amplifier. In some embodiments of the pseudo-envelope follower system, the parallel amplifier may also generate a threshold offset signal. The threshold offset signal may be configured to estimate the magnitude of the offset voltage appearing across the coupling circuit.

[00259] The multi-level buck converter may include a supply input configured to receive a direct current (DC) voltage, a switching voltage output coupled to a power inductor, a switcher control circuit, a multi-level charge pump circuit having a control input, a charge pump supply input configured to receive the DC voltage, a series switch having a first switch terminal, a second switch terminal, and a series control terminal and a shunt switch having a first switch terminal, a second switch terminal, and a shunt control terminal. The first terminal of the series switch may be coupled to the supply input of the multi-level buck converter. The second terminal of the series switch may be coupled to the first terminal of the

series switch to form a switching voltage output. The second terminal of the series switch may be coupled to ground. The boost charge pump circuit may include a charge pump control input, a charge pump supply input coupled to the supply input of the multi-level buck converter, and a charge pump output coupled to the supply input of the multi-level buck converter. The boost charge pump includes a plurality of switches and two flying capacitors that provide for three modes of operation. In a charging mode of operation, the flying capacitors are coupled in series between the charge pump supply input and ground, where the flying capacitors are switchably disconnected from the charge pump output. In a first boost mode of operation, the flying capacitors are arranged in parallel between the charge pump output and the charge pump supply input to generate a 3/2 x the DC voltage output at the charge pump output. In a second boost mode of operation, the flying capacitors are arranged in series between the charge pump output and the charge pump supply input to generate a 2 x the DC voltage output at the charge pump output. The multi-level buck converter may include four modes of operation. In a first mode of operation, the series switch is open, the boost charge pump is in the charging mode of operation, and the shunt switch is closed to generate zero volts at the switching voltage output. In a second mode of operation, the series switch is closed, the boost charge pump is in the charging mode of operation, and the shunt switch is open to generate the DC voltage output at the switching voltage output. In a third mode of operation, both the series switch and the shunt switch are open and the boost charge pump is in the first boost mode of operation to generate a 3/2 x the DC voltage output at the switching mode output. In a fourth mode of operation, both the series switch and the shunt switch are open and the boost charge pump is in the second boost mode of operation to generate a 2 x the DC voltage output at the switching mode output.

[00260] Figures 1A and 2A depict an example embodiment of pseudo-envelope follower power management system 10A including a multi-level charge pump buck converter 12, a parallel amplifier circuit 14, a power inductor 16, a coupling circuit 18, and a bypass capacitor 19. The bypass capacitor 19 has a

bypass capacitor capacitance, C_{BYPASS}. The multi-level charge pump buck converter 12 and the parallel amplifier circuit 14 may be configured to operate in tandem to generate a power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28 of the pseudo-envelope follower power management system 10A for a linear radio frequency power amplifier 22. The power amplifier supply output 28 provides an output current, I_{OUT}, to the linear radio frequency power amplifier 22. The linear radio frequency power amplifier 22 may include a radio frequency power amplifier input configured to receive a modulated radio frequency input signal having an input power P_{IN}. The linear radio freuquency power amplifier 22 may further include a radio frequency power amplifier output coupled to an output load, Z_{LOAD}. The radio frequency power amplifier 22 may generate an amplified modulated radio frequency output signal having an output power P_{OUT} in response to the modulated radio frequency input signal having an input power P_{IN}. As an example, the output load, Z_{LOAD}, may be an antenna. The radio frequency power amplifier output may generate the amplified modulated radio frequency output signal as a function of the modulated radio frequency input signal and the power amplifier supply voltage, V_{CC}. In some embodiments, the power amplifier supply voltage, V_{CC}, may be modulated to substantially follow the signal envelope characteristic of the modulated radio frequency input signal to improve the power efficiency of the pseudo-envelope follower power management system 10A. The modulated radio frequency output signal may be provide to the antenna for transmission. The multi-level charge pump buck converter 12 may include a supply input 24, (V_{BAT}), configured to receive a battery voltage, V_{BAT}, from a battery 20 and a switching voltage output 26 configured to provide a switching voltage, V_{SW}. The switching voltage output 26 may be coupled to the power amplifier supply output 28 by the power inductor 16, where the power inductor 16 couples to a bypass capacitor 19 to form an output filter 29 for the switching voltage output 26 of the multi-level charge pump buck converter 12. The power inductor 16 provides a power inductor current, I_{SW_OUT}, to the power amplifier supply output 28. The parallel amplifier circuit 14 may include a parallel amplifier supply input 30 configured to

receive the battery voltage, V_{BAT}, from the battery 20, a parallel amplifier output 32A, a first control input 34 configured to receive a V_{RAMP} signal, and a second control input configured to receive the power amplifier supply voltage, V_{CC}. The parallel amplifier output 32A of the parallel amplifier circuit 14 may be coupled to the power amplifier supply voltage V_{CC}, by a coupling circuit 18. The parallel amplifier output voltage, V_{PARA_AMP}, is provided by the parallel amplifier circuit 14.

[00261] As an example, the parallel amplifier circuit 14 may generate the parallel amplifier output voltage, V_{PARA_AMP}, based on the difference between the V_{RAMP} signal and the power amplifier supply voltage, V_{CC}. Thus, the V_{RAMP} signal may represent either an analog or digital signal that contains the required supply modulation information for a power amplifier collector of a linear radio frequency power amplifier. Typically, the V_{RAMP} signal is provided to the parallel amplifier circuit 14 as a differential analog signal to provide common mode rejection against any noise or spurs that could appear on this signal. The V_{RAMP} signal may be a time domain signal, $V_{RAMP}(t)$, generated by a transceiver or modem and used to transmit radio-frequency (RF) signals. For example, the V_{RAMP} signal may be generated by a digital baseband processing portion of the transceiver or modem, where the digital V_{RAMP} signal, $V_{RAMP_DIGITAL}$, is digital-to-analog converted to form the V_{RAMP} signal in the analog domain. In some embodiments, the "analog" V_{RAMP} signal is a differential signal. The transceiver or a modem may generate the V_{RAMP} signal based upon a known radio frequency modulation $Amp(t)*\cos(2*pi*f_{RF}*t + Phase(t))$. The V_{RAMP} signal may represent the target voltage for the power amplifier supply voltage, V_{CC}, to be generated at the power amplifier supply output 28 of the pseudo-envelope follower power management system 10A, where the pseudo-envelope follower power management system 10A provides the power amplifier supply voltage, V_{CC}, to the linear radio frequency power amplifier 22. Also the V_{RAMP} signal may be generated from a detector coupled to the radio frequency input power amplifier.

[00262] For example, the parallel amplifier circuit 14 includes a parallel amplifier output 32A that provides a parallel amplifier output voltage, V_{PARA_AMP},

to the coupling circuit 18. The parallel amplifier output 32A sources a parallel amplifier circuit output current, I_{PAWA_OUT}, to the coupling circuit 18. The parallel amplifier circuit 14, depicted in Figure 1A and Figure 1B, may provide a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to the multi-level charge pump buck converter 12 as an estimate of the parallel amplifier circuit output current I_{PAWA_OUT}, of the parallel amplifier circuit 14. Thus, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, represents an estimate of the parallel amplifier circuit output current I_{PAWA_OUT}, provided by the parallel amplifier circuit as a feedback signal to the multi-level charge pump buck converter 12. Based on the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, multi-level charge pump buck converter 12 may be configured to control the switching voltage, V_{SW}, provided at the switching voltage output 26 of the multi-level charge pump buck converter 12.

[00263] In some embodiments of the pseudo-envelope follower power management system 10A, depicted in Figure 1A, and the pseudo-envelope follower power management system 10B, depicted in Figure 1B, the coupling circuit 18 may be an offset capacitor, C_{OFFSET}. An offset voltage, V_{OFFSET}, may be developed across the coupling circuit 18. In other alternative embodiments, the coupling circuit may be a wire trace such that the offset voltage, V_{OFFSET}, between the parallel amplifier output voltage, V_{PARA_AMP}, and the power amplifier supply voltage output, V_{CC}, is zero volts. In still other embodiments, the coupling circuit may be a transformer.

[00264] As an example, a pseudo-envelope follower power management system 10A, depicted in Figure 2A, is an example embodiment of the pseudo-envelope follower power management systems 10, depicted in Figure 1A. Unlike the pseudo-envelope follower power management systems 10, depicted in Figure 1A, the pseudo-envelope follower power management system 10A depicted in Figure 2A includes an embodiment of the multi-level charge pump buck converter 12A and a parallel amplifier circuit 14A having parallel amplifier circuitry 32. The parallel amplifier circuitry 32 includes a parallel amplifier 35 and a parallel amplifier sense circuit 36. The parallel amplifier circuit 14A further

includes a parallel amplifier output impedance compensation circuit 37 configured to receive a $V_{RAMP:}$ signal and provide a compensated V_{RAMP} signal, V_{RAMP_C}, as an input to the parallel amplifier 35. The parallel amplifier circuit 14A further includes a parallel amplifier output impedance compensation circuit 37 configured to receive the V_{RAMP} signal and generate a compensated V_{RAMP} signal, V_{RAMP_C}, as a function of the V_{RAMP} signal. The parallel amplifier 35 generates a parallel amplifier output current, I_{PARA_AMP}, to produce a parallel amplifier output voltage, V_{PARA_AMP}, at the parallel amplifier output 32A based on the difference between the compensated V_{RAMP} signal, V_{RAMP_C} and the power amplifier supply voltage, V_{CC}, generated at power amplifier supply output 28. The parallel amplifier sense circuit 36 generates a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, which is a fractional representation of the parallel amplifier output current, I_{PARA_AMP}, generated by the parallel amplifier 35. Alternatively, in those embodiments of the parallel amplifier circuit 14 that do not include the parallel amplifier output impedance compensation circuit 37, the parallel amplifier 35 generates the parallel amplifier output current, I_{PARA_AMP}, to produce the parallel amplifier output voltage, V_{PARA_AMP}, based on the difference between the V_{RAMP} signal and the power amplifier supply voltage, V_{CC}. The parallel amplifier circuit 14A may further include an open loop assist circuit 39 configured to receive the feed forward control signal 38, $V_{SWITCHER}$, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the V_{RAMP} signal. In response to the feed forward control signal 38, $V_{SWITCHER}$, scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the V_{RAMP} signal, the open loop assist circuit 39 may be configured to generate an open loop assist current, I_{ASSIST}. The open loop assist current, I_{ASSIST}, may be provided to the parallel amplifier output 32A. The parallel amplifier output current, I_{PARA_AMP}, generated by the parallel amplifier 35 and the open loop assist circuit current, I_{ASSIST}, generated by the open loop assist circuit 39 may be combined to form the parallel amplifier circuit output current, I_{PAWA_OUT}, of the parallel amplifier circuit 14A. The parallel amplifier circuit 14A may further include a V_{OFFSET} loop circuit 41, configured to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$.

The threshold offset current 42, $I_{THRESHOLD_OFFSET}$, may be provided from the parallel amplifier circuit 14A as a feedback signal to the multi-level charge pump buck converter 12A. The V_{OFFSET} loop circuit 41 may be configured to provide a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, as an estimate of the magnitude of the offset voltage, V_{OFFSET}, appearing across the coupling circuit 18. In those cases where the coupling circuit is a wire trace such that the offset voltage, V_{OFFSET}, is always zero volts, the parallel amplifier circuit 14A may not provide the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the multi-level charge pump buck converter 12A. An embodiment of the V_{OFFSET} loop circuit 41 is depicted in Figure 8. In addition, another embodiment of the V_{OFFSET} loop circuit 41A, depicted in Figure 18A and Figure 18C, represents an alternative embodiment the V_{OFFSET} loop circuit 41 depicted in Figures 2A, 2B, 8, 18A, and 18C. Moreover, as also described below, an alternative embodiment of a V_{OFFSET} loop circuit 41B, depicted Figure 18B and Figure 18D, represents an alternative embodiment of the V_{OFFSET} loop circuit 41 depicted in Figures 2A, 2B, 8, 18B, and 18D. In addition, another example is the pseudo-envelope follower power management system 10B, depicted in Figure 2B, which is similar to the embodiment of the pseudo-envelope follower power management system 10B, depicted in Figure 1B. The pseudo-envelope follower power management system 10B operationally and functionally similar in form and function to the pseudo-envelope follower power management system 10A, depicted in Figure 2A. However, unlike the pseudo-envelope follower power management system 10A depicted in Figure 2A, the pseudo-envelope follower power management system 10B includes a multi-level charge pump buck converter 12B configured to generate an estimated switching voltage output 38B, V_{SW_EST}, and a parallel amplifier circuit 14B configured to receive the estimated switching voltage output 38B, V_{SW_EST}, instead of the feed forward control signal 38, $V_{SWITCHER}$. Consequentially, as depicted in Figure 2B, the open loop assist circuit 39 of the parallel amplifier circuit 14B in configured to use only the estimated switching voltage output 38B, V_{SW_EST}, instead of the feed forward control signal 38, $V_{SWITCHER}$.

[00265] The generation of the feed forward control signal 38, $V_{SWITCHER}$, depicted in Figure 1A and 2A, will now be explained with reference to Figure 3A. As an example, the multi-level charge pump buck converters 12 and 12A may each be configured to generate a feed forward control signal 38, $V_{SWITCHER}$, to provide an indication of the output state of the switching voltage output 26 to the parallel amplifier circuit 14. As an example, Figure 3A depicts an embodiment of the switcher control circuit 52, depicted in Figure 2A, as a switcher control circuit 52A. In Figure 3A, the feed forward control signal 38, $V_{SWITCHER}$, is provided by a switch 43. The switch 43 may be configured by the $V_{SWITCHER_CONTROL}$ signal to provide either an indication of the switching voltage output, V_{SW}, from the threshold detector and control circuit 132A or a scaled version of the switching voltage output, V_{SW}, from the scalar circuit as the feed forward control signal 38, $V_{SWITCHER}$. The threshold detector and control circuit 132A may generate an estimated switching voltage output 38B, V_{SW_EST}, based on the state of the switcher control circuit 52A, where the estimated switching voltage output 38B, V_{SW_EST}, provides an indication of the switching voltage output, V_{SW}, based on the state of the switcher control circuit 52A. Due to propagation delay within the switcher control circuit 52A, the multi-level charge pump circuit 56 and the switching circuit 58 of the multi-level charge pump buck converter 12A, the indication of the switching voltage output, V_{SW}, based on the state of the switcher control circuit 52A is a feed forward signal that indicates what the voltage level of the switching voltage output, V_{SW}, at the switching voltage output 26 will be based on the state of the switcher control circuit 52A instead of the current voltage level of the switching voltage output, V_{SW}, at the switching voltage output 26. Thus, the estimated switching voltage output 38B, V_{SW_EST}, may provide an early indication what the voltage level of the switching voltage output, V_{SW}, will be in the future instead of the present voltage level of the switching voltage output, V_{SW}, at the switching voltage output 26. In contrast, the scalar circuit may generate a scaled switching voltage output 38A, V_{SW_SCALED}, by scaling the switching voltage output 26, V_{SW}, where the scaled switching voltage output 38A, V_{SW_SCALED}, provides a scaled version of the switching

voltage output, V_{SW}. Thus, the scaled switching voltage output 38A, V_{SW_SCALED}, is a scaled version of the voltage level currently at the switching voltage output 26 instead of a future voltage level. Accordingly, the switch 43 may be configured such that the feed forward control signal 38, $V_{SWITCHER}$, provides either the estimated switching voltage output 38B, V_{SW_EST}, or the scaled switching voltage output 38A, V_{SW_SCALED}, as the feed forward control signal 38, $V_{SWITCHER}$.

[00266] Another embodiment of the pseudo-envelope follower power management system 10B, as depicted in Figure 1B, is described with reference to Figure 3B. As depicted in Figure 1B, the multi-level charge pump buck converter 12B may be configured to provide both a scaled switching voltage output 38A, V_{SW_SCALED}, and an estimated switching voltage output 38B, V_{SW_EST}, to the parallel amplifier circuit 14B. As still another example, the pseudo-envelope follower power management system 10B depicted in Figure 2B may be configured to only provide the estimated switching voltage output 38B, V_{SW_EST}, as a feed forward signal to the parallel amplifier circuit 14B.

[00267] The generation of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, depicted in Figure 1A and 1B will now be described with continuing reference to the embodiment of the parallel amplifier circuit 14A, depicted in Figure 2A, and the embodiment of the parallel amplifier circuit 14B depicted in Figure 2B. Embodiments of the parallel amplifier circuit 14A and the parallel amplifier circuit 14B, depicted in Figures 2A and 2B, may provide the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, where the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, includes a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and a scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}. The scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is a scaled estimate of the parallel amplifier output current, I_{PARA_AMP}, generated by the parallel amplifier sense circuit 36 of the parallel amplifier circuitry 32. In some alternative embodiments, the parallel amplifier 35 may generate the scaled estimate of the parallel amplifier output current, $I_{PARA_AMP_SENSE}$, directly. The scaled open loop assist circuit current estimate, I_{ASSIST_SENSE}, is a scaled estimate of the open loop

assist circuit current, I_{ASSIST}, generated by the open loop assist circuit 39. In other alternative embodiments of the parallel amplifier circuit 14 depicted in Figure 1A and Figure 1B, the parallel amplifier circuit 14 does not include the open loop assist circuit 39. In those embodiments of the parallel amplifier circuit 14 depicted in Figure 1A and Figure 1B that do not include the open loop assist circuit 39, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, may only be based on the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$.

[00268] Returning to Figures 1A and 1B, the pseudo-envelope follower power management systems 10A and 10B may further include a control bus 44 coupled to a controller 50. The control bus 44 may be coupled to a control bus interface 46 of the multi-level charge pump buck converter 12 and the control bus interface 48 of the parallel amplifier circuit 14. The controller 50 may include various logical blocks, modules, and circuits. The controller 50 may be implemented or performed with a processor, a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices. As an example, a combination of computing devices may include a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. The controller may further include or be embodied in hardware and in computer executable instructions that are stored in memory, and may reside, for example, in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, hard disk, a removable disk, a CD-ROM, or any other form of computer readable medium known in the art. An exemplary storage medium may be coupled to the

processor such that a processor can read information from, and write information to, the storage medium. In the alternative, the storage medium or a portion of the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC.

[00269] Figures 2A and 2B depict a pseudo-envelope follower power management system 10A and a pseudo-envelope follower power management system 10B, respectively, that include embodiments of the multi-level charge pump buck converter 12A and the multi-level charge pump buck converter 12B. As depicted in Figures 2A and 2B, some embodiments of the multi-level charge pump buck converter 12 of Figures 1A and 1B may include a frequency locked loop circuit 54, sometimes referred to as an FLL circuit. The frequency locked loop circuit 54 may be configured to interoperate with a switcher control circuit 52, as depicted in Figures 2A and 2B. Alternatively, some embodiments of the multi-level charge pump buck converter 12A and the multi-level charge pump buck converter 12B may disable the frequency locked loop circuit 54 in certain modes of operation. In some alternative embodiments, the multi-level charge pump buck converter 12A may not include the frequency locked loop circuit 54.

[00270] As further depicted in Figures 2A and 2B, some embodiments of the switcher control circuit 52 may be configured to control the operation of the multi-level charge pump circuit 56 and the switching circuit 58 to generate the switching voltage, V_{SW}, on the switching voltage output 26 of the multi-level charge pump buck converter 12A or the multi-level charge pump buck converter 12B, respectively. For example, the switcher control circuit 52 may use a charge pump mode control signal 60 to configure the operation of the multi-level charge pump circuit 56 to provide a charge pump output 64 to the switching circuit 58. Alternatively, the switcher control circuit 52 may generate a series switch control signal 66 to configure the switching circuit 58 to provide the switching voltage, V_{SW}, substantially equal to the DC voltage, V_{BAT}, from the battery 20 via a first switching element coupled between the supply input 24 and the switching voltage output 26. As another example, the switcher control circuit 52 may configure the switching circuit 58 to provide the switching voltage,

V_{SW}, through a second switching element coupled to ground such that the switching voltage, V_{SW}, is substantially equal to ground.

[00271] In addition, the parallel amplifier circuit 14A, depicted in Figure 2A, and the parallel amplifier circuit 14B, depicted in Figure 2B, may be configured to provide the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the switcher control circuit 52 in order to control the operation of the switcher control circuit 52. As discussed in detail below, some embodiments of the switcher control circuit 52 may be configured to receive and use the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and/or a combination thereof to control the operation of the switcher control circuit 52.

[00272] For example, the switcher control circuit 52 may use the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and/or a combination thereof to determine the magnitude of the voltage provided the switching voltage, V_{SW}, from the multi-level charge pump circuit 56.

[00273] Some embodiments of the switcher control circuit 52, depicted in Figure 2A and Figure 2B, may be configured to interoperate with the frequency locked loop circuit 54. As an example, Figure 3A depicts an example embodiment of a switcher control circuit 52A configured to interoperate with an example embodiment of the frequency locked loop circuit 54, which is depicted as frequency locked loop circuit 54A. For the sake of clarity, and not by limitation, the description of the operation of the switcher control circuit 52A and the frequency locked loop circuit 54A will be done with continuing reference to the multi-level charge pump buck converter 12A, depicted in Figure 2A.

[00274] As depicted in Figure 3A, some embodiments of the multi-level charge pump buck converter 12A may include switcher control circuit 52A, an embodiment of the frequency locked loop circuit 54A, (FLL circuit), a multi-level charge pump circuit 56, and the switching circuit 58. The switcher control circuit 52A may be in communication with the frequency locked loop circuit 54A.

The frequency locked loop circuit 54A may be in communication with a clock reference 139. The multi-level charge pump circuit 56 and the switching circuit 58 may be configured to receive the DC voltage, V_{BAT}, from the supply input 24 of the multi-level charge pump buck converter 12A.

[00275] The clock reference 139 may provide a clock reference signal 139A to the frequency locked loop circuit 54A. In addition, the switcher control circuit 52A may provide a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, to the frequency locked loop circuit 54A. The logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, is discussed relative to the logic circuit 148A of Figure 4A. In some embodiments of the multi-level charge pump buck converter 12 of Figures 1A and 1B, the multi-level charge pump buck converter 12 may not include the frequency locked loop circuit 54 and a clock reference 139, as depicted in Figures 3C and 3D.

[00276] Returning to continuing reference to the multi-level charge pump buck converter 12A of Figure 2A, the switcher control circuit 52A may be configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the parallel amplifier circuit 14A. The switcher control circuit 52A may provide a charge pump mode control signal 60 to the charge pump mode control input 62 of the multi-level charge pump circuit 56. Based upon the charge pump mode control signal 60, the multi-level charge pump circuit 56 may generate one of a plurality of output voltages or present an open circuit at the charge pump output 64. The switcher control circuit 52A may further provide a series switch control signal 66 and a shunt switch control signal 68 to the switching circuit 58.

[00277] The switching circuit 58 may include a series switch 70 and a shunt switch 72. The series switch 70 and the shunt switch 72 may be a solid state based switch such as a field effect transistor, an insulator-on-semiconductor based transistor, or a bipolar based transistor. The series switch 70 may include a first switch terminal 74, a second switch terminal 76, and a series switch control terminal 78 coupled to the series switch control signal 66. The shunt switch 72 may include a first switch terminal 80, a second switch terminal 82, and a shunt

switch control terminal 83 coupled to the shunt switch control signal 68. The first switch terminal 74 of the series switch 70 may be coupled to the supply input 24, (V_{BAT}), of the multi-level charge pump buck converters 12 and 12A, as depicted in Figures 1A and 2A. The second switch terminal 76 of the series switch 70 may be coupled to the first switch terminal 80 of the shunt switch 72 and the charge pump output 64 to form the switching voltage output 26. The second switch terminal 82 of the shunt switch 72 may be coupled to ground.

[00278] As depicted in Figure 7A, with continuing reference to Figures 1A, 2A and 3A, the multi-level charge pump circuit 56 may include a charge pump control circuit 84A, a switching network having a plurality of switches including a first switch 86, a second switch 88, a third switch 90, a fourth switch 92, a fifth switch 94, a sixth switch 96 and a seventh switch 98, a first flying capacitor 100 having a first terminal 100A and a second terminal 100B, and a second flying capacitor 102 having a first terminal 102A and a second terminal 102B. As depicted in Figure 7A, some alternative embodiments of the multi-level charge pump circuit 56 may further include an eighth switch 118 to advantageously provide an additional functional feature, described below. Each of the first switch 86, the second switch 88, the third switch 90, the fourth switch 92, the fifth switch 94, the sixth switch 96, the seventh switch 98, and the alternatively included eighth switch 118 may be a solid state based switch implemented with field effect transistors, insulator-on-semiconductor based transistors, or bipolar based transistors, or a combination thereof. Each of the first switch 86, the second switch 88, the third switch 90, the fourth switch 92, the fifth switch 94, the sixth switch 96, the seventh switch 98, and the alternatively included eighth switch 118 may be a solid state transmission gate. As another example, each of the first switch 86, the second switch 88, the third switch 90, the fourth switch 92, the fifth switch 94, the sixth switch 96, the seventh switch 98, and the alternatively included eighth switch 118 may be based on or implemented in a Gallium nitride process. The Gallium nitride process may also be referenced to as a GaN process. Alternatively, each of the first switch 86, the second switch 88, the third switch 90, the fourth switch 92, the fifth switch 94, the sixth

switch 96, the seventh switch 98, and the alternatively included eighth switch 118 may be micro-electromechanical systems (MEMS) contact type switches.

[00279] The first switch 86 may be coupled between the first terminal 100A of the first flying capacitor 100 and the charge pump output 64. The first switch 86 may include a first switch control input configured to receive a first switch control signal 104 from the charge pump control circuit 84A, where the first switch control signal 104 operably opens and closes the first switch 86 based upon the charge pump mode control signal 60. The second switch 88 may be coupled between the first terminal 100A of the first flying capacitor 100 and the supply input 24, (V_{BAT}), of the multi-level charge pump buck converter 12. The second switch 88 may include a second switch control input configured to receive a second switch control signal 106 from the charge pump control circuit 84A, where the second switch control signal 106 operably opens and closes the second switch 88 based upon the charge pump mode control signal 60. The third switch 90 may be coupled between the second terminal 100B of the first flying capacitor 100 and the supply input 24, (V_{BAT}), of the multi-level charge pump buck converter 12. The third switch 90 may include a third switch control input configured to receive a third switch control signal 108 from the charge pump control circuit 84A, where the third switch control signal 108 operably opens and closes the third switch 90 based upon the charge pump mode control signal 60. The fourth switch 92 may be coupled between the second terminal 100B of the first flying capacitor 100 and the first terminal 102A of the second flying capacitor 102. The fourth switch 92 may include a fourth switch control input configured to receive a fourth switch control signal 110 from the charge pump control circuit 84A, where the fourth switch control signal 110 operably opens and closes the fourth switch 92 based upon the charge pump mode control signal 60. The fifth switch 94 may be coupled between the supply input 24, (V_{BAT}), of the multi-level charge pump buck converter 12 and the second terminal 102B of the second flying capacitor 102. The fifth switch 94 may include a fifth switch control input configured to receive a fifth switch control signal 112 from the charge pump control circuit 84A, where the fifth switch control signal 112 operably opens and

closes the fifth switch 94 based upon the charge pump mode control signal 60. The sixth switch 96 may be coupled between the second terminal 102B of the second flying capacitor 102 and ground. The sixth switch 96 may include a sixth switch control input configured to receive a sixth switch control signal 114 from the charge pump control circuit 84A, where the sixth switch control signal 114 operably opens and closes the sixth switch 96 based upon the charge pump mode control signal 60. The seventh switch 98 may be coupled between the first terminal 102A of the second flying capacitor 102 and the charge pump output 64. The seventh switch 98 includes a seventh switch control input configured to receive a seventh switch control signal 116 from the charge pump control circuit 84A, where the seventh switch control signal 116 operably opens and closes the seventh switch 98 based upon the charge pump mode control signal 60.

[00280] Based upon the charge pump mode control signal 60 received at the charge pump control circuit 84A, the charge pump control circuit 84A may configure each of the first switch 86, the second switch 88, the third switch 90, the fourth switch 92, the fifth switch 94, the sixth switch 96, the seventh switch 98, and the alternatively included eighth switch 118 of the switching network to place the first flying capacitor 100 and the second flying capacitor 102 in various arrangements in order to place the multi-level charge pump circuit 56 in various modes of operation. As an example, the multi-level charge pump circuit 56 may be configured to operate in a "boost" or a "buck" mode of operation. As an example embodiment, the multi-level charge pump circuit 56 may have a charging mode to charge the first flying capacitor 100 and the second flying capacitor 102, a first boost mode to provide 3/2 x V_{BAT} at the charge pump output 64, and a second boost mode to provide 2 x V_{BAT} at the charge pump output 64. In some alternative embodiments of the multi-level charge pump circuit 56, the switching network may further include an eighth switch 118, the operation of which is discussed below with respect to providing a first output mode of operation. During the first boost mode and the second boost mode, the multi-level charge pump circuit 56 is configured to "boost" the supply

voltage from the supply input 24. However, during first output mode of operation, the multi-level charge pump circuit 56 may operate in a "buck" mode of operation to provide an output voltage at the charge pump output 64 that is less than a supply voltage from the supply input 24. For example, the multi-level charge pump may be configured to provide 1/2 x V_{BAT} at the charge pump output 64 while in the first output mode of operation. In a broader sense, the charge pump output 64 may be configured to provide one or more "buck" output voltages between the supply voltage and a reference voltage (ground) and also provide at least two boost output voltage levels. For example, in some embodiments of the multi-level charge pump circuit 56 may be configured to provide more than two boost voltage levels.

[00281] As an example, in response to receipt of the charge pump mode control signal 60 that indicates the multi-level charge pump circuit 56 should be in the charging mode of operation, the charge pump control circuit 84A configures the first flying capacitor 100 and the second flying capacitor 102 to be coupled in series between the supply input 24, (V_{BAT}), of the multi-level charge pump buck converter 12 and ground, where the first flying capacitor and the second flying capacitor may be switchably disconnected from the charge pump output 64. Assuming that the capacitance of the first flying capacitor 100 and the second flying capacitor 102 are equal, the first flying capacitor 100 and the second flying capacitor 102 each charge to a charged voltage of 1/2 x V_{BAT}. The charge pump control circuit 84A configures the first switch 86 to be open, the second switch 88 to be closed, the third switch 90 to be open, the fourth switch 92 to be closed, the fifth switch 94 to be open, the sixth switch 96 to be closed, and the seventh switch 98 to be open. In those embodiments of the multi-level charge pump circuit 56 that further include the eighth switch 118, the eighth switch 118 may be configured to be open.

[00282] In response to receipt of the charge pump mode control signal 60 that indicates the multi-level charge pump circuit 56 should be in the first boost mode of operation, the charge pump control circuit 84A configures the first flying capacitor 100 and the second flying capacitor 102 to be arranged in parallel

between the charge pump output 64 and the supply input 24, (V_{BAT}), to generate 3/2 x V_{BAT} at the charge pump output. The charge pump control circuit 84A configures the first switch 86 to be closed, the second switch 88 to be open, the third switch 90 to be closed, the fourth switch 92 to be open, the fifth switch 94 to be closed, the sixth switch 96 to be open, and the seventh switch 98 to be closed. In those embodiments of the multi-level charge pump circuit 56 that further include the eighth switch 118, the eighth switch 118 may be configured to be open.

[00283] In response to receipt of the charge pump mode control signal 60 that indicates the multi-level charge pump circuit 56 should be in the second boost mode of operation, the charge pump control circuit 84A configures the first flying capacitor 100 and the second flying capacitor 102 to be arranged in series between the charge pump output 64 and the supply input 24, (V_{BAT}), to generate 2 x V_{BAT} at the charge pump output 64. The charge pump control circuit 84A configures the first switch 86 to be closed, the second switch 88 to be open, the third switch 90 to be open, the fourth switch 92 to be closed, the fifth switch 94 to be closed, the sixth switch 96 to be open, and the seventh switch 98 to be open. In those embodiments of the multi-level charge pump circuit 56 that further include the eighth switch 118, the eighth switch 118 may be configured to be open.

[00284] As discussed above, some embodiments of the multi-level charge pump circuit 56 may further include an eighth switch 118 coupled between the second terminal 100B of the first flying capacitor 100 and ground in order to provide for a first output mode of operation. The eighth switch 118 may include an eighth switch control input configured to receive an eighth switch control signal 120 from the charge pump control circuit 84A, where the eighth switch control signal 120 operably opens and closes the eighth switch 118 based upon the charge pump mode control signal 60.

[00285] In the first output mode of operation, the multi-level charge pump circuit 56 may provide 1/2 x V_{BAT} at the charge pump output 64. In response to receipt of the charge pump mode control signal 60 that indicates the multi-level

charge pump circuit 56 should be in the first output mode of operation, the charge pump control circuit 84A configures the first flying capacitor 100 and the second flying capacitor 102 to be coupled in parallel between the charge pump output 64 and ground. The charge pump control circuit 84A configures the first switch 86 to be closed, the second switch 88 to be open, the third switch 90 to be open, the fourth switch 92 to be open, the fifth switch 94 to be open, the sixth switch 96 to be closed, the seventh switch 98 to be closed and the eighth switch 118 to be closed.

[00286] Otherwise, the charge pump control circuit 84A configures the eighth switch 118 to be open when the multi-level charge pump circuit 56 is in the charging mode of operation, the first boost mode of operation, or the second boost mode of operation. Advantageously, as depicted in Figure 7A, the multi-level charge pump circuit 56 only includes a first flying capacitor 100 and a second flying capacitor 102, where the switching network uses only the first flying capacitor 100 and second flying capacitor 102 to produce an output voltage at the charge pump output 64 substantially equal to one of 2 x V_{BAT}, 3/2 x V_{BAT}, and 1/2 x V_{BAT}.

[00287] Figure 7B depicts an embodiment of a multi-level charge pump circuit 258, depicted in Figures 18A and 18B, as multi-level charge pump circuit 258A. The multi-level charge pump circuit 258A is similar to the multi-level charge pump circuit 56 except the multi-level charge pump circuit 258A further includes a ninth switch 119 configured to provide an internal charge pump node parallel amplifier supply 294 as an additional output. The ninth switch 119 may be similar to the plurality of switches including the first switch 86, the second switch 88, the third switch 90, the fourth switch 92, the fifth switch 94, the sixth 96, the seventh switch 98, and eighth switch 118 of Figure 7A. In addition, the multi-level charge pump circuit 258A is similar to the multi-level charge pump circuit 56 except that the charge pump control circuit 84A is replaced by a charge pump control circuit 84B. Unlike the charge pump control circuit 84A, the charge pump control circuit 84B further includes a ninth switch control signal s configured to control the ninth switch 119.

[00288] The ninth switch 119 may include a ninth switch control input configured to receive a ninth switch control signal 121 from the charge pump control circuit 84B, where the ninth switch control signal 121 operably opens and closes the ninth switch 119 based upon the charge pump mode control signal 60. The ninth switch 119 may be operably coupled between the first terminal 102A of the second flying capacitor 102 and the internal charge pump node parallel amplifier supply 294.

[00289] Operationally, the charge pump control circuit 84B functions similar to the operation of the charge pump control circuit 84A. As an example, the multi-level charge pump circuit 258A may have a charging mode to charge the first flying capacitor 100 and the second flying capacitor 102, a first boost mode to provide 3/2 x V_{BAT} at the charge pump output 64, and a second boost mode to provide 2 x V_{BAT} at the charge pump output 64. However, unlike the charge pump control circuit 84A, the charge pump control circuit 84B is configured to operably close the ninth switch 119 when the multi-level charge pump circuit 258A is configured to operate in either the first boost mode to provide 3/2 x V_{BAT} at the charge pump output 64 or the second boost mode to provide 2 x V_{BAT} at the charge pump output 64. Thus, when the ninth switch 119 is in a closed state during either the first boost mode of operation or the second boost mode of operation, the voltage appearing on the first terminal 102A of the second flying capacitor 102, is substantially equal to 3/2 x V_{BAT}. Advantageously, the configuration of the multi-level charge pump circuit 258A provides the same voltage output level to the internal charge pump node parallel amplifier supply 294, which may improve the ripple noise on the power amplifier supply voltage V_{CC}.

[00290] Figure 7C depicts another embodiment of a multi-level charge pump circuit 258, depicted in Figures 18A and 18B, as multi-level charge pump circuit 258B. The multi-level charge pump circuit 258B is similar to the multi-level charge pump circuit 258A of Figure 7B except the ninth switch 119 may be operably coupled between the first terminal 100A of the first flying capacitor 100 and the internal charge pump node parallel amplifier supply 294.

[00291] Operationally, the charge pump control circuit 84C functions similar to the operation of the charge pump control circuit 84B. As an example, like the multi-level charge pump circuit 258A, the multi-level charge pump circuit 258B may have a charging mode to charge the first flying capacitor 100 and the second flying capacitor 102, a first boost mode to provide 3/2 x V_{BAT} at the charge pump output 64, and a second boost mode to provide 2 x V_{BAT} at the charge pump output 64. In addition, like the charge pump control circuit 84B, the charge pump control circuit 84C is configured to operably close the ninth switch 119 when the multi-level charge pump circuit 258B is configured to operate in either the first boost mode to provide 3/2 x V_{BAT} at the charge pump output 64 or the second boost mode to provide 2 x V_{BAT} at the charge pump output 64. Thus, when the ninth switch 119 is in a closed state during either the first boost mode of operation or the second boost mode of operation, the voltage appearing on the first terminal 100A of the first flying capacitor 100 may depend upon whether the multi-level charge pump circuit 258B is configured to operate in the first boost mode or the second boost mode. For example, due to the topological location of the first flying capacitor, the voltage output level provided to the internal charge pump node parallel amplifier supply 294 may be 3/2 x V_{BAT} when the multi-level charge pump circuit 258B is configured to operate in the first boost mode and 2.0 x V_{BAT} when the multi-level charge pump circuit 258B is configured to operate in the second boost mode. As a result, advantageously, the multi-level charge pump circuit 258B may provide a higher power supply rail for the parallel amplifier 35 of Figures 18A and 18B. In particular, in the case where the parallel amplifier 35 of Figures 18A and 18B is a rechargeable parallel amplifier, similar to the rechargeable parallel amplifier 35E of Figure 12E and the rechargeable parallel amplifier 35F of Figure 12F, the saved charge voltage, V_{AB}, on the charge conservation capacitor 228, C_{AB}, may be increased and result in a larger range of operation of the second output stage, as depicted in Figures 12E and 12F.

[00292] Figure 7D depicts another embodiment of the multi-level charge pump circuit 258, depicted in Figures 18A and 18B, and the multi-level charge pump

circuit 56, depicted in Figure 7A, as multi-level charge pump circuit 258C. The multi-level charge pump circuit 258C is similar in form and function to the multi-level charge pump circuit 258A of Figure 7B and the multi-level charge pump circuit 258A of Figure 7C. However, the multi-level charge pump circuit 258C may include a charge pump control circuit 84D that is similar in form and function to the charge pump control circuit 84A of Figure 7A, except the charge pump control circuit 84D further includes a ninth switch control configured to generate a ninth switch control signal 121A to control a ninth switch 119A and a tenth switch control signal 121B to control a tenth switch 119B. Thus, the multi-level charge pump circuit 258C may include a switching network having a plurality of switches including a first switch 86, a second switch 88, a third switch 90, a fourth switch 92, a fifth switch 94, a sixth switch 96 and a seventh switch 98, an eighth switch 118, a ninth switch 119A, and a tenth switch 119B.

[00293] As previously described with respect to the multi-level charge pump circuit 256A, depicted in Figure 7B, and the multi-level charge pump circuit 256B, depicted in Figure 7C, some embodiment of the multi-level charge pump circuit 256C may selectively disable the tenth switch 119B and control the ninth switch 119A in a fashion similar to the ninth switch 119 of the multi-level charge pump circuit 256B, depicted in Figure 7C, to generate a charge pump output voltage, V_{CP_OUTPUT}, on the charge pump output capacitor, C_{CP_OUTPUT}, substantially equal to 2 x V_{BAT}. Alternatively, some embodiments of the multi-level charge pump circuit 256C may selectively disable the ninth switch 119A and control the tenth switch 119B in a fashion similar to the ninth switch 119 of the multi-level charge pump circuit 256A, depicted in Figure 7B, to generate a charge pump output voltage, V_{CP_OUTPUT}, on the charge pump output capacitor, C_{CP_OUTPUT}, substantially equal to 3/2 x V_{BAT}. However, some embodiments of the multi-level charge pump circuit 256C may be further configured to generate a charge pump output voltage, V_{CP_OUTPUT}, on the charge pump output capacitor, C_{CP_OUTPUT}, substantially equal to 1/2 x V_{BAT} by enabling the tenth switch 119B when the multi-level charge pump circuit 256C is operating in either a shunt output mode of operation or a series output mode of operation.

[00294] Alternatively, the multi-level charge pump circuit 256C may be further configured to generate a charge pump output voltage, V_{CP_OUTPUT}, on the charge pump output capacitor, C_{CP_OUTPUT}, substantially equal to 1 x V_{BAT} by enabling the ninth switch 119A when the multi-level charge pump circuit 256C is operating in either a shunt output mode of operation or a series output mode of operation.

[00295] In addition, referring to Figures 40A-40C and Figures 46A-B, in some embodiments of the power management system 870 and 870A that include a multi-level charge pump 882 substantially similar to the multi-level charge pump circuit 256C depicted in Figure 7D. The multi-level charge pump circuit 256C may disable the first switch 86 and the seventh switch 98 to decouple the operation of the multi-level charge pump circuit 256C from the switching voltage output 26.

[00296] For example, referring to Figures 40B, the switch mode power supply converter 872 may be configured to operate in various modes of operation including at least one off mode, a number of various types of envelope tracking modes, and a number of various types of averge power tracking modes as a function of an expected output power to be generated during a data transmission by embodiments of a radio frequency power amplifier 869, depicted in Figures 40A and Figures 40C-E, and embodiments of a radio frequency power amplifier 869', depicted in Figure 46A-H. For example, in the off mode, the switch mode power supply converter 872 may cease generation of a switching voltage, and provide a high impedance path to ground at the switching voltage output 26. Some embodiments of the average power tracking modes may include a medium power average power tracking modulation mode during which the multi-level charge pump 882 does not provide the switching voltage, V_{SW}. In addition, in a low power modulation mode and a low power average tracking modulation mode, the switch mode power supply converter 872 may be in an off mode. In some embodiments of a medium power average power tracking modulation mode, the switch mode power supply converter 872 may operate in a "bang-bang" mode of operation to generate a switching voltage, V_{SW}, substantially equal to either the battery voltage, V_{BAT}, or ground. In these cases,

the charge pump control circuit 84D may configure the switching network of the multi-level charge pump circuit 256C to generate various fractional voltages of the battery voltage, V_{BAT}, in a fashion similar to the operation of the μC charge pump circuit 262A and the μC charge pump circuit 262B, depicted in Figures 19A and 19B. In other words, the charge pump control circuit 84D may be configured to operate in phases of operation to generate either boost output voltages or buck output voltages using only the first flying capacitor 100 and the second flying capacitor 102. As an example, the multi-level charge pump circuit 258C may be configured to generate a charge pump output voltage, V_{CP_OUTPUT}, substantially equal to 3 x V_{BAT}. In a first phase of operation, the charge pump control circuit 84D may enabling the third switch 90, the fourth switch 92 and the sixth switch 96 to generate a voltage across the second flying capacitor substantially equal to the battery voltage, V_{BAT}. In a second phase of operation, the charge pump control circuit 84D may enable the second switch 88 and the eighth switch 118 to generate a voltage across the first flying capacitor substantially equal to the battery voltage, V_{BAT}. And in a third phase of operation, the charge pump control circuit 84D may enable the fourth switch 92, the fifth switch 94, and the ninth switch 119A to transfer the charge stored on the first flying capacitor 100 and the second flying capacitor 102 to the charge pump output capacitor, C_{CP_OUTPUT}. The voltage on the first terminal 100A of the first flying capacitor 100 is substantially equal to 3 x V_{BAT}. Accordingly, the charge pump output voltage, V_{CP_OUTPUT}, may be substantially equal to 3 x V_{BAT}.

[00297] In some embodiments of the multi-level charge pump circuit 258C, some or all of the plurality of switches may be segmented in a fashion similar to the segmented series and shunt switches of the switching circuit 884, depicted in Figure 40B. In addition, in some embodiments, only those switches used to generate the charge pump output voltage, V_{CP_OUTPUT}, may be segmented based on the expected current load.

[00298] Returning to Figure 3A, for the sake of clarity and not by way of limitation, the following discussion of the operation of the circuits depicted in Figure 3A will be done with continuing reference to the multi-level charge pump

buck converter 12A depicted in Figure 2A. As depicted in Figure 3A, the switcher control circuit 52A may include a programmable threshold circuit 122 configured to receive a plurality of programmable threshold levels and one embodiment of a threshold detector and control circuit 132A. For example, in some embodiments, the plurality of threshold levels stored in the programmable threshold circuit 122 may include a shunt level threshold parameter, a series level threshold parameter, a first boost level threshold parameter, and a second boost level threshold parameter. In other embodiments, plurality of threshold levels stored in the programmable threshold circuit 122 may further include a first buck level threshold parameter or a first output level threshold level. In some embodiments of the programmable threshold circuit 122, the programmable threshold circuit 122 may include sets of programmable threshold levels, where each set of programmable threshold levels includes a plurality of threshold levels stored in the programmable threshold circuit 122.

[00299] The programmable threshold levels may be received from a controller 50 via the control bus 44. As an example, in some embodiments, the controller 50 may provide a shunt level threshold parameter, a series level threshold parameter, a first boost level threshold parameter, and a second boost level threshold parameter. Generally, the series level threshold parameter is set to a value greater than the shunt level threshold level parameter, the first boost level threshold parameter is set to a value greater than the series level threshold parameter, and the second boost level threshold parameter is set to a value greater than the first boost level threshold parameter. In another embodiment, the controller 50 may further provide a first output level threshold parameter. In some embodiments, the first output level threshold parameter is set to a value greater than the shunt level threshold parameter but less than the series level threshold parameter. In some embodiments, the switcher control circuit 52A may configure the multi-level charge pump buck converter 12A to operate at a desire average switching frequency. For example, in some embodiments of the switcher control circuit 52A, the threshold detector and control circuit 132A may determine the average frequency of operation based on the charge pump mode

control signal 60, the series switch control signal 66, and the shunt switch control signal 68. In other embodiments, logic circuit 148A of the threshold detector and control circuit 132A, depicted in Figure 4A, may determine the average frequency of operation. Based on the determined average frequency of operation, the controller 50 or the switcher control circuit 52 may configure or adjust the shunt level threshold parameter, the first buck level threshold, parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12A to operate at a desired or target average switching frequency. In those embodiments having a multi-level charge pump circuit 56 that includes a first output mode of operation, the controller 50 or the switcher control circuit 52 may configure or adjust the shunt level threshold parameter, the first output level threshold parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12A to operate at a desired or target average switching frequency.

[00300] As an example, each of the threshold levels may correspond to one of a plurality of output modes of the multi-level charge pump buck converter 12A. As an example, the shunt level threshold parameter may correspond to a shunt output mode of operation. In a shunt output mode of operation of the multi-level charge pump buck converter 12A, the series switch 70 is open (not conducting), the multi-level charge pump circuit 56 is in the charging mode of operation, and the shunt switch 72 is closed (conducting) to generate zero volts at the switching voltage output 26. The shunt output mode of operation provides a conduct path for current to continue flowing through the power inductor 16 when the multi-level charge pump circuit 56 is in the charging mode of operation and the series switch 70 is open (not conducting). The first output level threshold parameter may correspond to a first output mode of operation of the multi-level charge pump buck converter 12A. In the first output mode of operation, both the series switch 70 and the shunt switch 72 are open and the multi-level charge pump

circuit 56 is in the first output mode of operation to generate a switching voltage substantially equal to $V_{BAT}/2$ at the switching voltage output 26. In some embodiments, the multi-level charge pump circuit 56 may be configured to generate a switching voltage other than $V_{BAT}/2$ that is between a shunt level output voltage and a series level output when operating in first output mode of operation. The series level threshold parameter may correspond to a shunt output mode of operation of the multi-level charge pump buck converter 12A. In a series output mode of operation, the series switch 70 is closed (conducting), the multi-level charge pump circuit 56 is in the charging mode of operation, and the shunt switch 72 is open to generate V_{BAT} at the switching voltage output 26. The first boost level threshold parameter may correspond to a first boost output mode of operation of the multi-level charge pump buck converter 12A. In the first boost output mode of operation, both the series switch 70 and the shunt switch 72 are open and the multi-level charge pump circuit 56 is in the first boost mode of operation to generate 3/2 x V_{BAT} at the switching voltage output 26. The second boost level threshold parameter may correspond to a second boost output mode of operation of the multi-level charge pump buck converter 12A. In a second boost output mode of operation, both the series switch 70 and the shunt switch 72 are open and the multi-level charge pump circuit 56 is in the second boost mode of operation to generate a 2 x V_{BAT} at the switching voltage output 26.

[00301] Based upon the shunt level threshold parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter, the programmable threshold circuit 122 generates a shunt level threshold 124, a series level threshold 126, a first boost level threshold 128, and a second boost level threshold 130, respectively, which are provided to the threshold detector and control circuit 132A. In those embodiments that provide for a first output level threshold parameter and a first output mode of operation of the multi-level charge pump circuit 56, the programmable threshold circuit 122 may further generate a first output level threshold (not shown), which is provided to the threshold detector and control

circuit 132A. As depicted in Figure 3A, the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, the second boost level threshold 130 and the first output level threshold may be represented by a current level for use with a current comparator. In alternative embodiments, programmable threshold circuit 122 may be configured to generate the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, the second boost level threshold 130 and the first output level threshold as voltage levels to be used in conjunction with voltage comparator circuits.

[00302] The switcher control circuit 52A may also receive a mode switch control signal 131 from the controller 50. The mode switch control signal 131 may configure the threshold detector and control circuit 132A to operate the multi-level charge pump buck converter 12A in different modes of operation. As an example, the mode switch control signal 131 may configure operation of a state machine within the threshold detector and control circuit 132A that governs how the switching voltage output 26 transitions the switching voltage output 26 to provide different output levels. As a first example embodiment of a state machine within the threshold detector and control circuit 132A, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12A to operate in a first mode of operation, depicted in Figure 5A. As another example embodiment of a state machine within the threshold detector and control circuit 132A, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12A to operate in a second mode of operation, depicted in Figure 6A.

[00303] Continuing with Figure 3A, the switcher control circuit 52A may further include a multiplier circuit 134 and a summing circuit 136. The multiplier circuit may be configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT\ EST}$, and a threshold scalar 137A from the threshold detector and control circuit 132A. The threshold scalar 137A may be provided by frequency locked loop circuit 54A, which is one embodiment of the frequency locked loop circuit 54 depicted in Figure 2A.

[00304] The frequency locked loop circuit 54A receives a clock reference signal 139A from a clock reference 139 and a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$. The frequency locked loop circuit 54A extracts the operating frequency of the multi-level charge pump buck converter 12A based upon the logic level indication of the switching voltage output, $V_{SW_EST_OUT}$. Thereafter, the frequency locked loop circuit 54A compares the extracted operating frequency of the multi-level charge pump buck converter 12A to the clock reference signal 139A to generate the threshold scalar 137A. The magnitude of the threshold scalar 137A may be used to adjust the operating frequency of the multi-level charge pump buck converter 12A. In some embodiments (not shown), the frequency locked loop circuit 54A may provide the threshold scalar 137A directly to the multiplier circuit 134. As an example, the frequency locked loop circuit 54A may be configured to adjust the magnitude of the threshold scalar 137A to maintain an average switching frequency of operation of the multi-level charge pump buck converter 12A by controlling the magnitude of a feedback signal from the parallel amplifier circuit 14A. For example, the magnitude of a feedback signal from the parallel amplifier circuit 14A may be changed by multiplying the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to maintain an average switching frequency of operation of the multi-level charge pump buck converter 12A. The controller 50 may configure the frequency locked loop circuit to derive a target average switching frequency of operation from the clock reference signal 139A based on a target average frequency of operation parameter. The frequency locked loop circuit 54A compares the extracted operating frequency of the multi-level charge pump converter converter 12A to the target average switching frequency of operation derived from the clock reference signal 139A to generate the threshold scalar 137A. Alternatively, the controller may configure the clock reference 139 to provide the frequency locked loop circuit 54A a clock reference signal 139A based on the target average frequency of operation parameter, where the clock reference signal 139A has a frequency substantially equal to the target average switching frequency of operation. In this case, the frequency

locked loop circuit 54A compares the extracted operating frequency of the multi-level charge pump buck converter 12A to the target average switching frequency of operation provided by the clock reference signal 139A to generate the threshold scalar 137A.

[00305] The multiplier circuit 134 may multiply the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, by the threshold scalar 137A to generate a scaled parallel amplifier circuit output current estimate 138. The scaled parallel amplifier circuit output current estimate 138 is provided to the summing circuit 136. The summing circuit 136 subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the scaled parallel amplifier circuit output current estimate 138 to generate a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, which may be used as a composite control signal for the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 as depicted, for example, in Figure 4A. In those embodiments of the parallel amplifier circuit 14 that do not include the V_{OFFSET} loop circuit 41, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and summing circuit 136 are omitted.

[00306] The scaled parallel amplifier circuit output current estimate 138 may be used to control the operating frequency of the multi-level charge pump buck converter 12A by increasing or decreasing the magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. As an example, the frequency locked loop circuit 54A may be configured to increase the magnitude of the threshold scalar 137A to increase the magnitude of the scaled parallel amplifier circuit output current estimate 138. As the magnitude of the scaled parallel amplifier circuit output current estimate 138 increases, the operating frequency of the multi-level charge pump buck converter 12A will tend to also increase, which will tend to increase the power inductor current, I_{SW_OUT}, delivered by the power inductor 16. The frequency locked loop circuit 54A may be further be configured to decrease the magnitude of the threshold scalar 137A to decrease the magnitude of the scaled parallel amplifier circuit output current estimate 138. As the magnitude of the scaled parallel amplifier circuit output current estimate 138

decreases, the magnitude of the scaled parallel amplifier circuit output current estimate 138, will tend to decrease the operating frequency of the multi-level charge pump buck converter 12A. As the operating frequency of the multi-level charge pump buck converter 12A decreases, the power inductor current, I_{SW_OUT}, delivered by the power inductor 16, tends to decrease. The threshold offset current 42, $I_{THRESHOLD_OFFSET}$, may be used to control the offset voltage, V_{OFFSET}, which appears across the coupling circuit 18, depicted in Figure 2A.

[00307] Figure 8 depicts the V_{OFFSET} loop circuit 41 that generates the threshold offset current, $I_{THRESHOLD_OFFSET}$. Returning to Figure 3A, as the threshold offset current, $I_{THRESHOLD_OFFSET}$, increases above zero current, the value magnitude of the compensated parallel amplifier circuit output current estimate, $I_{PAWA_COMP_EST}$, is reduced, which tends to lower the output frequency of the multi-level charge pump buck converter 12A. As the output frequency of the multi-level charge pump buck converter 12A is decreased, the power inductor current, I_{SW_OUT}, delivered by the power inductor 16 will also decrease. As the power inductor current, I_{SW_OUT}, delivered by the power inductor 16 decreases, the offset voltage, V_{OFFSET}, also decreases because the parallel amplifier circuit output current, I_{PAWA_OUT}, tends to become positive to compensate for the reduction of the power inductor current, I_{SW_OUT}. As the threshold offset current, $I_{THRESHOLD_OFFSET}$, decreases below zero current, the value magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is increased, and as a result, the output frequency, also referred to as switching frequency, of the multi-level charge pump buck converter 12A tends to increase. As the output frequency of the multi-level charge pump buck converter 12A is increased, the power inductor current, I_{SW_OUT}, delivered by the power inductor 16 increases. As the power inductor current, I_{SW_OUT}, increases, the offset voltage, V_{OFFSET}, also tends to increase because the parallel amplifier circuit output current, I_{PAWA_OUT}, tends to become negative to absorb the increase of the power inductor current, I_{SW_OUT}. Because only the magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is scaled by the threshold scalar 137A, the average switching frequency of operation of the multi-level

charge pump buck converter 12A is adjusted independent of the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is used to regulate the offset voltage, V_{OFFSET}, between the power amplifier supply output 28 and the parallel amplifier output 32A. Alternatively, in some embodiments, (not depicted) the summing circuit 136 subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, where the difference between the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, is multiplied by the threshold scalar 137A with the multiplier circuit 134 to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}.

[00308] As depicted in Figure 4A, with continuing reference to Figures 2A and 3A, the threshold detector and control circuit 132A of the switcher control circuit 52A includes a first comparator 140, a second comparator 142, a third comparator 144, a fourth comparator 146, and a logic circuit 148A. The example embodiment of the logic circuit 148A may include a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gates or transistor logic, discrete hardware components, or any combination thereof. Some embodiments of the logic circuit 148A may be implemented in either a digital or analog processor. As depicted in Figure 4A, the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 may be configured as current comparators. However, in some alternative embodiments, the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 may be configured as voltage comparator circuits, where the input currents provided as inputs to the positive terminal and the negative terminal of each respective one of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 is first converted to a voltage level.

[00309] The first comparator 140 includes a positive terminal coupled to the shunt level threshold 124, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, and a first comparator output configured to generate a shunt level indication 150A, which is

provided to the logic circuit 148A. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the shunt level threshold 124, the shunt level indication 150A is asserted by setting output of the first comparator 140 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124, the shunt level indication 150A is de-asserted by setting output of the first comparator 140 to a digital logic high state. The second comparator 142 includes a positive terminal coupled to the series level threshold 126, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, and a second comparator output configured to generate a series level indication 152A, which is provided to the logic circuit 148A. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the series level threshold 126, the series level indication 152A is asserted by setting output of the second comparator 142 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the series level threshold 126, the series level indication 152A is de-asserted by setting output of the second comparator 150 to a digital logic high state. The third comparator 144 includes a positive terminal coupled to the first boost level threshold 128, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, and a third comparator output configured to generate a first boost level indication 154A, which is provided to the logic circuit 148A. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the first boost level threshold 128, the first boost level indication 154A is asserted by setting output of the third comparator 144 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the first boost level threshold 128, the first boost level indication 154A is de-asserted by setting output of the third comparator 144 to a digital logic high state. The fourth comparator 146 includes a positive terminal coupled to the second boost level threshold 130, a negative terminal coupled to the compensated parallel amplifier

circuit output current estimate, I_{PAWA_COMP}, and a fourth comparator output configured to generate a second boost level indication 156A, which is provided to the logic circuit 148A. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the second boost level threshold 130, the second boost level indication 156A is asserted by setting output of the fourth comparator 146 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the second boost level threshold 130, the second boost level indication 156A is de-asserted by setting output of the fourth comparator 146 to a digital logic high state.

[00310] The threshold detector and control circuit 132A may further include a first output buffer 158, a second output buffer 160, and a third output buffer 161. The logic circuit 148A may provide a charge pump mode control signal 60, a series switch control output 162, a provides a shunt switch control output 164, and a one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$. The logic circuit 148A generates the series switch control output 162 to drive the first output buffer 158, which provides the series switch control signal 66 to the series switch 70. The logic circuit 148A generates a shunt switch control output 164 to drive the second output buffer 160, which provides the shunt switch control signal 68 to the shunt switch 72. In addition, logic circuit 148A generates the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, to drive the third output buffer 161, which provide the estimated switching voltage output 38B, V_{SW_EST}. Each of the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, indicates a future output mode of the multi-level charge pump buck converter 12A. In other words, the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$ are a feed forward signal that represents a state of the switcher control circuit 52A that will be used to configure the multi-level charge pump buck converter 12A to provide a future voltage level of the switching voltage, V_{SW}, at the switching voltage output 26. In other words, due to delays in the switcher control circuit 52A, the multi-level charge pump circuit 56,

and the switching circuit 58, the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), may provide an early indication of what the switching voltage, V_{SW}, at the switching voltage output 26 will become before the voltage level at the switching voltage output 26 transitions to reflect the switching voltage, V_{SW}, indicated by the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s). Based upon one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), the third output buffer 161 generates the estimated switching voltage output 38B, V_{SW_EST}. The third output buffer 161 is supplied by the DC voltage, V_{BAT}, such that the output of the third output buffer 161 does not exceed the DC voltage, V_{BAT}.

[00311] Figure 11A through Figure 11F depict various waveforms that may be used to represent the estimated switching voltage output 38B, V_{SW_EST}. Figure 11A depicts one embodiment of the estimated switching voltage output 38B, V_{SW_EST}, When the multi-level charge pump buck converter 12A is in either the series output mode, the first boost output mode, or the second boost output mode, the third output buffer 161 outputs a boost/series mode level. Alternatively, when the multi-level charge pump buck converter 12A is in the shunt output mode, the third output buffer 161 outputs a shunt mode level.

[00312] Figure 11B depicts another embodiment of the estimated switching voltage output 38B, V_{SW_EST}. When the multi-level charge pump buck converter 12A is in the series output mode, the third output buffer 161 generates a series level. When the multi-level charge pump buck converter 12A is in either the first boost output mode or the second boost output mode, the third output buffer 161 outputs a boost mode level. Alternatively, when the multi-level charge pump buck converter 12A is in the shunt output mode, the third output buffer 161 outputs a shunt mode level.

[00313] Figure 11C depicts another embodiment of the estimated switching voltage output 38B, V_{SW_EST}. When the multi-level charge pump buck converter 12A is in the series output mode, the third output buffer 161 generates a series level. When the multi-level charge pump buck converter 12A is in the first boost output mode the third output buffer 161 generates a first boost level.

When the multi-level charge pump buck converter 12A is in the second boost output mode, the third output buffer 161 outputs a second boost mode level. Alternatively, when the multi-level charge pump buck converter 12A is in the shunt output mode, the third output buffer 161 outputs a shunt mode level.

[00314] Figure 11D depicts another embodiment of the estimated switching voltage output 38B, V_{SW_EST}, for the case where the multi-level charge pump circuit 56 includes a first output mode of operation. When the multi-level charge pump buck converter 12A is in the first output mode of operation, the third output buffer 161 generates a first output level. When the multi-level charge pump buck converter 12A is in the series output mode, the third output buffer 161 generates a series level. When the multi-level charge pump buck converter 12A is in the first boost output mode, the third output buffer 161 generates a first boost level. When the multi-level charge pump buck converter 12A is in the second boost output mode, the third output buffer 161 outputs a second boost mode level. Alternatively, when the multi-level charge pump buck converter 12A is in the shunt output mode, the third output buffer 161 outputs a shunt level.

[00315] Figure 11E depicts another embodiment of the estimated switching voltage output 38B, V_{SW_EST}, for the case where the multi-level charge pump circuit 56 includes a first output mode of operation. When the multi-level charge pump buck converter 12A is in the first output mode of operation, the third output buffer 161 generates a first output level. However, when the multi-level charge pump buck converter 12A is in either the series output mode, the first boost output mode, or the second boost output mode, the third output buffer 161 generates a boost/series level. Alternatively, when the multi-level charge pump buck converter 12A is in the shunt output mode, the third output buffer 161 outputs a shunt mode level.

[00316] Figure 11F depicts another embodiment of the estimated switching voltage output 38B, V_{SW_EST}, for the case where the multi-level charge pump circuit 56 includes a first output mode of operation. When the multi-level charge pump buck converter 12A is in either the series output mode, the first boost mode, or the second boost mode, the third output buffer 161 generates a

boost/series level. Alternatively, when the multi-level charge pump buck converter 12A is in either the first output mode of operation or the shunt output mode, the third output buffer 161 outputs a shunt level.

[00317] Figure 8 depicts an embodiment of the V_{OFFSET} loop circuit 41, depicted in Figures 2A and 2B. The embodiment of the V_{OFFSET} loop circuit 41, depicted in Figure 8, generates the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, based upon a calculated value of the offset voltage, V_{OFFSET}, and a target offset voltage, V_{OFFSET_TARGET}. For the sake of simplicity, and without limitation, the operation of the V_{OFFSET} loop circuit 41, depicted in Figure 8, will be done with continuing reference to Figure 2A.

[00318] The target offset voltage, V_{OFFSET_TARGET}, may be based upon a parameter provided by the controller 50 to the parallel amplifier circuit 14.

[00319] The V_{OFFSET} loop circuit 41 includes a first subtractor circuit, a second subtractor circuit, and an integrator circuit. The first subtractor circuit may be configured to receive the power amplifier supply voltage, V_{CC}, and the parallel amplifier output voltage, V_{PARA_AMP}. The first subtractor circuit subtracts the parallel amplifier output voltage, V_{PARA_AMP} from the power amplifier supply voltage, V_{CC}, to generate the offset voltage, V_{OFFSET}, which appears across the coupling circuit 18, depicted in Figure 2A. The second subtractor circuit receives the offset voltage, V_{OFFSET}, and the target offset voltage, V_{OFFSET_TARGET}. The second subtractor circuit subtracts the target offset voltage, V_{OFFSET_TARGET}, from the offset voltage, V_{OFFSET}, to generate an offset error voltage, V_{OFFSET_ERROR}, which is provided to the integrator circuit. The integrator circuit integrates the offset error voltage, V_{OFFSET_ERROR}, to generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is provided to the multi-level charge pump buck converter 12A, depicted in Figure 2A.

[00320] The operation of the logic circuit 148A of Figure 4A will now be discussed with continuing reference to Figures 2A, 3A, 5A, 6A, and 7A. The logic circuit 148A may be digital or analog based logic configured for one or more state machines of the threshold detector and control circuit 132A. As an example embodiment, the logic circuit 148A (Figure 4A) may have a first state machine

corresponding to a first mode of operation of the multi-level charge pump buck converter 12A, depicted in Figure 5A, and a second state machine corresponding to a second mode of operation of the multi-level charge pump buck converter 12A, depicted in Figure 6A. Based on the mode switch control signal 131 received by the threshold detector and control circuit 132A, the threshold detector and control circuit 132A may configure the logic circuit 148A to use the first state machine to govern operation of the multi-level charge pump buck converter 12A using the first state machine of the logic circuit 148A, depicted in Figure 5A. Alternatively, the threshold detector and control circuit 132A may configure the logic circuit 148A to use the second state machine to govern operation of the multi-level charge pump buck converter 12A using the second state machine of the logic circuit 148A, depicted in Figure 6A.

[00321] As depicted in Figure 4A, the logic circuit 148A may include a boost lockout counter 184 and a boost time counter 186. The boost time counter 186 may be used to keep track of the time that the multi-level charge pump buck converter 12A of Figure 2A is in either the first boost output mode or the second output boost mode. When the multi-level charge pump buck converter 12A is in either the first boost output mode or the second boost output mode, the multi-level charge pump circuit 56 (Figure 3A) is configured to be in either the first boost mode of operation or the second boost mode of operation, respectively. In one embodiment of the logic circuit 148A, when the logic circuit 148A determines that the multi-level charge pump buck converter 12A is in either the first boost output mode or the second output boost mode, the logic circuit 148A resets the counter output of the boost time counter 186 and enables the boost time counter 186 to begin counting up. The logic circuit 148A compares the counter output of the boost time counter 186 to a maximum boost time parameter, which may be provided by the controller 50. If the counter output of the boost time counter 186 is equal to or exceeds the maximum boost time parameter before the multi-level charge pump buck converter 12A is configured to return to either the shunt output mode of operation or the series output mode of operation, the logic circuit 148A asserts a minimum charge time indicator. However, if the

multi-level charge pump buck converter 12A returns to either the series output mode of operation or the shunt output mode of operation while the counter output of the boost time counter 186 is less than the maximum boost time parameter, the logic circuit 148A de-asserts the minimum charge time indicator.

[00322] The boost lockout counter 184 may be a count-down timer that is used to ensure that the multi-level charge pump circuit 56 of Figures 2A and 3A remains in a charging mode of operation for a minimum charge time period after the multi-level charge pump circuit 56 has been in either the first boost mode of operation or the second boost mode of operation. This permits the first flying capacitor 100 and the second flying capacitor 102, of Figure 7A, a sufficient amount of time to charge before the multi-level charge pump circuit 56 transitions again into either the first boost mode of operation or the second boost mode of operation. The minimum charge time period may be a parameter provided by the controller 50 via the control bus 44, as depicted in Figure 1A. Operationally, after the multi-level charge pump buck converter 12A transitions from either the first boost output mode or the second boost output mode to either the shunt output mode of operation or the series output mode of operation, the logic circuit 148A determines whether the minimum charge time indicator is asserted. If the minimum charge time indicator is asserted, the logic circuit 148A sets the count value of the boost lockout counter 184 to an equal minimum charge time period and enables the boost lockout counter 184 to begin counting down. Once the boost lockout counter 184 counts down to zero, the logic circuit 148A is configured to de-assert the minimum charge time indicator.

[00323] Operation of the first state machine implemented in the logic circuit 148A, which is depicted in Figure 5A, will now be described. The first state machine includes a shunt output mode 188A, a series output mode 190A, a first boost output mode 192A, and a second boost output mode 194A.

[00324] In the shunt output mode 188A, the logic circuit 148A (Figure 4A) configures the series switch control output 162 such that the series switch 70 (Figure 3A) is in an open state (not conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in

a closed state (conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 2A) to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to ground. In response to assertion of the series level indication 152A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the series level threshold 126, the logic circuit 148A configures the first state machine to transition to the series output mode 190A. Otherwise, the state machine remains in the shunt output mode 188A.

[00325] In the series output mode 190A, the logic circuit 148A configures the series switch control output 162 such that the series switch 70 is in a closed state (conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}.

[00326] In response to de-assertion of the shunt level indication 150A (Figure 4A), which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124, the logic circuit 148A configures the first state machine to transition to the shunt output mode 188A (Figure 5A). However, in response to assertion of the first boost level indication 154A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the first boost level threshold 128, the logic circuit 148A configures the first state machine to transition to the desired voltage level of the power amplifier supply voltage V_{CC}, that correspond to the first boost output mode 192A. Otherwise, the first state machine remains in the series output mode 190A.

[00327] In the first boost output mode 192A, the logic circuit 148A (Figure 4A) configures the series switch control output 162 such that the series switch 70 (Figure 3A) is in an open state (not conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the shunt level indication 150A (Figure 4A), which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124, the logic circuit 148A configures the first state machine to transition to the shunt output mode 188A (Figure 5A). However, in response to assertion of the second boost level indication 156A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the second boost level threshold 130, the logic circuit 148A configures the first state machine to transition to the second boost output mode 194A. Otherwise, the first state machine remains in the first boost output mode 192A.

[00328] In the second boost output mode 194A, the logic circuit 148A (Figure 4A) configures the series switch control output 162 such that the series switch 70 (Figure 3A) is in an open state (not conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}. In response to de-assertion of the shunt level indication 150A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124, the first state machine

transitions to the shunt output mode 188A. Otherwise, the state machine remains in the second boost output mode 194A. In some embodiments, the first state machine may further includes a first output mode (not shown). Under certain operational conditions, the first state machine may be configured to transition from the shunt output mode 188A to the first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the first output level threshold and from the first output mode to the shunt output mode 188A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124. In addition, in some embodiments, the first state machine may be further configured to transition from the first output mode to the series output mode 190A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the series level threshold 126 and from the series output mode 190A to the first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is either less than the first output level threshold or less than the series level threshold 126. In some alternative embodiments, the state machine may be configured to bypass the first output mode under certain conditions. For example, in some embodiments, the first state machine may transition from the series output mode 190A to first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than either the first output level threshold or the series level threshold but transition directly from the shunt output mode 188A to the series output mode 190A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the series level threshold 126. Conversely, in some embodiments, the first state machine may transition directly from the shunt output mode 188A to the series output mode 190A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the series level threshold 126 but transition from the series output mode 190A to the first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the first output level threshold but less than the series level threshold 126. In still other embodiments, the switcher control

circuit 52A may configure the first state machine to bypass the first output mode based on an amount of time the multi-level charge pump circuit 56 has been in the first boost output mode, the second output boost mode, the first output mode, and/or a combination thereof. As an alternative, the switcher control circuit 52A may configure the first state machine to bypass the first output mode based on an expected envelope characteristics of the signal to be transmitted, a frequency at which or a percentage of time the multi-level charge pump circuit 56 is providing the switching voltage, V_{SW}, and/or a measurement of a voltage across the first flying capacitor 100, the second flying capacitor 102, the first flying capacitor 100 and the second flying capacitor 102, average switching frequency of operation of the multi-level charge pump buck converter 12A and/or some combination thereof.

[00329] Operation of the second state machine of the logic circuit 148A, which is depicted in Figure 6A, will now be described. The second state machine includes a shunt output mode 196A, a series output mode 198A, a first boost output mode 200A, and a second boost output mode 202A. In addition, the second state machine uses the above-described boost lockout counter 184 and boost time counter 186 of the logic circuit 148A.

[00330] In the shunt output mode 196A, the logic circuit 148A (Figure 4A) configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in a closed state (conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3A) to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to ground. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to assertion of the series level indication 152A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the series level threshold 126, the second state machine transitions to the series

output mode 198A. Otherwise, the second state machine remains in the shunt output mode 196A.

[00331] In the series output mode 198A, the logic circuit 148A (Figure 4A) configures the series switch control output 162 such that the series switch 70 is in a closed state (conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to de-assertion of the shunt level indication 150A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124, the logic circuit 148A configures the second state machine to transition to the shunt output mode 196A. However, in response to assertion of the first boost level indication 154D, which indicates that the compensated power amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the first boost level threshold 128, the logic circuit 148A determines whether both the minimum charge time indicator is de-asserted and the first boost level indication 154A is asserted. If the minimum charge time indicator is de-asserted and the first boost level indication 154A is asserted, the logic circuit 148A configures the second machine to transition to the first boost output mode 200A. Otherwise, the logic circuit 148A prevents the second state machine from transitioning to the first boost output mode 200A until the minimum time indicator is de-asserted. Once both the minimum charge time indicator is de-asserted and the first boost level indication 154A is asserted, the logic circuit 148A configures the second state machine to transition to the first boost output mode 200A, resets the counter output of the boost time counter 186, and enables the boost time counter 186 to begin counting up. Otherwise, the second state machine remains in the series output mode 198A.

[00332] In the first boost output mode 200A, the logic circuit 148A configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the first boost level indication 154A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the first boost level threshold 128, the logic circuit 148A configures the second state machine to transition to the series output mode 198A. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148A asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148A sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. However, in response to assertion of the second boost level indication 156A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the second boost level threshold 130, the logic circuit 148A configures the second state machine to transition to the second boost output mode 202A. Otherwise, the second state machine remains in the first boost output mode 200A.

[00333] In the second boost output mode 202A, the logic circuit 148A configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148A also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148A configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3A) to be in a second boost mode of operation to provide 2 x V_{BAT} at the

charge pump output 64. As a result, the switching voltage output 26 of Figure 3A is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}.

[00334] In response to de-assertion of the first boost level indication 154A, which indicates that the compensated power amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the first boost level threshold 128, the logic circuit 148A configures the second state machine to transition to the series output mode 198A. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148A asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148A sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. Otherwise, the second state machine remains in the second boost output mode 202A. In some embodiments, the second state machine may further include a first output mode (not shown). Under certain operational conditions, the second state machine may be configured to transition from the shunt output mode 196A to the first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the first output level threshold and from the first output mode to the shunt output mode 196A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124. In addition, in some embodiments, the second state machine may be further configured to transition from the first output mode to the series output mode 198A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the series level threshold 126 and from the series output mode 198A to the first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the first output level threshold. In some alternative embodiments, the state machine may be configured to bypass the first output mode. For example, in some embodiments, the second state machine may transition from the series output mode 198A to first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the first output level threshold but transition directly from the shunt output mode 196A to the series output mode 190A when

the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the series level threshold 126. Conversely, in some embodiments, the second state machine may transition directly from the shunt output mode 195A to the series output mode 198A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than the series level threshold 126 but transition from the series output mode 198A to the first output mode when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the first output level threshold. In still other embodiments, the switcher control circuit 52A may configure the second state machine to bypass the first output mode based on an amount of time the multi-level charge pump circuit 56 has been in the first boost output mode, the second output boost mode, the first output mode, and/or a combination thereof. For example, the second state machine may bypass the first output mode after assertion of the minimum charge time indicator when the boost lockout counter 184 has not yet fully counted down to zero. For example, in some embodiments of the switcher control circuit 52, the boost time counter 186 is configured to count up when the state machine is in the first output mode, the first boost output mode 200A, and the second boost output mode 202A. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, for example 3 microseconds, the logic circuit 148A asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148A sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. For example, the boost lockout counter 184 may be configured to have a countdown that last at least 3 micro seconds to permit the first flying capacitor 100 and the second flying capacitor 102 to fully recharge before transitioning operating in the first boost output mode 200A, the second boost output mode 202A, or the first output mode. In other embodiments, the boost time counter 186 may be configured to keep track of the amount of time the multi-level charge pump circuit 56 is providing the switching voltage, V_{SW}, at the switching voltage output 26 of Figure 3A. For example, the boost time

counter 186 may be configured to count up when the second state machine is in first output mode, the first boost output mode 200A, and the second boost output mode 202A and countdown when the second state machine is in the series output mode 198A and the shunt output mode 196A. If the counter output of the boost time counter 186 is at least equal to the maximum boost time parameter, the logic circuit 148A asserts a minimum charge time indicator, which prevents the second state machine from transitioning to first output mode, the first boost output mode 200A, the second boost output mode 202A, or the first output mode until the minimum charge time indicator is de-asserted. As an alternative, the switcher control circuit 52A may configure the second state machine to bypass the first output mode based on an expected envelope characteristics of the signal to be transmitted, a frequency at which or a percentage of time the multi-level charge pump circuit 56 is providing the switching voltage, V_{SW}, and/or a measurement of a voltage across the first flying capacitor 100, the second flying capacitor 102, the first flying capacitor 100 and the second flying capacitor 102, average switching frequency of operation of the multi-level charge pump buck converter 12A, and/or a combination thereof. Although not discussed relative to the operation of the first state machine depicted in Figure 5A, the boost time counter 186 and the boost lockout counter 184 may be used to control whether the first state machine transitions into the first output mode.

[00335] The threshold and control circuit 132A further provides a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, which is a logic level representation of the switching voltage output, V_{SW}. The switching voltage output, $V_{SW_EST_OUT}$, may be based upon the $V_{SW_EST_CMOS_SIGNAL}$(s). In some embodiments of the threshold and control circuit 132A, the logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, may be asserted when the multi-level charge pump buck converter 12A is in either the series output mode, the first boost output mode, or the second boost output mode. The logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, is de-asserted when the multi-level charge pump buck converter 12A is in the shunt output mode.

[00336] Figure 3B depicts another embodiment of switcher control circuit 52, the switcher control circuit 52B, and another embodiment of the frequency locked loop circuit 54 of the multi-level charge pump buck converter 12A, frequency locked loop circuit 54B, which, for the sake of simplicity and not by way of limitation, will be described with continuing reference to the multi-level charge pump buck converter 12A of Figure 2A. The operation of the switcher control circuit 52B and the frequency locked loop circuit 54B will now be described.

[00337] Unlike the frequency locked loop circuit 54A depicted in Figure 3A, the frequency locked loop circuit 54B outputs a threshold scalar' 137B. Similar to the frequency locked loop circuit 54A, the frequency locked loop circuit 54B receives a clock reference signal 139A from a clock reference 139 and a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$. The frequency locked loop circuit 54B extracts the operating frequency of the multi-level charge pump buck converter 12A based upon the logic level indication of the switching voltage output, $V_{SW_EST_OUT}$. Thereafter, the frequency locked loop circuit 54B compares the extracted operating frequency of the multi-level charge pump buck converter 12A to the clock reference signal 139A to generate the threshold scalar' 137B. As an example, the frequency locked loop circuit 54B may be configured to adjust the magnitude of the threshold scalar' 137B to maintain an average switching frequency of operation of the multi-level charge pump buck converter 12A. For example, the threshold scalar' 137B may be configured to control the magnitude of each respective threshold level provide to the positive terminal of each of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 to maintain an average switching frequency of operation of the multi-level charge pump buck converter 12A. The controller 50 may configure the frequency locked loop circuit to derive a target average switching frequency of operation from the clock reference signal 139A based on a target average frequency of operation parameter. The frequency locked loop circuit 54B compares the extracted operating frequency of the multi-level charge pump buck converter 12A to the target average switching frequency of operation derived from the clock reference signal 139A to generate the

threshold scalar' 137B. Alternatively, the controller may configure the clock reference 139 to provide the frequency locked loop circuit 54B with a clock reference signal 139A based on the target average frequency of operation parameter, where the clock reference signal 139A has a frequency substantially equal to the target average switching frequency of operation. In this case, the frequency locked loop circuit 54B compares the extracted operating frequency of the multi-level charge pump buck converter 12A to the target average switching frequency of operation provided by the clock reference signal 139A to generate the threshold scalar' 137B. The magnitude of the threshold scalar' 137B may be used to adjust the operating frequency of the multi-level charge pump buck converter 12A. As will be discussed relative to the threshold detector and control circuit 132B of Figure 4B, the frequency locked loop circuit 54B provides the threshold scalar' 137B directly to a plurality of multiplier circuits, where the plurality of multiplier circuits includes a first multiplier circuit 168, a second multiplier circuit 170, a third multiplier circuit 172, and a fourth multiplier circuit 174. The first multiplier circuit 168, the second multiplier circuit 170, the third multiplier circuit 172, and the fourth multiplier circuit 174 may be used to scale the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130, respectively to generate a scaled shunt level threshold 176, a scaled series level threshold 178, a scaled first boost level threshold 180, and a scaled second boost level threshold 182, of Figure 4B. The scaled shunt level threshold 176, the scaled series level threshold 178, the scaled first boost level threshold 180, and the scaled second boost level threshold 182 may be used to control the operating frequency of the multi-level charge pump buck converter 12A.

[00338] As an example, the frequency locked loop circuit 54B may be configured to decrease the magnitude of the threshold scalar' 137B to decrease the magnitude of the scaled shunt level threshold 176, the scaled series level threshold 178, the scaled first boost level threshold 180, and the scaled second boost level threshold 182. As the magnitudes of the scaled shunt level threshold 176, the scaled series level threshold 178, the scaled first boost level

threshold 180, and the scaled second boost level threshold 182 decrease, the operating frequency of the multi-level charge pump buck converter 12A will tend to increase, which will tend to increase the power inductor current, I_{SW_OUT}, delivered by the power inductor 16.

[00339] The frequency locked loop circuit 54B may be configured to increase the magnitude of the threshold scalar' 137B to increase the magnitude of the scaled shunt level threshold 176, the scaled series level threshold 178, the scaled first boost level threshold 180, and the scaled second boost level threshold 182. As the scaled shunt level threshold 176, the scaled series level threshold 178, the scaled first boost level threshold 180, and the scaled second boost level threshold 182 are increased, the operating frequency of the multi-level charge pump buck converter 12A will tend to decrease, which will tend to decrease the power inductor current, I_{SW_OUT}, delivered by the power inductor 16. Alternatively, in some embodiments, the first output level threshold parameter is set to a value greater than the shunt level threshold parameter but less than the series level threshold parameter. In some embodiments, the switcher control circuit 52B may configure the multi-level charge pump buck converter 12A to operate at a desire average switching frequency. For example, in some embodiments of the switcher control circuit 52B, the threshold detector and control circuit 132B may determine the average frequency of operation based on the charge pump mode control signal 60, the series switch control signal 66, and the shunt switch control signal 68. In other embodiments, logic circuit 148B of the threshold detector and control circuit 132B, depicted in Figure 4B, may determine the average frequency of operation Based on the determined average frequency of operation, the controller 50 or the switcher control circuit 52 may configure or adjust the shunt level threshold parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12A to operate at a desired or target average switching frequency. In those embodiments having a multi-level charge pump circuit 56 that includes a first output mode of operation, the controller 50 or

the switcher control circuit 52 may configure or adjust the shunt level threshold parameter, the first output level threshold, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12A to operate at a desired or target average switching frequency.

[00340] Returning to Figure 3B, unlike the switcher control circuit 52A of Figure 3A, the switcher control circuit 52B includes a threshold detector and control circuit 132B. The switcher control circuit 52B omits the multiplier circuit 134. As will be discussed below relative to the threshold detector and control circuit 132B of Figure 4B, the summing circuit 136, is placed in the threshold detector and control circuit 132B.

[00341] Also, similar to the switcher control circuit 52A, the switcher control circuit 52B may also receive a mode switch control signal 131 from the controller 50. The mode switch control signal 131 may configure the threshold detector and control circuit 132B to operate the multi-level charge pump buck converter in different modes of operation. As an example, the mode switch control signal 131 may configure operation of a state machine within the threshold detector and control circuit 132B that governs how the switching voltage output 26 transitions the switching voltage output 26 to provide different output levels. As a first example embodiment of a state machine within the threshold detector and control circuit 132B, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12A to operate in a first mode of operation, depicted in Figure 5B. As another example embodiment of a state machine within the threshold detector and control circuit 132A, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12A to operate in a second mode of operation, depicted in Figure 6B.

[00342] Referring to Figure 4B, the frequency locked loop circuit 54B will now be discussed. Similar to frequency locked loop Circuit 54A of Figure 3A, the frequency locked loop circuit 54B may be configured to receive a clock reference signal 139A from the clock reference 139 and a logic level indication of the

switching voltage output, $V_{SW_EST_OUT}$, from the switcher control circuit 52B. The logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, may be provided by the logic circuit 148B of the threshold detector and control circuit 132B. As discussed above, the logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, is a logic level representation of the switching voltage output, V_{SW}.

[00343] The one embodiment of the threshold detector and control circuit 132B includes a first multiplier circuit 168, a second multiplier circuit 170, a third multiplier circuit 172, and a fourth multiplier circuit 174. The first multiplier circuit 168 may be configured to receive the shunt level threshold 124 and the receive threshold scalar' 137B. The first multiplier circuit 168 multiplies the shunt level threshold 124 by the received threshold scalar' 137B to generate a scaled shunt level threshold 176. The second multiplier circuit 170 may be configured to receive the series level threshold 126 and the threshold scalar' 137B. The second multiplier circuit 170 multiplies the series level threshold 126 by the threshold scalar' 137B to generate a scaled series level threshold 178. The third multiplier circuit 172 may be configured to receive the first boost level threshold 128 and the threshold scalar' 137B. The third multiplier circuit 172 may multiplies the first boost level threshold 128 by the threshold scalar' 137B to generate a scaled first boost level threshold 180. The fourth multiplier circuit 174 may be configured to receive the second boost level threshold 130 and the threshold scalar' 137B. The fourth multiplier circuit 174 multiplies the second boost level threshold 130 by the threshold scalar' 137B to generate the scaled second boost level threshold 182. The summing circuit 136 subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to generate a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', which may be used as a composite control signal for the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. As discussed before, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, may be used to control the offset voltage, V_{OFFSET}, that is generated across the coupling

circuit 18, as depicted in Figure 2A. In the case where the coupling circuit 18 is a wire, such that the parallel amplifier output 32A is directly coupled to the power amplifier supply output 28 , the V_{OFFSET} loop circuit 41 and the threshold offset current, $I_{THRESHOLD_OFFSET}$, are omitted such that I_{PAWA_COMP}' is the same as parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$.

[00344] The first comparator 140 includes a positive terminal coupled to the scaled shunt level threshold 176, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', and a first comparator output configured to generate a shunt level indication 150B, which is provided to the logic circuit 148B. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled shunt level threshold 176, the shunt level indication 150B is asserted by setting output of the first comparator 140 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled shunt level threshold 176, the shunt level indication 150B is de-asserted by setting output of the first comparator 140 to a digital logic high state. The second comparator 142 includes a positive terminal coupled to the scaled series level threshold 178, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', and a second comparator output configured to generate a series level indication 152B, which is provided to the logic circuit 148B. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled series level threshold 178, the series level indication 152B is asserted by setting output of the second comparator 142 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled series level threshold 178, the series level indication 152B is de-asserted by setting output of the second comparator 142 to a digital logic high state. The third comparator 144 includes a positive terminal coupled to the scaled first boost level threshold 180, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', and a third comparator output configured to generate a first boost level indication 154B,

which is provided to the logic circuit 148B. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than the scaled first boost level threshold 180, the first boost level indication 154B is asserted by setting output of the third comparator 144 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled first boost level threshold 180, the first boost level indication 154B is de-asserted by setting output of the third comparator 144 to a digital logic high state. The fourth comparator 146 includes a positive terminal coupled to the scaled second boost level threshold 182, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP} ', and a fourth comparator output configured to generate a second boost level indication 156B, which is provided to the logic circuit 148B. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than the scaled second boost level threshold 182, the second boost level indication 156B is asserted by setting output of the fourth comparator 146 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled second boost level threshold 182, the second boost level indication 156B is de-asserted by setting output of the fourth comparator 146 to a digital logic high state.

[00345] The logic circuit 148B will now be discussed. The logic circuit 148B is similar to the logic circuit 148A of Figure 4A. The example embodiment of the logic circuit 148B may include a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gates or transistor logic, discrete hardware components, or any combination thereof designed to perform. Some embodiments of the logic circuit 148B may be implemented in either a digital or analog processor. The logic circuit 148B generates the series switch control output 162, the shunt switch control output 164, the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), the charge pump mode control signal 60, and the logic level indication of the switching voltage output, $V_{SW_EST_OUT}$ in a similar fashion as the logic circuit 148A, which has been previously discussed.

[00346] The operation of the logic circuit 148B will now be discussed with continuing reference to Figures 2A, 3B, 4B, 5B, 6B, and 7A. Similar to the logic circuit 148A of Figure 4A, the logic circuit 148B may be digital or analog based logic configured for one or more state machines of the threshold detector and control circuit 132B. As an example embodiment, the logic circuit 148B (Figure 4B) may have a first state machine corresponding to a first mode of operation, depicted in Figure 5B and a second state machine corresponding to a second mode of operation, depicted in Figure 6B. Based on the mode switch control signal 131, depicted in Figure 3B, received by the threshold detector and control circuit 132B, the threshold detector and control circuit 132B may configure the logic circuit 148B to use the first state machine to govern operation of the multi-level charge pump buck converter using the first state machine of the logic circuit 148B, depicted in Figure 5B. Alternatively, the threshold detector and control circuit 132B may configure the logic circuit 148B to use the second state machine to govern operation of the multi-level charge pump buck converter using the second state machine of the logic circuit 148B, depicted in Figure 6B

[00347] Also similar to the logic circuit 148A, the logic circuit 148B may include a boost lockout counter 184 and a boost time counter 186. The boost time counter 186 may be used to keep track of the time that the multi-level charge pump buck converter 12A is in either the first boost output mode or the second boost output mode. When the multi-level charge pump buck converter 12A is in either the first boost output mode or the second boost output mode, the multi-level charge pump circuit 56 (Figure 3B) is configured to be in either the first boost mode of operation or the second boost mode of operation, respectively. In one embodiment of the logic circuit 148B, when the logic circuit 148B determines that the multi-level charge pump buck converter 12A is in either the first boost output mode or the second boost output mode, the logic circuit 148B resets the counter output of the boost time counter 186 and enables the boost time counter 186 to begin counting up. The logic circuit 148B compares the counter output of the boost time counter 186 to a maximum boost time parameter, which may be provided by the controller 50. If the counter output of the boost time

counter 186 is equal to or exceeds the maximum boost time parameter before the multi-level charge pump buck converter 12A is configured to return to either the shunt output mode of operation or the series output mode of operation, the logic circuit 148B asserts a minimum charge time indicator. However, if the multi-level charge pump buck converter 12A returns to either the series output mode of operation or the shunt output mode of operation while the counter output of the boost time counter 186 is less than the maximum boost time parameter, the logic circuit 148B de-asserts the minimum charge time indicator.

[00348] Similar to the boost lockout counter 184 of the logic circuit 148A, the boost lockout counter 184 of the logic circuit 148B may be a count-down timer that is used to ensure that the multi-level charge pump circuit 56, depicted in Figure 3B, remains in a charging mode of operation for a minimum charge time period after the multi-level charge pump circuit 56 has been in either the first boost mode of operation or the second boost mode of operation. This permits the first flying capacitor 100 and the second flying capacitor 102 of Figure 7A a sufficient amount of time to charge before the multi-level charge pump circuit 56 transitions again into either the first boost mode of operation or the second boost mode of operation. Similar to the logic circuit 148A, the minimum charge time period may be a parameter provided by the controller 50 via the control bus 44 to the logic circuit 148B. Operationally, after the multi-level charge pump buck converter 12A transitions from either the first boost output mode or the second boost output mode to either the shunt output mode of operation or the series output mode of operation, the logic circuit 148B determines whether the minimum charge time indicator is asserted. If the minimum charge time indicator is asserted, the logic circuit 148B sets the count value of the boost lockout counter 184 to equal the minimum charge time period and enables the boost lockout counter 184 to begin counting down. Once the boost lockout counter 184 counts down to zero, the logic circuit 148B is configured to de-assert the minimum charge time indicator.

[00349] Operation of the first state machine implemented in the logic circuit 148B, depicted in Figure 5B, will now be described. The first state

machine includes a shunt output mode 188B, a series output mode 190B, a first boost output mode 192B, and a second boost output mode 194B.

[00350] In the shunt output mode 188B, the logic circuit 148B (Figure 4B) configures the series switch control output 162 such that the series switch 70 (Figure 3B) is in an open state (not conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in a closed state (conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3B) to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3B is configured to provide a switching voltage, V_{SW}, substantially equal to ground. In response to assertion of the series level indication 152B, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled series level threshold 178, the logic circuit 148B configures the first state machine to transition to the series output mode 190B. Otherwise, the first state machine remains in the shunt output mode 188B.

[00351] In the series output mode 190B, the logic circuit 148B configures the series switch control output 162 such that the series switch 70 is in a closed state (conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3B is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}.

[00352] In response to de-assertion of the shunt level indication 150B (Figure 4B), which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled shunt level threshold 176, the logic circuit 148B configures the first state machine to transition to the shunt output mode 188B (Figure 5B). However, in response to assertion of the first boost level indication 154B which indicates that the compensated parallel

amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled first boost level threshold 180, the logic circuit 148B configures the first state machine to transition to the first boost output mode 192B. Otherwise, the first state machine remains in the series output mode 190B.

[00353] In the first boost output mode 192B, the logic circuit 148B (Figure 4B) configures the series switch control output 162 such that the series switch 70 (Figure 3B) is in an open state (not conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3B is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the shunt level indication 150B (Figure 4B), which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled shunt level threshold 176, the logic circuit 148B configures the first state machine to transition to the shunt output mode 188B (Figure 5B). However, in response to assertion of the second boost level indication 156B, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled second boost level threshold 182, the logic circuit 148B configures the first state machine to transition to the second boost output mode 194B. Otherwise, the first state machine remains in the first boost output mode 192B.

[00354] In the second boost output mode 194B, the logic circuit 148B (Figure 4B) configures the series switch control output 162 such that the series switch 70 (Figure 3B) is in an open state (not conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3B

is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}. In response to de-assertion of the shunt level indication 150B, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled shunt level threshold 176, the first state machine transitions to the shunt output mode 188B. Otherwise, the first state machine remains in the second boost output mode 194B.

[00355] Operation of the second state machine of the logic circuit 148B (Figure 3B), which is depicted in Figure 6B, will now be described. The second state machine includes a shunt output mode 196B, a series output mode 198B, a first boost output mode 200B, and a second boost output mode 202B. In addition, the second state machine uses the above-described boost lockout counter 184 and boost time counter 186 of the logic circuit 148B.

[00356] In the shunt output mode 196B, the logic circuit 148B, depicted in Figure 4B, configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in a closed state (conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56, depicted in Figure 2A, to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3B is configured to provide a switching voltage, V_{SW}, substantially equal to ground. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to assertion of the series level indication 152B, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled series level threshold 178, the second state machine transitions to the series output mode 198B. Otherwise, the second state machine remains in the shunt output mode 196B.

[00357] In the series output mode 198B, the logic circuit 148B (Figure 4B) configures the series switch control output 162 such that the series switch 70 is in a closed state (conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not

conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3B is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to de-assertion of the shunt level indication 150B, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled shunt level threshold 176, the logic circuit 148B configures the second state machine to transition to the shunt output mode 196B. However, in response to assertion of the first boost level indication 154B which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP},' is greater than or equal to the scaled first boost level threshold 180, the logic circuit 148B determines whether both the minimum charge time indicator is de-asserted and the first boost level indication 154B is asserted. If the minimum charge time indicator is de-asserted and the first boost level indication 154B is asserted, the logic circuit 148B configures the second machine to transition to the first boost output mode 200B. Otherwise, the logic circuit 148B prevents the second state machine from transitioning to the first boost output mode 200B until the minimum time indicator is de-asserted. Once both the minimum charge time indicator is de-asserted and the first boost level indication 154B is asserted, the logic circuit 148B configures the second state machine to transition to the first boost output mode 200B, resets the counter output of the boost time counter 186, and enables the boost time counter 186 to begin counting up. Otherwise, the second state machine remains in the series output mode 198B.

[00358] In the first boost output mode 200B, the logic circuit 148B configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first

boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3B is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the first boost level indication 154B, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled first boost level threshold 180, the logic circuit 148B configures the second state machine to transition to the series output mode 198B. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148B asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148B sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. However, in response to assertion of the second boost level indication 156B which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled second boost level threshold 182, the logic circuit 148B configures the second state machine to transition to the second boost output mode 202B. Otherwise, the second state machine remains in the first boost output mode 200B.

[00359] In the second boost output mode 202B, the logic circuit 148B configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148B also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148B configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3B is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}.

[00360] In response to de-assertion of the first boost level indication 154B which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the scaled first boost level threshold 180, the logic circuit 148B configures the second state machine to transition to the series

output mode 198B. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148B asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148B sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. Otherwise, the second state machine remains in the second boost output mode 202B.

[00361] Figure 3C depicts an embodiment of the pseudo-envelope follower power management system 10B, depicted in Figure 1B, that does not include a frequency locked loop circuit. The embodiment of the pseudo-envelope follower power management system 10B that do not include a frequency locked loop circuit may include a switcher control circuit 52C, which, for the sake of simplicity and not by way of limiation, will be described with continuing reference to the multi-level charge pump buck converter 12B depicted in Figure 2B. The switcher control circuit 52C may include a threshold detector and control circuit 132C, which is similar to the threshold detector and control circuit 132B of Figure 3B. However, unlike threshold detector and control circuit 132B, the threshold detector and control circuit 132C may not be configured to provide the logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, to a frequency locked loop circuit. Likewise, unlike threshold detector and control circuit 132B, the threshold detector and control circuit 132C may not be configured to receive a threshold scalar from a frequency locked loop circuit. Even so, in some embodiments, in some embodiments, the switcher control circuit 52C may configure the multi-level charge pump buck converter 12A to operate at a desire average switching frequency. For example, in some embodiments of the switcher control circuit 52C, the threshold detector and control circuit 132C may determine the average frequency of operation based on the charge pump mode control signal 60, the series switch control signal 66, and the shunt switch control signal 68. In other embodiments, logic circuit 148C of the threshold detector and control circuit 132C, depicted in Figure 4C, may determine the average frequency of operation Based on the determined average frequency of operation, the controller 50 or the switcher control circuit 52 may configure or

adjust the shunt level threshold parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12A to operate at a desired or target average switching frequency. In those embodiments having a multi-level charge pump circuit 56 that includes a first output mode of operation, the controller 50 or the switcher control circuit 52 may configure or adjust the shunt level threshold parameter, the first output level threshold, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12A to operate at a desired or target average switching frequency.

[00362] Figure 4C depicts an embodiment of the threshold detector and control circuit 132C. Similar to the threshold detector and control circuit 132B of Figure 4B, the threshold detector and control circuit 132C includes a summing circuit 136 configured to receive the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, generated by the parallel amplifier circuit. The summing circuit 136 subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to generate a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', which may be used as a composite control signal for the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. As discussed before, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, may be used to control the offset voltage, V_{OFFSET}, which is generated across the coupling circuit 18, as depicted in Figure 1A. In the case where the coupling circuit 18 is a wire, such that the parallel amplifier output 32A is directly coupled to the power amplifier supply output 28 , the V_{OFFSET} loop circuit 41 and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, are omitted such that I_{PAWA_COMP}' is the same as the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$.

[00363] As depicted in Figure 4C, with continuing reference to Figures 1A, 2A and 3C, the threshold detector and control circuit 132C may include a first comparator 140, a second comparator 142, a third comparator 144, a fourth comparator 146, and a logic circuit 148C. The example embodiment of the logic circuit 148C may include a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gates or transistor logic, discrete hardware components, or any combination thereof designed to perform. Some embodiments of the logic circuit 148C may be implemented in either a digital or analog processor.

[00364] The first comparator 140 includes a positive terminal coupled to the shunt level threshold 124, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', and a first comparator output configured to generate a shunt level indication 150C, which is provided to the logic circuit 148C. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the shunt level threshold 124, the shunt level indication 150C is asserted by setting output of the first comparator 140 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the shunt level threshold 124, the shunt level indication 150C is de-asserted by setting output of the first comparator 140 to a digital logic high state. The second comparator 142 includes a positive terminal coupled to the series level threshold 126, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP},' and a second comparator output configured to generate a series level indication 152C, which is provided to the logic circuit 148C. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP},' is greater than or equal to the series level threshold 126, the series level indication 152C is asserted by setting output of the second comparator 142 to a digital logic low state. When the compensated parallel amplifier cir0cuit output current estimate, I_{PAWA_COMP},' is less than the series level threshold 126, the series level indication 152C is de-asserted by setting output of the second comparator 142 to a digital logic high state. The third

comparator 144 includes a positive terminal coupled to the first boost level threshold 128, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', and a third comparator output configured to generate a first boost level indication 154C which is provided to the logic circuit 148C. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than the first boost level threshold 128, the first boost level indication 154C is asserted by setting output of the third comparator 144 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP},' is less than the first boost level threshold 128, the first boost level indication 154C is de-asserted by setting output of the third comparator 144 to a digital logic high state. The fourth comparator 146 includes a positive terminal coupled to the second boost level threshold 130, a negative terminal coupled to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP},' and a fourth comparator output configured to generate a second boost level indication 156C, which is provided to the logic circuit 148C. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP},' is greater than the second boost level threshold 130, the second boost level indication 156C is asserted by setting output of the fourth comparator 146 to a digital logic low state. When the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP},' is less than the second boost level threshold 130, the second boost level indication 156C is de-asserted by setting output of the fourth comparator 146 to a digital logic high state.

[00365] Similar to the logic circuit 148A of Figure 4A and the logic circuit 148B of Figure 4B, the logic circuit 148C of Figure 4C may be configured to generate a charge pump mode control signal 60, a series switch control output 162 provided to the first output buffer 158, a shunt switch control output 164 provided to the second output buffer 160, one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), provided to the third output buffer 161, and an estimated switching voltage output 38B, V_{SW_EST}. As previously described, the series switch control output 162, a shunt switch control output 164, and the

one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, may be configured to operate with the first output buffer 158, the second output buffer 160, and the third output buffer 161 to generate the series switch control signal 66, the shunt switch control signal 68, and the estimated switching voltage output 38B, V_{SW_EST}, respectively. Similar to the logic circuit 148A of Figure 4A and the logic circuit 148B of Figure 4B, the logic circuit 148C may include a boost lockout counter 184 and a boost time counter 186. The operation of the boost lockout counter 184 and a boost time counter 186 of the logic circuit 148C is substantially similar to the operation of the boost lockout counter 184 and a boost time counter 186 of the logic circuit 148A and 148B of Figures 4A and 4B, respectively.

[00366] Similar to the threshold detector and control circuit 132A of Figure 4A and the threshold detector and control circuit 132B of Figure 4B, the threshold detector and control circuit 132C may be configured to receive a mode switch control signal 131 from the controller 50, as depicted in Figure 3C, in order to configure the logic circuit 148C to operate the multi-level charge pump buck converter in different modes of operation. As an example, the mode switch control signal 131 may configure operation of a state machine within the threshold detector and control circuit 132C that governs how the switching voltage output 26 transitions the switching voltage output 26 to provide different output levels. As a first example embodiment of a state machine within the threshold detector and control circuit 132C, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12B to operate in a first mode of operation, depicted in Figure 5C. As another example embodiment of a state machine within the threshold detector and control circuit 132C, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12B to operate in a second mode of operation, depicted in Figure 6C.

[00367] The operation of the logic circuit 148C will now be discussed with continuing reference to Figures 2A, 3C, 4C, 5C, 6C, and 7A. Similar to the logic circuit 148A of Figure 4A and the logic circuit 148B of Figure 4B, the logic

circuit 148C may be digital or analog based logic configured for one or more state machines of the threshold detector and control circuit 132C.

[00368] Operation of the first state machine implemented in the logic circuit 148C, depicted in Figure 5C, will now be described. The first state machine includes a shunt output mode 188C, a series output mode 190C, a first boost output mode 192C, and a second boost output mode 194C.

[00369] In the shunt output mode 188C, the logic circuit 148C (Figure 4C) configures the series switch control output 162 such that the series switch 70 (Figure 3C) is in an open state (not conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72 is in a closed state (conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3C) to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to ground. In response to assertion of the series level indication 152C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the series level threshold 126, the logic circuit 148C configures the first state machine to transition to the series output mode 190C. Otherwise, the state machine remains in the shunt output mode 188C.

[00370] In the series output mode 190C, the logic circuit 148C configures the series switch control output 162 such that the series switch 70 is in a closed state (conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}.

[00371] In response to de-assertion of the shunt level indication 150C (Figure 4C), which indicates that the compensated parallel amplifier circuit output

current estimate, I_{PAWA_COMP}', is less than the shunt level threshold 124, the logic circuit 148C configures the first state machine to transition to the shunt output mode 188C (Figure 5C). However, in response to assertion of the first boost level indication 154C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the first boost level threshold 128, the logic circuit 148C configures the first state machine to transition to the first boost output mode 192C. Otherwise, the first state machine remains in the series output mode 190C.

[00372] In the first boost output mode 192C, the logic circuit 148C (Figure 4C) configures the series switch control output 162 such that the series switch 70 (Figure 3C) is in an open state (not conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the shunt level indication 150C (Figure 4C), which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the shunt level threshold 124, the logic circuit 148C configures the first state machine to transition to the shunt output mode 188C (Figure 5C). However, in response to assertion of the second boost level indication 156C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the second boost level threshold 130, the logic circuit 148C configures the first state machine to transition to the second boost output mode 194C. Otherwise, the first state machine remains in the first boost output mode 192C.

[00373] In the second boost output mode 194C, the logic circuit 148C (Figure 4C) configures the series switch control output 162 such that the series switch 70 (Figure 3C) is in an open state (not conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72

is in an open state (not conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}. In response to de-assertion of the shunt level indication 150C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the shunt level threshold 124, the first state machine transitions to the shunt output mode 188C. Otherwise, the state machine remains in the second boost output mode 194C.

[00374] Operation of the second state machine of the logic circuit 148C, depicted in Figure 6C, will now be described. The second state machine includes a shunt output mode 196C, a series output mode 198C, a first boost output mode 200C, and a second boost output mode 202C. In addition, the second state machine uses the above-described boost lockout counter 184 and boost time counter 186 of the logic circuit 148C.

[00375] In the shunt output mode 196C, the logic circuit 148C (Figure 4C) configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72 is in a closed state (conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3C) to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to ground. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to assertion of the series level indication 152C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the series level threshold 126, the second state machine transitions to the series output mode 198C. Otherwise, the second state machine remains in the shunt output mode 196C.

[00376] In the series output mode 198C, the logic circuit 148C (Figure 4C) configures the series switch control output 162 such that the series switch 70 is in a closed state (conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to de-assertion of the shunt level indication 150C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the shunt level threshold 124, the logic circuit 148C configures the second state machine to transition to the shunt output mode 196C. However, in response to assertion of the first boost level indication 154C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the first boost level threshold 128, the logic circuit 148C determines whether both the minimum charge time indicator is de-asserted and the first boost level indication 154C is asserted. If the minimum charge time indicator is de-asserted and the first boost level indication 154C is asserted, the logic circuit 148C configures the second machine to transition to the first boost output mode 200C. Otherwise, the logic circuit 148C prevents the second state machine from transitioning to the first boost output mode 200C until the minimum time indicator is de-asserted. Once both the minimum charge time indicator is de-asserted and the first boost level indication 154C is asserted, the logic circuit 148C configures the second state machine to transition to the first boost output mode 200C, resets the counter output of the boost time counter 186, and enables the boost time counter 186 to begin counting up. Otherwise, the second state machine remains in the series output mode 198C.

[00377] In the first boost output mode 200C, the logic circuit 148C configures the series switch control output 162 such that the series switch 70 is in an open

state (not conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3C) to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the first boost level indication 154C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the first boost level threshold 128, the logic circuit 148C configures the second state machine to transition to the series output mode 198C. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148C asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148C sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. However, in response to assertion of the second boost level indication 156C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the second boost level threshold 130, the logic circuit 148C configures the second state machine to transition to the second boost output mode 202C. Otherwise, the second state machine remains in the first boost output mode 200C.

[00378] In the second boost output mode 202C, the logic circuit 148C configures the series switch control output 162 such that the series switch 70 (Figure 3C) is in an open state (not conducting). The logic circuit 148C also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3C) is in an open state (not conducting). In addition, the logic circuit 148C configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3C) to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the

switching voltage output 26 of Figure 3C is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}.

[00379] In response to de-assertion of the first boost level indication 154C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the first boost level threshold 128, the logic circuit 148C configures the second state machine to transition to the series output mode 198C. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148C asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148C sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. Otherwise, the second state machine remains in the second boost output mode 202C.

[00380] The threshold and control circuit 132C further provides a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, which is a logic level representation of the switching voltage output, V_{SW}. The switching voltage output, $V_{SW_EST_OUT}$, may be based upon the $V_{SW_EST_CMOS_SIGNAL}$(s). In some embodiments of the threshold and control circuit 132C, the logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, may be asserted when the multi-level charge pump buck converter 12B is in either the series output mode, the first boost output mode, or the second boost output mode. The logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, is de-asserted when the multi-level charge pump buck converter 12B is in the shunt output mode of operation.

[00381] By way of example, and not by limitation, Figure 3D depicts an embodiment of the pseudo-envelope follower power management system 10B of Figure 1B that includes neither a frequency locked loop circuit nor a V_{OFFSET} loop circuit 41. In addition, Figure 3D depicts another embodiment of the pseudo-envelope follower power management system 10B, depicted in Figure 1B, where the coupling circuit 18 is a wire and the parallel amplifier output 32A of the parallel amplifier circuit 14 is directly coupled to the power amplifier supply output 28. Other embodiments of the pseudo-envelope follower power

management system 10B of Figure 1B that include the circuitry depicted in Figure 3D may include a coupling circuit 18 that does not directly couple the output of the parallel amplifier output 32A to the power amplifier supply output 28 , V_{CC}. In those cases, the circuitry depicted in Figure 3D may be included in a parallel amplifier circuit 14, of Figure 1A, that includes a V_{OFFSET} loop circuit 41.

[00382] Figure 3D depicts an embodiment of the multi-level charge pump buck converter having a switcher control circuit 52D, which is similar to the switcher control circuit 52C depicted in Figure 3C and, for the sake of simplicity but not by way of limitation, will be described with continuing reference to the multi-level charge pump buck converter 12B of Figure 2B. However, unlike the switcher control circuit 52C, the switcher control circuit 52D includes a threshold detector and control circuit 132D that is not configured to receive the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the parallel amplifier circuit 14.

[00383] Similar to the threshold detector and control circuit 132A of Figure 4A, the threshold detector and control circuit 132B of Figure 4B, and the threshold detector and control circuit 132C of Figure 4C, the threshold detector and control circuit 132D of Figure 4D may be configured to receive mode switch control signal 131, depicted in Figure 3D, from the controller 50 in order to configure the logic circuit 148D to operate the multi-level charge pump buck converter in different modes of operation. A threshold detector and control circuit 132D that governs how the switching voltage output 26 transitions the switching voltage output 26 to provide different output levels. As a first example embodiment of a first state machine within the threshold detector and control circuit 132D, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12 to operate in a first mode of operation, depicted in Figure 5D. As another example embodiment a second state machine within the threshold detector and control circuit 132D, the mode switch control signal 131 may configure the multi-level charge pump buck converter 12 to operate in a second mode of operation, depicted in Figure 6D. In addition, some embodiments of the switcher control circuit 52D may configure the multi-level charge pump buck converter 12B to operate at a desire average switching frequency. For example,

in some embodiments of the switcher control circuit 52D, the threshold detector and control circuit 132D may determine the average frequency of operation based on the charge pump mode control signal 60, the series switch control signal 66, and the shunt switch control signal 68. In other embodiments, logic circuit 148D of the threshold detector and control circuit 132D, depicted in Figure 4D, may determine the average frequency of operation Based on the determined average frequency of operation, the controller 50 or the switcher control circuit 52 may configure or adjust the shunt level threshold parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12D to operate at a desired or target average switching frequency. In those embodiments having a multi-level charge pump circuit 56 that includes a first output mode of operation, the controller 50 or the switcher control circuit 52 may configure or adjust the shunt level threshold parameter, the first output level threshold, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter to increase or decrease the average switching frequency of the multi-level charge pump buck converter 12D to operate at a desired or target average switching frequency.

[00384] One embodiment of the threshold detector and control circuit 132D is depicted in Figure 4D. The threshold detector and control circuit 132D is similar to the threshold detector and control circuit 132A, depicted in Figure 4A, except the logic circuit 148A is replace by a logic circuit 148D and the parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is replaced by the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. As discussed above, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, may include the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}. However, in some embodiments of the parallel amplifier circuit that do not include the open loop assist circuit 39, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, only includes the scaled parallel amplifier output current estimate,

$I_{PARA_AMP_SENSE}$, generated by the parallel amplifier sense circuit 36 of the parallel amplifier circuitry 32, as above described.

[00385] The threshold detector and control circuit 132D of Figure 4D will be described with continuing reference to Figure 3D. The threshold detector and control circuit 132D may include a first comparator 140, a second comparator 142, a third comparator 144, a fourth comparator 146, and a logic circuit 148D. The example embodiment of the logic circuit 148D may include a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gates or transistor logic, discrete hardware components, or any combination thereof designed to perform. Some embodiments of the logic circuit 148D may be implemented in either a digital or analog processor.

[00386] The first comparator 140 includes a positive terminal coupled to the shunt level threshold 124, a negative terminal coupled to the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and a first comparator output is configured to generate a shunt level indication 150D, which is provided to the logic circuit 148D. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the shunt level threshold 124, the shunt level indication 150D is asserted by setting output of the first comparator 140 to a digital logic low state. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the shunt level threshold 124, the shunt level indication 150D is de-asserted by setting output of the first comparator 140 to a digital logic high state. The second comparator 142 includes a positive terminal coupled to the series level threshold 126, a negative terminal coupled to the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and a second comparator output is configured to generate a series level indication 152D, which is provided to the logic circuit 148D. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the series level threshold 126, the series level indication 152D is asserted by setting output of the second comparator 142 to a digital logic low state. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the series level threshold 126, the series level indication 152D is de-asserted by

setting output of the second comparator 142 to a digital logic high state. The third comparator 144 includes a positive terminal coupled to the first boost level threshold 128, a negative terminal coupled to the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and a third comparator output is configured to generate a first boost level indication 154D, which is provided to the logic circuit 148D. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than the first boost level threshold 128, the first boost level indication 154D is asserted by setting output of the third comparator 144 to a digital logic low state. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the first boost level threshold 128, the first boost level indication 154D is de-asserted by setting output of the third comparator 144 to a digital logic high state. The fourth comparator 146 includes a positive terminal coupled to the second boost level threshold 130, a negative terminal coupled to the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and a fourth comparator output is configured to generate a second boost level indication 156D, which is provided to the logic circuit 148D. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than the second boost level threshold 130, the second boost level indication 156D is asserted by setting output of the fourth comparator 146 to a digital logic low state. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the second boost level threshold 130, the second boost level indication 156D is de-asserted by setting output of the fourth comparator 146 to a digital logic high state.

[00387] Similar to the logic circuit 148A of Figure 4A, the logic circuit 148B of Figure 4B, and the logic circuit 148C of Figure 4C, the logic circuit 148D may also be configured to generate charge pump mode control signal, a series switch control output 162 provided to the first output buffer 158, a shunt switch control output 164 provided to the second output buffer 160, one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), provided to the third output buffer 161, and an estimated switching voltage output 38B, V_{SW_EST}. As previously described, the series switch control output 162, the shunt switch

control output 164, and the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), may be configured to operate with the first output buffer 158, the second output buffer 160, and the third output buffer 161 to generate the series switch control signal 66, the shunt switch control signal 68, and the estimated switching voltage output 38B, V_{SW_EST}, respectively. Also similar to the logic circuit 148A of Figure 4A, the logic circuit 148B of Figure 4B, and the logic circuit 148C of Figure 4C, the logic circuit 148D may include a boost lockout counter 184 and a boost time counter 186. The operation of the boost lockout counter 184 and the boost time counter 186 of the logic circuit 148D is substantially similar to the operation of the boost lockout counter 184 and the boost time counter 186 of the logic circuit 148A, the logic circuit 148B, and the logic circuit 148C, depicted in Figures 4A, 4B, and 4C, respectively.

[00388] The example embodiment of the logic circuit 148D may include a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gates or transistor logic, discrete hardware components, or any combination thereof designed to perform. Some embodiments of the logic circuit 148D may be implemented in either a digital or analog processor. In addition, the logic circuit 148D may include an embodiment of the first state machine and the second state machine of the threshold detector and control circuit 132D.

[00389] Operation of the first state machine implemented in the logic circuit 148D, depicted in Figure 5D, will now be described. The first state machine includes a shunt output mode 188D, a series output mode 190D, a first boost output mode 192D, and a second boost output mode 194D.

[00390] In the shunt output mode 188D, the logic circuit 148D (Figure 4D) configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in an open state (not conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in a closed state (conducting). In addition, the logic circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3D) to be in a charging mode of operation. As a

result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to ground. In response to assertion of the series level indication 152D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the series level threshold 126, the logic circuit 148D configures the first state machine to transition to the series output mode 190D. Otherwise, the state machine remains in the shunt output mode 188D.

[00391] In the series output mode 190D, the logic circuit 148D configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in a closed state (conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in an open state (not conducting). In addition, the logic circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}.

[00392] In response to de-assertion of the shunt level indication 150D (Figure 4D), which indicates that the power amplifier circuit output current estimate, $I_{PAWA_OUT_EST}$, is less than the shunt level threshold 124, the logic circuit 148D configures the first state machine to transition to the shunt output mode 188D (Figure 5D). However, in response to assertion of the first boost level indication 154D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the first boost level threshold 128, the logic circuit 148D configures the first state machine to transition to the first boost output mode 192D. Otherwise, the first state machine remains in the series output mode 190D.

[00393] In the first boost output mode 192D, the logic circuit 148D (Figure 4D) configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in an open state (not conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in an open state (not conducting). In addition, the logic

circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the shunt level indication 150D (Figure 4D), which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the shunt level threshold 124, the logic circuit 148D configures the first state machine to transition to the shunt output mode 188D (Figure 5D). However, in response to assertion of the second boost level indication 156D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the second boost level threshold 130, the logic circuit 148D configures the first state machine to transition to the second boost output mode 194D. Otherwise, the first state machine remains in the first boost output mode 192D.

[00394] In the second boost output mode 194D, the logic circuit 148D (Figure 4D) configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in an open state (not conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in an open state (not conducting). In addition, the logic circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}. In response to de-assertion of the shunt level indication 150D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the shunt level threshold 124, the first state machine transitions to the shunt output mode 188D. Otherwise, the state machine remains in the second boost output mode 194D.

[00395] Operation of the second state machine of the logic circuit 148D, depicted in Figure 6D, will now be described. The second state machine

includes a shunt output mode 196D, a series output mode 198D, a first boost output mode 200D, and a second boost output mode 202D. In addition, the second state machine uses the above-described boost lockout counter 184 and boost time counter 186 of the logic circuit 148D.

[00396] In the shunt output mode 196D, the logic circuit 148D (Figure 4D) configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in an open state (not conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in a closed state (conducting). In addition, the logic circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3D) to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to ground. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to assertion of the series level indication 152D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the series level threshold 126, the second state machine transitions to the series output mode 198D. Otherwise, the second state machine remains in the shunt output mode 196D.

[00397] In the series output mode 198D, the logic circuit 148D (Figure 4D) configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in a closed state (conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in an open state (not conducting). In addition, the logic circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to de-assertion of the shunt level indication 150D, which indicates that the parallel amplifier circuit output current estimate 40,

$I_{PAWA_OUT_EST}$, is less than the shunt level threshold 124, the logic circuit 148D configures the second state machine to transition to the shunt output mode 196D. However, in response to assertion of the first boost level indication 154D, which indicates that parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the first boost level threshold 128, the logic circuit 148D determines whether both the minimum charge time indicator is de-asserted and the first boost level indication 154D is asserted. If the minimum charge time indicator is de-asserted and the first boost level indication 154D is asserted, the logic circuit 148D configures the second machine to transition to the first boost output mode 200D. Otherwise, the logic circuit 148D prevents the second state machine from transitioning to the first boost output mode 200D until the minimum time indicator is de-asserted. Once both the minimum charge time indicator is de-asserted and the first boost level indication 154D is asserted, the logic circuit 148D configures the second state machine to transition to the first boost output mode 200D, resets the counter output of the boost time counter 186, and enables the boost time counter 186 to begin counting up. Otherwise, the second state machine remains in the series output mode 198D.

[00398] In the first boost output mode 200D, the logic circuit 148D configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in an open state (not conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in an open state (not conducting). In addition, the logic circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the first boost level indication 154D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the first boost level threshold 128, the logic circuit 148D configures the second state machine to transition to the series

output mode 198D. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148D asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148D sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. However, in response to assertion of the second boost level indication 156D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the second boost level threshold 130, the logic circuit 148D configures the second state machine to transition to the second boost output mode 202D. Otherwise, the second state machine remains in the first boost output mode 200D.

[00399] In the second boost output mode 202D, the logic circuit 148D configures the series switch control output 162 such that the series switch 70 (Figure 3D) is in an open state (not conducting). The logic circuit 148D also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3D) is in an open state (not conducting). In addition, the logic circuit 148D configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 (Figure 3D) to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3D is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}.

[00400] In response to de-assertion of the first boost level indication 154D, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the first boost level threshold 128, the logic circuit 148D configures the second state machine to transition to the series output mode 198D. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148D asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148D sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. Otherwise, the second state machine remains in the second boost output mode 202D.

[00401] With respect to the cases where the first state machine or the second state machine of the logic circuit 148A, the logic circuit 148B, the logic circuit 148C, and the logic circuit 148D depicted in the respective Figures 4A, 4B, 4C, and 4D, are configured to be in either the first boost output mode 192A, the first boost output mode 192B, the first boost output mode 192C, and the first boost output mode 192D, or the first boost output mode 200A, the first boost output mode 200B, the first boost output mode 200C, or the first boost output mode 200D, respectively, when the multi-level charge pump circuit 56 is configured to be in a first boost mode of operation, the first switch 86, the third switch 90, the fifth switch 94 and the seventh switch 98 of the multi-level charge pump circuit 56 are configured to be closed such that charge from the supply input 24, (V_{BAT}), the first flying capacitor 100 and the second flying capacitor 102, arranged in parallel, is provided directly to the switching voltage output 26 via the charge pump output 64 in order to provide substantially 3/2 x V_{BAT} at the switching voltage output 26. The second switch 88, the fourth switch 92, and the sixth switch 96, and the eighth switch 118 of the multi-level charge pump are configured to be open.

[00402] Similarly, with respect to the cases where the first state machine or the second state machine of the logic circuit 148A, the logic circuit 148B, the logic circuit 148C, and logic circuit 148D depicted in the respective Figures 4A, 4B, 4C, and 4D, are configured to be in either the second boost output mode 194A, the second boost output mode 194B, the second boost output mode 194C, and the second boost output mode 194D, or the second boost output mode 202A, the second boost output mode 202B, the second boost output mode 202C, and the second boost output mode 202D, when the multi-level charge pump circuit 56 is configured to be in a second boost mode of operation, the first switch 86, the fourth switch 92, and the fifth switch 94 are configured to be closed such that charge from the supply input 24, (V_{BAT}), the first flying capacitor 100 and the second flying capacitor 102, arranged in series, is provided directly to the switching voltage output 26 via the charge pump output 64 in order to provide substantially 2 x V_{BAT} at the switching voltage

output 26. The second switch 88, the third switch 90, the sixth switch 96, and the seventh switch 98 of the multi-level charge pump circuit 56 are configured to be open. In those embodiments of the multi-level charge pump circuit 56 that further include the eighth switch 118, the eighth switch 118 may also be configured to be open.

[00403] Advantageously, this permits the multi-level charge pump circuit 56 to provide either substantially 3/2 x V_{BAT} or substantially 2 x V_{BAT} at the switching voltage output 26 without the need for a charge pump output capacitor. Moreover, while some embodiments of the multi-level charge pump circuit 56 may include more than two flying capacitors or inductive components to provide boost voltage levels, some embodiments of the multi-level charge pump circuit 56 only include the first flying capacitor 100 and the second flying capacitor 102. Even more advantageously, some embodiments of the multi-level charge pump circuit 56 that further include an eighth switch 118, may provide an additional first output mode of operation to provide substantially 1/2 x V_{BAT} at the switching voltage output 26 using only the first flying capacitor 100 and the second flying capacitor 102.

[00404] Returning to Figure 2A, an example embodiment of the parallel amplifier circuit 14A includes the parallel amplifier circuitry 32. The parallel amplifier circuitry 32 includes a parallel amplifier 35 and a parallel amplifier sense circuit 36. The parallel amplifier 35 generates the parallel amplifier output voltage, V_{PARA_AMP}, at the parallel amplifier output 32A based on the difference between the compensated V_{RAMP} signal, V_{RAMP_C}, and the power amplifier supply voltage, V_{CC}. In addition, the parallel amplifier 35 outputs a parallel amplifier output current, I_{PARA_AMP}. The parallel amplifier sense circuit 36 may include one or more current mirror circuits that are in communication with the parallel amplifier 35 depending upon the operational blocks included in the example embodiment of the parallel amplifier circuit 14A. Based upon the parallel amplifier output current, I_{PARA_AMP}, the parallel amplifier sense circuit 36 generates a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, which provides an indication of the parallel amplifier output current, I_{PARA_AMP}. In

those embodiments of the parallel amplifier circuit 14A that include an open loop assist circuit 39, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is combined with the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}, from the open loop assist circuit 39 to generate the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, which is provided to the multi-level charge pump buck converter 12A. However, in those embodiments of the parallel amplifier circuit 14A that do not include an open loop assist circuit 39, only the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, may be provided as a contribution to form the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, provided to the multi-level charge pump buck converter 12A. In addition, as depicted in Figure 2A, in those embodiments of the parallel amplifier circuit 14A that include a parallel amplifier output impedance compensation circuit 37, a copy of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is provided to the parallel amplifier output impedance compensation circuit 37. However, in those embodiments of the parallel amplifier circuit 14A that do not include a parallel amplifier output impedance compensation circuit 37, the parallel amplifier sense circuit 36 is configured to only provide the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, as a contribution to the formation of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, provided to the multi-level charge pump buck converter 12A.

[00405] Figure 12A depicts one embodiment of the parallel amplifier 35 as the parallel amplifier 35A. The parallel amplifier 35A depicts one embodiment of an AB class amplifier. The parallel amplifier 35A includes a parallel amplifier input voltage 204, a first amplifier 206, AMP_A, the second amplifier 208, AMP_B, a first output stage 210, and an amplifier feedback node 212. The parallel amplifier input voltage 204 may be configured to receive either the V_{RAMP} signal or the compensated V_{RAMP} signal, V_{RAMP_C}.

[00406] The first amplifier 206, AMP_A, includes a positive input terminal 206A, a negative input terminal 206B, and an output terminal 206C. Regarding the first amplifier 206, AMP_A, the positive input terminal 206A may be coupled to the

parallel amplifier input voltage 204. The negative input terminal 206B may be coupled to the amplifier feedback node 212, which is coupled to the power amplifier supply voltage, V_{CC}. A first resistor, R_A, and a first capacitor, C_A, are arranged in series between the output terminal 206C and the amplifier feedback node 212. The first resistor, R_A, and the first capacitor, C_A, are a feedback network used to extend the operating bandwidth by compensating for the dominant pole introduced by the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19. The feedback network may be configured to extend the modulation bandwidth of the first amplifier 206, AMP_A, out to approximately 30MHz. The first amplifier 206, AMP_A, generates a first amplifier output voltage, V_A, at the output terminal 206C based upon the difference between the parallel amplifier input voltage 204 appearing at the positive input terminal 206A and the power amplifier supply voltage, V_{CC}, appearing at the negative input terminal 206B.

[00407] Regarding the second amplifier 208, AMP_B, the positive input terminal 208A may be coupled to the parallel amplifier input voltage 204. The negative input terminal 208B may be coupled to the amplifier feedback node 212, which is coupled to the power amplifier supply voltage, V_{CC}. A second resistor, R_B, and a second capacitor, C_B, are arranged in series between the output terminal 208C and the amplifier feedback node 212. The second resistor, R_B, and the second capacitor, C_B, are a feedback network used to extend the operating bandwidth by compensating for the dominant pole introduced by the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19. The feedback network may be configured to extend the modulation bandwidth of the second amplifier 208, AMP_B, out to approximately 30MHz. The second amplifier 208, AMP_B, generates a second amplifier output voltage, V_B, at the output terminal 208C based upon the difference between the parallel amplifier input voltage 204 appearing at the positive input terminal 208A and the power amplifier supply voltage, V_{CC}, appearing at the negative input terminal 208B.

[00408] The first output stage 210 includes a first switching element, SW_{1A}, 214 and a second switching element, SW_{1B}, 216. As a non-limiting example, some

embodiments of the first switching element, SW_{1A}, 214 and the second switching element, SW_{1B}, 216, may be a solid state based switch such as a field effect transistor, an insulator-on-semiconductor based transistor, or a bipolar based transistor. These transistors may operate mainly in Class-AB mode, thus near to linear operation, even though the transistors are referred to as switches. In one example embodiment, the first switching element 214, SW_{1A}, may be a PFET device having a drain 214D, a gate 214G, and a source 214S. Likewise, the second switching element 216, SW_{1B}, may be an NFET device having a drain 216D, a gate 216G, and a source 216S.

[00409] The source 214S of the first switching element 214, SW_{1A}, may be coupled to the parallel amplifier supply input 30, (V_{BAT}), of the multi-level charge pump buck converter 12. The drain 214D of the first switching element 214, SW_{1A}, may be coupled to the drain 216D of the second switching element 216, SW_{1B}, to form a parallel amplifier output node 218 that provides the parallel amplifier output voltage, V_{PARA_AMP}, of the parallel amplifier 35A. The source 216S of the second switching element 216, SW_{1B}, may be coupled to ground.

[00410] The gate 214G of the first switching element 214, SW_{1A}, may be coupled to the output terminal 206C of the first amplifier 206, AMP_A, in order to receive the first amplifier output voltage, V_A. Similarly, the gate 216G of the second switching element 216, SW_{1B}, may be coupled to the output terminal 208C of the second amplifier 208, AMP_B, in order to receive the second amplifier output voltage, V_B.

[00411] The parallel amplifier 35A may be configured to source current from the parallel amplifier output node 218 and sink current to the parallel amplifier output node 218 based upon the difference between the parallel amplifier input voltage 204 (either V_{RAMP} or V_{RAMP_C}) and the power amplifier supply voltage, V_{CC}. For example, when the power inductor current, I_{SW_OUT}, delivered by the power inductor 16 and the bypass capacitor current, I_{BYPASS_CAP}, delivered by the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19 are insufficient to supply the output current, I_{OUT}, to the linear radio frequency power

amplifier 22, the parallel amplifier 35A turns on the first switching element 214, SW_{1A}, to provide additional current through the coupling capacitor 18A to the power amplifier supply output 28. However, when the power inductor current, I_{SW_OUT}, delivered by the power inductor 16, and the bypass capacitor current, I_{BYPASS_CAP}, from the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19 exceed the desired level of output current, I_{OUT}, to be delivered to the linear radio frequency power amplifier 22, the parallel amplifier 35A turns on the second switching element 216, SW_{1B}, to shunt the excess current provided to the power amplifier supply output 28 to ground.

[00412] In the case, as depicted in Figures 2A and 2B, where the parallel amplifier circuit 14A includes an open loop assist circuit 39 providing an open loop assist circuit current, I_{ASSIST}, the parallel amplifier 35A compensates for either an excess of current or the lack of current supplied to the power amplifier supply output 28. As an example, when the power inductor current, I_{SW_OUT}, the open loop assist current, I_{ASSIST}, and the bypass capacitor current, I_{BYPASS_CAP}, deliver less than the desired level of output current, I_{OUT}, to the linear radio frequency power amplifier 22, the parallel amplifier 35 turns on the first switching element 214, SW_{1A}, to provide the additional current desired by the linear radio frequency power amplifier 22. As another example, when the power inductor current, I_{SW_OUT}, the open loop assist current, I_{ASSIST}, and the bypass capacitor current, I_{BYPASS_CAP}, deliver excess current to the power amplifier supply output 28, the parallel amplifier 35A turns on the second switching element 216, SW_{1B}, such that the excess current is shunted to ground.

[00413] Figure 12B depicts another embodiment of the parallel amplifier 35 as the rechargeable parallel amplifier 35B. Unlike the parallel amplifier 35A of Figure 12A, the rechargeable parallel amplifier 35B includes a second output stage 220A, a charge conservation capacitor 228, C_{AB}, and an output control circuit 230A.

[00414] The second output stage 220A includes a first switching element 222, SW_{2A}, and a second switching element 224, SW_{2B}. As a non-limiting example, some embodiments of the first switching element 222, SW_{2A}, and the second

switching element 224, SW_{2B}, may be a solid state based switch such as a field effect transistor, an insulator-on-semiconductor transistor, or a bipolar based transistor. These transistors operate mainly in Class-AB mode, thus near to linear operation, even though the transistors are referred to as switches. In one example embodiment, the first switching element 222, SW_{2A}, may be a PFET device having a drain 222D, a gate 222G, and a source 222S. Likewise, the second switching element 224, SW_{2B}, may be an NFET device having a drain 224D, a gate 224G, and a source 224S.

[00415] The source 222S of the first switching element 222, SW_{2A}, may be coupled to the charge conservation capacitor 228, C_{AB}. The drain 222D of the first switching element 222, SW_{2A}, and the drain 224D of the second switching element 224, SW_{2B}, may be coupled to the parallel amplifier output node 218 to provide the parallel amplifier output voltage, V_{PARA_AMP}, of the rechargeable parallel amplifier 35B. The source 224S of the second switching element 224, SW_{2B}, may be coupled to the charge conservation capacitor 228, C_{AB}. As will be explained in further detail below, the second switching element 224, SW_{2B}, of the second output stage 220A may be turned on to sink excess current provided to the power amplifier supply output 28, where charge is stored on the charge conservation capacitor 228, C_{AB}, to generate a saved charge voltage, V_{AB}. Similarly, when insufficient current is provided to the power amplifier supply output 28, the first switching element 222, SW_{2A}, may be turned on to provide additional current to the power amplifier supply output 28 from the charge conservation capacitor 228, C_{AB}.

[00416] In order to operate in the linear mode of operation, the range of operation of the first switching element 222, SW_{2A}, and the second switching element 224, SW_{2B}, must take into consideration a minimum headroom voltage, $V_{HEADROOM}$, of each device. As an example, the first switching element 222, SW_{2A}, may operate in the linear mode provided the parallel amplifier output node 218 that provides the parallel amplifier output voltage, V_{PARA_AMP}, is less than the saved charge voltage, V_{AB}, minus the minimum headroom voltage, $V_{HEADROOM}$. Similarly, the second switching element 224, SW_{2B}, may operate in

the linear mode provided the parallel amplifier output node 218 that provides the parallel amplifier output voltage, V_{PARA_AMP}, is greater than the saved charge voltage, V_{AB}, plus the minimum headroom voltage, $V_{HEADROOM}$.

[00417] The output control circuit 230A includes a first amplifier output V_A input, V_{A_IN}, a second amplifier output V_B input, V_{B_IN}, a V_{AB} input, V_{AB_IN}, and a V_{PARA_AMP} input, $V_{PARA_AMP_IN}$. The first amplifier output V_A input, V_{A_IN}, may be coupled to the output terminal 206C of the first amplifier 206, AMP_A, to receive the first amplifier output voltage, V_A. The second amplifier V_B input, V_{B_IN}, may be coupled to the output terminal 208C of the second amplifier 208, AMP_B, to receive the second amplifier output voltage, V_B. The V_{PARA_AMP} input, $V_{PARA_AMP_IN}$, may be coupled to the parallel amplifier output node 218 to receive the parallel amplifier output voltage, V_{PARA_AMP}. The V_{AB} input, V_{AB_IN}, may be coupled to the saved charge voltage, V_{AB}.

[00418] The output control circuit 230A may include a first switch control output, V_{SW1A}, a second switch control output, V_{SW2A}, a third switch control output, V_{SW2B}, and a fourth switch control output, V_{SW1B}. The first switch control output, V_{SW1A}, may be coupled to the gate 214G of the first switching element 214, SW_{1A}. The second switch control output, V_{SW2A}, may be coupled to the gate 222G of the first switching element 222, SW_{2A}. The third switch control output, V_{SW2B}, may be coupled to the gate 224G of the second switching element 224, SW_{2B}. The fourth switch control output, V_{SW1B}, may be coupled to the gate 216G of the second switching element 216, SW_{1B}.

[00419] The output control circuit 230A selectively couples the first amplifier output V_A input, V_{A_IN}, to either the first switch control output, V_{SW1A}, or the second switch control output, V_{SW2A}, based upon the minimum headroom voltage, $V_{HEADROOM}$, the saved charge voltage, V_{AB}, and the parallel amplifier output voltage, V_{PARA_AMP}. For example, when the parallel amplifier output voltage, V_{PARA_AMP}, is greater than the saved charge voltage, V_{AB}, minus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230A couples the first amplifier output V_A input, V_{A_IN}, to the first switch control output, V_{SW1A}, of the first output stage 210 and sets the second switch control output, V_{SW2A}, to

disable the first switching element 222, SW_{2A}, of the second output stage 220A. As an example, the output control circuit 230A may pull up the second switch control output, V_{SW2A}, to the saved charge voltage, V_{AB}. As a result, the first amplifier output voltage, V_A, is coupled to the gate 214G of the first switching element 214, SW_{1A}, of the first output stage 210.

[00420] However, when the parallel amplifier output voltage, V_{PARA_AMP}, is less than or equal to the saved charge voltage, V_{AB}, minus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230A couples the first amplifier output V_A input, V_{A_IN}, to the second switch control output, V_{SW2A}, and sets the first switch control output, V_{SW_1A}, to disable the first switching element 214, SW_{1A}, of the first output stage 210. As an example, the output control circuit 230A may pull up the first switch control output, V_{SW1A}, to the parallel amplifier supply input 30, (V_{BAT}). As a result, the first amplifier output voltage, V_A, is coupled to the gate 222G of the first switching element 222, SW_{2A}, of the second output stage 220A.

[00421] The output control circuit 230A also selectively couples the second amplifier output V_B input, V_{B_IN}, to either the third switch control output, V_{SW2B}, or the fourth switch control output, V_{SW1B}, based upon the minimum headroom voltage, $V_{HEADROOM}$, the saved charge voltage, V_{AB}, and the parallel amplifier output voltage, V_{PARA_AMP}. For example, when the parallel amplifier output voltage, V_{PARA_AMP}, is greater than the saved charge voltage, V_{AB}, plus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230A couples the V_B input, V_{B_IN}, to the third switch control output, V_{SW2B}, and sets the fourth switch control output, V_{SW1B}, to disable the second switching element 216, SW_{1B}. As an example, the output control circuit 230A may pull down the fourth switch control output, V_{SW1B}, to ground. As a result, the second amplifier output voltage, V_B, is coupled to the gate 224G of the second switching element 224, SW_{2B}, of the second output stage 220A.

[00422] However, when the parallel amplifier output voltage, V_{PARA_AMP}, is less than or equal to the saved charge voltage, V_{AB}, plus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230A couples the fourth switch

control output, V_{SW1B}, to the second amplifier V_B input, V_{B_IN}, and sets the third switch control output, V_{SW2B}, to disable the second switching element 224, SW_{2B}. As an example, the output control circuit 230A may pull down the third switch control output, V_{SW2B}, to ground.

[00423] Figure 12C depicts another embodiment of the parallel amplifier 35 as the rechargeable parallel amplifier 35C. The rechargeable parallel amplifier 35C of Figure 12C is similar to the rechargeable parallel amplifier 35B of Figure 12B. However, unlike rechargeable parallel amplifier 35B, rechargeable parallel amplifier 35C includes an output control circuit 230B instead of the output control circuit 230A and a second output stage 220B instead of the second output stage 220A. The output control circuit 230B further includes a V_{CC} input, V_{CC_IN}, that is coupled to the power amplifier supply output 28 in order to receive the power amplifier supply voltage, V_{CC}. In addition, unlike rechargeable parallel amplifier 35B, in the rechargeable parallel amplifier 35C, the drain 224D of the second switching element 224, SW_{2B}, is coupled to the power amplifier supply output 28 instead of being coupled to the parallel amplifier output node 218, which is now labeled as the parallel amplifier output node 218C. Furthermore, as will be explained, the operation of the output control circuit 230B is different from the operation of output control circuit 230A in order to accommodate the coupling of the drain 224D of the second switching element, SW_{2B}, 224 to the power amplifier supply output 28.

[00424] Similar to the rechargeable parallel amplifier 35B, the rechargeable parallel amplifier 35C must also take into consideration the minimum headroom voltage, $V_{HEADROOM}$, of the first switching element 222, SW_{2A}, and the second switching element 224, SW_{2B}, in order to assure the first switching element 222, SW_{2A}, and the second switching element 224, SW_{2B}, operate in the linear mode. However, because the drain 224D of the second switching element 224, SW_{2B} is coupled to the power amplifier supply output 28, the power amplifier supply voltage, V_{CC}, must also be considered.

[00425] Similar to the rechargeable parallel amplifier 35B, the first switching element 222, SW_{2A}, of the rechargeable parallel amplifier 35C may operate in the

linear mode provided the parallel amplifier output node 218C that provides the parallel amplifier output voltage, V_{PARA_AMP}, is less than the saved charge voltage, V_{AB}, minus the minimum headroom voltage, $V_{HEADROOM}$. However, unlike the rechargeable parallel amplifier 35B, the second switching element 224, SW_{2B}, of the rechargeable parallel amplifier 35C may operate in the linear mode provided the power amplifier supply voltage, V_{CC}, is greater than the saved charge voltage, V_{AB}, plus the minimum headroom voltage, $V_{HEADROOM}$. Because the power amplifier supply voltage, V_{CC}, tends to be higher than the parallel amplifier output voltage, V_{PARA_AMP}, the rechargeable parallel amplifier 35C may store additional charge on the charge conservation capacitor 228, C_{AB}, which increases the charge voltage, V_{AB}. As a result, the operating range of the first switching element 222, SW_{2A}, is also increased.

[00426] Similar to the output control circuit 230A of Figure 12B, the output control circuit 230B of Figure 12C selectively couples the first amplifier output V_A input, V_{A_IN}, to either the first switch control output, V_{SW1A}, or the second switch control output, V_{SW2A}, based upon the minimum headroom voltage, $V_{HEADROOM}$, the saved charge voltage, V_{AB}, and the parallel amplifier output voltage, V_{PARA_AMP}. For example, when parallel amplifier output voltage, V_{PARA_AMP}, is greater than the saved charge voltage, V_{AB}, minus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230B couples the first amplifier output V_A input, V_{A_IN}, to the first switch control output, V_{SW1A}, and sets the second switch control output, V_{SW2A}, to disable the first switching element 222, SW_{2A}, of the second output stage 220B. As an example, the output control circuit 230B may pull up the second switch control output, V_{SW2A}, to the saved charge voltage, V_{AB}. As a result, the first amplifier output voltage, V_A, is coupled to the gate 214G of the first switching element 214, SW_{1A}, of the first output stage 210C.

[00427] However, when the parallel amplifier output voltage, V_{PARA_AMP}, is less than or equal to the saved charge voltage, V_{AB}, minus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230B couples the first amplifier output V_A input, V_{A_IN}, to the second switch control output, V_{SW2A}, of the second

output stage 220B and sets the first switch control output, V_{SW1A}, to disable the first switching element 214, SW_{1A}, of the first output stage 210C. As an example, the output control circuit 230B may pull up the first switch control output, V_{SW1A}, to the parallel amplifier supply input 30, (V_{BAT}). As a result, the first amplifier output voltage, V_A, is coupled to the gate 222G of the first switching element 222, SW_{2A}, of the second output stage 220B.

[00428] However, different from the output control circuit 230A, the output control circuit 230B also selectively couples the second amplifier output V_B input, V_{B_IN}, to either the third switch control output, V_{SW2B}, or the fourth switch control output, V_{SW1B}, based upon the minimum headroom voltage, $V_{HEADROOM}$, the saved charge voltage, V_{AB}, and the power amplifier supply voltage, V_{CC}. For example, when the power amplifier supply voltage, V_{CC}, is greater than the saved charge voltage, V_{AB}, plus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230B couples the V_B input, V_{B_IN}, to the third switch control output, V_{SW2B}, and sets the fourth switch control output, V_{SW1B}, to disable the second switching element 216, SW_{1B}. As an example, the output control circuit 230B may pull down the fourth switch control output, V_{SW1B}, to ground. As a result, the second amplifier output voltage, V_B, is coupled to the gate 224G of the second switching element 224, SW_{2B}, of the second output stage 220B.

[00429] However, when the power amplifier supply voltage, V_{CC}, is less than or equal to the saved charge voltage, V_{AB}, plus the minimum headroom voltage, $V_{HEADROOM}$, the output control circuit 230B couples the fourth switch control output, V_{SW1B}, to the V_B input, V_{B_IN}, and sets the third switch control output, V_{SW2B}, to disable the second switching element 224, SW_{2B}. As an example, the output control circuit 230B may pull down the third switch control output, V_{SW2B}, to ground. As a result, the second amplifier output voltage, V_B, is coupled to the gate 216G of the second switching element 216, SW_{1B}, of the first output stage 210C.

[00430] While the embodiments of the parallel amplifier 35A, the rechargeable parallel amplifier 35B, and the rechargeable parallel amplifier 35C of Figures 12A, Figure 12B, and Figure 12C, respectively, depict that the

source 214S of the first switching element 214, SW_{1A}, of the first output stage 210 and first output stage 210C are coupled to parallel amplifier supply input 30, (V_{BAT}), this is by way of illustration and non-limiting. In some embodiments, the supply voltage provided to the parallel amplifier 35A, rechargeable parallel amplifier 35B, and the rechargeable parallel amplifier 35C of Figures 12A, Figure 12B, and Figure 12C, may be provided by a separate power supply not depicted herein. The separate power supply may provide other voltage levels to power or bias the respective parallel amplifier 35A, rechargeable parallel amplifier 35B, and the rechargeable parallel amplifier 35C. As a non-limiting example, the separate power supply may provide a parallel amplifier supply voltage substantially equal to 2 x V_{BAT}. Accordingly, in these example embodiments of the parallel amplifier 35A, the rechargeable parallel amplifier 35B, and the rechargeable parallel amplifier 35C, source 214S of the first switching element 214, SW_{1A}, of the first output stage 210 may be coupled to the parallel amplifier supply voltage substantially equal to 2 x V_{BAT}.

[00431] As an example, discussed relative to Figures 18A-D, Figure 12D depicts a parallel amplifier 35D that is similar to the parallel amplifier 35A. The parallel amplifier 35D may be further configured to use a parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$. In some embodiments, the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, may be configured to come from various power supply voltage generation circuits depending upon the needs of the linear radio frequency power amplifier 22. As depicted in Figures 18A-D, the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, may be provided by a µC charge pump circuit 262 or by the multi-level charge pump circuit 258 of multi-level charge pump buck converter 12C. In addition, as discussed below, in some embodiments of the µC charge pump circuit 262, the µC charge pump circuit 262 generates a µC charge pump output voltage, $V_{\mu C_OUT}$, that may be configured to provide various voltage levels dependent upon the mode of operation of the µC charge pump circuit 262.

[00432] As depicted in Figure 12D, unlike the parallel amplifier 35A of Figure 12A, the parallel amplifier 35D may be configured to use the parallel

amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, instead of the parallel amplifier supply input 30, (V_{BAT}), provided by the battery 20. The parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, may be a discrete ratio of the parallel amplifier supply input 30, (V_{BAT}), provided by the battery 20. In other embodiments, however, the voltage level provided by the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, may be programmatically selected depending upon the operational conditions of the mobile device or pseudo-envelope follower power management system.

[00433] For example, as depicted in Figure 12D, the source 214S of the first switching element 214, SW_{1A}, may be coupled to the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$. Although not depicted in Figure 12D, the circuitry associated with the first amplifier 206, AMP_A, and the second amplifier 208, AMP_B, may also be supplied by the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$.

[00434] As another example, Figure 12E depicts an embodiment of the rechargeable parallel amplifier 35E that is similar to the rechargeable parallel amplifier 35B depicted in Figure 12B. Unlike the rechargeable parallel amplifier 35B, the rechargeable parallel amplifier 35E is configured to use the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, instead of the parallel amplifier supply input 30, (V_{BAT}), provided by the battery 20.

[00435] Accordingly, unlike the rechargeable parallel amplifier 35B, the rechargeable parallel amplifier 35E is configured such that the source 214S of the first switching element 214, SW_{1A}, is coupled to the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$. Similar to the parallel amplifier 35D of Figure 12D, the rechargeable parallel amplifier 35E may also be reconfigured to use the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, as the supply voltage of the first amplifier 206, AMP_A, the second amplifier 208, AMP_B, and the output control circuit 230A.

[00436] Figure 12F depicts another embodiment of the rechargeable parallel amplifier 35C, of Figure 12C, as a rechargeable parallel amplifier 35F. Similar to the parallel amplifier 35D, depicted in Figure 12D, and the rechargeable parallel amplifier 35E, depicted in Figure 12E, the rechargeable parallel amplifier 35F is

configured to use the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, instead of the parallel amplifier supply input 30, (V_{BAT}), supplied by the battery 20. Also similar to the parallel amplifier 35D and the rechargeable parallel amplifier 35E, rechargeable parallel amplifier 35F may be configured such that the source 214S of the first switching element 214, SW_{1A}, may be coupled to the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, instead of the parallel amplifier supply input 30, (V_{BAT}). Also similar to the rechargeable parallel amplifier 35E, depicted in Figure 12E, the first amplifier 206, AMP_A, the second amplifier 208, AMP_B, and the output control circuit 230B may also be further configured to use the parallel supply voltage, $V_{SUPPLY_PARA_AMP}$, as a supply source instead of the parallel amplifier supply input 30, (V_{BAT}).

[00437] Returning to Figure 2A, the open loop assist circuit 39 will now be discussed. As discussed above, the parallel amplifier circuit output current, I_{PAWA_OUT}, may be a combination of the parallel amplifier output current I_{PARA_AMP}, and the open loop assist circuit, I_{ASSIST}. The open loop assist circuit 39 may be used to reduce the amount of current that the parallel amplifier 35 of the parallel amplifier circuitry 32 may need to source and sink in order to regulate the power amplifier supply voltage, V_{CC}. In particular, the parallel amplifier 35 may sink excess power inductor current, I_{SW_OUT}, which may generate a large voltage ripple on the power amplifier supply voltage, V_{CC}. The large voltage ripple on the power amplifier supply voltage, V_{CC}, can be due to the interaction of the power inductor current, I_{SW_OUT}, with the non-zero impedance of parallel amplifier 35 over frequency in the pass band of the pseudo-envelope follower power management system. The open loop assist current, I_{ASSIST}, provided by the open loop assist circuit 39 can be configured to reduce the parallel amplifier output current, I_{PARA_AMP}, sourced or sunk by the parallel amplifier 35, which may reduce the ripple voltage on the power amplifier supply voltage, V_{CC}, because the non-zero output impedance of the parallel amplifier 35 is convoluted with less current.

[00438] One embodiment of the open loop assist circuit 39 may be configured to receive an estimated power inductor inductance parameter, L_{EST}, and a minimum power amplifier turn on a voltage parameter, V_{OFFSET_PA}, an estimated

bypass capacitor capacitance parameter, C_{BYPASS_EST}, and an estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$.

[00439] The estimated power inductor inductance parameter, L_{EST}, may be either the measured or estimated inductance of the power inductor 16 between a specific range of frequencies. For example, the estimated power inductor inductance parameter, L_{EST}, may be either the measured or estimated inductance of the power inductor 16 between approximately 10MHz and 30MHz. The minimum power amplifier turn on voltage parameter, V_{OFFSET_PA}, may be either the measured or estimated value of the minimum supply voltage at which the linear radio frequency power amplifier 22 will begin to operate. The estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}, may be either the measured or estimate capacitance of the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19 measured between a specific range of frequencies. For example, the estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}, may be either the measured or estimated capacitance of the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19 between approximately 10MHz and 30MHz. The estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, may be either the measured or estimated transconductance of the linear radio frequency power amplifier 22. Transconductance of the linear radio frequency power amplifier 22 may be $1/R_{LOAD}$, where R_{LOAD}, is the estimated resistive load of the linear radio frequency power amplifier 22. The estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, may be either the measured or estimated transconductance of the linear radio frequency power amplifier 22 between a specific range of frequencies. For example, the estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, may be either the measured or estimated transconductance of the linear radio frequency power amplifier 22 between approximately 10MHz and 30MHz.

[00440] The estimated power inductor inductance parameter, L_{EST}, the minimum power amplifier turn on voltage parameter, V_{OFFSET_PA}, the estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}, and the estimated power

amplifier transconductance parameter, $K_I_{OUT_EST}$ may be provided by the controller 50 through the control bus 44, as depicted in Figures 1A and 1B. Typically, values of the estimated power inductor inductance parameter, L_{EST}, the minimum power amplifier turn on the voltage parameter, V_{OFFSET_PA}, the estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}, and the estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, are obtained at calibration time of the pseudo-envelope follower system.

[00441] In addition, the open loop assist circuit 39 may be configured to receive the feed forward control signal 38, $V_{SWITCHER}$, from the multi-level charge pump buck converter 12. As discussed above, the feed forward control signal 38, $V_{SWITCHER}$, may be configured to provide either the scaled switching voltage output 38A, V_{SW_SCALED}, or the estimated switching voltage output 38B, V_{SW_EST}. The open loop assist circuit 39 may also be configured to receive the V_{RAMP} signal, from the first control input 34.

[00442] Figure 9A depicts a more detailed block diagram of an embodiment of the open loop assist circuit 39 of Figure 2A, which is depicted as an open loop assist circuit 39A. The open loop assist circuit 39A will be described with continuing reference to Figures 1A and 2A. The open loop assist circuit 39A includes an output current estimator 240, a bypass capacitor current estimator 242, a power inductor current estimator 244A, a summing circuit 246, and a controlled current source 248. The output current estimator 240 receives the V_{RAMP} signal, the estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, and the minimum power amplifier turn on voltage parameter, V_{OFFSET_PA}. The output current estimator 240 generates an output current estimate, I_{OUT_EST}, based upon the V_{RAMP} signal, the estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, and the minimum power amplifier turn on voltage parameter, V_{OFFSET_PA}. The output current estimate, I_{OUT_EST}, is an estimate of the output current, I_{OUT}, provided to the linear radio frequency power amplifier 22.

[00443] In one embodiment, the output current estimator 240 calculates the difference between the V_{RAMP} signal and the minimum power amplifier turn on

voltage parameter, V_{OFFSET_PA}, by subtracting the minimum power amplifier turn on voltage parameter, V_{OFFSET_PA}, from the V_{RAMP} signal, (V_{RAMP} - V_{OFFSET_PA}). Thereafter, the difference between the V_{RAMP} signal and the minimum power amplifier turn on voltage parameter, V_{OFFSET_PA}, is scaled by the estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, to generate the output current estimate, I_{OUT_EST}, where the output current estimate, I_{OUT_EST}, substantially equals $K_I_{OUT_EST}$* (V_{RAMP} - V_{OFFSET_PA}). Typical circuitry may include an operational amplifier to perform (V_{RAMP} - V_{OFFSET_PA}) and the voltage difference is applied to a transconductance amplifier, which the transconductance amplifier gain, Gm, is programmable and equal to $K_I_{OUT_EST}$.

[00444] The bypass capacitor current estimator 242 receives the V_{RAMP} signal and the estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}. The bypass capacitor current estimator 242 generates a bypass capacitor current estimate, I_{BYPASS_EST}, based upon the V_{RAMP} signal and the estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}. The bypass capacitor current estimate, I_{BYPASS_EST}, is an estimate of the bypass capacitor current, I_{BYPASS_CAP}, delivered by the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19.

[00445] In one embodiment, the V_{RAMP} signal is differentiated to provide a V_{RAMP} rate of change signal, $d(V_{RAMP})/dT$, which serves as an estimate of the rate of change of the voltage across the bypass capacitor 19. The V_{RAMP} rate of change signal, $d(V_{RAMP})/dT$, may be an estimate of the rate of change of the V_{RAMP} signal over time. In some embodiments, the V_{RAMP} rate of change signal, $d(V_{RAMP})/dT$, is generated by a high pass filter having a desired time constant. A simple high-pass filter followed by a gain circuit provides a frequency response below its corner frequency that have a +6dB/octave slope thus equivalent to "s Laplace transform" and thus creating a differentiator function below the corner frequency. The high-pass filter is typically made of a series capacitor and a shunt resistor. In some embodiments, the time constant of the high pass filter may be between the range of 8 nanoseconds and 16 nanoseconds.

[00446] The power inductor current estimator 244A receives the V_{RAMP} signal, the feed forward control signal 38, $V_{SWITCHER}$, and the estimated power inductor inductance parameter, L_{EST}. The power inductor current estimator 244A generates a power inductor current estimate, $I_{SW_OUT_EST}$, based upon the V_{RAMP} signal, the feed forward control signal 38, $V_{SWITCHER}$, and the estimated power inductor inductance parameter, L_{EST}. The power inductor current estimate, $I_{SW_OUT_EST}$, is an estimate of the power inductor current, I_{SW_OUT}, delivered by the power inductor 16.

[00447] In one embodiment of the power inductor current estimator 244A, the power inductor current estimator 244A subtracts the V_{RAMP} signal from the feed forward control signal 38, $V_{SWITCHER}$, to generate a difference voltage, $V_{DIFFERENCE}$. The power inductor current estimator 244A may include an integrator circuit (not shown) that integrates the difference voltage $V_{DIFFERENCE}$ to generate an accumulated difference signal. The power inductor current estimator 244A then scales an accumulated difference signal with a factor of $1/L_{EST}$, to generate the power inductor current estimate, $I_{SW_OUT_EST}$. The bandwidth of the integrator circuit used to integrate the difference voltage $V_{DIFFERENCE}$ may be between 5 MHz and 45 MHz. In some embodiments, the integrator slope may be programmable. For example, the controller 50 may adjust the gain of the transistors of the integrator circuit (not shown) of the power inductor current estimator 244A in order to adjust the integrator slope. Also, it is possible to use a low-pass filter followed by a gain which above the corner frequency the slope versus frequency is -6dB/octave similar to "1/s Laplace transform" thus acting as an integrator in the frequencies above the corner frequency. The corner frequency can be set below 5MHz and is made programmable.

[00448] In another embodiment of the power inductor current estimator 244A the power inductor current estimator 244A divides the accumulated difference signal by the estimated power inductor inductance parameter, L_{EST}, to generate the power inductor current estimate, $I_{SW_OUT_EST}$.

[00449] In still another embodiment of the power inductor current estimator 244A, the difference voltage, $V_{DIFFERENCE}$, is scaled by the factor of $1/L_{EST}$, or divided by the estimated power inductor inductance parameter, L_{EST}, to generate a scaled difference signal, $S_{DIFFERENCE_SCALED}$, (not shown) prior to integration. The power inductor current estimator 244A then integrates a scaled difference signal, $S_{DIFFERENCE_SCALED}$, (not shown) to generate the power inductor current estimate, $I_{SW_OUT_EST}$. In yet another embodiment of the power inductor current estimator 244A, the power inductor current estimator 244A scales the V_{RAMP} signal and the feed forward control signal 38, $V_{SWITCHER}$, by the factor of $1/L_{EST}$, or divides the V_{RAMP} signal and the feed forward control signal 38, $V_{SWITCHER}$, by the estimated power inductor inductance parameter, L_{EST}, prior to calculating the scaled difference signal, $S_{DIFFERENCE_SCALED}$, (not shown). Thereafter, the scaled difference signal, $S_{DIFFERENCE_SCALED}$, is integrated to generate the power inductor current estimate, $I_{SW_OUT_EST}$.

[00450] When the feed forward control signal 38, $V_{SWITCHER}$, is configured to provide the estimated switching voltage output 38B, V_{SW_EST}, to the open loop assist circuit 39, the power inductor current estimate, $I_{SW_OUT_EST}$, is generated based upon the estimated switching voltage output 38B, V_{SW_EST}. When the feed forward control signal 38, $V_{SWITCHER}$, is configured to provide the scaled switching voltage output 38A, V_{SW_SCALED}, to the open loop assist circuit 39, the power inductor current estimate, $I_{SW_OUT_EST}$, is generated based upon the switching voltage output, V_{SW_SCALED}, 38A.

[00451] The summing circuit 246 is configured to receive the output current estimate, I_{OUT_EST}, the bypass capacitor current estimate, I_{BYPASS_EST}, and power inductor current estimate, $I_{SW_OUT_EST}$. The summing circuit 246 subtracts the bypass capacitor current estimate, I_{BYPASS_EST}, and the power inductor current estimate, $I_{SW_OUT_EST}$, from the output current estimate, I_{OUT_EST}, to generate an estimate of the open loop assist current, I_{ASSIST_EST}. The open loop assist current, I_{ASSIST_EST}, is an estimate of the open loop assist current, I_{ASSIST}, provided by the open loop assist circuit 39A to the parallel amplifier output 32A in order to

generate the parallel amplifier circuit output current, I_{PAWA_OUT}, from the parallel amplifier circuit 14.

[00452] The controlled current source 248 is a controlled current source that generates the open loop assist current, I_{ASSIST}, based upon the open loop assist current, I_{ASSIST_EST}. The open loop assist current can be activated when reduced voltage ripple reduction is required and can be disabled when voltage ripple reduction is not required such as when operating at lower power amplifier output power. The open loop assist current can be made of three separate controlled current sources, where each controlled current source is controlled by the power inductor current estimate, $I_{SW_OUT_EST}$, the bypass capacitor current estimate, I_{BYPASS_EST}, and the output current estimate, I_{OUT_EST}, respectively. Also, the open loop assist current, I_{ASSIST}, in phase may be time aligned with the parallel amplifier output current, I_{PARA_AMP}. For example, when the open loop assist current, I_{ASSIST}, is positive, parallel amplifier output current, I_{PARA_AMP}, may be positive and when the open loop assist current, I_{ASSIST}, is negative, the parallel amplifier output current, I_{PARA_AMP}, may also be negative as such there is no wasted currents, where the parallel amplifier output current, I_{PARA_AMP}, that is sourced is not sunk by the open loop assist circuit 39A.

[00453] Figure 9B depicts another embodiment of the open loop assist circuit 39B. As depicted in Figure 9B, the open loop assist circuit 39B is similar to the open loop assist circuit 39A except that the open loop assist circuit 39B receives the estimated switching voltage output 38B, V_{SW_EST}, as the feed forward control signal instead of the feed forward control signal 38, $V_{SWITCHER}$. Accordingly, the estimated switching voltage output 38B, V_{SW_EST}, includes a power inductor current estimator 244B instead of the power inductor current estimator 244A. The power inductor current estimator 244B is similar to the power inductor current estimator 244A except the power inductor current estimator 244B only receives estimated switching voltage output 38B, V_{SW_EST}, instead of the feed forward control signal 38, $V_{SWITCHER}$.

[00454] As a result, the power inductor current estimate, $I_{SW_OUT_EST}$, generated by the power inductor current estimator 244B is based upon the estimated

switching voltage output 38B, V_{SW_EST}. As a result, the power inductor current estimator 244B is functionally like the power inductor current estimator 244A when the feed forward control signal 38, $V_{SWITCHER}$, provides the estimated switching voltage output 38B, V_{SW_EST}, as an output. Accordingly, the open loop assist circuit 39B operates in a manner that is similar to the operation of the open loop assist circuit 39A when the feed forward control signal 38, $V_{SWITCHER}$, provides the estimated switching voltage output 38B, V_{SW_EST}, to the open loop assist circuit 39A.

[00455] Returning to Figure 2A, the parallel amplifier output impedance compensation circuit 37 will now be discussed. The combination of the multi-level charge pump buck converter 12 and the parallel amplifier 35 of the parallel amplifier circuitry 32 may not have a flat frequency response across the modulation bandwidth of the power amplifier supply voltage, V_{CC}, provided to the linear radio frequency power amplifier 22. In particular, the desired modulation bandwidth of the power amplifier supply voltage, V_{CC}, is between 3/2 to 2.5 times the radio frequency modulation bandwidth of the linear radio frequency power amplifier 22. As an example, the Long Term Evolution (LTE) 3GPP standard of the radio frequency modulation bandwidth may be up to 20MHz. As a result, the desired modulation bandwidth of power amplifier supply voltage, V_{CC}, generated by the pseudo-envelope follower power management system 10A may be between 30 MHz to 40MHz. In some embodiments of the pseudo-envelope follower power management system 10A, the desired modulation bandwidth of the power amplifier supply voltage, V_{CC}, may be approximately 35MHz. However, at higher frequencies, the output impedance of the parallel amplifier 35 that regulates the power amplifier supply voltage, V_{CC}, may become inductive. The output impedance of the parallel amplifier 35 combines with the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19 to roll off the modulation frequency response of the parallel amplifier 35. The roll off of the modulation frequency response of the parallel amplifier 35 may result in increased ripple voltage in the power amplifier supply voltage, V_{CC}, due to the power inductor current, I_{SW_OUT}, provided by the power inductor 16. The parallel

amplifier output impedance compensation circuit 37 may be configured to pre-compensate the V_{RAMP} signal in order to provide a compensated V_{RAMP} signal, V_{RAMP_C}, to the parallel amplifier 35 in order to flatten the modulation frequency response of the parallel amplifier 35.

[00456] The parallel amplifier output impedance compensation circuit 37 depicted in Figure 2A is configured to receive the V_{RAMP} signal, an estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}, and a parallel amplifier inductance estimate parameter, L_{CORR_EST}. The parallel amplifier inductance estimate parameter, L_{CORR_EST}, may be an estimated inductance of the parallel amplifier 35 between the frequencies 10MHz and 30MHz, which is measured during calibration. The parallel amplifier inductance estimate parameter, L_{CORR_EST}, may be provided by the controller 50 via the control bus 44 at configuration time.

[00457] Figure 10 depicts an example embodiment of the parallel amplifier output impedance compensation circuit 37, depicted in Figures 2A, as a parallel amplifier output impedance compensation circuit 37A. The parallel amplifier output impedance compensation circuit 37A may include a first differentiator circuit 250, a second differentiator circuit 252, a frequency pre-distortion circuit 254, and a summing circuit 256.

[00458] The first differentiator circuit 250 receives the V_{RAMP} signal and the estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}. Similar to the bypass capacitor current estimator 242 of Figures 9A and 9B, the first differentiator circuit 250 generates a bypass capacitor current estimate, I_{BYPASS_EST}, based upon the V_{RAMP} signal and the bypass capacitor capacitance parameter, C_{BYPASS_EST}. The bypass capacitor current estimate, I_{BYPASS_EST}, is an estimate of the bypass capacitor current, I_{BYPASS_CAP}, delivered by the bypass capacitor capacitance, C_{BYPASS}, of the bypass capacitor 19. In some embodiments of the parallel amplifier output impedance compensation circuit 37A, the parallel amplifier output impedance compensation circuit 37A uses the bypass capacitor current estimate, I_{BYPASS_EST}, provided by the bypass capacitor current estimator 242 and the first differentiator circuit 250 is omitted.

In other embodiments of the parallel amplifier output impedance compensation circuit 37A, the time constant of the first differentiator circuit 250 may be different than the time constant of bypass capacitor current estimator 242 of the open loop assist circuit 39.

[00459] Similar to the bypass capacitor current estimator 242, in one embodiment of the first differentiator circuit 250, the V_{RAMP} signal is differentiated to provide a V_{RAMP} rate of change signal, $d(V_{RAMP})/dT$, which serves as an estimate of the rate of change of the voltage across the bypass capacitor 19. The V_{RAMP} rate of change signal, $d(V_{RAMP})/dT$, may be an estimate of the rate of change of the V_{RAMP} signal over time. In some embodiments, the V_{RAMP} rate of change signal, $d(V_{RAMP})/dT$, is generated by a high pass filter (not shown) having a desired time constant. As an example, a simple high-pass filter followed by a gain stage may provide a frequency response below its corner frequency that has a +6dB/octave slope, thus equivalent to the "s Laplace transform" and thus creating a differentiator function below the corner frequency. The high-pass filter (not shown) is typically made of a series capacitor and a shunt resistor. In some embodiments, the time constant of the high pass filter may be between the range of 8 nanoseconds and 16 nanoseconds.

[00460] The bypass capacitor current estimate, I_{BYPASS_EST}, and the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, are combined to create a dynamic current, $I_{DYNAMIC}$, which is provided to the second differentiator circuit 252. In some embodiments, for example, a summing circuit (not shown) may be used to combine the bypass capacitor current estimate, I_{BYPASS_EST}, and the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, to create the dynamic current, $I_{DYNAMIC}$. In other embodiments, the second differentiator circuit 252 may create the dynamic current, $I_{DYNAMIC}$, based on the bypass capacitor current estimate, I_{BYPASS_EST}, and the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. The dynamic current, $I_{DYNAMIC}$, represents the dynamic portion of the power inductor current, I_{SW_OUT}, delivered by the power inductor 16. The second differentiator circuit 252 is to replicate the parallel amplifier output impedance frequency response, which exhibits an output

impedance that increases at +6dB/octave, like an inductor, at the frequency range where the switcher current is operating, up to a resonance frequency equal to $\frac{1}{2\pi\sqrt{L_{CORR}\times C_{BYPASS}}}$.

[00461] The second differentiator circuit 252 is configured to receive the dynamic current, $I_{DYNAMIC}$, and the parallel amplifier inductance estimate parameter, L_{CORR_EST}.

[00462] The second differentiator circuit 252 differentiates the dynamic current, $I_{DYNAMIC}$, to provide a dynamic current rate of change signal, $d(I_{DYNAMIC})/dT$. The dynamic current rate of change signal, $d(I_{DYNAMIC})/dT$, estimates change of the dynamic current, $I_{DYNAMIC}$, with respect to time. In some embodiments, the dynamic current rate of change signal, $d(I_{DYNAMIC})/dT$, is generated by a high pass filter (not shown) having a desired time constant. The time constants of the second differentiator circuit 252 may be configured to optimize the modulation bandwidth of the parallel amplifier 35. The second differentiator can be made from a high-pass filter (not shown) followed by a gain to provide a frequency response below its corner frequency that has a +6dB/octave slope thus equivalent to "s Laplace transform" and thus creating a differentiator function below the corner frequency. The high-pass filter is typically made of a series capacitor and a shunt resistor. The time constant of the high-pass filter may be between 8 nanoseconds and 16 nanoseconds. The second differentiator circuit 252 scales the dynamic current rate of change signal, $d(I_{DYNAMIC})/dT$, by the parallel amplifier inductance estimate parameter, L_{CORR}, to generate a power amplifier supply ripple voltage estimate, V_{RIPPLE}, at the negative input of the summing circuit 256. The power amplifier supply ripple voltage estimate is an estimate of the ripple voltage component of the power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28.

[00463] The frequency pre-distortion circuit 254 may be configured to receive the V_{RAMP} signal and output a peaked V_{RAMP} signal, V_{RAMP_PEAKED}, which is received by the positive terminal of the summing circuit 256. The summing circuit 256 subtracts the power amplifier supply ripple voltage estimate, V_{RIPPLE}, from the peaked V_{RAMP} signal to generate a compensated V_{RAMP} signal. The

frequency pre-distortion circuit 254 may be a programmable peaking filter that may be configured to compensate for the roll off of the modulation frequency response of the parallel amplifier 35. The frequency pre-distortion circuit 254 may include a frequency equalizer circuit that includes a programmable pole time constant, Tau_Pole, and a programmable zero time constant, Tau_Zero. The frequency pre-distortion circuit Laplace transfer function, V_{RAMP_C} / V_{RAMP}, may be approximately equal to [1+Tau_Zero*s] / [1+Tau_Pole*s]. The programmable pole time constant, Tau_Pole, and the programmable zero time constant, Tau_Zero, may be adjusted to increase the frequency response of the frequency pre-distortion circuit 254, V_{RAMP_C} / V_{RAMP}, in order to flatten the overall modulation frequency response of the pseudo-envelope follower power management system 10A. In some embodiments of the frequency pre-distortion circuit 254, the programmable pole time constant, Tau_Pole, is configured to about .4 microseconds, (1/2.5MHz). The programmable zero time constant, Tau_Zero, may be configured to be about .192 microseconds, (1/5.8MHz). As a result, the pseudo-envelope follower power management system transfer function, V_{CC} / V_{RAMP}, may be flattened up to about 35MHz.

[00464] Figure 13 depicts an embodiment of a pseudo-envelope follower power management system 10G including a buck converter 13G and a parallel amplifier circuit 14G having an open loop assist circuit 39 and parallel amplifier circuitry 32. In some alternative embodiments of the pseudo-envelope follower power management system of Figure 13, the parallel amplifier 35 may be a rechargeable parallel amplifier. As an example, the parallel amplifier 35 may be a rechargeable parallel amplifier similar to the embodiments of the rechargeable parallel amplifier depicted in Figures 12B-C and Figures 12E-F.

[00465] Figure 14 depicts another embodiment of a pseudo-envelope follower power management system 10H including a multi-level charge pump buck converter 12H and a parallel amplifier circuit 14H having an open loop assist circuit 39 and parallel amplifier circuitry 32. In some alternative embodiments of the pseudo-envelope follower power management system of Figure 14, the parallel amplifier 35 may be a rechargeable parallel amplifier similar to the

embodiments of the rechargeable parallel amplifier depicted in Figures 12B-C and Figures 12E-F.

[00466] Figure 15 depicts another embodiment of a pseudo-envelope follower power management system 10I including a multi-level charge pump buck converter 12I and a parallel amplifier circuit 14I having a parallel amplifier circuitry 32 and a V_{OFFSET} loop circuit 41E. In some embodiments, the V_{OFFSET} loop circuit 41E may be similar to the V_{OFFSET} loop circuit 41A, depicted in Figure 18A, the V_{OFFSET} loop circuit 41B, depicted in Figure 18B, or the V_{OFFSET} loop circuit 41, depicted in Figure 8. Accordingly, although not shown in Figure 15, in some example embodiments, the V_{OFFSET} loop circuit 41E may be coupled to a controller 50, in a fashion similar to that depicted in Figures 18A-B. In those embodiments that include the controller 50 coupled to the V_{OFFSET} loop circuit 41E, the controller 50 may be used to configure the V_{OFFSET} loop circuit 41E. In addition, in some alternative embodiments of the pseudo-envelope follower power management system 10I, depicted in Figure 15, the parallel amplifier 35 may be a rechargeable parallel amplifier similar to the embodiments of the rechargeable parallel amplifier that are depicted in Figures 12B-C and Figures 12E-F.

[00467] Figure 16 depicts another embodiment of a pseudo-envelope follower power management system 10J including a multi-level charge pump buck converter 12J and parallel amplifier circuitry 32 having a parallel amplifier circuitry 32, a V_{OFFSET} loop circuit 41F, an open loop assist circuit 39 and a parallel amplifier output impedance compensation circuit 37. In some embodiments, the V_{OFFSET} loop circuit 41F may be similar to the V_{OFFSET} loop circuit 41A, depicted in Figure 18A, the V_{OFFSET} loop circuit 41B, depicted in Figure 18B, or the V_{OFFSET} loop circuit 41, depicted in Figure 8. Accordingly, although not shown in Figure 16, the V_{OFFSET} loop circuit 41F may be coupled to a controller 50, (as depicted in Figures 18A-B), which may be used to configure the V_{OFFSET} loop circuit 41F. In addition, in some alternative embodiments of the pseudo-envelope follower power management system 10J, depicted in Figure 16, the parallel amplifier 35 may be a rechargeable parallel amplifier

similar to the embodiments of the rechargeable parallel amplifier depicted in Figures 12B-C and Figures 12E-F.

[00468] Figure 17A depicts another embodiment of a pseudo-envelope follower power management system 10K including a buck converter 13K and parallel amplifier circuitry 32 having a rechargeable parallel amplifier 35B. The parallel amplifier output current, I_{PARA_AMP}, may be the sole contributor to the parallel amplifier circuit output current I_{PAWA_OUT}, of the parallel amplifier circuit 14K. In addition, because the parallel amplifier circuit 14K does not have an open loop assist circuit, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is equal to the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, current provided by the parallel amplifier sense circuit 36. Also, in some alternative embodiments of the pseudo-envelope follower power management system 10K, depicted in Figure 17A, the rechargeable parallel amplifier 35B may be a rechargeable parallel amplifier similar to the embodiments of the rechargeable parallel amplifier depicted in Figure 12E.

[00469] Figure 17B depicts another embodiment of a pseudo-envelope follower power management system 10L including a multi-level charge pump buck converter 12L and a parallel amplifier circuitry 32 having a parallel amplifier circuitry 32. The parallel amplifier output current, I_{PARA_AMP}, may be the sole contributor to the parallel amplifier circuit output current I_{PAWA_OUT}, of the parallel amplifier circuit 14L. In addition, because the parallel amplifier circuit 14L does not have an open loop assist circuit, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, may be equal to the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, current provided by the parallel amplifier sense circuit 36. In addition, in some alternative embodiments of the pseudo-envelope follower power management system 10L, depicted in Figure 17B, the rechargeable parallel amplifier 35C may be a rechargeable parallel amplifier similar to the embodiments of the rechargeable parallel amplifier depicted in Figure 12E-F.

[00470] Figure 18B depicts another embodiment of the pseudo-envelope follower power management system 10E, which is similar to the pseudo-

envelope follower power management systems 10A and 10B, as depicted in Figures 1A-B and 2A-B. The pseudo-envelope follower power management system 10E includes a multi-level charge pump buck converter 12C, a parallel amplifier circuit 14D, a controller 50, a clock management circuit 260, a μC charge pump circuit 262, a battery level sense circuit 264, and a parallel amplifier power source selection circuit 272 operably configured to generate a parallel amplifier supply voltage, V_{CC}, on the bypass capacitor 19. The bypass capacitor 19 has a bypass capacitance, C_{BYPASS}.

[00471] Similar to the embodiments of the pseudo-envelope follower power management system 10A-10B of Figures 2A-2B, the pseudo-envelope follower power management system 10E may include a multi-level charge pump buck converter 12C that is similar to the multi-level charge pump buck converters 12A-B, depicted in Figures 2A-B. Like the multi-level charge pump buck converters 12A-B, the multi-level charge pump buck converter 12C may include a switcher control circuit 52. However, unlike the multi-level charge pump buck converters 12A-B, the multi-level charge pump buck converter 12C further includes a multi-level charge pump circuit 258 configured to generate an internal charge pump node parallel amplifier supply 294. In some embodiments of the multi-level charge pump buck converter 12C, the multi-level charge pump circuit 258 may provide 3/2 x V_{BAT} as the internal charge pump node parallel amplifier supply 294. In other embodiments of the multi-level charge pump buck converter 12C, the multi-level charge pump circuit 258, the output voltage level of the internal charge pump node parallel amplifier supply 294 may vary between 3/2 x V_{BAT} and 2 x V_{BAT} depending upon the operational mode of the multi-level charge pump circuit 258. Example embodiments of the multi-level charge pump circuit 258 may include the multi-level charge pump circuit 258A and the multi-level charge pump circuit 258B, depicted in the respective Figures 7A-B. Also similar to the multi-level charge pump buck converters 12A-B, depicted in Figures 2A-B, the multi-level charge pump buck converter 12C may include a switching voltage output 26.

[00472] In addition, similar to the embodiments of the pseudo-envelope follower power management system 10A-10B, depicted in Figures 2A-2B, the switching voltage output 26 of the multi-level charge pump buck converter 12C may be coupled to a power inductor 16. The power inductor 16 is coupled to the bypass capacitor 19, which has a bypass capacitance, C_{BYPASS}, to form a low pass filter for the multi-level charge pump buck converter 12C. In addition, similar to the parallel amplifier circuit 14A and the parallel amplifier circuit 14B of Figures 2A-2B, the parallel amplifier circuit 14D may include a parallel amplifier output 32A that is coupled to the power amplifier supply voltage, V_{CC}, via the coupling circuit 18. In the case where the coupling circuit 18 provides AC (alternating current) coupling between the parallel amplifier output 32A of the parallel amplifier circuit 14D and the power amplifier supply voltage, V_{CC}, an offset voltage, V_{OFFSET}, may be developed across the coupling circuit 18. Also, the parallel amplifier circuit 14D may include the parallel amplifier circuitry 32 operably coupled to the parallel amplifier output 32A.

[00473] However, unlike the parallel amplifier circuit 14A, depicted in Figure 2A, and the parallel amplifier circuit 14B, depicted in Figure 2B, the parallel amplifier circuit 14D may be configured to power the parallel amplifier circuitry 32 with a parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, instead of the supply input 24, (V_{BAT}). The parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, may be provided by the parallel amplifier power source selection circuit 272. In one example embodiment of the parallel amplifier circuit 14D, the parallel amplifier 35 may be configured similar to the parallel amplifier 35D, depicted in Figure 12D. Alternatively, in other embodiments, the parallel amplifier 35 may be a rechargeable parallel amplifier similar to the rechargeable parallel amplifiers 35E-F, respectively depicted in Figures 12E-F.

[00474] The parallel amplifier power source selection circuit 272 may include a first input coupled to the µC charge pump output of the µC charge pump circuit 262 and a second input coupled to the internal charge pump node parallel amplifier supply 294 of the multi-level charge pump circuit 258. The parallel amplifier power source selection circuit 272 may also be coupled to the

controller 50 via a source selection control signal 296. The parallel amplifier power source selection circuit 272 may include an output configured to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, to the parallel amplifier circuit 14D based upon the state of the source selection control signal 296. In addition, the parallel amplifier power source selection circuit 272 may be coupled to the controller 50 via the source selection control signal 296. Via the source selection control signal 296, the controller 50 may configure the parallel amplifier power source selection circuit 272 to select either the internal charge pump node parallel amplifier supply 294 or the µC charge pump output in order to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, to the parallel amplifier circuit 14D. In some alternative embodiments of the pseudo-envelope follower power management system 10E, the parallel amplifier power source selection circuit 272 may be eliminated. In this case, either the internal charge pump node parallel amplifier supply 294 or the µC charge pump output of the µC charge pump circuit 262 may be directly coupled to the parallel amplifier circuit 14D in order to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$. For example, some embodiments of the multi-level charge pump buck converter 12C may not provide an internal charge pump node parallel amplifier supply 294 as an output. In this case, the µC charge pump output of the µC charge pump circuit 262 is directly coupled to the parallel amplifier circuit 14D to provide the parallel amplifier supply voltage $V_{SUPPLY_PARA_AMP}$, as the operational voltage for the parallel amplifier 35 and associated circuitry.

[00475] In still another alternative arrangement (not shown), some embodiments of the pseudo-envelope follower power management system 10E may eliminate the parallel amplifier power source selection circuit 272. In this case, the µC charge pump output of the µC charge pump circuit 262 and the internal charge pump node parallel amplifier supply 294 are coupled together to form a parallel amplifier supply node that provides the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$. As an example, in the case where the multi-level charge pump circuit 258 is similar to either the multi-level charge pump circuit 258A, depicted in Figure 7B, or the multi-level charge pump circuit 258B,

depicted in Figure 7C, the desired source for providing the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, may be managed by enabling and disabling the µC charge pump circuit 262 and controlling the switch state of the ninth switch 119 of either the multi-level charge pump circuit 258A or the multi-level charge pump circuit 258B. As an example, when the µC charge pump circuit 262 is disabled by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to OFF, the µC charge pump output floats. In a similar fashion, setting the switch state of the ninth switch 119 to be open, for either the multi-level charge pump circuit 258A or the multi-level charge pump circuit 258B, depicted in the respective Figures 7B-C, operably disconnects the internal circuitry of the multi-level charge pump circuit 258A and the multi-level charge pump circuit 258B from the parallel amplifier supply node.

[00476] The µC charge pump circuit 262 includes a supply input coupled to supply input 24, (V_{BAT}), provided by the battery and a µC charge pump output configured to provide a µC charge pump output voltage, $V_{\mu C_OUT}$. In addition, the µC charge pump circuit 262 may be configured to receive a µC charge pump clock 276 from the clock management circuit 260. The µC charge pump clock 276 may be used to govern the operation of the µC charge pump circuit 262. The µC charge pump circuit 262 is also coupled via a µC charge pump control bus 278 to the controller 50. As described below relative to Figures 19A-B, some embodiments of the µC charge pump circuit 262 may be configured to boost the supply input 24, (V_{BAT}), provided by the battery to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, that is greater than the supply input 24, (V_{BAT}). Other embodiments of the µC charge pump circuit 262 be may be configured to buck the supply input 24, (V_{BAT}) to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, that is less than the supply input 24, (V_{BAT}). The controller 50 may use the µC charge pump control bus 278 to configure the µC charge pump circuit 262 to operate in various operational modes in order to generate specific voltage levels at the µC charge pump output. For example, the µC charge pump circuit 262 may be configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, that provides various voltage levels dependent upon the

mode of operation of the μC charge pump circuit 262. This permits the multi-level charge pump buck converter 12C to provide a desired voltage level as the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, and/or the μC charge pump circuit 262 to provide the μC charge pump output voltage, $V_{\mu C_OUT}$, as the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, and dependent upon the need of the parallel amplifier 35 of the parallel amplifier circuit 14D with different voltage output levels dependent upon the needs of the pseudo-envelope follower power management system 10E, depicted in Figure 18B. For example, the controller 50 may determine whether to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, from the μC charge pump circuit 262 or the based on the internal charge pump node parallel amplifier supply 294 based on a minimum parallel amplifier supply voltage. The minimum parallel amplifier supply voltage may be based on the expected envelope characteristics of the signal to be transmitted.

[00477] The clock management circuit 260, depicted in Figure 18B, may include a clock reference 139, a divider circuit 266, a clock selection circuit 268, and an oscillator 270. The clock management circuit 260 may be coupled to controller 50 via various control signals and/or buses. Based upon control inputs received from the controller 50, the clock management circuit 260 may be configured to generate a μC charge pump clock 276, which is provided to the μC charge pump circuit 262. The controller 50 may configure the clock management circuit 260 to generate the μC charge pump clock 276 based upon a variety of clock sources.

[00478] The clock reference 139 may be operably configured to provide a clock reference signal 139A to the frequency locked loop circuit 54 of the multi-level charge pump buck converter 12C. The frequency locked loop circuit 54 may be configured to operate with the clock reference 139 similar to the operational description of the frequency locked loop circuit 54A of Figure 3A or the frequency locked loop circuit 54B of Figure 3B. In each case, as depicted in Figures 3A and 3B, the clock reference 139 may be configured to provide a clock reference signal 139A to the frequency locked loop circuit 54A or the frequency locked loop

circuit 54B. In addition to governing various timing aspects regarding operation of the multi-level charge pump buck converter 12C, similar to the frequency locked loop circuit 54A of Figure 3A, some embodiments of the frequency locked loop circuit 54 may be configured to provide a threshold scalar 137A signal, as depicted in or discussed in reference to Figure 3A, to adjust the operating frequency of the multi-level charge pump buck converter 12C. Alternatively, in other embodiments of the frequency locked loop circuit 54, similar to the frequency locked loop circuit 54B, depicted in Figure 3B, the frequency locked loop circuit 54 may be configured to provide a threshold scalar' 137B signal, as depicted in Figure 3B, to adjust the operating frequency of the multi-level charge pump buck converter 12C.

[00479] In addition, as depicted in Figure 18B, the frequency locked loop circuit 54 may be further configured to provide a frequency locked loop system clock 280 to the switcher control circuit 52 and the divider circuit 266. The frequency locked loop system clock 280 may be synchronized or based upon the operating frequency of the multi-level charge pump buck converter 12C, as previously described. As a result, in some embodiments of the pseudo-envelope follower power management system 10E, the frequency locked loop circuit 54 provides a frequency locked loop system clock 280 that is synchronized to the switching of the multi-level charge pump buck converter 12C.

[00480] The divider circuit 266 may be configured to receive a clock divider control signal 284 from the controller 50. Based upon the clock divider control signal 284 received from the controller 50, the divider circuit 266 may divide the frequency locked loop generated clock to provide a divided frequency locked loop clock 282 to the clock selection circuit 268. In addition, the clock selection circuit 268 may be configured to receive the clock reference signal 139A from the clock reference 139 and an oscillator reference clock 288 from the oscillator 270. Alternative embodiments of the multi-level charge pump buck converter 12C may not include a frequency locked loop circuit 54 or the frequency locked loop circuit 54 may not be configured to provide a frequency locked loop system clock 280 to the clock management circuit 260.

[00481] The oscillator 270 may be operably coupled to the controller 50 via an oscillator control signal 286. In some embodiments, the oscillator 270 may be a free running oscillator. In other embodiments, the controller 50 may be configured to modify the output frequency of the oscillator 270 via the oscillator control signal 286. The controller 50 may be further configured to disable or enable the oscillator 270 in order to reduce noise generated by the clock management circuit 260. In other embodiments of the clock management circuit 260, the oscillator 270 may be a fixed oscillator.

[00482] Accordingly, the controller 50 may configure the clock selection circuit 268 to provide one of the divided frequency locked loop clock 282, the clock reference signal 139A, or the oscillator reference clock 288 to the μC charge pump clock 276. As discussed below relative to Figures 19A-B, example embodiments of the μC charge pump circuit 262 may use the μC charge pump clock 276 to govern the timing between phases of operation of the μC charge pump circuit 262.

[00483] In some embodiments of the pseudo-envelope follower power management system 10E, depicted in Figure 18B, the controller 50 may advantageously configure the clock selection circuit 268 to provide the divided frequency locked loop Clock 282 as the μC charge pump clock 276. As a result, the switching operations of the μC charge pump circuit 262 may be substantially synchronous to the switching operations of the multi-level charge pump buck converter 12C. In some embodiments of the pseudo-envelope follower power management system 10E, the synchronicity of operations between the μC charge pump circuit 262 and the multi-level charge pump buck converter 12C may improve or reduce the noise performance provided at the power amplifier supply voltage, V_{CC}. Alternatively, the controller 50 may configure the clock selection circuit 268 to provide the clock reference signal 139A as the μC charge pump clock 276 to the μC charge pump circuit 262. In this mode of operation, the switching between various phases of operation in the μC charge pump circuit 262 may be relatively stable. Alternatively, in still other embodiments of the pseudo-envelope follower power management system 10E, the clock

selection circuit 268 is configured to provide the fixed frequency reference clock as the μC charge pump clock 276.

[00484] In addition, the controller 50 may further provide a frequency locked loop circuit control signal 292 to govern the operation of the frequency locked loop circuit 54 of the multi-level charge pump buck converter 12C. The frequency locked loop circuit control signal 292 may include one or more control signals used to configure the frequency locked loop circuit 54. Via the frequency locked loop circuit control signal 292, the controller 50 may configure various time constants and control parameters resident in the frequency locked loop circuit 54 (not shown) to optimally extract the operating frequency of the multi-level charge pump buck converter 12C so as to reduce the overall voltage ripple that occurs at the power amplifier supply voltage V_{CC}. The configuration of the frequency locked loop circuit 54 may depend upon various factors, including, but not limited to the maximum expected parallel amplifier supply voltage, V_{CC_MAX}, the minimum expected parallel amplifier supply voltage, V_{CC_MIN}, the expected waveform generated by the radio frequency power amplifier, the envelope and signal transmission characteristics of the signal to be transmitted, the peak-to-average ratio of the envelope of the signal to be transmitted, the data rate, the bandwidth of the channel and/or the type of modulation used to the desired waveform. Moreover, controller 50 may configure the frequency locked loop circuit 54 to minimize the overall noise or output ripple.

[00485] The parallel amplifier power source selection circuit 272 is configured to receive the internal charge pump node parallel amplifier supply 294 from the multi-level charge pump circuit 258, of the multi-level charge pump buck converter 12C, or the μC charge pump circuit output voltage, $V_{\mu C_OUT}$, which is generated at the μC charge pump output. The parallel amplifier power source selection circuit 272 may be configured to be operably coupled to the controller 50 via a source selection control signal. Via the source selection control signal 296, the controller 50 may configure the parallel amplifier power source selection circuit 272 to select a desired input supply from either the internal charge pump node parallel amplifier supply or the μC charge pump

output, to be provided as the parallel amplifier supply voltage $V_{SUPPLY_PARA_AMP}$ to the parallel amplifier circuitry 32.

[00486] In an alternative embodiment of the pseudo-envelope follower power management system 10E, the parallel amplifier power source selection circuit 272 may be eliminated in the case where the internal charge pump node parallel amplifier supply or the µC charge pump output are directly coupled to the parallel amplifier supply, $V_{SUPPLY_PARA_AMP}$. For example, some embodiments of the multi-level charge pump buck converter 12C may include a multi-level charge pump that does not provide an internal charge pump node parallel amplifier supply as an output. In this case, the µC charge pump output of the µC charge pump circuit 262 is directly coupled to the parallel amplifier circuit 14C to provide the parallel amplifier supply voltage $V_{SUPPLY_PARA_AMP}$, as the operational voltage for the parallel amplifier 35 and associated circuitry.

[00487] In addition, similar to the parallel amplifier circuit 14A and the parallel amplifier circuit 14B, depicted in Figures 2A-2B, the parallel amplifier circuit 14D may also include an embodiment of the V_{OFFSET} loop circuit 41 as V_{OFFSET} loop circuit 41B. The V_{OFFSET} loop circuit 41B may be configured to regulate the offset voltage, V_{OFFSET}, that is developed across the coupling circuit 18. Similar to the V_{OFFSET} loop circuit 41 of Figures 2A-2B, the V_{OFFSET} loop circuit 41B may provide a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the switcher control circuit 52 of the multi-level charge pump buck converter 12C, where the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, provides an estimate of the magnitude of the offset voltage, V_{OFFSET}, appearing across the coupling circuit 18.

[00488] The V_{OFFSET} loop circuit 41B may include a summing circuit 300, a V_{OFFSET} target signal section circuit 308, a pre-filter 313, and an integrator with zero compensation 314 operably configured to generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, based upon the power amplifier supply voltage, V_{CC}, the parallel amplifier output 32A, and a V_{OFFSET} target signal 302. The V_{OFFSET} target signal section circuit 308 may include a first input configured to receive a target offset voltage parameter, V_{OFFSET_TARGET}, a second input configured to receive the V_{RAMP} signal, and a third input configured to receive a

filtered V_{RAMP} signal from the pre-filter 313. The V_{OFFSET} target signal section circuit 308 may be configured to receive a target selection signal 310 from the controller 50. Based upon the target selection signal 310 received from the controller 50, the V_{OFFSET} target signal section circuit 308 provides one of the target offset voltage parameter, V_{OFFSET_TARGET}, the V_{RAMP} signal, or the filtered V_{RAMP} signal as a V_{OFFSET} target signal 302 to the summing circuit 300. In some alternative embodiments, the V_{OFFSET} target signal section circuit 308 may be controlled via a V_{OFFSET} control bus 312 that is coupled to the V_{OFFSET} loop circuit 41B.

[00489] The pre-filter 313 may be similar to the frequency pre-distortion circuit 254, depicted in Figure 10. Similar to the frequency pre-distortion circuit 254, the pre-filter 313 may include a frequency equalizer circuit that includes programmable time constants. Illustratively, the programmable time constants may include a programmable pole time constant, Tau_P, and a programmable zero time constant, Tau_Z. The controller 50 may adjust the values of the programmable pole time constant, Tau_P, and a programmable zero time constant, Tau_Z, to adjust the frequency response of the pre-filter 313. In some embodiments of the parallel amplifier circuit 14D, the output of the frequency pre-distortion circuit 254 may be used as the third input to the V_{OFFSET} target signal section circuit 308 instead of providing a pre-filter 313.

[00490] The summing circuit 300 may include a positive terminal operably coupled to the power amplifier supply voltage, V_{CC}. a first negative terminal coupled to the parallel amplifier output 32A, and a second negative terminal configured to receive the V_{OFFSET} target signal 302. The summing circuit 300 subtracts the parallel amplifier output 32A and the V_{OFFSET} target signal from the power amplifier supply voltage, V_{CC}, to generate a V_{OFFSET} error signal 304. The V_{OFFSET} error signal 304 may be provided to the integrator with zero compensation 314, which filters the V_{OFFSET} error signal 304 to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$.

[00491] The V_{OFFSET} loop circuit 41B may be configured to create an almost constant DC voltage across the coupling circuit 18 in order to shift the power

amplifier supply voltage, V_{CC}, down by a fixed amount in order to minimize the peak voltage present at the parallel amplifier output 32A.

[00492] As discussed with respect to the various embodiments of the switcher control circuits 52A-C and 52E-G, depicted in Figures 3A-C and E-G, Figures 4A-C and E-G, Figures 5A-C and E-G, and Figures 6A-C, the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and a second boost level threshold 130 may be offset by the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is generated by the V_{OFFSET} loop circuit 41B to control the offset voltage, V_{OFFSET}, across the coupling circuit 18, as depicted in Figures 18A-D.

[00493] The integrator with zero compensation 314 may include a filter having a first time constant, Tau_0, and a second time constant, Tau_1. The integrator with zero compensation 314 may have a filter response that is equivalent to a Laplace transfer function equal to $[(1+Tau_0 * s)/(Tau_1 * s)]$. The values of the first time constant, Tau_0, and a second time constant, Tau_1, may be programmed by the controller 50 via the V_{OFFSET} control bus 312. The values of the first time constant, Tau_0, and a second time constant, Tau_1, may be selected to optimize the bandwidth of the V_{OFFSET} loop circuit to provide loop stability and a desired response time depending upon the capacitance of the coupling circuit 18 across which the offset voltage, V_{OFFSET}, is developed.

[00494] In addition, the V_{OFFSET} loop circuit 41B may further be configured to permit selection of the value of the first time constant, Tau_0, and a second time constant, Tau_1, dependent upon whether the coupling circuit 18 requires pre-charging before initiation of a data burst to be sent by the linear radio frequency power amplifier 22, as depicted, for example, in Figures 1A-B and 2A-B. For example, if the data burst to be sent is a first data burst of the transmission, the controller 50 may determine that the coupling circuit 18 requires pre-charging prior to transmission of the first data burst.

[00495] In some embodiments of the V_{OFFSET} loop circuit 41B, the controller 50 may store a first startup time constant, Tau_0_startup, and a second startup time constant, Tau_1_startup, as local parameters. As an example, the local

parameters may be stored in a parameter storage circuit (not shown) of the V_{OFFSET} loop circuit 41B. For example, the parameter storage circuit (not shown) may store the first startup time constant, Tau_0_startup, and the second startup time constant, Tau_1_startup. In some embodiments, the parameter storage circuit (not shown) may further store the first normal time constant, Tau_0_normal, and the second normal time constant, Tau_1_normal. The V_{OFFSET} loop circuit 41B may be configured to use the first startup time constant, Tau_0_startup, and the second startup time constant, Tau_1_startup, during a pre-charging phase of operation of the V_{OFFSET} loop circuit 41B from the parameter storage circuit (not shown). When the V_{OFFSET} loop circuit 41B is configured to operate using the first startup time constant, Tau_0_startup, as the first time constant, Tau_0, and the second startup time constant, Tau_1_startup, as the second time constant, Tau_1, the operational bandwidth of the V_{OFFSET} loop circuit 41B is increased to permit faster pre-charging of the coupling circuit 18.

[00496] In addition, in some embodiments of the V_{OFFSET} loop circuit 41B, the controller 50 may store a first normal time constant, Tau_0_normal, and a second normal time constant, Tau_1_normal, as local parameters in the V_{OFFSET} loop circuit 41B. When the V_{OFFSET} loop circuit 41B is configured to operate using the first normal constant, Tau_0_normal, as the first time constant, Tau_0, and the second normal time constant, Tau_1_normal, as the second time constant, Tau_1, from the parameter storage circuit (not shown), the operational bandwidth of the V_{OFFSET} loop circuit 41B is decreased to operate in a normal mode of operation.

[00497] Some embodiments of the V_{OFFSET} loop circuit 41B may include a pre-charge mode of operation that permits the controller to place the V_{OFFSET} loop circuit 41B into a pre-charge mode of operation for a predetermined period of time. For example, the V_{OFFSET} loop circuit 41B may include a pre-charge timer (not shown) that may be programmed by the controller 50 to generate a timer event after a predetermined time period. When in the pre-charge mode of operation, the V_{OFFSET} loop circuit 41B uses the first startup time constant, Tau_0_startup, as the first time constant, Tau_0, and the second startup time constant, Tau_1_startup, as the second time constant, Tau_1, which increases the

operational bandwidth of the V_{OFFSET} loop circuit 41B. As an example, when starting from power-off mode to active mode, the time constant of the V_{OFFSET} loop circuit 41B may be programmatically reduced by the controller 50 by up to a factor of five to allow a quick initial pre-charging of the coupling circuit 18. For example, pre-charging may be done prior to the beginning of a transmission-slot in order to reduce the time to have the voltage completely settled to the target value for the first power-up. As an example, the transmission-slot may be a burst transmission-slot in which data is transmitted by the linear radio frequency power amplifier. The controller 50 may configure the V_{OFFSET} loop circuit 41B to operate in a higher bandwidth during the initial pre-charging of reactive components of the coupling circuit 18. As an alternative example, the V_{OFFSET} loop circuit 41B may include a control circuit (not shown) to configure the first time constant, Tau_0, and the second time constant, Tau_1, to place the V_{OFFSET} loop circuit 41B in a pre-charge mode of operation or a normal mode of operation prior to the beginning of a data transmission.

[00498] In some cases, the loop bandwidth of the V_{OFFSET} loop circuit 41B may be set to provide up to five times the bandwidth used at the beginning of a burst transmission time-slot. The controller 50 operably re-configures the V_{OFFSET} loop circuit 41B back to a lower or operational bandwidth at the beginning of the burst transmission-slot. In other alternative embodiments of the pseudo-envelope follower power management system, the controller 50 may re-configure the V_{OFFSET} loop circuit 41B to have a bandwidth between 3 and 7 times the bandwidth used at the beginning of a burst transmission time-slot. Advantageously, configuring the V_{OFFSET} loop circuit 41B to operate with a higher loop bandwidth during initial pre-charging of the reactive components of the coupling circuit 18 decreases the startup delay of the pseudo-envelope follower power management system, which provided an improvement in overall power efficiency.

[00499] The V_{OFFSET} loop circuit 41B may be monitored and modified in a dynamic fashion. For example, the timing/filter parameters associated with the integrator with zero compensation 314 and desired V_{OFFSET} voltage, set by the

target offset voltage, V_{OFFSET_TARGET}, parameter, may be monitored and modified by the controller 50 on a burst time-slot basis.

[00500] The V_{OFFSET} loop circuit 41B may be configured to operate in a higher loop band width mode of operation when no modulation is present on the V_{RAMP} signal. For example, at either the beginning of the slot or between inter-slots, when the V_{RAMP} signal is inactive, the controller 50 may configure the V_{OFFSET} loop circuit 41B to operate in a higher bandwidth mode of operation to improve initial startup regulation of the offset voltage, V_{OFFSET}. Alternatively, or in addition, the V_{OFFSET} loop circuit 41B may be configured to switch from the V_{OFFSET} loop lower loop bandwidth mode of operation to V_{OFFSET} loop higher loop band width mode of operation when no modulation is present on the V_{RAMP} signal. As another example, a control circuit (not shown) of the V_{OFFSET} loop circuit 41B may be configured to monitor the V_{RAMP} signal to determine when no modulation is present.

[00501] As another example, the controller 50 may program the pre-charge timer (not shown) to trigger an event after a predetermined pre-charge time period. Upon the trigger event, the V_{OFFSET} loop circuit 41B may be automatically re-configured to set the first normal time constant, Tau_0, to be equal to Tau_0_normal and the second time constant, Tau_1, to be equal to Tau_1_normal. As a result, after the predetermined pre-charge time period, the V_{OFFSET} loop circuit 41B is re-configured to operate with a normal bandwidth to ensure loop stability. This has the advantage of permitting the V_{OFFSET} loop circuit 41B to operate in a higher bandwidth mode during pre-charging and in a lower bandwidth mode during normal operation without requiring the controller 50 to reconfigure the V_{OFFSET} loop circuit 41B after a predetermined pre-charge period of time to operate in a mode having a bandwidth that is appropriate for normal operation of the pseudo-envelope follower power management system. Alternatively or in addition, controller 50 may configured the control circuit (not shown) of the V_{OFFSET} loop circuit 41B to operate the V_{OFFSET} loop circuit 41B in a pre-charge mode of operation for a pre-determined period of time. In response,

the control circuit (not shown) may enable the pre-charge timer (not shown) and configure the first time constant, Tau_0, and the second time constant, Tau_1.

[00502] In the various embodiments of the switcher control circuit depicted in Figures 3A-C and E-G, Figures 4A-C and E-G, Figures 5A-C and E-G, and Figures 6A-C, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, generated by the V_{OFFSET} loop circuit 41 is generally used to raise and lower the point at which the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 trigger. However, in some alternative embodiment of the threshold detector and control circuits 132A-C and 132E-G, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, may be used to only shift the triggering threshold of less than all of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. For example, referring to Figure 4C, the threshold detector and control circuit 132C may be reconfigured such that the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, only shifts the triggering threshold of the second comparator 142. The effect is to only shift the triggering threshold of the comparator associated with the series level threshold 126 based upon the threshold offset current 42, $I_{THRESHOLD_OFFSET}$. Similarly, as another example of an alternative embodiment, the threshold detector and control circuit 132G, depicted in Figure 4G, may be reconfigured such that the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, only shifts the triggering threshold of the first comparator 140. The effect is to only shift the triggering threshold of the comparator associated with the shunt level threshold 124 based upon the threshold offset current 42, $I_{THRESHOLD_OFFSET}$.

[00503] The shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 may be offset by threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is generated by the V_{OFFSET} loop circuit 41B to control the offset voltage, V_{OFFSET}, across the coupling circuit 18, as depicted in Figures 18A-D.

[00504] The battery level sense circuit 264 may be coupled to the controller 50 via the battery level sense signal. The battery level sense circuit 264 may be operably configured to measure or determine the voltage level of the battery,

(V_{BAT}). The voltage measured or determined voltage level of the battery may be provided to or obtained by the controller 50 via the battery level sense circuit 264. In alternative embodiments, not shown, the battery level sense circuit 264 may be configured to interface with the controller 50 via a control bus 44. Accordingly, the controller may use the voltage level of the battery, (V_{BAT}), to configure the various operational components of the pseudo-envelope follower power management system 10E.

[00505] Figure 18A further depicts another embodiment of a pseudo-envelope follower power management system 10C that is similar to the embodiment of the pseudo-envelope follower power management system 10E, depicted in Figure 18B, except that the parallel amplifier circuit 14D is replaced by the parallel amplifier circuit 14C. The parallel amplifier circuit 14C is similar to the parallel amplifier circuit 14D, depicted in Figure 18B, except that the V_{OFFSET} loop circuit 41B is replaced by the V_{OFFSET} loop circuit 41A. The V_{OFFSET} loop circuit 41A is operably configured to operate in a similar fashion as the V_{OFFSET} loop circuit 41B except that the integrator with zero compensation 314 is replaced with a K_{ERROR_GAIN} circuit 306 configured to receive the V_{OFFSET} error signal 304 from the summing circuit 300. The K_{ERROR_GAIN} circuit 306 may be configured to multiply the V_{OFFSET} error signal 304 by an offset voltage error gain, K_{ERROR_GAIN}, based on a K_{ERROR_GAIN} parameter to generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$. The controller 50 may be configured to modify the K_{ERROR_GAIN} parameter based on the operational needs of the linear radio frequency power amplifier. In some embodiments, the V_{OFFSET} loop circuit 41A, may automatically change the offset voltage error gain, K_{ERROR_GAIN}, based upon a mode of operation of the V_{OFFSET} loop circuit 41A. For example, the V_{OFFSET} loop circuit 41A may include a pre-charge mode of operation and a normal mode of operation. In some embodiments, the controller 50 may set the V_{OFFSET} loop circuit 41A in a pre-charge mode of operation based on a lack of activity on the V_{RAMP} signal or when a data transmission is not eliminate. In other example embodiments, the V_{OFFSET} loop circuit 41A may determine whether to operate in a pre-charge mode of operation or a normal mode of operation based on or in

response to receipt of an updated target offset voltage parameter, V_{OFFSET_TARGET} or an indication from the 50 indicating that a data transmission is about to commence.

[00506] Illustratively, unlike the operation of the V_{OFFSET} loop circuit 41B described above, where the filter having a first time constant, Tau_0, and the second time constant, Tau_1, may be modified to optimize the bandwidth of the V_{OFFSET} loop circuit 41B during pre-charging of the coupling circuit 18, prior to initiation of a data burst to be sent by the linear radio frequency power amplifier 22, as depicted, for example, in Figures 1A-B and 2A-B, the controller 50 may selectively modify the K_{ERROR_GAIN} value to provide a pre-charge mode of operation for a pre-determined period of time. During the pre-charge mode of operation, the controller 50 may increase the value of the K_{ERROR_GAIN} value to effectively provide higher loop bandwidth. After a predetermined period of time, the controller may decrease the K_{ERROR_GAIN} value to provide a lower loop bandwidth to ensure stable operation of the V_{OFFSET} loop circuit 41A. In some alternative embodiments, the V_{OFFSET} loop circuit 41A may be configured to use a pre-charge K_{ERROR_GAIN} value during a pre-charge mode of operation and a normal operation K_{ERROR_GAIN} value during a normal mode of operation. In some embodiments, the pre-charge K_{ERROR_GAIN} value is greater than the normal operation K_{ERROR_GAIN} value. The pre-charge K_{ERROR_GAIN} value and the normal operation K_{ERROR_GAIN} value may be stored locally to the V_{OFFSET} loop circuit 41A. For example, similar to the V_{OFFSET} loop circuit 41A, depicted in Figure 18B and Figure 18D, the V_{OFFSET} loop circuit 41A may also include a parameter storage circuit (not shown) to store the pre-charge K_{ERROR_GAIN} value and the normal operation K_{ERROR_GAIN} value. As an example, the pre-charge K_{ERROR_GAIN} value and the normal operation K_{ERROR_GAIN} value may be stored in a parameter storage circuit or memory.

[00507] Embodiments of the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B may be configured to determine whether to be in a normal mode of operation or a pre-charge mode of operation prior to a data transmission based on the offset voltage, V_{OFFSET}, across the coupling circuit 18. As another

example, each of the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41A may be configured to determine whether to operate in the pre-charge mode of operation or the normal mode of operation based on the V_{OFFSET} error signal 304. For example, the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B may each be configured to determine that the coupling circuit 18 requires pre-charging based on whether the V_{OFFSET} error signal 304 exceeds the V_{OFFSET} error signal threshold. As an example, based on a determination that the coupling circuit 18 requires pre-charging, the $K_{ERROR\ GAIN}$ circuit 306 may be configured to use the pre-charge $K_{ERROR\ GAIN}$ value to generate the threshold offset current 42, $I_{THRESHOLD\ OFFSET}$, for a pre-determined time period. After the pre-determined time period, the $K_{ERROR\ GAIN}$ circuit 306 may be configured to automatically use normal operation $K_{ERROR\ GAIN}$ value stored locally.

[00508] In a similar fashion, in response to a determination that the V_{OFFSET} error signal 304 exceeds the V_{OFFSET} error signal threshold, the integrator with zero compensation 314 may be configured to use the first startup time constant, Tau_0 startup, as the first time constant, Tau_0, and the second startup time constant, Tau_1 startup, as the second time constant, Tau_1, to generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, for a pre-determined time period. After the pre-determined time period, the integrator with zero compensation 314 may be configured to automatically transition to use the first normal time constant, Tau_0_normal, and the second normal time constant, Tau_1_normal, which may be stored locally.

[00509] In addition, the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B may be configured to switch from the normal mode of operation to a pre-charge mode of operation when no modulation is present on the V_{RAMP} signal. Also, in some embodiments, some or all of the operations to configure the V_{OFFSET} loop circuit 41A or the V_{OFFSET} loop circuit 41B to operate in one of the pre-charge mode of operation and the normal mode of operation may be carried out by the controller 50. Alternatively, the V_{OFFSET} loop circuit 41A, depicted in Figure 18A and Figure 18C, and the V_{OFFSET} loop circuit 41B, depicted in Figure 18B and Figure 18D, may include a control circuit (not shown)

that orchestrates the operation of the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B as described above based on receipt of a new target offset voltage parameter, V_{OFFSET_TARGET}, receipt of an indication of an upcoming data transmission, an indication to place the V_{OFFSET} loop circuit 41A or the V_{OFFSET} loop circuit 41Bk in one of a pre-charge mode of operation and a normal mode of operation from the controller 50, a determination that the V_{RAMP} signal is inactive, and/or a combination thereof.

[00510] While the pseudo-envelope follower power management system 10C, depicted in Figure 18A, and the pseudo-envelope follower power management system 10E, depicted in Figure 18B, only depict the respective parallel amplifier circuit 14C and parallel amplifier circuit 14D providing the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, as a feedback signal to the switcher control circuit 52 of the multi-level charge pump buck converter 12C, this is by example and not limitation. Accordingly, some embodiments of the pseudo-envelope follower power management system 10C and the pseudo-envelope follower power management system 10E may further include an open loop assist circuit similar to the open loop assist circuit 39, as depicted in Figure 2A with respect to the pseudo-envelope follower power management system 10A and depicted in Figure 10B with respect to the pseudo-envelope follower power management system 10B, and/ or the example embodiments of the open loop assist circuit 39, the open loop assist circuit 39A, depicted in Figure 9A, and the open loop assist circuit 39B, depicted in Figure 9B. In this case, as shown in Figures 2A-B, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is combined with the open loop assist circuit output current estimate, I_{ASSIST_SENSE}, as depicted in Figures 2A-B, to form the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, which is used as a feedback signal to the switcher control circuit 52. Accordingly, the switcher control circuit 52 and operation of the multi-level charge pump buck converter 12C depicted in Figures 18A-B may also incorporate various combinations of the operational features and functions of the embodiments of the switcher control circuits 52A-D, depicted in Figures 3A-D, the threshold detector and control

circuits 132A-D, depicted in Figures 4A-D, and the circuitry and state machines associated with the logic circuits 148A-D, depicted in Figures 4A-D.

[00511] Figure 18C depicts an embodiment of a pseudo-envelope follower power management system 10D that is similar to the pseudo-envelope follower power management system 10C, depicted in Figure 18A and discussed below. However, unlike the pseudo-envelope follower power management system 10C, depicted in Figure 18A, the multi-level charge pump buck converter 12C is replaced by a buck converter 13A. As depicted in Figure 18C, the buck converter 13A, depicted in Figure 18C, does not include a multi-level charge pump circuit 258.

[00512] Also similar to the pseudo-envelope follower power management system 10C, depicted in Figure 18A, the pseudo-envelope follower power management system 10D, depicted in Figure 18C, further includes an embodiment of a V_{OFFSET} loop circuit 41A configured to provide a threshold offset current 42, $I_{THRESHOLD_OFFSET}$. However, unlike the pseudo-envelope follower power management system 10D, depicted in Figure 18C, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, is provided to the switcher control circuit 259 of the buck converter 13A.

[00513] In addition, because the buck converter 13A does not include the multi-level charge pump circuit 258, the parallel amplifier power source selection circuit 272 is eliminated and the µC charge pump output of the µC charge pump circuit 262 is directly coupled to the parallel amplifier circuit 14C in order to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$ to the parallel amplifier 35 of the parallel amplifier circuitry 32.

[00514] As further depicted in Figure 18C, unlike the multi-level charge pump buck converter 12C, depicted in Figure 18A, the buck converter 13A also replaces the switcher control circuit 52 with a switcher control circuit 259. Like the switcher control circuit 52, the switcher control circuit 259 provides a series switch control signal 66 and a shunt switch control signal 68 to the switching circuit 58. Like the switcher control circuit 52 depicted in Figure 18A, the switcher control circuit 259, depicted in Figure 18C, may be further configured to

receive the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the V_{OFFSET} loop circuit 41A.

[00515] Although the embodiment of the pseudo-envelope follower power management system 10D, depicted in Figure 18C, only depicts that the switcher control circuit 259 is configured to receive the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, as discussed above with respect to the embodiment of the pseudo-envelope follower power management system 10E, depicted in Figure 18B, and discussed below, with respect to the pseudo-envelope follower power management system 10C, depicted in Figures 18A, this is by example and not by limitation. Some embodiments of the parallel amplifier circuit 14C of Figure 18C may further include an open loop assist circuit 39 similar to the open loop assist circuit 39 depicted in Figures 2A-B, and/or the example embodiments of the open loop assist circuit 39, the open loop assist circuit 39A, depicted in Figure 9A, and the open loop assist circuit 39B, depicted in Figure 9B. Accordingly, in those cases where an open loop assist circuit is included in the parallel amplifier circuit 14C, as depicted in Figures 2A-B, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is combined with the open loop assist circuit output current estimate, I_{ASSIST_SENSE}, depicted in Figures 2A-B, to form the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, that may be provided as a feedback signal to the switcher control circuit 259.

[00516] Accordingly, example embodiments of the switcher control circuit 259 of the buck converter 13A will now be described, as further depicted in Figures 3E-H. One example embodiment of the switcher control circuit 259 of the buck converter 13A is depicted in Figure 3E as switcher control circuit 52E. The switcher control circuit 52E is functionally similar to the switcher control circuit 52A, depicted in Figure 3A, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. As a result, for example, the threshold detector and control circuit 132E, of Figure 3E, does not include a first boost level threshold 128, a second boost level threshold 130, the third comparator 144, or the fourth comparator 146. Also, as discussed above, the parallel amplifier

circuit output current estimate 40, $I_{PAWA_OUT_EST}$, depicted in Figure 3E, may be provided by the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, or, in the case where an open loop assist circuit is included in the parallel amplifier circuit 14C of Figure 18C, the sum of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the open loop assist circuit output current estimate, I_{ASSIST_SENSE}. Also, as previously discussed with respect to Figure 3E, some embodiments of the switcher control circuit 52E (not depicted) may subtract the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, with the summing circuit 136, where the difference between the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, is multiplied by the threshold scalar 137A with the multiplier circuit 134 to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}.

[00517] One embodiment of the threshold detector and control circuit 132E is depicted in Figure 4E, which is described with continuing reference to Figure 3E and Figure 5E. The threshold detector and control circuit 132E may be functionally similar to the threshold detector and control circuit 132A, depicted in Figure 4A, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. As a result, the logic circuit 148E is configured to operate as a buck converter based upon the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, relative to the shunt level threshold 124 and the series level threshold 126. In addition, unlike the threshold detector and control circuit 132A depicted in Figure 4A, the first state machine used to control the logic circuit 148E may be simplified. Illustratively, Figure 5E depicts an example embodiment of a first state machine of the logic circuit 148E that may include a shunt output mode 188E and a series output mode 190E, and which is described with continuing reference to Figures 3E and 4E.

[00518] In the shunt output mode 188E, the logic circuit 148E configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series switch 70, depicted in

Figure 3E, is in an open state (not conducting). The logic circuit 148E also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72, depicted in Figure 3E, is in a closed state (conducting). As a result, the switching voltage output 26 of Figure 3E is configured to provide a switching voltage, V_{SW}, substantially equal to ground. As depicted in Figure 5E, in response to assertion of the series level indication 152A, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is greater than or equal to the series level threshold 126, the logic circuit 148E configures the first state machine to transition to the series output mode 190E. Otherwise, the first state machine remains in the shunt output mode 188E.

[00519] In the series output mode 190E, the logic circuit 148E configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series switch 70, depicted in Figure 3E, is in a closed state (conducting). The logic circuit 148E also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72, depicted in Figure 3E, is in an open state (not conducting). As a result, the switching voltage output 26, depicted in Figure 3E, is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}, provided by the battery 20. In response to de-assertion of the shunt level indication 150A, depicted in Figure 4E, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124, the logic circuit 148E configures the first state machine to transition to the shunt output mode 188E, as depicted in Figure 5E. Otherwise, the logic circuit 148E configures the first state machine to remain in the series output mode 190E.

[00520] Another embodiment of the switcher control circuit 259 of the buck converter 13A is depicted in Figure 3F as switcher control circuit 52F. The switcher control circuit 52F may be functionally similar to the switcher control circuit 52B, depicted in Figure 3B, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. As a result, for example, the threshold

detector and control circuit 132F, of Figure 3F, does not include the first boost level threshold 128, the second boost level threshold 130, the third comparator 144, or the fourth comparator 146. Also, as discussed above, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, depicted in Figure 3F, may be provided by the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, or, in the case where an open loop assist circuit is included in the parallel amplifier circuit 14C of Figure 18C, the sum of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the open loop assist circuit output current estimate, I_{ASSIST_SENSE}.

[00521] One embodiment of the threshold detector and control circuit 132F of Figure 3F is further depicted in Figure 4F. The threshold detector and control circuit 132F may be functionally similar to the threshold detector and control circuit 132B, depicted in Figure 4B, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. As a result, for example, the logic circuit 148F is configured to operate as a buck converter based upon the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', relative to the scaled shunt level threshold 176 and the scaled series level threshold 178. Accordingly, similar to the previously discussed embodiment of the multi-level charge pump buck converter 12A, the frequency locked loop circuit 54B may be configured to adjust the magnitude of the threshold scalar' 137B to maintain an average switching frequency of operation of the buck converter 13A based on a target average frequency of operation parameter. In addition, unlike the threshold detector and control circuit 132B, depicted in Figure 4B, the first state machine used to control the logic circuit 148F may be simplified. As an example, Figure 5F depicts an example embodiment of a first state machine of the logic circuit 148F that includes a shunt output mode 188F and a series output mode 190F, which is described with continuing reference to Figures 3F and 4F.

[00522] In the shunt output mode 188F, the logic circuit 148F, depicted in Figure 4F, configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series

switch 70, depicted in Figure 3F, is in an open state (not conducting). The logic circuit 148F also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72, depicted in Figure 3F, is in a closed state (conducting). As a result, the switching voltage output 26 of Figure 3F is configured to provide a switching voltage, V_{SW}, substantially equal to ground. As depicted in Figure 4F, in response to assertion of the series level indication 152B, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the scaled series level threshold 178, the logic circuit 148F configures the first state machine to transition to the series output mode 190F. Otherwise, the first state machine remains in the shunt output mode 188F.

[00523] In the series output mode 190F, the logic circuit 148F configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series switch 70, depicted in Figure 3F, is in a closed state (conducting). The logic circuit 148F also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72, depicted in Figure 3F, is in an open state (not conducting). As a result, the switching voltage output 26, depicted in Figure 3F, is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. In response to de-assertion of the shunt level indication 150B, depicted in Figure 4F, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than scaled shunt level threshold 176, the logic circuit 148F configures the first state machine to transition to the shunt output mode 188F, as depicted in Figure 5F. Otherwise, the logic circuit 148F configures the first state machine to remain in the series output mode 190F.

[00524] Another example embodiment of the switcher control circuit 259 of the buck converter 13A is depicted in Figure 3G as switcher control circuit 52G. The switcher control circuit 52G may be functionally similar to the switcher control circuit 52C, depicted in Figure 3C, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. As a result, for example, the threshold

detector and control circuit 132G, of Figure 3G, does not include a first boost level threshold 128, a second boost level threshold 130, the third comparator 144, or the fourth comparator 146. Also, as discussed above, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, depicted in Figure 3G, may be provided by the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, or, in the case where an open loop assist circuit is included in the parallel amplifier circuit 14C of Figure 18C, the sum of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the open loop assist circuit output current estimate, I_{ASSIST_SENSE}.

[00525] One embodiment of the threshold detector and control circuit 132G of Figure 3G is further depicted in Figure 4G. The threshold detector and control circuit 132G may be functionally similar to the threshold detector and control circuit 132C, depicted in Figure 4C, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. As a result, the logic circuit 148G is configured to operate as a buck converter based upon the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', relative to the shunt level threshold 124 and the series level threshold 126. In addition, unlike the threshold detector and control circuit 132C, depicted in Figure 4C, the first state machine used to control the logic circuit 148G may be simplified. As an example, Figure 5G depicts an example embodiment of a first state machine of the logic circuit 148G that includes a shunt output mode 188G and a series output mode 190G, and which is described with continuing reference to Figures 3G and 4G.

[00526] In the shunt output mode 188G, the logic circuit 148G, depicted in Figure 4G, configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series switch 70, depicted in Figure 3G, is in an open state (not conducting). The logic circuit 148G also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72 is in a closed state (conducting). As a result, the switching voltage output 26 of Figure 3G is configured to provide a switching voltage, V_{SW}, substantially equal to ground. In

response to assertion of the series level indication 152C, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is greater than or equal to the series level threshold 126, the logic circuit 148G configures the first state machine to transition to the series output mode 190G. Otherwise, the first state machine remains in the shunt output mode 188G.

[00527] In the series output mode 190G, the logic circuit 148G configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series switch 70, depicted in Figure 3G, is in a closed state (conducting). The logic circuit 148G also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72, depicted in Figure 3G, is in an open state (not conducting). As a result, the switching voltage output 26, depicted in Figure 3G, is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. In response to de-assertion of the shunt level indication 150C, depicted in Figure 4G, which indicates that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the shunt level threshold 124, the logic circuit 148G configures the first state machine to transition to the shunt output mode 188G, as depicted in Figure 5G. Otherwise, the logic circuit 148G configures the first state machine to remain in the series output mode 190G.

[00528] While Figures 3G and 4G do not depict the presence of a frequency locked loop circuit being used in combination with the switcher control circuit 52G, an embodiment of the frequency locked loop circuit may be provided for use in the buck converter in order to provide a frequency locked loop system clock 280 to either the switcher control circuit 52G or the clock management system of the pseudo-envelope follower power management system.

[00529] For the sake of completeness, another example embodiment of the switcher control circuit 259 of the buck converter 13A is depicted in Figure 3H as switcher control circuit 52H. The switcher control circuit 52H may be functionally similar to the switcher control circuit 52D, depicted in Figure 3D, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. Like

the switcher control circuit 52D of Figure 3D, the switcher control circuit 52H depicts the an embodiment of the switcher control circuit 259 that may be used when either the buck converter 13A does not use the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to control the operation of the switcher control circuit 259 or, for the sake of completeness, the corresponding parallel amplifier circuit does not provide the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the buck converter 13A.

[00530] Like the switcher control circuit 52D of Figure 3D, the switcher control circuit 52H provides a series switch control signal 66 and a shunt switch control signal 68 to the switching circuit 58. As a result, the threshold detector and control circuit 132H, of Figure 3H, include a first boost level threshold 128, a second boost level threshold 130, the third comparator 144 or the fourth comparator 146. Also, as discussed above, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, depicted in Figure 3H, may be provided by the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, or, in the case where an open loop assist circuit is included in the parallel amplifier circuit 14C of Figure 18C, the sum of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the open loop assist circuit output current estimate, I_{ASSIST_SENSE}.

[00531] One embodiment of the threshold detector and control circuit 132H of Figure 3H is further depicted in Figure 4H. The threshold detector and control circuit 132H may be functionally similar to the threshold detector and control circuit 132D, depicted in Figure 4D, except the circuitry associated with the multi-level charge pump circuit 56 is eliminated. For example, the threshold detector and control circuit 132D does not include a first boost level threshold 128, a second boost level threshold 130, the third comparator 144, or the fourth comparator 146. As a result, the logic circuit 148H is configured to operate as a buck converter based upon the magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, relative to the shunt level threshold 124 and the series level threshold 126. In addition, unlike the threshold detector and control circuit 132D, depicted in Figure 4D, the first state machine used to control

the logic circuit 148H may be simplified. As an example, Figure 5H depicts an example embodiment of a first state machine of the logic circuit 148H that includes a shunt output mode 188H and a series output mode 190H, and which is described with continuing reference to Figures 3H and 4H.

[00532] In the shunt output mode 188H, the logic circuit 148H, depicted in Figure 4H, configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series switch 70, depicted in Figure 3H, is in an open state (not conducting). The logic circuit 148H also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72, depicted in Figure 3H, is in a closed state (conducting). As a result, the switching voltage output 26 of Figure 3H is configured to provide a switching voltage, V_{SW}, substantially equal to ground. In response to assertion of the series level indication 152A, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the series level threshold 126, the logic circuit 148H configures the first state machine to transition to the series output mode 190H. Otherwise, the first state machine remains in the shunt output mode 188H.

[00533] In the series output mode 190H, the logic circuit 148H configures the series switch control output 162 to drive the first output buffer 158 to generate a series switch control signal 66 such that the series switch 70 is in a closed state (conducting). The logic circuit 148H also configures the shunt switch control output 164 to drive the second output buffer 160 such that the shunt switch 72 is in an open state (not conducting). As a result, the switching voltage output 26, depicted in Figure 3H, is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. In response to de-assertion of the shunt level indication 150D, depicted in Figure 4H, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the shunt level threshold 124, the logic circuit 148H configures the first state machine to transition to the shunt output mode 188H, as depicted in Figure 5H.

Otherwise, the logic circuit 148H configures the first state machine to remain in the series output mode 190H.

[00534] While Figures 3H and 4H do not depict the presence of a frequency locked loop circuit being used in combination with the switcher control circuit 52H, an embodiment of the frequency locked loop circuit may be provided for use in the buck converter in order to provide a frequency locked loop system clock 280 to either the switcher control circuit 52H or the clock management system of the pseudo-envelope follower power management system.

[00535] In addition, like the pseudo-envelope follower power management system 10C, depicted in Figure 18A, the pseudo-envelope follower power management system 10D, depicted in Figure 18C, includes the V_{OFFSET} loop circuit 41A, the operation of which is described below with respect to the V_{OFFSET} loop circuit 41B, depicted in Figure 18B.

[00536] Illustratively, unlike the operation of the V_{OFFSET} loop circuit 41B described above with respect Figure 18B, where the filter having a first time constant, Tau_0, and the second time constant, Tau_1, may be modified to optimize the bandwidth of the V_{OFFSET} loop circuit 41B during pre-charging of the coupling circuit 18, prior to initiation of a data burst to be sent by the linear radio frequency power amplifier 22, as depicted, for example, in Figures 1A-B and 2A-B, the controller 50, depicted in Figure 18C, may selectively modify the K_{ERROR_GAIN} value of the V_{OFFSET} loop circuit 41A to provide a pre-charge mode of operation for a pre-determined period of time. During the pre-charge mode of operation, the controller 50 may increase the K_{ERROR_GAIN} value to provide higher loop bandwidth. After a predetermined period of time, the controller 50 may decrease the K_{ERROR_GAIN} value to provide a lower loop bandwidth to ensure stable operation of the V_{OFFSET} loop circuit 41A.

[00537] Figure 18D depicts a pseudo-envelope follower power management system 10F that is similar to the pseudo-envelope follower power management system 10E, depicted in Figure 18B. Similar to the pseudo-envelope follower power management system 10E, depicted in Figure 18B, the pseudo-envelope follower power management system 10F includes the parallel amplifier

circuit 14D having the V_{OFFSET} loop circuit 41B. The various embodiments of the parallel amplifier circuit 14D, the parallel amplifier 35, and the V_{OFFSET} loop circuit 41B are described in detail relative to the pseudo-envelope follower power management system 10E of Figure 18B, and are therefore not repeated here.

[00538] However, unlike the pseudo-envelope follower power management system 10E, depicted in Figure 18B, the pseudo-envelope follower power management system 10F replaces the multi-level charge pump buck converter 12C with the buck converter 13A, depicted in Figure 18C.

[00539] As discussed before, because the buck converter 13A does not include the multi-level charge pump buck converter 12C, the parallel amplifier power source selection circuit 272 is eliminated and the µC charge pump output of the µC charge pump circuit 262 is directly coupled to the parallel amplifier circuit 14D in order to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, to the parallel amplifier 35.

[00540] In addition, like some embodiments of the pseudo-envelope follower power management system 10E, depicted in Figure 18B, some embodiments of the parallel amplifier circuit 14D of the pseudo-envelope follower power management system 10F, depicted in Figure 18D, may further include an open loop assist circuit 39 similar to the open loop assist circuit 39 depicted in Figures 2A-B, and/ or the example embodiments of the open loop assist circuit 39, the open loop assist circuit 39A, depicted in Figure 9A, and the open loop assist circuit 39B, depicted in Figure 9B. Accordingly, in those cases where an open loop assist circuit is included in the parallel amplifier circuit 14D, as depicted in Figures 2A-B, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is combined with the open loop assist circuit output current estimate, I_{ASSIST_SENSE}, to form the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, that may be provided as a feedback signal to the switcher control circuit 259 of the buck converter 13A.

[00541] Also, as discussed relative to the pseudo-envelope follower power management system 10D of Figure 18C, although the embodiment of the pseudo-envelope follower power management system 10F, depicted in

Figure 18D, only depicts the switcher control circuit 259 receiving the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, this is by example and not by limitation. Some embodiments of the parallel amplifier circuit 14D, of Figure 18D, may further include an open loop assist circuit 39 similar to the open loop assist circuit 39, depicted in Figures 2A-B, the example embodiment of the open loop assist circuit 39A, depicted in Figure 9A, and the example embodiment of the open loop assist circuit 39B, depicted in Figure 9B. Accordingly, in those cases where an open loop assist circuit is included in the parallel amplifier circuit 14D, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is combined with the open loop assist circuit output current estimate, I_{ASSIST_SENSE}, (depicted in Figures 2A-B), to form the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, that may be provided as a feedback signal to the switcher control circuit 259.

[00542] The operation of the buck converter 13A and the switcher control circuit 259 are described relative to the pseudo-envelope follower power management system 10D, depicted in Figure 18C. Accordingly, a detailed description of the operation of the buck converter 13A is omitted from the description of the pseudo-envelope follower power management system 10F, depicted in Figure 18D.

[00543] The μC charge pump circuit 262, depicted in Figures 18A-D, will now be discussed. Figure 19A depicts an embodiment of the μC charge pump circuit 262 of Figures 18A-D as a μC charge pump circuit 262A. The μC charge pump circuit 262A may be configured to generate a μC charge pump output voltage, $V_{\mu C_OUT}$, at the μC charge pump output based upon an operational mode of the μC charge pump circuit 262A. The μC charge pump circuit 262A may include four operational modes. The μC charge pump output voltage, $V_{\mu C_OUT}$, generated at the μC charge pump output may be based on an operational ratio of the μC charge pump, μBB_{RATIO}. As an example, the μC charge pump circuit 262A may include four operational modes: OFF mode, 1 x V_{BAT} mode, 4/3 x V_{BAT} mode, and 3/2 x V_{BAT} mode, where each operational mode corresponds to a particular operational ratio of the μC charge pump, μBB_{RATIO}. Table 1 shows, in

tabulated form, the relationships between the operational modes of the μC charge pump circuit 262A, the operational ratio of the μC charge pump, μBB_{RATIO}, and the μC charge pump output voltage, $V_{\mu C_OUT}$, substantially generated at the μC charge pump output.

5

MODE OF OPERATION OF µC CHARGE PUMP	OPERATIONAL RATIO OF µC CHARGE PUMP, (μBB_{RATIO})	µC CHARGE PUMP OUTPUT VOLTAGE, ($V_{\mu C_OUT}$), GENERATED AT µC CHARGE PUMP OUTPUT
OFF Mode	OFF	FLOATING
1 X V_{BAT} Mode	1	1 X V_{BAT}
4/3 X V_{BAT} Mode	4/3	4/3 X V_{BAT}
3/2 X V_{BAT} Mode	3/2	3/2 X V_{BAT}

TABLE 1

[00544] When the µC charge pump circuit 262A is configured to operate in the OFF mode, the µC charge pump circuit 262A is disabled and the µC charge pump output floats. When the µC charge pump circuit 262A is configured to operate in the 1 x V_{BAT} mode, the µC charge pump circuit 262A is configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to the supply input 24, (V_{BAT}). When the µC charge pump circuit 262A is configured to operate in the 4/3 x V_{BAT} mode, the µC charge pump circuit 262A is configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to the 4/3 x V_{BAT}. When the µC charge pump circuit 262A is configured to operate in the 3/2 x V_{BAT} mode, the µC charge pump circuit 262A is configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 3/2 x V_{BAT}.

[00545] The µC charge pump circuit 262A may include a µC charge pump control circuit 316A, a first flying capacitor 318 having a first terminal 318A and a second terminal 318B, a second flying capacitor 320 having a first terminal 320A, a second terminal, 320B and µC charge pump switching network having a plurality of switches including a first switch 322, (SW 1), a second switch 324, (SW 2), a third switch 326, (SW 3), a fourth switch 328, (SW 4), a fifth switch 330, (SW 5), a sixth switch 332, (SW 6), a seventh switch 334, (SW 7), an eighth switch 336, (SW 8), and a ninth switch 338, (SW 9). Each of the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3),

the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9) may be a solid state based switch implemented with field effect transistors, insulator-on-semiconductor based transistors, or bipolar based transistors, or a combination thereof. Each of the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9) may be a solid state transmission gate. As another example, each of the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9) may be based on a Gallium nitride process. Alternatively, each of the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9) may be micro-electromechanical systems (MEMS) contact type switches.

[00546] The first switch 322 may be coupled between the first terminal 320A of the second flying capacitor 320 and the supply input 24, (V_{BAT}). The first switch 322, (SW 1), may include a first switch control input configured to receive a first switch control signal 340 from the μC charge pump control circuit 316A, where the first switch control signal 340 operably opens and closes the first switch 322, (SW 1), based upon the operational mode of the μC charge pump circuit 262A. The second switch 324, (SW 2), may include a second switch control input configured to receive a second switch control signal 342 from the μC charge pump control circuit 316A, where the second switch control signal 342 operably opens and closes the second switch 324, (SW 2), based upon the operational mode of the μC charge pump circuit 262A. The second switch 324, (SW 2), may be coupled between the supply input 24, (V_{BAT}), and the second terminal 320B of the second flying capacitor 320. The third switch 326, (SW 3),

may include a third switch control input configured to receive a third switch control signal 344 from the μC charge pump control circuit 316A, where the third switch control signal 344 operably opens and closes the third switch 326, (SW 3), based upon the operational mode of the μC charge pump circuit 262A. The third switch 326, (SW 3), may be coupled between the second terminal 320B of the second flying capacitor 320 and ground. The fourth switch 328, (SW 4), may include a fourth switch control input configured to receive a fourth switch control signal 346 from the μC charge pump control circuit 316A, where the fourth switch control signal 346 operably opens and closes the fourth switch 328, (SW 4), based upon the operational mode of the μC charge pump circuit 262A. The fourth switch 328, (SW 4), may be coupled between the first terminal 320A of the second flying capacitor 320 and second terminal 318B of the first flying capacitor 318. The fifth switch 330, (SW 5), may include a fifth switch control input configured to receive a fifth switch control signal 348 from the μC charge pump control circuit 316A, where the fifth switch control signal 348 operably opens and closes the fifth switch 330, (SW 5), based upon the operational mode of the μC charge pump circuit 262A. The fifth switch 330, (SW 5), may be coupled between the second terminal 318B of the first flying capacitor 318 and second terminal 320B of the second flying capacitor 320. The sixth switch 332, (SW 6), may include a sixth switch control input configured to receive a sixth switch control signal 350 from the μC charge pump control circuit 316A, where the sixth switch control signal 350 operably opens and closes the sixth switch 332, (SW 6), based upon the operational mode of the μC charge pump circuit 262A. The sixth switch 332, (SW 6), may be coupled between the first terminal 318A of the first flying capacitor 318 and first terminal 320A of the second flying capacitor 320. The seventh switch 334, (SW 7), may include a seventh switch control input configured to receive a seventh switch control signal 352 from the μC charge pump control circuit 316A, where the seventh switch control signal 352 operably opens and closes the seventh switch 334 based upon the operational mode of the μC charge pump circuit 262A. The seventh switch 334, (SW 7), may be coupled between the second terminal 318B

of the first flying capacitor 318 and ground. The eighth switch 336, (SW 8), may include an eighth switch control input configured to receive an eighth switch control signal 354 from the μC charge pump control circuit 316A, where the eighth switch control signal 354 operably opens and closes the eighth switch 336, (SW 8), based upon the operational mode of the μC charge pump circuit 262A. The eighth switch 336, (SW 8), may be coupled between the second terminal 318B of the first flying capacitor 318 and the supply input 24, (V_{BAT}). The ninth switch 338, (SW 9), may include a ninth switch control input configured to receive a ninth switch control signal 356 from the μC charge pump control circuit 316A, where the ninth switch control signal 356 operably opens and closes the ninth switch 338, (SW 9), based upon the operational mode of the μC charge pump circuit 262A. The ninth switch 338, (SW 9), may be coupled between the first terminal 318A of the first flying capacitor 318 and the supply input 24, (V_{BAT}).

[00547] The μC charge pump control circuit 316A may be configured to couple to a μC charge pump clock 276 and a μC charge pump control bus 278. The μC charge pump control bus 278 may be used to configure the μC charge pump circuit 262A to operate in one of the four operational modes by setting an operational ratio of the μC charge pump, μBB_{RATIO}, of the μC charge pump circuit 262A, where the parameter corresponding to a selection of the operational ratio of the μC charge pump, μBB_{RATIO}, may be stored locally in the μC charge pump control circuit 316A. In addition, the μC charge pump control circuit 316A may use the μC charge pump clock 276 to operably switch between phases of operation of the μC charge pump circuit 262A. The switch state (open or closed) of each of the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9), may be changed depending upon the phase of operation of the μC charge pump circuit 262A. The relationship between the operational ratio of the μC charge pump, μBB_{RATIO}, the phase of operation of the μC charge pump circuit 262A, and the switch state of

the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9), is shown in TABLE 2.

	OPERATIONAL RATIO OF µC CHARGE PUMP, (μBB_{RATIO})			
SWITCHES	OFF	1	4/3	3/2
SW 1	OPEN	PHASE 1	PHASE 1 and PHASE 3	PHASE 2
SW 2	OPEN	OPEN	PHASE 2	PHASE 1
SW 3	OPEN	PHASE 1	PHASE 3	PHASE 2
SW 4	OPEN	OPEN	PHASE 1	OPEN
SW 5	OPEN	PHASE 1	PHASE 3	PHASE 2
SW 6	OPEN	PHASE	PHASE 2	PHASE 1
SW 7	OPEN	OPEN	PHASE 1 and PHASE 2	PHASE 1
SW 8	OPEN	OPEN	OPEN	PHASE 1
SW 9	OPEN	PHASE 1	OPEN	OPEN

TABLE 2

[00548] As used in TABLE 2, "PHASE 1" indicates the switch state (open or closed) of the identified switch is closed during a first phase of operation of the µC charge pump circuit 262A. "PHASE 2" indicates that the switch state (open or closed) of the identified switch is closed during a second phase of operation of the µC charge pump circuit 262A. "PHASE 3" indicates the switch state (open or closed) of the identified switch is closed during a third phase of operation of the µC charge pump circuit 262A. "OPEN" indicates the switch state (open or closed) of the identified switch is open during all the phases of operation of the µC charge pump circuit 262A. As depicted in Figure 19A, the µC charge pump circuit 262A generates the various µC charge pump output voltages described in TABLE 1 using only two flying capacitors, the first flying capacitor 318 and the second flying capacitor 320, and the µC charge pump output capacitor 357, $C_{\mu C_OUT}$.

[00549] As an example, the µC charge pump circuit 262A may be configured to operate in the OFF mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to OFF. When the operational ratio of the µC charge pump, μBB_{RATIO}, is set to OFF, the first switch 322, (SW 1), is configured to be open, the second switch 324, (SW 2), is configured to be open, the third switch 326, (SW 3), is configured to be open, the fourth switch 328, (SW 4), is configured to be open, the fifth switch 330, (SW 5), is configured to be open, the sixth switch 332, (SW 6), is configured to be open, the seventh switch 334, (SW 7), is configured to be open, the eighth switch 336, (SW 8), is configured to be open, and the ninth switch 338, (SW 9),is configured to be open at all times. Accordingly, the µC charge pump output voltage, $V_{\mu C_OUT}$, at the µC charge pump output floats with respect to ground when the µC charge pump circuit 262A is configured to operate in the OFF mode.

[00550] The µC charge pump circuit 262A may be configured to operate in the 4/3 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 4/3. When the operational ratio of the µC charge pump, μBB_{RATIO}, is set to 4/3, the µC charge pump circuit 262A may operate in a first phase, (PHASE 1), a second phase, (PHASE 2), and a third phase, (PHASE 3), as a function of the µC charge pump clock 276. Figure 20A depicts an example of the "effective" operation of the µC charge pump circuit 262A when the µC charge pump circuit 262A is configured to operate in either the first phase, (PHASE 1), the second phase, (PHASE 2), or the third phase, (PHASE 3). As depicted in Figure 20A, some embodiments of the µC charge pump circuit 262A may include a µC charge pump output capacitor 357, $C_{\mu C_OUT}$, coupled to the µC charge pump output. In some phases of operation, the µC charge pump output capacitor 357, $C_{\mu C_OUT}$, may store charge transferred from supply input 24, (V_{BAT}), to the µC charge pump output. In other phases of operation, the µC charge pump output capacitor 357, $C_{\mu C_OUT}$, may source previously transferred charge to the µC charge pump output.

[00551] As depicted in Figure 20A, during the first phase of operation, (PHASE 1), of the µC charge pump circuit 262A, when the µC charge pump

circuit 262A is configured to operate in the 4/3 x V_{BAT} mode, the switches of the μC charge pump circuit 262A are configured to couple the first terminal 318A of the first flying capacitor 318 to the supply input 24, (V_{BAT}), the second terminal 318B of the first flying capacitor 318 to the second terminal 320B of the second flying capacitor 320, and the first terminal 320A of the second flying capacitor 320 to the μC charge pump output. As a result, during the first phase of operation, (PHASE 1), of the μC charge pump circuit 262A, the μC charge pump circuit 262A delivers charge to the μC charge pump output capacitor, $C_{\mu C_OUT}$.

[00552] As further depicted in Figure 20A, during the second phase of operation, (PHASE 2), of the μC charge pump circuit 262A, when the μC charge pump circuit 262A is configured to operate in the 4/3 x V_{BAT} mode, the switches of the μC charge pump circuit 262A are configured to couple the second terminal 320B of the second flying capacitor 320 to the supply input 24, (V_{BAT}), the first terminal 320A of the second flying capacitor 320 to the first terminal 318A of the first flying capacitor 318 and the μC charge pump output, and decouple the second terminal 318B of the first flying capacitor 318 such that to the second terminal 318B of the first flying capacitor 318 floats relative to ground. As a result, during the second phase of operation, (PHASE 2), of the μC charge pump circuit 262A, the μC charge pump circuit 262A delivers charge to the μC charge pump output capacitor 357, $C_{\mu C_OUT}$.

[00553] As further depicted in Figure 20A, during the third phase of operation, (PHASE 3), of the μC charge pump circuit 262A, when the μC charge pump circuit 262A is configured to operate in the 4/3 x V_{BAT} mode, the switches of the μC charge pump circuit 262A are configured to couple the first terminal 320A of the second flying capacitor 320 to the supply input 24, (V_{BAT}), the second terminal 320B of the second flying capacitor 320 to the first terminal 318A of the first flying capacitor 318, and the second terminal 318B of the first flying capacitor 318 to ground. In addition, during the third phase of operation, (PHASE 3), of the μC charge pump circuit 262A, the μC charge pump output is decoupled from the first flying capacitor 318, the second flying capacitor, and the

supply input 24, (V_{BAT}), such that the charge previously stored in the µC charge pump output capacitor 357, $C_{\mu C_OUT}$, sources current to the µC charge pump output.

[00554] Accordingly, returning to TABLE 2, when the µC charge pump circuit 262A is configured to operate in the 4/3 x V_{BAT} mode, the first switch 322, (SW 1), is configured to be closed during the first phase of operation, (PHASE 1), the second switch 324, (SW 2), is configured to be closed during the second phase of operation, (PHASE 2), the third switch 326, (SW 3), is configured to be closed during the third phase of operation, (PHASE 3), the fourth switch 328, (SW 4), is configured to be closed during the third phase of operation, (PHASE 3), the fifth switch 330, (SW 5), is configured to be closed during the first phase of operation, (PHASE 1), and the sixth switch 332, (SW 6), is configured to be closed during the second phase of operation, (PHASE 2) of the µC charge pump circuit 262A. Otherwise, the µC charge pump control circuit 316A configures the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9), to be open. As a result, the µC charge pump output provides a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 4/3 x V_{BAT}.

[00555] As another example of the operation of the µC charge pump circuit 262A depicted in Figure 19A, the µC charge pump circuit 262A may be configured to operate in the 3/2 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 3/2. When the operational ratio of the µC charge pump, μBB_{RATIO}, is set to 3/2, the µC charge pump circuit 262A may operate in a first phase of operation, (PHASE 1) and a second phase of operation, (PHASE 2) dependent upon the µC charge pump clock 276. Figure 20B depicts the "effective" circuit topology of the µC charge pump circuit 262A during the first phase of operation, (PHASE 1) and a second phase of operation, (PHASE 2).

[00556] Illustratively, as depicted in Figure 20B, during the first phase of operation, (PHASE 1), of the µC charge pump circuit 262A, when the µC charge pump circuit 262A is configured to operate in the 3/2 x V_{BAT} mode, the switches of the µC charge pump circuit 262A are configured to couple the second terminal 318B of the first flying capacitor 318 and the second terminal 320B of the second flying capacitor 320 to the supply input 24, (V_{BAT}), the first terminal 318A of the first flying capacitor 318 and the first terminal 320A of the second flying capacitor 320 to the µC charge pump output. As a result, during the first phase of operation, (PHASE 1), of the µC charge pump circuit 262A, the µC charge pump circuit 262A delivers charge to the µC charge pump output capacitor 357, $C_{\mu C_OUT}$, from the supply input 24, (V_{BAT}), the first flying capacitor 318 and the second flying capacitor 320.

[00557] As further depicted in Figure 20B, during the second phase of operation, (PHASE 2), of the µC charge pump circuit 262A, when the µC charge pump circuit 262A is configured to operate in the 3/2 x V_{BAT} mode, the switches of the µC charge pump circuit 262A are configured to couple the first terminal 320A of the second flying capacitor 320 to the supply input 24, (V_{BAT}), the second terminal 320B of the second flying capacitor 320 to the first terminal 318A of the first flying capacitor 318, and the second terminal 318B of the first flying capacitor 318 to ground in order to charge the first flying capacitor 318 and the second flying capacitor 320 from the supply input 24, (V_{BAT}).

[00558] Accordingly, during the second phase of operation, (PHASE 2), of the µC charge pump circuit 262A, depicted in Figure 20 B, the µC charge pump output is decoupled from the first flying capacitor 318, the second flying capacitor, and the supply input 24, (V_{BAT}), such that the charge previously stored in the µC charge pump output capacitor 357, $C_{\mu C_OUT}$, sources current to the µC charge pump output.

[00559] Accordingly, returning to TABLE 2, when the µC charge pump circuit 262A is configured to operate in the 3/2 x V_{BAT} mode, the second switch 324, (SW 2), is configured to be closed during the first phase of operation,

(PHASE 1), the third switch 326, (SW 3), is configured to be closed during the second phase of operation, (PHASE 3), the fourth switch 328, (SW 4), is configured to be closed during the second phase of operation, (PHASE 2), the fifth switch 330, (SW 5), is configured to be closed during the first phase of operation, (PHASE 1), and the eighth switch 336, (SW 8), is configured to be closed during the first phase of operation, (PHASE 1) of the µC charge pump circuit 262A. Otherwise, the µC charge pump control circuit 316B configures the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9), to be open. As a result, the µC charge pump output provides a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 3/2 x V_{BAT}.

[00560] The µC charge pump circuit 262A may also be configured to operate in the 1 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 1. When the operational ratio of the µC charge pump, μBB_{RATIO}, is set to 1, the µC charge pump circuit 262A has one phase of operation, PHASE 1. Figure 20C depicts the "effective" circuit topology of the µC charge pump circuit 262A during the first phase of operation, (PHASE 1) when the µC charge pump circuit 262A is configured to operate in the 1 x V_{BAT} mode.

[00561] As depicted in Figure 20C, during the first phase of operation, (PHASE 1), of the µC charge pump circuit 262A, when the µC charge pump circuit 262A is configured to operate in the 1 x V_{BAT} mode, the switches of the µC charge pump circuit 262A are configured to couple the first terminal 320A of the second flying capacitor 320 to the supply input 24, (V_{BAT}), the second terminal 320B of the second flying capacitor 320 to the first terminal 318A of the first flying capacitor 318, and the second terminal 318B of the first flying capacitor 318 to ground in order to charge the first flying capacitor 318 and the second flying capacitor 320 from the supply input 24, (V_{BAT}). In addition, the supply input 24, (V_{BAT}), is coupled to the µC charge pump output such that

charge is delivered directly from the supply input 24, (V_{BAT}), to the μC charge pump output capacitor 357, $C_{\mu C_OUT}$.

[00562] As a result, shown in TABLE 2, the switch state of the first switch 322, (SW 1), the second switch 324, (SW 2), the third switch 326, (SW 3), the fourth switch 328, (SW 4), the fifth switch 330, (SW 5), the sixth switch 332, (SW 6), the seventh switch 334, (SW 7), the eighth switch 336, (SW 8), and the ninth switch 338, (SW 9), do not change over time. Accordingly, when the μC charge pump circuit 262A is configured to operate in the 1 x V_{BAT} mode, the first switch 322, (SW 1), is configured to be open, the second switch 324, (SW 2), is configured to be open, the third switch 326, (SW 3), is configured to be open, the fourth switch 328, (SW 4), is configured to be open, the fifth switch 330, (SW 5), is configured to be open, the sixth switch 332, (SW 6), is configured to be open, the seventh switch 334, (SW 7), is configured to be open, the eighth switch 336, (SW 8), is configured to be open, and the ninth switch 338, (SW 9), is configured to be closed at all times. As a result, the μC charge pump output generates a μC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1 x V_{BAT} because closing the ninth switch 338, (SW 9), couples the supply input 24, (V_{BAT}), to the μC charge pump output.

[00563] Figure 19B depicts another example embodiment of the μC charge pump circuit 262 of Figures 18A-D as a μC charge pump circuit 262B. Similar to the μC charge pump circuit 262A of Figure 19A, the μC charge pump circuit 262B may be configured to generate a μC charge pump output voltage, $V_{\mu C_OUT}$, at the μC charge pump output based upon an operational mode of the μC charge pump circuit 262B. However, unlike the μC charge pump circuit 262A, the μC charge pump circuit 262B may be configured to either "boost" or "buck" the supply input 24, (V_{BAT}), to generate the μC charge pump output voltage, $V_{\mu C_OUT}$, at the μC charge pump output. As an example, the operational modes of the μC charge pump circuit 262B may include an OFF mode, a 1/4 x V_{BAT} mode, 1/3 x V_{BAT} mode, a 1/2 x V_{BAT} mode, a 2/3 x V_{BAT} mode, 1 x V_{BAT} mode, a 4/3 x V_{BAT} mode, and a 3/2 x V_{BAT} mode, where each of the operational modes of the μC charge pump circuit 262B corresponds to a

particular operational ratio of the µC charge pump, μBB_{RATIO}. Table 3 shows, in tabulated form, the relationships between the operational modes of the µC charge pump circuit 262B, the operational ratio of the µC charge pump, μBB_{RATIO}, and the µC charge pump output voltage, $V_{\mu C_OUT}$, substantially generated at the µC charge pump output.

OPERATIONAL MODES OF µC CHARGE PUMP	OPERATIONAL RATIO OF µC CHARGE PUMP, (μBB_{RATIO})	µC CHARGE PUMP OUTPUT VOLTAGE, ($V_{\mu C_OUT}$), GENERATED AT µC CHARGE PUMP OUTPUT
OFF Mode	OFF	FLOATING
1/4 X V_{BAT} Mode	1/4	1/4 X V_{BAT}
1/3 X V_{BAT} Mode	1/3	1/3 X V_{BAT}
1/2 X V_{BAT} Mode	1/2	1/2 X V_{BAT}
2/3 X V_{BAT} Mode	2/3	2/3 X V_{BAT}
1 X V_{BAT} Mode	1	1 X V_{BAT}
4/3 X V_{BAT} Mode	4/3	4/3 X V_{BAT}
3/2 X V_{BAT} Mode	3/2	3/2 X V_{BAT}

TABLE 3

[00564] The operational modes of the µC charge pump circuit 262B are now described. As an example, when the µC charge pump circuit 262B is configured to operate in the OFF mode, the µC charge pump circuit 262B is disabled and the µC charge pump output floats. When the µC charge pump circuit 262B is configured to operate in the 1/4 x V_{BAT} mode, the µC charge pump circuit 262B is configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1/4 x the supply input 24, (V_{BAT}). When the µC charge pump circuit 262B is configured to operate in the 1/3 x V_{BAT} mode, the µC charge pump circuit 262B is configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1/3 x V_{BAT}. When the µC charge pump circuit 262B is configured to operate in the 1/2 x V_{BAT} mode, the µC charge pump circuit 262B is configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1/2 x V_{BAT}. When the µC charge pump circuit 262B is configured to operate in the 2/3 x V_{BAT} mode, the µC charge pump circuit 262B is configured to generate the µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 2/3

x V_{BAT}. When the µC charge pump circuit 262B is configured to operate in the 1 x V_{BAT} mode, the µC charge pump circuit 262B is configured to generate the µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1 x V_{BAT}. When the µC charge pump circuit 262B is configured to operate in the 4/3 x V_{BAT} mode, the µC charge pump circuit 262B is configured to generate the µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 4/3 x V_{BAT}. And, when the µC charge pump circuit 262B is configured to operate in the 3/2 x V_{BAT} mode, the µC charge pump circuit 262B is configured to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 3/2 x V_{BAT}. As depicted in Figure 19B, advantageously, the µC charge pump circuit 262B only includes two flying capacitors, the first flying capacitor 358 and the second flying capacitor 360, which are used to generate each the µC charge pump output voltage, $V_{\mu C_OUT}$, described in TABLE 3. As depicted in Figure 19B, the µC charge pump circuit 262A generates the various µC charge pump output voltages described in TABLE 1 using only two flying capacitors, the first flying capacitor 318 and the second flying capacitor 320, and the µC charge pump output capacitor 357, $C_{\mu C_OUT}$. In some phases of operation, the µC charge pump output capacitor 357, $C_{\mu C_OUT}$, may store charge transferred from supply input 24, (V_{BAT}), to the µC charge pump output. In other phases of operation, the µC charge pump output capacitor 357, $C_{\mu C_OUT}$, may source previously transferred charge to the µC charge pump output.

[00565] The µC charge pump circuit 262B may include a µC charge pump control circuit 316B, a first flying capacitor 358 having a first terminal 358A and a second terminal 358B, a second flying capacitor 360 having a first terminal 360A and a second terminal 360B, and a µC charge pump switching network including a first switch 362, (SW 1), a second switch 364, (SW 2), a third switch 366, (SW 3), a fourth switch 368, (SW 4), a fifth switch 370, (SW 5), a sixth switch 372, (SW 6), a seventh switch 374, (SW 7), an eighth switch 376, (SW 8), a ninth switch 378, (SW 9), a tenth switch 380, (SW 10), an eleventh switch 382, (SW 11), a twelfth switch 384, (SW 12), and a thirteenth switch 386, (SW 13). Each of the plurality of switches of the µC charge pump switching network in the

μC charge pump circuit 262B may be a solid state based switch implemented with field effect transistors, insulator-on-semiconductor based transistors, or bipolar based transistors, or a combination thereof. Each of the plurality of switches of the μC charge pump circuit 262B may be a solid state transmission gate. As another example, each of the plurality of switches of the μC charge pump circuit 262B may be based on a Gallium nitride process. Alternatively, each of the plurality of switches of the μC charge pump circuit 262B may be micro-electromechanical systems (MEMS) contact type switches.

[00566] Figure 19B depicts the μC charge pump switching network in relationship to the supply input 24, (V_{BAT}), the μC charge pump control circuit 316B, the first flying capacitor 358, the second flying capacitor 360m and the μC charge pump output capacitor 357, $C_{\mu C_OUT}$. As depicted in Figure 19B, the first switch 362, (SW 1), may be coupled between the first terminal 358A of the first flying capacitor 358 and the supply input 24, (V_{BAT}). The first switch 362, (SW 1), may include a first switch control input configured to receive a first switch control signal 388 from the μC charge pump control circuit 316B, where the first switch control signal 388 operably opens and closes the first switch 362, (SW 1), based upon the operational mode of the μC charge pump circuit 262B. The second switch 364, (SW 2), may include a second switch control input configured to receive a second switch control signal 390 from the μC charge pump control circuit 316B, where the second switch control signal 390 operably opens and closes the second switch 364, (SW 2), based upon the operational mode of the μC charge pump circuit 262B. The second switch 364, (SW 2), may be coupled between the first terminal 358A of the first flying capacitor 358 and the μC charge pump output. The third switch 366, (SW 3), may include a third switch control input configured to receive a third switch control signal 392 from the μC charge pump control circuit 316B, where the third switch control signal 392 operably opens and closes the third switch 366, (SW 3), based upon the operational mode of the μC charge pump circuit 262B. The third switch 366, (SW 3), may be coupled between the second terminal 358B of the first flying capacitor 358 and ground. The fourth switch 368, (SW 4), may include a fourth switch control input

configured to receive a fourth switch control signal 394 from the μC charge pump control circuit 316B, where the fourth switch control signal 394 operably opens and closes the fourth switch 368, (SW 4), based upon the operational mode of the μC charge pump circuit 262B. The fourth switch 368, (SW 4), may be coupled between the second terminal 358B of the first flying capacitor 358 and the μC charge pump output. The fifth switch 370, (SW 5), may include a fifth switch control input configured to receive a fifth switch control signal 396 from the μC charge pump control circuit 316B, where the fifth switch control signal 396 operably opens and closes the fifth switch 370, (SW 5), based upon the operational mode of the μC charge pump circuit 262B. The fifth switch 370, (SW 5), may be coupled between the second terminal 358B of the first flying capacitor 358 and first terminal 360A of the second flying capacitor 360. The sixth switch 372, (SW 6), may include a sixth switch control input configured to receive a sixth switch control signal 398 from the μC charge pump control circuit 316B, where the sixth switch control signal 398 operably opens and closes the sixth switch 372, (SW 6), based upon the operational mode of the μC charge pump circuit 262B. The sixth switch 372, (SW 6), may be coupled between the first terminal 360A of the second flying capacitor 360 and the supply input 24, (V_{BAT}). The seventh switch 374, (SW 7), may include a seventh switch control input configured to receive a seventh switch control signal 400 from the μC charge pump control circuit 316B, where the seventh switch control signal 400 operably opens and closes the seventh switch 374, (SW 7), based upon the operational mode of the μC charge pump circuit 262B. The seventh switch 374, (SW 7), may be coupled between the first terminal 360A of the second flying capacitor 360 and the μC charge pump output. The eighth switch 376, (SW 8), may include an eighth switch control input configured to receive an eighth switch control signal 402 from the μC charge pump control circuit 316B, where the eighth switch control signal 402 operably opens and closes the eighth switch 376, (SW 8), based upon the operational mode of the μC charge pump circuit 262B. The eighth switch 376, (SW 8), may be coupled between the second terminal 360B of the second flying capacitor 360 and ground. The ninth

switch 378, (SW 9), may include a ninth switch control input configured to receive a ninth switch control signal 404 from the μC charge pump control circuit 316B, where the ninth switch control signal 404 operably opens and closes the ninth switch 378, (SW 9), based upon the operational mode of the μC charge pump circuit 262B. The ninth switch 378, (SW 9), may be coupled between the second terminal 360B of the second flying capacitor 360 and the μC charge pump output. The tenth switch 380, (SW 10), may include a tenth switch control input configured to receive a tenth switch control signal 406 from the μC charge pump control circuit 316B, where the tenth switch control signal 406 operably opens and closes the tenth switch 380, (SW 10), based upon the operational mode of the μC charge pump circuit 262B. The tenth switch 380, (SW 10), may be coupled between the first terminal 358A of the first flying capacitor 358 and the first terminal 360A of the second flying capacitor 360. The eleventh switch 382, (SW 11), may include an eleventh switch control input configured to receive an eleventh switch control signal 408 from the μC charge pump control circuit 316B, where the eleventh switch control signal 408 operably opens and closes the eleventh switch 382, (SW 11), based upon the operational mode of the μC charge pump circuit 262B. The eleventh switch 382, (SW 11), may be coupled between the second terminal 358B of the first flying capacitor 358 and the supply input 24, (V_{BAT}). The twelfth switch 384, (SW 12), may include a twelfth switch control input configured to receive a twelfth switch control signal 410 from the μC charge pump control circuit 316B, where the twelfth switch control signal 410 operably opens and closes the twelfth switch 384, (SW 12), based upon the operational mode of the μC charge pump circuit 262B. The twelfth switch 384, (SW 12), may be coupled between the second terminal 360B of the second flying capacitor 360 and the supply input 24, (V_{BAT}). The thirteenth switch 386, (SW 13), may include a thirteenth switch control input configured to receive a thirteenth switch control signal 412 from the μC charge pump control circuit 316B, where the thirteenth switch control signal 412 operably opens and closes the thirteenth switch 386, (SW 13), based upon the operational mode of the μC charge pump circuit 262B. The thirteenth switch 386, (SW 13), may be

coupled between the second terminal 358B of the first flying capacitor 358 and the second terminal 360B of the second flying capacitor 360. Although not depicted in Figure 19B, some embodiments of the μC charge pump circuit 262B may further include a μC charge pump output capacitor 357, $C_{\mu C_OUT}$, coupled to the μC charge pump output in order to either store charge transferred from the supply input 24, (V_{BAT}), to the μC charge pump output or may source previously transferred charge to the μC charge pump output, as previously described relative to the operation of the μC charge pump circuit 262A.

[00567] Similar to the μC charge pump circuit 262A, the μC charge pump circuit 262B may be configured to operate in a respective operational mode based upon selection of an operational ratio of the μC charge pump, μBB_{RATIO}, that corresponds to the respective operational mode. Also, similar to TABLE 2, TABLE 4 provides the relationship between the operational ratio of the μC charge pump, μBB_{RATIO}, the phase of operation, and the switch state (open or closed) of the first switch 362, (SW 1), the second switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13).

[00568]

	OPERATIONAL RATIO OF µC CHARGE PUMP, (μBB_{RATIO})							
SWITCHES	OFF	1/4	1/3	1/2	2/3	1	4/3	3/2
SW 1	OPEN	PHASE 1	PHASE 1	PHASE 1	PHASE 1	PHASE 1 (CLOSED)	PHASE 1	PHASE 1
SW 2	OPEN	OPEN	PHASE 2	PHASE 2	PHASE 2	PHASE 1 (CLOSED)	PHASE 2	PHASE 2
SW 3	OPEN	PHASE 3	PHASE 2	PHASE 2	OPEN	OPEN	OPEN	OPEN
SW 4	OPEN	OPEN	OPEN	PHASE 1	PHASE 1	PHASE 1 (CLOSED)	OPEN	OPEN
SW 5	OPEN	PHASE 1	PHASE 1	OPEN	PHASE 2	OPEN	PHASE 1	PHASE 1
SW 6	OPEN	OPEN	OPEN	PHASE 1	PHASE 1	PHASE 1 (CLOSED)	PHASE 2	OPEN
SW 7	OPEN	PHASE 2	PHASE 2	PHASE 2	OPEN	PHASE 1 (CLOSED)	PHASE 3	PHASE 2
SW 8	OPEN	PHASE 2	PHASE 2	PHASE 2	PHASE 2	OPEN)	PHASE 1	PHASE 1
SW 9	OPEN	PHASE 1 & PHASE 3	PHASE 1	PHASE 1	PHASE 1	PHASE 1 (CLOSED)	OPEN	OPEN
SW 10	OPEN	PHASE 3	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
SW 11	OPEN	OPEN	OPEN	OPEN	OPEN	PHASE 1 (CLOSED)	OPEN	PHASE 2
SW 12	OPEN	OPEN	OPEN	OPEN	OPEN	PHASE 1 (CLOSED)	PHASE 3	PHASE 2
SW 13	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	PHASE 2	OPEN

TABLE 4

[00569] Similar to TABLE 2, in TABLE 4, "PHASE 1" indicates the switch state (open or closed) of the identified switch is closed during a first phase of operation of the μC charge pump circuit 262B. "PHASE 2" indicates the switch state (open or closed) of the identified switch is closed during a second phase of operation of the μC charge pump circuit 262B. "PHASE 3" indicates the switch state (open or closed) of the identified switch is closed during a third phase of operation of the μC charge pump circuit 262B. "OPEN" indicates the switch state (open or closed) of the identified switch is open during all the phases of operation of the μC charge pump circuit 262B.

[00570] Similar to the μC charge pump control circuit 316A, the controller 50, depicted in Figures 18A-D, may configure the μC charge pump control circuit 316B via the μC charge pump control bus 278 to operate in one of the operational modes, as shown in TABLE 3, by setting an operational ratio of the μC charge pump, μBB_{RATIO}, of the μC charge pump circuit 262B. Based on the operational ratio of the μC charge pump, μBB_{RATIO}, of the μC charge pump circuit 262B, the μC charge pump switching network is configured to couple only two flying capacitors, the first flying capacitor 358 and the second flying capacitor 360, with respect to one another, the supply voltage, (V_{BAT}), and the μC charge pump output capacitor 357, $C_{\mu C_OUT}$, to transfer charge to the μC charge pump output capacitor 357, $C_{\mu C_OUT}$, in order to provide a selected μC charge pump output voltage, $V_{\mu C_OUT}$. Also similar to the μC charge pump control circuit 316A, the μC charge pump control circuit 316B may store one or more parameters corresponding to a selection of the operational ratio of the μC charge pump, μBB_{RATIO}, locally in the μC charge pump control circuit 316B.

[00571] As an example, similar to the μC charge pump circuit 262A, the μC charge pump circuit 262B may be configured to operate in the OFF mode by setting the operational ratio of the μC charge pump, μBB_{RATIO}, to OFF. When the operational ratio of the μC charge pump, μBB_{RATIO}, is set to OFF, the first switch 362, (SW 1), is configured to be open, the second switch 364, (SW 2), is configured to be open, the third switch 366, (SW 3), is configured to be open, the fourth switch 368, (SW 4), is configured to be open, the fifth switch 370, (SW 5),

is configured to be open, the sixth switch 372, (SW 6), is configured to be open, the seventh switch 374, (SW 7), is configured to be open, the eighth switch 376, (SW 8), is configured to be open, the ninth switch 378, (SW 9), is configured to be open, the tenth switch 380, (SW 10), is configured to be open, the eleventh switch 382, (SW 11), is configured to be open, the twelfth switch 384, (SW 12), is configured to be open, and the thirteenth switch 386, (SW 13), is configured to be open at all times. Accordingly, the µC charge pump output voltage, $V_{\mu C_OUT}$, at the µC charge pump output floats with respect to ground when the µC charge pump circuit 262A is configured to operate in the OFF mode.

[00572] Also similar to the µC charge pump circuit 262A, the µC charge pump circuit 262B may be configured to operate in the 3/2 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 3/2. As indicated in Table 4, similar to the operation of the µC charge pump circuit 262A, when the operational ratio of the µC charge pump, μBB_{RATIO}, is set to 3/2, the µC charge pump circuit 262B may operate in a first phase of operation, (PHASE 1) and a second phase of operation, (PHASE 2) dependent upon the µC charge pump clock 276.

[00573] Accordingly, as indicated by TABLE 4, when the µC charge pump circuit 262B is configured to operate in the 3/2 x V_{BAT} mode, the first switch 362, (SW 1), the fifth switch 370, (SW 5), and the eighth switch 376, (SW 8), are configured to be closed when the µC charge pump circuit 262B operates in a first phase of operation, (PHASE 1). In addition, the second switch 364, (SW 2), the seventh switch 374, (SW 7), the eleventh switch 382, (SW 11) and the twelfth switch 384, (SW 12), are configured to be closed when the µC charge pump circuit 262B operates in a second phase of operation, (PHASE 2). Otherwise, the first switch 362, (SW 1), the second switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13), are configured to be open. As a result, the µC charge

pump output provides a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 3/2 x V_{BAT} when the µC charge pump circuit 262B is configured to operate in the 3/2 x V_{BAT} mode.

[00574] Also similar to the µC charge pump circuit 262A, the µC charge pump circuit 262B may be configured to operate in the 4/3 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 4/3. As indicated in TABLE 4, similar to the operation of the µC charge pump circuit 262A, when the operational ratio of the µC charge pump, μBB_{RATIO}, is set to 4/3, the µC charge pump circuit 262B may operate in a first phase of operation, (PHASE 1), a second phase of operation, (PHASE 2), and third phase of operation, (PHASE 3), dependent upon the µC charge pump clock 276.

[00575] Accordingly, as indicated by TABLE 4, when the µC charge pump circuit 262B is configured to operate in the 4/3 x V_{BAT} mode, the first switch 362, (SW 1), the fifth switch 370 (SW 5), and the eighth switch 376, (SW 8), are configured to be closed when the µC charge pump circuit 262B operates in a first phase of operation, (PHASE 1). In addition, the second switch 364 (SW 2), the sixth switch 372, (SW 6), and the thirteenth switch 386, (SW 13), are configured to be closed when the µC charge pump circuit 262B operates in a second phase of operation, (PHASE 2). Likewise, the seventh switch 374, (SW 7), and the twelfth switch 384, (SW 12), are configured to be closed when the µC charge pump circuit 262B operates in a third phase of operation, (PHASE 3). Otherwise, the first switch 362, (SW 1), the second switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13), are configured to be open. As a result, the µC charge pump output provides a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 4/3 x V_{BAT} when the µC charge pump circuit 262B is configured to operate in the 4/3 x V_{BAT} mode.

[00576] Also similar the µC charge pump circuit 262A, the µC charge pump circuit 262B may be configured to operate in the 1 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 1. As indicated in TABLE 4, similar to the operation of the µC charge pump circuit 262A, when the operational ratio of the µC charge pump, μBB_{RATIO}, is set to 1, the µC charge pump circuit 262B only operates in a first phase of operation, (PHASE 1) because the switches are statically switched into a configuration that provides a minimum impedance between the supply input 24, (V_{BAT}), and the µC charge pump output. In other words, when the µC charge pump circuit 262B is configured to operate in the 1 x V_{BAT} mode, the switch states of the indicated switches remain in either an open state or a closed state and do not change over time. The minimum impedance is provided by selectively turning on various switches to form parallel paths between the supply input 24, (V_{BAT}), and the µC charge pump output. Advantageously, the parallel paths lower the drop in voltage seen across the switches of the µC charge pump circuit 262B and reduce power consumption from the battery 20. However, for the sake of consistency with the other operational modes of the µC charge pump circuit 262B, the operation of the µC charge pump circuit 262B, when configured to operate in the 1 x V_{BAT} mode, is described as operating only in a first phase of operation (PHASE 1).

[00577] Accordingly, as indicated by TABLE 4, when the µC charge pump circuit 262B is configured to operate in the 1 x V_{BAT} mode, the first switch 362, (SW 1), the second switch 364, (SW 2), the fourth switch 368, (SW 4), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the ninth switch 378, (SW 9), the eleventh switch 382, (SW 11), and the twelfth switch 384, (SW 12), are configured to be closed. In addition, the third switch 366, (SW 3), the fifth switch 370, (SW 5), the eighth switch 376, (SW 8), the tenth switch 380, (SW 10), and the thirteenth switch 386, (SW 13), are configured to be open. As a result, the µC charge pump output provides a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1 x V_{BAT} when the µC charge pump circuit 262B is configured to operate in the 1 x V_{BAT} mode.

[00578] Also similar the µC charge pump circuit 262A, the µC charge pump circuit 262B may be configured to operate in the OFF mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to OFF. When the µC charge pump circuit 262B is configured to operate in the OFF mode, the µC charge pump circuit 262B is disabled and the µC charge pump output floats. As indicated by TABLE 4, when the µC charge pump circuit 262B is configured to operate in the OFF mode, the first switch 362, (SW 1), the second switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13), are configured to be open by the µC charge pump control circuit 316B. Accordingly, the µC charge pump output voltage, $V_{\mu C_OUT}$, at the µC charge pump output floats with respect to ground when the µC charge pump circuit 262B is configured to operate in the OFF mode.

[00579] Unlike the µC charge pump circuit 262A, the µC charge pump circuit 262B may be configured to operate in a 1/4 x V_{BAT} mode, 1/3 x V_{BAT} mode, a 1/2 x V_{BAT} mode, and a 2/3 x V_{BAT} mode,

[00580] The µC charge pump circuit 262B may be configured to operate in the 2/3 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 2/3. As indicated by TABLE 4, when the µC charge pump circuit 262B is configured to operate in the 2/3 x V_{BAT} mode, the first switch 362, (SW 1), the fourth switch 368, (SW 4), the sixth switch 372, (SW 6), and the ninth switch 378, (SW 9), are configured by the µC charge pump control circuit 316B to be closed when the µC charge pump circuit 262B operates in a first phase of operation, (PHASE 1). In addition, the µC charge pump control circuit 316B configures the second switch 364, (SW 2), the fifth switch 370, (SW 5), and the eighth switch 376, (SW 8), to be closed when the µC charge pump circuit 262B operates in a second phase of operation, (PHASE 2). Otherwise, the µC charge pump control circuit 316B configures the first switch 362, (SW 1), the second

switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13), to be open. As a result, the μC charge pump output provides a μC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 2/3 x V_{BAT} when the μC charge pump circuit 262B is configured to operate in the 2/3 x V_{BAT} mode.

[00581] The μC charge pump circuit 262B may be configured to operate in the 1/2 x V_{BAT} mode by setting the operational ratio of the μC charge pump, μBB_{RATIO}, to 1/2. As indicated by TABLE 4, when the μC charge pump circuit 262B is configured to operate in the 1/2 x V_{BAT} mode, the μC charge pump control circuit 316B configures the first switch 362, (SW 1), the fourth switch 368, (SW 4), the sixth switch 372, (SW 6), and the ninth switch 378, (SW 9), to be closed when the μC charge pump circuit 262B operates in a first phase of operation, (PHASE 1). In addition, the μC charge pump control circuit 316B configures the second switch 364, (SW 2), the third switch 366, (SW 3), the seventh switch 374, (SW 7), and the eighth switch 376, (SW 8), to be closed when the μC charge pump circuit 262B operates in a second phase of operation, (PHASE 2). Otherwise, the μC charge pump control circuit 316B configures the first switch 362, (SW 1), the second switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13), to be open. As a result, the μC charge pump output provides a μC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1/2 x V_{BAT} when the μC charge pump circuit 262B is configured to operate in the 1/2 x V_{BAT} mode.

[00582] The μC charge pump circuit 262B may be configured to operate in the 1/3 x V_{BAT} mode by setting the operational ratio of the μC charge pump,

μBB_{RATIO}, to 1/3. As indicated by TABLE 4, when the µC charge pump circuit 262B is configured to operate in the 1/3 x V_{BAT} mode, the µC charge pump control circuit 316B configures the first switch 362, (SW 1), the fifth switch 370, (SW 5), and the ninth switch 378, (SW 9), to be closed when the µC charge pump circuit 262B operates in a first phase of operation, (PHASE 1). In addition, the µC charge pump control circuit 316B configures the second switch 364, (SW 2), the third switch 366, (SW 3), the seventh switch 374, (SW 7), and the eighth switch 376, (SW 8), to be closed when the µC charge pump circuit 262B operates in a second phase of operation, (PHASE 2). Otherwise, the µC charge pump control circuit 316B configures the first switch 362, (SW 1), the second switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13), to be open. As a result, the µC charge pump output provides a µC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1/3 x V_{BAT} when the µC charge pump circuit 262B is configured to operate in the 1/3 x V_{BAT} mode.

[00583] The µC charge pump circuit 262B may be configured to operate in the 1/4 x V_{BAT} mode by setting the operational ratio of the µC charge pump, μBB_{RATIO}, to 1/4. Similar to the operation of the µC charge pump circuit 262A, when the µC charge pump circuit 262A is configured to operate in the 1/4 x V_{BAT} mode, the µC charge pump circuit 262B may include a first phase of operation, (PHASE 1), a second phase of operation, (PHASE 2), and a third phase of operation, (PHASE 3). As indicated by TABLE 4, when the µC charge pump circuit 262B is configured to operate in the 1/4 x V_{BAT} mode, the µC charge pump control circuit 316B configures the first switch 362, (SW 1), the fifth switch 370, (SW 5), and the ninth switch 378, (SW 9), to be closed when the µC charge pump circuit 262B operates in a first phase of operation, (PHASE 1). The µC charge pump control circuit 316B configures the seventh switch 374, (SW 7), and the eighth switch 376, (SW 8), to be closed when the µC charge pump

circuit 262B operates in a second phase of operation, (PHASE 2). The μC charge pump control circuit 316B configures the third switch 366, (SW 3), and the ninth switch 378, (SW 9), to be closed when the μC charge pump circuit 262B operates in a third phase of operation, (PHASE 3). Otherwise, the μC charge pump control circuit 316B configures the first switch 362, (SW 1), the second switch 364, (SW 2), the third switch 366, (SW 3), the fourth switch 368, (SW 4), the fifth switch 370, (SW 5), the sixth switch 372, (SW 6), the seventh switch 374, (SW 7), the eighth switch 376, (SW 8), the ninth switch 378, (SW 9), the tenth switch 380, (SW 10), the eleventh switch 382, (SW 11), the twelfth switch 384, (SW 12), and the thirteenth switch 386, (SW 13), to be open. As a result, the μC charge pump output provides a μC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1/4 x V_{BAT} when the μC charge pump circuit 262B is configured to operate in the 1/4 x V_{BAT} mode.

[00584] Figure 21 depicts a method 1000 to permit the controller 50, depicted in Figures 18A-D, to selectively configure the μC charge pump prior to transmission of a data burst by a linear radio frequency power amplifier. Accordingly, the description of method 1000 will be done with continuing reference to Figures 18A-D.

[00585] Prior to transmission of the data burst, the pseudo-envelope follower power management systems 10C-F may configure the μC charge pump circuit 262 and the V_{OFFSET} loop circuit 41A-B in order to provide a power amplifier supply voltage, V_{CC}, that is sufficient to power the linear radio frequency power amplifier during the transmission of the data burst. Accordingly, prior to initiation of a transmission of data by the linear radio frequency power amplifier, the controller 50 may determine the expected envelope characteristics of the signal to be transmitted. An example transmission of data may occur in a burst transmission time-slot. To determine the expected envelope characteristics of the signal to be transmitted, the controller 50 may consider the impact of data rate, the bandwidth of the channel and/or the type of modulation. Example types of modulation may include, but are not limited to quadrature phase shift keys (QPSK), or quadrature amplitude modulation (QAM). Alternatively, or in addition,

the controller 50 may determine and consider the peak-to-average ratio characteristic of the waveform to be generated by the linear radio frequency power amplifier 22.

[00586] Based upon an expected envelope characteristic of a signal to be transmitted by a power amplifier and a battery voltage, V_{BAT}, the controller 50 may be configured to determine a minimum operational ratio of a μC charge pump, μBB_{RATIO_MIN}. (Step 1002). In order to determine the minimum operational ratio of a μC charge pump, μBB_{RATIO_MIN}, the controller uses the expected envelope characteristics of the signal to be transmitted to determine the expected peak to peak swing of the power amplifier supply voltage, V_{CC_PKPK}, and obtains a measurement of the battery voltage, V_{BAT}, from the battery level sense circuit 264, as present on the supply input 24, (V_{BAT}). The expected peak to peak swing of the power amplifier supply voltage, V_{CC_PKPK}, represents the dynamic range of voltages that the controller 50 expects to be generated on the power amplifier supply voltage, V_{CC}, during the transmission of data. Effectively, the expected peak to peak swing of the power amplifier supply voltage, V_{CC_PKPK}, equals the difference between maximum expected power amplifier supply voltage, V_{CC_MAX}, and the minimum expected power amplifier supply voltage, V_{CC_MIN}, that the controller 50 expects to be generated on the power amplifier supply voltage, V_{CC}, during the data transmission.

[00587] In addition to the expected peak to peak swing of the power amplifier supply voltage, V_{CC_PKPK}, the controller may also take into consideration the minimum headroom voltage, $V_{HEADROOM}$, of the switching elements of the parallel amplifier 35. As an example, referring to Figures 12E-F, the controller 50 may consider the minimum headroom voltage, $V_{HEADROOM}$, for the first switching element, SW_{1A}, 214, and a second switching element, SW_{1B}, 216. In addition, in some embodiments, the controller 50 may consider the minimum headroom for each of the switching devices (SW_{1A}, 214 and SW_{1B}, 216) individually. As an example, for the case where the first switching element, SW_{1A}, 214 is a PFET device, the controller 50 may use the minimum PFET headroom voltage, $V_{HEADROOM_P}$, to determine the operational ratio of a μC charge pump, μBB_{RATIO}.

In the case where the second switching element, SW_{1B}, 216 is an NFET device, the controller 50 may use the minimum NFET headroom voltage, $V_{HEADROOM_N}$ to determine the operational ratio of a µC charge pump, μBB_{RATIO}.

[00588] Accordingly, in the general case, the controller 50 may determine the minimum operational ratio of a µC charge pump, μBB_{RATIO_MIN}, as shown in equation (1) as follows:

$$(1) \quad \mu BB_{RATIO_MIN} = [\ V_{CC_PKPK} + V_{HEADROOM_N} + V_{HEADROOM_P}\ ]/V_{BAT}$$

[00589] Based on the minimum operational ratio of the µC charge pump, μBB_{RATIO_MIN}, the controller 50 may be configured to select an operational ratio of the µC charge pump, μBB_{RATIO}, that is greater than the minimum operational ratio of the µC charge pump, μBB_{RATIO_MIN}, wherein V_{BAT} x μBB_{RATIO_MIN} is the minimum parallel amplifier supply voltage. (Step 1004). As indicated by TABLES 1 and 3, the available values of operational ratios of the µC charge pump, μBB_{RATIO}, depend upon the embodiment of the µC charge pump circuit 262. As an example, the embodiment of the µC charge pump circuit 262A, depicted in Figure 19A, provides several modes of operation where each mode of operation is associated with an operational ratio of the µC charge pump, μBB_{RATIO}, as shown in TABLE 1. Likewise, the example embodiment of the µC charge pump circuit 262B, depicted in Figure 19B, provides a number of modes of operation where each mode of operation is associated with an operational ratio of the µC charge pump, μBB_{RATIO}, as shown in TABLE 3. Depending upon the calculated value of the minimum operational ratio of a µC charge pump, μBB_{RATIO_MIN}, the controller 50 initially selects the smallest available operational ratio of the µC charge pump, μBB_{RATIO}, of the µC charge pump circuit 262 that is greater than the minimum operational ratio of a µC charge pump, μBB_{RATIO_MIN}. As an example, in the case where the µC charge pump circuit 262 is similar to the µC charge pump circuit 262B of Figure 19B (TABLE 3), if the minimum operational ratio of a µC charge pump, μBB_{RATIO_MIN}, is greater than 1/4 but less

than 1/3, the controller initially selects the operational ratio of the µC charge pump, μBB_{RATIO}, to be 1/3.

[00590] Thereafter, the controller 50 may be configured to calculate an expected offset in voltage, $V_{OFFSET_EXPECTED}$, to be generated as the offset voltage, V_{OFFSET},across a coupling device based upon the operational ratio of the µC charge pump, μBB_{RATIO}, of the µC charge pump, selected by the controller 50 (Step 1006). The expected offset voltage, $V_{OFFSET_EXPECTED}$, may be calculated as shown in equation (2) as follows:

(2) $$V_{OFFSET_EXPECTED} = V_{CC_MAX} - V_{BAT} \times \mu BB_{RATIO} + V_{HEADROOM_P}$$

[00591] Thereafter, the controller 50 may be configured to determine whether the expected offset voltage, $V_{OFFSET_EXPECTED}$, to be generated across the coupling device is greater than zero: $V_{OFFSET_EXPECTED}$, > 0. (Step 1008). In some alternative embodiments of method 1000, the controller 50 may determine whether the expected value for the expected offset voltage, $V_{OFFSET_EXPECTED}$, to be generated across the coupling device is greater than a minimum offset voltage, V_{OFFSET_MIN}, where the minimum offset voltage, V_{OFFSET_MIN}, is a configurable parameter. In this example embodiment of method 1000, it will be understood that the minimum offset voltage, V_{OFFSET_MIN}, is zero.

[00592] If the expected value for the offset voltage, V_{OFFSET}, to be generated across the coupling device is less than zero, $V_{OFFSET_EXPECTED}$, < 0, the controller 50 increments the value of the operational ratio of the µC charge pump, μBB_{RATIO}, to the next highest value of the operational ratio of the µC charge pump, μBB_{RATIO}, available for the µC charge pump circuit 262. (Step 1010). For example, in the case where the µC charge pump circuit 262 is similar to the µC charge pump circuit 262B of Figure 19B, if the initially determined value of the operational ratio of the µC charge pump, μBB_{RATIO}, of the µC charge pump circuit 262B is 1/3, the controller 50 will increment the value of the operational ratio of the µC charge pump, μBB_{RATIO}, to 1/2. Thereafter, method 1000 returns to Step 1008 to recalculate the expected value for an expected offset voltage,

$V_{OFFSET_EXPECTED}$, using the new value of the operational ratio of the μC charge pump, μBB_{RATIO}. This process continues until the controller 50 identifies the minimum value of the operational ratio of the μC charge pump, μBB_{RATIO}, of the μC charge pump circuit 262 for which the expected offset voltage, $V_{OFFSET_EXPECTED}$, is greater than zero volts.

[00593] After identifying the minimum value of the operational ratio of the μC charge pump, μBB_{RATIO}, of the μC charge pump circuit 262 for which the expected offset voltage, $V_{OFFSET_EXPECTED}$, is greater than zero volts, the controller 50 selects the operational ratio of the μC charge pump, μBB_{RATIO}, as a selected operational ratio of a μC charge pump, μBB_{RATIO_SEL}, to be used during the data transmission by the linear radio frequency power amplifier. (Step 1012). Alternatively, equation (2) may be rearranged to determine the minimum operational ratio of a μC charge pump, μBB_{RATIO}, to provide a minimum offset voltage, V_{OFFSET_MIN}, by setting the expected offset voltage, $V_{OFFSET_EXPECTED}$, equal to the minimum offset voltage, V_{OFFSET_MIN}. As a result, the minimum operational ratio of a μC charge pump, $\mu BB_{RATIO_OFFSET_MIN}$, is provided by equation (2.a) as follows:

$$(2.a) \qquad \mu BB_{RATIO_OFFSET_MIN} = [V_{CC_MAX} - V_{OFFSET_MIN} + V_{HEADROOM_P}]/V_{BAT}$$

[00594] Thus, although not depicted in Figure 21, in some embodiments, steps 1008, and 1010 may be replaced or eliminated by calculating the minimum offset voltage operational ratio of the μC charge pump, $\mu BB_{RATIO_OFFSET_MIN}$, and selecting the larger of the minimum operational ratio of a μC charge pump, μBB_{RATIO_MIN}, and the minimum offset voltage operational ratio of the μC charge pump, $\mu BB_{RATIO_OFFSET_MIN}$, as the minimum operational ratio of a μC charge pump, μBB_{RATIO_MIN}, used in step (1002). The controller 50 selects the operational ratio of the μC charge pump, μBB_{RATIO}, having the smallest value from among the one or more of the plurality of available operational ratios that are at least equal to both the minimum operational ratio of the μC charge pump, μBB_{RATIO}, and the minimum offset voltage operational ratio of the μC charge

pump, $\mu BB_{RATIO_OFFSET_MIN}$, as the selected operational ratio of the charge pump, μBB_{RATIO_SEL}. In some embodiments, the controller 50 determines which of the minimum operational ratio of a µC charge pump, μBB_{RATIO_MIN}, and the minimum offset voltage operational ratio of the µC charge pump, $\mu BB_{RATIO_OFFSET_MIN}$, has the greatest value. Based on the determination, the controller 50 sets the minimum operational ratio of the µC charge pump, μBB_{RATIO}, equal to the one of the minimum operational ratio of a µC charge pump, μBB_{RATIO_MIN}, and the minimum offset voltage operational ratio of the µC charge pump, $\mu BB_{RATIO_OFFSET_MIN}$, having the greatest value. Thereafter, the controller 50 selects the smallest of the available operational ratio of the charge pump from the one or more of the plurality of operational ratios that is at least equal to the minimum operational ratio of the µC charge pump, μBB_{RATIO_MIN}, as the selected operational ratio of the charge pump, μBB_{RATIO_SEL}. Via the µC charge pump control bus 278, the controller 50 configures the µC charge pump circuit 262 to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, on the µC charge pump output based upon the selected operational ratio of a µC charge pump, μBB_{RATIO_SEL}. (Step 1014).

[00595] Thereafter, in some embodiments of method 1000, the controller 50 configures the V_{OFFSET} loop circuit 41A-B to generate an offset voltage, V_{OFFSET}, substantially equal to a target expected offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, when the µC charge pump circuit 262 uses the selected operational ratio of a µC charge pump, μBB_{RATIO_SEL}. (Step 1016). Accordingly, the controller 50 may be configured to calculate the value of an expected target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, when the µC charge pump circuit 262 is configured to operate using the selected operational ratio of a µC charge pump, μBB_{RATIO_SEL}. The parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, is calculated by multiplying the supply voltage provided to the µC charge pump by the selected operational ratio of a µC charge pump, μBB_{RATIO_SEL}. For example, for the case where the supply voltage provided to the µC charge pump is the battery voltage, V_{BAT}, from the battery 20, the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, equals a product of the battery voltage, V_{BAT}, and the selected operational ratio of

a μC charge pump, μBB_{RATIO_SEL}. The value of the expected target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, may be calculated as shown in equation (3) as follows:

(3) $$V_{OFFSET_TARGET_EXPECTED} = V_{CC_PKPK} - V_{BAT} \times \mu BB_{RATIO_SEL} + V_{HEADROOM_P}$$

[00596] Thereafter, the controller 50 may be configured to use the value of the expected target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, to determine the value of target offset voltage parameter, V_{OFFSET_TARGET}, to be provided to the V_{OFFSET} loop circuits 41A-B. Via the μC charge pump control bus 278, the controller 50 provides the target offset voltage parameter, V_{OFFSET_TARGET}, to the V_{OFFSET} loop circuits 41A-B. Accordingly, as shown by method 1000, a target offset voltage parameter, V_{OFFSET_TARGET}, may also be determined based on an expected envelope characteristics of the signal to be transmitted prior to a data transmission. Based on the updated target offset voltage parameter, V_{OFFSET_TARGET}, various embodiments of the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B may be configured to pre-charge the coupling circuit 18, as depicted in Figures 18A-D. For example, based on the updated target offset voltage parameter, V_{OFFSET_TARGET}, various embodiments of the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B may operate in a pre-charge mode of operation for a predetermined period of time prior to the commencement of the data transmission, as discussed relative to a method 1100, depicted in Figure 22.

[00597] A method 1100, depicted in Figure 22, is described with continuing reference to Figures 18B and 18D. The method 1100 provides for the configuration of a V_{OFFSET} loop circuit 41B, depicted in Figures 18B and 18D, to minimize a pre-charging time period of the coupling circuit 18 to a desired offset voltage, V_{OFFSET}, prior to commencing a transmission, by the linear radio frequency power amplifier 22 (Figure 1A-B) of a data burst in a transmission-slot. As an example, prior to commencing the transmission of the data burst, the controller 50 may determine whether a coupling circuit 18 coupled between a parallel amplifier output 32A and a power amplifier supply voltage, V_{CC}, requires

pre-charging prior to initiation of the transmission by a radio frequency power amplifier, (Step 1102). Illustratively, the controller 50 may determine whether a data burst to be transmitted is a first data burst of a transmission of data by the linear radio frequency power amplifier 22. If the data burst to be transmitted is a first data burst of the transmission, the controller 50 may determine that the coupling circuit 18 requires pre-charging prior to transmission of the first data burst.

[00598] Alternatively, the controller 50 may determine whether the coupling circuit 18 requires pre-charging based upon the V_{OFFSET} error signal 304 generated by the summing circuit 300. As an example, the controller 50 may set the value of the V_{OFFSET_TARGET} parameter for the V_{OFFSET} loop circuit 41B. Thereafter, the controller 50 may obtain the V_{OFFSET} error signal 304 from the V_{OFFSET} loop circuit 41B via the V_{OFFSET} control bus 312. If the V_{OFFSET} error signal 304 is greater than a maximum V_{OFFSET} error threshold parameter, the controller 50 determines that the power amplifier supply voltage, V_{CC}, requires pre-charging prior to initiation of transmission of the first burst.

[00599] In response to the determination that the coupling circuit between the parallel amplifier and the power amplifier supply voltage, V_{CC}, requires pre-charging, the controller 50 may configure the V_{OFFSET} loop circuit 41B such that the V_{OFFSET} loop circuit 41B operates in a first bandwidth mode, where the first bandwidth mode increases the operable bandwidth of the V_{OFFSET} loop circuit 41B. (Step 1104). Alternatively or in addition, in some embodiments, for example, the controller 50 may provide an indication to the V_{OFFSET} loop circuit 41B that a data transmission is about to commence. For example, the V_{OFFSET} loop circuit 41B, may automatically determine whether a coupling circuit 18, depicted in Figure 18B and Figure 18D, requires pre-charging upon receiving an updated value of the target offset voltage parameter, V_{OFFSET_TARGET}. As a result, the control circuit (not shown) of the V_{OFFSET} loop circuit 41B may determine that the coupling circuit requires pre-charging based on the V_{OFFSET} error signal 304 and place the V_{OFFSET} loop circuit 41B in one of a pre-charge mode of operation or a normal operational mode of operation based on whether

the V_{OFFSET} error signal 304 exceeds the maximum V_{OFFSET} error threshold parameter.

[00600] As discussed relative to the description of Figures 18B and 18D, the integrator with zero compensation 314 may include a first time constant, Tau_0, and a second time constant, Tau_1. During normal operation of the V_{OFFSET} loop circuit 41B, the values of the first time constant, Tau_0, and a second time constant, Tau_1, may be configured to optimize regulation of the offset voltage, V_{OFFSET}, that is developed across the coupling circuit 18. For example, the controller 50 may configure the V_{OFFSET} loop circuit 41B to operate with a normal frequency bandwidth. Illustratively, to configure the V_{OFFSET} loop circuit 41B to operate with a normal frequency bandwidth, the controller 50 may configure the first time constant, Tau_0, to be equal to Tau_0_normal and the second time constant, Tau_1, to be equal to Tau_1_normal. In some embodiments of the V_{OFFSET} loop circuit 41B, the values of time constants Tau_0_normal and Tau_1_normal, may be stored locally with the V_{OFFSET} loop circuit 41B.

[00601] To decrease the time for pre-charging the coupling circuit 18, the controller may configure the first time constant, Tau_0, to be equal to a first startup time constant, Tau_0_startup, and the second time constant, Tau_1, to be equal to a second startup time constant, Tau_1_startup. Alternatively, some embodiments of the V_{OFFSET} loop circuit 41B may be configured to automatically set the first time constant, Tau_0, equal to the first startup time constant, Tau_0_startup, and the second time constant, Tau_1, when the V_{OFFSET} loop circuit 41B is placed in a pre-charge mode of operation.

[00602] In some embodiments of method 1100, the controller 50 may configure the V_{OFFSET} loop circuit 41B to initially operate using the first startup time constant, Tau_0_startup, and the second startup time constant, Tau_1_startup, by configuring the V_{OFFSET} loop circuit 41B operate in the pre-charge mode of operation for a period of time. As an example, in some embodiments of the V_{OFFSET} loop circuit 41B, the period of time in which the V_{OFFSET} loop circuit 41B operates in a pre-charge mode of operation may be configured by the controller 50 via the V_{OFFSET} control bus 312. In some embodiments of the

V_{OFFSET} loop circuit 41B, the period of time in which the V_{OFFSET} loop circuit 41B operates in a pre-charge mode of operation is a predetermined time period that may be configured by the controller 50 via V_{OFFSET} control bus 312. As an example, the V_{OFFSET} loop circuit 41B may include a pre-charge timer (not shown) that may be set to trigger a timer event after the predetermined time period.

[00603] Once the coupling circuit 18 is pre-charged, the V_{OFFSET} loop circuit 41B may be placed into a normal mode of operation. As an example, after a predetermined time period, the V_{OFFSET} loop circuit 41B may be re-configured such that the V_{OFFSET} loop circuit operates 41B in a second bandwidth mode, where the second bandwidth mode decreases the operable bandwidth of the V_{OFFSET} loop circuit 41B. (Step 1106). Accordingly, the bandwidth of the V_{OFFSET} loop circuit 41B that operates in the first bandwidth mode is greater than the bandwidth of the V_{OFFSET} loop circuit 41B that operates in the second bandwidth mode.

[00604] As an example, in order to place the V_{OFFSET} loop circuit 41B into the second bandwidth mode for normal operation during transmission of data by the linear radio frequency power amplifier 22, the controller 50 may configure the first time constant, Tau_0, to be equal to Tau_0_normal and the second time constant, Tau_1, to be equal to Tau_1_normal via the V_{OFFSET} control bus 312. Alternatively, as an example, V_{OFFSET} loop circuit 41B may automatically switch from the pre-charge mode of operation to a normal mode of operation upon triggering of the timer event by the pre-charge timer. Alternatively, or in addition, the control circuit (not shown) of the V_{OFFSET} loop circuit 41B may be configured to set the first time constant, Tau_0, and the second time constant, Tau_1, depending on whether the V_{OFFSET} loop circuit 41B is in a pre-charge mode of operation or a normal mode of operation. Although not previously described, the V_{OFFSET} loop circuit 41B may be likewise configured to operate in a pre-charge mode of operation or a normal mode of operation by automatically changing the values of the K_{ERROR_GAIN} value in a similar fashion as the V_{OFFSET} loop circuit 41B. For example, in some embodiments, the controller 50 may provide an indication to the V_{OFFSET} loop circuit 41A that a data transmission is about to commence.

Alternatively, for example, the V_{OFFSET} loop circuit 41A, may automatically determine whether a coupling circuit 18, depicted in Figure 18A and Figure 18C, requires pre-charging upon receiving an updated value of the target offset voltage parameter, V_{OFFSET_TARGET}. For example, in the pre-charge mode of operation, the V_{OFFSET} loop circuit 41A may be configured to set the K_{ERROR_GAIN} value to a pre-charge K_{ERROR_GAIN} value and in the nomal mode of operation, set the K_{ERROR_GAIN} value to a normal operation K_{ERROR_GAIN} value, where the pre-charge K_{ERROR_GAIN} value is greater than the normal operation K_{ERROR_GAIN} value. Effectively, the loop gain of the V_{OFFSET} loop circuit 41A is modified for a pre-determined period of time to permit the offset voltage across the coupling circuit 18 to be adjusted more rapidly than during normal operation. As a result, the offset voltage across the coupling circuit 18 may settle to a desired offset voltage based on the target offset voltage parameter, V_{OFFSET_TARGET}, prior to a data transmission. As previously described, because an expected target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, may be determined based on an expected envelope characteristics of the signal to be transmitted prior to a data transmission, a determination to operate in a pre-charge mode of operation for a predetermined period of time may be made based on the expected envelop characteristic of the signal to be transmitted.

[00605] Embodiments of an open loop ripple compensation assist circuit 414, depicted in Figures 23A-23D, will now be described. In order to provide context and not by way of limitation, the open loop ripple compensation assist circuit 414 will be described in the context of the example embodiments of a pseudo-envelope follower power management system 10MA, depicted in Figure 23A and Figure 23C, and a pseudo-envelope follower power management system 10MB, depicted in Figure 23B and Figure 23D.

[00606] Figures 23A-D depict the pseudo-envelope follower power management system 10MA and pseudo-envelope follower power management system 10MB, employ a switch mode power supply converter in combination with either an embodiment of the parallel amplifier circuit 14MA or an embodiment of the parallel amplifier circuit 14MB to provide techniques for modulating the power

amplifier supply voltage, V_{CC}, generated at the power amplifier supply output 28 for use by the linear radio frequency power amplifier 22.

[00607] As an example of a switch mode power supply converter, as depicted in Figure 23A, the pseudo-envelope follower power management system 10MA may include an embodiment of a multi-level charge pump buck converter 12M configured to interface with the parallel amplifier circuit 14MA. As another example of a configuration that includes a switch mode power supply converter, as depicted in Figure 23C, an alternative embodiment of the pseudo-envelope follower power management system 10MA may include an embodiment of a multi-level charge pump buck converter 12M configured to interface with the parallel amplifier circuit 14MB. As depicted in both Figure 23A and Figure 23C, the interface between the multi-level charge pump buck converter 12M and either the parallel amplifier circuit 14MA or the parallel amplifier circuit 14MB may be configured to provide a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, or a combination thereof, to the multi-level charge pump buck converter 12M.

[00608] As depicted in Figure 23A and Figure 23C, and not by way of limitation, some embodiments of the multi-level charge pump buck converter 12M may include a frequency locked loop circuit 54 similar to the frequency locked loop circuit 54 of the multi-level charge pump buck converter 12B, depicted in Figure 2B. For example, some embodiments of the multi-level charge pump buck converter 12M may include a switcher control circuit 52 similar to the switcher control circuit 52A, depicted in Figure 3A, or the switcher control circuit 52B, depicted in Figure 3B. However, alternative embodiments of the multi-level charge pump buck converter 12M, similar to the embodiments of the multi-level charge pump buck converter 12B that include an embodiment of the switcher control circuit 52 similar to the switcher control circuit 52C, depicted in Figure 3C, and/or the switcher control circuit 52D, depicted in Figure 3D, may not include a frequency locked loop circuit 54. Accordingly, operation of the multi-level charge pump buck converter 12M and the switcher control circuit 52, depicted in Figure 23A and Figure 23C, may also incorporate various

combinations of the operational features and functions of the embodiments of the switcher control circuits 52A-D, depicted in Figures 3A-D, the threshold detector and control circuits 132A-D, depicted in Figures 4A-D, and the circuitry and state machines depicted in Figures 5A-D and Figure 6A-D that are associated with the logic circuits 148A-D, depicted in Figures 4A-D.

[00609] As another example of a switch mode power supply converter, as depicted in Figure 23B, an embodiment of the pseudo-envelope follower power management system 10MB may include an embodiment of a buck converter 13L configured to interface with the parallel amplifier circuit 14MA. As another example of a configuration that includes a switch mode power supply converter, as depicted in Figure 23D, an alternative embodiment of the pseudo-envelope follower power management system 10MB may include an embodiment of the buck converter 13L configured to interface with the parallel amplifier circuit 14MB. As depicted in both Figure 23B and Figure 23D, the interface between the buck converter 13L and either the parallel amplifier circuit 14MA or the parallel amplifier circuit 14MB may be configured to provide a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, or a combination thereof, to the buck converter 13L. Likewise, similar to the buck converter 13A depicted in Figure 18C and Figure 18D, and not by way of limitation, some embodiments of the buck converter 13L may also include the frequency locked loop circuit 54, as depicted in Figure 23B and Figure 23D. For example, some embodiments of the buck converter 13L may include a switcher control circuit 259 similar to the switcher control circuit 52E, depicted in Figure 3E, or the switcher control circuit 52F, depicted in Figure 3F. Alternatively, some embodiments of the buck converter 13L similar to the embodiments of the buck converter 13A, depicted in Figure 18C and Figure 18D that include an embodiment of the switcher control circuit 259 similar to the switcher control circuit 52G, depicted in Figure 3G, or the switcher control circuit 52H, depicted in Figure 3H, may not include the frequency locked loop circuit 54. Accordingly, operation of the buck converter 13L and the switcher control circuit 259, depicted in Figure 23B and

Figure 23D, may also incorporate various combinations of the operational features and functions of the embodiments of the switcher control circuits 52E-H, depicted in Figures 3E-H, the threshold detector and control circuits 132E-H, depicted in Figures 4E-H, and the circuitry and state machine depicted in Figures 5E-H that are associated with the logic circuits 148E-H, depicted in Figures 4E-H.

[00610] Similar to the various example pseudo-envelope follower power management systems described above, the embodiments of the pseudo-envelope follower power management system 10MA and the pseudo-envelope follower power management system 10MB, depicted respectively in Figure 23A, Figure 23C, Figure 23B, and Figure 23D, may be configured to use modulated supply techniques to control the power amplifier supply voltage, V_{CC}, generated on the power amplifier supply output 28 in order to meet various communication system standards implemented in various communication devices. Example communication devices may include mobile terminals and mobile phones. Some of the communication system standards may include the use of wide-band modulation to send and receive information and data over a communication network.

[00611] As an example, the Long Term Evolution (LTE) communication standard may use wide-bandwidth modulation in specified transmission frequency bands and receive frequency bands to communicate information and data via the linear radio frequency power amplifier 22. In addition, the width of each band allocated for wide-band modulation may vary depending upon the transmission frequency band and the receive frequency band that an example communication device is assigned to use in the communication network. For example, the Long Term Evolution (LTE) standard may specify LTE band numbers, where each of the LTE band number corresponds to a specific transmit channel frequency band and a specific receive channel frequency band. As a non-limiting example, the LTE band number corresponds to a band of operation in which a communication device is assigned to operate in a mobile communication network. Thus, in some cases, the band of operation may

include a transmit channel and a receive channel. The transmit channel may have a transmit channel frequency band. The receive channel may have a receive channel frequency band. In addition, each band of operation may be assigned a specified duplex spacing, also referred to as a duplex offset, between the specific transmit channel frequency band and the specific receive channel frequency associated the band of operation. For example, the transmit channel and the receive channel for a band of operation may be spaced apart by a duplex offset. The transmit channel may have a transmit channel frequency band. The receive channel may have a receive channel frequency band. For example, each respective LTE band number may be assigned a specific duplex offset. As used herein, the term transmit to receive duplex offset is defined as a frequency having a magnitude substantially equal to the duplex offset between a transmit channel frequency band and a receive channel frequency band for a band of operation within a frequency spectrum. For example, an example band of operation assigned to a communication device may include a transmit channel and corresponding receive channel. The transmit channel may have a transmit channel frequency band between 1920 MHz and 1980 MHz. The corresponding receive channel may have a receive channel frequency band between 2110 MHz and 2170 MHz. As a result, the width of band for the transmit channel frequency band is 60MHz and the width of band for the receive channel frequency band is 60 MHz. The duplex offset between the transmit channel and the receive channel is 190MHz. As a result, the transmit to receive duplex offset is 190 MHz.

[00612] However, due to the non-ideal, (non-zero), output impedance of the parallel amplifier 35 and the large ripple currents associated with the power inductor currents, the modulated supply techniques implemented by the different embodiments of the pseudo-envelope follower power management system 10MA and the pseudo-envelope follower power management system 10MB, depicted in Figures 23A-D, may result in generation of ripple voltages in the power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28 supplied to the linear radio frequency power amplifier 22. Some of the generated ripple voltages may include high frequency ripple voltages that are located near a frequency

substantially equal to the transmit to receive duplex offset of a communication device. The high frequency ripple voltages may be spread out over a frequency band that is near the transmit to receive duplex offset associated for the band of operation of a communication device. For example, the high frequency ripple voltages may be within a frequency band centered about the frequency substantially equal to the transmit to receive duplex offset for the band of operation of the communication device. As a result, the high frequency ripple voltages that are within a band of frequencies substantially equal to at least the bandwidth of the receive channel frequency band, where the band of frequencies are is centered at the transmit to receive duplex offset associated with the band of operation of a communication device may be modulated into the radio frequency signal being generated for transmission by the linear radio frequency power amplifier 22.

[00613] To compensate for the ripple voltages in the power supply voltage, V_{CC}, the parallel amplifier will attempt to source or sink current to cancel out the ripple voltage on the power amplifier supply voltage, V_{CC}. However, because the parallel amplifier 35, depicted in Figures 23A-D, may exhibit a non-ideal output impedance in the operating frequency range of the linear radio frequency power amplifier 22. In addition, the non-ideal output impedance of the parallel amplifier 35 may also be non-linear. As a result, the parallel amplifier 35 may generate high frequency ripple voltages at the parallel amplifier output 32A. The generated high frequency ripple voltages generated by the parallel amplifier 35 may give rise to the generation of high frequency ripple voltages in the power amplifier supply voltage, V_{CC}, supplied to the linear radio frequency power amplifier 22. The frequencies of the high frequency ripple voltages may include frequencies that are near or within a band of frequencies substantially equal to at least the bandwidth of the receive channel frequency band that is centered at the transmit to receive duplex offset associated with the band of operation of a communication device. Thus, the high frequency ripple voltages may be near or in the operational bandwidth of the linear radio frequency power amplifier 22. Figures 23A-23D depict that the open loop ripple compensation assist circuit 414

is in communication with the power amplifier supply output 28 via the coupling circuit 18. As will be described below, embodiments of the open loop ripple compensation assist circuit 414, depicted in Figures 23A-23D, may be configured by the controller 50 to generate or provide a high frequency ripple compensation current 416, I_{COR}, at the parallel amplifier output 32A to reduce or cancel out the high frequency ripple currents at the power amplifier supply output 28 to minimize the high frequency ripple voltages generated by the parallel amplifier 35 in response to high frequency ripple currents at the power amplifier supply output 28, where the high frequency ripple currents are at frequencies that are near or within a band of frequencies centered near or at the transmit to receive duplex offset associated with the band of operation of a communication device and having a bandwidth substantially equal to at least the bandwidth of the receive channel frequency band for a mode operation. The high frequency ripple compensation current 416, I_{COR}, may be injected into the parallel amplifier output 32A to cancel out high frequency ripple currents at the power amplifier supply output 28 that are induced by the switching action of the switching voltage output 26. A ripple rejection response is a measure of the ability of the pseudo-envelope follower power management system to attenuate ripple voltages at the power amplifier supply output 28 that are due to the switching action at the switching voltage output 26. In other words, the ripple rejection response of the pseudo-envelope follower power management system is a measurement of the peak-to-peak ripple voltage on the power amplifier supply voltage, V_{CC}, with respect to the peak-to-peak switching voltage, V_{SW}. The high frequency ripple compensation current 416, I_{COR}, injected into the parallel amplifier output 32A cancels out high frequency ripple currents such that a ripple rejection response of the pseudo-envelope follower power management system includes a notch located in a frequency band within an operational bandwidth of a linear radio frequency power amplifier. For example, the notch of the ripple rejection response may be located at or near the transmit to receive duplex offset for a band of operation in which the linear radio frequency power amplifier is configured to be used. In addition, as will be described, some embodiments of

the open loop ripple compensation assist circuit 414, depicted in Figures 23A-23D, may be configured to generate the high frequency ripple compensation current 416, I_{COR}, independent of the non-ideal output impedance of the parallel amplifier 35.

[00614] Operationally, the open loop ripple compensation assist circuit 414 effectively develops an estimate of the high frequency current components in the power inductor current, I_{SW_OUT}, to be cancelled out. The open loop ripple compensation assist circuit 414 is in communication with the power amplifier supply output 28 via the coupling circuit 18. The high frequency ripple compensation current 416, I_{COR}, is injected into the parallel amplifier output 32A to substantially cancel out the high frequency current ripple currents in the power inductor current, I_{SW_OUT}, that correspond to a V_{RAMP} signal, where the high frequency current ripple currents are at frequencies that are near or within a band of frequencies centered near or at the transmit to receive duplex offset associated with the band of operation of a communication device, and where the band of frequencies has a bandwidth substantially equal to at least the bandwidth of the receive channel frequency band for a mode operation of the communication device. As a result, the high frequency ripple compensation current 416, I_{COR}, cancel out the high frequency ripple currents that would create noise on the transmit signal generated by the linear radio frequency power amplifier 22. To limit the frequency band of the portion of the power inductor current, I_{SW_OUT}, to be cancelled out by the injection of the high frequency ripple compensation current 416, I_{COR}, the open loop ripple compensation assist circuit 414 high pass filters an estimate of the power inductor current, I_{SW_OUT}, based on the transmit to receive duplex offset and the bandwidth of the receive channel frequency band for the band of operation the communication device is configured to used.

[00615] In contrast, as described above, Figure 10 depicts an embodiment of the parallel amplifier output impedance compensation circuit 37A that uses an estimated inductance of the parallel amplifier 35 at the frequencies near or within operational bandwidth of the linear radio frequency power amplifier 22 to

generate a compensated V_{RAMP} signal, V_{RAMP_C}. For example, the parallel amplifier output impedance compensation circuit 37A may use a programmable value of the parallel amplifier inductance estimate parameter, L_{CORR_EST}, as the estimated inductance of the parallel amplifier 35 at the frequencies near or within operational bandwidth of the linear radio frequency power amplifier 22. Accordingly, as described above with respect to the operation of the parallel amplifier output impedance compensation circuit 37A, the compensated V_{RAMP} signal, V_{RAMP_C}, is used by the parallel amplifier 35 instead of the V_{RAMP} signal in order to reduce the high frequency ripple voltages present in the parallel amplifier output voltage, V_{PARA_AMP}, generated by the parallel amplifier 35 in the parallel amplifier output 32A due to the non-ideal output impedance characteristics of the parallel amplifier. Thus, the effectiveness of the cancellation or reduction of the high frequency ripple voltages generated by the parallel amplifier 35 by the parallel amplifier output impedance compensation circuit 37A may be dependent on the frequency dependent output impedance characteristics of the parallel amplifier 35 measure at the time of calibration of the communication device.

[00616] Figure 23A depicts an embodiment of a pseudo-envelope follower power management system 10MA that that is similar to the pseudo-envelope follower power management system 10B, depicted in Figure 2B. However, unlike the pseudo-envelope follower power management system 10B, depicted in Figure 2B, the pseudo-envelope follower power management system 10MA, depicted in Figure 23A includes an embodiment of a multi-level charge pump buck converter 12M instead of multi-level charge pump buck converter 12B. Also, unlike the pseudo-envelope follower power management system 10B, depicted in Figure 2B, the pseudo-envelope follower power management system 10MA, depicted in Figure 23A includes an embodiment of a parallel amplifier circuit 14MA.

[00617] However, similar to the embodiment of the parallel amplifier circuit 14B, depicted in Figure 2B, the embodiment of the parallel amplifier circuit 14MA, depicted in Figure 23A, includes parallel amplifier circuitry 32 and a V_{OFFSET} loop circuit 41. The embodiment of the parallel amplifier circuitry 32,

depicted in Figure 23A, may include an embodiment of the parallel amplifier 35 and an embodiment of the parallel amplifier sense circuit 36, similar to the parallel amplifier 35 and the parallel amplifier sense circuit 36 depicted in Figure 2B. In addition, some embodiments of the parallel amplifier 35, depicted in Figure 23A, may be similar to one of the embodiments of the parallel amplifier 35. Example embodiments of the parallel amplifier 35 may include the parallel amplifier 35A, the rechargeable parallel amplifier 35B, the rechargeable parallel amplifier 35C, the parallel amplifier 35D, the rechargeable parallel amplifier 35E, and the rechargeable parallel amplifier 35F, as depicted in the respective Figures 12A-F.

[00618] Accordingly, although not depicted in Figure 23A for the sake of convenience, and not by way of limitation, some embodiments of the parallel amplifier circuit 14MA may be advantageously similar to the parallel amplifier circuit 14C, depicted in Figure 18A, and the parallel amplifier circuit 14D, depicted in Figure 18B, where a parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, is provided to provide a supply voltage to the parallel amplifier, parallel amplifier sense circuit 36, some portions of the parallel amplifier circuitry 32, and/or a combination thereof.

[00619] Thus, although not depicted in Figure 23A for the sake of simplicity and not by way of limitation, similar to the embodiments of the pseudo-envelope follower power management system 10C, depicted in Figure 18A, and the pseudo-envelope follower power management system 10E, depicted in Figure 18B, some embodiments of the pseudo-envelope follower power management system 10MA may be configured to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$. For example, some embodiments of the pseudo-envelope follower power management system 10MA may further include an embodiment of the µC charge pump circuit 262, depicted in Figures 18A-D, the µC charge pump circuit 262A, depicted in Figure 19A, or the µC charge pump circuit 262B, depicted in Figure 19B. Furthermore, although not depicted in Figure 23A for the sake of simplicity, and not by way of limitation, some embodiments of the multi-level charge pump buck converter 12M may replace

the multi-level charge pump circuit 56 with an embodiment of the multi-level charge pump circuit 258 of the multi-level charge pump buck converter 12C, depicted in Figure 18A and Figure 18B. In those embodiments of the multi-level charge pump buck converter 12M that are adapted to include an embodiment of the multi-level charge pump circuit 258, the multi-level charge pump buck converter 12M may be similar to either the example embodiment of the multi-level charge pump circuit 258A, depicted in Figure 7B, or the example embodiment of the multi-level charge pump circuit 258B, depicted in Figure 7C. Accordingly, the alternative embodiments of the multi-level charge pump buck converter 12M that include an embodiment of the multi-level charge pump circuit 258, (not depicted in Figure 23A), may generate an internal charge pump node parallel amplifier supply 294 (Figures 18A-B) to provide the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, to an embodiment of the parallel amplifier 35 similar to the parallel amplifier 35D, the rechargeable parallel amplifier 35E, or the rechargeable parallel amplifier 35F, respectively depicted in Figures 12D-F.

[00620] In the embodiments of the pseudo-envelope follower power management system 10MA, depicted in Figure 23A, the parallel amplifier circuit 14MA may include an embodiment of the V_{OFFSET} loop circuit 41 similar to the V_{OFFSET} loop circuit 41A, depicted in Figure 18A, the V_{OFFSET} loop circuit 41B, depicted in Figure 18B, or the V_{OFFSET} loop circuit 41, depicted in Figure 8. Accordingly, the parallel amplifier circuit 14MA may be configured to provide the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the switcher control circuit 52 of the multi-level charge pump buck converter 12M. Accordingly, similar to the embodiment of the multi-level charge pump buck converter 12B, depicted in Figure 2B, the multi-level charge pump buck converter 12M may use the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to adjust the switching operation of the multi-level charge pump buck converter 12M.

[00621] Continuing with the description of Figure 23A, as discussed above, the parallel amplifier circuit 14MA may further include an embodiment of the open loop ripple compensation assist circuit 414. The open loop ripple compensation

assist circuit 414 may be configured by the controller 50 via the control bus 44. The open loop ripple compensation assist circuit 414 may include or be associated with programmable filter parameter(s), programmable gain parameter(s), and programmable delay parameter(s). In some embodiments, some of the programmable filter parameter(s), the programmable gain parameter(s), and the programmable delay parameter(s) are determined at calibration. However, in some embodiments of the open loop ripple compensation assist circuit 414, at least some of the programmable filter parameter(s), the programmable gain parameter(s), and the programmable delay parameter(s) may be optimized by the controller 50 based on the operational mode of the pseudo-envelope follower power management system 10MA.

[00622] The open loop ripple compensation assist circuit 414 may be configured to inject the high frequency ripple compensation current 416, I_{COR}, at or into the parallel amplifier output 32A to provide the high frequency ripple compensation current 416, I_{COR}, to the power amplifier supply output 28. As will be discussed in further detail below, the open loop ripple compensation assist circuit 414 generates the high frequency ripple compensation current 416, I_{COR}, to minimize the high frequency ripple voltages on the power amplifier supply voltage, V_{CC}, supplied to the linear radio frequency power amplifier 22.

[00623] In some embodiments, the open loop ripple compensation assist circuit 414 may use the V_{RAMP} signal and an estimate of the switching voltage, V_{SW}, provided at the switching voltage output 26 of the multi-level charge pump buck converter 12M, to determine or generate an estimate of the ripple currents present at the power amplifier supply output 28. The open loop ripple compensation assist circuit 414 may be configured to high pass filter the estimate of the ripple currents present at the power amplifier supply output 28 to obtain an estimate of the high-frequency ripple currents located near or within a band of frequencies centered near or at the transmit to receive duplex offset associated with the band of operation in which the linear radio frequency power amplifier 22 is being used, where the band of frequencies has a bandwidth substantially equal to at least the bandwidth of the receive channel frequency band for a band of

operation at the power amplifier supply output 28. For example, some embodiments of the open loop ripple compensation assist circuit 414 may include programmable filters or filtering circuits, where the filter characteristics of the programmable filters may be adjusted based on the programmable filter parameter(s). For example, the programmable filters may provide a first high pass filter response and a second high pass filter response, where the first high pass filter response is associated with a first corner frequency, f_{C1}, and the second high pass filter response is associated with a second corner frequency, f_{C2}. The controller 50 may be configured to adjust the programmable filter parameter(s) associated with each of the first high pass filter response and a second high pass filter response. In addition, the magnitude of the high frequency ripple compensation current 416, I_{COR}, may be adjusted based on the programmable gain parameter(s). In some embodiments, the programmable gain parameter(s) may be parameters used to set a programmable transconductance related parameter.

[00624] Based on the estimate of the high-frequency ripple currents that include frequencies near or within a band of frequencies centered near or at the transmit to receive duplex offset associated with the band of operation in which the linear radio frequency power amplifier 22 is being used, where the band of frequencies has a bandwidth substantially equal to at least the bandwidth of the receive channel frequency band for the band of operation, the open loop ripple compensation assist circuit 414 may generate the high frequency ripple compensation current 416, I_{COR}. In addition, as will be discussed, the open loop ripple compensation assist circuit 414 may adjust the magnitude of the high frequency ripple compensation current 416, I_{COR}, and time align the generation of the high frequency ripple compensation current 416, I_{COR}, such that the high frequency ripple compensation current 416, I_{COR}, maximally cancels out the high-frequency ripple currents, present at the power amplifier supply output 28, that are near or within operational bandwidth of the linear radio frequency power amplifier 22. In other words, the controller 50 may configure the open loop ripple compensation assist circuit 414 to inject the high frequency ripple compensation

current 416, I_{COR}, at the parallel amplifier output 32A to create a notch in the ripple rejection response, measured at the power amplifier supply output 28, that is located near a transmit to receive duplex offset for a band of operation in which the linear radio frequency power amplifier is configured to be used. As an example, the controller 50 may adjust the programmable delay parameter(s) to move the location of the notch in the ripple rejection response a function of the transmit to receive duplex offset for the band of operation for which the linear radio frequency power amplifier 22 is configured to be used. For example, the controller 50 may be configured to adjust the programmable delay parameter(s) to temporally align the injection of the high frequency ripple compensation current 416, I_{COR}, at parallel amplifier output 32A to create a notch in a ripple rejection response of the power amplifier supply output that is located near a transmit to receive duplex offset for a band of operation in which the linear radio frequency power amplifier is configured to be used.

[00625] In addition, in some embodiments, the controller 50 may be configured to adjust the programmable filter parameter(s) to adjust the width, depth, shape, and/or a combination thereof such that the high frequency ripple compensation current 416 maximally cancels out the high-frequency ripple currents generated by the parallel amplifier 35 in frequencies near or within the operational bandwidth of the linear radio frequency power amplifier 22.

[00626] In addition, the open loop ripple compensation assist circuit 414 may be further configured to generate a scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}. The scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, may be a fractional representation of the high frequency ripple compensation current 416, I_{COR}, provided to the output of the parallel amplifier output 32A. For example, the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, may be linearly related to the high frequency ripple compensation current 416, I_{COR}, by the sense scaling factor, $C_{SENSE_SCALING}$. As depicted in Figure 23A, the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, may be combined with the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, generated by

the parallel amplifier sense circuit 36 to form the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. The parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, including the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, may be provided to the multi-level charge pump buck converter 12M. Accordingly, similar to the embodiment of the multi-level charge pump buck converter 12B, depicted in Figure 2B, the multi-level charge pump buck converter 12M may use the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to adjust the switching operation of the multi-level charge pump buck converter 12M.

[00627] For the sake of simplicity of description, and not by way of limitation, Figure 23A depicts the embodiment of the parallel amplifier circuit 14MA, as not including an open loop assist circuit 39, which is included as part of the parallel amplifier circuit 14B depicted in Figure 2B. Also, unlike the multi-level charge pump buck converter 12B depicted in Figure 2B, for the sake of simplicity of description, and not by way of limitation, the embodiment of the multi-level charge pump buck converter 12M depicted in Figure 23A does not depict the multi-level charge pump buck converter 12M providing an estimated switching voltage output 38B, V_{SW_EST}, as an output to the parallel amplifier circuit 14MA.

[00628] However, Figure 23C depicts an example embodiment of the pseudo-envelope follower power management system 10MA that includes a multi-level charge pump buck converter 12M and an embodiment of a parallel amplifier circuit 14MB that includes an open loop ripple compensation assist circuit 414 in combination with an open loop assist circuit 39, where the open loop assist circuit 39 may be similar to the embodiment of the open loop assist circuit 39 depicted in Figure 2B. Accordingly, as depicted in Figure 23C, embodiments of the pseudo-envelope follower power management system 10MA that include the parallel amplifier circuit 14MB, may provide a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to adjust the switching operation of the multi-level charge pump buck converter 12M, where the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is generated by combining the scaled parallel

amplifier output current estimate, $I_{PARA_AMP_SENSE}$, the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}.

[00629] As further depicted in Figure 23A, the multi-level charge pump buck converter 12M is further configured to provide a delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, to a programmable delayed switching voltage input (not shown) of the parallel amplifier circuit 14MA. The programmably delayed switching voltage input is in communication with the open loop ripple compensation assist circuit 414 of the parallel amplifier circuit 14MA and configured to receive the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$. Similar to the estimated switching voltage output 38B, V_{SW_EST}, generated by the multi-level charge pump buck converter 12B, depicted in Figure 2B, the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, is a feed forward signal generated based on the state of the switcher control circuit 52, where the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, provides an early indication of what the switching voltage, V_{SW}, will become based on the operational state of the switcher control circuit 52. Thus, the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, may be a feed forward signal that indicates a future voltage level of the switching voltage, V_{SW}, at the switching voltage output 26 based on the operational state of the switcher control circuit 52 before the switching voltage output 26 is configured to provide a switching voltage, V_{SW}, at the switching voltage output 26 substantially equal to the future voltage level of the switching voltage, V_{SW}. In other words, delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, provides a switching output voltage estimate that that may be programmably delayed by the programmable delay circuitry 432. In this way, the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, may be considered a version of the estimated switching voltage output 38B, V_{SW_EST}, that may be programmably delayed by the programmable delay circuitry 432 to time align generation of the high frequency ripple compensation current 416, I_{COR}. For example, the

programmable delay circuitry 432 may be configured to have a programmable delay period such that the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, is delayed in time by substantially the programmable delay period relative to the estimated switching voltage output 38B, V_{SW_EST}. The controller 50 may programmatically configure programmable delay circuitry in the multi-level charge pump buck converter 12M to provide a programmable delay period between generation of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, relative to generation of the estimated switching voltage output 38B, V_{SW_EST}. The controller 50 may adjust the programmable delay period to align the generation of the high frequency ripple compensation current 416, I_{COR}, to cancel out the high frequency ripple currents generated by the parallel amplifier 35 in response to the V_{RAMP} signal. Illustratively, the controller 50 may be configured to adjust the programmable delay period to temporally align the injection of the high frequency ripple compensation current 416, I_{COR}, at parallel amplifier output 32A, to create a notch in a ripple rejection response of the power amplifier supply output that is located near a transmit to receive duplex offset for a band of operation in which the linear radio frequency power amplifier is configured to be used.

[00630] As will be discussed below, the controller 50 may be further configured to programmatically change the values of the programmable filter parameter(s), programmable gain parameter(s), and programmable delay parameter(s) to obtain an optimized overall system response of the pseudo-envelope follower power management system 10MA to place a notch in the ripple rejection response at the power amplifier supply output 28 as a function of the duplex offset for each band of operation. Thus, depending on the band of operation in which the linear radio frequency power amplifier 22 is configured to be used, the controller 50 may configure the notch in the ripple rejection response to be located near or at the transmit to receive duplex offset associated with the selected band of operation. In addition, the bandwidth of the receiver channel frequency band for the band of operation is used to configure the ripple rejection response to substantially cancel output the high frequency ripple currents that

could be modulated onto the transmit signal generated by the linear radio frequency power amplifier. For example, Figure 25 depicts the notch response of example pseudo-envelope follower power management system 10MA and 10MB, as depicted in Figures 23A-D, as a function of the programmable delay period.

[00631] As previously discussed, Figure 23B depicts an embodiment of a pseudo-envelope follower power management system 10MB that includes a buck converter 13L and an embodiment of the parallel amplifier circuit 14MA. As discussed above, the buck converter 13L interfaces with the parallel amplifier circuit 14MA. The operation of the parallel amplifier circuit 14MA in conjunction with the buck converter 13L is substantially similar to the operation of the embodiments of the parallel amplifier circuit 14MA with the multi-level charge pump buck converter 12M. Likewise, the pseudo-envelope follower power management system 10MB may include the features and functions of the various embodiments and alternative embodiments of the pseudo-envelope follower power management system 10MA, as described above, except, similar to the pseudo-envelope follower power management system 10D, depicted in Figure 18C, and the pseudo-envelope follower power management system 10F, depicted in Figure 18D, the buck converter 13L may not generate an internal charge pump node parallel amplifier supply 294 because the buck converter 13L does not include an embodiment of the multi-level charge pump circuit 56 that is included in the multi-level charge pump buck converter 12M of the pseudo-envelope follower power management system 10MA, depicted in Figure 23A. Even so, although not depicted in Figure 23B, some alternative embodiments of the pseudo-envelope follower power management system 10MB may include an embodiment of the μC charge pump circuit 262 and associated circuitry similar to the pseudo-envelope follower power management system 10D, depicted in Figure 18C, and the pseudo-envelope follower power management system 10F, depicted in Figure 18D, in order to provide a parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, to an embodiment of the parallel amplifier 35 similar to the

parallel amplifier 35D, the rechargeable parallel amplifier 35E, or the rechargeable parallel amplifier 35F, respectively depicted in Figures 12D-F.

[00632] Figure 23C depicts an alternative embodiment of the pseudo-envelope follower power management system 10MA that is similar in form and function to the embodiments of the pseudo-envelope follower power management system 10MA discussed with reference to Figure 23A. However, unlike the alternative embodiment of the pseudo-envelope follower power management system 10MA depicted in Figure 23A, the pseudo-envelope follower power management system 10MA depicted in Figure 23C includes the parallel amplifier circuit 14MB instead of the parallel amplifier circuit 14MA. As previously discussed, the parallel amplifier circuit 14MB is similar in form and function to the parallel amplifier circuit 14MA, described previously, except that the parallel amplifier circuit 14MB include an embodiment of the open loop assist circuit 39. Accordingly, the alternative embodiment of the pseudo-envelope follower power management system 10MA depicted in Figure 23C is functionally similar to the embodiment of the pseudo-envelope follower power management system 10MA depicted in Figure 23A except the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, further includes the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}, and the open loop assist circuit 39 provides the open loop assist circuit current, I_{ASSIST}, at the parallel amplifier output 32A.

[00633] Figure 23D depicts an alternative embodiment of the pseudo-envelope follower power management system 10MB that is substantially similar in form and function to the embodiment of the pseudo-envelope follower power management system 10MB depicted in Figure 23B except the alternative embodiment of the pseudo-envelope follower power management system 10MB depicted in Figure 23D includes the parallel amplifier circuit 14MB instead of the parallel amplifier circuit 14MA. Accordingly, the alternative embodiment of the pseudo-envelope follower power management system 10MB depicted in Figure 23D is functionally similar to the pseudo-envelope follower power management system 10MB, depicted in Figure 23B, except the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, further includes the scaled open

loop assist circuit output current estimate, I_{ASSIST_SENSE}, and the open loop assist circuit 39 provides the open loop assist circuit current, I_{ASSIST}, at the parallel amplifier output 32A.

[00634] Figure 24 depicts an embodiment of the open loop ripple compensation assist circuit 414A and a portion of a switch mode power supply converter 420. The switch mode power supply converter 420 may be similar in form and function to the embodiment of the multi-level charge pump buck converter 12M, depicted in Figure 23A and Figure 23C, or the buck converter 13L, depicted in Figure 23B and Figure 23D. The switcher control circuit (not shown) of the switch mode power supply converter 420 may be configured as one of the embodiments of the switcher control circuit 52 when the switch mode power supply converter 420 is configured as one of the embodiments of a multi-level charge pump buck converter as described herein. Alternatively, the switcher control circuit (not shown) of the switch mode power supply converter 420 may be configured as one of the embodiments of the switcher control circuit 52 when the switch mode power supply converter 420 is configured as one of the embodiments of a buck converter as described herein. Accordingly, similar to the previously described embodiments of the multi-level charge pump buck converter 12M and the buck converter 13L, the switch mode power supply converter 420 may be configured to provide a delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, to the open loop ripple compensation assist circuit 414A. Although not depicted in Figure 24, it will be understood that controller 50, depicted in Figures 23A-D, may be configured to control or configure the elements of the open loop ripple compensation assist circuit 414A.

[00635] The open loop ripple compensation assist circuit 414A may include an embodiment of a combined filter and gain assist circuitry 422A. The combined filter and gain assist circuitry 422A may include a ripple cancellation circuit 424 and a Gm assist circuit 426. The Gm assist circuit 426 may include an input port 426A, a Gm assist I_{COR} output 426B, and a Gm assist I_{COR_SENSE}

output 426C. The controller 50 may be configured to adjust the transconductance of the Gm assist circuit 426.

[00636] The combined filter and gain assist circuitry 422A may include an integrator circuit 428 and high pass filter circuitry 430. The high pass filter circuitry 430 may include a high pass filter circuitry input 430A and a high pass filter circuitry output 430B. The controller 50 may configure the high pass filter circuitry 430 to provide a desired high pass frequency response by adjusting the time constants associated with the high pass filter circuitry 430. The integrator circuit 428 may include a non-inverting input 428A configured to receive the V_{RAMP} signal and an inverting input 428B configured to receive the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$. Although not depicted in Figure 24, in some embodiments of the open loop ripple compensation assist circuit 414A, the V_{RAMP} signal may be scaled by a scaling factor, K_{VRAMP_SCALE}, such that the non-inverting input 428A of the integrator circuit 428 receives a scaled V_{RAMP} signal, V_{RAMP_SCALED}, where $V_{RAMP_SCALED} = K_{VRAMP_SCALE} \times V_{RAMP}$. The integrator output 428C is coupled to the high pass filter circuitry input 430A of the high pass filter circuitry 430. The high pass filter circuitry output 430B of the high pass filter circuitry 430 is coupled to the input port 426A of the Gm assist circuit 426. Based on the integrated and high pass filtered signal generated by the ripple cancellation circuit 424, the Gm assist circuit 426 generates the high frequency ripple compensation current 416, I_{COR}, at the Gm assist I_{COR} output 426B and the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, at the Gm assist I_{COR_SENSE} output 426C.

[00637] In order to place a notch in the ripple rejection response of the power amplifier supply output 28 as a function of the transmit to receive duplex offset for each band of operation, the open loop ripple compensation assist circuit 414A may be configured to generate a predicted estimated inductor current, $I_{SW_OUT_EST}$, for the power inductor current, I_{SW_OUT}, that is provided by the power inductor 16, as depicted in Figure 23A, based on a difference between the V_{RAMP} signal and the delayed I_{COR} estimated switching voltage output 38C,

$V_{SW_EST_DELAY_ICOR}$, and the inductance value of the power inductor 16, depicted in Figures 23A-D. The predicted estimated inductor current, $I_{SW_OUT_EST}$, is an estimate of the power inductor current, I_{SW_OUT}, in the power inductor 16 corresponding temporally to when the switching voltage, V_{SW}, to be generated at the switching voltage output 26 which is represented by the value of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, and the V_{RAMP} signal reflects the voltage level of the power amplifier supply voltage, V_{CC}. However, in order to simplify circuitry, and because the high frequency ripple compensation current 416, I_{COR}, is injected at or into the parallel amplifier output 32A to cancel out the high frequency ripple components of the power inductor current, I_{SW_OUT}, near or within a band of frequencies substantially equal to at least the bandwidth of the receive channel frequency band that is centered at the transmit to receive duplex offset associated with the band of operation in which the of the linear radio frequency power amplifier 22 is being used, the ripple cancellation circuit generates the negative of the predicted estimated inductor current, $I_{SW_OUT_EST}$. As an example, the integrator circuit 428 may be configured to integrate the difference between the V_{RAMP} signal and the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, to generate the negative of the predicted estimated inductor current, $I_{SW_OUT_EST}$. The negative of the predicted estimated inductor current, $I_{SW_OUT_EST}$, may be represented by the Laplace transfer function of the integrator circuit 428, shown in equation (4) as follows:

$$-I_{SW_OUT_EST}(s) = \frac{(V_{RAMP} - V_{SW_OUT_EST})}{L_{POWER_INDUCTOR}s} \quad (4)$$

where $L_{POWER_INDUCTOR}$ represents the inductance of the power inductor 16 depicted in Figures 23A-D.

[00638] Thus, referring to Figures 23A-D, the predicted estimated inductor current, $I_{SW_OUT_EST}$, provides an estimate of the current through the power inductor 16 corresponding to the time when the delayed I_{COR} estimated switching

voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, reflects the voltage level of the switching voltage, V_{SW}, provided at the switching voltage output 26 and the V_{RAMP} signal reflects the voltage level of the power amplifier supply voltage, V_{CC}. The negative of the predicted estimated inductor current, $I_{SW_OUT_EST}$, is provided to the high pass filter circuitry 430, which high pass filters the negative of the predicted estimated inductor current, $I_{SW_OUT_EST}$, to generate an estimate of the predicted high frequency ripple currents, $I_{HIGH_FREQUENCY_RIPPLE}$, to be cancelled out, at the power amplifier supply output 28 when the switching voltage, V_{SW}, to be generated at the switching voltage output 26 is represented by the value of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, and the V_{RAMP} signal represents the power amplifier supply voltage, V_{CC}. The pass band characteristics of the high pass filter circuitry 430 may be adjusted by the controller 50 based on the programmable filter parameter(s) such that the frequency content of the predicted high frequency ripple currents $I_{HIGH_FREQUENCY_RIPPLE}$, to be cancelled out, at the power amplifier supply output 28, includes frequencies that are near or within a band of frequencies substantially equal to at least the bandwidth of the receive channel frequency band that is centered at the transmit to receive duplex offset associated with the band of operation for which the linear radio frequency power amplifier 22 is being used.

[00639] As an example, the high pass filter circuitry 430 may provide a first high pass filter response and a second high pass filter response, where the first high pass filter response corresponds to a first corner frequency, f_{C1}, and the second high pass filter response corresponds to a second corner frequency, f_{C2}. In some embodiments, the first corner frequency, f_{C1}, and the second corner frequency, f_{C2}, may be configured by the controller 50 (not shown). The first corner frequency, f_{C1}, and the second corner frequency, f_{C2}, may be adjusted based on the bandwidth of the receive channel frequency band associated with each band of operation of the linear radio frequency power amplifier 22.

[00640] The high pass filter circuitry 430 provides the predicted high frequency ripple currents to be cancelled out, $I_{HIGH_FREQUENCY_RIPPLE}$, to the Gm assist

circuit 426. The Gm assist circuit 426 gain scales the predicted high frequency ripple currents to be cancelled out, $I_{HIGH_FREQUENCY_RIPPLE}$, to generate the high frequency ripple compensation current 416, I_{COR}, based on the predicted high frequency ripple currents, $I_{HIGH_FREQUENCY_RIPPLE}$, to be cancelled out, and the programmable gain parameter(s) provided by the controller 50. In addition, the Gm assist circuit 426 also generates the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, which is a fractional representation of the high frequency ripple compensation current 416, I_{COR}, used to generate the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. Because the predicted estimated inductor current, $I_{SW_OUT_EST}$, is high pass filtered, the predicted high frequency ripple currents, $I_{HIGH_FREQUENCY_RIPPLE}$, to be cancelled out, do not reflect the low-frequency modulation of the power amplifier supply output 28. As a result, the high frequency ripple compensation current 416, I_{COR}, does not conflict with the efforts of the parallel amplifier 35 to compensate for the low-frequency modulation of the power amplifier supply voltage, V_{CC}, due to the change in the switching voltage, V_{SW}, at the switching voltage output 26, depicted in Figures 23A-D.

[00641] As further depicted in Figure 24, the switch mode power supply converter 420 includes programmable delay circuitry 432 and a buffer scalar 434. For the sake of simplicity, and not by way of limitation, the generation of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, by the switch mode power supply converter 420 will now be discussed with reference to the embodiment of the threshold detector and control circuit 132A, depicted in Figure 4A. As depicted in Figure 4A, the threshold detector and control circuit 132A may generate one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s). The one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), indicate the state of the switcher control circuit (not shown) of the switch mode power supply converter 420 before the switch mode power supply converter 420 transitions to provide the switching voltage, V_{SW}, at the switching voltage output represented by the switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s). For example, in the

case where the switch mode power supply converter 420 is similar to the embodiment of the multi-level charge pump buck converter 12B, depicted in Figure 2B, the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, may be used by the third output buffer 161 to generate one of the various embodiments of the estimated switching voltage output 38B, V_{SW_EST}, depicted in Figures 11A-11F. As depicted in Figure 11A, in the simplest form, the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, may be a single digital signal that represents the future state of the switching voltage output 26 as being in either the shunt level or providing a voltage greater than ground to the power inductor 16, as depicted in Figure 2B. Similarly, in the case where the switch mode power supply converter 420 is similar to the buck converter 13L depicted in Figure 23B, the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, may be a single digital signal that represents the future state of the switching voltage output 26 as being in either the shunt level or the series level.

[00642] Returning to Figure 24, the programmable delay circuitry 432 is configured to receive the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$. The controller 50 may use the programmable delay parameter(s) to delay the propagation of the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, through the programmable delay circuitry 432 by a programmable delay period to generate the one or more programmably delayed switching voltage output cmos signal(s) 166A, $V_{SW_EST_CMOS_DELAYED_SIGNAL}(s)$. The one or more programmably delayed switching voltage output cmos signal(s) 166A, $V_{SW_EST_CMOS_DELAYED_SIGNAL}(s)$ are provided to the buffer scalar 434. The controller 50 (not shown) may provide a scaling factor, M, based on a scaling factor parameter stored in association with the controller 50, the parallel amplifier circuit, or the switch mode power supply converter 420. Accordingly, based on the scaling factor parameter, the controller 50 may set the value of the scaling factor, M, received by the buffer scalar 434. Similar to the third output buffer 161, depicted in Figure 4A, the buffer scalar 434 generates the delayed I_{COR} estimated

switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, based on the one or more programmably delayed switching voltage output cmos signal(s) 166A, $V_{SW_EST_CMOS_DELAYED_SIGNAL}$(s), and the scaling factor, M, provided by the controller 50. The controller 50 (not shown) may adjust the value of the scaling factor, M, to account for variations in the magnitude of the V_{RAMP} signal and to ensure proper performance of the ripple cancellation circuit 424. In other embodiments, the controller 50 (not shown) may adjust the scaling factor, M, to compensate for changes in the battery voltage, V_{BAT}, from the battery 20. Example embodiments of the programmable delay circuitry 432 are depicted in Figures 29A-B and Figures 30A-C.

[00643] To time align the generation of the high frequency ripple compensation current 416, I_{COR}, the controller 50 programmatically adjusts the delay provided by the programmable delay circuitry 432 based on the programmable delay parameter(s). The controller 50 may configure the delay time through the programmable delay circuitry 432 to move the placement of the notch in the ripple rejection response of the pseudo-envelope follower power management system 10MA. As an example, the controller 50 may adjust the delay to place the notch in the ripple rejection response of the pseudo-envelope follower power management system 10MA as function of the transmit to receive duplex offset for each band of operation in which the linear radio frequency power amplifier 22 is configured to be used. Accordingly, as discussed above, the controller 50 may be configured to programmatically change the values of the programmable filter parameter(s), programmable gain parameter(s), and programmable delay parameter(s) to obtain an optimized notch depth, a notch width, and a notch frequency of the notch in the ripple rejection response of the embodiments of the pseudo-envelope follower power management system 10MA, depicted in Figure 23A and Figure 23C, and the pseudo-envelope follower power management system 10MB, depicted in Figure 23B and Figure 23D, as a function of the transmit to receive duplex offset for each band of operation for which the linear radio frequency power amplifier 22 is configured to be used.

[00644] Figure 25 depicts three example ripple rejection responses of an embodiment of the pseudo-envelope follower power management system similar to the pseudo-envelope follower power management system 10MA and the pseudo-envelope follower power management system 10MB, depicted in Figures 23A-D, where the desired maximum ripple rejection response is near 30 MHz.

[00645] The first ripple rejection response depicted in Figure 25 may be obtained by the controller 50 configuring the programmable delay circuitry 432 to provide a first programmable delay period substantially equal to $DELAY_1$ in order to temporally align the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, to provide a maximum ripple rejection response near 30 MHz. The second ripple rejection response depicted in Figure 25 may be obtained by the controller 50 configuring the programmable delay circuitry 432 to provide a second programmable delay period substantially equal to $DELAY_2$, where $DELAY_2 > DELAY_1$. This results in the second ripple rejection response having a maximum ripple rejection response at a frequency less than the desired 30 MHz and the depth of the notch in the ripple rejection response is reduced. The third ripple rejection response depicted in Figure 25 may be obtained by the controller 50 configuring the programmable delay circuitry 432 to provide a third programmable delay period substantially equal to $DELAY_3$, where $DELAY_1 > DELAY_3$. This results in the third ripple rejection response having a maximum ripple rejection response at a frequency greater than the desired 30MHz and locates the notch in the ripple rejection response at a frequency that is higher than the desired 30 MHZ. As depicted in Figure 25, the controller 50 may configure the programmable delay provided by the programmable delay circuitry 432 to locate the notch in the ripple rejection response of the pseudo-envelope follower power management systems 10MA and 10MB at or near the receive duplex offset for each band of operation for which the linear radio frequency power amplifier 22 is configured to be used.

[00646] Figure 26 depicts an embodiment of the high pass filter circuitry 430 that may include a first high pass filter circuit 435A and a second high pass filter

circuit 435B. The first high pass filter circuit 435A may have a first corner frequency, f_{C1}, which is determined by the first high pass filter time constant, τ_{C1}. The second high pass filter circuit 435B may have a second corner frequency, f_{C2}, which is determined by the second high pass filter time constant, τ_{C2}. Accordingly, the combined transfer function of the first high pass filter circuit 435A and the second high pass filter circuit 435B may provide a first high pass filter response and a second high pass filter response, where the first high pass filter response corresponds to a first corner frequency, f_{C1}, and the second high pass filter response corresponds to a second corner frequency, f_{C2}. The combined transfer function of the first high pass filter circuit 435A and the second high pass filter circuit 435B, $H_{HP}(s)$, may be represented by the Laplace transfer function shown in equation (5) as follows:

$$H_{HP}(s) = \left[\frac{\tau_{C1}s}{1+\tau_{C1}s}\right]\left[\frac{\tau_{C2}s}{1+\tau_{C2}s}\right]. \quad (5)$$

[00647] The first high pass filter time constant, τ_{C1} and the second high pass filter time constant, τ_{C2}, may be independently set such that the first corner frequency, f_{C1}, does not equal the second corner frequency, f_{C2}. For example, the first high pass filter time constant, τ_{C1}, may be configured by the controller 50 (not shown) such that the first corner frequency, f_{C1}, has a range between 3M Hz and 11.5 MHz. In some embodiments, the first corner frequency, f_{C1}, may have a range between 3 MHz and 8 MHz. Similarly, the controller may configure the second high pass filter time constant, τ_{C2}, such that the second corner frequency, f_{C2}, has a range between 3 MHz and 11.5 MHz. In some embodiments, the second corner frequency, f_{C2}, may have a range between 3 MHz and 8 MHz.

[00648] In some embodiments of the high pass filter circuitry 430, the first corner frequency, f_{C1}, of the first high pass filter circuit 435A and the second corner frequency, f_{C2}, of the second high pass filter circuit 435B are each set to be approximately 6 MHz. In some embodiments, the controller 50 (not shown) may configure the first high pass filter time constant, τ_{C1}, and the second high pass filter time constant, τ_{C2}. For example, the first high pass filter time constant,

τ_{C1}, may be configured by the controller 50 (not shown) such that the first corner frequency, f_{C1}, has a range between 3 MHz and 11.5 MHz. In some embodiments, the first corner frequency, f_{C1}, may have a range between 3 MHz and 11.5 MHz. In still other embodiments the first corner frequency, f_{C1}, and the second corner frequency, f_{C2}, may be configured to be substantially the same. For example, the first corner frequency, f_{C1}, may be configured to be around 6 MHz, and the second corner frequency, f_{C2}, may be configured to be around 6 MHz. In some embodiments, the first corner frequency, f_{C1}, and the second corner frequency, f_{C2}, are configured by the controller 50 as a function of the bandwidth of the receive channel frequency band associated with each band of operation.

[00649] Returning to Figure 24, assuming that the high pass filter circuitry 430 includes both the first high pass filter circuit 435A and the second high pass filter circuit 435B, the desired Laplace transfer function for the high frequency ripple compensation current 416, I_{COR}, provided at the Gm assist I_{COR} output 426B of the Gm assist circuit 426 is shown in equation (6) as follows:

(6) $$I_{COR}(s) = \frac{(V_{RAMP} - V_{SW_OUT_EST})}{L_{POWER_INDUCTOR} s} \frac{\tau_{C1} s}{1+\tau_{C1} s} \frac{\tau_{C2} s}{1+\tau_{C2} s}$$

[00650] where V_{RAMP} represents the future value of the power amplifier supply voltage, V_{CC}, the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, represents the future value of the switching voltage, V_{SW}, at the switching voltage output 26 based on the operational state of the switcher control circuit (not shown) of the switch mode power supply converter 420, and $L_{POWER_INDUCTOR}$ represents the inductance of the power inductor 16. In some embodiments of the open loop ripple compensation assist circuit 414A, the inductance of the power inductor 16 may be represented by the estimated power inductor inductance parameter, L_{EST}, discussed above with reference to the open loop assist circuit 39, depicted in Figure 2A and Figure 2B, where the estimated power inductor inductance parameter, L_{EST}, may be either the measured or

estimated inductance of the power inductor 16 between a specific range of frequencies. For example, the estimated power inductor inductance parameter, L_{EST}, may be either the measured or estimated inductance of the power inductor 16 between approximately 10MHz and 30MHz. As another example, the estimated power inductor inductance parameter, L_{EST}, may be either the measured or estimated inductance of the power inductor 16 within a band of frequencies near or within operational bandwidth of the linear radio frequency power amplifier 22. In this case, the Laplace transfer function for the high frequency ripple compensation current 416, I_{COR}, provided by the Gm assist circuit 426 may be given by equation (7) as follows:

(7) $$I_{COR}(s) = \frac{(V_{RAMP} - V_{SW_OUT_EST})}{L_{EST}} \frac{\tau_{C1}}{1+\tau_{C1}s} \frac{\tau_{C2}s}{1+\tau_{C2}s}$$

[00651] As shown in equation (7), the Laplace transfer function for the high frequency ripple compensation current 416 includes a low pass filter having a low pass time constant, τ_{C1}, and a high pass filter having a high pass time, τ_{C2}.

[00652] Figure 27A depicts another embodiment of the open loop ripple compensation assist circuit 414B which is similar to the open loop ripple compensation assist circuit 414 depicted in Figures 23A-D. For the sake of brevity, and not by way of limitation, the switch mode power supply converter 420 and circuitry associated with generation of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, depicted in Figure 24, are not depicted in Figure 27A. Also, while controller 50 is not depicted in Figure 27A, it will be understood that as depicted in Figures 23A-D, controller 50 (not shown) may configure the various elements of the open loop ripple compensation assist circuit 414B depicted in Figure 27A.

[00653] The open loop ripple compensation assist circuit 414B includes combined filter and gain assist circuitry 422B, a filter network 436, and a feedback network 438. The combined filter and gain assist circuitry 422B includes operational amplifier circuitry 440A having an operational amplifier 442, a Gm bias circuit 444, and an operational amplifier output isolation circuit 446.

[00654] The operational amplifier 442 includes a non-inverting input 442A, an inverting input 442B, and an operational amplifier output 442C. The operational amplifier 442 may include a first operational amplifier push-pull output stage circuit (not shown) that generates the operational amplifier output 442C. The non-inverting input 442A of the operational amplifier 442 is configured to receive the V_{RAMP} signal. The operational amplifier output 442C may be configured to source an operational amplifier output current, I_{AMP}, to produce an operational amplifier output voltage, V_{AMP}, across the Gm bias circuit 444.

[00655] In addition, the operational amplifier 442 may be further configured to generate or provide the high frequency ripple compensation current 416, I_{COR}, and the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}. As an example, the operational amplifier 442 may further include a second operational amplifier push-pull output stage circuit (not shown) configured to generate the high frequency ripple compensation current 416, I_{COR}. In addition, as another example, the operational amplifier 442 may further include a third operational amplifier push-pull output stage circuit (not shown) configured to generate the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}.

[00656] In some embodiments of the operational amplifier 442, the high frequency ripple compensation current 416, I_{COR}, generated by the second operational amplifier output state circuit may be substantially a mirrored current of the operational amplifier output current, I_{AMP}, provided by the first operational amplifier push-pull output stage circuit (not shown). Similarly, in some embodiments of the operational amplifier 442, the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, may be a mirrored current of the operational amplifier output current, I_{AMP}, provided by the first operational amplifier push-pull output stage circuit (not shown).

[00657] In the cases where the high frequency ripple compensation current 416, I_{COR}, and the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, are related to the operational amplifier output current, I_{AMP}, by a current mirroring arrangement, the relative dimensional relationships of

the channel widths of the respective transistor elements may be used to implement the first operational amplifier push-pull output stage circuit (not shown), the second operational amplifier push-pull output stage circuit (not shown), and the third operational amplifier push-pull output stage circuit (not shown), may be configured to relate the magnitudes of the operational amplifier output current, I_{AMP}, to the magnitudes of the high frequency ripple compensation current 416, I_{COR}, and the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}.

[00658] The operational amplifier output isolation circuit 446 includes a follower NFET 448, $NFET_{FOLLOWER}$, and an $I_{BIAS_FOLLOWER}$ current source 450. The drain of the follower NFET 448, $NFET_{FOLLOWER}$, is coupled to a circuit supply voltage, V_{DD}. In some embodiments, the supply voltage, V_{DD}, may track or be substantially equal to the battery voltage, V_{BAT}. The gate of the follower NFET 448, $NFET_{FOLLOWER}$, provides a high impedance input of the operational amplifier output isolation circuit 446, and is coupled to the operational amplifier output 442C. As a result, the gate voltage at the gate of the follower NFET 448, $NFET_{FOLLOWER}$ is equal to the operational amplifier output voltage, V_{AMP}. The follower NFET 448, $NFET_{FOLLOWER}$, may be configured such that the input gate impedance of the follower NFET 448, $NFET_{FOLLOWER}$, is very high relative to other impedances coupled to the operational amplifier output 442C in the operational frequency range of the open loop ripple compensation assist circuit 414B. As a result, the gate current, I_{GATE}, flowing into the gate of the follower NFET 448, $NFET_{FOLLOWER}$, approaches zero. The source of the follower NFET 448, $NFET_{FOLLOWER}$, is coupled to the first node 450A of the $I_{BIAS_FOLLOWER}$ current source 450. The second node 450B of the $I_{BIAS_FOLLOWER}$ current source 450 is coupled to ground. The $I_{BIAS_FOLLOWER}$ current source 450 may be configured to sink an $NFET_{FOLLOWER}$ bias current, $I_{BIAS_FOLLOWER}$, to provide a bias current for the follower NFET 448, $NFET_{FOLLOWER}$. The gate-to-source voltage of the follower NFET 448, $NFET_{FOLLOWER}$, is $V_{GS_NFET_FOLLOWER}$. The source voltage on the source of the follower NFET 448, $NFET_{FOLLOWER}$, is the feedback voltage, V_e, where $V_e = V_{AMP} - V_{GS_NFET_FOLLOWER}$. Thus, from a small signal modeling

perspective, the follower NFET 448, $NFET_{FOLLOWER}$, effectively isolates the feedback voltage, V_e, from the operational amplifier output 442C. As a result, the operational amplifier circuitry 440A includes an isolated feedback node 451 at the node created at the connection of the source of the follower NFET 448, $NFET_{FOLLOWER}$, and the first node 450A of the $I_{BIAS_FOLLOWER}$ current source 450. The isolated feedback node 451 provides the feedback voltage, V_e, to the feedback network 438.

[00659] The feedback network 438 may be coupled between the inverting input 442B of the operational amplifier 442 and the isolated feedback node 451 to provide the feedback path for the feedback current 456, $I_{FEEDBACK}$. The inverting input 442B of the operational amplifier 442 is also coupled to the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, via the filter network 436, as depicted in Figure 27A. The filter network 436 includes a filter resistor 458 coupled in series with a filter capacitor 460. The filter resistor 458 may have a filter resistance substantially equal to R_1. The filter capacitor 460 may have a filter capacitance substantially equal to C_1. The feedback network 438 may include a feedback resistor 462 coupled in parallel with a feedback capacitor 464. The feedback resistor 462 may have a feedback resistance substantially equal to R_2. The feedback capacitor 464 may have a feedback capacitance substantially equal to C_2. In some embodiments, the filter resistor 458 and/or the feedback resistor 462 may be configured to be programmable by the controller 50 (not shown). For example, the filter resistor 458 and/or the feedback resistor 462 may be a binary weighted resistor array configured to be controlled by the controller 50. As an example, the filter resistor 458 and/or the feedback resistor 462 may each be implemented as a resistor array including switches that may be programmed to be open or closed by the controller 50 (not shown). As a result, the controller 50 may selectively set the resistance value of the filter resistance, R_1 of the filter resistor 458, and the resistance value of the feedback resistance, R_2, of the feedback resistor 462, to change the frequency response of the open loop ripple compensation assist circuit 414B. In a similar fashion, or in addition to, in some embodiments, the

filter capacitor 460 and/or the feedback capacitor 464 may each be implemented as a capacitor array that may be configured by the controller 50. For example, the filter capacitor 460 and/or the feedback capacitor 464 may be a binary weighted capacitor array configured to be controlled by the controller 50. The effective capacitance of the capacitor array may be configured by the controller 50 by selectively switching in and out different capacitors in each respective capacitor array. As a result, in some embodiments, the controller 50 may be configured to selectively set the capacitance value of the filter capacitance, C_1, of the filter capacitor 460 and the capacitance value of the feedback capacitance, C_2, of the feedback capacitor 464, to change the frequency response of the open loop ripple compensation assist circuit 414B.

[00660] In addition, in some embodiments of the open loop ripple compensation assist circuit 414B, the filter resistance, R_1, of the filter resistor 458, the feedback resistance, R_2, of the feedback resistor 462, the filter capacitance, C_1, of the filter capacitor 460, and the feedback capacitance, C_2, of the feedback capacitor 464, are independently programmable by the controller 50.

[00661] Alternatively, in some embodiments, the capacitance value of the filter capacitance, C_1, of the filter capacitor 460 may be a fixed value. Similarly, in some embodiments, the feedback capacitance, C_2, of the feedback capacitor 464 may be a fixed value. Likewise, in other embodiments, the resistance value of the filter resistance, R_1, of the filter resistor 458 may be a fixed value and/or the resistance value of the feedback resistance, R_2, of the feedback resistor 462 may be a fixed value. Moreover, in some embodiments, different combinations of the filter resistance, R_1 the feedback resistance, R_2, the filter capacitance, C_1, and the feedback capacitance, C_2, of the respective filter resistor 458, the filter capacitor 460, the feedback resistor 462, and the feedback capacitor 464 may have either fixed values or programmable values of resistances and capacitances.

[00662] Similar to the open loop ripple compensation assist circuit 414A, depicted in Figure 24, the open loop ripple compensation assist circuit 414B,

depicted in Figure 27A, may be configured to provide substantially the same Laplace transfer function as the open loop ripple compensation assist circuit 414A without an integrator circuit 428 and high pass filter circuitry 430, where the high pass filter circuitry 430 includes a first high pass filter circuit 435A and a second high pass filter circuit 435B, as depicted in Figures 24 and 26 respective. Instead, the open loop ripple compensation assist circuit 414B, depicted in Figure 27A, may be described as having a low pass filter followed by a high pass filter. Similar to the open loop ripple compensation assist circuit 414A, depicted in Figure 24, the open loop ripple compensation assist circuit 414B, depicted in Figure 27, has a first time constant τ_1 and a second time constant τ_2, which may be configured by the controller 50. The first time constant τ_1 is associated with the filter network 436. The second time constant τ_2 is associated with the feedback network 438. The first time constant τ_1 is substantially equal to the product of the resistance, R_1, of the filter resistor 458 and the filter capacitance, C_1, of the filter capacitor 460, and corresponds to the first corner frequency, f_{C1}. The second time constant τ_2 is substantially equal to the product of the feedback resistance, R_2, of the feedback resistor 462 and the feedback capacitance, C_2, of the feedback capacitor 464, and corresponds to the second corner frequency, f_{C2}.

[00663] In some embodiments, the filter resistance, R_1, of the filter resistor 458 and the filter capacitance, C_1, of the filter capacitor 460 may be configured such that the first corner frequency, f_{C1}, may have a range between 3 MHz and 11.5 MHz. In other embodiments, the filter resistance, R_1, of the filter resistor 458 and the filter capacitance, C_1, of the filter capacitor 460 may be configured such that the first corner frequency, f_{C1}, may have a range between 3 MHz and 8 MHz. Similarly, the feedback resistance, R_2, of the feedback resistor 462 and the feedback capacitance, C_2, of the feedback capacitor 464 may be configured such that the second corner frequency, f_{C2}, may have a range between 3 MHz and 11.5 MHz. In other embodiments, the feedback resistance, R_2, of the feedback resistor 462 and the feedback capacitance, C_2, of the feedback capacitor 464 may be configured such that the

second corner frequency, f_{C2}, may have a range between 3 MHz and 8 MHz. As another example, the controller 50 may configure the filter resistance, R_1, the filter capacitance, C_1, feedback resistance, R_2, and the feedback capacitance, C_2, as a function of the bandwidth of the receive channel frequency band associated with each band of operation.

[00664] The Gm bias circuit 444 may include a bias resistor 452 coupled in series with a bias capacitor 454 between the operational amplifier output 442C and ground. The bias resistor 452 may have a bias resistance, R_0. As an example, in some embodiments, the bias resistor 452 may be a resistor array that is configurable by the controller 50. The value of the bias resistance, R_0, may be set by the controller 50 by selecting one or a combination of the resistors to obtain a desired effective resistance of the resistor array. In other embodiments, the value of the bias resistance, R_0, may be fixed. The bias capacitor 454 may have a bias capacitance C_0. In some embodiments, the bias capacitance, C_0, of the bias capacitor 454 may also be programmable by the controller 50. As an example, the bias capacitor 454 may be a capacitor array. As a result, the controller 50 may configure the value of the bias capacitance, C_0, of the bias capacitor 454 by selectively switching in and out various combinations of the capacitors in the capacitor array. However, in some embodiments, the value of the bias capacitance, C_0, may be fixed.

[00665] As an example configuration of the series arrangement of the bias resistor 452 and the bias capacitor 454 of the Gm bias circuit 444, the bias resistor 452 may include a first terminal and a second terminal. The bias capacitor 454 may include a first terminal coupled to the second terminal of the bias resistor 452 and a second terminal coupled to ground. The first terminal of the bias resistor 452 may be coupled to the operational amplifier output 442C.

[00666] The operational amplifier output voltage, V_{AMP}, generated at the operational amplifier output 442C may induce a Gm bias current, I_{Gm_BIAS}, through the Gm bias circuit 444. The impedance of the Gm bias circuit 444 is configured to set the transconductance of the operational amplifier 442 within the operational bandwidth of the operational amplifier 442. Because the bias

capacitor 454 blocks direct currents, the impedance of the Gm bias circuit 444 may be used to set the small signal transconductance of the operational amplifier 442. The bias capacitance, C_0, of the bias capacitor 454 may be selected such that the impedance of the Gm bias circuit 444 is dominated by the bias resistance, R_0, of the bias resistor 452 within the frequency band of operation of the open loop ripple compensation assist circuit 414B. For example, because the open loop ripple compensation assist circuit 414B is configured to generate the high frequency ripple compensation current 416, I_{COR}, to cancel out high frequency ripple currents at the power amplifier supply output 28, the bias capacitance, C_0, may be selected such that the impedance of the bias capacitor 454 is dominated by the impedance of the bias resistor 452 within the frequency band of operation of the open loop ripple compensation assist circuit 414B. Advantageously, the bias capacitor 454 is included in the Gm bias circuit 444 to reduce the current drawn by the operational amplifier 442. Accordingly, as will be described, the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442 within the frequency band of operation of the open loop ripple compensation assist circuit 414B may be set based on the value of the bias resistance, R_0, of the bias resistor 452, where the operational amplifier transconductance, Gm_{OP_AMP}, refers to the small signal transconductance of the operational amplifier 442. If the bias capacitor 454 is removed such that the bias resistor 452 is coupled between the operational amplifier output 442C and ground, the impedance of the Gm bias circuit 444 would set both the direct current transconductance and small signal transconductance of the operational amplifier 442.

[00667] Because the input gate impedance of the follower NFET 448, $NFET_{FOLLOWER}$, may be configured to be several orders of magnitude greater than the impedance of the Gm bias circuit 444, the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442 may be set based on the value of the bias resistance, R_0, of the bias resistor 452. In particular, assuming that the gate current, I_{GATE}, into the gate of the follower NFET 448, $NFET_{FOLLOWER}$, is near zero, the operational amplifier output current, I_{AMP}, is

equal to an operational amplifier output voltage, V_{AMP}, divided by the impedance of the Gm bias circuit 444. By selecting a value of the bias capacitance, C_0, of the bias capacitor 454 such that the impedance of the bias capacitor 454 is dominated by the bias resistance, R_0, of the bias resistor 452 within the frequency band of operation of the open loop ripple compensation assist circuit 414B, the impedance of the Gm bias circuit 444 is approximately equal to the bias resistance, R_0, of the bias resistor 452. As a result, the operational amplifier 442 may have an operational amplifier transconductance, Gm_{OP_AMP}, within the frequency band of operation of the open loop ripple compensation assist circuit 414B that is approximately $1/R_0$. In some embodiments, because the bias resistance, R_0, may be configured by the controller 50, the controller 50 may set the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442 by setting the resistance level of the bias resistance, R_0, of the bias resistor 452. However, if the bias capacitor 454 is removed such that the bias resistor 452 is coupled between the operational amplifier output 442C and ground, the impedance of the Gm bias circuit 444 would set both the direct current transconductance and small signal transconductance of the operational amplifier 442. The Laplace transfer function for the operational amplifier output current, I_{AMP}, when the Gm bias circuit 444 does not include the bias capacitor 454 is shown in equation (8) as follows:

$$I_{AMP}(s) = \frac{1}{R_0}\frac{R_2C_1s(V_{RAMP}-V_{SW_EST_DELAY_ICOR})}{(1+R_1C_1s)(1+R_2C_2s)} + I_{DC} \quad (8)$$

where I_{DC} represents the direct current flowing through the bias resistor 452 as if the bias capacitor 454 is not present and the bias resistor 452 is coupled between the operational amplifier output 442C and ground, and the V_{RAMP} signal represents the future value of the power amplifier supply voltage, V_{CC} and the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, represents the future value of the switching voltage, V_{SW}, at the switching voltage output 26. If the Gm bias circuit 444 includes the bias capacitor 454, where the bias capacitance, C_0, of the bias capacitor 454 is selected such the impedance of

the Gm bias circuit 444 within the frequency band of operation of the operational amplifier 442 is dominated by the bias resistance, R_0, of the bias resistor 452I, the Laplace transfer function for the operational amplifier output current, I_{AMP}, is given by equation (9) as follows:

(9) $$I_{AMP}(s) = \frac{1}{R_0}\frac{R_2C_1s(V_{RAMP}-V_{SW_EST_DELAY_ICOR})}{(1+R_1C_1s)(1+R_2C_2s)}$$

where, for the purposes of small single gain, the direct current, I_{DC}, is blocked by the bias capacitor 454.

[00668] As non-limiting example, mapping the elements of equation (7) to the elements of equation (9), shows the that open loop ripple compensation assist circuit 414B may provide the same Laplace transfer function as the open loop ripple compensation assist circuit 414A, depicted in Figure 24. For example, setting $\tau_{C1} = \tau_1 = R_1C_1$, $\tau_{C2} = \tau_2 = R_2C_2$ and $R_2C_1/R_0 = \tau_{C2}/ L_{EST}$, the transfer function of $I_{COR}(s) = I_{AMP}(s)$. Thus, for the transfer function of the open loop ripple compensation assist circuit 414B depicted in Figure 27, the first corner frequency, f_{C1}, = $1/(2\pi R_1C_1)$ and the second corner frequency, f_{C2}, = $1/(2\pi R_2C_2)$. Because the controller 50 may configure the filter resistance, R_1, of the filter resistor 458, the feedback resistance, R_2, of the feedback resistor 462, the filter capacitance, C_1, of the filter capacitor 460, and the feedback capacitance, C_2, of the feedback capacitor 464, the first high pass filter response having a first corner frequency, f_{C1}, and a second high pass filter response having a first corner frequency, f_{C2}, are also independently programmable.

[00669] If, for the sake of simplicity, and not by way of limitation, the filter capacitance, C_1, and the feedback capacitance, C_2, are selected such that $C_1=C_2=C$, mapping of the elements of equation (7) to the elements of equation (9) yields the relationships of $\tau_{C1=}R_1C$, $\tau_{C2=}R_2C$, and $R_0 = \frac{L_{EST}}{\tau_{C1}} = \frac{L_{EST}}{R_1C}$.

[00670] Based on the non-limiting example mapping described above, the transfer function for the operational amplifier output current, I_{AMP}, described in equation (9) would be substantially equal to the desired transfer function for the

high frequency ripple compensation current 416, I_{COR}, described in equation (7). However, as will be described below, in some embodiments of the open loop ripple compensation assist circuit 414B, the operational amplifier output current, I_{AMP}, is proportional to the high frequency ripple compensation current 416, I_{COR}, generated by the operational amplifier 442. In other words, the magnitude of the bias resistance, R_0, of the bias resistor 452, may be selected such that R_0 is proportional to $\frac{L_{EST}}{\tau_{C1}}$, where the relative ratios of the channel widths of the transistor elements used to implement the first operational amplifier push-pull output stage circuit of the operational amplifier 442 (not shown) and the transistor elements used to implement the second operational amplifier push-pull output stage circuit of the operational amplifier 442 (not shown) are configured such that the high frequency ripple compensation current 416, I_{COR}, generated by the operational amplifier 442 is consistent with the desired transfer function for the high frequency ripple compensation current 416, I_{COR}, described by equation (7), with respect to the open loop ripple compensation assist circuit 414A depicted in Figure 24.

[00671] As shown by the non-limiting example mapping of equation (7) to equation (9), the open loop ripple compensation assist circuit 414B, depicted in Figure 27A may be configured to provide a similar function as the open loop ripple compensation assist circuit 414A depicted in Figure 24. In other words, the embodiment of the open loop ripple compensation assist circuit 414B that includes the operational amplifier 442, the operational amplifier output isolation circuit 446, the feedback network 438, and the filter network 436, as depicted in Figure 27A, may be configured to provide a substantially similar transfer function as the open loop ripple compensation assist circuit 414A depicted in Figure 24.

[00672] Generation of the high frequency ripple compensation current 416, I_{COR}, and the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, as a function of the operational amplifier output current, I_{AMP}, will now be discussed with reference to Figure 31A and Figures 32A-32C.

[00673] Figure 31A depicts an embodiment of the operational amplifier circuitry 440A having the operational amplifier 442, where the operational

amplifier circuitry 440A includes the operational amplifier 442 in combination with both an embodiment of the Gm bias circuit 444 and an embodiment of the operational amplifier output isolation circuit 446. The embodiment of the operational amplifier circuitry 440A depicted in Figure 31A will be described with continuing reference to the operational amplifier circuitry 440A depicted in Figure 27, with reference to Figure 32A and Figure 32B, and the embodiments of the Gm Bias Circuit 444 and the operational amplifier output isolation circuit 446 depicted in Figure 32C.

[00674] The embodiment of the operational amplifier 442, depicted in Figure 31A, may include an embodiment of the operational amplifier front-end stage circuit 466, an embodiment of the operational amplifier push-pull output stage circuit 468, an embodiment of the operational amplifier controlled I_{COR} current circuit 470, and an embodiment of the operational amplifier controlled I_{COR_SENSE} current circuit 472. The embodiments of the operational amplifier front-end stage circuit 466, the operational amplifier push-pull output stage circuit 468, the operational amplifier controlled I_{COR} current circuit 470, and the operational amplifier controlled I_{COR_SENSE} current circuit 472, depicted in Figure 31A, are each configured receive the circuit supply voltage, V_{DD}. The embodiment of the operational amplifier output isolation circuit 446 depicted in Figure 32C is configured receive the circuit supply voltage, V_{DD}.

[00675] The operational amplifier push-pull output stage circuit 468 may be a push-pull output stage operably coupled to the operational amplifier output 442C. The operational amplifier push-pull output stage circuit 468 may be configured to provide an operational amplifier output current, I_{AMP}, and to generate a operational amplifier output voltage, V_{AMP}, at the operational amplifier output 442C.

[00676] The operational amplifier controlled I_{COR} current circuit 470 includes an operational amplifier controlled I_{COR} current output 470A configured to provide the high frequency ripple compensation current 416, I_{COR}. In addition, the operational amplifier controlled I_{COR} current circuit 470 may be configured as a push-pull output stage having a programmable transconductance, Gm_{ICOR}, where

the magnitude of the high frequency ripple compensation current 416, I_{COR}, is proportionally related to the amplifier output current, I_{AMP}, based on the relative dimensional relationships of the channel widths of the transistor elements used to implement the operational amplifier push-pull output stage circuit 468 and the operational amplifier controlled I_{COR} current circuit 470. Similarly, the operational amplifier controlled I_{COR_SENSE} current circuit 472 includes an operational amplifier controlled I_{COR_SENSE} current output 472A configured to provide the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, where the relative dimensional relationships of the channel widths of the transistor elements used to implement the operational amplifier controlled I_{COR} current circuit 470 and the operational amplifier controlled I_{COR_SENSE} current circuit 472 may be configured to determine a relationship between the magnitude of the high frequency ripple compensation current 416, I_{COR}, and the magnitude of the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}. For example, the relative dimensional relationships of the channel widths of the transistor elements used to implement the operational amplifier controlled I_{COR} current circuit 470 and the operational amplifier controlled I_{COR_SENSE} current circuit 472 may be configured such that the operational amplifier controlled I_{COR_SENSE} current circuit 472 may be configured to provide a scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, that is fractionally proportional to the high frequency ripple compensation current 416, I_{COR}. For example, the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, may be fractionally related to the high frequency ripple compensation current 416, I_{COR}, by a sense scaling factor, $C_{SENSE_SCALING}$.

[00677] The operational amplifier front-end stage circuit 466 includes a non-inverting input (+) that corresponds to the non-inverting input 442A of the operational amplifier 442 depicted in Figure 27A. In addition, the operational amplifier front-end stage circuit 466 includes an inverting input (-) that corresponds to the inverting input 442B of the operational amplifier 442 depicted in Figure 27A. Based on the voltage difference between the non-inverting input 442A and the inverting input 442B of the operational amplifier 442, the

operational amplifier front-end stage circuit 466 generates an output stage $PFET_A$ control signal 474 and an output stage $NFET_A$ control signal 476 that are used to control the operation of the operational amplifier push-pull output stage circuit 468, the operational amplifier controlled I_{COR} current circuit 470, and the operational amplifier controlled I_{COR_SENSE} current circuit 472.

[00678] The controller 50 may be configured to provide an I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0) and an I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0) to the operational amplifier controlled I_{COR} current circuit 470. As will be described, the controller 50 may programmatically control the magnitude of the high frequency ripple compensation current 416, I_{COR}, via the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0) and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0). Similarly, the controller 50 may be configured to provide an I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1), and an I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1), to the operational amplifier controlled I_{COR_SENSE} current circuit 472. As will also be described, the controller 50 may programmatically control the magnitude of a scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, via the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1), and the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1).

[00679] The operational amplifier push-pull output stage circuit 468 is configured to receive the output stage $PFET_A$ control signal 474 and the output stage $NFET_A$ control signal 476. Based on the output stage $PFET_A$ control signal 474 and the output stage $NFET_A$ control signal 476, the operational amplifier push-pull output stage circuit 468 is configured to generate the operational amplifier output current, I_{AMP}, at the operational amplifier output 442C.

[00680] As further depicted in Figure 32A, the operational amplifier push-pull output stage circuit 468 includes a first push-pull output PFET 486, $PFET_A$, and a first push-pull output NFET 488, $NFET_A$. The drain of the first push-pull output PFET 486, $PFET_A$, and the drain of the first push-pull output NFET 488, $NFET_A$,

are coupled to form a substantially symmetrical push-pull output arrangement of the operational amplifier output 442C. The source of the first push-pull output PFET 486, $PFET_A$, is coupled to the circuit supply voltage, V_{DD}. The source of the first push-pull output NFET 488, $NFET_A$, is coupled to ground. The gate of the first push-pull output PFET 486, $PFET_A$, is configured to receive the output stage $PFET_A$ control signal 474, which sets the voltage on the gate of the first push-pull output PFET 486, $PFET_A$, to a $PFET_A$ control voltage, $V_{PFET_A_CNTR}$. The gate of the first push-pull output NFET 488, $NFET_A$, is configured to receive the output stage $NFET_A$ control signal 476, which sets the voltage on the gate of the first push-pull output NFET 488, $NFET_A$, to an $NFET_A$ control voltage, $V_{NFET_A_CNTR}$.

[00681] The operational amplifier front-end stage circuit 466 controls the $PFET_A$ control voltage, $V_{PFET_A_CNTR}$ and the $NFET_A$ control voltage, $V_{NFET_A_CNTR}$ such that when the voltage difference between the non-inverting input 442A and the inverting input 442B of the operational amplifier 442 is substantially equal to zero, the current passing through the first push-pull output PFET 486, $PFET_A$, is substantially equal to the current passing through the first push-pull output NFET 488, $NFET_A$, such that the operational amplifier output current, I_{AMP}, generated by the operational amplifier push-pull output stage circuit 468, at the operational amplifier output 442C, is substantially equal to zero. As a result, the operational amplifier output voltage, V_{AMP}, generated at the connection of the drain of the first push-pull output PFET 486, $PFET_A$, and the drain of the first push-pull output NFET 488, $NFET_A$, is also substantially equal to zero.

[00682] Otherwise, depending upon the voltage difference developed between the non-inverting input 442A and the inverting input 442B of the operational amplifier 442, the operational amplifier front-end stage circuit 466 controls the $PFET_A$ control voltage, $V_{PFET_A_CNTR}$ and the $NFET_A$ control voltage, $V_{NFET_A_CNTR}$, such that the operational amplifier output current, I_{AMP}, generated by the operational amplifier push-pull output stage circuit 468 either sources or sinks current. When the operational amplifier push-pull output stage circuit 468 sources current, in other words, the operational amplifier output current, I_{AMP}, is

greater than zero, the current flowing through the drain of the first push-pull output PFET 486, $PFET_A$, is greater than the current flowing through the first push-pull output NFET 488, $NFET_A$. Correspondingly, when the operational amplifier push-pull output stage circuit 468 sinks current, in other words the operational amplifier output current, I_{AMP}, is less than zero, the current flowing through the drain of the first push-pull output PFET 486, $PFET_A$, is less than the current flowing through the first push-pull output NFET 488, $NFET_A$.

[00683] The operational amplifier controlled I_{COR} current circuit 470 may be configured as an array of mirrored transistor elements arranged to form a substantially symmetric push-pull output stage 489 for providing the high frequency ripple compensation current 416, I_{COR}. The substantially symmetric push-pull output stage 489 may include a programmable array of mirrored source current elements 490 and a programmable array of mirrored sink current elements 492 coupled to form a substantially symmetric programmable push-pull output stage 491. Each of the mirrored transistor elements in the programmable array of mirrored source current elements 490 is associated with a corresponding transistor element of the mirrored transistor elements in the programmable array of mirrored sink current elements 492.

[00684] The substantially symmetric push-pull output stage 489 may further include mirrored transistor elements configured to form a substantially symmetric I_{COR} current push-pull output stage 493. The substantially symmetric I_{COR} current push-pull output stage 493 may be configured to provide an I_{COR} offset current carrying capacity in the case where the programmable array of mirrored source current elements 490 and the programmable array of mirrored sink current elements 492 are disabled or turned off.

[00685] The mirrored source transistor elements of the substantially symmetric push-pull output stage 489 may include a first push-pull output PFET 486, $PFET_A$, a second mirrored PFET 496, $PFET_{A1}$, a third mirrored PFET 498, $PFET_{A2}$, a fourth mirrored PFET 500, $PFET_{A3}$, a fifth mirrored PFET 502, $PFET_{A4}$, a sixth mirrored PFET 504, $PFET_{A5}$, and a seventh mirrored PFET 506, $PFET_{A6}$.

[00686] The channel width of each of the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, and the sixth mirrored PFET 504, $PFET_{A5}$ are configured such that the current carrying capacity of the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, and the sixth mirrored PFET 504, $PFET_{A5}$, are binary weighted. As a result, the current carrying capacity of the second mirrored PFET 496, $PFET_{A1}$, is substantially twice the current carrying capacity of the first mirrored PFET 494, $PFET_{A0}$, the current carrying capacity of the third mirrored PFET 498, $PFET_{A2}$ is substantially twice the current carrying capacity of the second mirrored PFET 496, $PFET_{A1}$, the current carrying capacity of the fourth mirrored PFET 500, $PFET_{A3}$ is substantially twice the current carrying capacity of the third mirrored PFET 498, $PFET_{A2}$, the current carrying capacity of the fifth mirrored PFET 502, $PFET_{A4}$, is substantially twice the current carrying capacity of the fourth mirrored PFET 500, $PFET_{A3}$, and the current carrying capacity of the sixth mirrored PFET 504, $PFET_{A5}$ is substantially twice the current carrying capacity of the fifth mirrored PFET 502, $PFET_{A4}$. The channel width of the seventh mirrored PFET 506, $PFET_{A6}$ is configured relative to the channel width of the first push-pull output PFET 486, $PFET_{A}$, to provide an I_{COR} offset source current carrying capacity for the substantially symmetric I_{COR} current push-pull output stage 493 of the operational amplifier controlled I_{COR} current circuit 470.

[00687] The programmable array of mirrored source current elements 490 may further include a first control mirrored PFET 508, $PFET_{CP0}$, a second control mirrored PFET 510, $PFET_{CP1}$, a third control mirrored PFET 512, $PFET_{CP2}$, a fourth control mirrored PFET 514, $PFET_{CP3}$, a fifth control mirrored PFET 516, $PFET_{CP4}$, and a sixth control mirrored PFET 518, $PFET_{CP5}$. As further depicted in Figure 32A, the programmable array of mirrored source current elements 490 may be coupled to or further include the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0). The I_{COR} source current weight control bus 478,

CNTR_CP_BUS (5:0) includes a first control mirrored PFET signal 520, CNTR_CP0, a second control mirrored PFET signal 522, CNTR_CP1, a third control mirrored PFET signal 524, CNTR_CP2, a fourth control mirrored PFET signal 526, CNTR_CP3, a fifth control mirrored PFET signal 528, CNTR_CP4, and a sixth control mirrored PFET signal 530, CNTR_CP5.

[00688] The first control mirrored PFET signal 520, CNTR_CP0, the second control mirrored PFET signal 522, CNTR_CP1, the third control mirrored PFET signal 524, CNTR_CP2, the fourth control mirrored PFET signal 526, CNTR_CP3, the fifth control mirrored PFET signal 528, CNTR_CP4, and the sixth control mirrored PFET signal 530, CNTR_CP5 are respectively coupled to and configured so as to control the gate of each of the first control mirrored PFET 508, $PFET_{CP0}$, the second control mirrored PFET 510, $PFET_{CP1}$, the third control mirrored PFET 512, $PFET_{CP2}$, the fourth control mirrored PFET 514, $PFET_{CP3}$, the fifth control mirrored PFET 516, $PFET_{CP4}$, and the sixth control mirrored PFET 518, $PFET_{CP5}$.

[00689] Accordingly, as will be described in further detail below, the programmable array of mirrored source current elements 490 includes the first control mirrored PFET 508, $PFET_{CP0}$, the second control mirrored PFET 510, $PFET_{CP1}$, the third control mirrored PFET 512, $PFET_{CP2}$, the fourth control mirrored PFET 514, $PFET_{CP3}$, the fifth control mirrored PFET 516, $PFET_{CP4}$, and the sixth control mirrored PFET 518, $PFET_{CP5}$, that are respectively combined with the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, and the sixth mirrored PFET 504, $PFET_{A5}$ in order to form a first programmable mirrored source current element 494A, a second programmable mirrored source current element 496A, a third programmable mirrored source current element 498A, a fourth programmable mirrored source current element 500A, a fifth programmable mirrored source current element 502A, and a sixth programmable mirrored source current element 504A.

[00690] The programmable array of mirrored source current elements 490 of the substantially symmetric push-pull output stage 489 will now be described. The gate of each of the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, the sixth mirrored PFET 504, $PFET_{A5}$, and the seventh mirrored PFET 506, $PFET_{A6}$ are each coupled to the output stage $PFET_A$ control signal 474 such that the each of the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, and the sixth mirrored PFET 504, $PFET_{A5}$, and the seventh mirrored PFET 506, $PFET_{A6}$ is current mirrored to the first push-pull output PFET 486, $PFET_A$ of the operational amplifier push-pull output stage circuit 468. As a result, the gate voltage for each of the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, and the sixth mirrored PFET 504, $PFET_{A5}$, and the seventh mirrored PFET 506, $PFET_{A6}$ is substantially set equal to the $PFET_A$ control voltage, $V_{PFET_A_CNTR}$.

[00691] The programmable array of mirrored source current elements 490 includes the first programmable mirrored source current element 494A, the second programmable mirrored source current element 496A, the third programmable mirrored source current element 498A, the fourth programmable mirrored source current element 500A, the fifth programmable mirrored source current element 502A, and the sixth programmable mirrored source current element 504A, where the current carrying capacity of the first programmable mirrored source current element 494A, the second programmable mirrored source current element 496A, the third programmable mirrored source current element 498A, the fourth programmable mirrored source current element 500A, the fifth programmable mirrored source current element 502A, and the sixth programmable mirrored source current element 504A, are substantially binary weighted. The current contribution of each of the first programmable mirrored

source current element 494A, the second programmable mirrored source current element 496A, the third programmable mirrored source current element 498A, the fourth programmable mirrored source current element 500A, the fifth programmable mirrored source current element 502A, and the sixth programmable mirrored source current element 504A, to form the high frequency ripple compensation current 416, I_{COR}, is governed by the controller 50 via the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0).

[00692] The first programmable mirrored source current element 494A includes the first mirrored PFET 494, $PFET_{A0}$, and is formed by coupling the source of the first mirrored PFET 494, $PFET_{A0}$, to circuit supply voltage, V_{DD}, and the drain of the first mirrored PFET 494, $PFET_{A0}$, to the source of the first control mirrored PFET 508, $PFET_{CP0}$. The drain of the first control mirrored PFET 508, $PFET_{CP0}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the first control mirrored PFET 508, $PFET_{CP0}$, is coupled to the first control mirrored PFET signal 520, CNTR_CP0, such that the controller 50 may control the operation state (on/off) of the first programmable mirrored source current element 494A. The second programmable mirrored source current element 496A includes the second mirrored PFET 496, $PFET_{A1}$, and is formed by coupling the source of the second mirrored PFET 496, $PFET_{A1}$, to circuit supply voltage, V_{DD}, and the drain of the second mirrored PFET 496, $PFET_{A1}$, to the source of the second control mirrored PFET 510, $PFET_{CP1}$. The drain of the second control mirrored PFET 510, $PFET_{CP1}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the second control mirrored PFET 510, $PFET_{CP1}$, is coupled to the second control mirrored PFET signal 522, CNTR_CP1, such that the controller 50 may control the operation state (on/off) of the second programmable mirrored source current element 496A. The third programmable mirrored source current element 498A includes the third mirrored PFET 498, $PFET_{A2}$, and is formed by coupling the source of the third mirrored PFET 498, $PFET_{A2}$, to circuit supply voltage, V_{DD}, and the drain of the third mirrored PFET 498, $PFET_{A2}$, to the source of the third control mirrored PFET 512, $PFET_{CP2}$. The drain of the third control mirrored

PFET 512, $PFET_{CP2}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the third control mirrored PFET 512, $PFET_{CP2}$, is coupled to the third control mirrored PFET signal 524, CNTR_CP2, such that the controller 50 may control the operation state (on/off) of the third programmable mirrored source current element 498A. The fourth programmable mirrored source current element 500A includes the fourth mirrored PFET 500, $PFET_{A3}$, and is formed by coupling the source of the fourth mirrored PFET 500, $PFET_{A3}$, to circuit supply voltage, V_{DD}, and the drain of the fourth mirrored PFET 500, $PFET_{A3}$, to the source of the fourth control mirrored PFET 514, $PFET_{CP3}$. The drain of the fourth control mirrored PFET 514, $PFET_{CP3}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the fourth control mirrored PFET 514, $PFET_{CP3}$, is coupled to the fourth control mirrored PFET signal 526, CNTR_CP3, such that the controller 50 may control the operation state (on/off) of the fourth programmable mirrored source current element 500A. The fifth programmable mirrored source current element 502A includes the fifth mirrored PFET 502, $PFET_{A4}$, and is formed by coupling the source of the fifth mirrored PFET 502, $PFET_{A4}$, to circuit supply voltage, V_{DD}, and the drain of the fifth mirrored PFET 502, $PFET_{A4}$, to the source of the fifth control mirrored PFET 516, $PFET_{CP4}$. The drain of the fifth control mirrored PFET 516, $PFET_{CP4}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the fifth control mirrored PFET 516, $PFET_{CP4}$, is coupled to the fifth control mirrored PFET signal 528, CNTR_CP4, such that the controller 50 may control the operation state (on/off) of the fifth programmable mirrored source current element 502A. The sixth programmable mirrored source current element 504A includes the sixth mirrored PFET 504, $PFET_{A5}$, and is formed by coupling the source of the sixth mirrored PFET 504, $PFET_{A5}$, to circuit supply voltage, V_{DD}, and the drain of the sixth mirrored PFET 504, $PFET_{A5}$, to the source of the sixth control mirrored PFET 518, $PFET_{CP5}$. The drain of the sixth control mirrored PFET 518, $PFET_{CP5}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the sixth control mirrored PFET 518, $PFET_{CP5}$, is coupled to the sixth control mirrored PFET signal 530,

CNTR_CP5, such that the controller 50 may control the operation state (on/off) of the sixth programmable mirrored source current element 504A.

[00693] Similar to the programmable array of mirrored source current elements 490, the programmable array of mirrored sink current elements 492 of the mirrored sink transistor elements of the substantially symmetric push-pull output stage 489 may include a first mirrored NFET 532, $NFET_{A0}$, a second mirrored NFET 534, $NFET_{A1}$, a third mirrored NFET 536, $NFET_{A2}$, a fourth mirrored NFET 538, $NFET_{A3}$, a fifth mirrored NFET 540, $NFET_{A4}$, a sixth mirrored NFET 542, $NFET_{A5}$, and a seventh mirrored NFET 543, $NFET_{A6}$.

[00694] The channel width of each of the first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, and the sixth mirrored NFET 542, $NFET_{A5}$ are binary weighted or configured such that current carrying capacity of the second mirrored NFET 534, $NFET_{A1}$, is substantially twice the current carrying capacity of the first mirrored NFET 532, $NFET_{A0}$, the current carrying capacity of the third mirrored NFET 536, $NFET_{A2}$ is substantially twice the current carrying capacity of the second mirrored NFET 534, $NFET_{A1}$, the current carrying capacity of the fourth mirrored NFET 538, $NFET_{A3}$ is substantially twice the current carrying capacity of the third mirrored NFET 536, $NFET_{A2}$, the current carrying capacity of the fifth mirrored NFET 540, $NFET_{A4}$, is substantially twice the current carrying capacity of the fourth mirrored NFET 538, $NFET_{A3}$, and the current carrying capacity of the sixth mirrored NFET 542, $NFET_{A5}$ is substantially twice the current carrying capacity of the fifth mirrored NFET 540, $NFET_{A4}$. The channel width of the seventh mirrored NFET 543, $NFET_{A6}$ is configured relative to the channel width of the first push-pull output NFET 488, $NFET_A$, to provide an I_{COR} offset sink current carrying capacity for the substantially symmetric I_{COR} current push-pull output stage 493 of the operational amplifier controlled I_{COR} current circuit 470.

[00695] Furthermore, the channel width of each of the first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540,

$NFET_{A4}$, the sixth mirrored NFET 542, $NFET_{A5}$, and the seventh mirrored NFET 543, $NFET_{A6}$, is configured such that the current carrying capacity of each of the first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, the sixth mirrored NFET 542, $NFET_{A5}$, and the seventh mirrored NFET 543, $NFET_{A6}$, substantially matches the respective current carrying capacity of the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, the sixth mirrored PFET 504, $PFET_{A5}$ and the seventh mirrored PFET 506, $PFET_{A6}$.

[00696] Accordingly, the respective channel widths of the first mirrored PFET 494, $PFET_{A0}$, and the first mirrored NFET 532, $NFET_{A0}$, are configured such that the current sourcing capacity of the first mirrored PFET 494, $PFET_{A0}$, is substantially matched to the current sinking capacity of the first mirrored NFET 532, $NFET_{A0}$. The respective channel widths of the second mirrored PFET 496, $PFET_{A1}$, and the second mirrored NFET 534, $NFET_{A1}$, are configured such that the current sourcing capacity of the second mirrored PFET 496, $PFET_{A1}$, is substantially matched to the current sinking capacity of the second mirrored NFET 534, $NFET_{A1}$. The respective channel widths of the third mirrored PFET 498, $PFET_{A2}$, and the third mirrored NFET 536, $NFET_{A2}$, are configured such that the current sourcing capacity of the third mirrored PFET 498, $PFET_{A2}$, is substantially matched to the current sinking capacity of the third mirrored NFET 536, $NFET_{A2}$. The respective channel widths of the fourth mirrored PFET 500, $PFET_{A3}$, and the fourth mirrored NFET 538, $NFET_{A3}$, are configured such that the current sourcing capacity of the fourth mirrored PFET 500, $PFET_{A3}$, is substantially matched to the current sinking capacity of the fourth mirrored NFET 538, $NFET_{A3}$. The respective channel widths of the fifth mirrored PFET 502, $PFET_{A4}$, and the fifth mirrored NFET 540, $NFET_{A4}$, are configured such that the current sourcing capacity of the fifth mirrored PFET 502, $PFET_{A4}$, is substantially matched to the current sinking capacity of the fifth mirrored NFET 540, $NFET_{A4}$. The respective channel widths of the sixth mirrored

PFET 504, $PFET_{A5}$, and the sixth mirrored NFET 542, $NFET_{A5}$, are configured such that the current sourcing capacity of the sixth mirrored PFET 504, $PFET_{A5}$, is substantially matched to the current sinking capacity of the sixth mirrored NFET 542, $NFET_{A5}$. And, the respective channel widths of the seventh mirrored PFET 506, $PFET_{A6}$, and the seventh mirrored NFET 543, $NFET_{A6}$, are configured such that the current sourcing capacity of the seventh mirrored PFET 506, $PFET_{A6}$, is substantially matched to the current sinking capacity of the seventh mirrored NFET 543, $NFET_{A6}$.

[00697] The programmable array of mirrored sink current elements 492 may further include a first control mirrored NFET 544, $NFET_{CN0}$, a second control mirrored NFET 546, $NFET_{CN1}$, a third control mirrored NFET 548, $NFET_{CN2}$, a fourth control mirrored NFET 550, $NFET_{CN3}$, a fifth control mirrored NFET 552, $NFET_{CN4}$, and a sixth control mirrored NFET 554, $NFET_{CN5}$. As further depicted in Figure 32A, the programmable array of mirrored sink current elements 492 may further include or be coupled to the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0). The I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0) includes a first control mirrored NFET signal 556, CNTR_CN0, a second control mirrored NFET signal 558, CNTR_CN1, a third control mirrored NFET signal 560, CNTR_CN2, a fourth control mirrored NFET signal 562, CNTR_CN3, a fifth control mirrored NFET signal 564, CNTR_CN4, and a sixth control mirrored NFET signal 566, CNTR_CN5.

[00698] The first control mirrored NFET signal 556, CNTR_CN0, the second control mirrored NFET signal 558, CNTR_CN1, the third control mirrored NFET signal 560, CNTR_CN2, the fourth control mirrored NFET signal 562, CNTR_CN3, the fifth control mirrored NFET signal 564, CNTR_CN4, and the sixth control mirrored NFET signal 566, CNTR_CN5 are respectively coupled to and configured so as to control the gate of each of the first control mirrored NFET 544, $NFET_{CN0}$, the second control mirrored NFET 546, $NFET_{CN1}$, the third control mirrored NFET 548, $NFET_{CN2}$, the fourth control mirrored NFET 550, $NFET_{CN3}$, the fifth control mirrored NFET 552, $NFET_{CN4}$, and the sixth control mirrored NFET 554, $NFET_{CN5}$.

[00699] Accordingly, as will be described in further detail below, the programmable array of mirrored sink current elements 492 includes the first control mirrored NFET 544, $NFET_{CN0}$, a second control mirrored NFET 546, $NFET_{CN1}$, a third control mirrored NFET 548, $NFET_{CN2}$, a fourth control mirrored NFET 550, $NFET_{CN3}$, a fifth control mirrored NFET 552, $NFET_{CN4}$, and a sixth control mirrored NFET 554, $NFET_{CN5}$, that are respectively combined with the first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, and the sixth mirrored NFET 542, $NFET_{A5}$ in order to form a first programmable mirrored sink current element 532A, a second programmable mirrored sink current element 534A, a third programmable mirrored sink current element 536A, a fourth programmable mirrored sink current element 538A, a fifth programmable mirrored sink current element 540A, and a sixth programmable mirrored sink current element 542A.

[00700] The programmable array of mirrored sink current elements 492 of the substantially symmetric push-pull output stage 489 will now be described. The gate of each of the first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, the sixth mirrored NFET 542, $NFET_{A5}$, and the seventh mirrored NFET 543, $NFET_{A6}$ are each coupled to the output stage $NFET_A$ control signal 476 such that the each of the first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, the sixth mirrored NFET 542, $NFET_{A5}$, and the seventh mirrored NFET 543, $NFET_{A6}$ is current mirrored to the first push-pull output NFET 488, $NFET_A$, of the *o*perational amplifier push-pull output stage circuit 468. As a result, the gate voltage for each of the first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, the sixth mirrored NFET 542, $NFET_{A5}$, and the seventh mirrored

NFET 543, $NFET_{A6}$ is substantially set equal to the $NFET_A$ control voltage, $V_{NFET_A_CNTR}$.

[00701] The programmable array of mirrored sink current elements 492 includes the first programmable mirrored sink current element 532A, the second programmable mirrored sink current element 534A, the third programmable mirrored sink current element 536A, the fourth programmable mirrored sink current element 538A, the fifth programmable mirrored sink current element 540A, and the sixth programmable mirrored sink current element 542A, where the current carrying capacity of the first programmable mirrored sink current element 532A, the second programmable mirrored sink current element 534A, the third programmable mirrored sink current element 536A, the fourth programmable mirrored sink current element 538A, the fifth programmable mirrored sink current element 540A, and the sixth programmable mirrored sink current element 542A are substantially binary weighted. The current contribution of each of the first programmable mirrored sink current element 532A, the second programmable mirrored sink current element 534A, the third programmable mirrored sink current element 536A, the fourth programmable mirrored sink current element 538A, the fifth programmable mirrored sink current element 540A, and the sixth programmable mirrored sink current element 542A to form the high frequency ripple compensation current 416, I_{COR}, is governed by the controller 50 via the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0).

[00702] The first programmable mirrored sink current element 532A includes the first mirrored NFET 532, $NFET_{A0}$, and is formed by coupling the source of the first mirrored NFET 532, $NFET_{A0}$, to ground and the drain of the first mirrored NFET 532, $NFET_{A0}$, to the source of the first control mirrored NFET 544, $NFET_{CN0}$. The drain of the first control mirrored NFET 544, $NFET_{CN0}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the first control mirrored NFET 544, $NFET_{CN0}$, is coupled to the first control mirrored NFET signal 556, CNTR_CN0, such that the controller 50 may control the operation state (on/off) of the first programmable mirrored sink current

element 532A. The second programmable mirrored sink current element 534A includes the second mirrored NFET 534, $NFET_{A1}$, and is formed by coupling the source of the second mirrored NFET 534, $NFET_{A1}$, to ground, and the drain of the second mirrored NFET 534, $NFET_{A1}$, to the source of the second control mirrored NFET 546, $NFET_{CN1}$. The drain of the second control mirrored NFET 546, $NFET_{CN1}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the second control mirrored NFET 546, $NFET_{CN1}$, is coupled to the second control mirrored NFET signal 558, CNTR_CN1, such that the controller 50 may control the operation state (on/off) of the second programmable mirrored sink current element 534A. The third programmable mirrored sink current element 536A includes the third mirrored NFET 536, $NFET_{A2}$, and is formed by coupling the source of the third mirrored NFET 536, $NFET_{A2}$, to ground, and the drain of the third mirrored NFET 536, $NFET_{A2}$, to the source of the third control mirrored NFET 548, $NFET_{CN2}$. The drain of the third control mirrored NFET 548, $NFET_{CN2}$, is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the third control mirrored NFET 548, $NFET_{CN2}$, is coupled to the third control mirrored NFET signal 560, CNTR_CN2, such that the controller 50 may control the operation state (on/off) of the third programmable mirrored sink current element 536A. The fourth programmable mirrored sink current element 538A includes the fourth mirrored NFET 538, $NFET_{A3}$, and is formed by coupling the source of the fourth mirrored NFET 538, $NFET_{A3}$, to ground, and the drain of the fourth mirrored NFET 538, $NFET_{A3}$, to the source of the fourth control mirrored NFET 550, $NFET_{CN3}$. The drain of the fourth control mirrored NFET 550, $NFET_{CN3}$ is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the fourth control mirrored NFET 550, $NFET_{CN3}$, is coupled to the fourth control mirrored NFET signal 562, CNTR_CN3, such that the controller 50 may control the operation state (on/off) of the fourth programmable mirrored sink current element 538A. The fifth programmable mirrored sink current element 540A includes the fifth mirrored NFET 540, $NFET_{A4}$, and is formed by coupling the source of the fifth mirrored NFET 540, $NFET_{A4}$, to ground, and the drain of the

fifth mirrored NFET 540, $NFET_{A4}$, to the source of the fifth control mirrored NFET 552, $NFET_{CN4}$. The drain of the fifth control mirrored NFET 552, $NFET_{CN4}$ is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the fifth control mirrored NFET 552, $NFET_{CN4}$, is coupled to the fifth control mirrored NFET signal 564, CNTR_CN4, such that the controller 50 may control the operation state (on/off) of the fifth programmable mirrored sink current element 540A. The sixth programmable mirrored sink current element 542A includes the sixth mirrored NFET 542, $NFET_{A5}$, and is formed by coupling the source of the sixth mirrored NFET 542, $NFET_{A5}$, to ground, and the drain of the sixth mirrored NFET 542, $NFET_{A5}$, to the source of the sixth control mirrored NFET 554, $NFET_{CN5}$. The drain of the sixth control mirrored NFET 554, $NFET_{CN5}$ is coupled to the operational amplifier controlled I_{COR} current output 470A. The gate of the sixth control mirrored NFET 554, $NFET_{CN5}$, is coupled to the sixth control mirrored NFET signal 566, CNTR_CN5, such that the controller 50 may control the operation state (on/off) of the sixth programmable mirrored sink current element 542A.

[00703] The substantially symmetric I_{COR} current push-pull output stage 493 may include the seventh mirrored PFET 506, $PFET_{A6}$, and the seventh mirrored NFET 543, $NFET_{A6}$. As described above, the respective channel widths of the seventh mirrored PFET 506, $PFET_{A6}$, and the seventh mirrored NFET 543, $NFET_{A6}$, are configured such that the current sourcing capacity of the seventh mirrored PFET 506, $PFET_{A6}$, is substantially matched to the current sinking capacity of the seventh mirrored NFET 543, $NFET_{A6}$. As a result, the substantially symmetric I_{COR} current push-pull output stage 493 may provide an I_{COR} offset current carrying capacity when the programmable array of mirrored source current elements 490 and the programmable array of mirrored sink current elements 492 are disabled or turned off. Because the channel widths of the seventh mirrored PFET 506, $PFET_{A6}$ and the seventh mirrored NFET 543, $NFET_{A6}$, are configured such that the current carry capacity of the seventh mirrored PFET 506, $PFET_{A6}$, matches the seventh mirrored NFET 543, $NFET_{A6}$, the I_{COR} offset current carrying capacity is governed by the ratio of the channel

width of the seventh mirrored PFET 506, $PFET_{A6}$, to the first push-pull output PFET 486, $PFET_A$, and the ratio of the channel width of the seventh mirrored NFET 543, $NFET_{A6}$, to the first push-pull output NFET 488, $NFET_A$.

[00704] To maintain symmetric operation of the substantially symmetric I_{COR} current push-pull output stage 493, the controller 50 controls the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0), and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0), such that the operational state of the first programmable mirrored source current element 494A follows the operational state of the corresponding first programmable mirrored sink current element 532A, the operational state of the second programmable mirrored source current element 496A follows the operational state of the corresponding second programmable mirrored sink current element 534A, the operational state of the third programmable mirrored source current element 498A follows the operational state of the corresponding third programmable mirrored sink current element 536A, the operational state of the fourth programmable mirrored source current element 500A follows the operational state of the corresponding fourth programmable mirrored sink current element 538A, the operational state of the fifth programmable mirrored source current element 502A follows the operational state of the corresponding fifth programmable mirrored sink current element 540A, and the operational state of the sixth programmable mirrored source current element 504A follows the operational state of the corresponding sixth programmable mirrored sink current element 542A.

[00705] In the case where the controller 50 configures the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0), and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0), to turn off the first programmable mirrored source current element 494A, the second programmable mirrored source current element 496A, the third programmable mirrored source current element 498A, the fourth programmable mirrored source current element 500A, the fifth programmable mirrored source current element 502A, the sixth programmable mirrored source current element 504A, the first programmable mirrored sink current element 532A, the second programmable mirrored sink

current element 534A, the third programmable mirrored sink current element 536A, the fourth programmable mirrored sink current element 538A, the fifth programmable mirrored sink current element 540A, and the sixth programmable mirrored sink current element 542A. The substantially symmetric I_{COR} current push-pull output stage 493 provides the I_{COR} offset current capacity as the output of the substantially symmetric push-pull output stage 489 of the operational amplifier controlled I_{COR} current circuit 470.

[00706] The programmable I_{COR} transconductance, Gm_{ICOR}, of the operational amplifier controlled I_{COR} current circuit 470 may now be described. For the sake of simplicity of the description, and not by way of limitation, the first push-pull output PFET 486, $PFET_A$, and the first push-pull output NFET 488, $NFET_A$, of the operational amplifier push-pull output stage circuit 468 are used as a reference transistor such that the characteristics of the first mirrored PFET 494, $PFET_{A0}$, are similar to the characteristics of the first push-pull output PFET 486, $PFET_A$, and the characteristics of the first mirrored NFET 532, $NFET_{A0}$, are similar to the characteristics of the first push-pull output NFET 488, $NFET_A$. As previously discussed, the relative channel widths of the first push-pull output PFET 486, $PFET_A$, and the first push-pull output NFET 488, $NFET_A$, to the channel widths of the first mirrored PFET 494, $PFET_{A0}$, and the first mirrored NFET 532, $NFET_{A0}$, may be configured to obtain a desired proportionality between the high frequency ripple compensation current 416, I_{COR}, to the operational amplifier output current, I_{AMP}.

[00707] The individual control signals of the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0), and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0), may be characterized as corresponding to a six bit programmable control word CNTRN, where the least significant bit corresponds to the state of the CNTR_CP0 and CNTR_CN0, and the most significant bit corresponds to the state of CNTR_CP5 and CNTR_CN5. As a result, the programmable control word CNTRN may be characterized as having the binary weighted values of between 0 and 63. Thus, the six bit programmable control word may be characterized as the function CNTRN = P, such that $0 \leq P \leq$

63. Thus, the programmable I_{COR} transconductance, Gm_{ICOR}, of the operational amplifier controlled I_{COR} current circuit 470 may be characterized by equation (10) as follows:

(10) $$Gm_{ICOR}(P) = \frac{(P+P_{OFFSET})}{R_0}$$

where P_{OFFSET} reflects the contribution of the substantially symmetric I_{COR} current push-pull output stage 493.

[00708] Figure 33 depicts the programmable I_{COR} transconductance Gm_{ICOR} of the operational amplifier controlled I_{COR} current circuit 470 versus the value (P) of the programmable control word, CNTRN. In some embodiments, the channel width ratio of the seventh mirrored PFET 506, $PFET_{A6}$ to the channel width of the seventh mirrored NFET 543, $NFET_{A6}$ may be configured such that P_{OFFSET} has a minimum value of around 20. In the case where P_{OFFSET} = 20, the minimum programmable I_{COR} transconductance $Gm_{ICOR_MIN} = 20/R_0$, where R_0 is the bias resistance of the bias resistor 452 of the Gm bias circuit 444, depicted in Figure 32C.

[00709] Furthermore, relative channel widths of the first mirrored PFET 494, $PFET_{A0}$, the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, the sixth mirrored PFET 504, $PFET_{A5}$, and the seventh mirrored PFET 506, $PFET_{A6}$, to the channel width of the first push-pull output PFET 486, $PFET_A$, and the relative channel widths of first mirrored NFET 532, $NFET_{A0}$, the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, the sixth mirrored NFET 542, $NFET_{A5}$, and the seventh mirrored NFET 543, $NFET_{A6}$, to the first push-pull output NFET 488, $NFET_A$, may be adjusted such that the operational amplifier output current, I_{AMP}, is proportional to the high frequency ripple compensation current 416, I_{COR}. It will be appreciated that when the operational amplifier controlled I_{COR} current circuit 470 is configured to have the minimum programmable I_{COR} transconductance Gm_{ICOR_MIN}, the high frequency

ripple compensation current 416, I_{COR}, is sourced only by the substantially symmetric I_{COR} current push-pull output stage 493.

[00710] Typically, the ratio of the channel width of the first push-pull output PFET 486, $PFET_A$, to the channel width of the first mirrored PFET 494, $PFET_{A0}$, and the ratio of the channel width of the first push-pull output NFET 488, $NFET_A$, to the channel width of the first mirrored NFET 532, $NFET_{A0}$, is approximately set to one. However, in some embodiments, the ratio of the channel width of the first push-pull output PFET 486, $PFET_A$, to the channel width of the first mirrored PFET 494, $PFET_{A0}$, and the ratio of the channel width of the first push-pull output NFET 488, $NFET_A$, to the channel width of the first mirrored NFET 532, $NFET_{A0}$, may be greater than one or less than one. For example, in the case where the ratio of the channel width of the first push-pull output PFET 486, $PFET_A$, to the channel width of the first mirrored PFET 494, $PFET_{A0}$, and the ratio of the channel width of the first push-pull output NFET 488, $NFET_A$, to the channel width of the first mirrored NFET 532, $NFET_{A0}$, is less than one, the bias resistance, R_0, of the bias resistor 452, depicted in Figure 32C, may be increased to obtain the same value of the programmable I_{COR} transconductance, Gm_{ICOR}, of the operational amplifier controlled I_{COR} current circuit 470, depicted in Figure 32A, and reduce the Gm bias current, I_{Gm_BIAS}. However, this may reduce the operational bandwidth of the operational amplifier 442.

[00711] Figure 33 depicts a graphical representation of the programmable I_{COR} transconductance, Gm_{ICOR}, of the operational amplifier controlled I_{COR} current circuit 470 provided at the operational amplifier controlled I_{COR} current output 470A as a function of the six bit programmable control word, CNTRN, formed by the bits of the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0), and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0). The programmable control word, CNTRN, may be characterized as having the binary weighted values equal to "P" such that $0 \leq P \leq 63$. As depicted in Figure 33, the programmable I_{COR} transconductance, Gm_{ICOR}, is substantially linear with respect to "P" for $0 \leq P \leq 63$. The minimum programmable I_{COR} transconductance Gm_{ICOR_MIN}, corresponds to the value of

$Gm_{ICOR}(0)$. In other words, the programmable I_{COR} transconductance, Gm_{ICOR}, of the operational amplifier controlled I_{COR} current circuit 470 may be configured to provide 64 transconductance values.

[00712] The embodiment of the operational amplifier controlled I_{COR_SENSE} current circuit 472, depicted in Figure 32B, is similar in form and function to the embodiment of the operational amplifier controlled I_{COR} current circuit 470 depicted in Figure 32A. Similar to the operational amplifier controlled I_{COR} current circuit 470, the operational amplifier controlled I_{COR_SENSE} current circuit 472 may be configured as an array of mirrored transistor element arranged to form a substantially symmetric push-pull output stage 567 for providing the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}. The substantially symmetric push-pull output stage 567 may include a programmable array of mirrored sense source current elements 568 and a programmable array of mirrored sense sink current elements 570 coupled to form a substantially symmetric programmable I_{COR_SENSES} push-pull output stage 569. Each of the mirrored transistor elements in the programmable array of mirrored sense source current elements 568 is associated with a corresponding transistor element of the mirrored transistor elements in the programmable array of mirrored sense sink current elements 570.

[00713] The substantially symmetric programmable I_{COR_SENSES} push-pull output stage 569 may further include mirrored transistor elements configured to form a substantially symmetric I_{COR_SENSE} current push-pull output stage 571. The substantially symmetric I_{COR_SENSE} current push-pull output stage 571 may be configured to provide an I_{COR_SENSE} offset current carrying capacity in the case when the programmable array of mirrored sense source current elements 568 and the programmable array of mirrored sense sink current elements 570 are disabled or turned off. Accordingly, the substantially symmetric I_{COR_SENSE} current push-pull output stage 571 complements the operation of the substantially symmetric I_{COR} current push-pull output stage 493. Accordingly, as will be described, the minimum I_{COR_SENSE} transconductance, $Gm_{ICOR_SENSE_MIN}$ of the operational amplifier controlled I_{COR_SENSE} current circuit 472 is scaled by the

sense scaling factor, $C_{SENSE_SCALING}$, such that $Gm_{ICOR_SENSE_MIN} = Gm_{ICOR_MIN} \times C_{SENSE_SCALING}$.

[00714] However, by way of example and not by limitation, unlike the substantially symmetric programmable push-pull output stage 491 of the operational amplifier controlled I_{COR} current circuit 470, depicted in Figure 32A, which includes six programmable sense mirrored source current elements and six programmable sense mirrored sink current elements, as will be described, the embodiment of the substantially symmetric programmable I_{COR_SENSES} push-pull output stage 569 of the operational amplifier controlled I_{COR_SENSE} current circuit 472, depicted in Figure 32B, includes five programmable sense mirrored source current elements and five corresponding programmable sense mirrored sink current elements. In addition, the channel widths of the sense mirrored transistor element of the operational amplifier controlled I_{COR_SENSE} current circuit 472 may be scaled by the sense scaling factor, $C_{SENSE_SCALING}$, such that the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, generated by the operational amplifier controlled I_{COR_SENSE} current circuit 472, is a fractional representation of the high frequency ripple compensation current 416, I_{COR}, generated by the operational amplifier controlled I_{COR} current circuit 470. For example, in some embodiments of the operational amplifier controlled I_{COR_SENSE} current circuit 472, the sense scaling factor, $C_{SENSE_SCALING}$, is 1/20. In other words, the magnitude of the high frequency ripple compensation current 416, I_{COR}, is substantially linearly related to the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, by the sense scaling factor, $C_{SENSE_SCALING}$, such that $I_{COR} = I_{COR_SENSE} \times C_{SENSE_SCALING}$.

[00715] In addition, as described above, in some embodiments of the operational amplifier controlled I_{COR_SENSE} current circuit 472, the programmable array of mirrored sense source current elements 568 and the programmable array of mirrored sense sink current elements 570 may each have fewer mirrored transistor elements than the programmable array of mirrored source current elements 490 and the programmable array of mirrored sink current elements 492 of the operational amplifier controlled I_{COR} current circuit 470. For example,

because the embodiment of the operational amplifier controlled I_{COR_SENSE} current circuit 472, depicted in Figure 32B, only includes five programmable sense mirrored source current elements and five corresponding programmable sense mirrored sink current elements, changes in the magnitude of the current of the high frequency ripple compensation current 416, I_{COR}, due to the operation of the first programmable mirrored source current element 494A and the first programmable mirrored sink current element 532A are not represented by a corresponding change in the magnitude of current of the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}.

[00716] The substantially symmetric push-pull output stage 567 may include a first sense mirrored PFET 572, $PFET_{S1}$, a second sense mirrored PFET 574, $PFET_{S2}$, a third sense mirrored PFET 576, $PFET_{S3}$, a fourth sense mirrored PFET 578, $PFET_{S4}$, a fifth sense mirrored PFET 580, $PFET_{S5}$, and a sixth sense mirrored PFET 582, $PFET_{S6}$. The respective channel widths of each of the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, and the fifth sense mirrored PFET 580, $PFET_{S5}$, may be configured such that the current carrying capacity of each one of the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, and the fifth sense mirrored PFET 580, $PFET_{S5}$, is fractionally related to the current carrying capacity of the second mirrored PFET 496, $PFET_{A1}$, the third mirrored PFET 498, $PFET_{A2}$, the fourth mirrored PFET 500, $PFET_{A3}$, the fifth mirrored PFET 502, $PFET_{A4}$, and the sixth mirrored PFET 504, $PFET_{A5}$, of the operational amplifier controlled I_{COR} current circuit 470, respectively, by the sense scaling factor, $C_{SENSE_SCALING}$. In other words, the channel widths of the transistor elements of the programmable array of mirrored sense source current elements 568 of the operational amplifier controlled I_{COR_SENSE} current circuit 472 are configured such that the current providing capacity of the programmable array of mirrored sense source current elements 568 is fractionally related to the current providing capacity of the programmable array of mirrored source current

elements 490 of the operational amplifier controlled I_{COR} current circuit 470. As an example, the channel width of the first sense mirrored PFET 572, $PFET_{S1}$, may be substantially related to the channel width of the second mirrored PFET 496, $PFET_{A1}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the second sense mirrored PFET 574, $PFET_{S2}$, may be substantially related to the channel widths of the third mirrored PFET 498, $PFET_{A2}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the third sense mirrored PFET 576, $PFET_{S3}$, may be substantially related to the channel width of the fourth mirrored PFET 500, $PFET_{A3}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the fourth sense mirrored PFET 578, $PFET_{S4}$, may be substantially related to the channel width of the fifth mirrored PFET 502, $PFET_{A4}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the fifth sense mirrored PFET 580, $PFET_{S5}$, may be substantially related to the channel width of the sixth mirrored PFET 504, $PFET_{A5}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. As a result, the current carrying capacity of the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, the fifth sense mirrored PFET 580, $PFET_{S5}$, are also configured to be substantially binary weighted. For example, the channel width of the mirrored source transistor elements of the programmable array of mirrored sense source current elements 568 may be configured such that the current carrying capacity of the second sense mirrored PFET 574, $PFET_{S2}$, is substantially twice the current carrying capacity of the first sense mirrored PFET 572, $PFET_{S1}$, the current carrying capacity of the third sense mirrored PFET 576, $PFET_{S3}$ is substantially twice the current carrying capacity of the second sense mirrored PFET 574, $PFET_{S2}$, the current carrying capacity of the fourth sense mirrored PFET 578, $PFET_{S4}$ is substantially twice the current carrying capacity of the third sense mirrored PFET 576, $PFET_{S3}$, and the current carrying capacity of the fifth sense mirrored PFET 580, $PFET_{S5}$, is substantially twice the current carrying capacity of the fourth sense mirrored PFET 578, $PFET_{S4}$. As a result, the current carrying capacities of the transistor

elements of the programmable array of mirrored sense source current elements 568 may be substantially related to the corresponding transistor elements of the programmable array of mirrored source current elements 490 of the operational amplifier controlled I_{COR} current circuit 470 by the sense scaling factor, $C_{SENSE_SCALING}$, in order to maintain the fractional relationship of the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, generated by the operational amplifier control I_{COR_SENSE} current circuit 472, to the high frequency ripple compensation current 416, I_{COR}, generated by the operational amplifier controlled I_{COR} current circuit 470.

[00717] The programmable array of mirrored sense source current elements 568 may further include a first control sense mirrored PFET 584, $PFET_{SP1}$, a second control sense mirrored PFET 586, $PFET_{SP2}$, a third control sense mirrored PFET 588, $PFET_{SP3}$, a fourth control sense mirrored PFET 590, $PFET_{SP4}$, and a fifth control sense mirrored PFET 592, $PFET_{SP5}$. The first control sense mirrored PFET 584, $PFET_{SP1}$, the second control sense mirrored PFET 586, $PFET_{SP2}$, the third control sense mirrored PFET 588, $PFET_{SP3}$, the fourth control sense mirrored PFET 590, $PFET_{SP4}$, and the fifth control sense mirrored PFET 592, $PFET_{SP5}$, may be used in conjunction with the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, the fifth sense mirrored PFET 580, $PFET_{S5}$, and the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1) to create a first control sense mirrored PFET 584, $PFET_{SP1}$, a second control sense mirrored PFET 586, $PFET_{SP2}$, a third control sense mirrored PFET 588, $PFET_{SP3}$, a fourth control sense mirrored PFET 590, $PFET_{SP4}$, and a fifth control sense mirrored PFET 592, $PFET_{SP5}$, respectively, to form a first programmable sense mirrored source current element 572A, a second programmable sense mirrored source current element 574A, a third programmable sense mirrored source current element 576A, a fourth programmable sense mirrored source current element 578A, and a fifth programmable sense mirrored source current element 580A.

[00718] As further depicted in Figure 32B, the programmable array of mirrored sense source current elements 568 may be operably coupled to the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1). The I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1) may include a first control sense mirrored PFET signal 594, CNTR_SP1, coupled to the gate of the first control sense mirrored PFET 584, $PFET_{SP1}$, a second control sense mirrored PFET signal 596, CNTR_SP2, coupled to the gate of the second control sense mirrored PFET 586, $PFET_{SP2}$, a third control sense mirrored PFET signal 598, CNTR_SP3, coupled to the gate of the third control sense mirrored PFET 588, $PFET_{SP3}$, a fourth control sense mirrored PFET signal 600, CNTR_SP4, coupled to the gate of the fourth control sense mirrored PFET 590, $PFET_{SP4}$, and a fifth control sense mirrored PFET signal 602, CNTR_SP5, coupled to the gate of the fifth control sense mirrored PFET 592, $PFET_{SP5}$.

[00719] The first control sense mirrored PFET signal 594, CNTR_SP1, may be configured to control the operational state (ON/OFF) of the first control sense mirrored PFET 584, $PFET_{SP1}$. The second control sense mirrored PFET signal 596, CNTR_SP2, may be configured to control the operational state (ON/OFF) of the second control sense mirrored PFET 586, $PFET_{SP2}$. The third control sense mirrored PFET signal 598, CNTR_SP3, may be configured to control the operational state (ON/OFF) of the third control sense mirrored PFET 588, $PFET_{SP3}$. The fourth control sense mirrored PFET signal 600, CNTR_SP4, may be configured to control the operational state (ON/OFF) of the fourth control sense mirrored PFET 590, $PFET_{SP4}$. The fifth control sense mirrored PFET signal 602, CNTR_SP5 may be configured to control the operational state (ON/OFF) of the fifth control sense mirrored PFET 592, $PFET_{SP5}$.

[00720] The first programmable sense mirrored source current element 572A may be formed by coupling the source of the first sense mirrored PFET 572, $PFET_{S1}$, to the circuit supply voltage, V_{DD}, and the drain of the first sense mirrored PFET 572, $PFET_{S1}$, to the source of the first control sense mirrored PFET 584, $PFET_{SP1}$. The drain of the first control sense mirrored PFET 584,

$PFET_{SP1,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The second programmable sense mirrored source current element 574A may be formed by coupling the source of the second sense mirrored PFET 574, $PFET_{S2}$, to the circuit supply voltage, V_{DD}, and the drain of the second sense mirrored PFET 574, $PFET_{S2}$, to the source of the second control sense mirrored PFET 586, $PFET_{SP2}$. The drain of the second control sense mirrored PFET 586, $PFET_{SP2,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The third programmable sense mirrored source current element 576A, may be formed by coupling the source of the third sense mirrored PFET 576, $PFET_{S3}$, to the circuit supply voltage, V_{DD}, and the drain of the third sense mirrored PFET 576, $PFET_{S3}$, to the source of the third control sense mirrored PFET 588, $PFET_{SP3}$. The drain of the third control sense mirrored PFET 588, $PFET_{SP3,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The fourth programmable sense mirrored source current element 578A may be formed by coupling the source of the fourth sense mirrored PFET 578, $PFET_{S4}$, to the circuit supply voltage, V_{DD}, and the drain of the fourth sense mirrored PFET 578, $PFET_{S4}$, to the source of the fourth control sense mirrored PFET 590, $PFET_{SP4}$. The drain of the fourth control sense mirrored PFET 590, $PFET_{SP4,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The fifth programmable sense mirrored source current element 580A may be formed by coupling the source of the fifth sense mirrored PFET 580, $PFET_{S5}$, to the circuit supply voltage, V_{DD}, and the drain of the fifth sense mirrored PFET 580, $PFET_{S5}$, to the source of the fifth control sense mirrored PFET 592, $PFET_{SP5}$. The drain of the fifth control sense mirrored PFET 592, $PFET_{SP4,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A.

[00721] The gate of each of the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, the fifth sense mirrored PFET 580, $PFET_{S5}$, and the sixth sense mirrored PFET 582, $PFET_{S6}$, is coupled to the output stage $PFET_A$ control signal 474 such that the each of the first sense

mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, the fifth sense mirrored PFET 580, $PFET_{S5}$, and the sixth sense mirrored PFET 582, $PFET_{S6}$, is current mirrored to the first push-pull output PFET 486, $PFET_A$, of the operational amplifier push-pull output stage circuit 468. As a result, the gate voltage for each of the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, the fifth sense mirrored PFET 580, $PFET_{S5}$, and the sixth sense mirrored PFET 582, $PFET_{S6}$, is substantially set equal to the $PFET_A$ control voltage, $V_{PFET_A_CNTR}$, provided by the output stage $PFET_A$ control signal 474.

[00722] Accordingly, the magnitude of the current provided by the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, and the fifth sense mirrored PFET 580, $PFET_{S5}$, is governed by the $PFET_A$ control voltage, $V_{PFET_A_CNTR}$. The controller 50 may configure the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1), to selectively place the first programmable sense mirrored source current element 572A, the second programmable sense mirrored source current element 574A, the third programmable sense mirrored source current element 576A, the fourth programmable sense mirrored source current element 578A, and the fifth programmable sense mirrored source current element 580A, in an OFF state or an ON state to govern the contribution of current sourced by each of the first sense mirrored PFET 572, $PFET_{S1}$, the second sense mirrored PFET 574, $PFET_{S2}$, the third sense mirrored PFET 576, $PFET_{S3}$, the fourth sense mirrored PFET 578, $PFET_{S4}$, and the fifth sense mirrored PFET 580, $PFET_{S5}$, to form the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}. Because the sixth sense mirrored PFET 582, $PFET_{S6}$, is not part of a programmable source current element, the sixth sense mirrored PFET 582, $PFET_{S6}$, sources current to the output of the operational amplifier controlled I_{COR_SENSE} current output 472A

dependent upon the $PFET_A$ control voltage, $V_{PFET_A_CNTR}$. The current sourced by the sixth sense mirrored PFET 582, $PFET_{S6}$, may be used to provide the I_{COR_SENSE} offset current carrying capacity of the substantially symmetric I_{COR_SENSE} current push-pull output stage 571.

[00723] As a non-limiting example, the programmable array of mirrored sense sink current elements 570 may include fewer mirrored transistor elements than the programmable array of mirrored sink current elements 492 of the operational amplifier controlled I_{COR} current circuit 470. However, in order for the substantially symmetric push-pull output stage 567 to be balanced, the programmable array of mirrored sense source current elements 568 and the programmable array of mirrored sense sink current elements 570 have complementary numbers of mirrored transistor elements. Accordingly, in the example embodiment of the operational amplifier controlled I_{COR_SENSE} current circuit 472, the substantially symmetric push-pull output stage 567 further includes a first sense mirrored NFET 604, $NFET_{S1}$, a second sense mirrored NFET 606, $NFET_{S2}$, a third sense mirrored NFET 608, $NFET_{S3}$, a fourth sense mirrored NFET 610, $NFET_{S4}$, a fifth sense mirrored NFET 612, $NFET_{S5}$, and a sixth sense mirrored NFET 614, $NFET_{S6}$. The first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, and the fifth sense mirrored NFET 612, $NFET_{S5}$, may be configured to form the programmable array of mirrored sense sink current elements 570.

[00724] Similar to the substantially symmetric push-pull output stage 567, the channel widths of the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$, are configured such that current carrying capacity of each one of the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$, is

fractionally related to the current carrying capacity of the second mirrored NFET 534, $NFET_{A1}$, the third mirrored NFET 536, $NFET_{A2}$, the fourth mirrored NFET 538, $NFET_{A3}$, the fifth mirrored NFET 540, $NFET_{A4}$, the sixth mirrored NFET 542, $NFET_{A5}$, and the seventh mirrored NFET 543, $NFET_{A6}$, of the programmable array of mirrored sink current elements 492, respectively, by the sense scaling factor, $C_{SENSE_SCALING}$.

[00725] In other words, the channel widths of the transistor elements of the programmable array of mirrored sense sink current elements 570 of the operational amplifier controlled I_{COR_SENSE} current circuit 472 are configured such that the current providing capacity of the programmable array of mirrored sense sink current elements 570 is fractionally related to the current providing capacity of the programmable array of mirrored sink current elements 492 of the operational amplifier controlled I_{COR} current circuit 470. As an example, the channel width of the first sense mirrored NFET 604, $NFET_{S1}$, may be substantially related to the channel widths of the second mirrored NFET 534, $NFET_{A1}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the second sense mirrored NFET 606, $NFET_{S2}$, may be substantially related to the channel width of the third mirrored NFET 536, $NFET_{A2}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the third sense mirrored NFET 608, $NFET_{S3}$, may be substantially related to the channel width of the fourth mirrored NFET 538, $NFET_{A3}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the fourth sense mirrored NFET 610, $NFET_{S4}$, may be substantially related to the channel width of the fifth mirrored NFET 540, $NFET_{A4}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$. The channel width of the fifth sense mirrored NFET 612, $NFET_{S5}$, may be substantially related to the channel width of the sixth mirrored NFET 542, $PFET_{A5}$, as a function of the sense scaling factor, $C_{SENSE_SCALING}$.

[00726] As a result, the current carrying capacity of the second sense mirrored NFET 606, $NFET_{S2}$, is substantially twice the current carrying capacity of the first sense mirrored NFET 604, $NFET_{S1}$, the current carrying capacity of the third sense mirrored NFET 608, $NFET_{S3}$ is substantially twice the current carrying

capacity of the second sense mirrored NFET 606, $NFET_{S2}$, the current carrying capacity of the fourth sense mirrored NFET 610, $NFET_{S4}$ is substantially twice the current carrying capacity of the third sense mirrored NFET 608, $NFET_{S3}$, and the current carrying capacity of the fifth sense mirrored NFET 612, $NFET_{S5}$, is substantially twice the current carrying capacity of the fourth sense mirrored NFET 610, $NFET_{S4}$. Thus the channel widths of the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, are substantially configured to sink binary weighted current.

[00727] As a result, similar to the programmable array of mirrored sense source current elements 568, the current carrying capacities of the transistor elements of the programmable array of mirrored sense sink current elements 570 may be substantially related to the corresponding transistor elements of the programmable array of mirrored sink current elements 492 of the operational amplifier controlled I_{COR} current circuit 470 by the sense scaling factor, $C_{SENSE_SCALING}$, in order to maintain the fractional relationship of the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, generated by the operational amplifier control I_{COR_SENSE} current circuit 472, to the high frequency ripple compensation current 416, I_{COR}, generated by the operational amplifier controlled I_{COR} current circuit 470.

[00728] The programmable array of mirrored sense sink current elements 570 may further include a first control sense mirrored NFET 616, $NFET_{SN1}$, a second control sense mirrored NFET 618, $NFET_{SN2}$, a third control sense mirrored NFET 620, $NFET_{SN3}$, a fourth control sense mirrored NFET 622, $NFET_{SN4}$, and a fifth control sense mirrored NFET 624, $NFET_{SN5}$. The first control sense mirrored NFET 616, $NFET_{SN1}$, the second control sense mirrored NFET 618, $NFET_{SN2}$, the third control sense mirrored NFET 620, $NFET_{SN3}$, the fourth control sense mirrored NFET 622, $NFET_{SN4}$, and the fifth control sense mirrored NFET 624, $NFET_{SN5}$, may be used in conjunction with the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored

NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, and the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1) to form a first programmable sense mirrored sink current element 604A, a second programmable sense mirrored sink current element 606A, a third programmable sense mirrored sink current element 608A, a fourth programmable sense mirrored sink current element 610A, and a fifth programmable sense mirrored sink current element 612A.

[00729] In some alternative embodiments of the operational amplifier circuitry 440A, portions of the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1), the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1), the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0), and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0) may be combined to form a single control bus that controls both the operational amplifier controlled I_{COR} current circuit 470 and the operational amplifier controlled I_{COR_SENSE} current circuit 472.

[00730] As further depicted in Figure 32B, the programmable array of mirrored sense sink current elements 570 may be operably coupled to the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1). The I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1) may include a first control sense mirrored NFET signal 626, CNTR_SN1, coupled to the gate of the first control sense mirrored NFET 616, $NFET_{SN1}$, a second control sense mirrored NFET signal 628, CNTR_SN2, coupled to the gate of the second control sense mirrored NFET 618, $NFET_{SN2}$, a third control sense mirrored NFET signal 630, CNTR_SN3, coupled to the gate of the third control sense mirrored NFET 620, $NFET_{SN3}$, a fourth control sense mirrored NFET signal 632, CNTR_SN4, coupled to the gate of the fourth control sense mirrored NFET 622, $NFET_{SN4}$, and a fifth control sense mirrored NFET signal 634, CNTR_SN5, coupled to the gate of the fifth control sense mirrored NFET 624, $NFET_{SN5}$.

[00731] The first control sense mirrored NFET signal 626, CNTR_SN1, may be configured to control the operational state (ON/OFF) of the first control sense mirrored NFET 616, $NFET_{SN1}$. The second control sense mirrored NFET

signal 628, CNTR_SN2, may be configured to control the operational state (ON/OFF) of the second control sense mirrored NFET 618, $NFET_{SN2}$. The third control sense mirrored NFET signal 630, CNTR_SN3, may be configured to control the operational state (ON/OFF) of the third control sense mirrored NFET 620, $NFET_{SN3}$. The fourth control sense mirrored NFET signal 632, CNTR_SN4, may be configured to control the operational state (ON/OFF) of the fourth control sense mirrored NFET 622, $NFET_{SN4}$. The fifth control sense mirrored NFET signal 634, CNTR_SN5 may be configured to control the operational state (ON/OFF) of the fifth control sense mirrored NFET 624, $NFET_{SN5}$.

[00732] The first programmable sense mirrored sink current element 604A may be formed by coupling the source of the first sense mirrored NFET 604, $NFET_{S1}$, to ground, and the drain of the first sense mirrored NFET 604, $NFET_{S1}$, to the source of the first control sense mirrored NFET 616, $NFET_{SN1}$. The drain of the first control sense mirrored NFET 616, $NFET_{SN1,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The second programmable sense mirrored sink current element 606A may be formed by coupling the source of the second sense mirrored NFET 606, $NFET_{S2}$, to ground, and the drain of the second sense mirrored NFET 606, $NFET_{S2}$, to the source of the second control sense mirrored NFET 618, $NFET_{SN2}$. The drain of the second control sense mirrored NFET 618, $NFET_{SN2,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The third programmable sense mirrored sink current element 608A, may be formed by coupling the source of the third sense mirrored NFET 608, $NFET_{S3}$, to ground, and the drain of the third sense mirrored NFET 608, $NFET_{S3}$, to the source of the third control sense mirrored NFET 620, $NFET_{SN3}$. The drain of the third control sense mirrored NFET 620, $NFET_{SN3,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The fourth programmable sense mirrored sink current element 610A may be formed by coupling the source of the fourth sense mirrored NFET 610, $NFET_{S4}$, to ground, and the drain of the fourth sense mirrored NFET 610, $NFET_{S4}$, to the source of the fourth control sense mirrored NFET 622, $NFET_{SN4}$. The drain of the

fourth control sense mirrored NFET 622, $NFET_{SN4,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. The fifth programmable sense mirrored sink current element 612A may be formed by coupling the source of the fifth sense mirrored NFET 612, $NFET_{S5,}$ to ground, and the drain of the fifth sense mirrored NFET 612, $NFET_{S5}$, to the source of the fifth control sense mirrored NFET 624, $NFET_{SN5}$. The drain of the fifth control sense mirrored NFET 624, $NFET_{SN4,}$ is coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A.

[00733] The gate of each of the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$, is coupled to the output stage $NFET_A$ control signal 476 such that the each of the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$,is current mirrored to the first push-pull output NFET 488, $NFET_A$, of the operational amplifier push-pull output stage circuit 468. As a result, the gate voltage for each of the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$, is substantially set equal to the $NFET_A$ control voltage, $V_{NFET_A_CNTR}$, provided by the output stage $NFET_A$ control signal 476.

[00734] Accordingly, the magnitude of the current provided by the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, is governed by the $NFET_A$ control voltage, $V_{NFET_A_CNTR}$, provided by the output stage $NFET_A$ control signal from the operational amplifier front-end stage circuit 466.

[00735] The controller 50 may configure the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1), to selectively place the first programmable sense mirrored sink current element 604A, the second programmable sense mirrored sink current element 606A, the third programmable sense mirrored sink current element 608A, the fourth programmable sense mirrored sink current element 610A, and the fifth programmable sense mirrored sink current element 612A, in an OFF state or an ON state to govern the contribution of current sunk by each of the first sense mirrored NFET 604, $NFET_{S1}$, the second sense mirrored NFET 606, $NFET_{S2}$, the third sense mirrored NFET 608, $NFET_{S3}$, the fourth sense mirrored NFET 610, $NFET_{S4}$, the fifth sense mirrored NFET 612, $NFET_{S5}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$. Because the sixth sense mirrored NFET 614, $NFET_{S6}$, is not part of a programmable sink current element, the sixth sense mirrored NFET 614, $NFET_{S6}$, sinks current from the output of the operational amplifier controlled I_{COR_SENSE} current output 472A dependent upon the $NFET_A$ control voltage, $V_{NFET_A_CNTR}$.

[00736] Accordingly, the substantially symmetric I_{COR_SENSE} current push-pull output stage 571 is formed by coupling the source of the sixth sense mirrored PFET 582, $PFET_{S6}$, to the circuit supply voltage, V_{DD}, and the source of the sixth sense mirrored NFET 614, $NFET_{S6}$, to ground. The drain of the sixth sense mirrored PFET 582, $PFET_{S6}$, and the drain of the sixth sense mirrored NFET 614, $NFET_{S6}$, are each coupled to the operational amplifier controlled I_{COR_SENSE} current output 472A. As previously described, the gate of the sixth sense mirrored PFET 582, $PFET_{S6}$, is coupled to the output stage $PFET_A$ control signal 474 and the gate of the sixth sense mirrored NFET 614, $NFET_{S6}$, are coupled to the output stage $NFET_A$ control signal 476. The sixth sense mirrored PFET 582, $PFET_{S6}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$, form the substantially symmetric I_{COR_SENSE} current push-pull output stage 571 that is mirrored to the operational amplifier output current, I_{AMP}, provided by the operational amplifier push-pull output stage circuit 468.

[00737] Furthermore, the channel width of the sixth sense mirrored PFET 582, $PFET_{S6}$, and the sixth sense mirrored NFET 614, $NFET_{S6}$, are configured to be proportionally scaled to the seventh mirrored PFET 506, $PFET_{A6}$, and the seventh mirrored NFET 543, $NFET_{A6}$, such that the I_{COR_SENSE} offset current capacity is fractionally related to the I_{COR} offset current carrying capacity by the sense scaling factor, $C_{SENSE_SCALING}$.

[00738] In order to configure the programmable array of mirrored sense source current elements 568 and the programmable array of mirrored sense sink current elements 570 to operate as a substantially symmetric programmable I_{COR_SENSES} push-pull output stage 569, the controller 50 controls the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1), and the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1), such that the operational state of the first programmable sense mirrored source current element 572A is associated with the operational state of the corresponding first programmable sense mirrored sink current element 604A, the operational state of the second programmable sense mirrored source current element 574A is associated with the operational state of the corresponding second programmable sense mirrored sink current element 606A, the operational state of the third programmable sense mirrored source current element 576A is associated with the operational state of the corresponding third programmable sense mirrored sink current element 608A, the operational state of the fourth programmable sense mirrored source current element 578A is associated with the operational state of the fourth programmable sense mirrored sink current element 610A, and the operational state of the fifth programmable sense mirrored source current element 580A is associated with the operational state of the corresponding fifth programmable sense mirrored sink current element 612A.

[00739] In addition, to maintain proper scaling between the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and the high frequency ripple compensation current 416, I_{COR}, the current carrying capacity of the first programmable sense mirrored source current element 572A, the second programmable sense mirrored source current element 574A, the third

programmable sense mirrored source current element 576A, the fourth programmable sense mirrored source current element 578A, the fifth programmable sense mirrored source current element 580A, the first programmable sense mirrored sink current element 604A, the second programmable sense mirrored sink current element 606A, the third programmable sense mirrored sink current element 608A, the fourth programmable sense mirrored sink current element 610A, and the fifth programmable sense mirrored sink current element 612A, and the symmetric I_{COR_SENSE} current push-pull output stage 571 are scaled based on the sense scaling factor, $C_{SENSE_SCALING}$, with respect to the current carrying capacity of the second programmable mirrored source current element 496A, the third programmable mirrored source current element 498A, the fourth programmable mirrored source current element 500A, the fifth programmable mirrored source current element 502A, the sixth programmable mirrored source current element 504A, the second programmable mirrored sink current element 534A, the third programmable mirrored sink current element 536A, the fourth programmable mirrored sink current element 538A, the fifth programmable mirrored sink current element 540A, the sixth programmable mirrored sink current element 542A, and the substantially symmetric I_{COR} current push-pull output stage 493.

[00740] In some embodiments, the controller configures the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1) and the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1), based on the five most significant bits of the programmable control word, CNTRN, used to configure the programmable I_{COR} transconductance, Gm_{ICOR}, of the operational amplifier controlled I_{COR} current circuit 470.

[00741] As an example, the controller 50 may configure the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS (5:1) and the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS (5:1), to substantially track the operation of the I_{COR} source current weight control bus 478, CNTR_CP_BUS (5:0), and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS (5:0) in

order to maintain the sense scaling factor, $C_{SENSE_SCALING}$, relationship between the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and the high frequency ripple compensation current 416, I_{COR}.

[00742] Illustratively, in the embodiment of the operational amplifier controlled I_{COR_SENSE} current circuit 472 depicted in Figure 32B, which includes five programmable sense mirrored source current elements and five corresponding programmable sense mirrored sink current elements, the controller 50 may configure the second control mirrored PFET signal 522, CNTR_CP1, the second control mirrored NFET signal 558, CNTR_CN1, the first control sense mirrored PFET signal 594, CNTR_SP1, and the first control sense mirrored NFET signal 626, CNTR_SN1, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. The controller 50 may configure the third control mirrored PFET signal 524, CNTR_CP2, the third control mirrored NFET signal 560, CNTR_CN2, the second control sense mirrored PFET signal 596, CNTR_SP2, and the second control sense mirrored NFET signal 628, CNTR_SN2, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. The controller 50 may also configure the fourth control mirrored PFET signal 526, CNTR_CP3, the fourth control mirrored NFET signal 562, CNTR_CN3, the third control sense mirrored PFET signal 598, CNTR_SP3, and the third control sense mirrored NFET signal 630, CNTR_SN3, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. The controller 50 may also configure the fifth control mirrored PFET signal 528, CNTR_CP4, the fifth control mirrored NFET signal 564, CNTR_CN4, the fourth control sense mirrored PFET signal 600, CNTR_SP4, and the fourth control sense mirrored NFET signal 632, CNTR_SN4, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. And, the controller 50 may also configure the sixth control mirrored PFET signal 530, CNTR_CP5, the sixth control mirrored NFET signal 566, CNTR_CN5, the fifth control sense mirrored PFET signal 602, CNTR_SP5, and the fifth control sense mirrored

NFET signal 634, CNTR_SN5, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN.

[00743] As an example, the controller 50 may configure the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS(5:1) and the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS(5:1), to substantially track the operation of the I_{COR} source current weight control bus 478, CNTR_CP_BUS(5:0), and the I_{COR} sink current weight control bus 480, CNTR_CN_BUS(5:0) in order to maintain the sense scaling factor, $C_{SENSE_SCALING}$, relationship between the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and the high frequency ripple compensation current 416, I_{COR}.

[00744] Illustratively, in the embodiment of the operational amplifier controlled I_{COR_SENSE} current circuit 472 depicted in Figure 32B, which includes five programmable sense mirrored source current elements and five corresponding programmable sense mirrored sink current elements, the controller 50 may configure the second control mirrored PFET signal 522, CNTR_CP1, the second control mirrored NFET signal 558, CNTR_CN1, the first control sense mirrored PFET signal 594, CNTR_SP1, and the first control sense mirrored NFET signal 626, CNTR_SN1, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. The controller 50 may configure the third control mirrored PFET signal 524, CNTR_CP2, the third control mirrored NFET signal 560, CNTR_CN2, the second control sense mirrored PFET signal 596, CNTR_SP2, and the second control sense mirrored NFET signal 628, CNTR_SN2, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. The controller 50 may also configure the fourth control mirrored PFET signal 526, CNTR_CP3, the fourth control mirrored NFET signal 562, CNTR_CN3, the third control sense mirrored PFET signal 598, CNTR_SP3, and the third control sense mirrored NFET signal 630, CNTR_SN3, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. The controller 50 may also configure the fifth control mirrored PFET signal 528, CNTR_CP4, the

fifth control mirrored NFET signal 564, CNTR_CN4, the fourth control sense mirrored PFET signal 600, CNTR_SP4, and the fourth control sense mirrored NFET signal 632, CNTR_SN4, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN. And, the controller 50 may also configure the sixth control mirrored PFET signal 530, CNTR_CP5, the sixth control mirrored NFET signal 566, CNTR_CN5, the fifth control sense mirrored PFET signal 602, CNTR_SP5, and the fifth control sense mirrored NFET signal 634, CNTR_SN5, to have the same on/off state based on the most significant bits of the programmable control word, CNTRN.

[00745] In addition, the controller 50 is configured to control the I_{COR} source current weight control bus 478, CNTR_CP_BUS(5:0), the I_{COR} sink current weight control bus 480, CNTR_CN_BUS(5:0), the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS(5:1), and the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS(5:1), to maintain the desired scaling between the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and the high frequency ripple compensation current 416, I_{COR}.

[00746] The programmable I_{COR_SENSE} transconductance, Gm_{ICOR_SCALED}, of the operational amplifier controlled I_{COR_SENSE} current circuit 472 is similar to the programmable I_{COR} transconductance, Gm_{ICOR}, of the operational amplifier controlled I_{COR} current circuit 470, except that the programmable I_{COR_SENSE} transconductance, Gm_{ICOR_SCALED}, of the operational amplifier controlled I_{COR_SENSE} current circuit 472, Gm_{ICOR_SCALED}, is reduced by a factor of the sense scaling factor, $C_{SENSE_SCALING}$. In addition, the granularity of the programmability of the programmable I_{COR_SENSE} transconductance, Gm_{ICOR_SCALED}, of the operational amplifier controlled I_{COR_SENSE} current circuit is limited by the five bits of the I_{COR_SENSE} source current weight control bus 482, CNTR_SP_BUS(5:1) and the five bits of the I_{COR_SENSE} sink current weight control bus 484, CNTR_SN_BUS(5:1).

[00747] Continuing with the description of the operational amplifier circuitry 440A depicted in Figure 31A, Figure 32C depicts an example embodiment of the Gm bias circuit and operational amplifier isolation circuit of

the embodiment of the operational amplifier circuitry depicted in Figure 31A. As previously discussed with respect to Figure 27A, the Gm bias circuit 444 may include the bias resistor 452 coupled in series with the bias capacitor 454 between the operational amplifier output 442C (not shown) and ground. As previously described, a Gm bias current, I_{Gm_BIAS}, passes through the bias resistor 452 and the bias capacitor 454 to ground. Accordingly, as previously described, the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442 may be set as a function of the bias resistance, R_0, of the bias resistor 452. Because operation of the Gm bias circuit 444 has been previously described with respect to the operational amplifier circuitry 440A, depicted in Figure 27A, further additional further description is not provided here.

[00748] Figure 32C further depicts the operational amplifier output isolation circuit 446 that includes an operational amplifier output isolation circuit input in communication with the follower NFET 448, $NFET_{FOLLOWER}$, where the source of the follower NFET 448, $NFET_{FOLLOWER}$, is coupled in series to the $I_{BIAS_FOLLOWER}$ current source 450. The drain of the follower NFET 448, $NFET_{FOLLOWER}$, is coupled to the circuit supply voltage, V_{DD}. The gate voltage at the gate of the follower NFET 448, $NFET_{FOLLOWER}$ is equal to the operational amplifier output voltage, V_{AMP}. As previously discussed, with respect to Figure 27A, the gate current, I_{GATE}, that flows into the gate of the follower NFET 448, $NFET_{FOLLOWER}$, approaches zero due to the high gate impedance of the follower NFET 448, $NFET_{FOLLOWER}$. The $I_{BIAS_FOLLOWER}$ current source 450 may include a bias follower NFET 636, $NFET_{BIAS_FOLLOWER}$. The source of the bias follower NFET 636, $NFET_{BIAS_FOLLOWER}$ is coupled to the first node 450A of the $I_{BIAS_FOLLOWER}$ current source 450. The source of the bias follower NFET 636, $NFET_{BIAS_FOLLOWER}$ is coupled to the second node 450B, where the second node 450B is coupled to ground. The gate of the bias follower NFET 636, $NFET_{BIAS_FOLLOWER}$, is coupled to a follower bias voltage, $V_{BIAS_FOLOWER}$, that may be provided by a biasing circuit (not shown) associated with the operational amplifier circuitry 440A. As previously discussed with respect to Figure 27A, the feedback voltage, V_e, is provided at an isolated feedback node 451 created at the junction of the source

of the follower NFET 448, $NFET_{FOLLOWER}$, to the drain of the bias follower NFET 636, $NFET_{BIAS_FOLLOWER}$. The isolated feedback node 451 provides the feedback voltage, V_e, as an output of the operational amplifier output isolation circuit 446. Accordingly, as previously discussed, from a small signal perspective, the follower NFET 448, $NFET_{FOLLOWER}$, provides an isolated feedback node 451 such that, referring back to the open loop ripple compensation assist circuit 414B, depicted in Figure 27A, the feedback current 456 does not impact the Gm bias current, I_{Gm_BIAS}, that is used to set the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442, depicted in Figure 31A.

[00749] In contrast to the open loop ripple compensation assist circuit 414B, depicted in Figure 27A and the operational amplifier circuitry 440A, depicted in Figure 31A, an alternative example of the open loop ripple compensation assist circuit 414, depicted in Figure 27B, is an open loop ripple compensation assist circuit 414C that does not include the operational amplifier output isolation circuit 446. Except for the exclusion of the operational amplifier output isolation circuit 446, the open loop ripple compensation assist circuit 414C is similar in form and function to the open loop ripple compensation assist circuit 414B. Likewise, while controller 50 is not depicted in Figure 27A, it will be understood that as depicted in Figures 23A-D, controller 50 (not shown) may configure the various elements of the open loop ripple compensation assist circuit 414C depicted in Figure 27B.

[00750] As a result, the open loop ripple compensation assist circuit 414C includes a combined filter and gain circuitry 422C having only the operational amplifier circuitry 440B. Thus, unlike the operational amplifier circuitry 440B, depicted in Figure 27A and Figure 31A, the operational amplifier circuitry 440B, depicted in Figure 27B and Figure 31B, does not include the operational amplifier output isolation circuit 446. As a result, the operational amplifier output 442C of the operational amplifier 442 is tied directly to the feedback network 438.

[00751] Referring briefly to the embodiment of the operational amplifier circuitry 440B, depicted in Figure 31B, the operational amplifier circuitry 440B is

similar in form and function to the operational amplifier circuitry 440A, depicted in Figure 31A, except, the operational amplifier output isolation circuit 446, depicted in Figure 32C, is eliminated. Thus, as depicted in Figure 32D, the Gm bias circuit 444 is not isolated from the feedback network 438, depicted in Figure 27B.

[00752] Accordingly, the operational amplifier output 442C may be configured to provide the operational amplifier output current, I_{AMP}, to provide the Gm bias current, I_{Gm_BIAS}, and the feedback current 456, $I_{FEEDBACK}$. In order to obtain ripple rejection response characteristics that are similar to the ripple rejection response characteristics obtained using the embodiment of the open loop ripple compensation assist circuit 414B , depicted in Figure 27A, the ratio of the Gm bias current, I_{Gm_BIAS}, to the feedback current 456, $I_{FEEDBACK}$, must be controlled such that the feedback current 456, $I_{FEEDBACK}$, is at least 20dB lower in amplitude than the Gm bias current, I_{Gm_BIAS}, passing through the Gm bias circuit 444. In other words, to minimize the non-isolative effect of providing the feedback current 456, $I_{FEEDBACK}$, directly from the operational amplifier output 442C, it is desirable for the ratio of $I_{Gm_BIAS} / I_{FEEDBACK} \geq 10$.

[00753] The series impedance of the bias resistance, R_0, of the bias resistor 452, and the bias capacitance, C_0, of the bias capacitor 454, form a transconductance setting impedance, Z_{Gm}. The parallel impedance of the feedback resistance, R_2, of the feedback resistor 462 and the feedback capacitance, C_2, of the feedback capacitor 464 in combination with the series impedance of the filter resistance, R_1, of the filter resistor 458 and the filter capacitance, C_1, of the filter capacitor 460 form a feedback current setting impedance, $Z_{FEEDBACK}$.

[00754] To ensure the ratio of $I_{Gm_BIAS} / I_{FEEDBACK} \geq 10$, the fixed valued resistances and capacitances and the programmable valued resistances and capacitances of the respective bias resistor 452, feedback capacitor 464, filter resistor 458, filter capacitor 460, may be configured such that $Z_{Gm}, \geq 10 \times Z_{FEEDBACK}$.

[00755] Thus, in some embodiments of the open loop ripple compensation assist circuit 414B, the controller 50 may configure the filter resistor 458 to have

a resistance value substantially equal to the filter resistance, R_1, the feedback resistor 462 to have a resistance value substantially equal to the feedback resistance, R_2, the filter capacitor 460 to have a capacitance value substantially equal to the filter capacitance, C_1, and the feedback capacitor 464 to have a capacitance value substantially equal to the feedback capacitance, C_2, such that relative to the series impedance formed by the bias resistance, R_0, of the bias resistor 452, and the bias capacitance, C_0, of the bias capacitor 454, result in the feedback current 456, $I_{FEEDBACK}$, passing through the parallel impedance of the feedback resistor 462 and feedback capacitor 464 to be around $1/10^{th}$ the magnitude of the Gm bias current, I_{Gm_BIAS}, passing through the bias resistor 452 and the bias capacitor 454 in the range of frequencies near or within operational bandwidth of the linear radio frequency power amplifier 22. In other words, in some embodiments of the open loop ripple compensation assist circuit 414C, the impedances of the filter network 436 and the feedback network 438 are configured such that the ratio of the transconductance setting impedance, Z_{Gm}, to the feedback current setting impedance, $Z_{FEEDBACK}$, minimizes the impact of the feedback current 456, $I_{FEEDBACK}$, on the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442 set based on the bias resistance, R_0, of the bias resistor 452. Illustratively, for the ratio of Z_{Gm} : $Z_{FEEDBACK}$ equal to or greater than 1:10, the magnitude of the feedback current 456, $I_{FEEDBACK}$, relative to the Gm bias current, I_{Gm_BIAS}, may minimally affect the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442. In other embodiments, the ratio of Z_{Gm} : $Z_{FEEDBACK}$ may be equal to or greater than 1:8 without substantially impacting the ability to set the operational amplifier transconductance, Gm_{OP_AMP}, of the operational amplifier 442 based on the bias resistance, R_0, of the bias resistor 452.

[00756] However, in some embodiments of the open loop ripple compensation assist circuit 414C, depicted in Figure 27B, the relative impedance relationship between the transconductance setting impedance, Z_{Gm}, and the feedback current setting impedance, $Z_{FEEDBACK}$, may result in reduced ripple rejection response characteristics of the pseudo-envelope follower power management systems.

[00757] By way of example, and not by limitation, Figure 28A depicts the ripple rejection response characteristics of an embodiment of the pseudo-envelope follower power management systems similar to the pseudo-envelope follower power management systems depicted in Figures 23A-D, where the open loop ripple compensation assist circuit 414, depicted in Figures 23A-D, is similar to the open loop ripple compensation assist circuit 414B, depicted in Figure 27A. For the sake of illustration, and not by way of limitation, the bias resistance, R_0, of the bias resistor 452 is substantially equal to 500Ω, and the bias capacitance, C_0, of the bias capacitor 454 is substantially equal to 100pF. For the sake of simplicity, and not by way of limitation, the ripple rejection response curves are based on configuring the resistance values of the filter resistor 458 and the feedback resistor 462 such that $R_1 = R_2$. In addition, for the sake of simplicity, and not by way of limitation, the ripple rejection response curves are based on configuring the capacitance values of the filter capacitor 460 and the feedback capacitor 464 such that $C_1 = C_2$.

[00758] Figure 28A depicts a first ripple rejection response curve labeled "FIRST RESPONSE (1pF)," a second ripple rejection response curve labeled "SECOND RESPONSE (3pF)," and a third ripple rejection response curve labeled "THIRD RESPONSE (5pF)" for a pseudo-envelope follower power management system similar to the pseudo-envelope follower power management systems depicted in Figures 23A-D, where the open loop ripple compensation assist circuit 414, depicted in Figures 23A-D, is similar to the open loop ripple compensation assist circuit 414B, depicted in Figure 27A. The first ripple rejection response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 1pF, ($C_1 = C_2 = 1$pF), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 26.5 KΩ, ($R_1 = R_2 = 26.5$ KΩ). Referring back to the mapping between the elements of equation (7) and equation (9), for $R_1 = R_2 = 26.5$ KΩ and $C_1 = C_2 = 1$pF, the open loop ripple compensation assist circuit 414B provides a high pass filtering response, where the first corner frequency, f_{c1}, and the second corner frequency, f_{C2}, are approximately 6.003MHz. The second ripple rejection

response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 3pF, ($C_1 = C_2 = 3pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 26.5 KΩ, ($R_1 = R_2 = 8.3$ KΩ). Referring back to the mapping between the elements of equation (7) and equation (9), for $R_1 = R_2 = 8.8$ KΩ and $C_1 = C_2 = 3pF$, the open loop ripple compensation assist circuit 414B provides a high pass filtering response, where the first corner frequency, f_{c1}, and the second corner frequency, f_{C2}, are approximately 6.026 MHz. The third ripple rejection response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 5pF, ($C_1 = C_2 = 5pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 5.3 KΩ, ($R_1 = R_2 = 8.3$ KΩ). Referring back to the mapping between the elements of equation (7) and equation (9), for $R_1 = R_2 = 5.3$ KΩ and $C_1 = C_2 = 5pF$, the open loop ripple compensation assist circuit 414B provides a high pass filtering response, where the first corner frequency, f_{c1}, and the second corner frequency, f_{C2}, are approximately 6.003 MHz. The first ripple rejection response curve, the second ripple rejection response curve, and the third ripple rejection response curve are substantially similar with respect to placement, width, and depth of the notch in the ripple rejection response of the above-described pseudo-envelope follower power management systems.

[00759] As depicted in Figure 28A, the ripple rejection response curves for the embodiments of the pseudo-envelope follower power management systems similar to the pseudo-envelope follower power management systems, depicted in Figures 23A-D, that include the open loop ripple compensation assist circuit 414B, depicted in Figure 27A, which includes the operational amplifier output isolation circuit 446, are substantially insensitive to the values of the filter resistance, R_1, the feedback resistance, R_2, the filter capacitance, C_1, and the feedback capacitance, C_2. In addition, the depth of the notch in the first ripple rejection response curve, the second ripple rejection response curve, and the third ripple rejection response curve are substantially similar. Thus, advantageously, the values of the filter resistance, R_1, the feedback resistance,

R_2, the filter capacitance, C_1, and the feedback capacitance, C_2.filter resistance, R_1, the feedback resistance, R_2, the filter capacitance, C_1, the feedback capacitance, C_2, of the open loop ripple compensation assist circuit 414B may be selected such that parasitic capacitances and resistances present in the layout and circuitry of the example pseudo-envelope follower power management system minimally impact the location, width, and depth of the notch.

[00760] As another non-limiting example, Figure 28B depicts ripple rejection response curves for an embodiment of the pseudo-envelope follower power management systems similar to the pseudo-envelope follower power management systems depicted in Figures 23A-D, where the open loop ripple compensation assist circuit 414, depicted in Figures 23A-D, is similar to the open loop ripple compensation assist circuit 414C, depicted in Figure 27B. In addition, Figure 28 also depicts a reference ripple rejection curve, labeled ""REFERENCE RESPONSE," which is the reference rejection response of the open loop ripple compensation assist circuit 414B, depicted in Figure 27A, for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 5pF, ($C_1 = C_2 = 5pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 5.3 KΩ, ($R_1 = R_2 = 8.3$ KΩ).

[00761] Figure 28B depicts a ripple rejection response curve, labeled "REFERENCE RESPONSE," that corresponds to, for the embodiment of the pseudo-envelope follower power management systems, depicted in Figure 27A, where the capacitance values of the filter capacitor 460 and the feedback capacitor 464 such that $C_1 = C_2 = 5pF$ and the resistance values of the filter resistor 458 and the feedback resistor 462 are substantially set such that $R_1 = R_2 = 5.3K\Omega$. Figure 28A further depicts a first ripple rejection response curve labeled "FIRST RESPONSE (1pF)," a second ripple rejection response curve labeled "SECOND RESPONSE (2pF)," a third ripple rejection response curve labeled "THIRD RESPONSE (3pF)," a fourth ripple rejection response curve labeled "THIRD RESPONSE (4pF)" and a fifth ripple rejection response curve labeled "THIRD RESPONSE (5pF)" for a pseudo-envelope follower power management system similar to the pseudo-envelope follower power

management systems depicted in Figures 23A-D, where the open loop ripple compensation assist circuit 414, depicted in Figures 23A-D, is similar to the open loop ripple compensation assist circuit 414C, depicted in Figure 27B.

[00762] The first ripple rejection response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 1pF, ($C_1 = C_2 = 1pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 26.5 KΩ, ($R_1 = R_2 = 26.5$ KΩ).

[00763] The second ripple rejection response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 2pF, ($C_1 = C_2 = 2pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 13.25 KΩ, ($R_1 = R_2 = 13.25$ KΩ).

[00764] The third ripple rejection response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 3pF, ($C_1 = C_2 = 3pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 8.8 KΩ, ($R_1 = R_2 = 8.8$ KΩ).

[00765] The fourth ripple rejection response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 3pF, ($C_1 = C_2 = 4pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 6.6 KΩ, ($R_1 = R_2 = 6.6$ KΩ).

[00766] The fifth ripple rejection response curve is for the case where the filter capacitance, C_1 and the feedback capacitance, C_2 are substantially equal to 5pF, ($C_1 = C_2 = 5pF$), and the filter resistance R_1 and the feedback resistance, R_2 are substantially equal to 5.3 KΩ, ($R_1 = R_2 = 5.3$ KΩ).

[00767] In contrast to the ripple rejection response curves depicted in Figure 28A, ripple rejection response curves, depicted in Figure 28B, vary substantially based on the values of the filter resistance, R_1, the feedback resistance, R_2, the filter capacitance, C_1, the feedback capacitance, C_2. For example, the notch depth and location of the first ripple rejection response curve labeled "FIRST RESPONSE (1pF), depicted in Figure 28B, is substantially different than the location, width, and depth of the notch of the first ripple rejection response curve labeled "FIFTH RESPONSE (5pF), depicted in

Figure 28B. In addition, advantageously, the typical depth of the notch in the first ripple rejection response curve, the second ripple rejection response curve labeled, the third ripple rejection response curve, the fourth ripple rejection response curve, and the fifth ripple rejection response curve, depicted in Figure 28B, is deeper than the "Reference Response," which represents the ripple rejection response curves obtained with the open loop ripple compensation assist circuit 414B.

[00768] Figure 29A depicts an embodiment of the programmable delay circuitry 432, depicted in Figure 24, as the programmable delay circuitry 432A, where the embodiment of the programmable delay circuitry 432A includes both fixed delay circuitry 638 and variable delay circuitry 640A. The fixed delay circuitry 638 includes an input stage 642 including an input node 642A, a first PFET 644, $PFET_1$, a first NFET 646, $NFET_1$, a first fixed current source 648, a second fixed current source 650, and a first fixed delay capacitor 652. The first fixed delay capacitor 652 has a first delay capacitance, C_{DELAY1}. The input node 642A of the input stage 642 is configured to receive an input voltage, V_{IN}, having a digital logic level signal, where the digital logic level signal is to be delayed by the programmable delay circuitry 432A. The input stage 642 is formed by coupling the gate of the first PFET 644, $PFET_1$, and the gate of the first NFET 646, $NFET_1$, to the input node 642A. The first fixed current source 648 is coupled between the circuit supply voltage, V_{DD}, and the source of the first PFET 644, $PFET_1$. The second fixed current source 650 is coupled between the source of the first NFET 646, $NFET_1$, and ground. The first fixed delay capacitor 652 is coupled between ground and the drain of the first PFET 644, $PFET_1$, and the drain of the first NFET 646. During normal operation, when the input voltage, V_{IN}, at the input node 642A is sufficiently low such that the input voltage, V_{IN} is substantially equal to a logic low threshold voltage, the first PFET 644, $PFET_1$, is configured to be in a conducting state and the first NFET 646, $NFET_1$, is configured to be in a non-conducting state. When the first PFET 644, $PFET_1$, is turned on, the first fixed current source 648 sources a fixed bias current, I_{BIAS}, to the first fixed delay capacitor 652 with a first fixed capacitor

current, I_{C1}. Assuming that most of the first fixed bias current, I_{BIAS}, from the first fixed current source 648 is used to charge the first fixed delay capacitor 652, the first fixed capacitor current, I_{C1}, is substantially equal to the fixed bias current, I_{BIAS}, provided from the first fixed current source 648 through first PFET 644, $PFET_1$. As the first fixed delay capacitor 652 is charged, the first delay voltage, V_{D1}, continues to increase and eventually rises above a voltage level that is greater than a logic high threshold voltage that may trigger an action by the variable delay circuitry 640A.

[00769] Otherwise, when the input voltage, V_{IN}, at the input node 642A is sufficiently high such that the input voltage, V_{IN} is substantially equal to a logic high threshold voltage, the first PFET 644, $PFET_1$, is configured to be in a non-conducting state and the first NFET 646, $NFET_1$, is configured to be in a conducting state. When the first NFET 646, $NFET_1$, is turned on, the second fixed current source 650 sinks a fixed bias current, I_{BIAS}, from the first fixed delay capacitor 652 to generate the first fixed capacitor current, I_{C1}, of opposite magnitude than when the first fixed delay capacitor 652 is being charged by the first fixed current source 648. Assuming that most of the fixed bias current, I_{BIAS}, sunk through the first NFET 646, $NFET_1$ by the second fixed current source 650 is used to discharge the first fixed delay capacitor 652, the magnitude of the first fixed capacitor current, I_{C1}, is substantially equal to the magnitude of the fixed bias current, I_{BIAS}, sunk by the second fixed current source 650 through first NFET 646, $NFET_1$. As the first fixed delay capacitor 652 is discharged, the first delay voltage, V_{D1}, continues to decreases and eventually falls below a voltage level that is less than a logic low threshold voltage that may trigger an action by the variable delay circuitry 640A.

[00770] Because the first fixed current source 648 and the second fixed current source 650 each source and sink, respectively, a current equal to the fixed bias current, I_{BIAS}, the first fixed delay capacitor 652 is charged and discharged at the same rate. The first fixed delay time associated with the fixed delay circuitry 638 is due to the generation of the first delay voltage, V_{D1}. Because the current sourced by the first fixed current source 648 and sunk by the second fixed

current source 650 are substantially equal, the rise time and fall time of the first delay voltage, V_{D1}, are substantially equal. Effectively, the first fixed delay time is due to the time required to propagate the digital logic state represented by the input voltage, V_{IN}, through the fixed delay circuitry 638 and provide first delay voltage, V_{D1}, that represents a digital logic state to an input stage 654 of the variable delay circuitry 640A.

[00771] The variable delay circuitry 640A includes the input stage 654 having an input node 654A coupled to the drain of the first PFET 644, $PFET_1$, the drain of the first NFET 646, $NFET_1$, and the first fixed delay capacitor 652. The variable delay circuitry 640A further includes a second PFET 656, $PFET_2$, a second NFET 658, $NFET_2$, a first variable current source 660, a second variable current source 662, and a second fixed delay capacitor 664. The second fixed delay capacitor 664 has a second delay capacitance, C_{DELAY2}.

[00772] The input stage 654 of the variable delay circuitry 640A is formed by coupling the gate of the second PFET 656, $PFET_2$, and the gate of the second NFET 658, $NFET_2$, to the input node 654A. The variable delay circuitry 640A is further formed by coupling the first variable current source 660 between the circuit supply voltage, V_{DD}, and the source of the second PFET 656, $PFET_2$, such that the first variable current source 660 may provide a variable bias current, I_{BIAS_VAR}, to the source of the second PFET 656, $PFET_2$ when the second PFET 656, $PFET_2$, is in a conducting state. In addition, the second variable current source 662 is coupled between the source of the second NFET 658, $NFET_2$, and ground such that the second variable current source 662 may sink a variable bias current, I_{BIAS_VAR}, from the source of the second NFET 658, $NFET_2$, when the second NFET 658, $NFET_2$, is in a conducting state. The second fixed delay capacitor 664 is coupled between ground and the drain of the second PFET 656, $PFET_2$, and the drain of the second NFET 658.

[00773] In addition, the variable delay circuitry 640A further includes an output buffer stage 666 that includes a third PFET 668, $PFET_3$ operablely coupled to a third NFET 670, $NFET_3$ to form an input node 666A. The output buffer stage 666 includes an input node 666A formed by coupling the gate of the third PFET 668,

$PFET_3$, to the gate of the third NFET 670, $NFET_3$. The source of the third PFET 668, $PFET_3$, is couple to the circuit supply voltage, V_{DD}. The source of the third NFET 670, $NFET_3$, is coupled to ground. The output buffer stage 666 further includes an output buffer stage output 672 that corresponds to the output of the programmable delay circuitry 432A. The output buffer stage output 672 may be formed by coupling the drain of the third PFET 668, $PFET_3$, to the drain of the third NFET 670, $NFET_3$. The output buffer stage 666 is configured to generate an output voltage, V_{OUT}, at the output buffer stage output 672. Generally, the output voltage, V_{OUT}, generated by the output buffer stage 666 at the output buffer stage output 672 will represent either a digital logic high state or a digital logic low state. For example, when the output voltage, V_{OUT}, is substantially equal to the circuit supply voltage, V_{DD}, the output voltage, V_{OUT}, represents a digital logic high state. When the output voltage, V_{OUT}, is substantially equal to the ground voltage, the output voltage, V_{OUT}, represents a digital logic low state.

[00774] During operation of the variable delay circuitry 640A, a second delay voltage, V_{D2}, increases as the second fixed delay capacitor 664 is charged and decreases as the second fixed delay capacitor 664 is discharged. When the second delay voltage, V_{D2}, is sufficiently low such that the second delay voltage, V_{D2}, is substantially equal to or below a logic low threshold voltage, the third PFET 668, $PFET_3$, is configured to be in a conducting state and the third NFET 670, $NFET_3$ is configured to be in a non-conducting state. In this case, when the third PFET 668, $PFET_3$, is turned on, the output buffer stage output 672 is coupled to the circuit supply voltage, V_{DD}, via the third PFET 668, $PFET_3$. As a result, the output voltage, V_{OUT}, at the output buffer stage output 672 is substantially equal to the circuit supply voltage, V_{DD}, and the output voltage, V_{OUT}, represents a digital logic high state.

[00775] However, when the second delay voltage, V_{D2}, is sufficiently high such that the second delay voltage, V_{D2}, is substantially equal to or above a logic high threshold voltage, the third PFET 668, $PFET_3$, is configured to be in a non-conducting state and the third NFET 670, $NFET_3$ is configured to be in a

conducting state. In this case, the third NFET 670, $NFET_3$, is turned on and the output buffer stage output 672 is coupled to ground via the third NFET 670, $NFET_3$. As a result, the output voltage, V_{OUT}, at the output buffer stage output 672 is substantially equal to the ground voltage, and the output voltage, V_{OUT}, represents a digital logic low state.

[00776] During normal operation, when the first delay voltage, V_{D1}, at the input node 654A is sufficiently low to be equal to or lower than a logic low threshold voltage, the second PFET 656, $PFET_2$, is configured to be in a conducting state and the second NFET 658, $NFET_2$, is configured to be in a non-conducting state. Accordingly, when the second PFET 656, $PFET_2$, is turned on, the first variable current source 660 sources the variable bias current, I_{BIAS_VAR}, through the second PFET 656, $PFET_2$, to charge the second fixed delay capacitor 664 with a second fixed capacitor current, I_{C2}. Assuming that most of the variable bias current, I_{BIAS_VAR}, from the first variable current source 660 is used to charge the second fixed delay capacitor 664, the second fixed capacitor current, I_{C2} is substantially equal to the variable bias current, I_{BIAS_VAR}, provided by the first variable current source 660. As the second fixed delay capacitor 664 is charged by the variable bias current, I_{BIAS_VAR}, the magnitude of the second delay voltage, V_{D2}, continues to increase and eventually rises above a voltage level that is greater than the logic high threshold voltage that may trigger an action by the output buffer stage 666. For example, once the second delay voltage, V_{D2}, reaches or exceeds the logic high threshold voltage, the output buffer stage 666 will trigger so as to generate an output voltage, V_{OUT} that represents a digital logic low state.

[00777] Otherwise, during normal operation, when the first delay voltage, V_{D1}, at the input node 654A is sufficiently high to be equal to exceed a logic high threshold voltage, the second PFET 656, $PFET_2$, is configured to be in a non-conducting state and the second NFET 658, $NFET_2$, is configured to be in a conducting state. Accordingly, when the second NFET 658, $NFET_2$, is turned on, the second variable current source 662 sinks the variable bias current, I_{BIAS_VAR}, through the second NFET 658, $NFET_2$, to discharge the second fixed delay

capacitor 664 with the second fixed capacitor current, I_{C2}, by removing charge from the second fixed delay capacitor 664. Assuming that most of the variable bias current, I_{BIAS_VAR}, sunk by the second variable current source 662 is used to discharge the second fixed delay capacitor 664, the magnitude of the second fixed capacitor current, I_{C2}, that removes charge from the second fixed delay capacitor 664 is substantially equal to the variable bias current, I_{BIAS_VAR}, sunk by second variable current source 662. As the second fixed delay capacitor 664 is discharged by the variable bias current, I_{BIAS_VAR}, the magnitude of the second delay voltage, V_{D2}, continues to decrease or eventually fall below a voltage level that is less than the logic low threshold voltage that may trigger an action by the output buffer stage 666. For example, once the second delay voltage, V_{D2}, reaches or falls below the logic low threshold voltage, the output buffer stage 666 will trigger, and the output buffer stage 666 will generate an output voltage, V_{OUT}, that represents a digital logic high state.

[00778] The variable delay time provided by the variable delay circuitry 640A is created by the time period required to charge and discharge the second fixed delay capacitor 664 with the variable bias current, I_{BIAS_VAR}, where the variable bias current, I_{BIAS_VAR}, varies in magnitude. As depicted in Figure 29A, the first variable current source 660 and the second variable current source 662 are each configured to respectively source and sink currents that are both equal to the variable bias current, I_{BIAS_VAR}. As a result, the variable delay time of the variable delay circuitry 640A is symmetrically divided into equal parts. However, in some embodiments, the first variable current source 660 and the second variable current source 662 may source and sink different magnitudes of current. Depending upon the magnitude of the variable bias current, I_{BIAS_VAR}, the time to charge and discharge the second fixed delay capacitor 664 such that the magnitude of the second delay voltage, V_{D2}, changes logic state represented by the output voltage, V_{OUT}, at output buffer stage output 672 may change.

[00779] Furthermore, as depicted in Figure 24, the controller 50 may be configured to control the programmable delay circuitry 432. Accordingly, although not depicted in Figure 29A, in some embodiments of the programmable

delay circuitry 432A, the controller 50 may be further configured to control the first variable current source 660 and the second variable current source 662 to set the magnitude of the variable bias current, I_{BIAS_VAR}, and thereby the variable delay time provided by the variable delay circuitry 640A.

[00780] Figure 29B depicts the programmable delay circuitry 432B, which is another embodiment of the programmable delay circuitry 432, depicted in Figure 24. The embodiment of the programmable delay circuitry 432B, depicted in Figure 29B, is similar to the programmable delay circuitry 432A, depicted in Figure 29A, except the embodiment of the variable delay circuitry 640A, depicted in Figure 29A, is replaced by the variable delay circuitry 640B, depicted in Figure 29B.

[00781] As depicted in Figure 29B, the programmable delay circuitry 432B is similar to the programmable delay circuitry 432A, depicted in Figure 29A, except the first variable current source 660, the second variable current source 662, and the second fixed delay capacitor 664 are replaced, respectively, with a third fixed current source 674, a fourth fixed current source 678, and a variable delay capacitor 680. In addition, for the sake of clarity, and not by way of limitation, the voltage across the variable delay capacitor 680 is the third voltage, V_{D3}. The variable delay capacitor 680 having a variable delay capacitance C_{DELAY_VAR}, where the capacitance value of the variable delay capacitance C_{DELAY_VAR}, may be programmatically configured.

[00782] As discussed relative to the programmable delay circuitry 432A, the operational parameters of the programmable delay circuitry 432B may be configured by the controller 50, (not depicted in Figure 29B), which is depicted in Figure 24. For example, the variable delay capacitor 680 may be a capacitor array or a varactor under the control of the controller 50. Accordingly, as will be described, the controller 50 may be configured to increase the variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 680 in order to increase the delay time provided by the programmable delay circuitry 432B. Likewise, the controller 50 may be configured to decrease the variable delay capacitance,

C_{DELAY_VAR}, of the variable delay capacitor 680 to decrease the delay time provided by the programmable delay circuitry 432B.

[00783] Continuing with the description of the programmable delay circuitry 432B, depicted in Figure 29B, the function and operation of the fixed delay circuitry 638 of the programmable delay circuitry 432B, and thereby the fixed delay time provided by the fixed delay circuitry 638, are substantially the same in the programmable delay circuitry 432B, depicted in Figure 29B. Accordingly, description of the fixed delay circuitry 638 is omitted.

[00784] As discussed above, the variable delay circuitry 640B is similar to the variable delay circuitry 640A except that the variable delay circuitry 640B replaces the first variable current source 660, the second variable current source 662, and the second fixed delay capacitor 664 of the variable delay circuitry 640A, with the third fixed current source 674, the fourth fixed current source 678, and the variable delay capacitor 680, respectively. Thus, the variable delay circuitry 640B includes the input stage 654 having the input node 654A, the second PFET 656, $PFET_2$, the second NFET 658, $NFET_2$, the third fixed current source 674, the fourth fixed current source 678, and the variable delay capacitor 680 having a variable delay capacitance, C_{DELAY_VAR}, where the controller 50 (not shown) may be configured to change the capacitance value of the variable delay capacitance, C_{DELAY_VAR}.

[00785] Similar to the variable delay circuitry 640A, the variable delay circuitry 640B also includes the output buffer stage 666 that includes the third PFET 668, $PFET_3$, and the third NFET 670, $NFET_3$. The output buffer stage 666 includes the input node 666A formed by coupling the gate of the third PFET 668, $PFET_3$, to the gate of the third NFET 670, $NFET_3$. The source of the third PFET 668, $PFET_3$, is coupled to the circuit supply voltage, V_{DD}. The source of the third NFET 670, $NFET_3$, is coupled to ground. The output buffer stage output 672 of the output buffer stage 666, which is also the output of the programmable delay circuitry 432B, is formed by coupling the drain of the third PFET 668, $PFET_3$, to the drain of the third NFET 670, $NFET_3$. The output buffer stage 666 is configured to generate an output voltage, V_{OUT}, at the output buffer

stage output 672. For example, as will be discussed, a third delay voltage, V_{D3}, across the variable delay capacitor 680 increases and decreases at a rate that depends on the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 680 and the magnitude of a variable capacitance current, I_{C_VAR}, that charges and discharges the variable delay capacitor 680. When the third delay voltage, V_{D3}, across the variable delay capacitor 680 is sufficiently low such that the third delay voltage, V_{D3} is substantially equal to a logic low threshold voltage, the third PFET 668, $PFET_3$, is configured to be in a conducting state and the third NFET 670, $NFET_3$, is configured to be in a non-conducting state. In this case, when the third PFET 668, $PFET_3$, is turned on, the output buffer stage output 672 is coupled to the circuit supply voltage, V_{DD}. As a result, the output voltage, V_{OUT}, at the output buffer stage output 672 is substantially equal to the circuit supply voltage, V_{DD}, when the third PFET 668, $PFET_3$, is in the conducting state. However, when the third delay voltage, V_{D3}, across the variable delay capacitor 680 is sufficiently high such that the third delay voltage, V_{D3} is substantially equal to a logic high threshold voltage, the third NFET 670, $NFET_3$, is configured to be in a conducting state and the third PFET 668, $PFET_3$, is configured to be in a non-conducting state. In this case, when the third NFET 670, $NFET_3$, is turned on, the output buffer stage output 672 is coupled to ground. As a result, the output voltage, V_{OUT}, at the output buffer stage output 672 is substantially equal to the ground voltage when the third NFET 670, $NFET_3$, is turned on. In this way, the output voltage, V_{OUT}, at the output buffer stage output 672 toggles between a digital logic high state and a logic log state.

[00786] Continuing with the description of the variable delay circuitry 640B, depicted in Figure 29B, the variable delay circuitry 640B includes an input stage 654 having an input node 654A configured to receive the signal generated by the charging and discharging of the first fixed delay capacitor 652, where the first fixed delay capacitor 652 has a capacitance value substantially equal to the first fixed delay capacitance, C_{DELAY1}. The voltage generated across the first fixed delay capacitor 652 is substantially equal to the first delay voltage, V_{D1}.

The input stage 654 is formed by coupling the gate of the second PFET 656, $PFET_2$, and the gate of the second NFET 658, $NFET_2$, to the input node 654A. The third fixed current source 674 is coupled between the circuit supply voltage, V_{DD}, and the source of the second PFET 656, $PFET_2$. The fourth fixed current source 678 is coupled between the source of the second NFET 658, $NFET_2$, and ground. The variable delay capacitor 680 is coupled between ground and the drain of the second PFET 656, $PFET_2$, and the drain of the second NFET 658.

[00787] During normal operation, when the first delay voltage, V_{D1}, at the input node 654A is sufficiently low, the second PFET 656, $PFET_2$, is configured to be in a conducting state. At the same time, when the first delay voltage, V_{D1}, at the input node 654A is sufficiently low to turn on the second PFET 656, $PFET_2$, the second NFET 658, $NFET_2$, is configured to be in a non-conducting state. When the second PFET 656, $PFET_2$, is turned on, the third fixed current source 674 sources a second fixed bias current, I_{BIAS2}, to charge the variable delay capacitor 680. The second fixed bias current, I_{BIAS2}, charges the variable delay capacitor 680 with a variable capacitance current, I_{C_VAR}. The rate of change in the third delay voltage, V_{D3}, across the variable delay capacitor 680 depends upon the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 680 and the magnitude of the variable capacitance current, I_{C_VAR}. Assuming that most of the second fixed bias current, I_{BIAS2}, from the third fixed current source 674 is used to charge the variable delay capacitor 680, the variable capacitance current, I_{C_VAR}, is substantially equal to the second fixed bias current, I_{BIAS2}. As the variable delay capacitor 680 is charged by the second fixed bias current, I_{BIAS2}, the magnitude of the third delay voltage, V_{D3}, increases. As described above, after the third delay voltage, V_{D3}, increases to a logic high threshold voltage, the third PFET 668, $PFET_3$, is turned off and the third NFET 670, $NFET_3$, is turned on, which changes the output voltage, V_{OUT}, at the output buffer stage output 672 to be substantially equal to ground.

[00788] Otherwise, when the first delay voltage, V_{D1}, at the input node 654A is sufficiently high, the second NFET 658, $NFET_2$, is configured to be in a

conducting state and the fourth fixed current source 678 is permitted to sink a second fixed bias current, I_{BIAS2}, in order to discharges the variable delay capacitor 680. At the same time, when the first delay voltage, V_{D1}, at the input node 654A is sufficiently low to turn on the second NFET 658, $NFET_2$, the second PFET 656, $PFET_2$, is configured to be in a non-conducting state. When the second NFET 658, $NFET_2$, is turned on, the fourth fixed current source 678 sinks the second fixed bias current, I_{BIAS2}, to discharge the variable delay capacitor 680 with a current substantially equal to I_{C_VAR}. The rate of change in the third delay voltage, V_{D3}, across the variable delay capacitor 680 depends upon the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 680 and the magnitude of the variable capacitance current, I_{C_VAR}. Assuming that most of the second fixed bias current, I_{BIAS2}, from the fourth fixed current source 678 is used to discharge the variable delay capacitor 680, the variable capacitance current, I_{C_VAR}, is substantially equal to the second fixed bias current, I_{BIAS2}. As the variable delay capacitor 680 is discharged by the second fixed bias current, I_{BIAS2}, the magnitude of the third delay voltage, V_{D3}, decreases. As described above, after the third delay voltage, V_{D3}, decreases to a logic low threshold voltage, the third NFET 670, $NFET_3$, is turned off and the third PFET 668, $PFET_3$, is turned on, which changes the output voltage, V_{OUT}, at the output buffer stage output 672 to be substantially equal to the circuit supply voltage, V_{DD}.

[00789] The variable delay time provided by the variable delay circuitry 640B is created by the time period required to charge and discharge the variable delay capacitor 680, which depends upon the capacitance value of the variable capacitance, C_{DELAY_VAR}, and the magnitude of the second fixed bias current, I_{BIAS2}. Because the variable delay capacitor 680 is either charged or discharged using a current substantially equal to the second fixed bias current, I_{BiAS2}, either sourced by the third fixed current source 674 or sunk by the fourth fixed current source 678, the variable time period required for the third delay voltage, V_{D3}, to increase to the logic high threshold voltage or decrease to the logic high threshold voltage used to trigger the operation of the operation of the output

buffer stage 666 is dependent upon the variable capacitance, C_{DELAY_VAR} of the variable delay capacitor 680.

[00790] As previously discussed with respect to Figure 24, although not depicted in Figure 29B, the controller 50 may be configured to control the programmable delay circuitry 432B. Accordingly, although not depicted in Figure 29B, in some embodiments of the programmable delay circuitry 432B, the controller 50 may be further configured to control the variable capacitance, C_{DELAY_VAR} of the variable delay capacitor 680 in order to change the delay time provided by the programmable delay circuitry 432B. Assuming that the third fixed current source 674 and the fourth fixed current source 678 respectively source and sink the second fixed bias current, I_{BIAS2}, where the second fixed bias current, I_{BIAS2}, is constant, the variable delay capacitor current, I_{C_VAR}, will likewise be constant. Consequently, the variable delay time provided by the variable delay circuitry 640B when charging the variable delay capacitor 680 is substantially equal to the variable delay time provided by the variable delay circuitry 640B when discharging the variable delay capacitor 680. In alternative embodiments of the variable delay circuitry 640B, the third fixed current source 674 and the fourth fixed current source 678 could be configured to source and sink different magnitudes of current. In this case, the variable delay time of the variable delay circuitry 640B would have a charging period and a discharging period, where the charging period would not equal the discharging period.

[00791] Figure 30A depicts a programmable delay circuitry 432C, which is another embodiment of the programmable delay circuitry 432, depicted in Figure 24. Although the controller 50 is not depicted in Figure 30A, similar to the programmable delay circuitry 432, depicted in Figure 24, it will be understood that the controller 50, depicted in Figures 23A-D, may be configured to control, configure, align, or change the parameter values and functions of the various circuits and elements to be described as being part of or related to the embodiment of the programmable delay circuitry 432C, depicted in Figure 30A.

[00792] The programmable delay circuitry 432C, depicted in Figure 30, is configured to delay a single digital logic level signal. It will be understood that

embodiments of the programmable delay circuitry 432, depicted in Figure 24, are configured to delay multiple digital logic level signals may include multiple embodiments of the programmable delay circuitry 432C arranged in parallel to provide a delay signal path for each of the multiple digital logic level signals to be delayed.

[00793] In addition, total delay time provided by the programmable delay circuitry 432C may include a fixed delay time and a variable delay time, where the variable delay time may be configured based on the programmable delay parameter(s), as discussed above. In addition, the fixed delay time may be sub-divided and distributed between the input buffer circuit 682 and the variable delay circuitry 684.

[00794] As depicted in Figure 30A, the programmable delay circuitry 432C includes an input buffer circuit 682, a variable delay circuitry 684, a voltage divider circuit 686, and a bias current and mirror circuit 688. The input buffer circuit 682 may include a first input buffer circuit 690 having a first input buffer input 690A configured to receive an input voltage, V_{IN}, where the input voltage, V_{IN}, is a digital logic level signal. The digital logic signal may have either a digital logic high state or a digital logic low state. The digital logic signal may have either a digital logic high state or a digital logic low state. The first input buffer circuit 690 may include a first PFET 692, $PFET_1$, and a first NFET 694, $NFET_1$. The gate of the first PFET 692, $PFET_1$, and the gate of the first NFET 694, $NFET_1$, may be coupled to form the first input buffer input 690A of the first input buffer circuit 690. The source of the first PFET 692, $PFET_1$, may be coupled to the circuit supply voltage, V_{DD}. As discussed above, the supply voltage, V_{DD}, may tracks or be substantially equal to the battery voltage, V_{BAT}, from a battery. The source of the first NFET 694, $NFET_1$, may be coupled to ground. The drain of the first PFET 692, $PFET_1$, and the drain of the first NFET 694, $NFET_1$, may be coupled to form a first input buffer output at a first voltage node 696.

[00795] The input buffer circuit 682 may further include a second input buffer circuit 698 operably coupled to the first input buffer output at the first voltage node 696. The second input buffer circuit 698 may include a second PFET 700,

$PFET_2$, and a second NFET 702, $NFET_2$. The gate of the second PFET 700, $PFET_2$, and the gate of the second NFET 702, $NFET_2$, may be coupled to the drain of the first PFET 692, $PFET_1$, and the drain of the first NFET 694, $NFET_2$, at the first voltage node 696. The source of the second PFET 700, $PFET_2$, may be coupled to the circuit supply voltage, V_{DD}. The source of the second NFET 702, $NFET_2$, may be coupled to ground. The drain of the second PFET 700, $PFET_2$, and the drain of the second NFET 702, $NFET_2$, may be coupled to form a second input buffer output at a second voltage node 704.

[00796] During operation of the first input buffer circuit 690, when the input voltage, V_{IN}, at the first input buffer input 690A is sufficiently low such that the input voltage, V_{IN} is substantially equal to or less than a logic low threshold voltage, the first PFET 692, $PFET_1$, is configured to be in a conducting state and couples the circuit supply voltage, V_{DD}, to the first voltage node 696. As a result, the voltage level at the first voltage node 696 is substantially equal to the circuit supply voltage, V_{DD}, and the first input buffer circuit 690 provides an output voltage level representative of a digital logic high state at the first voltage node 696. In addition, the first NFET 694, $NFET_1$, is configured to be in a non-conducting state when the input voltage, V_{IN}, at the first input buffer input 690A is sufficiently low such that the input voltage, V_{IN} is substantially equal to or less than the logic low threshold voltage.

[00797] However, when the input voltage, V_{IN}, at the first input buffer input 690A is sufficiently high such that the input voltage, V_{IN} is substantially equal to or greater than a logic high threshold voltage, the first NFET 694, $NFET_1$, is configured to be in a conducting state and couples the first voltage node 696 to ground. As a result, the voltage level at the first voltage node 696 is substantially equal to ground, and the first input buffer circuit 690 provides an output voltage level representative of a digital logic low state at the first voltage node 696. In addition, the first PFET 692, $PFET_1$, is configured to be in a non-conducting state when the input voltage, V_{IN}, at the first input buffer input 690A is sufficiently high such that the input voltage, V_{IN} is substantially equal to or greater than the logic high threshold voltage.

[00798] In a similar fashion, the operation of the second input buffer circuit 698 is dependent on the voltage level at the first voltage node 696, which is coupled to the first input buffer output of the first input buffer circuit 690. Accordingly, when the first input buffer circuit 690 provides a digital logic low state at the first voltage node 696 such that the voltage level at the first voltage node 696 is substantially equal to or less than the logic low threshold voltage, the second PFET 700, $PFET_2$, is configured to be in a conducting state and couples the circuit supply voltage, V_{DD}, to the second voltage node 704. As a result, the voltage level at the second input buffer circuit 698 is substantially equal to the circuit supply voltage, V_{DD}, and the second input buffer circuit 698 provides a digital logic high state at the second voltage node 704. In addition, the second NFET 702, $NFET_2$, is configured to be in a non-conducting state when the first input buffer circuit 690 provides an output voltage level representative of a digital logic low state at the first voltage node 696.

[00799] However, in a similar fashion as the operation of the first input buffer circuit 690, when the first input buffer circuit 690 provides a digital logic high state at the first voltage node 696 such that the voltage level at the first voltage node 696 is substantially equal to or higher than the logic low threshold voltage, the second NFET 702, $NFET_2$, is configured to be in a conducting state and couples the second voltage node 704 to ground. As a result, the voltage level at the second input buffer circuit 698 is substantially equal to the ground voltage, and the second input buffer circuit 698 provides a digital logic low state at the second voltage node 704. In addition, the second PFET 700, $PFET_2$, is configured to be in a non-conducting state when the first input buffer circuit 690 provides an output voltage level representative of a digital logic high state at the first voltage node 696

[00800] It will be appreciated that the propagation time of the digital logic level signal, represented by the input voltage, V_{IN}, through the input buffer circuit may be considered as a first portion of a fixed delay provided by the programmable delay circuitry 432C and is a function of the switching time of the transistors. The first portion of the fixed delay time provided by the input buffer circuit 682

depends upon the switching time of the respective first input buffer circuit 690 and the second input buffer circuit 698. In some alternative embodiments of the programmable delay circuitry 432C, additional input buffer circuits, (not depicted in Figure 30A), may be added to the input buffer circuit 682 to increase the first portion of the fixed delay provided by the input buffer circuit 682. In addition to providing a first portion of the fixed delay time through the programmable delay circuitry 432C, the combination of the first input buffer circuit 690 and the second input buffer circuit 698, may also provide the further benefit of isolating analog characteristics of the input voltage, V_{IN}, that represents the digital logic level signal from the variable delay circuitry. In some embodiments of the programmable delay circuitry 432C, the number of input buffer circuits used to provide isolation between the input voltage, V_{IN}, and the variable delay circuitry 684 may result in improved controllability of the variable delay provided by the variable delay circuitry 684.

[00801] The variable delay circuitry 684 includes an input stage 706 including a third PFET 708, $PFET_3$, a third NFET 710, $NFET_3$, a fourth PFET 714, $PFET_4$, a fourth NFET 716, $NFET_4$, a fifth PFET 718, $PFET_5$, and a fifth NFET 720, $NFET_5$. As will be explained, a portion of the input stage 706 of the variable delay circuitry 684 may include a correction start voltage circuit 712 that is formed by the interconnections of the third PFET 708, $PFET_3$ and the third NFET-710, $NFET_3$, to the fourth PFET 714, $PFET_4$, and the fourth NFET 716, $NFET_4$. The variable delay circuitry 684 further includes a variable delay capacitor 722. In some embodiments, the variable delay capacitor 722 may be configured as a programmable capacitor array.

[00802] As depicted in Figure 30A, the variable delay capacitor 722 may be coupled between a third voltage node 724 and ground. The variable delay capacitor 722 is configured to have a variable delay capacitance, C_{DELAY_VAR}. In addition, although not depicted in Figure 30A, the controller 50 (depicted in Figure 24) may be configured to govern or set various parameters to adjust the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, in order to adjust the variable delay time, $T_{VARIABLE_DELAY_TIME}$, provided by the variable delay

circuitry 684. For example, in some embodiments of the programmable delay circuitry 432C, the variable delay capacitor 722 may be configured to couple to the controller 50 (not shown), where the controller 50 is configured to control the capacitance value of the variable delay capacitance, C_{DELAY_VAR}. in some embodiments of the programmable delay circuitry 432C, the variable delay capacitor 722 may be configured to increase as the value of a binary capacitor control word, CNTR_CD, increases, as described relative to Figure 36.

[00803] For example, in some embodiments of the variable delay circuitry 684, the variable delay capacitor 722 may be configured as a programmable capacitor array. The programmable capacitor array may include multiple capacitors, where each of the capacitors is arranged in series with a switch element. Each switch element may have a switch state (open or closed) that may be controlled by the controller 50 such that the effective capacitance of the programmable capacitor array has a desired effective capacitance. In some embodiments, the programmable capacitor array may be a linear capacitor array, where each of the capacitors has the same value. In other embodiments, the programmable capacitor array may be a binary weighted capacitor array. The controller 50 may adjust the effective capacitance of the programmable capacitor array by controlling the switch state (open or closed) of each switch to combine different combinations of the multiple capacitors in parallel. Alternatively, the variable delay capacitor 722 may be a programmable varactor configured to be controlled by the controller 50. Depending on the topology and type of programmable capacitor, for example, the controller 50 may govern the effective capacitance of the programmable varactor by changing the distance between the two parallel plates that form the varactor or a voltage applied across the terminals of the varactor.

[00804] The variable delay circuitry 684 may further include an output buffer stage 726. By way of example, and not by way of limitation, the output buffer stage 726 depicted in Figure 30A includes only one level of output buffering. Thus, as depicted in Figure 30A, the output buffer stage 726 includes a sixth PFET 728, $PFET_6$, and a sixth NFET 730, $NFET_6$, operably coupled to form an

output buffer having an output buffer output 732. The output buffer input is formed by coupling the gate of the sixth PFET 728, $PFET_6$, and the gate of the sixth NFET 730, $NFET_6$, to the third voltage node 724. The output buffer output 732 is formed by coupling the drain of the sixth PFET 728, $PFET_6$, to the drain of the sixth NFET 730, $NFET_6$. The source of the sixth PFET 728, $PFET_6$, is coupled to the circuit supply voltage, V_{DD}. The source of the sixth NFET 730, $NFET_6$ is coupled to ground.

[00805] However, similar to the input buffer circuit, some alternative embodiments of the variable delay circuitry 684 may include an embodiment of the output buffer stage 726 that includes multiple levels of output buffering in order to provide additional isolation between the interior circuitry of the variable delay circuitry 684 and the digital logic level signal to be generated by the programmable delay circuitry 432C. For example, some alternative embodiments of the variable delay circuitry 684 may include additional output buffering to improve the drive level at the output of the programmable delay circuitry 432C, where as depicted in Figure 24, the programmable delay circuitry 432 is configured to drive the input of the buffer scalar 434 of the switch mode power supply converter 420.

[00806] The operation of the output buffer stage 726 depends upon the voltage level at the third voltage node 724. When the voltage level at the third voltage node 724 is equal to or less than the logic low threshold voltage such that the sixth PFET 728, $PFET_6$, is turned on and in the saturation state, the output buffer output 732 is effectively coupled to the circuit supply voltage, V_{DD}, through the sixth PFET 728, $PFET_6$. Simultaneously, the sixth NFET 730, $NFET_6$, is configured to be turned off when the sixth PFET 728, $PFET_6$ is turned on. As a result, the output buffer stage 726 provides an output voltage, V_{OUT}, substantially equal to the circuit supply voltage, V_{DD}, which represents a digital logic high state. Thus, when the voltage level at the third voltage node 724 is equal to or less than the logic low threshold voltage such that the sixth PFET 728, $PFET_6$ is turned, the output buffer stage 726 is triggered to transition from a digital logic low state to a digital logic low state at the output buffer output 732.

[00807] However, when the voltage level at the third voltage node 724 is equal to or greater than the logic high threshold voltage, such that the sixth NFET 730, $NFET_6$, is turned on and in the saturation state, the output buffer output 732 is effectively coupled to the ground through the sixth NFET 730, $NFET_6$. Simultaneously, the sixth PFET 728, $PFET_6$, is configured to be turned off when the sixth NFET 730, $NFET_6$ is turned on. As a result, the output buffer stage 726 provides an output voltage, V_{OUT}, substantially equal to ground, which represents a digital logic low state. Thus, when the voltage level at the third voltage node 724 is equal to or greater than the logic high threshold voltage such that the sixth PFET 728, $PFET_6$, is turned, the output buffer stage 726 is triggered to transition from a digital logic high state to a digital logic low state at the output buffer output 732.

[00808] The time period during which the digital logic level signal, represented by the voltage level at the third voltage node 724, propagates through the output buffer stage 726 may be a second portion of the fixed delay time provided by the programmable delay circuitry 432C. The second portion of the fixed delay time provided by the output buffer stage 726 depends on the switching time of the output buffer stage 726. Some alternative embodiments of the variable delay circuitry 684 may include additional output buffering. Accordingly, the propagation time through the output buffer stage of the variable delay circuitry 684 may be increased by addition of additional output buffering. Thus, the fixed delay time of the programmable delay circuitry 432C includes the first portion of the fixed delay time of the input buffer circuit 682 and the second portion of the fixed delay time of the output buffer stage 726.

[00809] Returning to the description of the variable delay circuitry 684 depicted in Figure 30A, to form the input stage 706 of the variable delay circuitry 684, the gate of the fourth PFET 714, $PFET_4$, and the gate of the fourth NFET 716, $NFET_4$, are coupled to the second input buffer output at the second voltage node 704. The source of the fourth PFET 714, $PFET_4$, is coupled to the drain of the fifth PFET 718, $PFET_5$. The source of the fifth PFET 718, $PFET_5$, is coupled to the circuit supply voltage, V_{DD}. The source of the fourth NFET 716, $NFET_4$, is

coupled to the drain of the fifth NFET 720, $NFET_5$. The source of the fifth NFET-720, $NFET_5$, is coupled to ground. As will be described with respect to the operation of the voltage divider circuit 686 and the bias current and mirror circuit 688, the bias current and mirror circuit 688 is configured to generate a first gate voltage on the gate of the fifth PFET 718, $PFET_5$, such that the fifth PFET-718, $PFET_5$, is configured to provide a first bias current, I_{BIAS_1}, when the fourth PFET 714, $PFET_4$, is turned on. Similarly, the bias current and mirror circuit 688 is further configured to generate a second gate voltage on the gate of the fifth NFET 720, $NFET_5$, such that the fifth NFET 720, $NFET_5$, is configured to sink a second bias current, I_{BIAS_2}, when the fourth NFET 716, $PFET_4$, is turned on. The drain of the fourth PFET 714, $PFET_4$, is coupled to the drain of the fourth NFET-716, $NFET_4$, to provide an input stage output at the third voltage node 724. The variable delay capacitor 722 is coupled between the third voltage node 724 and ground. As a result, the variable delay capacitor 722 is coupled to the drain of the fourth PFET 714, $PFET_4$, the drain of the fourth NFET 716, $NFET_4$, the gate of the sixth PFET 728, $PFET_6$, and the gate of the sixth NFET 730, $NFET_6$. The fourth PFET 714, $PFET_4$, and the fourth NFET 716, $NFET_4$, are configured such that when the fourth PFET 714, $PFET_4$, is in a conducting mode of operation (ON), the fourth NFET 716, $NFET_4$, is in a non-conducting mode (OFF). Likewise, the fourth PFET 714, $PFET_4$, and the fourth NFET 716, $NFET_4$, are configured such that when the fourth NFET 716, $NFET_4$, is in a conducting mode (ON) of operation, the fourth PFET 714, $PFET_4$, is in a non-conducting mode (OFF).

[00810] Accordingly, the fixed delay time of the programmable delay circuitry 432C may further include a third portion of the fixed delay time, where the third portion of the fixed delay time is associated with the switching time of the fourth PFET 714, $PFET_4$, and the switching time of the fourth NFET 716, $NFET_4$.

[00811] As a result, when the voltage level on the second voltage node 704 is substantially equal to or less than the logic low threshold voltage such that the fourth PFET 714, $PFET_4$, is in the conducting mode of operation (ON), the first

bias current, I_{BIAS_1}, passes through the fourth PFET 714, $PFET_4$, pushes charge into the variable delay capacitor 722 to charge the variable delay capacitor 722. As the variable delay capacitor 722 is charged, the voltage across the variable delay capacitor 722, which is substantially equal to the voltage level on the third voltage node 724, increases. However, when the voltage level on the second voltage node 704 is substantially equal to or greater than the logic high threshold voltage such that the fourth NFET 716, $NFET_4$, is in the conducting mode of operation (ON), the second bias current, I_{BIAS_2}, sunk by the fifth NFET 720, $NFET_5$, passes through the fourth NFET 716, $NFET_4$, and pulls charge from the variable delay capacitor 722 to discharge the variable delay capacitor 722. As a result, the voltage across the variable delay capacitor 722, which is substantially equal to the voltage level on the third voltage node 724, falls.

[00812] The correction start voltage circuit 712 is formed by coupling the gate of the third PFET 708, $PFET_3$ and the gate of the third NFET 710, $NFET_3$, to the second voltage node 704, such that the gates of the third PFET 708, $PFET_3$, the third NFET 710, $NFET_3$, the fourth PFET 714, $PFET_4$, and the fourth NFET 716, $NFET_4$, are coupled. The source of the third PFET 708, $PFET_3$, is coupled to the circuit supply voltage, V_{DD}. The drain of the third PFET 708, $PFET_3$, is coupled to the source of the fourth NFET 716, $NFET_4$, and the drain of the fifth NFET 720, $NFET_5$. The source of the third NFET 710, $NFET_3$, is coupled to ground. The drain of the third NFET 710, $NFET_3$, is coupled to the source of the fourth PFET-714, $PFET_4$, and the drain of the fifth PFET 718, $PFET_5$.

[00813] The correction start voltage circuit 712 is configured to provide a first known voltage level at the source of the fourth PFET 714, $PFET_4$, while the fourth PFET 714, $PFET_4$, is in the non-conducting state such that the voltage level present at the source of the fourth PFET 714, $PFET_4$, is at the first known voltage level at the moment the fourth PFET 714, $PFET_4$ transitions from the non-conducting state to the conducting state. In order to provide the first known voltage level at the source of the fourth PFET 714, $PFET_4$, while the fourth PFET 714, $PFET_4$, is in the non-conducting state, the third NFET 710, $NFET_3$, is configured to be turned on while the fourth PFET 714, $PFET_4$, is in the non-

conducting state. As a result, the source of the fourth PFET 714, $PFET_4$, is coupled to ground through the third NFET 710, $NFET_3$. In the embodiment of the correction start voltage circuit 712 depicted in Figure 30A, the first known voltage is substantially equal to ground. However, in alternative embodiments, the source of the third NFET 710, $NFET_3$, may be coupled to a voltage level other than ground such that the first known voltage is not substantially equal to ground. As an example, in some embodiments, the correction start voltage circuit 712 may be configured such that the first known voltage is substantially equal to one half the circuit supply voltage, $V_{DD}/2$.

[00814] In some embodiments of the correction start voltage circuit 712, the parasitic capacitance of the source of the fourth PFET 714, $PFET_4$, the parasitic capacitance of the drain of the fifth PFET 718, $PFET_5$, and/or a combination thereof is configured such that the voltage level present on the source of the fourth PFET 714, $PFET_4$, remains at the first known voltage level momentarily at the moment the fourth PFET 714, $PFET_4$ transitions from the non-conducting state to the conducting state. In other embodiments of the correction start voltage circuit 712, the parasitic capacitance of the drain of the third NFET 710, $NFET_3$, may also be configured to improve the ability of the correction start voltage circuit 712 to provide the first known voltage on the source of the fourth PFET 714, $PFET_4$, momentarily at the moment the fourth PFET 714, $PFET_4$, transitions from the non-conducting state to the conducting state. In addition, the third NFET 710, $NFET_3$ may be further configured to turn off just prior to or coincidentally with the fourth PFET 714, $PFET_4$, transitioning from the non-conducting state to the conducting state. Otherwise, after the charge present in the parasitic capacitance(s) is discharged, the voltage level on the source of the fourth PFET 714, $PFET_4$, is determined by the operational state of the fourth PFET 714, $PFET_4$, and the first bias current, I_{BIAS_1}, provided by the fifth PFET-718, $PFET_5$.

[00815] In a similar fashion, the correction start voltage circuit 712 is configured to provide a second known voltage level at the source of the fourth NFET 716, $NFET_4$, while the fourth NFET 716, $NFET_4$, is in the non-conducting state such

that the voltage level present at the source of the fourth NFET 716, $NFET_4$, is at the second known voltage level at the moment the fourth NFET 716, $NFET_4$ transitions from the non-conducting state to the conducting state. In order to provide the second known voltage level at the source of the fourth NFET 716, $NFET_4$, while the fourth NFET 716, $NFET_4$, is in the non-conducting state, the third PFET 708, $PFET_3$, is configured to be turned on when the fourth NFET 716, $NFET_4$, is in the non-conducting state. As a result, the source of the fourth NFET 716, $NFET_4$, is coupled through the third PFET 708, $PFET_3$, to the circuit supply voltage V_{DD}. As a result, in the embodiment of the correction start voltage circuit 712 depicted in Figure 30A, the second known voltage is substantially equal to the circuit supply voltage, V_{DD}. However, in alternative embodiments, the source of the third PFET 708, $PFET_3$, may be coupled to a voltage level other than the circuit supply voltage, V_{DD}, such that the second known voltage is not substantially equal to the circuit supply voltage, V_{DD}. As an example, in some embodiments, the correction start voltage circuit 712 may be configured such that the second known voltage is substantially equal to one half the circuit supply voltage, $V_{DD}/2$.

[00816] In some embodiments of the correction start voltage circuit 712, the parasitic capacitance of the source of the fourth NFET 716, $NFET_4$, the parasitic capacitance of the drain of the fifth NFET 720, $NFET_5$, and/or a combination thereof is configured such that the voltage level present on the source of the fourth NFET 716, $NFET_4$, remains at the second known voltage level momentarily at the moment the fourth NFET 716, $NFET_4$ transitions from the non-conducting state to the conducting state. In other embodiments of the correction start voltage circuit 712, the parasitic capacitance of the drain of the third PFET 708, $PFET_3$, may also be configured to improve the ability of the correction start voltage circuit 712 to provide the second known voltage on the source of the fourth NFET 716, $NFET_4$, momentarily at the moment the fourth NFET 716, $NFET_4$, transitions from the non-conducting state to the conducting state. In addition, the third PFET 708, $PFET_3$ may be further configured to turn off just prior to or coincidentally with the fourth NFET 716, $NFET_4$, transitioning

from the non-conducting state to the conducting state. Otherwise, after the charge present in the parasitic capacitance(s) is discharged, the voltage level on the source of the fourth NFET 716, $NFET_4$, is determined by the operational state of the fourth NFET 716, $NFET_4$, and the second bias current, I_{BIAS_2}, sunk by the fifth NFET 720, $NFET_5$.

[00817] Advantageously, because the correction start voltage circuit 712 is configured to ensure the voltage level on the source of the fourth PFET 714, $PFET_4$, is substantially equal to the first known voltage when the fourth PFET 714, $PFET_4$, is in the non-conducting state and the voltage level on the source of the fourth NFET 716, $NFET_4$, is substantially equal to the second known voltage when the fourth NFET 716, $NFET_4$, is in the non-conducting state, the initial change in the voltage level at the third voltage node 724 that occurs as a result of charge stored in the capacitances associated with the source of the fourth PFET 714, $PFET_4$, or the charge stored in the capacitances associated with the source of the fourth NFET 716, $NFET_4$, (referred to as a state transition voltage charge) is predictable and substantially consistent. As a result, the state transition voltage charge may be controlled such that the voltage across the variable delay capacitor 722 is not substantially disturbed when either the fourth PFET 714, $PFET_4$, or the fourth NFET 716, $NFET_4$, transition to be in the conducting state.

[00818] For example, as previously described, when the second input buffer circuit 698 provides a digital logic high state, the second input buffer provides an output voltage at the second voltage node 704 substantially equal to the circuit supply voltage, V_{DD}. In this case, the gate of the fourth NFET 716, $NFET_4$, is greater than the logic high threshold level. As a result, the fourth NFET 716, $NFET_4$, turns on and discharges the variable delay capacitor 722 until the voltage level at the third voltage node 724 is substantially equal to ground. In addition, the third NFET 710, $NFET_3$, of the correction start voltage circuit 712 is configured to turn on and couple the source of the fourth PFET 714, $PFET_4$, to ground such that the charge stored on the source of the fourth PFET 714, $PFET_4$, is at a voltage level substantially equal to ground. As a result, the charge

stored on the source of the fourth PFET 714, $PFET_4$, minimally affects the charging period, $\Delta T_{CHARGING_PERIOD}$, of the variable delay circuitry 684, where the charging period, $\Delta T_{CHARGING_PERIOD}$, is a period of time during which the variable delay capacitor 722 is being charged until the third voltage node 724 is equal to or exceeds the logic high threshold voltage of the output buffer stage 726.

[00819] Similarly, when the second input buffer circuit 698 provides a digital logic low state, the second input buffer provides an output voltage at the second voltage node 704 substantially equal to ground. In this case, the gate of the fourth PFET 714, $PFET_4$, is less than the logic low threshold level. As a result, fourth PFET 714, $PFET_4$, turns on and charges the variable delay capacitor 722 until the voltage level at the third voltage node 724 is substantially equal to the circuit supply voltage, V_{DD}. In addition, the third PFET 708, $PFET_3$, of the correction start voltage circuit 712 is configured to turn on and couple the source of the fourth NFET 716, $NFET_4$, to the circuit supply voltage, V_{DD}, such that the charge stored on the source of the fourth NFET 716, $NFET_4$, is at a voltage level substantially equal to ground. As a result, the charge stored on the source of the fourth NFET 716, $NFET_4$, minimally affect the charging period, $\Delta T_{DISCHARGING_PERIOD}$, of the variable delay circuitry 684, where the charging period, $\Delta T_{DISHARGING_PERIOD}$, is a period of time during which the variable delay capacitor 722 is being discharged until the third voltage node 724 is equal to or less than the logic low threshold voltage of the output buffer stage 726.

[00820] Otherwise, if the correction start voltage circuit 712 is not present, the source of the fourth PFET 714, $PFET_4$, and the source of the fourth NFET 716, $NFET_4$, will each tend to float to an undetermined voltage level when either the fourth PFET 714, $PFET_4$, or the fourth NFET 716, $NFET_4$, are in the non-conducting state. As a result, state transition voltage change is unpredictable.

[00821] The operation of the output buffer stage 726 depends upon the voltage level at the third voltage node 724. When the voltage level at the third voltage node 724 is equal to or less than the logic low threshold voltage such that the sixth PFET 728, $PFET_6$ is turned on and in the saturation state, the output buffer output 732 is effectively coupled to the circuit supply voltage, V_{DD}, through the

sixth PFET 728, $PFET_6$. Simultaneously, sixth NFET 730, $NFET_6$, is configured to be turned off when the sixth PFET 728, $PFET_6$ is turned on. As a result, the output buffer stage 726 provides an output voltage, V_{OUT}, substantially equal to the circuit supply voltage, V_{DD}, which represents a digital logic high state.

[00822] However, when the voltage level at the third voltage node 724 is equal to or greater than the logic high threshold voltage such that the sixth NFET 730, $NFET_6$ is turned on and in the saturation state, the output buffer output 732 is effectively coupled to the ground through the sixth NFET 730, $NFET_6$. Simultaneously, the sixth PFET 728, $PFET_6$, is configured to be turned off when the sixth NFET 730, $NFET_6$ is turned on. As a result, the output buffer stage 726 provides an output voltage, V_{OUT}, substantially equal to ground, which represents a digital logic low state.

[00823] The variable delay time, $T_{VARIABLE_DELAY_TIME}$, provided by the variable delay circuitry 684 is a function of a charging period, $\Delta T_{CHARGING_PERIOD}$ and a discharging period, $\Delta T_{DISCHARGING_PERIOD}$, of the variable delay capacitor 722. The charging period, $\Delta T_{CHARGING_PERIOD}$, is a period of time during which the variable delay capacitor 722 is being charged until the third voltage node is equal to or exceeds the logic high threshold voltage. During the charging period, $\Delta T_{CHARGING_PERIOD}$, the change in the voltage across the variable delay capacitor 722, necessary to change the digital logic state at the input of the output buffer stage 726, is the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$. The discharging period, $\Delta T_{DISCHARGING_PERIOD}$, is a period of time during which the variable delay capacitor 722 is being charged until the third voltage node 724 is equal to or exceed the logic high threshold voltage. During the discharging period, $\Delta T_{DISCHARGING_PERIOD}$, the change in the voltage across the variable delay capacitor 722, necessary to change the digital logic state at the input of the output buffer stage 726, is the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$.

[00824] The average variable delay time, $T_{AVERAGE_VARIABLE\ DELAY}$, provided by the variable delay circuitry 684 is provided by equation (11):

(11) $$T_{AVERAGE_VARIABLE_DELAY} = \frac{T_{CHARGEING_PERIOD} + T_{DISCHARGING_PERIOD}}{2}.$$

[00825] The charging period, $\Delta T_{CHARGING_PERIOD}$, of the variable delay capacitor 722 is dependent upon the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, and the magnitude of the variable delay capacitor current, I_{C_VAR}, where the magnitude of the variable delay capacitor current, I_{C_VAR}, is substantially equal to the first bias current, I_{BIAS_1} during the charging period, $\Delta T_{CHARGING_PERIOD}$. Similarly, the discharging period, $\Delta T_{DISCHARGING_PERIOD}$, of the variable delay capacitor 722 is dependent upon the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, and the magnitude of the variable delay capacitor current, I_{C_VAR}, where the magnitude of the variable delay capacitor current, I_{C_VAR}, is substantially equal to the second bias current, I_{BIAS_2} during the discharging period, $\Delta T_{DISCHARGING_PERIOD}$.

[00826] During the charging period, $\Delta T_{CHARGING_PERIOD}$, the variable delay capacitor current, I_{C_VAR}, is given by equation (12):

(12) $$I_{C_VAR} = \frac{\Delta V_{DELAY_VAR_CAP_CHARGING} \times C_{DELAY_VAR}}{\Delta T_{CHARGING_PERIOD}}$$

[00827] Similarly, during the discharging period, $\Delta T_{DISCHARGING_PERIOD}$, the variable delay capacitor current, I_{C_VAR}, is given by equation (13) as follows:

(13) $$I_{C_VAR} = \frac{\Delta V_{DELAY_VAR_CAP_DISCHARGING} \times C_{DELAY_VAR}}{\Delta T_{DISCHARGING_PERIOD}}$$

[00828] Assuming the variable delay capacitor current, I_{C_VAR}, is substantially equal to the first bias current, I_{BIAS_1}, provided by the fifth PFET 718, $PFET_5$, during the charging period, $\Delta T_{CHARGING_PERIOD}$, the charging period, $\Delta T_{CHARGING_PERIOD}$, is given by equation (14) as follows:

(14) $$\Delta T_{CHARGING_PERIOD} = \frac{\Delta V_{DELAY_VAR_CAP_CHARGING} \times C_{DELAY_VAR}}{I_{BIAS_1}}.$$

[00829] Likewise, assuming the magnitude of the variable delay capacitor current, I_{C_VAR}, is substantially equal to the second bias current, I_{BIAS_2}, sunk by the fifth NFET 720, $NFET_5$, during the discharging period, $\Delta T_{DISCHARGING_PERIOD}$, the discharging period, $\Delta T_{DISCHARGING_PERIOD}$, is given by equation (15):

$$\Delta T_{DISCHARGEING_PERIOD} = \frac{\Delta V_{DELAY_VAR_CAP_DISCHARGING} \times C_{DELAY_VAR}}{I_{BIAS_2}}. \quad (15)$$

[00830] In some embodiments of the programmable delay circuitry 432C the channel width of the fifth PFET 718, $PFET_5$, and the channel width of the fifth NFET 720, $NFET_5$, are configured such that the first bias current, I_{BIAS_1}, is substantially equal to the second bias current, I_{BIAS_2}, where the magnitude of the first bias current, I_{BIAS_1}, and the magnitude of the second bias current, I_{BIAS_2}, are substantially equal to a bias current, I_{BIAS}.

[00831] Some embodiments of the output buffer stage 726 may be configured such that the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, is substantially equal to the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$. For example, in some embodiments, the output buffer stage 726 logic low threshold voltage and a logic high threshold are configured such that the voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, is substantially equal to the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$. In the case where the magnitude of the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, is substantially equal to the magnitude of the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$, such that the magnitude of the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, and the magnitude of the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$, are substantially equal to a transition voltage change, $\Delta_{DELAY_VAR_CAP_TRANSITION}$, the variable delay time, $T_{VARIABLE_DELAY_TIME}$, of the variable delay circuitry 684 is given by equation (16):

$$\Delta T_{VARIABLE_DELAY_TIME} = \frac{\Delta V_{DELAY_VAR_CAP_TRANSITION} \times C_{DELAY_VAR}}{I_{BIAS}}. \quad (16)$$

[00832] In other embodiments of the programmable delay circuitry 432C, the channel width of the fifth PFET 718, $PFET_5$, and the channel width of the fifth NFET 720, $NFET_5$, may be configured such that the first bias current, I_{BIAS_1}, is not substantially equal to the second bias current, I_{BIAS_2}. In this case, the charging period, $\Delta T_{CHARGING_PERIOD}$, and the discharging period, $\Delta T_{DISHARGING_PERIOD}$, may not be substantially equal. As an example, in some embodiments, the charging period, $\Delta T_{CHARGING_PERIOD}$, is longer than the discharging period, $\Delta T_{DISHARGING_PERIOD}$. In other embodiments, the charging period, $\Delta T_{CHARGING_PERIOD}$, is less than the discharging period, $\Delta T_{DISHARGING_PERIOD}$.

[00833] As an alternative embodiment, the logic low threshold voltage and the logic high threshold of the output buffer stage 726 may be configured such the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, is substantially equal to the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$.

[00834] In addition, as discussed above, in some embodiments of the programmable delay circuitry 432C, the controller 50, as depicted in Figure 24, may be coupled to the variable delay capacitor 722. The controller 50 may be configured to control the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, based on a binary capacitor control word, CNTR_CD, such that as the value of the binary capacitor control word, CNTR_CD increases, the variable delay capacitance, C_{DELAY_VAR}, linearly increases or decreases in a substantially linear fashion. In some alternative embodiments of the variable delay capacitor 722, the variable delay capacitance, C_{DELAY_VAR}, has a minimum capacitance value, $C_{DELAY_VAR_MIN}$, that corresponds to the minimum delay provided by charging and discharging of the variable delay capacitor 722 of the variable delay circuitry 684. As an example, the minimum capacitance value, $C_{DELAY_VAR_MIN}$, of the variable delay capacitor 722 may be provided by a fixed capacitance (not depicted) in parallel with a programmable binary capacitor array. An example of a programmable binary capacitor array is depicted in Figure 36.

[00835] Furthermore, as discussed above, in some embodiments of the programmable delay circuitry 432C, the controller 50, as depicted in Figure 24, may be configured to control the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, based on a binary capacitor control word, CNTR_CD, such that as the value of the binary capacitor control word, CNTR_CD increases, the variable delay capacitance, C_{DELAY_VAR}, linearly increases or decreases in a substantially linear fashion. As a result, the variable delay circuitry 684 may be configured such that the variable delay time, $T_{VARIABLE_DELAY_TIME}$, increases in a substantially linear fashion as the variable delay capacitance, C_{DELAY_VAR}, increases in a substantially linear fashion. In addition, the delay step size, $\Delta_{VARIABLE_DELAY_TIME}$, of the variable delay circuitry 684 between any two adjacent values of the variable delay capacitance, C_{DELAY_VAR}, may be substantially equal.

[00836] Because the first input buffer circuit 690, the second input buffer circuit 698, the input stage 706 of the variable delay circuitry 684, the correction start voltage circuit 712, and the output buffer stage 726 are substantially symmetric in construction, the first input buffer circuit 690, the second input buffer circuit 698, the input stage 706 of the variable delay circuitry 684, the correction start voltage circuit 712, and the output buffer stage 726 may be configured such that the logic low threshold voltage and the logic high threshold voltage tend to proportionally track the circuit supply voltage, V_{DD}. As a result, the magnitude of the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, and the magnitude of the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$, will also tend to proportionally track the circuit supply voltage, V_{DD}. However, the variations in the variable delay time, $T_{VARIABLE_DELAY_TIME}$, provided by the variable delay circuitry 684 due to changes in the voltage level of the circuit supply voltage, V_{DD}, may be minimized or controlled by configuring the programmable delay circuitry 432C such that the magnitude of the first bias current, I_{BIAS_1}, and the magnitude of the second bias current, I_{BIAS_2}, change proportionally with respect to a change in the voltage level of the circuit supply voltage, V_{DD}. For example, because the logic high threshold and the logic low threshold tend to proportionally track the circuit supply voltage, V_{DD}, some embodiments of the

programmable delay circuitry 432C may be configured such that the variations in the variable delay time, $T_{VARIABLE_DELAY_TIME}$, are minimized or controlled with respect to a change in the circuit supply voltage, V_{DD}. In this case, the variable delay time, $T_{VARIABLE_DELAY_TIME}$, is substantially insensitive to the circuit supply voltage because a change in the magnitude of the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, and change in the magnitude of the discharging voltage change, $\Delta_{DELAY_VAR_CAP_}$, due to a change in the circuit supply voltage, V_{DD}, are substantially cancelled out by a corresponding change in a magnitude of the first bias current, I_{BIAS_1}, and a change in the magnitude of the second bias current, I_{BIAS_2}, due to the change in the magnitude of the circuit supply voltage, V_{DD}.

[00837] Alternatively, the dependence of the variable delay time, $T_{VARIABLE_DELAY_TIME}$, on the circuit supply voltage, V_{DD}, may be used advantageously. As an example, some embodiments of multi-level charge pump buck converter 12M, depicted in Figures 23A, have a switcher propagation delay. The switcher propagation delay is a time period between when the state of the switcher control circuit 52 changes to a new state and the switching voltage, V_{SW}, generated in response to the new state of the switcher control circuit 52 is generated at the switching voltage output 26. The switcher propagation delay may be due to a combination of the delays in the switcher control circuit 52, the multi-level charge pump circuit 56 and the switching circuit 58. In some embodiments the multi-level charge pump buck converter 12M, the switcher propagation delay may change as a function of the battery voltage, V_{BAT}, received from the battery and/or temperature. Likewise, the buck converter 13L depicted in Figure 23B, may also have a switcher propagation delay. As an example, the switcher propagation delay may decrease as the battery voltage, V_{BAT}, increases. As another example, the switcher propagation delay may increase as the battery voltage, V_{BAT}, decreases. Refering to Figure 24, the programmable delay circuitry 432 is configured to provide a programmable delay period to temporally align the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, with respect to the V_{RAMP} signal such that the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$,

substantially represents the switching voltage, V_{SW}, and the V_{RAMP} signal substantially represents the power amplifier supply voltage, V_{CC}, in order to time align the generation of the high frequency ripple compensation current 416, I_{COR}.

[00838] Returning to Figure 30A, in order to maintain the relationship between the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, and the V_{RAMP} signal, the programmable delay circuitry 432C may be configured such that either a change in the variable delay time, $T_{VARIABLE_DELAY_TIME}$, of the variable delay circuitry 684 or a change in the programmable delay period of the programmable delay circuitry 432C due to a change in the circuit supply voltage, V_{DD}, substantially tracks or compensates for a change in the switcher propagation delay due to change in a voltage level of the battery voltage, V_{BAT}, where the circuit supply voltage, V_{DD}, may be substantially equal to or derived from the battery voltage, V_{BAT}.

[00839] As an example, the voltage divider circuit 686 and bias current and mirror circuit 688 may be configured such that the first bias current, I_{BIAS_1}, provided by the fifth PFET 718, $PFET_5$, and the second bias current, I_{BIAS_2}, sunk by the fifth NFET 720, $NFET_5$, are related to the voltage level of the circuit supply voltage, V_{DD}, such that the variations in the variable delay time, $T_{VARIABLE_DELAY_TIME}$, provided by the variable delay circuitry 684 due to changes in the voltage level of the circuit supply voltage, V_{DD}, may be minimized or controlled.

[00840] The bias current and mirror circuit 688 includes a seventh PFET 734, $PFET_7$, a seventh NFET 736, $NFET_7$, an eighth PFET 738, $PFET_8$, an eighth NFET 740, $PFET_9$, a bias reference current setting resistor 744, and a bias resistor 746. The bias reference current setting resistor 744 has a bias reference current setting resistance, R_3. The bias resistor 746 has a bias resistance, R_4.

[00841] The source of the seventh PFET 734, $PFET_7$, is coupled to the circuit supply voltage, V_{DD}. The gate of the seventh PFET 734, $PFET_7$, is coupled to the source of the seventh PFET 734, $NFET_7$, and the drain of the eighth NFET 740, $NFET_8$. In addition, the gate and drain of the seventh PFET 734, $PFET_7$, is coupled to the gate of the fifth PFET 718, $PFET_5$.

[00842] The gate and drain of the seventh PFET 734, $PFET_7$, is coupled to the drain of the eighth NFET 740, $NFET_8$, The source of the eighth NFET 740, $NFET_8$, is coupled to the drain of the seventh NFET 736, $NFET_7$. The sources of the eighth NFET 740, $NFET_8$, and the seventh NFET 736, $NFET_7$, are coupled to ground. The gate of the seventh NFET 736, $NFET_7$, is coupled to the drain and gate of the ninth NFET 742, $NFET_9$. In addition, the gate of the seventh NFET 736, $NFET_7$, and the gate and drain of the ninth NFET 742, $NFET_9$, are coupled to the gate of the fifth NFET 720, $NFET_5$, of the variable delay circuitry 684.

[00843] The bias reference current setting resistor 744 is coupled between the circuit supply voltage, V_{DD}, and the source of the eighth PFET 738, $PFET_8$. The bias resistor 746 is coupled between the drain of the eighth PFET 738, $PFET_8$, and the drain and gate of the ninth NFET 742, $NFET_9$, and the gate of the seventh NFET 736, $NFET_7$.

[00844] The voltage divider circuit 686 includes a first voltage divider resistor 748, a tenth PFET 750, $PFET_{10}$, an eleventh PFET 752, $PFET_{11}$, and a second voltage divider resistor 754. The first voltage divider resistor 748 has a first voltage divider resistance, R_1. The second voltage divider resistor 754 has a second voltage divider resistance, R_2. The first voltage divider resistance, R_1, of the first voltage divider resistor 748 is substantially equal to the second voltage divider resistance, R_2, of the second voltage divider resistor 754.

[00845] The first voltage divider resistor 748 is coupled between the circuit supply voltage, V_{DD}, and the source of the tenth PFET 750, $PFET_{10}$. The gate of the tenth PFET 750, $PFET_{10}$, is coupled to the drain of the tenth PFET 750, $PFET_{10}$ and the source of the eleventh PFET 752, $PFET_{11}$. The gate of the eleventh PFET 752, $PFET_{11}$, is coupled to the drain of the eleventh PFET 752, $PFET_{11}$. The second voltage divider resistor 754 is coupled between the drain of the eleventh PFET 752, $PFET_{11}$, and ground. Because the gate of the tenth PFET 750, $PFET_{10}$, is coupled to the drain of the tenth PFET 750, and the gate of the eleventh PFET 752, $PFET_{11}$, is coupled to the drain of the eleventh PFET 752, $PFET_{11}$, both the tenth PFET 750, $PFET_{10}$, and the eleventh

PFET 752, $PFET_{11}$, are biased to be on in a saturation mode of operation. The source-to-drain voltage across the tenth PFET 750, $PFET_{10}$, and the source-to-drain voltage across the eleventh PFET 752, $PFET_{11}$, are substantially equal. Because the first voltage divider resistance, R_1, of the first voltage divider resistor 748 is substantially equal to the second voltage divider resistance, R_2, of the second voltage divider resistor 754, the voltage divider circuit 686 may be configured to set a bias voltage substantially equal to one-half of the circuit supply voltage, V_{DD}, on the drain of the tenth PFET 750, $PFET_{10}$, and the source of the eleventh PFET 752, $PFET_{11}$.

[00846] The operation of the bias current and mirror circuit 688 is now explained with reference to the voltage divider circuit 686. The bias current and mirror circuit 688 is coupled to the voltage divider circuit 686 by coupling the gate of the eighth PFET 738, $PFET_8$, to the gate and drain of the eleventh PFET 752, $PFET_{11}$. The eighth PFET 738, $PFET_8$, of the bias current and mirror circuit 688 and the eleventh PFET 752, $PFET_{11}$, of the voltage divider circuit 686 are configured such that the gate-to-source voltage of the eighth PFET 738, $PFET_8$, is substantially equal to the gate-to-source voltage of the eleventh PFET 752, $PFET_{11}$. As a result, the voltage on the source of the eighth PFET 738, $PFET_8$, is substantially equal to the voltage on the source of the eleventh PFET 752, $PFET_{11}$. As discussed above with respect to the operation of the voltage divider circuit 686, a reference voltage, V_{REF}, on the source of the eleventh PFET 752, $PFET_{11}$, is substantially equal to $V_{DD}/2$. Accordingly, the voltage on the source of the eighth PFET 738, $PFET_8$, is also substantially equal to $V_{DD}/2$. The current through the bias reference current setting resistor 744, which is the reference bias current, I_{BIAS_REF}, is provided by equation (17) as follows:

$$I_{BIAS_REF} = \frac{V_{DD} - \frac{V_{DD}}{2}}{R_3} = \frac{V_{DD}}{2 \times R_3} \quad (17)$$

[00847] Accordingly, the drain-to-source current of the ninth NFET 742, $NFET_9$, is substantially equal to I_{BIAS_REF}. Because the gate and drain of the ninth

NFET 742, $NFET_9$, are coupled to the gate of the seventh NFET 736, $NFET_7$, and the gate of the fifth NFET 720, $NFET_5$, the source- to-drain current flowing through the ninth NFET 742, $NFET_9$, is mirrored such that the drain-to-source current flowing through the seventh NFET 736, $NFET_7$, and the drain-to-source current flowing through the fifth NFET 720, $NFET_5$, are proportional to the drain-to-source current flowing through the ninth NFET 742, $NFET_9$. Furthermore, the source-to-drain current flowing through the seventh PFET 734, $PFET_7$, is substantially equal to the drain-to-source current flowing through the seventh NFET 736, $NFET_7$. Because the gate-to-source voltage of the fifth PFET 718, $PFET_5$, is substantially equal to the gate voltage of the seventh PFET 734, $PFET_7$, the source-to-drain current of the seventh PFET 734, $PFET_7$, is proportional to the bias reference current, I_{BIAS_REF}, where the bias reference current setting resistance, R_3, of the bias reference current setting resistor 744 sets the bias reference current, I_{BIAS_REF}. As a result, the first bias current, I_{BIAS_1}, proportionally tracks the circuit supply voltage, V_{DD}. Similarly, the second bias current, I_{BIAS_2}, proportionally tracks the circuit supply voltage, V_{DD}. As a result, for the case where rate of change of the first bias current, I_{BIAS_1}, and second bias current, I_{BIAS_2}, with respect to the circuit supply voltage, V_{DD}, is substantially equal to the rate of change of the charging voltage change, $\Delta_{DELAY_VAR_CAP_CHARGING}$, and the discharging voltage change, $\Delta_{DELAY_VAR_CAP_DISCHARGING}$, as change, the charging period, $\Delta T_{CHARGING_PERIOD}$, and the discharging period, $\Delta T_{DISCHARGING_PERIOD}$, will be substantially insenstivie to a change in the circuit suppy voltage, V_{DD}.

[00848] As an example, the magnitude of the first bias current, I_{BIAS_1}, and second bias current, I_{BIAS_2}, is balanced out by the change in the logic low threshold voltage and the logic high threshold voltage. As a result, the variable delay time, $T_{VARIABLE_DELAY_TIME}$, will be substantially unchanged as the circuit supply voltage, V_{DD}, changes. In some embodiments, the input buffer circuit 682 and the output buffer stage 726 may be configured to be substantially insensitive to the circuit supply voltage, V_{DD}. However, in some embodiments of the variable delay circuitry 684, the variable delay circuitry 684 may be configured such that

the variable delay time, $T_{VARIABLE_DELAY_TIME}$, the fixed delay of the input buffer circuit 682 and the output buffer stage 726, and/or a combination thereof change proportionally with respect to the circuit supply voltage, V_{DD}. For example, some embodiments of the programmable delay circuitry 432C may be configured such that the programmable delay period changes with respect to the circuit supply voltage, V_{DD}. As an example, in some embodiments of the variable delay circuitry 684, the bias current and mirror circuit 688 may be configured with respect to the fifth PFET 718, $PFET_5$, and the fifth NFET 720, $NFET_5$ such that the magnitude of the first bias current, I_{BIAS_1}, and the magnitude of the second bias current, I_{BIAS_2}, change more than the magnitude of the logic low threshold voltage and the magnitude of the logic high threshold voltage with respect to the circuit supply voltage, V_{DD}. In this case, because the charging period, $\Delta T_{CHARGING_PERIOD}$, and discharging period, $\Delta T_{DISCHARGING_PERIOD}$, of the variable delay capacitor 722 proportionally track the first bias current, I_{BIAS_1}, and second bias current, I_{BIAS_2}, respectively, the variable delay time, $T_{VARIABLE_DELAY_TIME}$, changes with respect to the circuit supply voltage. As an example, as the circuit supply voltage, V_{DD}, increases, if the bias reference current, I_{BIAS_REF}, increases at a faster rate than the logic low threshold voltage and the logic high threshold voltage, the variable delay time, $T_{VARIABLE_DELAY_TIME}$, decreases because the charging period, $\Delta T_{CHARGING_PERIOD}$ and discharging period, $\Delta T_{DISCHARGING_PERIOD}$, of the variable delay capacitor 722 decrease. In addition, as the circuit supply voltage, V_{DD}, decreases, the bias reference current, I_{BIAS_REF}, will decrease such that the variable delay time, $T_{VARIABLE_DELAY_TIME}$ will increase because the charging period, $\Delta T_{CHARGING_PERIOD}$ and discharging period, $\Delta T_{DISCHARGING_PERIOD}$, of the variable delay capacitor 722 will increase. Accordingly, some embodiments of the programmable delay circuitry 432C may be configured to change the programmable delay period at a desired rate with respect to the circuit supply voltage in order to compensate for a change in the switcher propagation delay as the battery voltage, V_{BAT}, from the battery changes. As a result, the programmable delay circuitry 432C may be configured to substantially

maintain a temporal alignment over a range of voltage levels of the circuit supply voltage, V_{DD}.

[00849] In some embodiments, the bias reference current setting resistance, R_3, resistance value may be configured to minimize or control the sensitivity of the variable delay time, $T_{VARIABLE_DELAY_TIME}$, provided by the variable delay circuitry 684 to a change in the voltage level of the circuit supply voltage, V_{DD}. In addition, in some embodiments, the channel width ratios of the channel width of the ninth NFET 742, $NFET_9$, to each of the channel widths of the seventh PFET 734, $PFET_7$, the seventh NFET 736, $NFET_7$, the fifth PFET 718, $PFET_5$ and the fifth NFET 720, $NFET_5$, may be configured to minimize or control the sensitivity of the variable delay time, $T_{VARIABLE_DELAY_TIME}$, provided by the variable delay circuitry 684 due to changes in the voltage level of the circuit supply voltage, V_{DD}.

[00850] Figure 36 depicts an example embodiment of the variable delay capacitor 722, depicted in Figure 30A, as variable delay capacitor 722A. The variable delay capacitor 722A may be configured as a programmable capacitor array 758. The programmable capacitor array 758 may be coupled to the controller 50 via a variable capacitance control bus 760, CNTR_CD (5:1). The variable delay capacitor 722A has a variable delay capacitance, C_{DELAY_VAR}. The controller 50 may be configured to control the variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 722A by configuring the programmable capacitor array 758.

[00851] The variable capacitance control bus 760, CNTR_CD (5:1), may include a first capacitor control signal 762, CNTR_CD1, a second capacitor control signal 764, CNTR_CD2, a third capacitor control signal 766, CNTR_CD3, a fourth capacitor control signal 768, CNTR_CD4, and a fifth capacitor control signal 770, CNTR_CD5.

[00852] The programmable capacitor array 758 may include a first array capacitor 772, a second array capacitor 774, a third array capacitor 776, a fourth array capacitor 778, and a fifth array capacitor 780. The first array capacitor 772 may have a capacitance substantially equal to a first array capacitor capacitance,

C_{D1}. The second array capacitor 774 may have a capacitance substantially equal to a second array capacitor capacitance, C_{D2}. The third array capacitor 776 may have a capacitance substantially equal to a third array capacitor capacitance, C_{D3}. The fourth array capacitor 778 may have a capacitance substantially equal to a fourth array capacitor capacitance, C_{D4}. The fifth array capacitor 780 may have a capacitance substantially equal to a fifth array capacitor capacitance, C_{D5}.

[00853] In addition, the programmable capacitor array 758 may further include a first switch element 782, $NFET_{11}$, a second switch element 784, $NFET_{12}$, a third switch element 786, $NFET_{13}$, a fourth switch element 788, $NFET_{14}$, and a fifth switch element 790, $NFET_{15}$. In Figure 36, by way of example and not by way of limitation, the first switch element 782, $NFET_{11}$, the second switch element 784, $NFET_{12}$, the third switch element 786, $NFET_{13}$, the fourth switch element 788, $NFET_{14}$, and the fifth switch element 790, $NFET_{15}$ are each depicted as NFET devices.

[00854] The programmable capacitor array 758 includes a first programmable capacitance 792, a second programmable capacitance 794, a third programmable capacitance 796, a fourth programmable capacitance 798, and a fifth programmable capacitance 800. The first programmable capacitance 792 may be formed by coupling the first array capacitor 772 between the third voltage node 724 and the drain of the first switch element 782, $NFET_{11}$, where the source of the first switch element 782, $NFET_{11}$, is coupled to ground and the gate of first switch element 782, $NFET_{11}$, is coupled to the first capacitor control signal 762, CNTR_CD1, of the variable capacitance control bus 760, CNTR_CD (5:1). The second programmable capacitance 794 may be formed by coupling the second array capacitor 774 between the third voltage node 724 and the drain of the second switch element 784, $NFET_{12}$, where the source of the second switch element 784, $NFET_{12}$, is coupled to ground and the gate of second switch element 784, $NFET_{12}$, is coupled to the second capacitor control signal 764, CNTR_CD2, of the variable capacitance control bus 760, CNTR_CD (5:1). The third programmable capacitance 796 may be formed by coupling the third array

capacitor 776 between the third voltage node 724 and the drain of the third switch element 786, $NFET_{13}$, where the source of the third switch element 786, $NFET_{13}$, is coupled to ground and the gate of third switch element 786, $NFET_{13}$, is coupled to the third capacitor control signal 766, CNTR_CD3, of the variable capacitance control bus 760, CNTR_CD (5:1). The fourth programmable capacitance 798 may be formed by coupling the fourth array capacitor 778 between the third voltage node 724 and the drain of the fourth switch element 788, $NFET_{14}$, where the source of the fourth switch element 788, $NFET_{14}$, is coupled to ground and the gate of fourth switch element 788, $NFET_{14}$, is coupled to the fourth capacitor control signal 768, CNTR_CD4, of the variable capacitance control bus 760, CNTR_CD (5:1). The fifth programmable capacitance 800 may be formed by coupling the fifth array capacitor 780 between the third voltage node 724 and the drain of the fifth switch element 790, $NFET_{15}$, where the source of the fifth switch element 790, $NFET_{15}$, is coupled to ground and the gate of the fifth switch element 790, $NFET_{15}$, is coupled to the fifth capacitor control signal 770, CNTR_CD5, of the variable capacitance control bus 760, CNTR_CD (5:1).

[00855] As an example, in some embodiments, the variable delay capacitor 722A is configured such that the programmable capacitor array 758 is a linearly programmable capacitor array. The variable delay capacitor 722A may be configured to be a linearly programmable capacitor array by configuring the first array capacitor capacitance, C_{D1}, the second array capacitor capacitance, C_{D2}, the third array capacitor capacitance, C_{D3}, the fourth array capacitor capacitance, C_{D4}, and the fifth array capacitor capacitance, C_{D5}, to have the same capacitance value.

[00856] As an alternative example, in some embodiments of the variable delay capacitor 722A, the programmable capacitor array 758 may be configured as a binary weighted programmable capacitor array. The binary weighted programmable capacitor array may be configured such that the second array capacitor capacitance, C_{D2}, has substantially twice the capacitance as the first array capacitor capacitance, C_{D1}, the third array capacitor capacitance, C_{D3}, has

substantially twice the capacitance as the second array capacitor capacitance, C_{D2}, the fourth array capacitor capacitance, C_{D4}, has substantially twice the capacitance as the third array capacitor capacitance, C_{D3}, and the fifth array capacitor capacitance, C_{D5}, has substantially twice the capacitance as the fourth array capacitor capacitance, C_{D4}.

[00857] The controller 50 may be configured to selectively control the variable capacitance bus, CNTR_CD (5:1), to set the capacitance value of the variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 722A. The first capacitor control signal 762, CNTR_CD1, the second capacitor control signal 764, CNTR_CD2, the third capacitor control signal 766, CNTR_CD3, the fourth capacitor control signal 768, CNTR_CD4, and the fifth capacitor control signal 770, CNTR_CD5, may form a binary capacitor control word, CNTR_CD, where $0 \geq CNTR_CD \geq 31$.

[00858] Accordingly, the programmable capacitor array 758 may be configured such that as the value of the binary capacitor control word, CNTR_CD increases from 0 to 31, the effective capacitance of the programmable capacitor array 758 changes linearly.

[00859] Accordingly, returning to Figure 30A, with continuing reference to Figures 23A-27D, Figure 24, Figures 27A-27B, and Figure 36, in those embodiments of the programmable delay circuitry 432C that include an embodiment of the variable delay capacitor 722A, depicted in Figure 36, the delay step size, $\Delta_{VARIABLE_DELAY_TIME}$, of the variable delay circuitry 684 between any two adjacent values of the variable delay capacitance, C_{DELAY_VAR}, may be a function of the granularity of the effective capacitance of the binary capacitor control word, CNTR_CD changes, and the number of array capacitors present in the binary weighted programmable capacitor array. In some embodiments of the programmable delay circuitry 432C, the variable delay circuitry 684 may be configured such that the average delay step size, $\Delta_{VARIABLE_DELAY_TIME}$, of the variable delay time, $T_{VARIABLE_DELAY_TIME}$, is about 136 picoseconds. In other embodiments of the programmable delay circuitry 432C, the variable delay circuitry 684 may be configured such that the average delay step size,

$\Delta_{VARIABLE_DELAY_TIME}$, of the variable delay time, $T_{VARIABLE_DELAY_TIME}$, is about 100 picoseconds.

[00860] Illustratively, by way of example, and not by limitation, in some embodiments of the programmable capacitor array 758 used to provide the variable delay capacitance, C_{DELAY_VAR}, of the variable delay circuitry 684, the first array capacitor capacitance, C_{D1}, of the first array capacitor 772 may have a capacitance of around 18.25pF. The second array capacitor capacitance, C_{D2}, of the second array capacitor 774 may have a capacitance of around 30.93pF. The third array capacitor capacitance, C_{D3}, of the third array capacitor 776 may have a capacitance of around 61.86pF. The fourth array capacitor capacitance, C_{D4}, of the fourth array capacitor 778 may have a capacitance of around 123.72pF. The fifth array capacitor capacitance, C_{D5}, of the fifth array capacitor 780 may have a capacitance of around 247.45pF.

[00861] Accordingly, referring to the example embodiments of the open loop ripple compensation assist circuit 414A, depicted in Figure 24, the open loop ripple compensation assist circuit 414B, depicted in Figure 27A, and the open loop ripple compensation assist circuit 414C, depicted in Figured 27B, the variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 722, depicted in Figure 30A, may be configured by the controller 50 by incrementally changing the variable delay time, $T_{VARIABLE_DELAY_TIME}$, provided by the programmable delay circuitry 432C, depicted in Figure 30A, in steps substantially equal to the average delay step size, $\Delta_{VARIABLE_DELAY_TIME}$. For example, for the case where the average delay step size, $\Delta_{VARIABLE_DELAY_TIME}$, is substantially equal to 136 picoseconds, the high frequency ripple compensation current 416, I_{COR}, may be aligned to within an accuracy of less than136 picoseconds. The precision of the average temporal alignment may be based upon the granularity of the capacitance values of the capacitors of the binary capacitor array.

[00862] Figure 37 depicts an example graph of the total delay time provided by the programmable delay circuitry 432C, depicted in Figure 30A, as a function of the binary capacitor control word, CNTR_CD, of the programmable capacitor array 758, depicted in Figure 36, with respect to temperature. As depicted in

Figure 37, the fixed delay time of the programmable delay circuitry 432C is approximately 2.45ns when the programmable delay circuitry 432C operates at 30 °C. The variable delay capacitance, C_{DELAY_VAR}, of the variable delay capacitor 722 provides around 4ns of variable delay time, $T_{VARIABLE_DELAY_TIME}$, with an average delay step size, $\Delta_{VARIABLE_DELAY_TIME}$, substantially equal to 132ns.

[00863] Returning to Figure 30A, some alternative embodiments of the programmable delay circuitry 432C may include embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C", depicted in Figure 30B and Figure 30C, respectively. The programmable delay circuitry 432C' and the programmable delay circuitry 432C" having a programmable delay period similar to the programmable delay period provided the programmable delay circuitry 432C, depicted in Figure 30A. The various embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may automatically adjust the programmable delay period as a function of the circuit supply voltage, V_{DD}, to track a change in the switcher propagation delay period with respect to a change in the battery voltage, V_{BAT}. In addition, some of the various embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may automatically adjust the programmable delay period as a function of temperature to track a change in the switcher progagation delay period over temperature. And several embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may adjust the programmable delay period as a function of both a change in the temperature and a change in the circuit supply voltage, V_{DD}, to track a change in the switcher propagation delay period over both temperature and changes in the battery voltage, V_{BAT}. In addition, various embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may adjust the programmable delay period over both temperate and changes in the battery voltage, V_{BAT}, and/or the circuit suppy voltage, V_{DD}, that further compensate the programmable delay period to account for the propagation of the switching voltage, V_{SW}, to the modulated power supply

output 876 as a function of temperature, the circuit supply voltage, V_{DD}, the battery voltage, V_{BAT}, and/or some combination thereof. Still further embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may also compensate for the propagation delay in various embodiments of active noise reduction circuity as a function of temperature, the circuit supply voltage, V_{DD}, the battery voltage, V_{BAT}, and/or some combination thereof. For example, the various embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may offset changes in the switcher propagation delay and an active noise reduction circuit propagation delay in various embodiments of an active noise reduction circuit. An example of at least one embodiment of an active noise reduction circuit may include the various embodiments of the open loop ripple compensation assist circuits 414 and 414A-B, depicted in Figures 23A-D, Figure 24-26, and Figures 31A-D, and the various embodiments of the parallel amplifier output impedance compensation circuits 37B-F, depicted in Figures 34A-E. As an example, the active noise reduction circuit propagation delay of the open loop ripple compensation assist circuit 414 may include the propagation delay between arrival of the delayed I_{COR} estimated switching voltage output 38C at the open loop ripple compensation assist circuit 414 and application of high frequency ripple compensation current 416, I_{COR}, to the modulated power supply output 876, depicted in Figures 46B-H. As another example, the various embodiments of the parallel amplifier output impedance compensation circuit 37B, the parallel amplifier output impedance compensation circuit 37C, the parallel amplifier output impedance compensation circuit 37D, the parallel amplifier output impedance compensation circuit 37E, and the parallel amplifier output impedance compensation circuit 37F, depicted in Figures 34A-E, may each include an active noise reduction circuit propagation delay. As an example, the active noise reduction circuit propagation delay of the parallel amplifier output impedance compensation circuit 37B may include the propagation delay between arrival of the delayed estimated switching voltage output, 38D, $V_{SW_EST_DELAYED}$, at the parallel amplifier output impedance compensation circuit 37B and the

application of the parallel amplifier circuit output current, I_{PAWA_OUT}, that include the parallel amplifier output current, I_{PARA_AMP}, generated in response to the compensated V_{RAMP} signal, V_{RAMP_C}, generated based on the delayed estimated switching voltage output, 38D, $V_{SW_EST_DELAYED}$. In other words, the programmable delay period may be automatically adjusted with respect to changes in the temperature, the circuit supply voltage, V_{DD}, the battery voltage, V_{BAT}, and/or some combination thereof to maintain a temporial alignment of the various example embodiments of the active noise reduction circuit.

[00864] The description of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" will be made with continuing reference to the various embodiments of the programmable delay circuitry 432C, the controller 50, the battery level sense circuit 264, the programmable delay circuitry 432, various embodiments of the open loop ripple compensation assist circuits 414 and 414A-B, and the modulated power supply output 876 of the various embodiments of the embodiments of the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A, depicted in the Figure 30A, Figures 23A-D, Figure 24, Figures 34A-E, Figures 40A-E, and Figures 46A-H.

[00865] As a non-limiting example, some embodiments of multi-level charge pump buck converter 12M, depicted in Figures 23A, have a switcher propagation delay. The switcher propagation delay is a time period between when the state of the switcher control circuit 52 changes to a new state and the switching voltage, V_{SW}, generated in response to the new state of the switcher control circuit 52 is generated at the switching voltage output 26. The switcher propagation delay may be due to a combination of the delays in the switcher control circuit 52, the multi-level charge pump circuit 56 and the switching circuit 58. In some embodiments the multi-level charge pump buck converter 12M, the switcher propagation delay may change as a function of the battery voltage, V_{BAT}, received from the battery 20, temperature, and/or a combination of the battery voltage, V_{BAT}, received from the battery and temperature. Likewise, the buck converter 13L, depicted in Figure 23B, may also

have a switcher propagation delay. As an example, the switcher propagation delay may decrease as the battery voltage, V_{BAT}, increases. As another example, the switcher propagation delay may increase as the battery voltage, V_{BAT}, decreases. In addition, some embodiments of the open loop ripple compensation assist circuit 414, depicted in Figures 23A-D, may also include a propagation delay that changes with respect to variations in temperature, the battery voltage, V_{BAT}, and/or a combination thereof.

[00866] Refering briefly to Figure 24, the programmable delay circuitry 432 is configured to provide a programmable delay period to temporally align the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, with respect to the V_{RAMP} signal such that the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, substantially represents the switching voltage, V_{SW}, and the V_{RAMP} signal substantially represents the power amplifier supply voltage, V_{CC}, in order to time align the generation of the high frequency ripple compensation current 416, I_{COR}.

[00867] Returning to Figures 30B and 30C, in order to maintain the relationship between the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, and the V_{RAMP} signal, the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may be configured to automatically adjust the programmable delay period of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" of the with respect to temperature, the circuit supply voltage, V_{DD}, and/or a combination thereof to substantially track or compensate for a change in the switcher propagation delay due to change in temperature and/or the battery voltage, V_{BAT}, where the circuit supply voltage, V_{DD}, may substantially equal or be derived from the battery voltage, V_{BAT}.

[00868] Accordingly, some embodiments of the programmable delay circuitry 432C' and the programmable delay circuitry 432C" may be adapted to adjust the programmable delay period to automatically adjust the programmable delay period to offset changes in the switcher propagation delay, the over temperature and variations in the battery voltage, V_{BAT}, and the circuit supply

voltage, V_{DD}, on the performance of the various embodiments of the open loop ripple compensation assist circuit 414, depicted in Figures 23A-D.

[00869] Figure 30B depicts a programmable delay circuitry 432C' configured to compensate for changes in a programmable deplay period due to variations in the temperature, the supply voltage, V_{DD}, and/or a combination thereof. The programmable delay circuitry 432C' may be substantially similar in form and function to the programmable delay circuitry 432C depicted in Figure 30A. The programmable delay circuitry 432C' further includes a first compensation current source 968A coupled between the drain of the tenth PFET 750, $PFET_{10}$, and the source of the eleventh PFET 752, $PFET_{11}$, and ground. The first compensation current source 968A may be configured to sink current provided from the tenth PFET 750, $PFET_{10}$. As the magnitude of the current sunk by the first compensation current source 968A increases, the current through the first voltage divider resistor 748 also increases. As a result, the reference voltage, V_{REF}, present on the source of the eleventh PFET 752, $PFET_{11}$, may increase and decrease as a function of the current sunk by the first compensation current source 968A. Accordingly, the voltage drop across the bias reference current setting resistor 744 may also increase and decrease as a function of the current sunk by the first compensation current source 968A. As a result, sensitivity of the first compensation current source 968A to a change in temperature and a change in the supply voltage, V_{DD}, may be configured to increase or decrease the reference bias current, I_{BIAS_REF}, which sets the magnitude of the variable capacitance current, I_{C_VAR}, used to charge and discharge the variable delay capacitor 680. Because magnitude of the variable capacitance current, I_{C_VAR}, determines the variable delay time of the variable delay circuitry 640A, the sensitivity of the compensation current source 968A to a change in temperature and the change in the supply voltage, V_{DD}, may be configured to change the programmable delay period provided by the programmable delay circuitry 432C' as a function of temperature and the supply voltage, V_{DD}, in a controlled manner and at a desired rate. In addition, the sensitivity of the first compensation current source 968A to temperature and the supply voltage may be configured to

compensate for changes in the propagation time through the input buffer circuit 682 and variable delay circuitry 684, where the variable delay circuitry 684 may include the output buffer stage 726.

[00870] To reduce the programmable delay period provided by the programmable delay circuitry 432C' as a function of a temperature increase or an increase in the supply voltage, V_{DD}, the first compensation current source 968A may be configured to sink additional current as a function of an increase in the temperature or the supply voltage, V_{DD}. For example, the first compensaction current source 968A may include a temperature dependent current source (not shown) and a voltage dependent current source (not shown). The temperature dependent current sourse (not shown) may generate a temperature dependent current. The supply voltage dependent current source (not shown) may generate a supply voltage dependent current.

[00871] In some embodiments, the temperature dependent current source (not shown) may be configured to increase the current sunk by the first compensation current source 968A as temperature increases. For example, the temperature dependent current source may be a proportional to absolute temperature (PTAT) current source configured to generate a proportional to absolute temperature (PTAT) output current. In some embodiments, the proportional to absolute temperature (PTAT) current source may include a programmable resistor array having a programmable resistance that may set the slope of the proportional to absolute temperature (PTAT) output current. Alternatively, in some embodiments, the temperature dependent current source (not shown) may be configured to decrease the current sunk by the first compensation current source 968A as temperature increases. As an example, the temperature dependent current source may be an inverse proportional to absolute temperature (Inverse PTAT) current source configured to generate a proportional to absolute temperature (Inverse PTAT) output current. In some embodiments, the inverse proportional to absolute temperature (Inverse PTAT) current source may include a programmable resistor array having a programmable resistance that may be configured to set the magnitude of the inverse proportional to

absolute temperature (Inverse PTAT) output current). In other embodiments of the proportional to absolute temperature (PTAT) current source and the inverse proportional to absolute temperature (Inverse PTAT) current source may not include a programmable resistor array. Accordingly, first compensation current source 968A may be configured to either increase or decrease the programmable delay period of the programmable delay circuitry 432C' with respect to temperature to compensate for the sensitivity of the switcher propagation delay to temperature.

[00872] Similarly, in some embodiments, the voltage dependent current source (not shown) may be configured to increase the current sunk by the first compensation current source 968A in response to an increase in the supply voltage, V_{DD}. Alternatively, in some embodiments, the voltage dependent current source (not shown) may be configured to decrease the current sunk by the first compensation current source in response to a decrease in the supply voltage, V_{DD}. For example, some embodiments of the voltage dependent current source may include a bandgap reference device may include a bandgap reference voltge output configured to provide a bandgap reference voltage that is substantially insensitive to temperature. In some embodiments, the voltage dependent current source may use a difference between the bandgap reference voltage and the supply voltage, $V_{DD,}$ to generate either a proportional to supply voltage current or an inversely proportional to supply voltage current that is substantially insensitive to a change in temperature. In this case, the bandgap reference circuit may be configured to have a low sensitivity to both temperature and the suppy voltage, V_{DD}.

[00873] Alternatively, some embodiments of the supply voltage dependent current source may include a bandgap voltage device configured to generate a bandgap reference voltage that is sensitive to the supply voltage, V_{DD}. In this case, the bandgap reference voltage may be used to generate a proportional to supply voltage current as a function of the change in the bandgap reference voltage with respect to the supply voltage, V_{DD}. In a similar fashion, the bandgap reference voltage may be used to generate an inversely proportional to supply

voltage current as a function of the change in the bandgap reference voltage with respect to the supply voltage, V_{DD}.

[00874] Although not depicted in Figure 30B, the supply voltage dependent current source may include a first programmable resistor array in communication with the controller 50, and the temperature dependent current source may include a second programmable resistor array in communication with the controller 50. The controller 50 may adjust the resistance of the first programmable resistor array to calibrate programmable delay period of the programmable delay circuitry 432C' with respect to a temperature change. For example, during factory calibration, the controller 50 may be configured to adjust the resistance of the first programmable resistor array to obtain a desired programmable delay period at a particular test temperature. Alternatively, the resistance of the first programmable resistor array may be configured based on simulation results and the lot characteristics of an integrated chip. In addition, the controller 50 may store different settings for the resistance of the first programmable resistor array depending on the operational configuration of the embodiments of the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A, depicted in Figures 40A-E and Figures 46A-H. For example, referring to the embodiments of the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A depicted in Figures 40A-C and Figures 46A-B, the sensitivity of the switcher propagation delay through the switch mode power supply converter 872 may vary dending upon the segmentation of the switching circuit 884. For example, referring to the power management systems 870 and 870A depicted in Figures 40A-C and 46A-B, the controller 50 may adjust the resistance of the first programmable resistor array based on a power level modulation mode in which the respective power management systems 870 and 870A are configured to operate.

[00875] As a non-limiting example, the propagation delay period provided by the programmable delay circuitry 432C' may be configured to compensate for a

change in the switcher propagation delay. For example, referring briefly to Figure 40B, the switcher propagation delay may include the time period between a change in an operational state of the switcher control circuit 880 to generate a switching voltage, V_{SW}, and the application or generation of the switching voltage, V_{SW} at the switching voltage output 26. As depicted in Figure 40A, the switcher propagation delay of the switch mode power supply converter 872 may be related to both the signal propagation from the switcher control circuit 880 to a multi-level charge pump 882 and a switching circuit 884 and the delay associated with transitioning between a present value of the switching voltage, V_{SW}, and the to be generated switching voltage, V_{SW}. As an example, the segmentation mode of the switching circuit 884 may impact the switcher propagation delay. Accordingly, in some embodiments, the controller 50 may configure the first compensation current source 968A as a function of the segmentation mode of the switching circuit 884. In other embodiments, the controller 50 may configure the first compensation current source 968A as a function of the expected output power of the radio frequency power amplifier 869.

[00876] The programmable delay circuitry 432C" may be substantially similar in form and function to the programmable delay circuitry 432C depicted in Figure 30A. The programmable delay circuitry 432C" further includes a second compensation current source 968B coupled between the drain of the ninth NFET 742, $NFET_9$, and ground. The second compensation current source 968B may be configured to sink a portion of the reference bias current, I_{BIAS_REF}, provided from the drain of the eighth PFET 738, $PFET_8$. As the magnitude of the current sunk by the second compensation current source 968B increases, the gate voltage on the gate of the ninth NFET 742, $NFET_9$, the voltage on the gate of the fifth NFET 720, $NFET_5$, and the gate of the seventh NFET 736, $NFET_7$, may decrease. In response to the reduced gate voltage, drain-to-source current of the fifth NFET 720, $NFET_5$, and the gate of the seventh NFET 736, $NFET_7$, may be reduced. The reduced drain-to-source current of the seventh NFET 736, $NFET_7$, may reduce the source-to-drain current of the seventh PFET 734, $PFET_7$, and the source-to-drain current of the fifth PFET 718, $PFET_5$. As a result, the

magnitude of the variable capacitance current, I_{C_VAR}, used to charge and discharge the variable delay capacitor 680 may decrease in response to an increase in the magnitude of the current sunk by the second compensation circuit source 968B.

[00877] To increase the programmable delay period provided by the programmable delay circuitry 432C" as a function of an increase in temperature, the second compensation current source 968B may be configured to sink additional current as the temperature increases. To decrease the programmable delay period provided by the programmable delay circuitry 432C" as a function of an increase in the supply voltage, V_{DD}, the second compensation current source 968B may be further configured to sink less current as the supply voltage increases.

[00878] For example, the second compensation current source 968B may include an absolute temperature (PTAT) current source configured to generate a proportional to absolute temperature (PTAT) output current. As temperature increases, the proportional to absolute temperature (PTAT) current source may sink additional current. In some embodiments, the proportional to absolute temperature (PTAT) current source may include a first programmable resistor array having one or more resistors in parallel. The resistance of the first programmable resistor array may be configured by the controller 50 to set a slope of a current increase with respect to temperature change. The controller 50 may configure the resistance of the first programmable resistor array to set the rate of change in the variable capacitance current, I_{C_VAR}, versus temperature such that the programmable delay period of the by the programmable delay circuitry 432C" substantially tracks the change in the switcher propagation delay with respect to temperature.

[00879] Similarly, the second compensation current source 968B may further include an inversely proportional to supply voltage current source voltage configured to generate an inversely proportional to supply voltage current. For example, the second compensation current source 968B may include a bandgap reference voltge output configured to provide a bandgap reference voltage that is

substantially insensitive to temperature. The voltage dependent current source may be configured to generate an inversely proportional to supply voltage current based on a difference voltage between the bandgap reference voltage and the supply voltage, V_{DD}. As an example, the difference voltage may increase as the supply voltage, V_{DD}, increases. A differential voltage circuit may be configured to receive the difference voltage and differential reference voltage, where the differential reference voltage is based on the bandgap reference voltage. The inverting output of the differential voltage circuit may be combined with a current mirror to generate the inversely proportional to supply voltage current as a function of the differential voltage and the bang gap reference voltage. As the supply voltage, V_{DD}, increases, the inversely proportional to the supply voltage, V_{DD}, the inversely proportional to supply voltage current may decrease, where the inversely proportional to supply voltage current is substantially independent of a change in temperature. As a result, as the supply voltage, V_{DD}, increases, the variable capacitance current, I_{C_VAR}, will tend to increase shorten the variable delay period. Similarly, as the supply voltage, V_{DD}, decreases, the variable capacitance current, I_{C_VAR}, will tend to increase shorten the variable delay period.

[00880] The inversely proportional to supply voltage current source may further include a second resistor array including one or more resistors that may be configured by the controller 50 to set the slope of inversely proportional to supply voltage current with respect to a change in the supply voltage, V_{DD}. The controller 50 may adjust the resistance of the first programmable resistor array to calibrate programmable delay period of the programmable delay circuitry 432C" with respect to a temperature change. For example, during factory calibration, the controller 50 may be configured to adjust the resistance of the first programmable resistor array and the resistance of the second programmable array to obtain a desired programmable delay period at a particular test temperature and supply voltage. Alternatively, the resistance of the first programmable resistor array and the resistance of the second programmable resistor array may be configured based on simulation results and the lot

characteristics of an integrated chip. In addition, the controller 50 may store different settings for the resistance of the first programmable resistor array and the resistance of the second programmable resistor array depending on various operational configuration parameters.

[00881] For example, referring Figures 40A-C and Figure 46A-B, the embodiments of the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A may be configured to operate in a number of operational modes including buck converter modes, pseudo-envelope follower modes, and average power tracking modes of operation. Depending on the operational mode of operation, the switch mode power supply converter 872 may have different switcher propagation delay as a function of the segmentation configuration of the switching circuit 884 and a mode of operation of the multi-level charge pump 882. For example, referring to the power management systems 870 and 870A depicted in Figures 40A-C and 46A-B, the controller 50 may adjust the resistance of the first programmable resistor array and resistance of the second programmable resistor array based on a power level modulation mode in which the respective power management systems 870 and 870A are configured to operate.

[00882] In addition, the open loop ripple compensation assist circuit 414, depicted in Figures 23A-D, the open loop ripple compensation assist circuit 414A, depicted in Figure 24, the open loop ripple compensation assist circuit 414B, depicted in Figure 27A, and the open loop ripple compensation assist circuit 414C, depicted in Figured 27B may include a compensation circuit propagation delay that varies with respect to temperature, the battery voltage, V_{BAT}, from the battery 20, and/or a combination thereof. For example, the compensation circuit propagation delay maybe include the time period between arrival of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, with respect to the V_{RAMP} signal, until generation and/or application of high frequency ripple compensation current 416, I_{COR}, to the modulated power supply output 876, as depicted in Figures 46B-H. In some

embodiments, a switcher propagation delay period may further include the propagation delay between the switching voltage output 26 and the modulated power supply output 876.

[00883] Figure 34A depicts an example embodiment of a pseudo-envelope follower power management system 10PA that is similar in form and function to the pseudo-envelope follower power management system 10B, depicted in Figure 2B. However, unlike the pseudo-envelope follower power management system 10B, depicted in Figure 2B, the pseudo-envelope follower power management system 10PA may include a switch mode power supply converter 802 instead of the multi-level charge pump buck converter 12B. The switch mode power supply converter 802 may include a switcher control circuit 804 and programmable delay circuitry 806. In addition, unlike the pseudo-envelope follower power management system 10B, depicted in Figure 2B, the pseudo-envelope follower power management system 10PA includes a parallel amplifier circuit 14PA.

[00884] Similar to the switch mode power supply converter 420 depicted in Figure 24, but not by way of limitation, the switch mode power supply converter 802, depicted in Figures 34A-34E, may be either a multi-level charge pump buck converter or a buck converter. For example, the switch mode power supply converter 802 may be configured to be similar in form and function to the previously described embodiments of the multi-level charge pump buck converter 12M, depicted in Figure 23A and Figure 23C. Alternatively, in some embodiments, the switch mode power supply converter 802 may be configured to be similar in form and function to the buck converter 13L, depicted in Figure 23B and Figure 23D. However, unlike the switch mode power supply converter 420, depicted in Figure 24, the switch mode power supply converter uses the switcher control circuit 804 in combination with the programmable delay circuitry 806 to generate a delayed estimated switching voltage output, 38D, $V_{SW_EST_DELAYED}$, instead of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$. Similar to the generation of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, depicted in Figure 24,

controller 50 may configure the delay provided by the programmable delay circuitry 806 to temporally shift the delayed estimated switching voltage output, 38D, $V_{SW_EST_DELAYED}$, with respect to the estimated switching voltage output 38B, V_{SW_EST}. Accordingly, similar to the generation of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, depicted in Figure 24, the controller 50 may temporally align the generation of the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, with respect to the V_{RAMP} signal to improve performance of the circuitry and systems to be described.

[00885] In addition, some embodiments of the switch mode power supply converter 802 may include a frequency locked loop circuit (not depicted) similar to the frequency locked loop circuit 54. Likewise, as a non-limiting example, when the switch mode power supply converter 802 is configured as a multi-level charge pump buck converter, the switcher control circuit 804 may be similar to or incorporate various combinations of the operational features and functions of the embodiments of the switcher control circuits 52A-D, depicted in Figures 3A-D, the threshold detector and control circuits 132A-D, depicted in Figures 4A-D, and the circuitry and state machines depicted in Figures 5A-D and Figure 6A-D that are associated with the logic circuits 148A-D, depicted in Figures 4A-D. Alternatively, as another non-limiting example, when the switch mode power supply converter 802 is configured as a buck converter, the switcher control circuit 804 may be similar to or incorporate the various combinations of the operational features and functions of the embodiments of the switcher control circuits 52E-H, depicted in Figures 3E-H, the threshold detector and control circuits 132E-H, depicted in Figures 4E-H, and the circuitry and state machine depicted in Figures 5E-H that are associated with the logic circuits 148E-H, depicted in Figures 4E-H.

[00886] Similar to the generation of the estimated switching voltage output 38B, V_{SW_EST}, by the switcher control circuit 52 of the multi-level charge pump buck converter 12B, depicted in Figure 2B, the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, provides an indication of the

switching voltage output, V_{SW}, to be generated at the switching voltage output 26 based on the state of the switcher control circuit 804, except the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, may be delayed by an alignment period, $T_{ALIGNMENT}$. In contrast to the estimated switching voltage output 38B, V_{SW_EST}, generated by embodiments of the switcher control circuits 52A-H, the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, provides an indication of the switching voltage, V_{SW}, to be generated at the switching voltage output 26 that may be delayed by the alignment period, $T_{ALIGNMENT}$, to compensate for delays in either the switch mode power supply converter 802 or the parallel amplifier circuit 14PA.

[00887] As an example, and not by way of limitation, similar to the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, depicted in Figure 24, the programmable delay circuitry 806 of the switch mode power supply converter 802 may be configured by the controller 50 to provide a delay alignment period, $T_{ALIGNMENT}$, in order to generate the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$. As a non-limiting example, the programmable delay circuitry 806 may be similar in form and function to the embodiments of the programmable delay circuitry 432, depicted in Figure 24, including the programmable delay circuitry 432A, depicted in Figure 29A, the programmable delay circuitry 432B, depicted in Figure 29B, or the programmable delay circuitry 432C, 432C', and 432C", depicted in Figures 30A-C.

[00888] In addition, the switcher control circuit 804 may include a threshold detector and control circuit (not shown) similar to the threshold detector and control circuit 132A of the switcher control circuit 52A, depicted in Figure 3A, that generates the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, to be provided to the programmable delay circuitry 806. Thus, similar to the switch mode power supply converter 420, depicted in Figure 24, the controller 50 may configure the programmable delay circuitry 806 to delay the one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}(s)$, by the alignment period, $T_{ALIGNMENT}$, in order to delay generation of the delayed estimated switching voltage output 38D,

$V_{SW_EST_DELAYED}$, relative to the state of the switcher control circuit 804. In addition, similar to the switch mode power supply converter 420 depicted in Figure 24, the controller 50 may configure the switch mode power supply converter 802 to scale the magnitude of the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, such that the magnitude of the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, tracks variations in the supply input 24, (V_{BAT}).

[00889] The pseudo-envelope follower power management system 10PA further includes a V_{RAMP} digital-to-analog (D/A) circuit 808 and a parallel amplifier circuit 14PA that is similar in form and function to the parallel amplifier circuit 14B, depicted in Figure 2B. However, unlike the parallel amplifier circuit 14B, the parallel amplifier circuit 14PA may be further configured to receive both the estimated switching voltage output 38B, V_{SW_EST}, and the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, generated by the switch mode power supply converter 802. In addition, the V_{RAMP} digital-to-analog (D/A) circuit 808 may be configured to receive a digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, from a baseband portion of a transceiver or modem (not depicted). The V_{RAMP} digital-to-analog (D/A) circuit 808 converts the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, to provide a version of the V_{RAMP} signal in the analog domain. The version of the V_{RAMP} signal may be either a differential or a single ended signal. The V_{RAMP} digital-to-analog (D/A) circuit 808 provides the V_{RAMP} signal to the first control input 34 of the parallel amplifier circuit 14PA.

[00890] The pseudo-envelope follower power management system 10PA includes a parallel amplifier output impedance compensation circuit 37B configured to generate a compensated V_{RAMP} signal, V_{RAMP_C}, for use by the parallel amplifier 35 in lieu of the V_{RAMP} signal in order to reduce the high frequency ripple voltages generated in the parallel amplifier output voltage, V_{PARA_AMP}, by the parallel amplifier 35 at the parallel amplifier output 32A due to the non-ideal output impedance characteristics of the parallel amplifier 35. For example, as previously discussed with respect to the parallel amplifier output impedance compensation circuit 37A, depicted in Figure 10, one of the non-ideal

output impedance characteristics of the parallel amplifier 35 is that the parallel amplifier 35 an output impedance response that is inductive and increases approximately +6dB/octave near and around the switching frequency of the switch mode power supply converter 802. Thus, for example, the output impedance of the parallel amplifier 35 may be characterized as having a parallel amplifier inductance, L_{CORR}, as previously discussed with respect to Figure 10.

[00891] Returning to Figure 34A, in addition, the parallel amplifier output impedance compensation circuit 37B includes a digital V_{RAMP} pre-distortion filter circuit 812. The frequency response of the digital V_{RAMP} pre-distortion filter circuit 812 may be configured to equalize the response of the pseudo-envelope follower power management system 10PA. As an example, the digital V_{RAMP} pre-distortion filter circuit 812 may be configured to pre-distort the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, in order to compensate for different combinations of the power inductor inductance of the power inductor 16 and the bypass capacitance, C_{BYPASS}, of the bypass capacitor 19, the transfer function of the parallel amplifier 35, the power amplifier associated inductance, L_{PA}, (not shown), and the power amplifier filter associated capacitance, C_{PA}, (not shown), and/or some combination thereof.

[00892] For example, the power amplifier associated inductance, L_{PA}, (not shown) includes any parasitic inductance or filter inductance added between the power amplifier supply voltage, V_{CC}, controlled by the parallel amplifier circuit 14PA, and the power amplifier collector 22A of a linear radio frequency power amplifier 22. The power amplifier associated capacitance, C_{PA},(not shown) includes any parasitic capacitance of a load line between the power amplifier supply voltage, V_{CC}, controlled by the parallel amplifier circuit 14PA and any added decoupling capacitance related to a power amplifier decoupling capacitor (not shown) coupled to the power amplifier collector 22A. The power amplifier associated inductance, L_{PA}, and the power amplifier associated capacitance, C_{PA}, (not shown) may be determined at the time of calibration of an electronic device that includes the pseudo-envelope follower power management system 10PA. The power amplifier associated inductance, L_{PA}, (not shown) in

combination with the power amplifier associated capacitance, C_{PA}, (not shown) may form a power amplifier low pass filter (not shown) such that the frequency response of the combination of the power amplifier low pass filter and the pseudo-envelope follower power management system 10PA is not substantially flat through the operating frequency range of the linear radio frequency power amplifier 22. Accordingly, the frequency response of the digital V_{RAMP} pre-distortion filter circuit 812 may be configured to compensate the frequency response of the pseudo-envelope follower power management system 10PA such that the overall frequency response, as measured between the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, and the power amplifier collector 22A, is substantially flat through the operating frequency range of the linear radio frequency power amplifier 22.

[00893] As depicted in Figure 34A, in some embodiments of the parallel amplifier output impedance compensation circuit 37B, the digital V_{RAMP} pre-distortion filter circuit 812 is located in a digital baseband processing portion of a transceiver or modem of a communication device (not shown). The digital V_{RAMP} pre-distortion filter circuit 812 is in communication with the parallel amplifier circuit 14PA, and provides a pre-filtered V_{RAMP} signal 814, $V_{RAMP_PRE\text{-}FILTERED}$. In some alternative embodiments of the pseudo-envelope follower power management system 10PA, (not shown), the digital V_{RAMP} pre-distortion filter circuit 812 may be included in the parallel amplifier circuit 14PA.

[00894] Accordingly, unlike the parallel amplifier circuit 14B, depicted in Figure 2B, the parallel amplifier circuit 14PA, depicted in Figure 34A, includes a portion of a parallel amplifier output impedance compensation circuit 37B that is in communication with a digital V_{RAMP} pre-distortion filter circuit 812. Whereas the embodiments of the parallel amplifier output impedance compensation circuit 37, depicted in Figure 2B, and the parallel amplifier output impedance compensation circuit 37A, depicted in Figure 10, are depicted as receiving an analog V_{RAMP} signal, the digital V_{RAMP} pre-distortion filter circuit 812 of the parallel amplifier output impedance compensation circuit 37B is configured to receive a digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, from the baseband portion of a transceiver

or modem. The digital V_{RAMP} pre-distortion filter circuit 812 provides a pre-filtered V_{RAMP} signal 814, $V_{RAMP_PRE\text{-}FILTERED}$. As will be discussed, the digital V_{RAMP} pre-distortion filter circuit 812 filters the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, to generate the pre-filtered V_{RAMP} signal 814, $V_{RAMP_PRE\text{-}FILTERED}$, to equalize the overall frequency response of the pseudo-envelope follower power management system 10PA.

[00895] Figure 35 is described with continuing reference to Figure 34A. Figure 35 depicts an embodiment of V_{RAMP} digital-to-analog (D/A) circuit 808 and the digital V_{RAMP} pre-distortion filter circuit 812. As depicted in Figure 35, the V_{RAMP} digital-to-analog (D/A) circuit 808 may include a digital delay circuit 808A, a first digital-to-analog (D/A) converter circuit 808B, and an anti-aliasing filter 808C. The V_{RAMP} digital-to-analog (D/A) circuit 808 may be coupled to the control bus 44, from controller 50 (not depicted), and configured to receive the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$. Via the control bus 44, the controller 50 may configure the operation of the digital delay circuit 808A, the first digital-to-analog (D/A) converter circuit 808B, and the anti-aliasing filter 808C. The V_{RAMP} digital-to-analog (D/A) circuit 808 may be configured to generate the V_{RAMP} signal in the analog domain. For example, in some embodiments, the V_{RAMP} digital-to-analog (D/A) circuit 808 may generate a differential analog version of the V_{RAMP} signal. The digital delay circuit 808A may be configured to receive the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$. The digital delay circuit 808A may be a programmable tapped delay line configured to delay the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, such that the generated the V_{RAMP} signal is temporally aligned with the pre-filtered V_{RAMP} signal 814, $V_{RAMP_PRE\text{-}FILTERED}$. The digital delay circuit provides the delayed version of the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, to the first digital-to-analog (D/A) converter circuit 808B. The first digital-to-analog (D/A) converter circuit 808B converts the delayed version of the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, into an analog representation of the V_{RAMP} signal, which is anti-aliasing filtered by the anti-aliasing filter 808C to generate the V_{RAMP} signal.

[00896] The digital V_{RAMP} pre-distortion filter circuit 812 may include a pre-filter circuit 812A, a second digital-to-analog converter (D/A) circuit 812B, and an anti-aliasing filter 812C. The pre-filter circuit 812A may be configured to be either an infinite impulse response (IIR) filter or a finite impulse response (FIR) filter configured to receive the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$. The pre-filter circuit 812A may be configured by the controller 50 to control the frequency response of the pre-filter circuit 812A. The pre-filter circuit 812A may include one or more coefficients that may be configured by the controller 50 to shape the frequency response of the pre-filter circuit 812A.

[00897] As an example, in the case where the pre-filter circuit 812A is configured to be an infinite impulse response (IIR) filter, the pre-filter circuit 812A may include feed forward filter coefficients and feedback filter coefficients. Likewise, the pre-filter circuit 812A may be configured to be a multiple order filter. For example, in some embodiments of the digital V_{RAMP} pre-distortion filter circuit 812, the pre-filter circuit 812A may be configured to be a first order filter. In alternative embodiments of the digital V_{RAMP} pre-distortion filter circuit 812, the pre-filter circuit 812A may be a filter having two or more orders. As a result, the digital V_{RAMP} pre-distortion filter circuit 812 may permit the controller to have additional degrees of control of the pre-distortion of the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, which is used to provide a pre-distorted V_{RAMP} signal. As an example, the controller 50 may configure the feed forward coefficients and the feedback coefficients of the digital V_{RAMP} pre-distortion filter circuit 812 to provide frequency peaking to compensate for the low pass filter effect of the combination of the power amplifier associated inductance, L_{PA}, (not shown), and the power amplifier filter associated capacitance, C_{PA}, (not shown), as described above.

[00898] As an alternative case, in some embodiments the pre-filter circuit 812A may be a finite impulse response (FIR) filter having multiple weighting coefficients. The controller 50 may configure each of the weighting coefficients to configure the frequency response of the digital V_{RAMP} pre-distortion filter circuit 812 to pre-distort the digital V_{RAMP} signal, $V_{RAMP_DIGITAL}$, to also equalize the overall frequency response of the pseudo-envelope follower power

management system 10PA. In addition, the digital V_{RAMP} pre-distortion filter circuit 812 may be further configured to compensate for the power amplifier associated inductance, L_{PA}, (not shown), and the power amplifier filter associated capacitance, C_{PA}, (not shown), such that the overall frequency response, as measured between the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, and the power amplifier collector 22A, is substantially flat through the operating frequency range of the linear radio frequency power amplifier 22.

[00899] The output of the pre-filter circuit 812A is digital to analog converted by the second digital-to-analog converter (D/A) circuit 812B, where the output of the second digital-to-analog converter (D/A) circuit 812B is anti-alias filtered by the anti-aliasing filter 812C to provide the pre-filtered V_{RAMP} signal 814, $V_{RAMP_PRE\text{-}FILTERED}$. The frequency response of the pre-filter circuit 812A may be configured to equalize the overall transfer function response between the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, and the power amplifier collector 22A. As an example, the amount or shape of the equalization provided by the frequency response of the pre-filter circuit 812A, and thus the digital V_{RAMP} pre-distortion filter circuit 812, may depend upon the bypass capacitance, C_{BYPASS}, of the bypass capacitor 19, the power amplifier associated inductance, L_{PA}, (not shown), the power amplifier associated capacitance, C_{PA}, (not shown), the frequency response of the parallel amplifier 35, and/or a combination thereof.

[00900] In addition, the controller 50 may adjust the frequency response of the pre-filter circuit 812A by modifying the one or more coefficients of the pre-filter circuit 812A to equalize the relative transfer function response between the power amplifier supply voltage V_{CC}, and the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$. The controller 50 adjusts the frequency response of the pre-filter circuit 812A such that the frequency response of the overall transfer function response between the digital V_{RAMP} signal 810, $V_{RAMP_DIGITAL}$, and the power amplifier collector 22A is substantially flattened through a desired frequency range. Illustratively, in some embodiments, the controller 50 may configure the equalization or frequency response of the pre-filter circuit 812A such that the frequency response of the overall transfer function response the digital V_{RAMP}

signal 810, $V_{RAMP_DIGITAL}$, and the power amplifier collector 22A is substantially flattened out to around 20MHz.

[00901] As an example, where the pre-filter circuit 812A is configured as an IIR filter, the pre-filter circuit 812A is configured to operate at a clock rate of about 312 MHz. Illustratively, for the case where the bypass capacitance, C_{BYPASS}, of the bypass capacitor 19 is approximately 2nF, the controller 50 may configure the frequency response of the pre-filter circuit 812A to have a pole at approximately 14.5 MHz and a zero at approximately 20MHz.

[00902] In addition, in some embodiments of the digital V_{RAMP} pre-distortion filter circuit 812, the controller 50 may configure the equalization or frequency response provided by the pre-filter circuit 812A as a function of the operational bandwidth of the linear radio frequency power amplifier 22 needed to provide the wide-band modulation corresponding to a specific LTE band number. As an example, in a case where the LTE band has a 15MHz bandwidth, the controller 50 may configure the digital V_{RAMP} pre-distortion filter circuit 812 to provide additional V_{RAMP} pre-distortion such that the radio frequency signal generated by the linear radio frequency power amplifier falls within the spectrum mask requirements for an LTE 15 MHz test case.

[00903] Returning to Figure 34A, the parallel amplifier output impedance compensation circuit 37B may further include an estimated switching voltage output selection switch 816, S_1, having a first input 816A configured to receive the estimated switching voltage output 38B, V_{SW_EST}, a second input 816B configured to receive the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, and an estimated switching voltage output selection switch output 816C. The controller 50 may configure the estimated switching voltage output selection switch 816, S_1, to provide either the estimated switching voltage output 38B, V_{SW_EST}, or the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, as an estimated switching voltage input signal 820, V_{SW_I}, at the estimated switching voltage output selection switch output 816C.

[00904] The parallel amplifier output impedance compensation circuit 37B further includes a first subtracting circuit 822, Z_{OUT} compensation high pass

filter 824, a G_{CORR} scalar circuit 826, a second subtracting circuit 828, a tune circuit 830, and a summing circuit 832. The first subtracting circuit 822 includes a positive terminal configured to receive the V_{RAMP} signal provided to the first control input 34 of the parallel amplifier circuit 14PA and a negative terminal configured to receive the estimated switching voltage input signal 820, V_{SW_I}. The first subtracting circuit 822 subtracts the estimated switching voltage input signal 820, V_{SW_I}, from the V_{RAMP} signal to generate an expected difference signal 834, which is provided to the Z_{OUT} compensation high pass filter 824. The expected difference signal 834 represents the difference between the target voltage level of the power amplifier supply voltage V_{CC}, to be generated at the power amplifier supply output 28 in response to the V_{RAMP} signal and the switching voltage, V_{SW}, to be provided at the switching voltage output 26 of the switch mode power supply converter 802 at the time when the parallel amplifier 35 generates the parallel amplifier output voltage, V_{PARA_AMP}, at the parallel amplifier output 32A based on the difference between the power amplifier supply voltage, V_{CC}, and the compensated V_{RAMP} signal, V_{RAMP_C}.

[00905] The frequency response of the Z_{OUT} compensation high pass filter 824 may be configurable. As an example, the Z_{OUT} compensation high pass filter 824 may include programmable time constants. The Z_{OUT} compensation high pass filter 824 may include resistor arrays or capacitance arrays that may be configurable by the controller 50 to set the value of programmable time constants. For example, the resistor arrays may be binary weighted resistor arrays similar to the binary weighted resistor arrays previously described. The capacitor arrays may be binary weighted capacitor arrays similar to the binary weighted capacitor arrays previously described. The controller 50 may configure the programmable time constants of the Z_{OUT} compensation high pass filter 824 to obtain a desired high pass filter response. In addition, the controller 50 may configure the programmable time constants of the Z_{OUT} compensation high pass filter 824 to obtain a desired high pass filter response as a function of the operational bandwidth or the wide-bandwidth modulation associated with the LTE

band number for which the linear radio frequency power amplifier 22 is configured to operate.

[00906] Illustratively, in some embodiments, the Z_{OUT} compensation high pass filter 824 may have a programmable time constant set to 40 nanoseconds. For example, the programmable time constant may be obtained by the controller 50 configuring the resistance of a programmable resistor to be substantially equal to 4K ohms and the capacitance of a programmable capacitor to be substantially equal to 10pF. In this scenario, the high pass cutoff frequency, f_{HPC}, of the example Z_{OUT} compensation high pass filter 824 may be approximately equal to 4 MHz. In some embodiments, the Z_{OUT} compensation high pass filter 824 may be a multiple-order high pass filter having multiple programmable time constants. In the case where the Z_{OUT} compensation high pass filter 824 is a multiple-order high pass filter, the controller 50 may be configured to set multiple programmable time constants to obtain a desired high pass frequency response from the Z_{OUT} compensation high pass filter 824. As an example, the Z_{OUT} compensation high pass filter 824 may be a second order high pass filter having a first time constant and a second time constant corresponding to a first high pass cutoff frequency, f_{HPC1}, and a second high pass cutoff frequency, f_{HPC2}. In this case, the controller 50 may configure the first time constant and the second time constant of the Z_{OUT} compensation high pass filter 824 to obtain a desired high pass frequency response. In other embodiments, the Z_{OUT} compensation high pass filter 824 may be configured as an active filter.

[00907] When the controller 50 configures the estimated switching voltage output selection switch 816, S_1, to provide the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, as the estimated switching voltage input signal 820, V_{SW_I}, the controller 50 may configure the programmable delay circuitry 806 to provide a delay substantially equal to an alignment period, $T_{ALIGNMENT}$, in order to time align the indication of the switching voltage output, V_{SW}, represented by the estimated switching voltage input signal 820, V_{SW_I}, with the V_{RAMP} signal. The expected difference signal 834 is provided to the Z_{OUT} compensation high pass filter 824. The Z_{OUT} compensation high pass filter 824

high pass filters the expected difference signal 834 to generate an estimated high frequency ripple signal 836. The high pass filtering of the Z_{OUT} compensation high pass filter 824 substantially extracts only the high frequency content of the expected difference signal 834, where the high frequency content of the expected difference signal 834 represents a scaled derivative of the ripple current in the power inductor current, I_{SW_OUT}, of the power inductor 16 generated by the switch mode power supply converter 802 due to the changes in the switching voltage, V_{SW}, associated with the estimated switching voltage input signal 820, V_{SW_I}. Thus, the estimated high frequency ripple signal 836 represents an estimated high frequency ripple current at the power amplifier supply output 28 that may cause the parallel amplifier 35 to generate high frequency ripple voltages in the parallel amplifier output voltage, V_{PARA_AMP}, at the parallel amplifier output 32A. The delay period provided by the programmable delay circuitry 806 may be configured by the controller 50 to temporally align the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, with the V_{RAMP} signal to improve the accuracy of the estimated high frequency ripple signal 836.

[00908] In contrast, the controller 50 may configure the estimated switching voltage output selection switch 816, S_1, to provide the estimated switching voltage output 38B, V_{SW_EST}, as the estimated switching voltage input signal 820, V_{SW_I}, to the Z_{OUT} compensation high pass filter 824. In this case, the Z_{OUT} compensation high pass filter 824 high pass filters the expected difference signal 834 to generate the estimated high frequency ripple signal 836. The estimated high frequency ripple signal 836 substantially corresponds to a scaled derivative of a switcher ripple current in the power inductor current, I_{SW_OUT}, of the power inductor 16 based on the estimated switching voltage output 38B, V_{SW_EST}. However, because the generation of the estimated switching voltage output 38B, V_{SW_EST}, cannot be temporally aligned by adjusting a delay period provided by the programmable delay circuitry 806, the controller 50 may not configure the programmable delay circuitry 806 to minimize the peak-to-peak ripple voltages on the power amplifier supply voltage, V_{CC}, by improving the temporal alignment

of the estimated switching voltage output 38B, V_{SW_EST}, with respect to the V_{RAMP} signal.

[00909] As previously discussed, the Z_{OUT} compensation high pass filter 824 high pass filters the expected difference signal 834 generated based on the estimated switching voltage output 38B, V_{SW_EST}, to generate the estimated high frequency ripple signal 836. The pass band of the Z_{OUT} compensation high pass filter 824 extract only the high frequency content of the estimated switching voltage input signal 820, V_{SW_I}, where the expected difference signal 834 represents the expected difference between the switching voltage output, V_{SW}, and the target voltage level of the power amplifier supply voltage, V_{CC}, based on the V_{RAMP} signal.

[00910] Because the Z_{OUT} compensation high pass filter 824 high pass filters the expected difference signal 834, the direct current content of the expected difference signal 834 is not present in the estimated high frequency ripple signal 836. The G_{CORR} scalar circuit 826 scales the estimated high frequency ripple signal 836 based on a scaling factor, G_{CORR}, to generate a high frequency ripple compensation signal 838. The high frequency ripple compensation signal 838 is added to the pre-filtered V_{RAMP} signal 814, $V_{RAMP_PRE\text{-}FILTERED}$, by the summing circuit 832 to generate the compensated V_{RAMP} signal, V_{RAMP_C}. The high frequency ripple compensation signal 838 is added to the pre-filtered V_{RAMP} signal 814, $V_{RAMP_PRE\text{-}FILTERED}$, to compensate for the non-ideal output impedance of the parallel amplifier 35. The compensated V_{RAMP} signal, V_{RAMP_C}, is provided as an input to the parallel amplifier 35. The parallel amplifier generates the parallel amplifier output voltage, V_{PARA_AMP}, based on the difference between the compensated V_{RAMP} signal, V_{RAMP_C}, and the power amplifier supply voltage, V_{CC}.

[00911] Generation of the scaling factor, G_{CORR}, will now be discussed. The second subtracting circuit 828 is configured to subtract the power amplifier supply voltage, V_{CC}, from the V_{RAMP} signal to provide a G_{CORR} feedback signal 840 that is received by the tune circuit 830. In some embodiments of the parallel amplifier output impedance compensation circuit 37B, the tune circuit 830 may be configured to dynamically provide the scaling factor, G_{CORR}, to the G_{CORR}

scalar circuit 826 based on the G_{CORR} feedback signal 840. As an example, the controller 50 may configure the tune circuit 830 to provide a different value of the scaling factor, G_{CORR}, on a block-by-block transmission basis dependent upon the operational mode of the linear radio frequency power amplifier 22. For example, the tune circuit 830 may be configured by the controller 50 during a calibration procedure to develop at least one G_{CORR} curve. In other embodiments, the tune circuit 830 may have multiple G_{CORR} curves that may be used to provide a scaling factor, G_{CORR}, based on the G_{CORR} feedback signal 840 and the operational mode of the linear radio frequency power amplifier 22. As an example, the controller 50 may configure the tune circuit 830 to use a particular one of the G_{CORR} curves depending on the configuration and/or operational mode of the pseudo-envelope follower power management system 10PA, the parallel amplifier 35, or a combination thereof. Each G_{CORR} curve may include several coefficients or values for the scaling factor, G_{CORR}, that correspond to the magnitude of the G_{CORR} feedback signal 840. In some embodiments, the controller 50 may select a G_{CORR} curve to be used on a block-by-block transmission basis depending on the operational mode of the linear radio frequency power amplifier 22.

[00912] For example, the controller 50 may select a first G_{CORR} curve to be used by the tune circuit 830 when the linear radio frequency power amplifier 22 is in a first operational mode. The controller 50 may select a second G_{CORR} curve to be used by the tune circuit 830 when the linear radio frequency power amplifier 22 is in a second operational mode. In still other embodiments of the parallel amplifier output impedance compensation circuit 37B, the tune circuit 830 may only have one G_{CORR} curve to be used by the tune circuit 830 to provide the scaling factor, G_{CORR}, to the G_{CORR} scalar circuit 826 based on the G_{CORR} feedback signal 840.

[00913] As an example, in some embodiments of the parallel amplifier output impedance compensation circuit 37B, the scaling factor, G_{CORR}, is tuned by the tune circuit 830 based on a built-in calibration sequence that occurs at power start-up. As an example, the controller 50 may configure the switch mode power

supply converter 802 to operate with a switching frequency that is a fixed frequency to create a switcher ripple current in the power inductor current, I_{SW_OUT}, of the power inductor 16 at a frequency of concern for the pseudo-envelope follower power management system 10PA. In those cases where the switch mode power supply converter 802 is configured as a multi-level charge pump buck converter, the controller 50 may configure the switch mode power supply converter 802 to operate in a "bang-bang mode" of operation. When operating in the "bang-bang mode" of operation, the controller 50 configures the switcher control circuit 804 such that the switch mode power supply converter 802 operates in a fashion similar to a buck converter. Thus, when operating in the "bang-bang mode" of operation, the switch mode power supply converter 802 switcher control circuit 804 does not permit the switch mode power supply converter 802 to provide a boosted output voltage at the switching voltage output 26.

[00914] As a non-limiting example, to tune the scaling factor, G_{CORR}, the controller 50 may configure the switch mode power supply converter 802 to operate at a calibration frequency with a fixed duty cycle in order to create a switcher ripple current at the calibration frequency. For example, the controller 50 may set the calibration frequency to 10MHz. The V_{RAMP} signal is set to a constant value in order to create a constant output value for the power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28. As discussed previously, the controller 50 may configure the switch mode power supply converter 802 to operate in a "bang-bang mode" of operation. The direct current voltage present at the power amplifier supply voltage, V_{CC}, may be primarily set by the duty cycle of the switch mode power supply converter 802. The direct current (DC) voltage may be mainly set by the duty cycle on the switching voltage output 26 of the switch mode power supply converter 802. The tune circuit 830 determines the peak-to-peak ripple voltage on the power amplifier supply voltage, V_{CC}, based on the G_{CORR} feedback signal 840. Based on the magnitude of the peak-to-peak ripple voltage on the power amplifier supply voltage, V_{CC}, the tune circuit 830 adjusts the value of the scaling factor,

G_{CORR}, until the peak-to-peak ripple voltage on the G_{CORR} feedback signal 840 is minimized. In some embodiments, to adjust the value of the scaling factor, G_{CORR}, based on the G_{CORR} feedback signal 840, the controller 50 may determine the degree of adjustment to provide based on the estimated power inductor inductance parameter, L_{EST}, the estimated bypass capacitor capacitance parameter, C_{BYPASS_EST}, and the estimated power amplifier transconductance parameter, $K_I_{OUT_EST}$, as previously described. Based on the scaling factor, G_{CORR}, that provides the minimum the peak-peak ripple voltage on the power amplifier supply voltage, V_{CC}, the tune circuit 830 selects the scaling factor, G_{CORR}, to be provided to the G_{CORR} scalar circuit 826. In some embodiments, the controller 50 may configure the switch mode power supply converter 802 to operate at various calibration frequencies to develop one or more G_{CORR} curves, where each G_{CORR} curve corresponds to an operational mode of the linear radio frequency power amplifier 22.

[00915] The determination of the scaling factor, G_{CORR}, and/or the development of the G_{CORR} curves is substantially orthogonal to the temporal alignment of the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$. Thus, following calibration of the tune circuit 830 to provide the scaling factor, G_{CORR}, appropriate for the operational mode of the linear radio frequency power amplifier 22, the controller 50 may be further configure to adjust the alignment period, $T_{ALIGNMENT}$, associated with the programmable delay circuitry 806 to temporally align the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, in order to further minimize the peak-to-peak ripple voltage on the power amplifier supply voltage, V_{CC}. Thus, after the controller 50 completes the calibration of the tune circuit 830 to minimize the peak-to-peak ripple voltage on the power amplifier supply voltage, V_{CC}, the controller 50 may configure the programmable delay circuitry 806 to iteratively adjust the alignment period, $T_{ALIGNMENT}$, provided by the programmable delay circuitry 806 to further minimize the peak-to-peak ripple voltage on the power amplifier supply voltage, V_{CC}. In some embodiments, the controller 50 may determine the alignment period, to be

provided by the programmable delay circuitry 806, for different operational modes of the linear radio frequency power amplifier 22.

[00916] Figure 34B depicts another example embodiment of a pseudo-envelope follower power management system 10PB that is similar in form and function to the pseudo-envelope follower power management system 10PA, depicted in Figure 34A. However, unlike the pseudo-envelope follower power management system 10PA, the pseudo-envelope follower power management system 10PB includes a parallel amplifier output impedance compensation circuit 37C that is divided between a parallel amplifier circuit 14PB and the digital baseband processing portion of a transceiver or modem. The example embodiment of the parallel amplifier output impedance compensation circuit 37C is similar in form and function to the parallel amplifier output impedance compensation circuit 37B, depicted in Figure 34A, except the scaling factor, G_{CORR}, is provided by a G_{CORR} function circuit 842 instead of the tune circuit 830, depicted in Figure 35A.

[00917] The G_{CORR} function circuit 842 is configured to receive the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, generated by the parallel amplifier sense circuit 36 of the parallel amplifier circuitry 32. The value of the scaling factor, G_{CORR}, may be based on a G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, where the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, characterizes values of the scaling factor, G_{CORR}, as a function of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. In some embodiments, the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, may be a polynomial function. In other embodiments, the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, may be a linear function. For example, the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, may have G_{CORR} scaling function coefficients that may be configurable by the controller 50 via the control bus 44. As a non-limiting example, equation (18) provides an example of the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, having two G_{CORR} scaling function coefficients. For example, the G_{CORR} scaling function coefficients may include a first G_{CORR} scaling function coefficient, $G_{CORR}(0)$, and a second G_{CORR} scaling function coefficient,

$G_{CORR}(1)$, where the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, is a linear function characterized by equation (18) as follows:

$$G_{CORR}(I_{PARA_AMP_SENSE}) = G_{CORR}(0) + G_{CORR}(1) \times I_{PARA_AMP_SENSE} \quad (18)$$

[00918] The first G_{CORR} scaling function coefficient, $G_{CORR}(0)$, may represent a scaling factor that is independent of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the second G_{CORR} scaling function coefficient, $G_{CORR}(1)$, represents a first order coefficient of the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, that captures the dependency of the scaling factor, G_{CORR}, on the change of value of the parallel amplifier inductance, L_{CORR}, as a function of the parallel amplifier output current, I_{PARA_AMP}. For example, in some embodiments, the second G_{CORR} scaling function coefficient, $G_{CORR}(1)$ may be based on the parallel amplifier inductance estimate parameter, L_{CORR_EST}, where the parallel amplifier inductance estimate parameter, L_{CORR_EST}, is an estimated inductance of the parallel amplifier 35 between the frequencies 10 MHz and 30 MHz.

[00919] In addition, because the parallel amplifier output current, I_{PARA_AMP}, may change depending upon the operational mode of the linear radio frequency power amplifier 22, the values of the first G_{CORR} scaling function coefficient, $G_{CORR}(0)$, and the value of the second G_{CORR} scaling function coefficient, $G_{CORR}(1)$, may be calibrated for each mode of operation of the linear radio frequency power amplifier 22. As an example, the G_{CORR} function circuit 842 may include a first set of G_{CORR} scaling function coefficients that correspond to a first LTE band number and a second set of G_{CORR} scaling function coefficients that correspond to a second LTE band number. In other words, the controller 50 may configure the G_{CORR} function circuit 842 to adaptively determine the G_{CORR} scaling function coefficients to be used to characterize the G_{CORR} scaling function, $G_{CORR}(I_{PARA_AMP_SENSE})$, based upon the operational mode of the pseudo-envelope follower power management system 10PB and/or the band of operation at which the linear radio frequency power amplifier 22 is transmitting.

[00920] In some alternative embodiments, the G_{CORR} function circuit 842 may be configured by the controller 50 to provide a fixed value of the scaling factor, G_{CORR}, as depicted in equation (19) as follows:

(19) $$G_{CORR} = \frac{L_{CORR_EST}}{L_{EST}}$$

[00921] where the estimated power inductor inductance parameter, L_{EST}, represents the measured or estimated inductance of the power inductor 16 between a specific range of frequencies and the parallel amplifier inductance estimate parameter, L_{CORR_EST}, estimates the inductance of the parallel amplifier 35 between a specific range of frequencies, as discussed above.

[00922] Figure 34C depicts an example embodiment of a pseudo-envelope follower power management system 10PC that is similar in form and function to the pseudo-envelope follower power management system 10PA, depicted in Figure 34A. However, unlike the pseudo-envelope follower power management system 10PA, depicted in Figure 34A, the pseudo-envelope follower power management system 10PC includes a parallel amplifier circuit 14PC that includes a parallel amplifier output impedance compensation circuit 37D. Unlike the parallel amplifier output impedance compensation circuit 37B of the pseudo-envelope follower power management system 10PA, depicted in Figure 34A, the parallel amplifier output impedance compensation circuit 37D, depicted in Figure 34C, includes an analog V_{RAMP} pre-distortion filter circuit 844 configured to receive the V_{RAMP} signal in the analog domain. Similar to the digital V_{RAMP} pre-distortion filter circuit 812, depicted in Figure 34A, the analog V_{RAMP} pre-distortion filter circuit 844 pre-distorts the V_{RAMP} signal in the frequency domain to generate an analog pre-filtered V_{RAMP} signal 814A, $V_{RAMP_ANALOG_PRE\text{-}FILTERED}$. The controller 50 may configure the analog V_{RAMP} pre-distortion filter circuit 844 to filter the V_{RAMP} signal such that the analog pre-filtered V_{RAMP} signal 814A, $V_{RAMP_ANALOG_PRE\text{-}FILTERED}$, may be used to equalize the response of the pseudo-envelope follower power management system 10PC and compensate for the bypass capacitance, C_{BYPASS}, of the bypass capacitor 19, the power amplifier

associated inductance, L_{PA}, (not shown), the power amplifier filter associated capacitance, C_{PA}, (not shown), and the frequency response of the transfer function of the parallel amplifier 35.

[00923] As a non-limiting example, the analog V_{RAMP} pre-distortion filter circuit 844 may include programmable time constants that may be configured by the controller 50. The controller 50 may configure the frequency response of the analog V_{RAMP} pre-distortion filter circuit 844 to equalize the response of the pseudo-envelope follower power management system 10PA by adjusting the value of the programmable time constants.

[00924] In some embodiments of the parallel amplifier circuit 14PC, the analog V_{RAMP} pre-distortion filter circuit 844 may be configured to compensate for the transfer function of the parallel amplifier 35 in conjunction with the power amplifier filter associated capacitance, C_{PA}, the power amplifier associated inductance, L_{PA}, (not shown), and the bypass capacitance, C_{BYPASS}, of the bypass capacitor 19. For example, the controller 50 may configure the analog V_{RAMP} pre-distortion filter circuit 844 to provide frequency peaking to compensate for the low pass filter response due to the combination of the power amplifier associated inductance, L_{PA}, (not shown) and the power amplifier associated capacitance, C_{PA}, (not shown) associated with the linear radio frequency power amplifier 22. In some embodiments, the Laplace transfer function of the analog V_{RAMP} pre-distortion filter circuit 844 may be represented by equation (20), as follows:

$$(20) \qquad H(s)_{\text{Analog Pre-Distortion Filter Circuit}} = \frac{(1+\tau_{ZERO_PRE}s)}{(1+\tau_{POLE_PRE}s)}$$

[00925] where, τ_{ZERO_PRE} is a first time constant associated with a real-zero in the Laplace transfer function of the analog V_{RAMP} pre-distortion filter circuit 844, and τ_{POLE_PRE} is a second time constant associated with real-pole in the Laplace transfer function of the analog V_{RAMP} pre-distortion filter circuit 844. The first time constant, τ_{ZERO_PRE}, and the second time constant, τ_{POLE_PRE}, may be configured

by the controller 50 to pre-distort the V_{RAMP} signal prior to adding the high frequency ripple compensation signal 838 to compensate for the non-ideal parallel amplifier output impedance of the parallel amplifier 35. The controller 50 may configure the first time constant, τ_{ZERO_PRE}, and the second time constant, τ_{POLE_PRE}, of the analog V_{RAMP} pre-distortion filter circuit 844 based on the radio frequency modulation bandwidth of the linear radio frequency power amplifier 22 associated with a wide-bandwidth modulation of a mode of operation of a communication device that includes the pseudo-envelope follower power management system 10PC. As an example, the controller 50 may configure the first time constant, τ_{ZERO_PRE}, and second time constant, τ_{POLE_PRE}, to provide peaking of the V_{RAMP} signal in order to flatten the overall modulation frequency response of the pseudo-envelope follower power management system 10PC based on the wide-bandwidth modulation of a mode of operation of a communication device.

[00926] As another example, the controller 50 may configure the analog V_{RAMP} pre-distortion filter circuit 844 to pre-distort the frequency response of the V_{RAMP} signal such that the overall transfer function between the first control input 34, which receives the V_{RAMP} signal, and the power amplifier collector 22A of the linear radio frequency power amplifier 22 is substantially flat through the operating frequency range of the linear radio frequency power amplifier 22. As a non-limiting example, the controller 50 may configure first time constant, τ_{ZERO_PRE}, to place a real-zero at around 11 MHz and the second time constant, τ_{POLE_PRE}, to locate a real-pole at around 20 MHz. Accordingly, the analog V_{RAMP} pre-distortion filter circuit 844 may be configured to provide a peaking response in order to compensate for the frequency response of the pseudo-envelope follower power management system 10PC and the low pass filter effects of the combination of the power amplifier associated inductance, L_{PA}, (not shown), and the power amplifier filter associated capacitance, C_{PA}, (not shown).

[00927] Otherwise, similar to the parallel amplifier output impedance compensation circuit 37B, depicted in Figure 34A, the parallel amplifier output impedance compensation circuit 37D, depicted in Figure 34C, may include an

estimated switching voltage output selection switch 816, S_1, having a first input 816A configured to receive the estimated switching voltage output 38B, V_{SW_EST}, a second input 816B configured to receive the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, and an estimated switching voltage output selection switch output 816C. The controller 50 may configure the estimated switching voltage output selection switch 816, S_1, to provide either the estimated switching voltage output 38B, V_{SW_EST}, or the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, as an estimated switching voltage input signal 820, V_{SW_I}, at the estimated switching voltage output selection switch output 816C.

[00928] The parallel amplifier output impedance compensation circuit 37D also includes the first subtracting circuit 822, the Z_{OUT} compensation high pass filter 824, the G_{CORR} scalar circuit 826, the second subtracting circuit 828, the tune circuit 830, and the summing circuit 832. The first subtracting circuit 822 is configured to subtract the estimated switching voltage input signal 820, V_{SW_I}, from the V_{RAMP} signal to generate an expected difference signal 834, which is provided to the Z_{OUT} compensation high pass filter 824. As discussed previously, the controller 50 may configure the programmable time constants associated with the Z_{OUT} compensation high pass filter 824 to high pass filter the expected difference signal 834 in order to generate an estimated high frequency ripple signal 836.

[00929] Alternatively, the controller 50 may configure the estimated switching voltage output selection switch 816, S_1, to provide the estimated switching voltage output 38B, V_{SW_EST}, as the estimated switching voltage input signal 820, V_{SW_I}, to the Z_{OUT} compensation high pass filter 824. In this case, the Z_{OUT} compensation high pass filter 824 high pass filters the expected difference signal 834 to generate the estimated high frequency ripple signal 836. As such, the estimated high frequency ripple signal 836 substantially corresponds to a scaled derivative of a switcher ripple current in the power inductor current, I_{SW_OUT}, of the power inductor 16 based on the estimated switching voltage output 38B, V_{SW_EST}. Similar to the parallel amplifier output impedance

compensation circuit 37B, when the controller configures the estimated switching voltage output selection switch 816, S_1, to provide the estimated switching voltage output 38B, V_{SW_EST}, as the estimated switching voltage input signal 820, V_{SW_I}, the controller does not have the ability to adjust temporal alignment of the estimated switching voltage output 38B, V_{SW_EST}, with the V_{RAMP} signal in order to minimize the peak-to-peak ripple voltage on the power amplifier supply voltage, V_{CC}, due to the non-ideal output impedance of the parallel amplifier 35.

[00930] In contrast, when the controller 50 configures the estimated switching voltage output selection switch 816, S_1, to provide the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, as the estimated switching voltage input signal 820, V_{SW_I}, the controller 50 may adjust the delay provided by the programmable delay circuitry 806 to temporally align the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, with the V_{RAMP} signal.

[00931] The Z_{OUT} compensation high pass filter 824 high pass filters the expected difference signal 834 to generate an estimated high frequency ripple signal 836 that may be scaled by the G_{CORR} scalar circuit 826 to create the high frequency ripple compensation signal 838. The high frequency ripple compensation signal 838 is added to the analog pre-filtered V_{RAMP} signal 814A, $V_{RAMP_ANALOG_PRE\text{-}FILTERED}$, to form the compensated V_{RAMP} signal, V_{RAMP_C}. The compensated V_{RAMP} signal, V_{RAMP_C}, is provided as an input to the parallel amplifier 35. The parallel amplifier generates the parallel amplifier output voltage, V_{PARA_AMP}, based on the difference between the compensated V_{RAMP} signal, V_{RAMP_C}, and the power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28.

[00932] The operation, configuration, and calibration of the tune circuit 830 of the parallel amplifier output impedance compensation circuit 37D, depicted in Figure 34C, is substantially similar to the operation of the tune circuit 830 previously described with respect to the embodiment of the parallel amplifier output impedance compensation circuit 37B, depicted in Figure 34A. As such, a detailed description of the operation of the tune circuit 830 herein is omitted.

[00933] Figure 34D depicts an example embodiment of a pseudo-envelope follower power management system 10PD that is similar to the pseudo-envelope follower power management system 10PC, depicted in Figure 34C. However, the pseudo-envelope follower power management system 10PD includes a parallel amplifier circuit 14PD. The parallel amplifier circuit 14PD includes a parallel amplifier output impedance compensation circuit 37E configured to provide the compensated V_{RAMP} signal, V_{RAMP_C} to the parallel amplifier 35. Similar to the parallel amplifier output impedance compensation circuit 37D, depicted in Figure 34C, the parallel amplifier output impedance compensation circuit 37E includes an analog V_{RAMP} pre-distortion filter circuit 844 configured to receive the V_{RAMP} signal in the analog domain. In addition, as previously described with respect to the analog V_{RAMP} pre-distortion filter circuit 844, the controller 50 may configure the frequency response of the analog V_{RAMP} pre-distortion filter circuit 844 to pre-distort the received the V_{RAMP} signal.

[00934] Illustratively, as described before, the first time constant, τ_{ZERO_PRE}, and second time constant, τ_{POLE_PRE}, may be adjusted by controller 50 to provide peaking of the V_{RAMP} signal in order to equalize the overall frequency response between the first control input 34, which received the V_{RAMP} signal, and the power amplifier collector 22A of a linear radio frequency power amplifier 22. The controller 50 may configure the frequency response of the analog V_{RAMP} pre-distortion filter circuit 844 to equalize the response of the pseudo-envelope follower power management system 10PA by adjusting the value of the programmable time constants of the analog V_{RAMP} pre-distortion filter circuit 844, as previously described. In addition, similar to the parallel amplifier output impedance compensation circuit 37D, the controller 50 may configure the analog V_{RAMP} pre-distortion filter circuit 844 of the parallel amplifier output impedance compensation circuit 37E to pre-distort the frequency response of the V_{RAMP} signal such that the overall transfer function between the first control input 34, which received the V_{RAMP} signal, and the power amplifier collector 22A of a linear radio frequency power amplifier 22 is substantially flat through the operating frequency range of the linear radio frequency power amplifier 22. For example,

as described above, the controller 50 may configure the analog V_{RAMP} pre-distortion filter circuit 844 to provide frequency peaking to compensate for the low pass filter response due to the combination of the power amplifier associated inductance, L_{PA}, (not shown) and the power amplifier associated capacitance, C_{PA}, (not shown) associated with the linear radio frequency power amplifier 22.

[00935] However, unlike the parallel amplifier output impedance compensation circuit 37D, depicted in Figure 34C, the parallel amplifier output impedance compensation circuit 37E, depicted in Figure 34D, is configured to provide a high frequency ripple compensation signal 838 to generate the compensated V_{RAMP} signal, V_{RAMP_C}, in a fashion that is similar to the parallel amplifier output impedance compensation circuit 37C, depicted in Figure 34B, where the scaling factor, G_{CORR}, is provided by the G_{CORR} function circuit 842. Thus, similar to the parallel amplifier output impedance compensation circuit 37C, depicted in Figure 34B, the parallel amplifier output impedance compensation circuit 37E includes a G_{CORR} function circuit 842 configured to provide the scaling factor, G_{CORR}, to the G_{CORR} scalar circuit 826. The form and function of the G_{CORR} function circuit 842 of the parallel amplifier output impedance compensation circuit 37E is similar to the operation of the G_{CORR} function circuit 842 of parallel amplifier output impedance compensation circuit 37C, depicted in Figure 34B.

[00936] Accordingly, the parallel amplifier output impedance compensation circuit 37E, may include an estimated switching voltage output selection switch 816, S_1, having a first input 816A configured to receive the estimated switching voltage output 38B, V_{SW_EST}, a second input 816B configured to receive the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, and an estimated switching voltage output selection switch output 816C. The controller 50 may configure the estimated switching voltage output selection switch 816. S_1, to provide either the estimated switching voltage output 38B, V_{SW_EST}, or the second input configured to receive the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, as a estimated switching voltage input signal 820, V_{SW_I}, at the estimated switching voltage output selection switch output 816C. As discussed above, if the controller 50 configures the estimated

switching voltage output selection switch 816, S_1, to provide the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, the controller 50 may configure the delay provided by the programmable delay circuitry 806 to temporally optimize the relationship between estimated switching voltage input signal 820, V_{SW_I}, and the V_{RAMP} signal to minimize the high frequency voltage ripple generated as a result of the non-ideal output impedance characteristics of the parallel amplifier 35.

[00937] Similar to the parallel amplifier output impedance compensation circuit 37C, the parallel amplifier output impedance compensation circuit 37E also includes the first subtracting circuit 822, Z_{OUT} compensation high pass filter 824, the G_{CORR} scalar circuit 826, and the summing circuit 832. The first subtracting circuit 822 is configured to subtract the estimated switching voltage input signal 820, V_{SW_I}, from the V_{RAMP} signal to generate an expected difference signal 834, which is provided to the Z_{OUT} compensation high pass filter 824. Similar to the operation of the parallel amplifier output impedance compensation circuit 37D, depicted in Figure 34C, the controller 50 may configure the programmable time constants associated with of the Z_{OUT} compensation high pass filter 824 to high pass filter the expected difference signal 834 in order to generate an estimated high frequency ripple signal 836, which is scaled by G_{CORR} scalar circuit 826 to create the high frequency ripple compensation signal 838.

[00938] Unlike the parallel amplifier output impedance compensation circuit 37D, depicted in Figure 34C, the parallel amplifier output impedance compensation circuit 37E, depicted in Figure 34D, provides the scaling factor, G_{CORR}, to the G_{CORR} scalar circuit 826 from the G_{CORR} function circuit 842. The G_{CORR} function circuit 842 of the parallel amplifier output impedance compensation circuit 37E, depicted in Figure 34D, is similar in form and function to the G_{CORR} function circuit 842 of the parallel amplifier output impedance compensation circuit 37C, depicted in Figure 34B. For example, the G_{CORR} function circuit 842 of the parallel amplifier output impedance compensation circuit 37E may be configured to receive the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, generated by the parallel amplifier sense

circuit 36 of the parallel amplifier circuitry 32. In some embodiments of the parallel amplifier output impedance compensation circuit 37E, the G_{CORR} function circuit 842 provides the scaling factor, G_{CORR}, to the G_{CORR} scalar circuit 826 as a function of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, as previously described with respect to the parallel amplifier output impedance compensation circuit 37C, depicted in Figure 34B. Alternatively, in some embodiments of the parallel amplifier output impedance compensation circuit 37E, the G_{CORR} function circuit 842 may be configured by the controller 50 to provide the scaling factor, G_{CORR}, based on the ratio of the parallel amplifier inductance estimate parameter, L_{CORR_EST}, to the estimated power inductor inductance parameter, L_{EST}, of the pseudo-envelope follower power management system 10PD, as described in equation (19), which is described above.

[00939] Alternatively, in some embodiments of the parallel amplifier output impedance compensation circuit 37E, controller 50 characterizes the G_{CORR} function circuit 842 during either calibration of the pseudo-envelope follower power management system 10PD as described relative to the parallel amplifier output impedance compensation circuit 37C depicted in Figure 34B, the details of which are omitted here for the sake of brevity.

[00940] Figure 34E depicts an example embodiment of a pseudo-envelope follower power management system 10PE that is similar to the pseudo-envelope follower power management system 10PD, depicted in Figure 34D. However, the pseudo-envelope follower power management system 10PE includes a parallel amplifier circuit 14PE. The parallel amplifier circuit 14PE includes a parallel amplifier output impedance compensation circuit 37F that is similar to the parallel amplifier output impedance compensation circuit 37E. However, unlike the parallel amplifier output impedance compensation circuit 37E, depicted in Figure 34D, the parallel amplifier output impedance compensation circuit 37F, depicted in Figure 34E, applies a parallel output impedance correction signal 838A to the V_{RAMP} signal prior to applying equalization of the input signal provided to the parallel amplifier 35.

[00941] Similar to the parallel amplifier output impedance compensation circuit 37E, depicted in Figure 34D, the parallel amplifier output impedance compensation circuit 37E, depicted in Figure 34F, may include an estimated switching voltage output selection switch 816, S_1, having a first input 816A configured to receive the estimated switching voltage output 38B, V_{SW_EST}, a second input 816B configured to receive the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$. The controller 50 may configure the estimated switching voltage output selection switch 816, S_1, to provide either the estimated switching voltage output 38B, V_{SW_EST}, or the delayed estimated switching voltage output 38D, $V_{SW_EST_DELAYED}$, as the estimated switching voltage input signal 820, V_{SW_I}, to the first subtracting circuit 822. The first subtracting circuit 822 is configured to subtract the estimated switching voltage input signal 820, V_{SW_I}, from the V_{RAMP} signal to generate an expected difference signal 834, which is provided to the Z_{OUT} compensation high pass filter 824. As previously described, the controller 50 may configure the programmable time constants associated with of the Z_{OUT} compensation high pass filter 824 to high pass filter the expected difference signal 834 in order to generate an estimated high frequency ripple signal 836. The estimated high frequency ripple signal 836 is then scaled by the G_{CORR} scalar circuit 826 based on the scaling factor, G_{CORR}, received from the G_{CORR} function circuit 842 to generate the high frequency ripple compensation signal 838A. The operation and configuration of the G_{CORR} function circuit 842, depicted in Figure 34E, is similar in form and function as the G_{CORR} function circuit 842, previously described and depicted in Figure 34B and Figure 34D, and therefore a detailed description of the calibration, function and operation of the G_{CORR} function circuit 842 is here omitted.

[00942] Unlike the previously described embodiments of the parallel amplifier output impedance compensation circuits 37B-E, depicted in Figure 34A-D, the parallel amplifier output impedance compensation circuit 37F, depicted in Figure 34E, includes a pre-distortion subtraction circuit 846 configured to subtract the high frequency ripple compensation signal 838A from the V_{RAMP} signal prior to pre-distorting the V_{RAMP} signal to form a non-filtered parallel amplifier output

impedance compensated signal 848. The non-filtered parallel amplifier output impedance compensated signal 848 represents a V_{RAMP} signal that has been compensated to take into consideration the non-ideal output impedance characteristics of the parallel amplifier 35. The parallel amplifier output impedance compensation circuit 37F further includes a V_{RAMP} post-distortion filter circuit 850 configured to filter the non-filtered parallel amplifier output impedance compensated signal 848 to generate the compensated V_{RAMP} signal, V_{RAMP_C}.

[00943] The V_{RAMP} post-distortion filter circuit 850 may have a Laplace transfer function similar to the transfer function described by equation (21), as follows:

$$(21) \qquad H(s)_{V_{RAMP}\ \text{Post-Distortion Filter Circuit}} = \frac{(1+\tau_{ZERO_POST}s)}{(1+\tau_{POLE_POST}s)}$$

[00944] where, τ_{ZERO_POST}, is a first post distortion time constant associated with zero in the V_{RAMP} post-distortion filter circuit 850 and, τ_{POLE_POST}, is a second post distortion time constant associated with pole of the V_{RAMP} post-distortion filter circuit 850. The first post distortion time constant, τ_{ZERO_POST}, and the second post distortion time constant, τ_{POLE_POST}, may be configured to distort the non-filtered parallel amplifier output impedance compensated signal 848 to equalize the overall modulation frequency response of the pseudo-envelope follower power management system 10PE. As an example, similar to the analog V_{RAMP} pre-distortion filter circuit 844, depicted in Figure 34C and Figure 34D, the controller 50 may be configured to adjust the first post distortion time constant, τ_{ZERO_POST}, and the post distortion time constant, τ_{POLE_POST}, to provide peaking of the non-filtered parallel amplifier output impedance compensated signal 848 in order to equalize the overall modulation frequency response of the pseudo-envelope follower power management system 10PE, depicted in Figure 34E, as well as the low pass filtering characteristics of the combination of the power amplifier associated inductance, L_{PA}, (not shown), and the power amplifier filter associated capacitance, C_{PA}, (not shown). The controller 50 may configure of the first post distortion time constant, τ_{ZERO_POST}, and the second post distortion

time constant, τ_{POLE_POST}, such that the transfer function of the V_{RAMP} post-distortion filter circuit 850 is based on the radio frequency modulation bandwidth of the linear radio frequency power amplifier 22 associated with a wide-bandwidth modulation of a mode of operation of electronic device or mobile terminal that includes the pseudo-envelope follower power management system 10PE. As an example, the controller 50 may configure the first post distortion time constant, τ_{ZERO_PRE}, and second post distortion time constant, τ_{POLE_POST}, to provide peaking of the non-filtered parallel amplifier output impedance compensated signal 848 in order to flatten the overall modulation frequency response of the pseudo-envelope follower power management system 10PC based on the wide-bandwidth modulation of a mode of operation of electronic device or mobile terminal.

[00945] Figure 38A depicts an embodiment of a pseudo-envelope follower power management system 10QA. As a non-limiting example, the pseudo-envelope follower power management system 10QA includes a multi-level charge pump buck converter 12Q, a parallel amplifier circuit 14Q, the power inductor 16, the coupling circuit 18, the bypass capacitor 19, and the power amplifier supply output 28. Similar to the previously described embodiments of the pseudo-envelope follower power management systems, the multi-level charge pump buck converter 12Q and the parallel amplifier circuit 14QA of the embodiment of a pseudo-envelope follower power management system 10QA may be configured to operate in tandem with the power inductor 16, the coupling circuit 18, and the bypass capacitor 19 to generate a power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28 of the for a linear radio frequency power amplifier 22. The power inductor 16 is coupled between the switching voltage output 26 and the power amplifier supply output 28. The bypass capacitor 19 is coupled between the power amplifier supply output 28 and ground. In addition, the parallel amplifier circuit 14Q may be coupled to the battery 20 and the controller 50. The parallel amplifier circuit 14Q may include a parallel amplifier output 32A and be configured to receive the power amplifier supply voltage, V_{CC}, as a feedback voltage. The coupling circuit 18 may be

coupled between the parallel amplifier output 32A and the power amplifier supply output 28. In addition, the parallel amplifier circuit 14Q may be configured to regulate the power amplifier supply voltage, V_{CC}, based on the difference between the V_{RAMP} signal and the power amplifier supply voltage, V_{CC}. Likewise, as an example, the parallel amplifier circuit 14Q may be configured to provide the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the multi-level charge pump buck converter 12Q as feedback signals to govern the operation of the multi-level charge pump buck converter 12Q.

[00946] As an example, in the pseudo-envelope follower power management system 10QA depicted in Figure 38A, the parallel amplifier circuit 14Q acts as a master to control the power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28 while controlling the multi-level charge pump buck converter 12Q. The parallel amplifier circuit 14Q regulates the power amplifier supply voltage, V_{CC}, by sourcing and sinking current through the coupling circuit 18, based on the received V_{RAMP} signal, to compensate for either the over or under generation of the power inductor current, I_{SW_OUT}, provided from the power inductor 16 due to changes in the switching voltage, V_{SW}, provided at the switching voltage output 26 of the multi-level charge pump buck converter 12Q. The parallel amplifier circuit 14Q controls the changes in the switching voltage, V_{SW}, provided at the switching voltage output 26 based on the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, provided to the multi-level charge pump buck converter 12Q as feedback signals. The parallel amplifier circuit 14Q may include a parallel amplifier circuit delay. The parallel amplifier circuit delay is the period of time in the V_{RAMP} processing path between the first control input 34 and the power amplifier supply output 28. As an example, the parallel amplifier circuit delay of the embodiment of the parallel amplifier circuit 14Q depicted in Figure 38A may include the period of time between the V_{RAMP} signal arriving at the first control input 34 and a change in the value of the power amplifier supply voltage, V_{CC}, generated by the parallel amplifier circuit 14Q in response to the

V_{RAMP} signal arriving at the first control input 34. The parallel amplifier circuit delay may be due to the internal propagation of the V_{RAMP} signal through the parallel amplifier 35 and/or portions of the parallel amplifier circuitry 32 and pre-processing circuitry. Pre-processing delay associated with pre-processing circuitry may include the propagation delay between the first control input 34 and input of the parallel amplifier 35. As an example, depicted in Figure 34C, the pre-processing delay associated with the V_{RAMP} signal may include the propagation or signal processing delay associated with the analog V_{RAMP} pre-distortion filter circuit 844 and the summing circuit 832. In addition, the feedback delay may vary depending on the operational state of the parallel amplifier circuit 14Q.

[00947] Returning to Figure 38A, the pseudo-envelope follower power management system 10QA may include delays that can affect the operation of the switcher control circuit 52 and cause increases in the magnitude of the parallel amplifier output current, I_{PARA_AMP}, provided by the parallel amplifier 35. The delays in the pseudo-envelope follower power management system 10QA may result in the parallel amplifier 35 either sourcing or sinking additional current to regulate the power amplifier supply voltage, V_{CC}. The increase in magnitude of the parallel amplifier output current, I_{PARA_AMP}, provided by the parallel amplifier 35, may contribute to reduced power efficiency.

[00948] As a non-limiting example, in some cases, the delays may be internal to the switcher control circuit 52. In other cases, the delays that reduce the power efficiency of the pseudo-envelope follower power management system 10QA may be related to feedback delays. One example of feedback delay is the time period associated with generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, which is also referred to as a parallel amplifier feedback delay. For example, the parallel amplifier circuit 14Q may configure the parallel amplifier sense circuit 36 to generate the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. The parallel amplifier circuit 14Q may use the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, to provide at least a portion of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. The parallel amplifier circuit output current

estimate 40, $I_{PAWA_OUT_EST}$, is provided as a feedback signal to the multi-level charge pump buck converter 12Q such that the parallel amplifier circuit 14Q may control changes in the switching voltage, V_{SW}, based on the magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, in order to minimize the magnitude of the parallel amplifier output current, I_{PARA_AMP}, provided by the parallel amplifier 35. The feedback delay associated with generating and providing the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, to the switcher control circuit 52 may delay the response of the multi-level charge pump buck converter 12Q to changes in the V_{RAMP} signal. As a result, the response of the multi-level charge pump buck converter 12Q to a change in the V_{RAMP} signal may be delayed such that the power inductor current provided from the power inductor 16 may not correlate to the change in the target voltage level of the power amplifier supply voltage V_{CC}, which is represented by the V_{RAMP} signal. As a result, the parallel amplifier output current, I_{PARA_AMP}, sourced or sunk by the parallel amplifier 35 may be increased due to the feedback delay associated with generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, due to the lag in the response time of the multi-level charge pump buck converter 12Q. By minimizing the magnitude of the parallel amplifier output current, I_{PARA_AMP}, provided by the parallel amplifier 35, the power efficiency of the pseudo-envelope follower power management system 10QA may be improved.

[00949] As another example, in the case where the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, also includes contributions from the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, as depicted in Figure 23A, and/or the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}, as depicted in Figure 23C, delays associated with the generation of the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and/or the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}, may also contribute to the reduced power efficiency of the pseudo-envelope follower power management system 10QA. Thus, the parallel amplifier circuit 14Q may have a parallel amplifier circuit feedback delay

associated with generation of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, which is an estimate of the parallel amplifier circuit output current, I_{PAWA_OUT}.

[00950] In order to compensate for the delays in the pseudo-envelope follower power management system 10QA that may contribute to reduced power efficiency, the example embodiment of the pseudo-envelope follower power management system 10QA depicted in Figure 38A further includes a feedback delay compensation circuit 852 configured to minimize the negative impact of feedback delay on the power conversion efficiency of the pseudo-envelope follower power management system 10QA.

[00951] In some embodiments of the pseudo-envelope follower power management system 10QA, the feedback delay compensation circuit 852 may be incorporated into the multi-level charge pump buck converter 12Q. For the sake of simplicity of description of operation of the feedback delay compensation circuit 852, and not by way of limitation, the operation and functionality of the multi-level charge pump buck converter 12Q may be similar to the operation and function of either the multi-level charge pump buck converter 12A, depicted in Figure 2A, or the multi-level charge pump buck converter 12B, depicted in Figure 2B. Also, for the sake of simplicity of description of the feedback delay compensation circuit 852, and not by way of limitation, neither the feed forward control signal 38, $V_{SWITCHER}$, nor the estimated switching voltage output 38B, V_{SW_EST}, are depicted in Figure 38A.

[00952] In addition, some embodiments of the parallel amplifier circuit 14Q may include the parallel amplifier circuitry 32 and the V_{OFFSET} loop circuit 41. For example, some embodiments of the parallel amplifier circuit 14Q may include an embodiment of the V_{OFFSET} loop circuit 41 similar to the embodiment of the V_{OFFSET} loop circuit 41 depicted in Figure 8, the V_{OFFSET} loop circuit 41A depicted in Figure 18A, or the V_{OFFSET} loop circuit 41B depicted in Figure 18B. However, as will be discussed, some embodiments of the parallel amplifier circuit 14Q do not include an embodiment of the V_{OFFSET} loop circuit 41. In addition, although not depicted for the sake of simplicity, some embodiments of the parallel

amplifier circuit 14Q depicted in Figure 38A may include an embodiment of the parallel amplifier output impedance compensation circuit 37, an embodiment of the open loop assist circuit 39, similar to the open loop assist circuit 39A, depicted in Figure 9A, or the open loop assist circuit 39B, depicted in Figure 9B, and/or an embodiment of the open loop ripple compensation assist circuit 414 similar to the open loop ripple compensation assist circuit 414A, depicted in Figure 24, the open loop ripple compensation assist circuit 414B, depicted in Figure 27A, the open loop ripple compensation assist circuit 414C, depicted in Figure 27B, and/or a combination thereof, as previously described.

[00953] While Figure 38A depicts that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, provided to the multi-level charge pump buck converter 12Q only includes the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, this is by way of example and not by limitation. Accordingly, as an example, some embodiments of the parallel amplifier circuit 14Q may provide a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, that includes the summation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, as depicted in Figure 23A. Likewise, as another example, some embodiments of the parallel amplifier circuit 14Q may provide a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, that includes the summation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}, as depicted in Figure 23C. In addition, as depicted in Figure 2A and Figure 2B, some embodiments of the parallel amplifier circuit 14Q may provide a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, that includes the summation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE}, as depicted in Figure 23C.

[00954] For example, and not by way of limitation, the pseudo-envelope follower power management system 10QA may be configured similar in form and

function to some of the other embodiments of the pseudo-envelope follower power management systems, described above, that include a multi-level charge pump buck converter. As a non-limiting example, some embodiments of the multi-level charge pump buck converter 12Q may be configured, in form and function, similar to multi-level charge pump buck converter and operate similar to the multi-level charge pump buck converters 12, 12A, 12B, 12C, 12H, 12I, 12J, 12L, and 12M, depicted in Figures 1A-B, Figures 2A-B, Figures 18A-B, Figure 14, Figure 15, Figure 16, Figure 17B, Figure 23A, and Figure 23C, except, the multi-level charge pump buck converter 12Q is further configured to receive a feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, from the feedback delay compensation circuit 852. In some embodiments of the pseudo-envelope follower power management system 10QA, the feedback delay compensation circuit 852 may be incorporated into the multi-level charge pump buck converter 12Q. However, for the sake of simplicity of description, and not by way of limitation, the feedback delay compensation circuit 852, depicted in Figure 38A, is shown as being separate from the multi-level charge pump buck converter 12Q.

[00955] Returning to the description of the feedback delay compensation circuit 852 depicted in Figure 38A, some example embodiments of the feedback delay compensation circuit 852 may provide a feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to the multi-level charge pump buck converter 12Q. As depicted in Figure 38A, the switcher control circuit 52 may be configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The switcher control circuit 52 may be further configured to use the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to govern the operation of the multi-level charge pump circuit 56 and the switching circuit 58 to control or govern the switching voltage, V_{SW}, provided at the switching voltage output 26 of the multi-level charge pump buck converter 12Q.

[00956] Figure 38A further depicts that the feedback delay compensation circuit 852 may be coupled to the battery 20 and configured to communicate with the controller 50 via the control bus 44. The feedback delay compensation circuit 852 may generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, based on a slope of a derivative of the V_{RAMP} signal. For example, the feedback delay compensation circuit 852 may determine the slope of the derivative of the V_{RAMP} signal by high pass filtering the V_{RAMP} signal with a capacitor/resistor network (not shown), where the capacitor/resistor network (not shown) has a high pass corner frequency, f_{HP_CF}. Alternatively, the feedback delay compensation circuit 852 may determine the slope of the derivative of the V_{RAMP} signal by high pass filtering the V_{RAMP} signal with an active filter (not shown) to generate the derivative of the V_{RAMP} signal, where the active filter (not shown) has a high pass corner frequency, f_{HP_CF}.

[00957] In addition, in some embodiments, the feedback delay compensation circuit 852 may be coupled to the controller via the control bus 44, a capacitor array control bus 856, or a combination thereof. In some embodiments, the controller 50 may be configured to modify the high pass corner frequency, f_{HP_CF}, and control the 90 degree phase lead of the high pass filtering response in order to maximize the power efficiency of either the parallel amplifier 35 or the pseudo-envelope follower power management system 10QA as a whole.

[00958] Prior to discussing the operation of the multi-level charge pump buck converter 12Q with respect to the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, the embodiments of the feedback delay compensation circuit 852 depicted in Figure 39A and Figure 39B will be described. Figure 39B depicts a differential feedback delay compensation circuit 852A, which is a differential embodiment of the feedback delay compensation circuit 852, depicted in Figure 39A. As depicted in Figure 39B, the V_{RAMP} signal may be a differential V_{RAMP} signal having a non-inverted V_{RAMP} signal component, $V_{RAMP}+$, and an inverted V_{RAMP} signal component, $V_{RAMP}-$.

[00959] Figure 39A depicts an example embodiment of the feedback delay compensation circuit 852, which will be discussed with continuing reference to

Figure 38A. The feedback delay compensation circuit 852 includes a capacitor/resistor network 858 having a high pass derivative filter capacitor 860 and a high pass derivative filter resistor 862 and a Gm feedback compensation circuit 864. The Gm feedback compensation circuit 864 may include an input port 864A and a feedback delay compensation signal output 864B configured to provide the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The capacitor/resistor network 858 may have an input port 858A configured to receive the V_{RAMP} signal. The capacitor/resistor network 858 may have an output port 858B coupled to the input port 864A of the Gm feedback compensation circuit 864. The high pass derivative filter capacitor 860 is coupled between the input port 858A of the capacitor/resistor network 858 and the output port of the capacitor/resistor network 858. The high pass derivative filter resistor 862 is coupled between the output port of the capacitor/resistor network 858 and ground. The output port of the capacitor/resistor network 858 is coupled to the input port 864A of the Gm feedback compensation circuit 864.

[00960] The high pass derivative filter capacitor 860 may have a capacitance level substantially equal to a high pass corner frequency capacitance, C_{HP_CF}. The high pass derivative filter resistor 862 may have a resistance level substantially equal to a high pass corner frequency resistance, R_{HP_CF}. The high pass derivative filter capacitor 860 and the high pass derivative filter resistor 862 of the capacitor/resistor network 858 may be configured to form a high pass filter. The capacitor/resistor network 858 high pass filters the V_{RAMP} signal to generate a high pass filtered V_{RAMP} signal. The high pass filtered V_{RAMP} signal provides a 90 degree phase lead below the high pass corner frequency, f_{HP_CF}, of the capacitor/resistor network as compared to the V_{RAMP} signal, where the slope of the derivative of the V_{RAMP} signal provides an indication of whether the target voltage for the power amplifier supply voltage, V_{CC}, is increasing or decreasing.

[00961] Because the derivative of the V_{RAMP} signal is used to generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, effectively provides a feedback current to the switcher control circuit 52 that has a 90 degree phase lead, as compared to

the V_{RAMP} signal, below the high pass corner frequency, f_{HP_CF}, of the capacitor/resistor network 858. As a result, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an early indication of the direction in which the target voltage for the power amplifier supply voltage, V_{CC}, is headed to the switcher control circuit 52. For example, if the slope of the derivative of the V_{RAMP} signal is positive, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an indication that the target voltage for the power amplifier supply voltage, V_{CC}, is increasing to the switcher control circuit 52, which is independent of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. Alternatively, when the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an indication that the target voltage for the power amplifier supply voltage, V_{CC}, is decreasing to the switcher control circuit 52, which is also is independent of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. For example, the switcher control circuit 52 may be configured to use the information contained in the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to raise or lower the effective thresholds used by the switcher control circuit 52 to control changes between modes of operation of the multi-level charge pump buck converter 12Q, where each mode of operation corresponds to a particular voltage level of the switching voltage, V_{SW}, provided at the switching voltage output 26 to the power inductor 16.

[00962] The capacitor/resistor network 858 includes a high pass corner time constant, τ_{HF_CF}, substantially equal to the product of the high pass corner frequency capacitance, C_{HP_CF}, and the high pass frequency resistance, R_{HP_CF}. The high pass corner frequency, f_{HP_CF}, of the capacitor/resistor network 858 is provided by equation (22) as follows:

$$(22) \qquad f_{\mathrm{HP_CF}} = \frac{1}{(2\mathrm{x}\,\Pi\,\mathrm{x}\,C_{HP_CF}\,\mathrm{x}\,R_{HP_CF})}$$

[00963] As will be discussed, in some embodiments of the feedback delay compensation circuit 852, the high pass corner frequency, f_{HP_CF}, of the

capacitor/resistor network 858 may be configured by the controller 50. For example, in some embodiments, the high pass corner frequency resistance, R_{HP_CF}, of the high pass derivative filter resistor 862 may be a programmable resistance. For example, the high pass derivative filter resistor 862 may be a binary weighted resistor array. In other embodiments, the high pass derivative filter resistor 862 may be a fixed value resistor. Likewise, the high pass corner frequency capacitance, C_{HP_CF}, of the high pass derivative filter capacitor 860 may be a programmable capacitance. For example, the high pass derivative filter capacitor 860 may be a binary weighted capacitor array. However, in some embodiments, the high pass derivative filter capacitor 860 may be a fixed value capacitor.

[00964] In some embodiments of the feedback delay compensation circuit 852, the controller 50 may be configured to change the high pass corner frequency, f_{HP_CF}, to between 30 MHz to 50 MHz in 5 MHz increments. In other embodiments of the feedback delay compensation circuit 852, the feedback delay compensation circuit 852 may be configured to limit the bandwidth of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to improved stability.

[00965] The Gm feedback compensation circuit 864 may be configured to generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, based on the slope of the derivative output response of the capacitor/resistor network 858. In other words, the Gm feedback compensation circuit 864 may be configured to generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, based on the high pass filtered V_{RAMP} signal, where the slope of the high pass filtered V_{RAMP} signal indicates the direction in which the target voltage for the power amplifier supply voltage, V_{CC}, is heading in response to the V_{RAMP} signal. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is based on the derivative of the V_{RAMP} signal, the rate of change of the V_{RAMP} signal results in a change in the magnitude (positive or negative) of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. For example, when the slope of the derivative of the V_{RAMP} signal is positive, the Gm feedback compensation circuit 864 may be configured to source current such that the feedback delay compensation

signal 854, $I_{FEEDBACK_TC}$, has a positive magnitude. However, when the slope of the derivative of the V_{RAMP} signal is negative, the Gm feedback compensation circuit 864 may be configured to sink current such that the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, has a negative magnitude. In addition, the greater the slope of the derivative of the V_{RAMP} signal, the large the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[00966] The Gm feedback compensation circuit 864 may be coupled to the controller 50 via control bus 44. The Gm feedback compensation circuit 864 may have a Gm feedback compensation transconductance, $Gm_{FEEDBACK_TC}$. In some embodiments of the Gm feedback compensation circuit 864, the Gm feedback compensation transconductance, $Gm_{FEEDBACK_TC}$, may be programmable by the controller 50. Accordingly, the controller 50 may adjust the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, by increasing or decreasing the Gm feedback compensation transconductance, $Gm_{FEEDBACK_TC}$. For example, in some cases, the controller 50 may increase or decrease the Gm feedback compensation transconductance, $Gm_{FEEDBACK_TC}$, with an increment size of .1A/V, where $.7A/V \leq Gm_{FEEDBACK_TC} \leq 1.3$ A/V.

[00967] As an example, in some embodiments of the pseudo-envelope follower power management system 10QA, the effects of feedback delay on the power efficiency of the parallel amplifier circuit 14Q may vary depending on the operational mode of the communication device. For example, the parallel amplifier circuit feedback delay may change depending on the configuration of the parallel amplifier circuit 14Q and/or the operational mode of the communication device. Alternatively, depending on the signal processing path associated with the operational mode of the communication device, the feedback delay of the parallel amplifier circuit 14Q may vary. As another example, the parallel amplifier feedback delay may vary depending on the configuration of the operation of the pseudo-envelope follower power management system 10QA and/or the parallel amplifier 35. For example, the parallel amplifier delay may vary depending on the operational mode of the communication device or the band of operation that the communication device is using within a network. As

another example, the feedback delay associated with the generation of the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, may be dependent upon the band of operation of the communication device or the temporal alignment of the open loop ripple compensation assist circuit 414. Thus, in some embodiments, the controller 50 may configure the high pass corner frequency, f_{HP_CF}, based on the operational state of the parallel amplifier circuit 14Q in order to compensate for increases or decrease in the feedback delays associated with generation of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, in order to maximize the power efficiency of the parallel amplifier circuit 14Q, the parallel amplifier 35, or the pseudo-envelope follower power management system 10QA, depicted in Figure 38A, and the pseudo-envelope follower power management system 10QB, depicted in Figure 38B.

[00968] The controller 50 may configure the high pass corner frequency, f_{HP_CF}, of the high pass filter to set the apparent gain of the feedback delay compensation circuit 852 at a given frequency. As a non-limiting example, some embodiments of the feedback delay compensation circuit 852 may be configured such that the high pass frequency resistance, R_{HP_CF}, is substantially equal to 25.3 KΩ. In addition, the high pass derivative filter capacitor 860 may be binary capacitor array, where the high pass corner frequency capacitance, C_{HP_CF}, may have a capacitance value that ranges between 0 Farads to 3pF in increments substantially equal to .2pF. When the capacitance of the high pass corner frequency capacitance, C_{HP_CF}, equals zero Farads, the feedback delay compensation circuit 852 may be effectively disabled. For the case where the high pass corner frequency capacitance, C_{HP_CF}, is configured to have a capacitance substantially equal to .2pF, an apparent gain of the high pass derivative filter capacitor 860 may be substantially equal to -12dBm at 10 MHz. However, for the case where the high pass corner frequency capacitance, C_{HP_CF}, is configured to have a capacitance substantially equal to 3pF, the apparent gain of the high pass derivative filter capacitor 860 may be substantially equal to 10 dBm at 10 MHz. Thus, the aggressiveness of the feedback

compensation provided by the feedback delay compensation circuit 852 may be configured by adjusting the high pass corner frequency, f_{HP_CF}. As an example, as the high pass corner frequency capacitance, C_{HP_CF}, increases, the high pass corner frequency, f_{HP_CF}, decreases, which increases the apparent gain of the feedback delay compensation circuit 852. Because the apparent gain of the feedback delay compensation circuit 852 is increased, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, increases, which tends to improve the power efficiency of the parallel amplifier circuit 14Q. For example, as the apparent gain of the feedback delay compensation circuit 852 is increased, the magnitude of the parallel amplifier output current, I_{PARA_AMP}, generated by the parallel amplifier 35 may tend to decrease. However, in the case where the apparent gain of the feedback delay compensation circuit 852 is too high, the switcher control circuit 52 may pre-maturely change the switching voltage, V_{SW}, which may increase the magnitude of the parallel amplifier output current, I_{PARA_AMP}, generated by the parallel amplifier 35. Thus, depending on the operational mode of the pseudo-envelope follower power management system 10QA and/or the band of operation of the communication device, the controller 50 may configure the high pass corner frequency, f_{HP_CF}, of the high pass filter to maximize power efficiency either the parallel amplifier 35 or the parallel amplifier circuit 14Q as a whole.

[00969] As another example, the controller 50 may configure the high pass corner time constant, τ_{HF_CF}, by programmably changing the capacitance of the high pass corner frequency capacitance C_{HP_CF}, the resistance value of the high pass frequency resistance, R_{HP_CF}, and/or a combination thereof. Similarly, the controller 50 may adjust the high pass corner frequency, f_{HP_CF}, based on the operational state of the pseudo-envelope follower power management system 10QA in order to maximize power efficiency of the system. For example, during configuration of the pseudo-envelope follower power management system 10QA, the controller 50 may be configured to store high pass corner frequency parameters that correspond to various operational states of either the parallel amplifier 35, the pseudo-envelope follower power management

system 10QA, and/or a combination thereof. Each of the stored high pass corner frequency parameters may be associated with a particular operational state of the parallel amplifier 35, the pseudo-envelope follower power management system 10QA, and/or a combination thereof. The high pass corner frequency parameters may include settings to adjust the value of the high pass corner frequency capacitance C_{HP_CF}, the value of the high pass frequency resistance, R_{HP_CF}, and/or a combination thereof. In some embodiments, only the high pass derivative filter capacitor 860 is configured to be programmable whereas the high pass derivative filter resistor 862 is configured to have a fixed value. In other embodiments, only the high pass derivative filter resistor 862 is configured to be programmable whereas the high pass derivative filter capacitor 860 is configured to have a fixed value.

[00970] As another example, the feedback delay compensation circuit 852 may be configured to set the high pass corner frequency, f_{HP_CF}, to a first frequency value when the pseudo-envelope follower power management system 10QA is in a first operational mode and set the high pass corner frequency, f_{HP_CF}, to a second frequency when the pseudo-envelope follower power management system 10QA is in a second operational mode in order to maximize the power efficiency of the pseudo-envelope follower power management system 10QA in each operation mode. Alternatively, the high pass corner frequency, f_{HP_CF}, may be set only during calibration of the pseudo-envelope follower power management system 10QA. The high pass corner frequency, f_{HP_CF}, may be independently set from the bandwidth of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. For example, the controller 50 may configure Gm feedback compensation circuit 864 to limit the frequency pass band of the Gm feedback compensation circuit 864 in order to the improve stability of the pseudo-envelope follower power management system 10QA when operating in a particular operational mode. For example, for the case where the feedback delay of the parallel amplifier circuit is 5ns, the controller 50 may configure the high pass corner frequency, f_{HP_CF}, to be substantial equal to 40MHz and the Gm feedback compensation transconductance, $Gm_{FEEDBACK_TC}$, to be substantially

equal to 1A/V in order to maximize the power efficiency of the parallel amplifier 35.

[00971] As an example, the high pass derivative filter capacitor 860 may be coupled to the controller 50 via the capacitor array control bus 856. The high pass derivative filter capacitor 860 may be configured to be a binary weighted programmable capacitor array similar to the programmable capacitor array 758, depicted in Figure 36. The high pass derivative filter capacitor 860 may include several capacitors arranged in parallel that may be switched in parallel to provide an equivalent capacitance level. The high pass derivative filter capacitor 860 may also have a bypass mode to set the high pass corner frequency capacitance, C_{HP_CF}, equal to zero Farads. The capacitor array control bus 856 may be multi-bit control bus configured to selectively switch in or out one or more of the binary weighted capacitors that are in a parallel arrangement or to switch into the bypass mode. Similar to the variable capacitance control bus 760, CNTR_CD (5:1), depicted in Figure 36, the capacitor array control bus 856 may include multiple bits that may form a binary word that may be used by the controller 50 to control the capacitance of the high pass derivative filter capacitor 860. The high pass derivative filter capacitor 860 may be configured to be a binary weighted programmable capacitor array such that the effective capacitance of the high pass derivative filter capacitor 860 may be a linearly controlled capacitance similar to the programmable capacitor array 758, depicted in Figure 36. For example, in some embodiments of the feedback delay compensation circuit 852, the high pass corner frequency capacitance, C_{HP_CF} of the high pass derivative filter capacitor 860 may be controlled by controller 50 to have a capacitance range of between .2pF to 3pF. As a result, the high pass filter having a high pass corner frequency, f_{HP_CF}, of the capacitor/resistor network 858 may be adjusted by modifying the high pass corner frequency capacitance, $C_{HP_CF,}$ of the high pass derivative filter capacitor 860.

[00972] Figure 39B depicts a differential feedback delay compensation circuit 852A, which is another embodiment of the feedback delay compensation circuit 852 depicted in Figure 39A. The differential feedback delay compensation

circuit 852A will be discussed with continuing reference to Figure 38A. The differential feedback delay compensation circuit 852A functions in a similar fashion as the feedback delay compensation circuit 852, depicted in Figure 39A, except the signal processing is done differentially. The differential feedback delay compensation circuit 852A may be configured to generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, based on the derivative the differential V_{RAMP} signal.

[00973] Figure 39B depicts a differential capacitor/resistor network 858' configured to receive the differential V_{RAMP} signal. In some embodiments, the differential capacitor/resistor network 858' is a differential high pass filter. Similar to the capacitor/resistor network 858, depicted in Figure 39A, the differential capacitor/resistor network 858' may act as a high pass filter to provide the derivative of the differential V_{RAMP} signal, where the high pass filter has a high pass corner frequency, f_{HP_CF}, which corresponds to the high pass corner time constant, τ_{HF_CF}. The differential capacitor/resistor network 858' includes a non-inverting high pass filter input configured to receive the non-inverted V_{RAMP}+ signal component and an inverting high pass filter input configured to receive the inverted V_{RAMP} signal component, V_{RAMP}-. The differential capacitor/resistor network 858' may include a non-inverted high pass filtered output and an inverted high pass filtered output. The non-inverted high pass filtered output may be formed by coupling a first high pass derivative filter capacitor 860A to a first high pass derivative filter resistor 862A, where the first high pass derivative filter resistor 862A is coupled between the non-inverted high pass filtered output and a differential reference voltage, V_{DIFF_REF}. The inverted high pass filtered output may be formed by coupling a second high pass derivative filter capacitor 860B to a second high pass derivative filter resistor 862B, where the second high pass derivative filter resistor 862B is coupled between the inverted high pass filtered output and the differential reference voltage, V_{DIFF_REF}. The first high pass derivative filter capacitor 860A may be coupled between the non-inverting high pass filter input and the non-inverted high pass filtered output. The second high pass derivative filter capacitor 860B may be coupled between the inverting high

pass filter input and the inverted high pass filtered output. The differential reference voltage, V_{DIFF_REF}, may provide a common voltage reference for the non-inverted V_{RAMP} signal component, $V_{RAMP}+$, and the inverted V_{RAMP} signal component, $V_{RAMP}-$. In some embodiments, the differential reference voltage, V_{DIFF_REF}, is tied to ground. The differential capacitor/resistor network 858' high pass filters the differential V_{RAMP} signal to generate a high pass filtered V_{RAMP} signal, where the high pass filtered V_{RAMP} signal is used as the derivative of the V_{RAMP} signal. The high pass filtered V_{RAMP} signal is provided as a differential signal between the non-inverted high pass filtered output and the inverted high pass filtered output.

[00974] The first high pass derivative filter capacitor 860A and the second high pass derivative filter capacitor 860B may each be configured as a binary capacitor array that is similar in form and function to the high pass derivative filter capacitor 860. Via the capacitor array control bus 856, the controller 50 may configure the capacitance value of the first high pass derivative filter capacitor 860A and the second high pass derivative filter capacitor 860B to be substantially equal to the high pass corner frequency capacitance, C_{HP_CF}. As a non-limiting example, the high pass corner frequency capacitance, C_{HP_CF}, may have a capacitance between 0 farads and 3pF in increments substantially equal to .2pF. When the capacitance of the high pass corner frequency capacitance, C_{HP_CF}, equals zero, the differential feedback delay compensation circuit 852A may be effectively disabled. Similarly, in some embodiments, the first high pass derivative filter resistor 862A and the second high pass derivative filter resistor 862B may be configured as binary resistor arrays. Via the control bus 44, the controller 50 may configure the first high pass derivative filter resistor 862A and the second high pass derivative filter resistor 862B to have a resistance level substantially equal to the high pass corner frequency resistance, R_{HP_CF}. The differential capacitor/resistor network 858' has a high pass corner time constant, τ_{HF_CF}. The high pass corner time constant, τ_{HF_CF}, is the product of the high pass corner frequency capacitance, C_{HP_CF}, and the high pass frequency resistance, R_{HP_CF}. The controller 50 may be configured to adjust the

high pass corner frequency capacitance, C_{HP_CF}, the high pass frequency resistance, R_{HP_CF}, and/or a combination thereof in order to configure the high pass corner time constant, τ_{HF_CF}. However, in some embodiments, (not shown) the first high pass derivative filter capacitor 860A and the second high pass derivative filter capacitor 860B may be fixed value capacitors while the first high pass derivative filter resistor 862A and the second high pass derivative filter resistor 862B may be programmable. In other embodiments, the first high pass derivative filter capacitor 860A and the second high pass derivative filter capacitor 860B may be programmable while the first high pass derivative filter resistor 862A and the second high pass derivative filter resistor 862B have a fixed value.

[00975] The differential Gm feedback compensation circuit 864' includes an inverting input and a non-inverting input. The non-inverting input of the differential Gm feedback compensation circuit 864' may be in communication with the first high pass derivative filter capacitor 860A and the first high pass derivative filter resistor 862A, which form the non-inverted high pass filtered output of the differential capacitor/resistor network 858'. The inverting input of the differential Gm feedback compensation circuit 864' may be in communication with the second high pass derivative filter capacitor 860B and the second high pass derivative filter resistor 862B, which form the inverted high pass filtered output of the differential capacitor/resistor network 858'. The differential Gm feedback compensation circuit 864' may be configured to generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, based on the derivative output response of the differential capacitor/resistor network 858'. In the case where the slope of the derivative of the differential V_{RAMP} signal is positive, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is a positive. As a result, the differential Gm feedback compensation circuit 864' sources current when the slope of the derivative of the differential V_{RAMP} signal is positive. In the case where the slope of the derivative of the differential V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is a negative current. In other words, the differential Gm feedback compensation circuit 864' sinks

current when the slope of the derivative of the V_{RAMP} signal is negative. Similar to the Gm feedback compensation circuit 864, depicted in Figure 39A, the differential Gm feedback compensation circuit 864' also has a Gm feedback compensation transconductance, $Gm_{FEEDBACK_TC}$, which may be configured by the controller 50. Similar to the feedback delay compensation circuit 852, depicted in Figure 39A, the controller 50 may configure the Gm feedback compensation transconductance, $Gm_{FEEDBACK_TC}$, of the differential Gm feedback compensation circuit 864' to optimize or calibrate the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[00976] Returning to Figure 38A, the application of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, in the multi-level charge pump buck converter 12Q will now be discussed. For the sake of simplicity, and not by way of limitation, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is assumed to substantially equal the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. Accordingly, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, reflects the magnitude of the parallel amplifier output current, I_{PARA_AMP}, generated by the parallel amplifier 35.

[00977] Although the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides a 90 degree phase lead with respect to the V_{RAMP} signal, the feedback delay compensation circuit 852 may have a signal generation propagation delay associated with generation of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. In order to temporally align the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, with the operation of the parallel amplifier 35, the parallel amplifier circuit delay may be adjusted. As an example, in some embodiments, the parallel amplifier circuit 14Q may be configured to add a feedback compensation propagation delay between the first control input 34 and the output of the parallel amplifier 35. As an example, the parallel amplifier circuit delay may be a fixed delay added to the parallel amplifier 35, the parallel amplifier circuitry 32, and/or a combination thereof. In other embodiments, the feedback compensation propagation delay may be added by adjusting the propagation time through a combination of the pre-processing circuitry, the parallel amplifier

circuitry 32, the parallel amplifier 35, and/or a combination thereof. In other embodiments, the parallel amplifier circuit delay may be a programmable delay that is configured by the controller 50.

[00978] As depicted in Figure 38A, some embodiments of the multi-level charge pump buck converter 12Q may be configured to interoperate with a frequency locked loop circuit 54 in a fashion similar to the multi-level charge pump buck converter 12A, depicted in Figure 2A, or the multi-level charge pump buck converter 12B, depicted in Figure 2B. Figure 3I depicts an embodiment of the switcher control circuit 52I that is configured to interoperate with the frequency locked loop circuit 54. The switcher control circuit 52I, depicted in Figure 3I, is similar in form and function to the embodiment of the switcher control circuit 52A, depicted in Figure 3A, except, as depicted in Figure 3I, the switcher control circuit 52I is further configured to receive and use the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$ to control the operation of the multi-level charge pump buck converter 12Q. Unlike the switcher control circuit 52A depicted in Figure 3A, Figure 3I depicts that the switcher control circuit 52I includes a summing circuit 136A configured to receive a scaled parallel amplifier circuit output current estimate 138 from the multiplier circuit 134, the threshold offset current 42, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The summing circuit 136A subtracts the threshold offset current 42 from the sum of the scaled parallel amplifier circuit output current estimate 138 and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to form a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, that is received by the threshold detector and control circuit 132I, depicted in Figure 4I. The compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, may also be referred to as a composite control signal. In this case, because only the magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is scaled by the threshold scalar 137A, the average switching frequency of operation of the multi-level charge pump buck converter 12Q is adjusted independent of the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is used to regulate the offset voltage, V_{OFFSET}, between the power amplifier

supply output 28 and the parallel amplifier output 32A, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Alternatively, similar to the alternative embodiments discussed with respect to Figure 3A, some embodiments of the switcher control circuit 52I (not depicted) may scale a sum of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, with the threshold scalar 137A before subtracting the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. In this case, because the magnitude of the sum of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is scaled by the threshold scalar 137A, the average switching frequency of operation of the multi-level charge pump buck converter 12Q is adjusted independent of the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is used to regulate the offset voltage, V_{OFFSET}. In still another alternative embodiment of the switcher control circuit 52I (not depicted), the multiplier circuit 134 scales the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, less the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, by the threshold scalar 137A before adding the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. In this case, the frequency locked loop circuit 54A adjusts the average switching frequency of operation of the multi-level charge pump buck converter 12Q independent of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As another alternative embodiment, the switcher control circuit 52I (not depicted) may scale the sum of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, less the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, by the threshold scalar 137A to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}.

[00979] The threshold detector and control circuit 132I, depicted in Figure 4I, is similar in form and function to the threshold detector and control circuit 132A, depicted in Figure 4A. The threshold detector and control circuit 132I includes

the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130, coupled to the positive terminal of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146, respectively. Operationally, the threshold detector and control circuit 132I, depicted in Figure 4I, functions substantially the same as the threshold detector and control circuit 132A, depicted in Figure 4A. However, the effective level of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 relative to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, may be raised or lowered based on the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Because the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, depends on the slope of the derivative of the V_{RAMP} signal, the effective level of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 relative to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, are changed based on the rate of change of the V_{RAMP} signal and the direction of the change. For example, in the case where the slope of the derivative of the V_{RAMP} signal is positive, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is positive, which will tend to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. As a result, the relative magnitude of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 decrease with respect to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. In contrast, for example, in the case where the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is negative, which will tend to decrease the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. Because the decrease the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is lowered by the feedback delay

compensation signal 854, $I_{FEEDBACK_TC}$, the relative magnitude of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 increase with respect to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$.

[00980] For example, for the case where the magnitude of the V_{RAMP} signal is increasing, such that the slope of the derivative of the V_{RAMP} signal is positive, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will tend to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. As a result, the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, needed to increase the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, to a level that causes one of the first comparator 140, the second comparator 142, the third comparator 144, or the fourth comparator 146, to transition to a digital logic low state is decreased. In other words, the effect of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, being positive is to lower the threshold points at which each of the shunt level indication 150A, the series level indication 152A, the first boost level indication 154A, or the second boost level indication 156A transitions from being de-asserted to being asserted. As a result, the switcher control circuit 52I will tend to increase the switching voltage, V_{SW}, based on the in the magnitude of the V_{RAMP} signal sooner than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present because the switcher control circuit 52I does not have to depend solely on the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, to provide an indication of whether the target voltage for the power amplifier supply voltage, V_{CC}, is being increased based on the increase in the magnitude of the V_{RAMP} signal.

[00981] As another example, for the case where the magnitude of the V_{RAMP} signal is decreasing, such that the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will tend to decrease the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. As a result, the magnitude of the scaled parallel

amplifier output current estimate, $I_{PARA_AMP_SENSE}$, needed to decrease the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, to a level that causes one of the first comparator 140, the second comparator 142, the third comparator 144, or the fourth comparator 146, to transition from a digital logic low state to a digital logic high state is decreased. In other words, the effect of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, being negative is to increase the threshold points at which each of the shunt level indication 150A, the series level indication 152A, the first boost level indication 154A, or the second boost level indication 156A transitions from being asserted to being de-asserted. As a result, the switcher control circuit 52l will tend to decrease the switching voltage, V_{SW}, based on the in the magnitude of the V_{RAMP} signal sooner than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present because the switcher control circuit 52l does not have to depend solely on the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, to provide an indication that the target voltage for the power amplifier supply voltage, V_{CC}, is being decreased based on the decreased magnitude of the V_{RAMP} signal. Alternatively, when the V_{RAMP} signal is decreasing, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, lowers the value of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. Because the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is lower in value, the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, needed such that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, causes the first comparator 140, the second comparator 142, the third comparator 144, or the fourth comparator 146, to transition from a digital logic low state to a logic high state is increased. As a result, the switcher control circuit 52l will tend to decrease the switching voltage, V_{SW}, sooner than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present.

[00982] Figure 4l depicts the threshold and control circuit 132l of the switcher control circuit 52l. The threshold and control circuit 132l is similar in form and function to the threshold and control circuit 132A, depicted in Figure 4A, except

the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, includes a contribution from the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Thus, the operation of the first state machine, depicted in Figure 5A, and the second state machine, depicted in Figure 5B, associated with the logic circuit 148A will be influenced by the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As an example, the behavior of the first state machine, depicted in Figure 5A, and the second state machine, depicted in Figure 6A, associated with the logic circuit 148A relative to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, will change depending on the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. In the case where the V_{RAMP} signal is increasing such that the slope of the derivative of the V_{RAMP} signal is positive, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, tends to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. As a result, the first state machine of the logic circuit 148A will tend to shift into a mode of operation that provides a higher switching voltage, V_{SW}, at the switching voltage output 26 for a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, having a corresponding lower magnitude because the effect is to lower the threshold points at which each of the shunt level indication 150A, the series level indication 152A, the first boost level indication 154A, or the second boost level indication 156A transitions from being de-asserted to being asserted due to the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[00983] As a result, for example, when the first state machine associated with the logic circuit 148A, depicted in Figure 5A, is in the shunt output mode 188A, the first state machine transitions to the series output mode 190A when the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is at a lower magnitude due to the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. In this case, the addition of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, causes the first state machine to advance in time to the point at which the first state machine transitions from the shunt output mode 188A to the series output mode 190A in response to an increase in the magnitude of the

V_{RAMP} signal, where the increase in the magnitude of the V_{RAMP} signal indicates that the target voltage for the power amplifier supply voltage, V_{CC}, will be increased. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an earlier indication that the target voltage for the power amplifier supply voltage, V_{CC}, is being increased, based on the positive slope of the derivative of the V_{RAMP} signal, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by lowering the effective threshold level of the series level threshold 126, which is provided as an input to the positive terminal of the second comparator 142.

[00984] As a second example, when the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will lower the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. As a result, the first state machine will tend to shift to a mode of operation that provides a lower switching voltage, V_{SW}, at the switching voltage output 26 for a particular magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. For example, as depicted in Figure 5A, when the first state machine of the logic circuit 148A, depicted in Figure 4I, is in the series output mode 190A, the first state machine transitions from the series output mode 190A to the shunt output mode 188A when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, is less than the shunt level threshold 124. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, lowers the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, when the slope of the derivative of the V_{RAMP} signal is negative, the transition from the series output mode 190A to the shunt output mode 188A for a particular magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, occurs earlier than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not used to form the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an earlier indication that the target voltage for the power amplifier supply voltage, V_{CC}, is

being decreased, based on the negative slope of the derivative of the V_{RAMP} signal, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by raising the effective threshold level of the series level threshold 126, which is provided as an input to the positive terminal of the first comparator 140. The effect is to advance in time when the first state machine of the logic circuit 148A transitions from the series output mode 190A to the shunt output mode 188A relative to the decrease in the magnitude of the V_{RAMP} signal, where the decrease in the magnitude of the V_{RAMP} signal indicates that the target voltage for the power amplifier supply voltage, V_{CC}, is decreasing. As a result, the switching voltage, V_{SW}, will be lowered sooner in response to the V_{RAMP} signal decreasing in value than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present.

[00985] The feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by lowering or raising the effective threshold level of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 as a function of the slope of the V_{RAMP} signal, where the slope of the V_{RAMP} signal indicates a corresponding increase or decrease in the target voltage for the power amplifier supply voltage, V_{CC}. The feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, likewise impacts the operational performance of the second state machine of the logic circuit 148A of the threshold detector and control circuit 132I, depicted in Figure 6A, in a similar fashion.

[00986] Returning to Figure 38A, because the V_{RAMP} signal represents the target voltage for the power amplifier supply voltage, V_{CC}, the parallel amplifier 35 is configured to generate a parallel amplifier output current, I_{PARA_AMP}, to drive the power amplifier supply voltage, V_{CC}, to the target voltage until the multi-level charge pump buck converter 12Q responds to the change in the target voltage level for the power amplifier supply voltage, V_{CC}. Because the feedback delay

compensation signal 854, $I_{FEEDBACK_TC}$, provides an early indication of the target voltage level for the power amplifier supply voltage, V_{CC}, based on the slope of the derivative of the V_{RAMP} signal, the multi-level charge pump buck converter 12Q responds to the change in the V_{RAMP} signal when the parallel amplifier output current, I_{PARA_AMP}, is at a lower magnitude, which reduces the average current sourced and sunk by the parallel amplifier 35.

[00987] Some embodiments of the multi-level charge pump buck converter 12Q, depicted in Figure 38A, are configured to interoperate with the frequency locked loop circuit 54. As an example, the multi-level charge pump buck converter 12Q may include a switcher control circuit 52 similar to the switcher control circuit 52J depicted in Figure 3J. The switcher control circuit 52J, depicted in Figure 3J, is similar in form and function to the switcher control circuit 52B, depicted in Figure 3B. However, unlike the switcher control circuit 52B depicted in Figure 3B, the switcher control circuit 52J depicted in Figure 3J includes a threshold and control circuit 132J configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Figure 4J depicts that the threshold and control circuit 132J is similar in form and function to the threshold and control circuit 132B, depicted in Figure 4B, except the threshold and control circuit 132J depicted in Figure 4J includes a summing circuit 136A configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, generated by the parallel amplifier circuit, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The summing circuit 136A subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the sum of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to generate a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', which may be used as a composite control signal for the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. Similar to the operation of the threshold and control circuit 132B depicted in Figure 3B, the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}' is provided to the negative terminal of each

of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146.

[00988] Similar to the operation of the threshold detector and control circuit 132I, depicted in Figure 4I, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, may be used to raise or lower the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}' depending upon the slope of the V_{RAMP} signal, which is used to form the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As a result, similar to the behavior of the first state machine, depicted in Figure 5A, and the second state machine, depicted in Figure 6A, associated with the logic circuit 148A, depicted in Figure 4I, the behavior of the first state machine, depicted in Figure 5B, and the second state machine, depicted in Figure 6B, associated with the logic circuit 148B of the threshold detector and control circuit 132J, depicted in Figure 4J, relative to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, will change depending on the feedback delay compensation signal 854. In the case where the V_{RAMP} signal is increasing such that the slope of the derivative of the V_{RAMP} signal is positive, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, tends to increase the magnitude of a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the first state machine of the logic circuit 148B of the threshold detector and control circuit 132J, depicted in Figure 4J, will tend to shift into a mode of operation that provides a higher switching voltage, V_{SW}, at the switching voltage output 26 for a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, having a corresponding lower magnitude because the effect is to lower the threshold points at which each of the shunt level indication 150B, the series level indication 152B, the first boost level indication 154B, or the second boost level indication 156B transitions from being de-asserted to being asserted due to the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[00989] As a result, for example, when the first state machine associated with the logic circuit 148B, depicted in Figure 5B, is in the shunt output mode 188B, the first state machine transitions to the series output mode 190B when the

scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is at a lower magnitude due to the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. In this case, the addition of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is to cause the first state machine to advance in time to the point at which the first state machine transitions from the shunt output mode 188B to the series output mode 190B in response to an increase in the magnitude of the V_{RAMP} signal, where the increase in the magnitude of the V_{RAMP} signal indicates that the target voltage for the power amplifier supply voltage, V_{CC}, will be increased. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an earlier indication that the target voltage for the power amplifier supply voltage, V_{CC}, is being increased, based on the positive slope of the derivative of the V_{RAMP} signal, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by lowering the effective threshold level of the series level threshold 126, which is provided as an input to the positive terminal of the second comparator 142.

[00990] As a second example, when the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will lower the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the first state machine associated with the logic circuit 148B of the threshold and control circuit 132J will tend to shift to a mode of operation that provides a lower switching voltage, V_{SW}, at the switching voltage output 26 for a particular magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. For example, as depicted in Figure 5B, when the first state machine of the logic circuit 148B, depicted in Figure 4J, is in the series output mode 190B, the first state machine transitions from the series output mode 190B to the shunt output mode 188B when the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is less than the shunt level threshold. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, lowers the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, when the slope of the derivative of the V_{RAMP} signal is

negative, the transition from the series output mode 190B to the shunt output mode 188B for a particular magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, occurs earlier than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not used to form the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an earlier indication that the target voltage for the power amplifier supply voltage, V_{CC}, is being decreased, based on the negative slope of the derivative of the V_{RAMP} signal, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by raising the effective threshold level of the series level threshold 126, which is provided as an input to the positive terminal of the first comparator 140. The effect is to advance in time when the first state machine of the logic circuit 148B transitions from the series output mode 190B to the shunt output mode 188B relative to the decrease in the magnitude of the V_{RAMP} signal, where the decrease in the magnitude of the V_{RAMP} signal indicates that the target voltage for the power amplifier supply voltage, V_{CC}, is decreasing. As a result, the switching voltage, V_{SW}, will be lowered sooner in response to the V_{RAMP} signal decreasing in value than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present.

[00991] The feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by lowering or raising the effective threshold level of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 as a function of the slope of the V_{RAMP} signal, where the slope of the V_{RAMP} signal indicates a corresponding increase or decrease in the target voltage for the power amplifier supply voltage, V_{CC}. The feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, likewise impacts the operational performance of the second state machine of the logic circuit 148B of the threshold detector and control circuit 132J, depicted in Figure 6B.

[00992] As a first example, when the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is greater than zero, the first state machine tends to shift to a mode of operation that provides a higher switching voltage, V_{SW}, at the switching voltage output 26 at a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, having a corresponding lower magnitude. However, when the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is less than zero, the first state machine tends to shift to a mode of operation that provides a lower switching voltage, V_{SW}, at the switching voltage output 26 at a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, having a corresponding lower magnitude.

[00993] For example, in the case where the slope of derivative of the V_{RAMP} signal is positive, the V_{RAMP} signal is increasing in value and the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will be positive. As a result, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, tends to increase the value of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, which effectively lowers the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, need to trigger a change in the output of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. Thus, the addition of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, effectively lowers the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130, relative to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$.

[00994] Returning to Figure 38A, as discussed previously, because the V_{RAMP} signal represents the target voltage for the power amplifier supply voltage, V_{CC}, the parallel amplifier 35 is configured to generate a parallel amplifier output current, I_{PARA_AMP}, to drive the power amplifier supply voltage, V_{CC}, to the target voltage until the multi-level charge pump buck converter 12Q responds to the change in the target voltage level for the power amplifier supply voltage, V_{CC}. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an

early indication of the target voltage level for the power amplifier supply voltage, V_{CC}, based on the slope of the derivative of the V_{RAMP} signal, the multi-level charge pump buck converter 12Q responds to the change in the V_{RAMP} signal sooner than if the multi-level charge pump buck converter 12Q was being configured solely based on the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. Accordingly, the multi-level charge pump buck converter 12Q tends to respond to the change in the V_{RAMP} signal when the parallel amplifier output current, I_{PARA_AMP}, has a lower magnitude, which reduces the average current sourced and sunk by the parallel amplifier 35.

[00995] Although Figure 38A depicts the multi-level charge pump buck converter 12Q as having the frequency locked loop circuit 54, some embodiments of the multi-level charge pump buck converter 12Q may not include the frequency locked loop circuit 54, or the frequency locked loop circuit 54 may be disabled. In this case, the switcher control circuit 52 of the multi-level charge pump buck converter 12Q may be configured similar to the switcher control circuit 52K depicted in Figure 3K. The switcher control circuit 52K, depicted in Figure 3K, is similar in form and function to the switcher control circuit 52C, depicted in Figure 3C, except the threshold detector and control circuit 132K is configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As depicted in Figure 4K, the threshold detector and control circuit 132K is similar in form and function to the threshold detector and control circuit 132C, depicted in Figure 3C, except the threshold detector and control circuit 132K, depicted in Figure 4K, includes the summing circuit 136A configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The summing circuit 136A subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the sum of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to generate a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', which may be used as a composite control signal for the first comparator 140, the second

comparator 142, the third comparator 144, and the fourth comparator 146. Similar to the operation of the threshold and control circuit 132C depicted in Figure 3C, the threshold and control circuit 132K is configured such that the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}' is provided to the negative terminal of each of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. Similar to the previously described threshold detector and control circuit 132I, depicted in Figure 4I, and the threshold detector and control circuit 132J, depicted in Figure 4J, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, may be used to raise or lower the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}' depending on the slope of the derivative of the V_{RAMP} signal, which is used to generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[00996] Accordingly, similar to the behavior of the first state machine, depicted in Figure 5A, and the second state machine, depicted in Figure 6A, associated with the logic circuit 148A, and the first state machine, depicted in Figure 5B and the second state machine depicted in Figure 6B, associated with the logic circuit 148B, the behavior of the first state machine, depicted in Figure 5C, and the second state machine, depicted in Figure 6C, associated with the logic circuit 148C of the threshold and control circuit 132K, depicted in Figure 4K, changes relative to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, depending on whether the feedback delay compensation signal 854 is positive or negative. As a first example, in the case where the V_{RAMP} signal is increasing such that the slope of the derivative of the V_{RAMP} signal is positive, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, tends to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the first state machine of the logic circuit 148C, depicted in Figure 5C, tends to shift into a mode of operation that provides a higher switching voltage, V_{SW}, at the switching voltage output 26 for a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, having a corresponding lower magnitude because the effect is to

lower the threshold points at which each of the shunt level indication 150C, the series level indication 152C, the first boost level indication 154C, or the second boost level indication 156C transitions from being de-asserted to being asserted due to the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As a result, the addition of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to form the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', is to cause the first state machine, depicted in Figure 5C, to advance in time to the point at which the first state machine of the logic circuit 148C transitions from the shunt output mode 188C to the series output mode 190C in response to an increase in the magnitude of the V_{RAMP} signal, where the increase in the magnitude of the V_{RAMP} signal indicates that the target voltage for the power amplifier supply voltage, V_{CC}, will be increased. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an earlier indication that the target voltage for the power amplifier supply voltage, V_{CC}, is being increased, based on the positive slope of the derivative of the V_{RAMP} signal, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by lowering the effective threshold level of the series level threshold 126, which is provided as an input to the positive terminal of the second comparator 142. Similarly, in the case where the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will lower the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the transition from the series output mode 190C to the shunt output mode 188A for a particular magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, occurs earlier than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not used to form the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. Because the negative slope of the derivative of the V_{RAMP} signal provides an earlier indication that the target voltage for the power amplifier supply voltage, V_{CC}, is being decreased, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback

delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by raising the effective threshold level of the series level threshold 126, which is provided as an input to the positive terminal of the first comparator 140. The effect is to advance in time when the first state machine of the logic circuit 148C transitions from the series output mode 190C to the shunt output mode 188C in response to the decrease in the magnitude of the V_{RAMP} signal, where the decrease in the magnitude of the V_{RAMP} signal indicates that the target voltage for the power amplifier supply voltage, V_{CC}, is decreasing. As a result, the switching voltage, V_{SW}, will be lowered sooner in response to the V_{RAMP} signal decreasing in value than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present, which reduces the average current sourced and sunk by the parallel amplifier 35.

[00997] Although Figure 38A depicts the multi-level charge pump buck converter 12Q as having a V_{OFFSET} loop circuit 41, some embodiments of the multi-level charge pump buck converter 12Q may not include a V_{OFFSET} loop circuit 41. For example, in the case where the coupling circuit 18 is a wire, the offset voltage, V_{OFFSET}, generated across the coupling circuit 18 is approximately zero. By way of example, and not by limitation, for an embodiment of the multi-level charge pump buck converter 12Q that does not include the V_{OFFSET} loop circuit 41, the multi-level charge pump buck converter 12Q may include a switcher control circuit 52 similar to the switcher control circuit 52L, depicted in Figure 3L. The switcher control circuit 52L, depicted in Figure 3L, is similar in form and function to the switcher control circuit 52D, depicted in Figure 3D. However, unlike the switcher control circuit 52D, depicted in Figure 3D, the switcher control circuit 52L includes a threshold and control circuit 132L configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Figure 4L depicts an embodiment of the threshold and control circuit 132L that is similar in form and function to the embodiment of the threshold and control circuit 132D, depicted in Figure 4D. However, unlike the threshold and control circuit 132D depicted in Figure 4D, the threshold and control circuit 132L, depicted in Figure 4L, includes a summer circuit 136B configured to receive the

feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. The summer circuit 136B adds the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to generate a feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, which may be used as a composite control signal for the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. In addition, the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is coupled to the negative terminal of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146, respectively. The threshold and control circuit 132L includes the logic circuit 148D. The operation of the first state machine and the second state machine of the logic circuit 148D is changed by the addition of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to form the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. For example, unlike the operation of the first state machine, depicted in Figure 5D, and the second state machine, depicted in Figure 6D, the first state machine, depicted in Figure 5L, and the second state machine, depicted in Figure 6L, of logic circuit 148D as used by the threshold detector and control circuit 132L, depicted in Figure 4L, transition between the operational states of second state machine the based on the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, instead of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$.

[00998] As an example, operation of the first state machine of the logic circuit 148D of the threshold and control circuit 132L, depicted in Figure 4L, is depicted in Figure 5L. As depicted in Figure 5L, the transitions between the shunt output mode 188D, the series output mode 190D, the first boost output mode 192D, and the second boost output mode 194D, of the first state machine, depicted in Figure 5L, are dependent upon the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. For example, in the first state machine, depicted in Figure 5L, the logic circuit 148D transitions the first state machine from the shunt output mode 188D to the series output mode 190D when the

feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the series level threshold 126. Similarly, the logic circuit 148D transitions the first state machine from the series output mode 190D to the shunt output mode 188D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124. The logic circuit 148D transitions the first state machine from the series output mode 190D to the first boost output mode 192D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the first boost level threshold 128. The logic circuit 148D transitions the first state machine from the first boost output mode 192D to the second boost output mode 194D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the second boost level threshold 130. The logic circuit 148D transitions the first state machine from the first boost output mode 192D to the shunt output mode 188D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124. Similarly, the logic circuit 148D transitions the first state machine from the second boost output mode 194D to the shunt output mode 188D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124. Otherwise, the operation of the first state machine of the logic circuit 148D, with respect to the shunt output mode 188D, the series output mode 190D, the first boost output mode 192D, and the second boost output mode 194D, is substantially the same as the operation of the first state machine, depicted in Figure 5D.

[00999] Similarly, as another example, the second machine of the logic circuit 148D of the threshold and control circuit 132L, depicted in Figure 4L, is depicted in Figure 6L. As depicted in Figure 6L, the transitions between the shunt output mode 196D, the series output mode 198D, the first boost output mode 200D, and the second boost output mode 202D of the second state machine are dependent upon the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}.

[001000] For example, in the second state machine depicted in Figure 6L, the logic circuit 148D transitions the second state machine from the shunt output mode 196D to the series output mode 198D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the series level threshold 126. Similarly, the logic circuit 148D transitions the second state machine from the series output mode 198D to the shunt output mode 196D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124. The logic circuit 148D transitions the second state machine from the series output mode 198D to the first boost output mode 200D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the first boost level threshold 128 and the boost lockout counter = 0. The logic circuit 148D transitions the second state machine from the first boost output mode 200D to the series output mode 198D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the first boost level threshold 128. The logic circuit 148D transitions the second state machine from the first boost output mode 200D to the second boost output mode 202D when feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the second boost level threshold 130. The logic circuit 148D transitions the second state machine from the second boost output mode 202D to the series output mode 198D when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the first boost level threshold 128. Otherwise, the operation of the second state machine of the logic circuit 148D of threshold detector and control circuit 132L, depicted in Figure 6L, with respect to the shunt output mode 196D, the series output mode 198D, the first boost output mode 200D, and the second boost output mode 202D, is substantially the same as the operation of the second state machine depicted in Figure 6D. Because operation of the shunt output mode 196D, the series output mode 198D, the first boost output mode 200D, and the second boost output mode 202D have been otherwise previously described in detail with respect to the operation of the second state machine depicted in Figure 6D, a detailed discussion of the

operation of the shunt output mode 196D, the series output mode 198D, the first boost output mode 200D, and the second boost output mode 202D are here omitted.

[001001] Operationally, when the slope of the derivative of the V_{RAMP} signal is positive, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is positive, which increases the magnitude of the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. As a result, each of the shunt level indication 150D, the series level indication 152D, the first boost level indication 154D, or the second boost level indication 156D will tend to transition from being de-asserted to being asserted when the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is lower. Thus, when the V_{RAMP} signal is increasing in magnitude, the switcher control circuit 52L, depicted in Figure 3L, tends to increase the switching voltage, V_{SW}, sooner than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not added to the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to form the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. Similarly, when the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will decrease the magnitude of the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. As a result, each of the shunt level indication 150D, the series level indication 152D, the first boost level indication 154D, or the second boost level indication 156D will tend to transition from being asserted to being de-asserted when the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is lower. Accordingly, the first state machine, depicted in Figure 5L, and the second state machine, depicted in Figure 6L, tends to shift to a mode of operation that provides a lower switching voltage, V_{SW}, at the switching voltage output 26 at a corresponding lower magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an early indication of the direction in which the target voltage level for the power amplifier supply voltage, V_{CC}, to the multi-level charge pump buck converter 12Q.

[001002] In some embodiments of the switcher control circuit 52 of the multi-level charge pump buck converter 12Q, depicted in Figure 38A, the negative terminal of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 do not all receive a composite control signal that is adjusted based on the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. In other words, some embodiments of the threshold detector and control circuits of the embodiments of the switcher control circuit 52 may provide a first control signal to the negative terminal of each of the first comparator 140 and the second comparator 142, and a second signal to the negative terminal of the third comparator 144, and the fourth comparator 146, where the level of the second control signal is independent of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[001003] As a non-limiting example, some embodiments of the switcher control circuit 52 of the multi-level charge pump buck converter 12Q may be similar to the switcher control circuit 52R depicted in Figure 3R. The switcher control circuit 52R, depicted in Figure 3R, may be similar in form and function to the switcher control circuit 52L depicted in Figure 3L. However, unlike the switcher control circuit 52L depicted in Figure 3L, the switcher control circuit 52R, depicted in Figure 3R, includes the threshold detector and control circuit 132R depicted in Figure 4R.

[001004] The threshold detector and control circuit 132R is similar in form and function to the threshold detector and control circuit 132L except the negative terminal of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 are not each coupled to the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. Instead, the negative terminal of each of the first comparator 140 and the second comparator 142 receives the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. However, the negative terminal of the third comparator 144 and the fourth comparator 146 receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. In addition, the logic circuit 148D is replaced by the logic circuit 148R. The logic circuit 148R is similar

in form and function to the logic circuit 148D. The logic circuit 148R includes a boost lockout counter 184 and a boost time counter 186, as described above. The first state machine associated with the logic circuit 148R is depicted in Figure 5R. The second state machine associated with the logic circuit 148R is depicted in Figure 6R.

[001005] As a result, when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the shunt level threshold 124, the output of the first comparator 140 is set to a digital logic low state to assert the shunt level indication 150R. When the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124, the output of the first comparator 140 is set to a digital logic high state to de-assert the shunt level indication 150R. The shunt level indication 150R is provided as an input to the logic circuit 148R. Similarly, when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the series level threshold 126, the output of the second comparator 142 is set to a digital logic low state to the series level indication 152R. However, when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the series level threshold 126, the output of the second comparator 142 is set to a digital logic high state to de-assert the series level indication 152R. The series level indication 152R is provided as an input to the logic circuit 148R.

[001006] In addition, when the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than the first boost level threshold 128, the output of the third comparator 144 is set to a digital logic low state to assert the first boost level indication 154R. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the first boost level threshold 128, the output of the third comparator 144 is set to a digital logic high state to de-assert the first boost level indication 154R. The first boost level indication 154R is provided as an input to the logic circuit 148R. Similarly, when the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than the second boost level threshold 130, the output of the fourth comparator 146 is set

to a digital logic low state to assert the second boost level indication 156R. When the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the second boost level threshold 130, the output of the fourth comparator 146 is set to a digital logic high state to de-assert the second boost level indication 156R. The second boost level indication 156R is provided as an input to the logic circuit 148R.

[001007] As a result, the generation of the shunt level indication 150R and the series level indication 152R is affected by the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, from the feedback delay compensation circuit 852. In the case where the V_{RAMP} signal is increasing, the feedback delay compensation circuit 852 increases the value of the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, such that a lower magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, will trigger the shunt level indication 150R or the series level indication 152R. Thus, referring to the diagram of the first state machine associated with the logic circuit 148R, depicted in Figure 5R, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, affects the condition for transitioning from the shunt output mode 188R to the series output mode 190R. In addition, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, affects the conditions for transitioning from the series output mode 190R, the first boost output mode 192R, and the second boost output mode 194R to the shunt output mode 188R. However, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, does not affect the condition for transitioning from the series output mode 190R to the first boost output mode 192R or the condition for transitioning from the first boost output mode 192R to the second boost output mode 194R.

[001008] The operation of the first state machine associated with the logic circuit 104R, depicted in Figure 4R, will be described with continuing reference to Figure 3R and Figure 5R. In the shunt output mode 188R, the logic circuit 148R configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72 is in a closed state

(conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3R is configured to provide a switching voltage, V_{SW}, substantially equal to ground. In response to assertion of the series level indication 152R, which indicates that the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the series level threshold 126, the logic circuit 148R configures the first state machine to transition to the series output mode 190R. Otherwise, the state machine remains in the shunt output mode 188R.

[001009] In the series output mode 190R, the logic circuit 148R configures the series switch control output 162 such that the series switch 70 (Figure 3R) is in a closed state (conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72 (Figure 3R) is in an open state (not conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26 of Figure 3R is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}.

[001010] In response to de-assertion of the shunt level indication 150R, which indicates that feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124, the logic circuit 148R configures the first state machine to transition to the shunt output mode 188R. However, in response to assertion of the first boost level indication 154R, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the first boost level threshold 128, the logic circuit 148R configures the first state machine to transition to the first boost output mode 192R. Otherwise, the first state machine remains in the series output mode 190R.

[001011] In the first boost output mode 192R, the logic circuit 148R configures the series switch control output 162 such that the series switch 70 is in an open

state (not conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3R is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the shunt level indication 150R, which indicates that the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124, the logic circuit 148R configures the first state machine to transition to the shunt output mode 188R. However, in response to assertion of the second boost level indication 156R, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the second boost level threshold 130, the logic circuit 148R configures the first state machine to transition to the second boost output mode 194R. Otherwise, the first state machine remains in the first boost output mode 192R.

[001012] In the second boost output mode 194R, the logic circuit 148R, depicted in Figure 4R, configures the series switch control output 162 such that the series switch 70, depicted in Figure 3R, is in an open state (not conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72, depicted in Figure 3R, is in an open state (not conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26, depicted in Figure 3R, is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}. In response to de-assertion of the shunt level indication 150R, which indicates that the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124, the first state machine transitions to the shunt output mode 188R. Otherwise, the state machine remains in the second boost output mode 194R.

[001013] As a result, the transition from the shunt output mode 188R to the series output mode 190R and the transition back into the shunt output mode 188R may be affected by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Otherwise, transitions between the series output mode 190R and the first boost output mode 192R and between the first boost output mode 192R and the second boost output mode 194R are not affected by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[001014] Operation of the second state machine of the logic circuit 148R, depicted in Figure 6R, will now be described with continuing reference to Figure 3R and Figure 4R. The second state machine includes a shunt output mode 196R, a series output mode 198R, a first boost output mode 200R, and a second boost output mode 202R. In addition, the second state machine uses the above-described boost lockout counter 184 and boost time counter 186 of the logic circuit 148R, which are the same in function and form as the boost lockout counter 184 and boost time counter 186 of the logic circuit 148R.

[001015] In the shunt output mode 196R, the logic circuit 148R configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72 is in a closed state (conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26, depicted in Figure 3R, is configured to provide a switching voltage, V_{SW}, substantially equal to ground. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to assertion of the series level indication 152R, which indicates that the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the series level threshold 126, the second state machine transitions to the series output mode 198R. Otherwise, the second state machine remains in the shunt output mode 196R.

[001016] In the series output mode 198R, the logic circuit 148R configures the series switch control output 162 such that the series switch 70 is in a closed state (conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a charging mode of operation. As a result, the switching voltage output 26, depicted in Figure 3R, is configured to provide a switching voltage, V_{SW}, substantially equal to the battery voltage, V_{BAT}. If the boost lockout counter 184 is enabled, the boost lockout counter 184 continues to countdown. In response to de-assertion of the shunt level indication 150R, which indicates that the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124, the logic circuit 148R configures the second state machine to transition to the shunt output mode 196R. However, in response to assertion of the first boost level indication 154R, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the first boost level threshold 128, the logic circuit 148R determines whether both the minimum charge time indicator is de-asserted and the first boost level indication 154R is asserted. If the minimum charge time indicator is de-asserted and the first boost level indication 154R is asserted, the logic circuit 148R configures the second machine to transition to the first boost output mode 200R. Otherwise, the logic circuit 148R prevents the second state machine from transitioning to the first boost output mode 200R until the minimum time indicator is de-asserted. Once both the minimum charge time indicator is de-asserted and the first boost level indication 154R is asserted, the logic circuit 148R configures the second state machine to transition to the first boost output mode 200R, resets the counter output of the boost time counter 186, and enables the boost time counter 186 to begin counting up. Otherwise, the second state machine remains in the series output mode 198R.

[001017] In the first boost output mode 200R, the logic circuit 148R configures the series switch control output 162 such that the series switch 70 is in an open

state (not conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a first boost mode of operation to provide 3/2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3R is configured to provide a switching voltage, V_{SW}, substantially equal to 3/2 x V_{BAT}. In response to de-assertion of the first boost level indication 154R, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the first boost level threshold 128, the logic circuit 148R configures the second state machine to transition to the series output mode 198R. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148R asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148R sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. However, in response to assertion of the second boost level indication 156R, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is greater than or equal to the second boost level threshold 130, the logic circuit 148R configures the second state machine to transition to the second boost output mode 202R. Otherwise, the second state machine remains in the first boost output mode 200R.

[001018] In the second boost output mode 202R, the logic circuit 148R configures the series switch control output 162 such that the series switch 70 is in an open state (not conducting). The logic circuit 148R also configures the shunt switch control output 164 such that the shunt switch 72 is in an open state (not conducting). In addition, the logic circuit 148R configures the charge pump mode control signal 60 to instruct the multi-level charge pump circuit 56 to be in a second boost mode of operation to provide 2 x V_{BAT} at the charge pump output 64. As a result, the switching voltage output 26 of Figure 3R is configured to provide a switching voltage, V_{SW}, substantially equal to 2 x V_{BAT}.

[001019] In response to de-assertion of the first boost level indication 154R, which indicates that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is less than the first boost level threshold 128, the logic circuit 148R configures the second state machine to transition to the series output mode 198R. If the count output of the boost time counter 186 exceeds the maximum boost time parameter, the logic circuit 148R asserts a minimum charge time indicator. In response to the minimum charge time indicator being asserted, the logic circuit 148R sets the count value of the boost lockout counter 184 and enables the boost lockout counter 184 to begin counting down. Otherwise, the second state machine remains in the second boost output mode 202R.

[001020] Accordingly, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, only affect the operation of the second state machine associated with the logic circuit 148R when the second state machine is transitioning between the shunt output mode 196R and the series output mode 198R.

[001021] As a result, the transitions from the shunt output mode 196R to the series output mode 198R may be affected by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Otherwise, transitions between the series output mode 198R and the first boost output mode 200R, between the first boost output mode 200R and the second boost output mode 202R are not affected by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[001022] Figure 38B depicts another embodiment of a pseudo-envelope follower power management system 10QB configured to minimize the negative impact of feedback delay on the power conversion efficiency of the pseudo-envelope follower power management system 10QB. The embodiment of the pseudo-envelope follower power management system 10QB depicted in Figure 38B is similar in form and function to the pseudo-envelope follower power management system 10QA depicted in Figure 38A except the multi-level charge pump buck converter 12Q is replaced with a buck converter 13M. The buck converter 13M is similar in form and function to the previously described embodiments of the buck converters 13A, 13G, 13K, 13L depicted respectively in Figures 18C-D, Figure13, Figure 17A, Figure 23B and Figure 23D, except the buck

converter 13M is configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, from the feedback delay compensation circuit 852. As depicted in Figure 38B, the switcher control circuit 259 is configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[001023] The parallel amplifier circuit 14Q in the pseudo-envelope follower power management system 10QB depicted in Figure 38B functions similar to the manner in which the parallel amplifier circuit 14Q acts in the pseudo-envelope follower power management system 10QB depicted in Figure 38B. Thus, the parallel amplifier circuit 14Q acts as a master to control the power amplifier supply voltage, V_{CC}, at the power amplifier supply output 28 while controlling the buck converter 13M. The parallel amplifier circuit 14Q regulates the power amplifier supply voltage, V_{CC}, by sourcing and sinking current through the coupling circuit 18, based on the received V_{RAMP} signal, to compensate for either the over or under generation of the power inductor current, I_{SW_OUT}, provided from the power inductor 16 due to changes in the switching voltage, V_{SW}, provided at the switching voltage output 26 of the buck converter 13M. The parallel amplifier circuit 14Q controls the changes in the switching voltage, V_{SW}, provided at the switching voltage output 26, based on the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, provided to the buck converter 13M as feedback signals to govern the operation of the buck converter 13M. As discussed previously with respect to the pseudo-envelope follower power management system 10QA depicted in Figure 38A, by way of example, and not by limitation, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, depicted in Figure 38B, is formed by the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, from the parallel amplifier sense circuit 36. Thus, as discussed above, in other embodiments of the pseudo-envelope follower power management system 10QB, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, may also include contributions from the scaled high frequency ripple compensation current

estimate 418, I_{COR_SENSE}, and/or the scaled open loop assist circuit output current estimate, I_{ASSIST_EST}. Accordingly, while Figure 38A depicts that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, provided to the multi-level charge pump buck converter 12Q only includes the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, this is by way of example and not by limitation. As previously discussed, other embodiments of the parallel amplifier circuit 14Q of the pseudo-envelope follower power management system 10QB may include an embodiment of the open loop assist circuit 39, depicted in Figure 2A, and/or an embodiment of the open loop ripple compensation assist circuit 414 depicted in Figure 23B. Thus, in some embodiments of the pseudo-envelope follower power management system 10QB, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, may further include the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, and/or the scaled open loop assist circuit output current estimate, I_{ASSIST_SENSE},

[001024] In some embodiments of the pseudo-envelope follower power management system 10QB, the feedback delay compensation circuit 852 may be incorporated into the buck converter 13M. However, for the sake of simplicity of description, and not by way of limitation, the feedback delay compensation circuit 852 depicted in Figure 38B is shown as being separate from the buck converter 13M.

[001025] Similar to the operation of the switcher control circuit 52 of the multi-level charge pump buck converter 12Q depicted in Figure 38A, the switcher control circuit 259 may be configured to use to raise or lower the effective thresholds used by the switcher control circuit 259 to control changes between modes of operation of the buck converter 13M, where each mode of operation corresponds to a particular voltage level of the switching voltage, V_{SW}, provided at the switching voltage output 26 to the power inductor 16.

[001026] The operation of the embodiment of the feedback delay compensation circuit 852 depicted in Figure 39A and the embodiment of the differential feedback delay compensation circuit 852A depicted in Figure 39B described above are applicable to the various embodiments of the buck converter 13M that

are configured to use the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, generated by the feedback delay compensation circuit 852. For the sake of simplicity, and not by way of limitation, the discussion of the embodiments of the buck converter 13M that are configured to use the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will be done with the understanding that the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, depicted in Figure 38B, is substantially equal to the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$.

[001027] As depicted in Figure 38B, some embodiments of the buck converter 13M may be configured to interoperate with a frequency locked loop circuit 54 in a fashion similar to the buck converter 13A depicted in Figure 18C. One example embodiment of the switcher control circuit 259 of the buck converter 13M is the switcher control circuit 52M, depicted in Figure 3M, which is configured to interoperate with the frequency locked loop circuit 54. The switcher control circuit 52M, depicted in Figure 3M, is similar in form and function to the embodiment of the switcher control circuit 52E depicted in Figure 3E, except, the switcher control circuit 52M, depicted in Figure 3M, is configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Unlike the switcher control circuit 52E, depicted in Figure 3E, the switcher control circuit 52M includes a summing circuit 136A configured to receive a scaled parallel amplifier circuit output current estimate 138 from the multiplier circuit 134, the threshold offset current 42, , $I_{THRESHOLD_OFFSET}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The summing circuit 136A subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the sum of the scaled parallel amplifier circuit output current estimate 138 and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to form a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, that is received by the threshold detector and control circuit 132E. The compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, may be used as a composite control signal for the first comparator 140 and the second comparator 142, as depicted in Figure 4E. The threshold detector and control circuit 132E, depicted in Figure 4E, includes the

shunt level threshold 124 and the series level threshold 126 coupled to the positive terminal of the first comparator 140 and the second comparator 142, respectively. The negative terminal of the first comparator 140 and the second comparator 142 are configured to receive the compensated parallel amplifier circuit output current estimate I_{PAWA_COMP}. In this case, because only the magnitude of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is scaled by the threshold scalar 137A, the average switching frequency of operation of the buck converter 13M is adjusted independent of the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is used to regulate the offset voltage, V_{OFFSET}, between the power amplifier supply output 28 and the parallel amplifier output 32A, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. Alternatively, similar to the alternative embodiments discussed with respect to Figure 3A, some embodiments of the switcher control circuit 52M (not depicted) may scale a sum of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, with the threshold scalar 137A before subtracting the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. In this case, because the magnitude of the sum of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is scaled by the threshold scalar 137A, the average switching frequency of operation of the buck converter 13M is adjusted independent of the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, which is used to regulate the offset voltage, V_{OFFSET}. In still another alternative embodiment of the switcher control circuit 52M (not depicted), the multiplier circuit 134 scales the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, less the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, by the threshold scalar 137A before adding the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. In this case, the frequency locked loop circuit 54A adjusts the average switching frequency of operation of the multi-level charge pump buck converter 12Q

independent of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As another alternative embodiment, the switcher control circuit 52M (not depicted) may scale the sum of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, less the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, by the threshold scalar 137A to generate the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}.

[001028] Operationally, the threshold detector and control circuit 132E functions substantially the same as previously described relative to the buck converter 13A, depicted in Figure 18C. However, the effective level of the shunt level threshold 124 and the series level threshold 126 relative to the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, may be raised or lowered by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. For example, in the case where the slope of the V_{RAMP} signal is positive, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is positive, which will tend to raise the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will tend to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, the relative magnitude of the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, needed to cause the shunt level indication 150A and the series level indication 152A to transition from being de-asserted to being asserted is asserted is decreased. In other words, when the slope of the V_{RAMP} signal is positive, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, lowers the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, at which each of the first comparator 140 and the second comparator 142, transitions from a digital logic low state to a digital logic high state. As a result, the switcher control circuit 52M, depicted in Figure 3M, tends to increase the switching voltage, V_{SW}, sooner than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present. Alternatively, when the V_{RAMP} signal is decreasing such that the slope of the derivative of the V_{RAMP}

signal is negative, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is negative, which will tend to lower the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will tend to lower the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, needed to cause the shunt level indication 150A and the series level indication 152A to transition from being asserted to being de-asserted is decreased. As a result, when the slope of the derivative of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, tends to cause the switcher control circuit 52M, depicted in Figure 3M, to decrease the switching voltage, V_{SW}, sooner than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present.

[001029] As an example, the behavior of the first state machine, depicted in Figure 5E, associated with the logic circuit 148E, depicted in Figure 4E, relative to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, changes depending on the value of the feedback delay compensation signal 854. As a first example, when the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, raises the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}, the first state machine tends to shift to a mode of operation that provides a higher switching voltage, V_{SW}, at the switching voltage output 26. As a result, for example, when the first state machine, depicted in Figure 5E, is in the shunt output mode 188E, the first state machine tends to transition to the series output mode 190E when the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, is at a lower magnitude. This effectively causes the first state machine to advance in time the transition from the shunt output mode 188E to the series output mode 190E in response to the V_{RAMP} signal. The earlier transition by the first state machine from the shunt output mode 188E to the series output mode 190E is due to the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, lowering the effective threshold level of the series level threshold 126 by increasing the magnitude of the compensated

parallel amplifier circuit output current estimate, I_{PAWA_COMP}. As a result, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by lowering the effective threshold level of the series level threshold 126.

[001030] However, as a second example, when the slope of the derivative of the V_{RAMP} signal is negative, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will lower the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. As a result, the first state machine tends to shift to a mode of operation that provides a lower switching voltage, V_{SW}, at the switching voltage output 26. For example, when the first state machine, depicted in Figure 5E, is in the series output mode 190E, the first state machine tends to transition to the shunt output mode 188E more readily with respect to the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is lowering the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}. This effectively causes the first state machine to advance in time the transition from the series output mode 190E to the shunt output mode 188E.

[001031] As another alternative embodiment of the buck converter 13M, depicted in Figure 38B, that interoperates with the frequency locked loop circuit 54, the buck converter 13M may include a switcher control circuit 259 similar to the switcher control circuit 52N depicted in Figure 3N. The switcher control circuit 52N depicted in Figure 3N is similar in form and function to the switcher control circuit 52F, depicted in Figure 3F. However, unlike the switcher control circuit 52F depicted in Figure 3F, the switcher control circuit 52N, depicted in Figure 3N, includes a threshold and control circuit 132N configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As depicted in Figure 4N, the threshold and control circuit 132N includes the logic circuit 148F and is similar in form and function to the threshold and control circuit 132F, depicted in Figure 4F, except the threshold and control circuit 132N includes a

summing circuit 136A configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, generated by the parallel amplifier circuit 14Q, depicted in Figure 38B, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The summing circuit 136A subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the sum of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to generate a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', which may be used as a composite control signal for the first comparator 140 and the second comparator 142, depicted in Figure 4N. Similar to the operation of the threshold and control circuit 132F, depicted in Figure 4F, the threshold and control circuit 132N depicted in Figure 4N is configure to provide the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}' to the negative terminal of the first comparator 140 and the second comparator 142, depicted in Figure 4N. Also similar to the operation of the threshold and control circuit 132F, depicted in Figure 4F, the threshold and control circuit 132N depicted in Figure 4N includes the frequency locked loop circuit 54B. The frequency locked loop circuit 54B may be configured to adjust the magnitude of the threshold scalar' 137B to maintain an average switching frequency of operation of the buck converter 13M based on a target average frequency of operation parameter.

[001032] Similar to the operation of the threshold detector and control circuit 132M, depicted in Figure 4M, the threshold detector and control circuit 132N is configured such that the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, can raise or lower the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}' depending upon the slope of the derivative of the V_{RAMP} signal. As a result, similar to the behavior of the first state machine, depicted in Figure 5E, associated with the logic circuit 148E, the behavior of the first state machine, depicted in Figure 5F, associated with the logic circuit 148F, relative to the magnitude of the scaled parallel amplifier output current estimate,

$I_{PARA_AMP_SENSE}$, will change depending on the slope of the V_{RAMP} signal used to generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[001033] As a first example, for the case where the slope of the V_{RAMP} signal is positive, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will be positive, which increases the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the first state machine, depicted in Figure 5F, will have a greater tendency to shift to or stay in the series output mode 190F. However, for the case where the slope of the V_{RAMP} signal is negative, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is negative, which decreases the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the first state machine, depicted in Figure 5F, will have a greater tendency to shift to or stay in the shunt output mode 188F.

[001034] For example, in the case where the V_{RAMP} signal is increasing in magnitude, the slope of the derivative of the V_{RAMP} signal is positive. The magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is positive, which increases the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will tend to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, effectively decreases the effective threshold points at which the shunt level indication 150B and the series level indication 152B transition from being de-asserted to being asserted with respect to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. Thus, the buck converter 13M will tend to respond to the change in the V_{RAMP} signal when the parallel amplifier output current, I_{PARA_AMP}, is at a lower magnitude, which reduces the average current sourced and sunk by the parallel amplifier 35.

[001035] Although Figure 38B depicts the buck converter 13M as having the frequency locked loop circuit 54, some embodiments of the buck converter 13M may not include the frequency locked loop circuit 54 or the frequency locked loop

circuit 54 may be disabled. In this case, the switcher control circuit 259 of the buck converter 13M may be configured similar to the switcher control circuit 52P depicted in Figure 3P. The switcher control circuit 52P, depicted in Figure 3P, is similar in form and function to the switcher control circuit 52G, depicted in Figure 3G, except the switcher control circuit 52P includes a threshold detector and control circuit 132P that is configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As depicted in Figure 4P, the threshold detector and control circuit 132P is similar in form and function to the threshold detector and control circuit 132G, depicted in Figure 3G, except the threshold detector and control circuit 132P includes the summing circuit 136A configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. The summing circuit 136A subtracts the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from the sum of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, and the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to generate a compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', which may be used as a composite control signal for the first comparator 140 and the second comparator 142, depicted in Figure 4P.

[001036] As depicted in Figure 4P, the threshold detector and control circuit 132P is configured such that the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, can raise or lower the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}' depending upon the slope of the derivative of the V_{RAMP} signal. As a result, the behavior of the first state machine of the logic circuit 146G, depicted in Figure 5G, relative to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, will change depending on the slope of the V_{RAMP} signal used to generate the feedback delay compensation signal 854.

[001037] As a first example, referring to Figure 5G with continuing reference to Figure 4P, for the case where the slope of the V_{RAMP} signal is positive, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is

positive, which will tend to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the first state machine, depicted in Figure 5G, will have a greater tendency to shift to or stay in the series output mode 190G. However, for the case where the slope of the V_{RAMP} signal is negative, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is negative, which will tend to decrease the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. As a result, the first state machine, depicted in Figure 5G, will have a greater tendency to shift to or stay in the shunt output mode 188G.

[001038] For example, in the case where the slope of derivative of the V_{RAMP} signal is positive, the V_{RAMP} signal is increasing in magnitude. The magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is positive, which tends to increase the value of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}'. Because the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, will tend to increase the magnitude of the compensated parallel amplifier circuit output current estimate, I_{PAWA_COMP}', the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, effectively decreases the effective threshold points at which the shunt level indication 150C or the series level indication 152C transition from being de-asserted to being asserted with respect to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. Thus, the buck converter 13M having the switcher control circuit 52P, depicted in Figure 3P, will tend to responds to the change in the V_{RAMP} signal when the parallel amplifier output current, I_{PARA_AMP}, is at a lower magnitude, which reduces the average current sourced and sunk by the parallel amplifier 35.

[001039] Although Figure 38B depicts the buck converter 13M as having a V_{OFFSET} loop circuit 41, some embodiments of the buck converter 13M may not include a V_{OFFSET} loop circuit 41. For example, in the case where the coupling circuit 18 is a wire, the offset voltage, V_{OFFSET}, generated across the coupling circuit 18 is approximately zero. By way of example, and not by limitation, for an embodiment of the buck converter 13M that does not include the V_{OFFSET} loop

circuit 41, the buck converter 13M may include a switcher control circuit 259 similar to the switcher control circuit 52Q depicted in Figure 3Q. The switcher control circuit 52Q depicted in Figure 3Q is similar in form and function to the switcher control circuit 52H depicted in Figure 3H. However, unlike the switcher control circuit 52H, depicted in Figure 3H, the switcher control circuit 52Q includes a threshold and control circuit 132Q configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$.

[001040] Figure 4Q depicts an embodiment of the threshold and control circuit 132Q that is similar in form and function to the embodiment of the threshold and control circuit 132H, depicted in Figure 4H. However, unlike threshold and control circuit 132H, depicted in Figure 4H, the threshold and control circuit 132Q includes a summer circuit 136B configured to receive the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. The summer circuit 136B adds the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, and the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to generate a feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, which may be used as a composite control signal for the first comparator 140 and the second comparator 142, depicted in Figure 4Q. The feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is coupled to the negative terminal of the first comparator 140 and the second comparator 142. Similar to the threshold and control circuit 132H, depicted in Figure 4H, the threshold and control circuit 132Q, depicted in Figure 4Q, includes the logic circuit 148H.

[001041] The operation of the first state machine of the logic circuit 148H is changed by the addition of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, to form the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. For example, unlike the operation of the first state machine, depicted in Figure 5H, of logic circuit 148H, the transition between the states of the first state machine of the logic circuit 148H used in the threshold and control circuit 132Q, depends on the feedback compensated parallel

amplifier circuit estimate 866, I_{PAWA_FB}, instead of the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$.

[001042] As an example, the operation of the first state machine of the logic circuit 148H of the threshold and control circuit 132Q, depicted in Figure 4Q, is depicted in Figure 5Q. As depicted in Figure 5Q, the transitions between the shunt output mode 188Q and the series output mode 190Q are dependent upon the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. For example, the logic circuit 148H transitions the first state machine from the shunt output mode 188Q to the series output mode 190Q when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is greater than or equal to the series level threshold 126. Similarly, the logic circuit 148H transitions the first state machine from the series output mode 190Q to the shunt output mode 188Q when the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, is less than the shunt level threshold 124. Otherwise, the form and function of the shunt output mode 188Q and the series output mode 190Q are substantially the same as the shunt output mode 188H and series output mode 190H of the state first machine of the logic circuit 148H, depicted in Figure 5H.

[001043] Thus, when the slope of the derivative of the V_{RAMP} signal is positive, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is positive, which will tend to increase the magnitude of the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}. As a result, the effective threshold level at which the shunt level indication 150D and the series level indication 152D transition from being de-asserted to being asserted is lowered relative to the magnitude of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. Accordingly, the switcher control circuit 52Q will tend to increase the switching voltage, V_{SW}, sooner than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not added to the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to form the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB} when the slope of the derivative of the V_{RAMP} signal is positive. Similarly, when the slope of the derivative of the V_{RAMP}

signal is negative, the magnitude of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, is negative, which will tend to reduce the magnitude of the feedback compensated parallel amplifier circuit estimate 866, I_{PAWA_FB}, relative to the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. As a result, as depicted in Figure 5Q, the first state machine of the logic circuit 148H as used in the threshold and control circuit 132Q will tend to shift to a mode of operation that provides a lower switching voltage, V_{SW}, at the switching voltage output 26 when the magnitude the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is lower because feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, provides an early indication of the direction in which the target voltage level for the power amplifier supply voltage, V_{CC}, to the buck converter 13M. Thus, as described above, the example embodiments of the multi-level charge pump buck converter 12M, depicted in Figure 38A, and the example embodiments of buck converter 13M, depicted in Figure 38B, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, compensates for the feedback delay associated with generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, by providing an early indication of the direction in which the target voltage level of the power amplifier supply voltage, V_{CC}, is moving based on the slope of the derivative of the V_{RAMP} signal.

[001044] In some alternative embodiments (not depicted) of the pseudo-envelope follower power management system 10QA and the pseudo-envelope follower power management system 10QB, the switcher control circuit 52 may be configured to change the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 based on the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As a result, the threshold levels at which the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 change between an asserted state and an unasserted state are modified by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, in order to compensate for the feedback delay. As an example, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, may be used to reduce the magnitude of

the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 provided to the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 when the slope of the V_{RAMP} signal is positive. Likewise, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, may be used to increase the magnitude of the magnitude of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128 provided to the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 when the slope of the V_{RAMP} signal is negative. As a result, similar to the above discussed embodiments of the multi-level charge pump buck converter 12Q, for example, when the slope of the V_{RAMP} signal is positive, the effective thresholds used by the switcher control circuit 52 to control a change between each mode of operation of the multi-level charge pump buck converter 12Q is reduced. As an example, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, may be provided to the programmable threshold circuit 122 (not depicted) to change the threshold levels used by the switcher control circuit 52 to control the switching voltage, V_{SW}, at the switching voltage output 26. In this case, the programmable threshold circuit 122 may be configured to generate the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, based on the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, in combination with the shunt level threshold parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter. As a result, the programmable threshold circuit 122 may be configured to decrease the magnitude of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 when the slope of the derivative of the V_{RAMP} signal is positive and increase the magnitude of the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 when the slope of the derivative of the V_{RAMP} signal is negative.

[001045] Alternatively, the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, may be subtracted from the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128 to create a feedback compensated shunt level threshold, a feedback compensated series level threshold, a feedback compensated first boost level threshold, and a feedback compensated second boost level threshold, where the feedback compensated shunt level threshold, the feedback compensated series level threshold, the feedback compensated first boost level threshold, and the feedback compensated second boost level threshold are provided to the positive input of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146, respectively. As a result, the switching voltage, V_{SW}, will be increased sooner in response to the V_{RAMP} signal increasing in value than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present. Similarly, when the slope of the V_{RAMP} signal is negative, the effective thresholds used by the switcher control circuit 52 to control a change between each mode of operation of the multi-level charge pump buck converter 12Q is increased. As a result, the switching voltage, V_{SW}, will be lowered sooner in response to the V_{RAMP} signal decreasing in value than if the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, was not present. In each case, the overall impact is to compensate for the feedback delay associated with the generation of the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and reduce the average current sourced and sunk by the parallel amplifier 35. A similar technique may be applied to the embodiments of the switcher control circuit 259 of the buck converter 13M.

[001046] Figure 40A depicts a high level illustration of a pseudo-envelope tracking modulated power supply system 868 that may include a radio frequency power amplifier 869 configured to be powered by or under the control of a power management system 870.

[001047] The pseudo-envelope tracking modulated power supply system 868 may be similar in form and function and include the various combinations of the features, functions, circuits, circuitry, techniques, and methods as those

previously described with respect to embodiments of the pseudo-envelope follower power management systems 10, 10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10MA, 10MB, 10PA, 10PB, 10PC, 10PD, 10PE, 10Q and 10QB. As discussed with respect to respect to embodiments of pseudo-envelope follower power management systems 10, 10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L, 10MA, 10MB, 10PA, 10PB, 10PC, 10PD, 10PE, 10Q and 10QB, the power amplifier supply voltage, V_{CC}, may also be referred to as a modulated power supply voltage, V_{CC}, that is generated at a modulated power supply output 876.

[001048] Similar to other previously described switch mode power supply converters, multi-level charge pump buck converters, and parallel amplifier circuits, the switch mode power supply converter 872 and the parallel amplifier circuit 874 may be configured to receive an input supply voltage from a battery 20. The battery 20 may provide a supply voltage substantially equal to the battery voltage, V_{BAT}.

[001049] For the sake of simplicity of description, and not by way of limitation, the pseudo-envelope tracking modulated power supply system 868 may include a controller 50 coupled via a control bus 44 to the switch mode power supply converter 872 and the parallel amplifier circuit 874. The switch mode power supply converter 872 may be arranged to cooperatively operate with a parallel amplifier circuit 874 to generate the modulated power supply voltage, V_{CC}, at the modulated power supply output 876. For example, in some embodiments, the controller 50 may configure the switch mode power supply converter 872 and the parallel amplifier circuit 874 to operate in various power level modulation modes depending upon the expected output power to be generated by the radio frequency power amplifier 869 during a transmission of information. In some embodiments, the control functions described with respect to the controller 50 may be incorporated into a digital baseband modem or transceiver circuit that provides a differential V_{RAMP} signal as a control signal to the power management system 870 based on a radio frequency input signal provided to the radio frequency power amplifier 869 for transmission.

[001050] The power management system 870 may be configured to receive a differential V_{RAMP} signal having a non-inverted V_{RAMP} signal component, V_{RAMP}+, and an inverted V_{RAMP} signal component, V_{RAMP}-. In some alternative embodiments, the power management system 870 may be configured to receive a V_{RAMP} signal that is a single ended V_{RAMP} signal, a differential V_{RAMP} signal, and/or both the single ended V_{RAMP} signal and the differential V_{RAMP} signal. The differential V_{RAMP} signal may be provided as a control signal to govern generation of the modulated power supply voltage, V_{CC}. Illustratively, the switch mode power supply converter 872 and the parallel amplifier circuit 874 may each be configured to receive the differential V_{RAMP} signal.

[001051] The switch mode power supply converter 872 may include the switching voltage output 26 in communication with the modulated power supply output 876. A power inductor 16 may be coupled between the switching voltage output 26 and the modulated power supply output 876.

[001052] The parallel amplifier circuit 874 may include a parallel amplifier circuit output 874A in communication with the modulated power supply output 876. Illustratively, in some embodiments, a coupling capacitor 18A is coupled between the modulated power supply output 876 and the parallel amplifier circuit output 874A. In addition, the parallel amplifier circuit 874 may also include a first linear regulator output 874B, LDO_1 OUTPUT, in communication with the modulated power supply output 876. In some power level modulation modes, the power management system 870 may configure the first linear regulator output 874B, LDO_1 OUTPUT, to provide a high impedance path with respect to ground. In other power level modulation modes, the power management system 870 may configure the first linear regulator output 874B, LDO_1 OUTPUT, to apply a first linear regulator output current 878A, I_{LDO}, to the modulated power supply output 876 to regulate the modulated power supply voltage, V_{CC}.

[001053] The parallel amplifier circuit 874 may also include a second linear regulator output 874D, LDO_2 OUTPUT, in communication with a CMOS logic supply input 869C. In some power level modulation modes, the power management system 870 may configure the second linear regulator output 874D,

LDO_2 OUTPUT, to provide a second linear regulator output voltage, V_{LDO2}, to the CMOS logic supply input 869C as a function of the battery voltage, V_{BAT}. As an example, the CMOS logic supply input 869C include a minimum CMOS logic supply voltage threshold. Accordingly, the power management system 870 may configure the second linear regulator output 874D, LDO_2 OUTPUT, to provide a second linear regulator output voltage, V_{LDO2}, to the CMOS logic supply input 869C that is at least equal to the minimum CMOS logic supply voltage threshold.

[001054] The parallel amplifier circuit 874 may also include a switch mode power supply converter control output 874E configured to output a switch mode power supply feedback signal 40A to the switch mode power supply converter 872, depicted in Figures 40B and 46A. In addition, the parallel amplifier circuit 874 may provide a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the switch mode power supply converter 872. The parallel amplifier circuit 874 may receive the modulated power supply voltage, V_{CC}, from the modulated power supply output 876 at a modulated power supply voltage feedback input 874F. The parallel amplifier circuit 874F may use the input to the power supply voltage feedback input 874F may be used as a feedback signal to regulate the modulated power supply voltage, V_{CC}.

[001055] In some embodiments, the radio frequency power amplifier 869 may be a linear radio frequency power amplifier. The radio frequency power amplifier 869 may include a radio frequency power amplifier input configured to receive a modulated radio frequency input signal from a digital baseband processing portion of the transceiver or modem, where the modulated radio frequency input signal has an input power, P_{IN}. In addition, the radio frequency power amplifier 869 may also include a radio frequency power amplifier output in communication with an antenna via the radio frequency duplexer and switch (not shown). The radio frequency power amplifier 869 may generate an amplified modulated radio frequency output signal having an output power P_{OUT} at the radio frequency power amplifier output.

[001056] In some embodiments, the radio frequency power amplifier 869 may include a collector voltage supply input 869A configured to receive the modulated power supply voltage, V_{CC}, from the modulated power supply output 876. The radio frequency power amplifier 869 may further include a battery voltage supply input 869B configured to receive the battery voltage, V_{BAT}, from the battery 20. The radio frequency power amplifier 869 may also include a CMOS logic supply input 869C configured to receive a second linear regulator output voltage, V_{LDO2}.

[001057] Another example embodiment of the radio frequency power amplifier 869 is the radio frequency power amplifier 869' depicted in Figure 46B. Figure 46B depicts that the radio frequency power amplifier 869' includes CMOS logic 869E, a driver 869F, and a final output stage 869G. In some embodiments, the driver supply voltage input 869D may have a minimum driver supply voltage that is a function of the output power to be generated by the radio frequency power amplifer 869'. For example, the driver 869F may have a minimum driver supply voltage threshold that is based on a relationship between a minimum driver supply voltage and the output power P_{OUT} generated by the radio frequency power amplifier 869'. In some embodiments, the minimum driver supply voltage threshold may be further dependent on the input power P_{IN} or drive level of the radio frequency input signal provide to the radio frequency power amplifer 869' for transmission.

[001058] Similar to the radio frequency power amplifier 869, the radio frequency power amplifier 869' may include a collector voltage supply input 869A configured to receive the modulated power supply voltage, V_{CC}, a battery voltage supply input 869B configured to receive the battery voltage, V_{BAT}, a CMOS logic supply input 869C configured to receive a CMOS logic supply voltage 878C, V_{CMOS}, and a driver supply voltage input 869D configured to receive the second linear regulator output voltage, V_{LDO2}.

[001059] Returning to Figure 40A with continuing reference to Figure 46B, in some embodiments, the radio frequency power amplifier 869 may be configured to selectively provide either the battery voltage, V_{BAT}, received at the battery voltage supply input, 869B, or the second linear regulator output voltage, V_{LDO2},

received at the CMOS logic supply input 869C to power the CMOS logic 869E as a function of the battery voltage and the minimum CMOS logic supply voltage threshold. For example, in the case where the battery voltage, V_{BAT}, is above the minimum CMOS logic supply voltage threshold, the radio frequency power amplifier 869 supplies the battery voltage, V_{BAT}, to the CMOS logic 869E. In the cases where the battery voltage, V_{BAT}, falls below the minimum CMOS logic supply voltage threshold, the radio frequency power amplifier 869 configures the CMOS logic 869E to be powered from the CMOS logic supply input 869C.

[001060] In some embodiments of the power management system 870, the power management system 870 may be configured to operate in various power level modulation modes based on an expected output power to be generated by the radio frequency power amplifier 869 during a data transmission. In addition, the power management system 870 may be reconfigured prior to each data transmission to minimize the energy drawn from the battery 20 during the data transmission. For example, some embodiments of the power management system 870 may be configured to operate in one of many power level modulation modes on a data transmission slot by data transmission slot basis.

[001061] As a non-limiting list of example power level modulation modes of operation, the power management system 870 may be configured to operate in a set of power level modulation modes including a high power modulation mode, a medium power modulation mode, and lower power modulation mode. As another example, in other embodiments, the power management system 870 may be configured to operate in a set of power level modulation modes including a high power modulation mode, a medium power modulation mode, a medium power average power tracking modulation modes, and a low power average power tracking modulation mode.

[001062] As a further example, in the slow tracking mode of operation, the power management system 870 may disable the switch mode power supply converter 872, and configure the parallel amplifier circuit 874 to track an envelope of a modulated radio frequency input signal to be transmitted by the radio frequency power amplifier 869 as a function of a slowly modulated or

unmodulated differential V_{RAMP} signal. In the no tracking mode of operation, the power management system 870 may further configure the parallel amplifier circuit 874 to provide a modulated power supply output voltage, V_{CC}, based on a substantially unmodulated differential V_{RAMP} signal. In the no tracking mode, the power management system 870 may be configured to generate a modulated power supply output voltage, V_{CC} that has a substantially fixed voltage level. In the slow tracking mode of operation, the parallel amplifier circuit 874 may be configured to slowly track the envelope differential V_{RAMP} signal.

[001063] To minimize energy consumed from the battery during a data transmission, the power management system 870 may enable and disable various elements and signal processing functions of the switch mode power supply converter 872 and the parallel amplifier circuit 874 as a function of the power level modulation mode of operation. In some embodiments, the power management system 870 may disable the least energy efficient element and signal processing functions as a function of the expected output power to be generated by the radio frequency power amplifier 869. For example, the power management system 870 may disable portions of the switch mode power supply converter 872, the parallel amplifier circuit 874, and/or a combination thereof as the expected output power of the radio frequency power amplifier 869 decreases to achieve an overall decrease in energy consumption from the battery during a data transmission. In addition, some embodiments of the power management system 870 may generate the modulated power supply output 876 using a less energy efficient device or power generation circuit in response to an expected output power of the radio frequency power amplifier 869 falling below a lower power modulation mode threshold in order to disable other energy consuming circuitry and achieve an overall reduction in energy drawn from the battery 20 during a data transmission.

[001064] As a non-limiting example, in some embodiments of the high power level modulation mode and the medium power modulation mode, the power management system 870 may configure the switch mode power supply converter 872 and the parallel amplifier circuit 874 to generate the modulated

power supply voltage, V_{CC}, based on the differential V_{RAMP} signal as a function of the expected output power to be generated by the radio frequency power amplifier 869 during the data transmission. As an example, in some embodiments of the high power modulation mode and the medium power modulation mode, the parallel amplifier circuit 874 may be configured to govern the operation of the switch mode power supply converter 872, regulate generation of the modulated power supply voltage, V_{CC}, as a function of the differential V_{RAMP} signal, and regulate the offset voltage, V_{OFFSET}, across the coupling capacitor 18A.

[001065] As an example, the parallel amplifier circuit 874 may be configured to apply a parallel amplifier output current, I_{PAWA_OUT}, from the parallel amplifier to regulate the modulated power supply voltage, V_{CC}, as a function of the differential V_{RAMP} signal. The parallel amplifier circuit may provide the switch mode power supply feedback signal 40A and a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to govern the operation of the switch mode power supply converter 872 and regulate the offset voltage, V_{OFFSET}, across the coupling capacitor 18A. In response to the switch mode power supply feedback signal 40A and a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and the differential V_{RAMP} signal, the switch mode power supply converter 872 may generate the switching voltage, V_{SW}, at the switching voltage output 26, and provide a delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, to the parallel amplifier circuit 874. In addition, the parallel amplifier circuit 874 may configure the first linear regulator output 874B, LDO_1 OUTPUT, to provide a high impedance path to ground. Depending on the battery voltage, V_{BAT}, the parallel amplifier circuit 874 may configure the second linear regulator output 874D, LDO_2 OUTPUT, to provide the second linear regulator output voltage, V_{LDO2}, at least equal to the minimum CMOS logic supply voltage to the CMOS logic supply input 869C of the radio frequency power amplifier 869.

[001066] As another non-limiting example, in some embodiments of the low power modulation mode, the power management system 870 may disable the switch mode power supply converter 872 and configure the switching voltage

output 26 to provide a high impedance path to ground. In addition, the parallel amplifier circuit output 874A may be configured to provide a low impedance path to ground to short the negative terminal of the coupling capacitor 18A to ground. To generate the modulated power supply voltage, V_{CC}, the first linear regulator output 874B, LDO_1 OUTPUT, may be configured to apply a linear regulator output current, I_{LDO}, to the modulated power supply output 876 as a function of the differential V_{RAMP} signal and a selected tracking mode of operation. The differential V_{RAMP} signal may be substantially constant or only slowly modulated during the data transmission. In the case where the differential V_{RAMP} signal is substantially contstant, the power management system 870 may configure the parallel amplifier circuit 874 to operate in a no tracking mode of operation. In the no tracking mode of operation, the first linear regulator output 874B, LDO_1 OUTPUT, may regulate the modulated power supply voltage, V_{CC}, to be substantially constant or unmodulated during data transmission. Alternatively, in the case where the differential V_{RAMP} signal slowly changes relative to the envelope of the radio frequency input signal provided to the radio frequency power amplifier 869, the power management system 870 may configure the first linear regulator output 874B, LDO_1 OUTPUT, to slowly track the differential V_{RAMP} signal during the data transmission.

[001067] In some embodiments of the low power modulation mode, the parallel amplifier circuit 874 may disable the second linear regulator output 874D, LDO_2 OUTPUT. In some alternative embodiments of the low power modulation mode, the parallel amplifier circuit 874 may configure the second linear regulator output 874D, LDO_2 OUTPUT, to selectively output a second linear regulator output voltage, V_{LDO2}, to a CMOS logic supply input 869C as a function of the battery voltage, V_{BAT}.

[001068] Figure 40B depicts a non-limiting example of the embodiments of the switch mode power supply converter 872 that may be selectively configured to operate in a number of various buck converter modes, a number of various envelope tracking modes, a number of various average power tracking modes, and/or a combination thereof as a function of an expected output power to be

generated by the radio frequency power amplifiers 869 and 869', depicted Figures 40A, 40C-E, and 46A-H. The switch mode power supply converter 872 may further include an off mode. The various embodiments of the switch mode power supply converter 872 are described with continuing reference to the various embodiments of the power management system 870, depicted in Figures 40A-C, the power management system 870A, depicted in Figures 46A-C, the power management system 870B and parallel amplifier circuit 874B', depicted in Figure 40D, the power management system 870C and parallel amplifier circuit 874C', depicted in Figure 40E, the power management system 870E and parallel amplifier circuit 874E', depicted in Figure 46E, power management system 870F and parallel amplifier circuit 874F', depicted in Figure 46F, the power management system 870G and parallel amplifier circuit 874G', depicted in Figure 46G, and the power management system 870H and parallel amplifier circuit 874H', depicted in Figure 46H.

[001069] As an example, the various envelope tracking modes may include one or more envelope tracking power modes of operation including a high power mode and a medium power mode. As another example, the various average power tracking modes may include one or more average power tracking modes of operation include a medium power average power tracking mode. The controller 50 may configure the switch mode power supply converter 872 to operate in the medium power average power tracking mode when the power management systems 870A-C and 870E-H are configured to operate in a medium power average power tracking modulation mode. The controller 50 may configure the switch mode power supply converter 872 to be in a high power mode when the power management systems 870, 870A-C, and 870E-H are configured to operate in the high power modulation mode. The controller 50 may configure the switch mode power supply converter 872 to be in a medium power mode when the power management systems 870, 870A-C, and 870E-H are configured to operate in the medium power modulation mode. The controller 50 may configure the switch mode power supply converter 872 to be in an off mode when the power management systems 870, 870A-C, and 870E-H are configured

to operate in either a low power modulation mode or a low power average power tracking modulation mode.

[001070] The switch mode power supply converter 872 may include embodiments of a switcher control circuit 880, the multi-level charge pump 882, a switching circuit 884, and an average frequency control circuit 885. The switcher control circuit 880, the multi-level charge pump 882, the switching circuit 884, and the feedback delay compensation circuit 852 may be configured to receive the battery voltage, V_{BAT}. Some embodiments of the switch mode power supply converter 872 may further include the feedback delay compensation circuit 852. The controller 50 may configure the switcher control circuit 880 to govern the operation of the multi-level charge pump 882 and the switching circuit 884 as a function of the power level modulation mode and the expected output power to be generated by the embodiments of the radio frequency power amplifiers 869 and 869' in response to a modulated radio frequency input signal to be transmitted. In some embodiments, the switcher control circuit 880 may also be configured to control the operation of the feedback delay compensation circuit 852 as a function of the power level modulation mode and the expected output power of the radio frequency power amplifiers 869 and 869'. In addition, in some embodiments, the feedback delay compensation circuit 852 may generate the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, as a function of the power level modulation mode and the expected output power of the radio frequency power amplifiers 869 and 869'.

[001071] As a non-limiting example, in the high power mode of operation, the controller 50 or the switcher control circuit 880 may configure the feedback delay compensation circuit 852 to operate as a function of a high power mode apparent gain to increase the aggressiveness of the feedback compensation provided by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. As the apparent gain of the feedback delay compensation circuit 852 is increased, the switch mode power supply converter 972 may respond to a change in the target voltage for the modulated power supply voltage, V_{CC}, provided by the differential V_{RAMP} circuit, which may increase the power efficiency of the various embodiments of

the parallel amplifier 928, depicted in Figures 40C-D and Figures 46B, 46E, and 46H, the parallel amplifier 928', depicted in Figures 46F-G,the parallel amplifier 928", depicted in Figures 40E.

[001072] In the medium power mode of operation, the controller 50 or the switcher control circuit 880 may configure the feedback delay compensation circuit 852 to operate as a function of a medium power mode apparent gain to decrease the aggressiveness of the feedback compensation provided by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, in order to prevent the switcher control circuit 880 from pre-maturely changing the switching voltage, V_{SW}. The feedback delay compensation circuit 852 may operate in an over aggressive manner when the apparent gain is set too high with respect to the expected output power to be generated by the radio frequency power amplifier 869 or 869' during a data transmission. Over aggressiveness of feedback compensation provided by the feedback delay compensation circuit 852 may result in pre-mature changes the switching voltage, V_{SW}, because the switch mode power supply converter 972 may overreact to a change in the target voltage for the modulated power supply voltage, V_{CC}, provided by the differential V_{RAMP} circuit. As a result, the switch mode power supply converter 872 may generate a switching voltage that provides too much or too little energy to the modulated power supply voltage, which may decrease the power efficiency of the various embodiments of the parallel amplifier 928, depicted in Figures 40C-D and Figures 46B, 46E, and 46H, the parallel amplifier 928', depicted in Figures 46F-G, the parallel amplifier 928", depicted in Figures 40E.

[001073] In some embodiments of the medium power mode, the controller 50 may set the apparent gain of the feedback delay compensation circuit 852 based on a sliding scale as a function of the expected output power to be generated by the radio frequency power amplifier 869 or 869' during the data transmission. As an alternative example, some embodiments of the switcher control circuit 880 may be further configured to adjust the apparent gain of the feedback delay compensation circuit 852 based on a segmentation mode of the switching

circuit 884. In some embodiments, the controller 50 or the switcher control circuit 880 may disable the feedback delay compensation circuit 852 the average power tracking mode and the off mode. For example, referring briefly to Figures 46A-B, some embodiments of a power management system 870A may disable the feedback delay compensation circuit 852 a medium power average power tracking mode and a low power average power tracking modulation mode. Similarly, referring briefly to referring briefly to Figures 40A-C and Figures 46A-B, some embodiments of the power manage system 870 and power management system 870A may disable the feedback delay compensation circuit 852 in a low power modulation mode, and enable the feedback delay compensation circiuit 852 in a high power modulation mode and a medium power modulation mode.

[001074] The switcher control circuit 880 may be configured to operate in the average power tracking mode in response to the power management systems 870A-C and 870E-H being configured to operate in the medium power average power tracking modulation mode. In the off mode, the switcher control circuit 880 may disable the multi-level charge pump 882 and the switching circuit 884, and configure the switching voltage output 26 to provide a high impedance path to ground. In the off mode, the switch mode power supply converter 872 may be configured to disable clocking signal that may be used by the µC charge pump circuit 262, depicted in Figures 40C, Figure 46B, and Figures 46E-H.

[001075] In a buck converter "bang-bang" mode of operation, the switcher control circuit 880 may disable the multi-level charge pump 882, and control the switching circuit 884 to swing the switching voltage, V_{SW}, between the battery voltage, V_{BAT}, and ground. In the multi-level charge pump buck converter mode, the switcher control circuit 880 may enable both the multi-level charge pump 882 and the switching circuit 884. The switcher control circuit 880 may further control the multi-level charge pump 882 and the switching circuit 884 to generate both buck level voltages and boost level voltages to provide the switching voltage,

V_{SW}, at the switching voltage output 26 as a function of the operational state of the switcher control circuit 880 and the power level modulation mode.

[001076] In the medium power average power tracking mode of operation, the switcher control circuit 880 may be configured to operate in a number of average power tracking "bang-bang" modes of operation. As an example, in some embodiments of an average power tracking "bang-bang" mode of operation, the switcher control circuit 880 may configure the multi-level charge pump 882 and the switching circuit 884 to switch the switching voltage, V_{SW}, between only a first bang-bang switching voltage, V_{SW_BB1}, and a second bang-bang switching voltage, V_{SW_BB2}, during a data transmission, where the first bang-bang switching voltage, V_{SW_BB1}, is less than the second bang-bang switching voltage, V_{SW_BB2}. But unlike a buck converter mode of operation in which the switching voltage swings between ground and the battery supply, V_{BAT}, the first bang-bang switching voltage, V_{SW_BB1}, may be substantially equal to ground, the battery voltage, V_{BAT}, or a switching voltage between ground and the battery voltage, V_{BAT}. The second bang-bang switching voltage, V_{SW_BB2}, may be substantially equal to the supply voltage, V_{BAT}, or a charge pump output voltage generated by the multi-level charge pump 882 from the battery voltage, V_{BAT}. The average power tracking "bang-bang" modes of operation may include an average power tracking "buck-buck" mode of operation and an average power tracking "buck-boost" mode of operation.

[001077] In the average power tracking "buck-buck" mode of operation, the switcher control circuit 880 may configured the multi-level charge pump 882 and the switching circuit 884 to generate a first bang-bang switching voltage, V_{SW_BB1}, and the second bang-bang switching voltage, V_{SW_BB2}, that are no greater than the battery voltage, V_{BAT}. For example, the switcher control circuit 880 may configure the multi-level charge pump 882 to generate only a bucked output voltage at the charge pump output 64. As an example, the switcher control circuit may configure the multi-level charge pump 882 to generate a first buck mode output voltage, V_{FIRST_BUCK}, substantially equal to 1/2 x V_{BAT} in a first buck mode of operation. In the average power tracking "buck-buck" mode, the

switcher control circuit 880 may disable the multi-level charge pump 882 provided the first bang-bang switching voltage, V_{SW_BB1}, and the second bang-bang switching voltage, V_{SW_BB2}, are a shunt mode output voltage substantially equal to ground and a series mode output voltage substantially equal to V_{BAT}.

[001078] In the average power tracking "buck-boost" mode, the first bang-bang switching voltage, V_{SW_BB1}, may be no greater than the battery voltage, V_{BAT}, and the second bang-bang switching voltage, V_{SW_BB2}, is a boost voltage that is greater than the battery voltage, V_{BAT}. In the average power tracking "buck-boost" mode, the switcher control circuit 880 may configure the multi-level charge pump 882 and the switching circuit 884 to generate the first bang-bang switching voltage, V_{SW_BB1}. The switcher control circuit 880 may configure the multi-level charge pump 882 to generate the second bang-bang switching voltage, V_{SW_BB2}. A further description of the average power tracking "bang-bang" modes of operation is provided below.

[001079] The switcher control circuit 880 may receive a feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, from a feedback delay compensation circuit 852 and a switch mode power supply feedback signal 40A from the parallel amplifier circuit 874. The switcher control circuit 880 may also receive the threshold offset current 42, $I_{THRESHOLD_OFFSET,}$ from the V_{OFFSET} loop circuit 41, depicted in Figure 40C and Figure 46B, or the V_{OFFSET} loop circuit 41C, depicted in Figures 40D-E and Figures 46E-H.

[001080] Some embodiments of the switcher control circuit 880 may be configured to form a composite control signal as a function of the various envelope tracking modes, the various average power tracking modes, and buck converter modes. As an example, the various embodiments of the switcher control circuit 880 may combine the various fractional amounts and combinations of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, the switch mode power supply feedback signal 40A, and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to form one or more composite control signals as a function of the power level modulation mode. In some embodiments, the composite control signal may depend on the power level modulation mode.

[001081] Some embodiments of the switcher control circuit 880 may form a composite control signal in a similar manner as the previously described embodiments of switcher control circuits 52, 52A-D, 52I-L, and 52R, depicted at least in Figures 2A, 2B, 3A-D, 3I-L, 3R, 4A-D, 4I-L, 4R, 5A-D, 5I-L, 5R, 6A-D, 6L, and 6R, where the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is replace by the switch mode power supply feedback signal 40A. As an example, referring to the various embodiments of the threshold detector and control circuits 132A-D and 132I-L depicted in Figures 4A-D, 4I-L, and 4R, the composite control signal is provided to the inverting input of each of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146. As an example, similar to the switcher control circuit 52D, depicted in Figure 4D, some embodiments of the switcher control circuit 880 may replace the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, with the switch mode power supply feedback signal 40A such that the switch mode power supply feedback signal 40A may be used as the composite control signal. In those embodiments of the switcher control circuit 880 that are similar the switcher control circuits 52R, depicted in Figure 4R, the switcher control circuit 880 may replace the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, with the switch mode power supply feedback signal 40A to form a first composite control signal and a second composite control signal. The first composite control signal may be provided to the inverting input of the first comparator 140 and the second comparator 142, and the second composite control signal may be provided to the inverting inputs of the third comparator 144 and the fourth comparator 146.

[001082] Depending on the power level modulation mode the expected output power to be generated by the radio frequency power amplifiers 869 and 869', and/or a combination thereof, the switcher control circuit 880 may compare the one or more composite control signals to one or more threshold levels to set an operational state of the switcher control circuit 880. In some embodiments, the level of contribution of the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, the switch mode power supply feedback signal 40A, and the threshold offset

current 42, $I_{THRESHOLD_OFFSET}$, to form the composite control signal may depend on the power level modulation mode. Also, as described below, in some embodiments of the power management system 870, depicted in Figures 40A-C, the power management system 870A, depicted in Figures 46A-C, the power management system 870B and parallel amplifier circuit 874B', depicted in Figure 40D, the power management system 870C and parallel amplifier circuit 874C', depicted in Figure 40E, the power management system 870E and parallel amplifier circuit 874E', depicted in Figure 46E, power management system 870F and parallel amplifier circuit 874F', depicted in Figure 46F, the power management system 870G and parallel amplifier circuit 874G', depicted in Figure 46G, and the power management system 870H and parallel amplifier circuit 874H', depicted in Figure 46H, the generation of the switch mode power supply feedback signal 40A, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, and/or a combination therof may depend on the power level modulation mode in which each of the embodiments of the power management systems 870 and 870A-H are configured to operate.

[001083] As an example, Figure 40C depicts an embodiment of the power management system 870 in which the parallel amplifier 928 may generate the switch mode power supply feedback signal 40A in the high power modulation mode and the low power modulation mode. In addition, the V_{OFFSET} loop circuit 41 may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the high power modulation mode and the medium power modulation mode.

[001084] As an example, Figure 40D depicts an embodiment of the power management system 870B in which the parallel amplifier 928 may generate the switch mode power supply feedback signal 40A in the high power modulation mode and the low power modulation mode. In addition, the V_{OFFSET} loop circuit 41C may generate the threshold offset current 42, $I_{THRESHOLD}$, in the high power modulation mode, the low power modulation mode, and the medium power average power tracking modulation mode.

[001085] As a further example, Figure 40E depicts an embodiment of the power management system 870C in which a parallel amplifier 928" may generate the

switch mode power supply feedback signal 40A in the high power modulation mode, the low power modulation mode, and the medium power average power tracking modulation mode. In addition, the V_{OFFSET} loop circuit 41C may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the high power modulation mode, the low power modulation mode, and the medium power average power tracking modulation mode. In some embodiments, the power management system 870C may disable one of the parallel amplifier 928" and the V_{OFFSET} loop circuit 41C as a function of the average some average power tracking "bang-bang" mode of operation.

[001086] As an example, Figure 46B depicts an embodiment of the power management system 870A in which the parallel amplifier 928 may generate the switch mode power supply feedback signal 40A in the high power modulation mode and the medium power modulation mode. In addition, the V_{OFFSET} loop circuit 41 may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the high power modulation mode and the medium power modulation mode. And the average power tracking controller 44 may generate an average power tracking control signal 966, which is provided as the switch mode power supply feedback signal 40A in the medium power average power tracking modulation mode.

[001087] As an example, the power management system 870C may disable the parallel amplifier 928" based on a selection of one of the average power tracking "buck-buck" modes and the average power tracking "buck-buck" modes the in order to regulate the generation of the switching voltage, V_{SW}, as a function of the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, generated by the V_{OFFSET} loop circuit 41C in the medium power average power tracking modulation mode. Alternatively, the power management system 870C may disable the based on a selection of one of the average power tracking "buck-buck" modes and the average power tracking "buck-buck" modes the in order to regulate the generation of the switching voltage, V_{SW}, as a function of the switch mode power supply feedback signal 40A generated by the parallel amplifier 928" in the medium power average power tracking modulation mode.

[001088] Advantageously, the power management system 870C may form the composite control signal to obtain the benefits associated with each of the various embodiments of the parallel amplifier 928" and the V_{OFFSET} loop circuit 41C. As an example, in the medium power average power tracking modulation mode, some embodiments of the parallel amplifier 928" may generate a modulation mode feedback signal that provides an indication of an instantaneous error voltage between the V_{RAMP} signal and the modulated power supply voltage, V_{CC}. In contrast, in the medium power average power tracking modulation mode, some embodiments of the V_{OFFSET} threshold circuit 41C may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to provide an indication of a weighted error voltage between the V_{RAMP} signal and the modulated power supply voltage, V_{CC}. The weighted error voltage signal includes an instantaneous error voltage component and an average error voltage component. Some embodiments of the V_{OFFSET} threshold circuit 41C may be further configured to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to provide a composite control signal to the switcher control circuit 880 that is substantially equivalent to the modulation mode feedback signal generated by the parallel amplifier 928" in the medium power average power tracking mode.

[001089] As another example, Figure 46E depicts an embodiment of the power management system 870E in which a parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is provided as the switch mode power supply feedback signal 40A in the high power modulation mode and the low power modulation mode. In addition, the V_{OFFSET} loop circuit 41C may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the high power modulation mode, the medium power modulation mode, and the medium power average power tracking modulation mode.

[001090] As a further example, Figure 46F depicts an embodiment of the power management system 870F in which a parallel amplifier 928' may generate the switch mode power supply feedback signal 40A in the high power modulation mode, the low power modulation mode, and the medium power average power tracking modulation mode. In addition, the V_{OFFSET} loop circuit 41C may generate

the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the high power modulation mode, the low power modulation mode, and the medium power average power tracking modulation mode. Because the open loop ripple compensation circuit 414 is disabled in the medium power average power tracking mode, the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, provided as the switch mode power supply feedback signal 40A only includes the modulation mode feedback signal generated by the parallel amplifier 928' in the medium power average power tracking modulation mode. Similar to the power management system 870C, in some embodiments, the power management system 870F may disable one of the parallel amplifier 928' and the V_{OFFSET} loop circuit 41C as a function of the average some average power tracking "bang-bang" mode of operation.

[001091] As another example, Figure 46G depicts an embodiment of the power management system 870G that is similar to the power management system 870F except the parallel amplifier 928" may generate the switch mode power supply feedback signal 40A in the high power modulation mode, the low power modulation mode, and the medium power average power tracking modulation mode.

[001092] As a further example, Figure 46H depicts an embodiment of the power management system 870H in which a parallel amplifier 928 may generate the switch mode power supply feedback signal 40A in the high power modulation mode and the low power modulation mode. The V_{OFFSET} loop circuit 41C may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the high power modulation mode, the medium power modulation mode, and the medium power average power tracking mode.

[001093] The operation of the switcher control circuit 880 in each operational state of a set of operational states may be dependent on the expected output power of the radio frequency power amplifier during a data transmission. Some embodiments of the switcher control circuit 880 may include firmware, logic circuits, discrete logic circuits, controllers, processors, comparators, delays elements, counters, analog logic circuitry, switches, multiplexers, transistor logic,

diode logic, registers, buffers, data buffers, level detectors, programmable logic circuits, and/or combinations thereof to implement and govern the operation of one or more state machines. The one or more state machines may be configured to govern the transitions between the various operational states of the switcher control circuit 880 as a function of the composite control signal, the power level modulation mode, and the expected output power generated by the radio frequency power amplifier 869 or the radio frequency power amplifier 869' during a data transmission. Based on the operational state of the switcher control circuit 880, the switcher control circuit 880 may generate the charge pump mode control signal 60, the series switch control signal 66, the shunt switch control signal 68, and the segmentation control signal 880A.

[001094] The switcher control circuit 880 may provide a charge pump mode control signal 60 to the multi-level charge pump 882 to configure the operation of the multi-level charge pump 882. In response to the charge pump mode control signal 60, the multi-level charge pump 882 may generate a boost output voltage or a buck output voltage at the charge pump output 64. The switcher control circuit 880 may generate the charge pump mode control signal 60 as a function of the power level modulation mode. In some embodiments, the switcher control circuit 880 may generate the charge pump mode control signal 60 as a function of both the powel level modulation mode and the expected output power to be generated by the radio frequency power amplifiers 869 and 869' during a data transmission.

[001095] The switcher control circuit 880 may also provide a series switch control signal 66 and a shunt switch control signal 68 to the switching circuit 884. In response to an assertion of the series switch control signal 66, the switching circuit 884 couples the switching voltage output 26 to the battery voltage, V_{BAT}, to generate the switching voltage, V_{SW}, substantially equal to V_{BAT}. In reponse to the shunt switch control signal 68, the switching circuit 884 couples the switching voltage output 26 to ground to provide generate the switching voltage, V_{SW}, substantially equal to zero volt. In addition, the switcher control circuit 880 provides a segmentation control signal 880A to the switching circuit 884 as a

function of the power level modulation mode. In some embodiments, the switcher control circuit 880 may generate the segmentation control signal 880A as a function of the power level modulation mode and the expected output power to be generated by the radio frequency power amplifiers 869 and 869' during a data transmission. For example, some embodiments of the power management systems 870 and 870A may be configured to generate the segmentation control signal 880A based on an average expected output power, P_{OUT_AVE}, the radio frequency power amplifier that maximizes the efficiency of the switch mode power supply converter 872.

[001096] The switcher control circuit 880 may configured to switch mode power supply converter 872 to generate a switching voltage, V_{SW}, at the switching voltage output 26 based on an operational state of the switcher control circuit 880 as a function of a power level modulation mode, which is dependent on the expected output power to be generated by the radio frequency power amplifiers 869 and 869' during a data transmission. In some embodiments, the switcher control circuit 880 may configure the multi-level charge pump 882 and the switching circuit 884 to operate in one of a buck converter "bang-bang" mode, a multi-level charge pump buck converter mode, and an average power tracking mode of operation as a function of the power level modulation mode and operational mode of the switcher control circuit 880.

[001097] Although not depicted in Figure 40B, some embodiments of the switch mode power supply converter 872 may include an embodiment of the programmable delay circuitry 432, depicted in Figure 24, which may be used to generate the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$. The delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, may be used by those embodiments of the parallel amplifier circuit 874 that include various embodiments of an active noise cancellation circuit. As an example, the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, may be used by an embodiment of the open loop ripple compensation assist circuit 414 to generate high frequency ripple compensation current 416, I_{COR}. Alternatively, in some embodiments, the delayed I_{COR}

estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, may be used in the place of the generate a delayed estimated switching voltage output, 38D, $V_{SW_EST_DELAYED}$, to provide an estimate of the future value of the switching voltage, V_{SW}, to an embodiments of the parallel amplifier output impedance compensation circuits 37B-F, depicted in Figures 34A-E. As previously discussed, the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, and the delayed estimated switching voltage output, 38D, $V_{SW_EST_DELAYED}$, are each feed forward signal generated based on the operational state of the switcher control circuit 880, and each provides an early indication of what the switching voltage, V_{SW}, will become based on the operational state of the switcher control circuit 880.

[001098] In each case, switcher control circuit 880 or the controller 50 may adjust the programmable delay period of the embodiments of the programmable delay circuitry 432 maintain a temporally alignment between the early indication of what the switching voltage, V_{SW}, will become based on the operational state of the switcher control circuit 880 and the differential V_{RAMP} signal. For example, as previously discussed, the difference between the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, and the magnitude of the V_{RAMP} signal used to generate the high frequency ripple compensation current 416, I_{COR}, reflects a predicted or future voltage across the power inductor 16 that corresponds to the parallel amplifier output current, I_{PARA_AMP}, to be generated by the parallel amplifier 928 in response to the V_{RAMP} signal. Referring to Figure 24, the magnitude of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, may be adjusted by the scaling factor, M, to compensated for changes in the battery voltage, V_{BAT}, and the magnitude of the V_{RAMP} signal used to generate the corresponding the parallel amplifier output current, I_{PARA_AMP}.

[001099] Referring to Figure 40C and 46B, in some embodiments, the control signal 926 received at the non-inverting input of the parallel amplifier 928 to generate the parallel amplifier output current, I_{PARA_AMP}, may be generated by the differential filter 924 as a function of the power level modulation mode. For example, in the high power modulation mode, the differential filter 924 may

provide an increased level of frequency compensation or correction as compared to the frequency compensation or correction provided by the differential filter 924 in the medium power modulation mode. Accordingly, some embodiments of the switcher control circuit 880, the switch mode power supply converter 872, the parallel amplifier circuits 874 and 874', and/or a combination thereof, may be further adapted to adjust the scaling factor, M, provided to the buffer scalar 434 and/or the magnitude of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, as a function of the power level modulation mode.

[001100] Some alternative embodiments of the switcher control circuit 880, the switch mode power supply converter 872, the parallel amplifier circuits 874 and 874', and/or combinations thereof, may be further configured to adjust the magnitude of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, based on the magnitude of the control signal 926 that is received by at the non-inverting input of the parallel amplifier 928, which is generated by the differential filter 924. In some embodiments, the switcher control circuit 880 may selectively adjust the scaling factor, M, as a function of the magnitude of the differential V_{RAMP} signal and the power level modulation mode. For example, in some embodiments of the switcher control circuit 880, the scaling factor, M, may be further adjusted as a function of the power level modulation mode to reflect the amount of frequency compensation or correction applied by the differential filter 924 to generate the control signal 926 received at the non-inverting input 928A of the parallel amplifier 928, depicted in Figures 40C and 46B.

[001101] In some embodiments of the power management system 870 and 870A, either the switch mode power supply converter 872 or the parallel amplifier circuit 874 may be further adapted to adjust the scaling factor, M, based on the magnitude of the control signal 926 or the power level modulation mode. For example, in some embodiments, the magnitude of the delayed I_{COR} estimated switching voltage output 38C, $V_{SW_EST_DELAY_ICOR}$, used by the open loop ripple compensation assist circuit 414 may be adjusted as a function of the power level

modulation mode, the magnitude of the differential V_{RAMP} signal, and the expected frequency response of the parallel amplifier 928 when operating in each of the respective power level modulation modes.

[001102] For example, some embodiments of the switch mode power supply converter 872 may include one of the embodiments of the programmable delay circuitry 432A, depicted in Figures 28A-B, the programmable delay circuitry 432B, depicted in Figures 29A-B, or the programmable delay circuitry 432C, 432C', and 432C", depicted in Figures 30A-C. As previously described with respect to the programmable delay circuitry 432, depicted in Figure 24, the switch mode power supply converter 872 may be configured to generate the delayed I_{COR} estimated switching voltage output 38C based on the operational state of the switcher control circuit 880. In addition, the controller 50 may be configured to adjust the programmable delay period as a function of the power level modulation mode, the segmentation mode of the switching circuit 884, and or a combination thereof.

[001103] For example, the switcher propagation delay is a time period between when the state of the switcher control circuit 880 changes to a new operational state and the switching voltage, V_{SW}, generated in response to the new operational state of the switcher control circuit 880 is generated at the switching voltage output 26. In some embodiments of the switch mode power supply converter 872, the switcher propagation delay may vary based on being configured to operate in the envelope tracking mode of operation and the average power tracking mode. Thus, the controller 50 may be configured to adjust the programmable delay period as a function of an expected output power to be generated by the radio frequency power. Alternatively, the switcher control circuit 880 may be configured to adjust the programmable delay period of the programmable delay circuitry 432 as a function of the power level modulation mode.

[001104] As another example, in some embodiments, the switching circuit 884 may be a segmented switching circuit having a number of sets of series switch and shunt switch pairs. The sets of series switch and shunt switch pairs may be

arranged in parallel and operably coupled to form a segmented series switch and shunt switch network. The switcher control circuit 880 may generate the series switch control signal 66, the shunt switch control signal 68, and the segmentation control signal 880A based on an operational state of the switcher control circuit 880 to control the operation of the switching circuit 884. In addition, the segmentation control signal 880A may be dependent on the power level modulation mode of the power management systems 870 and 870A. For example, the switcher control circuit 880 may configure the segmentation control signal 880A to enable or disable various combinations of the sets of series switch and shunt switch pairs of the switching circuit 884 based on the power level modulation mode of operation of the respective power management system 870, depicted in Figure 40A-C, and the power management system 870A, depicted in Figure 46A-B. As an example, in some embodiments of the medium power modulation mode, the switcher control circuit 880 may generate a segmentation control signal 880A to enable either 75% or 50% of the number of sets of series switch and shunt switch pairs of the switching circuit 884.

[001105] In some embodiments of the switching circuit 884, the switcher propagation delay the switcher propagation delay may vary depending on the number of sets of series switch and shunt switch pairs are configured to operate during a data transmission. In some embodiments, the switcher control circuit 880 may be configured to adjust the programmable delay period of the programmable delay circuitry 432 depending on the segmentation control signal 880A to maintain the temporal alignment of the delayed I_{COR} estimated switching voltage output 38C with respect to the switching voltage, V_{SW}, provided at the switching voltage output 26.

[001106] The switching circuit 884 may include a segmentation control circuit 886 configured to receive a segmentation control signal 880A from the switcher control circuit 880. The switching circuit 884 may further include segmented series switches 888 and segmented shunt switches 890 in communication with the segmentation control circuit 886. The segmented series switches 888 may include a first series switch 892, a second series switch 894, a

third series switch 896, and the fourth series switch 898. The segmented shunt switches 890 may include a first shunt switch 900, a second shunt switch 902, a third shunt switch 904, and a fourth shunt switch 906.

[001107] A source 892S of the first series switch 892, a source 894S of the second series switch 894, a source 896S of the third series switch 896, and a source 898S of the fourth series switch 898 are in communication with a supply voltage received from the battery 20 substantially equal to the battery voltage, V_{BAT}. A drain 892D of the first series switch 892, a drain 894D of the second series switch 894, a drain 896D of the third series switch 896, and a drain 898D of the fourth series switch 898 are respectively coupled to a drain 900D of the first shunt switch 900, a drain 902D of the second shunt switch 902, a drain 904D of the third shunt switch 904, and a drain 906D of the fourth shunt switch 906 to form the switching voltage output 26. A source 900S of the first shunt switch 900, a source 902S of the second shunt switch 902, a source 904S of the third shunt switch 904, and the source 906S of the fourth shunt switch 906 are in communication with a reference voltage substantially equal to ground.

[001108] The segmentation control circuit 886 may include a first series switch control output 908 coupled to the gate 892G of the first series switch 892, a first shunt switch control output 910 coupled to the gate 900G of the first shunt switch 900, a second series switch control output 912 couple to the gate 894G of the second series switch 894, a second shunt switch control output 914 coupled to the gate 902G of the second shunt switch 902, a third series switch control output 916 coupled to the gate 896G of the third series switch 896, a third shot control output 918 coupled to the gate 904G of the third shunt switch 904, a fourth series switch control output 920 couple to the gate 898G of the fourth series switch 898, and a fourth shunt switch control output 992 coupled to the gate 906G of the fourth shunt switch 906.

[001109] Operationally, the segmentation control circuit 886 may divide the segmented series switches 888 and segmented shunt switches 890 into logical groupings of sets of series and shunt switches such that each set of series and shunt switches includes one of the segmented series switches 888 and one of

the segmented shunt switches 890. For example, a first set of series and shunt switches may include a first series switch 892 and the first shunt switch 900. A second set of series and shunt switches may include the second series switch 894 and the second shunt switch 902. A third set of series and shunt switches may include the third series switch 896 and the third shunt switch 904. The forth set of series and shunt switches may include the fourth series switch 898 and the fourth shunt switch 906.

[001110] The segmentation control circuit 886 is configured to receive a series switch control signal 66 and a shunt switch control signal 68 from the switcher control circuit 880. The power management system 870 may configure the switcher control circuit 880 to generate a segmentation control signal 880A to select which of the segmented series switches 888 and segmented shunt switches 890 are to be enabled by the segmentation control circuit 886 to generate the switching voltage, V_{SW}, at the switching voltage output 26 as a function of the average expected output power, P_{OUT_AVE}, to be generated by the radio frequency power amplifier 869 during the data transmission. Illustratively, in the case where there are four sets of series and shunt switches, the operation of the segmentation control circuit 886 may be divided into four regions or modes of operation.

[001111] In some embodiments, the switcher control circuit 880 may determine generate the segmentation control signal 800A as a function of the average expected output power, P_{OUT_AVE}, and a set of switcher output power thresholds including a first switcher output power threshold, P_{OUT1}, a second switcher output power threshold, P_{OUT2}, and a third switcher output power threshold, P_{OUT3}. The values of the first switcher output power threshold, P_{OUT1}, the second switcher output power threshold, P_{OUT2}, and the third switcher output power threshold, P_{OUT3}, may be determined to maximize the efficiency of the switch mode power supply converter 872 with respect to the expected output power of the radio frequency power amplifier as a function of the power level modulation mode and the expected load line, $R_{RF_AMP_EXP}$, of the radio frequency power amplifier 869 or 869' during the data transmission.

[001112] In the case where the average expected output power, P_{OUT_AVE}, of the radio frequency power amplifier is at least equal to the first switcher output power threshold, P_{OUT1}, the segmentation control signal 880A may configure the segmentation control circuit 886 to enable all four of the series switch and shunt switch segments. In the case where the average expected output power, P_{OUT_AVE}, of the radio frequency power amplifier is less than the first switcher output power threshold, P_{OUT1}, and at least equal to the second switcher output power threshold, P_{OUT2}, the segmentation control signal 880A may configure the segmentation control circuit 886 to enable three of the series switch and shunt switch segments. In the case where the average expected output power, P_{OUT_AVE}, of the radio frequency power amplifier is less than the second switcher output power threshold, P_{OUT2}, and at least equal to the third switcher output power threshold, P_{OUT3}, the segmentation control signal 880A may configure the segmentation control circuit 886 to enable two of the series switch and shunt switch segments. And in the case where the average expected output power, P_{OUT_AVE}, of the radio frequency power amplifier is less than the third switcher output power threshold, P_{OUT3}, the segmentation control signal 880A may configure the segmentation control circuit 886 to enable one of the series switch and shunt switch segments.

[001113] Some embodiments of the multi-level charge pump 882 may be similar to the embodiments of the multi-level charge pump circuit 56 and 256A-D, depicted in Figures 7A-D, as previously described. The multi-level charge pump 882 may include a number of switches and only a first flying capacitor and a second flying capacitor switchably coupled to form a multi-level charge pump switching network. The multi-level charge pump 882 may configure the multi-level charge pump switching network to generate a variety of "boost" output voltages and "buck" output voltage as a function of a charge pump mode control signal 60 received from the switcher control circuit 880. Some embodiments of the multi-level charge pump 882 may generate a variety of "boost" output voltages and "buck" output voltage as a multi-level charge pump output voltage, V_{MLCP}, in response to the charge pump mode control input 60 generated by the

switcher control circuit 52. The multi-level charge pump 882 may provide the multi-level charge pump output voltage, V_{MLCP}, to the charge pump output 64. , which may be coupled through the switching circuit 884 to the switching voltage output 26.

[001114] As previously describe with respect to the operation of the embodiments of the multi-level charge pump circuit 56 and the multi-level charge pump circuit 258A-C, depicted in Figures 7A-D, the switcher control circuit 880 may configure the multi-level charge pump 882 to generate a boost output voltage or a buck output voltage, which is provided to the switching voltage output 26 as the switching voltage, $V_{SW,}$ depending on the state of operation of the switcher control circuit 880. The multi-level charge pump 882 may generate a number of "boost" output voltages, "buck" output voltages, and/or a combination thereof as a multi-level charge pump output voltage, V_{MLCP}. The multi-level charge pump 882 may provide the multi-level charge pump output voltage, V_{MLCP}, to the charge pump output 64. In some embodiments, the charge pump output 64 may be coupled through the switching circuit 884 to the switching voltage output 26. In some alternative embodiments, the charge pump output 64 may be coupled to the switching voltage output 26. In still other embodiments, the charge pump output 64 may be switchably coupled to the switching voltage output 26. In some embodiments, the segment series switches and segmented shunt switches of the switching circuit 884 in combination with switching network of the multi-level charge pump 882 may be referred to as a combined switching network of the switch mode power supply converter 872.

[001115] As an example, and not by way of limitation, similar to the multi-level charge pump circuit 56 depicted in Figure 7A, the multi-level charge pump 882 may generate a number of "boost" output voltages and "buck" output voltage" in response to charge pump mode control signal 60 generated by the switcher control circuit 880.

[001116] For example, in a second boost mode of operation, the multi-level charage pump 882 may configure the sw switching network to generate a second boost mode output voltage, V_{SECOND_BOOST}, substantially equal to 2 x V_{BAT} at the

charge pump output 64. In a first boost mode of operation, the multi-level charge pump 882 may configure the switching network to generate a first boost mode output voltage at the charge pump output 64 substantially equal to 3/2 x V_{BAT}. In a first buck mode of operation, the multi-level charge pump 882 may configure the switching network to generate a first buck mode output voltage at the charge pump output 64 substantially equal to 1/2 x V_{BAT}. In some alternative embodiments, the multi-level charge pump 882 may be configured to generate other ratios of boost mode output voltages and buck mode output voltage.

[001117] Similar to the µC charge pump circuit 262 and the multi-level charge pump circuit 56, described above, some embodiments of the multi-level charge pump 882 may only include two flying capacitors that are switchably coupled in various arrangements with respect to each other, the battery voltage, V_{BAT}, and the charge pump output 64 to generate the various charge pump output voltages at the charge pump output 64. For example, similar to the µC charge pump circuit 262, some embodiments of the multi-level charge pump 882 may generate various ratios of output voltages that may be provided as a boost output voltage or a buck output voltage to the switching voltage output 26 as the switching voltage, V_{SW}. In still other alternative embodiments, the multi-level charge pump 882 may generate a boost output voltage or a buck output voltage with respect to a supply voltage other than the battery voltage, V_{BAT}, where the supply voltage may be greater than the battery voltage, V_{BAT}, or less than the battery voltage, V_{BAT}. In some alternative embodiments, the supply voltage provided to the multi-level charge pump 882 may be a boosted voltage or a bucked voltage derived from the battery voltage, V_{BAT}.

[001118] Based on the power level modulation mode, in some embodiments of the multi-level charge pump buck converter mode of operation, the switcher control circuit 880 may configure the switch mode power supply converter 872 to generate a series output voltage substantially equal to the battery voltage, V_{BAT}, a shunt output voltage substantially equal to a ground voltage, and a subset of the available charge pump output voltages. As an example, as a function of the power level modulation mode, the switcher control circuit 880 may configure the

multi-level charge pump 882 and the switching circuit 884 to generate a shunt mode output voltage substantially equal to a ground voltage, in the shunt output mode, a series mode output voltage substantially equal to V_{BAT}, in the series output mode, and a first boost mode output voltage substantially equal to 3/2 x V_{BAT} in the first boost output mode. As another non-limiting example, as a function of the power level modulation mode, in some power level modulation modes, the switcher control circuit 880 may configure the multi-level charge pump 882 to provide a first buck mode output voltage substantially equal to 1/2 x V_{BAT} in the first buck mode of operation. As an example, as a function of the power level modulation mode, the switcher control circuit 880 may configure the multi-level charge pump 882 and the switching circuit 884 to generate a shunt mode output voltage substantially equal to ground, a first buck mode output voltage substantially equal to 1/2 x V_{BAT}, a series mode output voltage substantially equal to V_{BAT}, and a first boost mode output voltage substantially equal to 3/2 x V_{BAT} as a function of the operational state of the switcher control circuit 880. As still another non-limiting example, in some power level modulation modes, the switcher control circuit 880 may configure the multi-level charge pump 882 to only operate in a first boost mode of operation to generate a first boot output voltage, V_{FIRST_BOOST}, substantially equal to 3/2 x V_{BAT}.

[001119] As another example, in some power level modulation modes, the multi-level charge pump 882 may be configured to only operate in the second boost mode of operation. In still another example, in some power level modulation modes, the multi-level charge pump 882 may be configured to operate in the first buck mode and either the first boost mode or the second boost mode of operation. For example, in some power level modulation modes, the switcher control circuit 880 may configure the multi-level charge pump 882 to provide either a first buck mode output voltage substantially equal to 1/2 x V_{BAT} and a first boost mode output voltage substantially equal to 3/2 x V_{BAT} as a function of the operational state of the switcher control circuit 880. In other power level modulation modes, the switcher control circuit may configure the multi-level charge pump 882 to provide a buck output voltage substantially equal to 1/2 x

V_{BAT} in the first buck mode and a second boost level output voltage substantially equal to 2 x V_{BAT} as a function of the operational state of the switcher control circuit 880.

[001120] In some embodiments, the first buck level threshold may be substantially the same as the first output level threshold, discussed relative to the switcher control circuit depicted in Figure 3A. For example, in some embodiments, the first buck level threshold may be associated with a first buck output mode. In some embodiments, the multi-level charge pump 882 may generate a first buck mode output voltage substantially equal to 1/2 x V_{BAT}, when the switcher control circuit 880 is a first buck mode of operation. Alternatively, some embodiments of the multi-level charge pump 882 may generate a first buck mode output voltage substantially equal to m/n x V_{BAT}, as a function of the power level modulation mode, where m/n is less than one.

[001121] As another example, some embodiments of the switcher control circuit 880 may be similar to the switcher control circuit 52S depicted in Figure 4S, which will be described with continuing reference to Figures 40A-C and 46B. Some embodiment so the switcher control circuit 52S may be similar to the previously described embodiments of switcher control circuits 52, 52A-D, 52I-L, and 52R, depicted at least in Figures 2A, 2B, 3A-D, 3I-L, 3R, 4A-D, 4I-L, 4R, 5A-D, 5I-L, 5R, 6A-D, 6L, and 6R.

[001122] The switcher control circuit 52S may be in communication with the controller 50 via the control bus 44. Similar to the previously described embodiments of switcher control circuits 52, 52A-D, 52I-L, and 52R, the threshold detector and control circuit 132S may include a first comparator 140, a second comparator 142, a third comparator 144, and a fourth comparator 146 configured to receive the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130, respectively. In addition, the threshold detector and control circuit 132 may further include a fifth comparator 141 configured to receive a first buck level threshold 125. The first buck level threshold 125 may govern the generation of a first buck level voltage as the switching voltage, V_{SW}.

[001123] Accordingly, the switcher control circuit 52S may include the first comparator 140, the fifth comparator 141, the second comparator 142, the third comparator 144, and the fourth comparator 146 configured to generate a shunt level indication 150S, a first buck output level indication 151S, a series level indication 152S, a first boost output level indication 154S, and a second boost output level indication 156S based on the difference between the composite control signal and each of the shunt level threshold 124, the first buck level threshold 125, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 signals, respectively.

[001124] As previously discussed with respect to the switcher control circuit 880, some embodiments of the switcher control circuit 52S may form the composite control signal as a function of the feedback delay compensation signal 854, $I_{FEEDBACK\ TC}$, the switch mode power supply feedback signal 40A, and the threshold offset current 42, $I_{THRESHOLD\ OFFSET,}$ and/or some combination thereof, as depicted in Figure 3A-B, 3I-J, 4A-B, 4I-L, and 4R, where the parallel amplifier circuit output current estimate 40, $I_{PAWA\ OUT\ EST}$, is replace by the switch mode power supply feedback signal 40A.

[001125] Referring to Figures 3A-B, 3I-J, 4B, and 4J, some embodiments of the switcher control circuit 52S may include a frequency locked loop circuit similar to either the frequency locked loop circuit 54A or the frequency locked loop circuit 54B configured to regulate the switching frequency of the switch mode power supply converter 872.

[001126] As a not limiting example, some embodiments of the switcher control circuit 880 may include an embodiment of the frequency locked loop circuit 54B that is further configured to adjust the magnitude of each of the shunt level threshold 124, the first buck level threshold 125, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 to modify or control the switching frequency of the switch mode power supply converrter 872. In some alternative embodiments, the switcher control circuit 880 may include an embodiment of the frequency locked loop circuit 54B that controls the switching frequency by adjusting only some of a set of

comparator thresholds. An example set of comparator thresholds may include the shunt level threshold 124, the first buck level threshold 125, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130. Another example set of comparator thresholds may include only the shunt level threshold 124, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130.

[001127] In some embodiments, the set of comparator thresholds available to govern the switching frequency of the switch mode power supply converter 876 may be dependent on a power level mode of operation or whether the multi-level charge pump 884 is configured to operate in one of the many embodiments of a first boost output modes and/or one of the many embodiments of a second boost output mode. For example, in some embodiments of the power level modulations modes, the switcher control cirucuit 880 may restrict the operation of the multi-level charge pump 884 to generate only a first boost mode. In other embodiments of the power level modulation modes, switcher control cirucuit 880 may restrict the operation of the multi-level charge pump 884 to generate neither a first buck output mode nor a first output mode. As another example, in some alternative embodiments, the frequency locked loop circuit 54B may only adjust the magnitude of a subset of comparator thresholds to control the switching frequency of the switch mode power supply converter 872.

[001128] In some embodiments, the switcher control circuit 880 may adjust only the shunt level threshold 124 and the series level threshold 126 to operate at a target switching frequency because the first boost level threshold 128 and the second boost level threshold 130 may be set substantially higher than the series level threshold 126 and/or the shunt level threshold 124. As a result, the embodiments that adust only the shunt level threshold 124 and the series level threshold 126 may provide more predictivable frequency tracking with less complexity. In still other embodiments, the switcher control circuit 880 may adjust only the shunt level threshold 124 to operate with a switching frequency substantially equal to a target switching frequency governed by the frequency locked loop circuit 54B. Advantagesously, the embodiments that adjust only the

shunt level threshold 124 may provide improved or more predictive frequency tracking. For example, in some embodiments, the switcher control circuit 880 may always use the shunt level threshold 124 to govern generation of the switching voltage, V_{SW}. In other words, the switcher control circuit 880 may be configured to use the shunt level threshold as a common threshold level that is used in each mode of operation of the switch mode power supply converter 872. Some embodiments of the switch mode power supply converter 872 may be further configured to operate in a free running switching frequency mode. In the free running switching frequency mode, the switcher control circuit 880 operates at a switching frequency as a function of a set of comparator thresholds and an output power level delivered from the switch mode power supply converter 872 to the modulated power supply output 876. For example, the power level delivered from the switch mode power supply converter 872 to the modulated power supply output 876 may be a function of the expected output power to be generated by the respective radio frequency power amplifiers 869 and 869' during a data transmission. In the free running switching frequency mode, the switching frequency of the switch mode power supply converter 872 be a function of the power level mode of operation. In the free running switching frequency mode, a controller 50 may adjust the magnitudes of one or more of the set of comparator thresholds used by the switcher control circuit 880 in a particular mode of operation to regulate the switching frequency of the switch mode power supply converter 872. As an example, in some embodiments, only a subset of the set of comparator thresholds associated with the switcher control cicuit 880 may be adjusted or controlled to set a desired switching frequency. For example, depending on a band of operation assigned to the communication device, some embodiments of the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A may adjust one or more of the set of comparator thresholds stored in the programmable threshold circuit 122, as depicted in Figures 3A-3R and Figure 59, to adjust the switching frequency of the switch mode power supply converter. For example, in some embodiments, the only the shunt level

threshold parameter may be adjusted to control the switching frequency of the switch mode power supply converter 872. In some embodiments, the set of comparator threshold may be adjusted to ensure harmonics of the swiching frequency of the switch mode power supply converter 872 are located outside of a particular frequency spectrum.

[001129] Depending on a power level modulation mode, a characterist of the data transmission, and/or a desired distribution of harmonics of the switching frequency within the frequency spectrum, the controller 50 may configure the comparators thresholds to set the equivalent main ripple voltage level at the modulated power supply output 876 and/or the switching frequency of the switch mode power supply converter 872. For example, in the medium power average power tracking modulation mode

[001130] Similarly, some embodiments of the average frequency control circuit 885 may be configured to adjust the magnitude of one or more of the shunt level threshold 124, the first buck level threshold 125, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 to modify or control the switching frequency of the switch mode power supply converrter 872. As an example, in some embodiments, the average frequency control circuit 885 may adjust the magnitude of each of the shunt level threshold 124, the first buck level threshold 125, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 based on a target switching frequency. The target frequency may be set to move the switching frequency of the switch mode power supply converter 872 away from a band of frequencies to reduce the generation of noise in a data transmission signal, where the noise is associated with generation of the switching voltage, V_{SW}, at the switching frequency.

[001131] Alternatively, in some embodiments, the average frequency control circuit 885 may only adjust the magnitude of the shunt level threshold 124 to configure the switch mode power supply converter 872 to operate at a switching frequency substantially equal to the target frequency. As an example, the average frequency control circuit 885 may increase the magnitude of the shunt

level threshold 124 to decrease the switching frequency of the switch mode power supply converter 872. The average frequency control circuit 885 may decrease the magnitude of the shunt level threshold 124 to increase the switching frequency of the switch mode power supply converter 872. The average frequency control circuit 885 may be enabled in the high power modulation mode, the medium power modulation mode, and the medium power average power tracking mode. The average frequency control circuit 885 may be disabled in the low power modulation mode and the low power average power tracking mode. However, in some alternative embodiments of the power management systems 870, 870A-C and 870E-H, depicted in Figures 40A-E and Figures 46A-B and 46E-H, the average frequency control cirdcuit 885 may be enabled to set the average frequency of the switch mode power supply converter to a target frequency.

[001132] As depicted in Figure 59, some embodiment so the switcher control circuit 52S may include an embodiment of a programmable threshold circuit 122A configured to store one or more sets of comparator threshold levels. The controller 50 may configure the programmable threshold circuit 122A to store one or more sets of threshold levels, where each of the sets of threshold levels may include the shunt level threshold parameter, the first buck level threshold parameter, the series level threshold parameter, the first boost level threshold parameter, and the second boost level threshold parameter.

[001133] Returning to Figure 4S with continuing reference to Figure 59, each set of programmable threshold levels may correspond to a desired or target switching frequency for an associated band of operation. For example, in some embodiments of the programmable threshold circuit 122A, a first set of programmable threshold levels may corresponds to generating a switching voltage, V_{SW}, at the switching voltage output 26 as a function of a first average switching frequency, where the first average switching frequency is a target switching frequency for a particular band of operation in a communication network. For example, the controller 50 may configure the programmable threshold circuit 122A to use the first set of programmable threshold level to

move a switching frequency into a desired range of frequencies while the communication device is configured to transmit data in a first band of operation.

[001134] In doing so, the controller 50 may distribute the harmonic frequencies of the switching frequency in the frequency spectrum away from a band of operation that has a challenging or tight tolerance level regarding spurious emissions. As a non-limiting example, a communication network may configure a communication device to operate in the LTE band 13, which is close to a band of frequencies associated with the public safety band. The controller 50 may configure the programmable threshold circuit 122A to use the first set of programmable threshold levels in order to move the switching frequency either outside of the public safety band to meet the present -50dBm/1MHz spurious emission requirement, which is substantially higher than the -60dBm/6.7MHz requirements for spurious emission for other LTE bands, where each LTE band is a non-limiting example of a band of operation in which the communication devive may operate in a communication network.

[001135] In some alternative embodiments, the controller 50 may program the threshold levels stored in the programmable threshold circuit 122A for each band of operation that has a tight tolerance level for spurious signals. In other embodiments, the programmable threshold circuit 122A may include registers, a look up table, or other memory to store a number of sets of programmable threshold levels to configure the communication device to operate in a particular mode of operation, band of operation, or mode of communication. For example, in some embodiments, the communication device may transmit information or data as a function of resource blocks. Each band of operation may have an assigned number of resource blocks that the communication device may use to transmit information or data to base station or communication hub within a communication network. As a non-limiting example, some embodiments of a communication network may include subcarriers that have a constant spacing. As an example, in some communication networks, a particular frequency band or band of frequency spectrum may include sub-bands, where each sub-band has a subcarrier. The resource block may include a number of subcarriers that are

grouped together to provide a portion of the frequency spectrum to the communication device. In some embodiments of a LTE communication system, one resource block may include 12 subcarriers. Each resource block may have a resource block size. In some embodiments, the resource block size may be the same for all bandwidths. However, different LTE bandwidths may have a different number of resource blocks. Depending on the location of the resource blocks relative to other bands of operation and the number of resource blocks allocated, the controller 50 may configured the programmable threshold circuit 122A to use a particular set of threshold levels stored in the programmable threshold circuit 122A to move the harmonic frequencies associated with the switching frequency of the switch mode power supply converter 872 to a desired location in the frequency spectrum.

[001136] If for example we have an LTE signal using one resource block located at the bottom edge of the LTE band13, any ripple voltage at the modulated power supply output 876 may appear on both sidebands of the amplified modulated radio frequency signal generated by the radio frequency power amplifier 869' when only one resource block is allocated for the transmission. As a result, some harmonic frequencies associated with the switching frequency of the switch mode power supply converter 872 may fall into the public safety band when the average frequency of the ripple frequency offset is between 2MHz and 14MHz

[001137] To avoid this problem, the switcher control circuit 52S may adjust the average frequency of the modulated ripple noise of the switch mode power supply converter 872 to move the modulated ripple noise to higher frequency offset that is outside of the public safety band. Although the increase in switching frequency may slightly degrade the efficiency of the switch mode power supply converter 872, moving to a higher average switching frequency may ensure that the modulated ripple noise is located outside the public safety band. As a result, the modulate power system 870 and 870 may avoid the need to meet the more stringent spurious signal requirement of -60dBm/6.25KHz associated with the public safety band.

[001138] In some modes of operation, either the controller 50 or the switcher control circuit 52S may either increase or decrease the average switching frequency of the switch mode power supply converter 872 to move the ripple frequency energy into specific frequency location that is away from the public safety band. For example, the controller 52S may configure the switching frequency of the switch mode power supply converter 872 in either the average power tracking mode of operation, the envelope tracking mode of operation, or the buck mode of operation to reduce the level of harmonic switching frequencies that may fall inside a band of operation that is sensitive to spurious noise. The radio frequency power amplifier 869 or 869' may generate the harmonic switching frequencies as a function of the amplification of the modulated radio frequency input signal and ripple voltages present at the modulated power supply output 876. The ripple voltage may be due in part to the high frequency ripple current generated by the switching action of the switch mode power supply converter 872, the non-ideal impedance of the parallel amplifier 928, and/or a combination thereof. By controlling the location of the switching frequency in the frequency spectrum, the various embodiments of the power management systems 870, 870A-C and 870E-H, depicted in Figures 40A-E and Figures 46A-B and 46E-H, may reduce the maximum energy level or power level of the harmonic switching frequencies generated within a receive channel or transmit channel of another band of operation.

[001139] As an example, depending on the power level modulation mode, the power management systems 870, 870A-C, and 870E-H may use either an open loop or a closed control loop to govern the switching frequency of the switch mode power supply converter 872.

[001140] In the high power modulation mode and the medium power modulation mode, various embodiments of the power management systems 870, 870A-C, and 870E-H may enable the average frequency control circuit 885 to govern the switching frequency of the switch mode power supply converter 872 based on a target switching frequency. In some embodiments, the average frequency control circuit 885 may be configured to govern the switching frequency of the

switch mode power supply converter 872 to generate a switching frequency such that the average of the switching frequency is substantially near or equal to the target switching frequency. As a result, the controller 50 may configure the average frequency control circuit 885 to move the switching frequency of the switch mode power supply converter 872 to a location such that some of the energy associated with the harmonic frequencies of the switching frequency may be moved out of or away from a sensitive band of operation and/or the maximum energy level or power level at the harmonic switching frequencies within the sensitive band of operation may be reduced.

[001141] As discussed in detail below, Figures 59-60 depict an embodiment of a switch mode power supply switching frequency control system 3000 that includes an embodiment of the average frequency control circuit 885, depicted as the average frequency control circuit 3002. The average frequency control circuit 3002 may be configured to generate an adjusted shunt level threshold 3032 based on the shunt level threshold parameter stored in an embodiment of the programmable threshold circuit 122A of the switcher control circuit 52S, a pre-determined counter value 3006 provided as a counter preload to the counter 3016, and a counter clock that is derived from a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$. The pre-determined counter value 3006 may correspond to a target switching frequency, and a counter clock 3022 derived from a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$.

[001142] The logic level indication of the switching voltage output, $V_{SW_EST_OUT}$ may effectively provide an indication of the switching frequency of the switch mode power supply converter 872. Depending on the overflow indicator 3009 of the counter 3016, the accumulator 3018 may either increase or decrease the value of the shunt level threshold parameter to provide an adjusted shunt level threshold 3032. In some embodiments, the average frequency control circuit 3002 may include a toggle circuit 3040. In some embodiments, the toggle circuit 3040 may be configured to toggle the magnitude of the adjusted shunt level threshold 3032 with a toggle signal 3044 generated based on a programmable toggle value. In other embodiments, the toggle circuit 3040 may be configured to

toggle the magnitude of the adjusted shunt level threshold 3032 by one-half of a least significant bit of the adjusted shunt level threshold 3032. For example, in some embodiments, the toggle circuit 3040 may toggle the magnitude of the adjusted shunt level threshold 3032 on every transmission slot boundary to obtain an average switching frequency near or at the target switching frequency set by the pre-determined counter value. In doing so, the average frequency control circuit 3002 may effectively provide an additional effective resolution or granularity substantially equal to one-half of the least significant bit of the shunt level threshold parameter. Toggling the magnitude of the shunt level threshold 124 may tend to spread the energy present in any spurious emissions across a band of frequencies, which may reduce the maximum peak energy level of the spurious emissions related to the switching frequency of the switch mode power supply converter as a function of how fast the switch mode power supply converter 872 changes the average switching frequency of the switch mode power supply converter 872. At the same time, toggling the magnitude of the shunt level threshold 124 may also have an effect similar to frequency hopping.

[001143] In addition, some embodiments of the average frequency control circuit 3002 may further include a dither circuit 3042 configured to provide a dither signal 3046 having a programmable dither magnitude. The dither signal 3046 may be applied to the sum of the adjusted shunt level threshold 3032 and the toggle signal 3044 during a data transmission. The dither circuit 3044 may generate different degrees or magnitudes of dithering. The higher the magnitude of the dither signal 3046, the greater the spreading of the energy in the harmonic switching frequencies. As an example, in some embodiments, the dither signal 3044 may have a substantially random or pseudo-random magnitude. In some embodiments, the dither signal 3044 may have a mean value substantially equal to zero. The dither signal 3044 may either increase or decrease the switching frequency of the switch mode power supply converter 872. In some embodiments, dither signal 3046 may be generated based on a pseudo-random binary sequence having an auto correlation function substantially equal to zero and a duty cycle. In some embodiments, the controller 50 may configure the

duty cycle of the pseudo-random binary sequence. In other embodiments, the duty cycle of the pseudo-random binary sequence may be fixed. When applied to the adjusted shunt level threshold 3032, the toggle signal 3044 and the dither signal 3046 generate an adjusted shunt level threshold parameter 3048 that may be selectively used by the switcher control circuit 52S to govern the generation of the switching frequency in a closed loop system while also spreading energy of the harmonics of the switching frequency to lower the magnitude of the peak energy in the harmonics of the switching frequency.

[001144] In addition, in some embodiments of the high power modulation mode and the medium power modulation mode, the controller 50 may configure the first corner frequency, f_{C1}, and the second corner frequency, f_{C2}, of the open loop ripple compensation assist circuit 414 to reduce the high frequency ripple current at the switching frequency of the switch mode power supply converter 872 as well as the energy or power level at the harmonic switching frequencies that may fall inside a band of operation that is sensitive to spurious noise. As another example, referring to Figures 27A-B, the controller 50 may selectively set the resistance value of the filter resistance, R_1 of the filter resistor 458, and the resistance value of the feedback resistance, R_2, of the feedback resistor 462, to change the frequency response of the open loop ripple compensation assist circuit 414B. Similarly, in some embodiments, the controller 50 may selectively set the capacitance value of the filter capacitance, C_1, of the filter capacitor 460 and the capacitance value of the feedback capacitance, C_2, of the feedback capacitor 464, to change the frequency response of the open loop ripple compensation assist circuit 414B. Thus, in the case where the switching frequency of the switch mode power supply converter 872 may be operating at a frequency that may generate harmonic frequency within a sensitive band of operation, the controller 50 may configured the high pass filter characteristics of the open loop ripple compensation assist circuit 414 to substantially reduce the magnitude of the high frequency ripple currents and corresponding high frequency ripple voltages at the switching frequency of the switch mode power supply converter 872. Because the magnitude of the high frequency ripple

currents and corresponding high frequency ripple voltages at the switching frequency of the switch mode power supply converter 872 are reduces, the magnitude of any spurious signals generated at harmonics of the switching frequency of the switch mode power supply converter 872 may also be reduced. In the medium power average power tracking mode, the average frequency control circuit 885 may be disabled to save power. In this case, the controller 50 may configured one or more of the set of threshold levels to move the switching frequency of the switch mode power supply converter 872 away from a sensitive band of operation.

[001145] The switcher control circuit 52S may also receive a mode switch control signal 131 and various control parameter via the control bus 44 from the controller 50. As an example, the controller 50 may configure the logic circuit 148S to operate the switch mode power supply converter 872 in one of a number of power level modulation modes. The controller 50 may configured the logic circuit 148S to use one of a plurality of state machines to govern the operational state of the switcher control circuit 52S as a function of the power level modulation mode. The power level modulation modes may be determined based on an expected output power to be generated by the radio frequency power amplifier 869 during a data transmission. In some embodiments, the power level modulation mode may be determined based on an average expected output power, P_{OUT_AVE}, to be generated by the radio frequency power amplifiers 869 and 869' during a data transmission. The logic circuit 148S may be further configured to generate the segmentation control signal 880A to control the segmentation of the switching circuit 884 as a function of a mode switch control signal 131 and the power level modulation mode provided by the controller 50. In addition, the logic circuit 148S may be configured to operate the switch mode power supply converter in various envelope tracking modes of operation and various average power tracking modes.

[001146] The mode switch control signal 131 may configure the threshold detector and logic circuit 148S to operate the switch mode power supply converter 872 in a number of pseudo-envelope tracking modes, buck converter

"bang-bang" modes, and/or average power tracking "bang-bang" modes of operation. For example, similar the previously described embodiment of the logic circuit 148 A, the logic circuit 148B, the logic circuit 148C, the logic circuit 148D, the logic circuit 148I, the logic circuit 148J, and the logic circuit 148R, the logic circuit 148S may be configured to generate a series switch control output 162 to drive the first output buffer 158 as a function of operational state of the switcher control circuit 52S, which generates the series switch control signal 66. The logic circuit 148S may be configured to generate a shunt switch control output 164 to drive the second output buffer 160 as a function of operational state of the switcher control circuit 52S, which generates the shunt switch control signal 68.

[001147] The logic circuit 148S may also configured to generate one or more switching voltage output cmos signal(s) 166, $V_{SW_EST_CMOS_SIGNAL}$(s), as a function of the operational state of the switcher control circuit 52S, which may be used by the third output buffer 161 to generate one of the various embodiments of the estimated switching voltage output 38B, V_{SW_EST}, and the combination of the programmable delay circuitry 432 and the buffer scalar 434, depicted in Figure 24, to generate the delayed I_{COR} estimated switching voltage output 38C.

[001148] The logic circuit 148S may also configured to generate the charge pump mode control signal 60 as a function of the operational state of the switcher control circuit 880. The logic circuit 148S may be further configured to generate a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$. In addition, the logic circuit 148S may be further configured to generate the segmentation control signal 880A to control the switching circuit 884, as previously described with respect to the switcher control circuit 880.

[001149] Some embodiments of the switcher control circuit 52S may operate the switch mode power supply converter 872 in one of a number of average power tracking modes of operation. In addition, in some average power tracking modes of operation, the switcher control circuit 52S may configure the multi-level charge pump 882 and switching circuit 884 to operate in various average power tracking "bang-bang" modes to generate the switching voltage, V_{SW}, at the switching voltage output 26.

[001150] In some embodiments of the many average power tracking "bang-bang" modes, the switcher control circuit 52S may operate in one of a number of average power tracking "buck-buck" modes or in one of a number of average power tracking "buck-boost" modes as a function of the battery voltage, V_{BAT}, the envelope characteristics of modulated radio frequency input signal to be transmitted, a maximum desired ripple voltage at the modulated power supply output 876, the overall efficiency of the switch mode power supply converter 872, a maximum target duty cycle, and/or some combination thereof.

[001151] In the average power tracking "buck-buck" mode, the switcher control circuit 52S may configure the multi-level charge pump 882 and the switching circuit 884 to generate a first bang-bang switching voltage, V_{SW_BB1}, and a second bang-bang switching voltage, V_{SW_BB2}, that are each no greater than the battery voltage, V_{BAT}. In the average power tracking "buck-boost" mode, the switcher control circuit 52S may configure the multi-level charge pump 882 and the switching circuit 884 to generate a first bang-bang switching voltage, V_{SW_BB1}, that is no greater than the battery voltage, V_{BAT}, and a second bang-bang switching voltage, V_{SW_BB2}, that is greater than the battery voltage, V_{BAT}. In addition, the control loop of the switch mode power supply converter 872 may depend on the various embodiments of the power management system 870 and 870A. For example, in some embodiments, the composite control signal may be formed differently and/or have different characteristics as a function of the one of the average power tracking "buck-buck" modes selected from amoung the average power tracking "buck-buck" modes.

[001152] For example, in some embodiments of the medium power average power tracking mode, the feedback delay compensation circuit 852 and all active notice reduction circuits may be disabled. As an example, the open loop ripple compensation assist circuit 414 may be disabled. In addition, in some embodiments of the medium power average power tracking mode, the parallel amplifer 928 may be disabled and the V_{OFFSET} loop circuit 41 may be disable. In this case, as depicted in Figure 46B, the power management system 870A may configure the parallel amplifier cirucuit 874' to generate a power tracking control

signal 966 as a function of the differential V_{RAMP} signal, which is described below. The parallel amplifier cirucuit 874' may provide the power tracking control signal 966 as the switch mode power supply feedback signal 40A from the switch mode power supply converter control output 874E. Because the other contribritors to the composite control signal may be disabled, the composite control signal may be a function of the power tracking control signal 966. The average power tracking control signal 966 may be proportional to an error voltage substantially equal to a V_{RAMP} signal less the modulated power supply voltage, V_{CC}, where the V_{RAMP} signal is a single ended version of the differential V_{RAMP} signal. Alternatively, in some embodiments, the As explained below with respect to the parallel amplifier 2000, depicted in Figure 46C, in still other embodiments, the composite control signal may be provided by an embodiment of the parallel amplifier 928 configured to provide a modulation mode feedback signal that is substantially equivalent to the average power tracking control signal 966 while the parallel amplifier output 928C is configured to provide a high impedance path to ground. In still other embodiments, the composite control signal may be provided by an embodiment of the V_{OFFSET} loop circuit 41 adapted to regulate the switch mode power supply converter 872 in various average power tracking modulation modes of operation. For example, Figure 46D depicts an embodiment of a V_{OFFSET} loop circuit 41C adapted to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to provide a composite control signal substantially equivalent to the average power tracking control signal 966. However, in some embodiments, V_{OFFSET} loop circuit 41C may be adapted to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, that is based on a weighted error voltage between a target voltage for the modulated power supply output 876 and the modulate power supply voltage, V_{CC}. In some embodiments, the V_{OFFSET} loop circuit 41C may be further adapted to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to provide a composite control signal substantially equivalent to the average power tracking control signal 966 when the switcher control circuit 52S is configured to operate in one of the average power tracking "buck-buck" modes, and generate a threshold offset current 42,

$I_{THRESHOLD_OFFSET}$, that is based on a weighted error voltage between a target voltage for the modulated power supply output 876 and the modulate power supply voltage, V_{CC}, when the switcher control circuit 52S is configured to operate in one of the average power tracking "buck-boost" modes.

[001153] In addition, in the medium power average power tracking modulation mode, the various embodiments of the power management system 870 and 870A may the parallel amplifier circuit output 874A to provide a low impedance path to ground such that the coupling capacitor 18A is substantially coupled between the modulated power supply output 876 and ground. The coupling capacitor 18A may be substantially in parallel with the bypass capacitor 19, which may reduce the voltage ripple generated at the modulated power supply output 876 by the switching action of switch mode power supply converter 872.

[001154] In addition, as depicted in Figures 40D-E and Figure 46E-H, the bypass capacitor 19 may be replace by a capacitor array 19A. Depending on the mode of operation of the communication device, a band of operation in which the communication device is operating, a number of resource blocks allocated for a data transmission, some embodiments of the parallel amplifier circuits 847B'-C' and 874E'-H' may switchably control the capacitor array 19A to increase the amount of bypass capacitance between the modulated power supply output 876. For example, increase in the amount of bypass capacitance provide by the capacitor array 19A may increase the ripple rejection at the modulate power supply output 876, which decreases ripple voltage in the modulated power supply voltage, V_{CC}, provided to the various embodiments of the radio frequency power amplifier 869 and the radio frequency power amplifier 869'. As an example, the various embodiments of the power management system 870 and 870A may configured the decoupling capacitance at the modulated power supply output 876 as a function of the number of resource blocks to be used for a particular LTE band number assigned to a communication device. As discussed above, the LTE band number may correspond to a band of operation in which a communication device is assigned to operate in a mobile communication

network. As a futher example, the decoupling capacitance provided by decoupling capacitor array 19A may be switchably configured to provide substantially near between 1nF to 2 nF when at least twelve resource blocks are to be used during a data transmission. Alternatively, the decoupling capacitor array 19A may be switchably configured to provide substantially near between 4nF to 8 nF when at less than twelve resource blocks are to be used during a data transmission.

[001155] Similarly, when configured to operate in the medium power average power tracking mode, the decoupling capacitor array 19A may be switchably configured to provide additional decoupling capacitance to reduce the ripple voltage generated at the switch mode power supply output 876 as a function of the selected average power tracking "bang-bang" mode. For example, as the magnitude of the swing of the switching voltage, V_{SW}, increases switch generated at the switching voltage output

[001156] For example, referring to Figure 46B, in some embodiments of the medium power average power tracking modulation mode, the switcher control circuit 52S and/or the controller 50 may enable the average power tracking controller circuit 944, and disable any embodiment of an active noise reduction circuit such as an open loop ripple compensation assist circuit 414. The controller 50 may further disable the feedback delay compensation circuit 852, and the V_{OFFSET} loop circuit 41, and the parallel amplifier 928, depicted in Figures 40B and 46B, to generate a composite control signal substantially based on the average power tracking control signal 966 generated by the average power tracking controller circuit 944 as a function of the differential V_{RAMP} signal.

[001157] As discussed below with respect to Figure 46B, the parallel amplifier circuit 874' may provide an average power tracking control signal 966 as the switch mode power supply feedback signal 40A. The average power tracking control signal 966 is an error signal generated based on a different between a target output voltage of the modulated power supply voltage, V_{CC}, provided by the differential V_{RAMP} signal and the modulated power supply voltage, V_{CC}, received at the modulated power supply voltage feedback input 874F. The

average power tracking control signal 966 may represent an error signal between a present voltage at the modulated power supply output 876 and a target voltage to be generated at the modulated power supply output 876 by the switch mode power supply converter 872.

[001158] As described below, the power tracking control signal 966 may be substantially equal to a product of the programmable average power tracking transconductance, Gm_{APT}, and a difference voltage substantially equal to the V_{RAMP} signal less the modulated power supply voltage, V_{CC}: The composite control signal may be expressed mathematically as being substantially equal to Gm_{APT} x (V_{RAMP} - V_{CC}). The frequency of operation of the switch mode power supply converter may be adjusted by adjusting the magnitude of the programmable average power tracking transconductance, Gm_{APT}, the inductance of the power inductor 16, and the level thresholds used to switch between the first bang-bang switching voltage, V_{SW_BB1}, and the second bang-bang switching voltage, V_{SW_BB2}.

[001159] Because the parallel amplifier circuit output 874A is configured to provide a low impedance path to ground, the switcher control circuit 52S may be configured to regulate the modulated power supply voltage, V_{CC}, by providing a switching voltage, V_{SW}, to the switching voltage output 26 to induce a switching current provided to the modulated power supply output 876. As a result, in the "buck-buck" mode of operation, the shunt level threshold 124, the first buck level threshold 125, and the series level threshold 126 provide to the first comparator 140, the fifth comparator 141, and the second comparator 142, may be configured to control the frequency of operation of the switch mode power supply converter 872 and a ripple voltage at the modulated power supply output 876. In addition, or alternatively, in some embodiments, the magnitude of the average power tracking control signal 966 may be increased or decreased to control the switching frequency of the switch mode power supply converter 872 and the ripple voltage at the modulated power supply output 876. In some embodiments, the switcher control circuit 52S may enable the frequency locked loop circuit similar to either the frequency locked loop circuit 54A or the frequency

locked loop circuit 54B to regulate the switching frequency of the switch mode power supply converter 872. Alternatively, the switcher control circuit 52S may operate in a free-running mode. In the free-running mode, the switching frequency of the switch mode power supply converter 872 may be determined by selected values of the shunt level threshold 124, the first buck level threshold 125, and the series level threshold 126.

[001160] As another example, in those embodiments of the parallel amplifier circuits 874 and 874' that include a V_{OFFSET} loop circuit 41 similar to an embodiment of the V_{OFFSET} loop circuit 41C, depicted in Figure 46D, the switcher control circuit 52S may be configured to operate in the average power tracking "buck-boost" mode.

[001161] To enable the switcher control circuit 52S to operate in the average power tracking "buck-boost" mode, the switcher control circuit 52S may disable the input configured to receive the switch mode power supply feedback signal 40A. Alternatively, the controller 50 may disable the average power tracking controller circuit 944. The controller 50 may enable the V_{OFFSET} loop circuit 41 to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$. As a result, the composite control signal is substantially equal to $-I_{THRESHOLD_OFFSET}$.

[001162] Referring to Figues 4S and 5S, the logic circuit 148S may include various embodiments of state machines to control the operation of the switch mode power supply converter 872 in a number of different average power tracking modes. For example, Figure 5S depicts an example state machine 2240 provided for by the logic circuit 148S. The state machine 2240 may include a first average power tracking "band-bang" output mode 2242 and a second average power tracking "bang-bang" output mode 2244. In the the first average power tracking "band-bang" output mode 2242, the logic unit 104S may configure the series switch control output 162, the shunt switch control output 164, and the charge pump mode control signal 60 to govern the operation of generation of a first "bang-bang" switching voltage, $V_{SW_BB1,}$ at the switching voltage output 26. In the second average power tracking "bang-bang" output mode 2244, the logic unit 104S may configure the series switch control output 162, the shunt switch

control output 164, and the charge pump mode control signal 60 to govern the operation of generation of a first "bang-bang" switching voltage, V_{SW_BB1}, at the switching voltage output 26. To ensure symmetric switching between the first average power tracking "band-bang" output mode 2242 and the second average power tracking "bang-bang" output mode 2244, the controller 50 may configure the logic unit 104S to use the shunt level threshold 124 and the series level threshold 126 to govern switching between the first average power tracking "band-bang" output mode 2242 and the second average power tracking "bang-bang" output mode 2244. In some embodiments, the controller 50 may futher configure the logic unit 104S to ignore the first buck output level indication 151S, the first boost output level indication 154S, and the second boost output level indication 156S provided as inputs to the logic unit 140S while the switcher control circuit 52S is configured to operate in the average power tracking "bang-bang" mode of operation. The controller 50 may configure programmable threshold levels of the shunt level threshold parameter and thea series level threshold parameter stored in the programmable threshold circuit 122,

In the first average power tracking "band-bang" output mode 2242, the control unit 104S compares the composite control signal to the series level threshold to determine whether the composite control signal is at least equal to the series level threshold 126. Based on a determination that the the composite control signal is at least equal the series level threshold 126, the state machine 2240 transitions from the first average power tracking "band-bang" output mode 2242 to the second average power tracking "bang-bang" output mode 2244. Otherwise, based on a determination that the composite control signal is less than the shunt level threshold 124, the state machine 2240 remains in the first average power tracking "band-bang" output mode 2242. While in the first average power tracking "band-bang" output mode 2242, the switch mode power supply converter 872 may be configured to generate one of the first "bang-bang" switching voltages, as provided in Table 5. The power management system 870A may set the average power tracking mode of operation as a function of the battery voltage, V_{BAT}, and the expected output power to be

generated by the radio frequency power amplifier 869'. As an example, the power management system 879A may determine the maximum power amplifier supply voltage, V_{CC_MAX}, is expected to be generated based on the envelope characteristics of the modulate radio frequency input signal to be transmitted by the radio frequency power amplifier 869'. Based on a determination that the maximum power amplifier supply voltage, V_{CC_MAX}, is not greater than the battery voltage, V_{BAT}, less the headroom of the switching circuit 884, the power management system 870 may select an average power tracking "buck-buck" mode of operation to provide the modulated power supply voltage, V_{CC}, at the modulate power supply output 876. As an example, the head room of the headroom of the switching circuit 884 may be between 100mV and 300mV. On the other hand, based on a determination that the maximum power amplifier supply voltage, V_{CC_MAX}, is greater than the battery voltage, V_{BAT}, less the headroom of the switching circuit 884, but maximum power amplifier supply voltage, V_{CC_MAX}, is does not exceed the battery voltage, V_{BAT}. The power management system 870 may select an average power tracking "buck-boost" mode of operation to provide the modulated power supply voltage, V_{CC}, at the modulate power supply output 876. As an example, the power management system 870 may select the First "Buck-Boost" Mode, where the first "bang-bang" switching voltage, V_{SW_BB1}, is substantially equal to zero volts and the second "bang-bang" switching voltage, V_{SW_BB2}, is substantially equal to 3/2 x V_{BAT}. In this case, the power management system 870 to operate in a low duty cycle. Yet, as another example, based on a determination that the maximum power amplifier supply voltage, V_{CC_MAX}, is exceeds the battery voltage, V_{BAT}, the power management system 870 may select the second "buck-boost" mode in order to benefit from a lower voltage change between the first "bang-bang" switching voltage, V_{SW_BB1}, and the second "bang-bang" switching voltage, V_{SW_BB2}, which will tend to reduce the ripple voltage or ripple currents generated at the modulated power supply output 867 and improve efficiency of the switch mode power supply coverter 872.

[001163] In some embodiments, the controller 50 may configure the switcher control circuit 52S to operate in a number of average power tracking "bang-bang" modes. For example, in some embodiments, the average power tracking "bang-bang" modes may include a number of average power tracking "buck-buck" modes and a number of average power tracking "buck-boost" modes, which are depicted in TABLE 5.

Average Power Tracking "Bang-Bang" Mode of Operation	First "Bang-Bang" Switching Voltage (V_{SW_BB1})	Second "Bang-Bang" Switching Voltage (V_{SW_BB2})
First "Buck-Buck" Mode	0	V_{BAT}
Second "Buck-Buck" Mode	1/2 x V_{BAT}	V_{BAT}
Third "Buck-Buck" Mode	0	1/2 x V_{BAT}
First "Buck-Boost" Mode	0	3/2 x V_{BAT}
Second "Buck-Boost" Mode	1/2 x V_{BAT}	3/2 x V_{BAT}
Third "Buck-Boost" Mode	1 x V_{BAT}	3/2 x V_{BAT}
Fourth "Buck-Boost" Mode	0	2 x V_{BAT}
Fifth "Buck-Boost" Mode	1/2 x V_{BAT}	2 x V_{BAT}
Sixth "Buck-Boost" Mode	1 x V_{BAT}	2 x V_{BAT}

TABLE 5

[001164] As an example, the average power tracking "buck-buck" modes may include at least a first "buck-buck" mode, a second "buck-buck" mode, and a third "buck-buck" mode. The average power tracking "buck-boost" modes may include a first "buck-boost" mode, a second "buck-boost", a third "buck-boost", a fourth "buck-boost", a fifth "buck-boost" mode, and a sixth "buck-boost" mode. To configure the switcher control circuit 52S to operate in one of the average power tracking "buck-buck" modes, the controller 50 may set an average power tracking boost mode parameter to disabled. To configure the switcher control circuit 52S to operate in one of the "buck-boost" modes, the controller 50 may set an average power tracking boost mode parameter to enabled.

[001165] In the first "buck-buck" mode the switcher control circuit 52S may disable the multi-level charge pump 882. The switcher control circuit 52S may configure the switching circuit 884 to generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to zero volts and a second bang-bang switching voltage, V_{SW_BB1} substantially equal to the battery voltage, V_{BAT}.

[001166] respectively. In addition, the threshold detector and control circuit 132 may further include a fifth comparator configured to receive a first buck level threshold 125.

[001167] Referring to Figures 40C and 46B, some embodiments of the V_{OFFSET} loop circuit 41 may be configured to provide a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the switcher control circuit 880 in the medium power average power tracking modulation mode. As an example, Figure 46D depicts embodiments of a V_{OFFSET} loop circuit 41C that may generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, as a function of the differential V_{RAMP} signal and the modulated power supply voltage, V_{CC}, received at the modulated power supply voltage feedback input 874F. In some embodiments, the V_{OFFSET} loop circuit 41C may be configured to generate the threshold offset current 42, $I_{THRESHOLD_TARGET}$, by integrating a difference between the modulated power supply voltage, V_{CC}, and the target output voltage of the modulated power supply voltage, V_{CC}, derived from the differential V_{RAMP} signal. In some embodiments, the programmable time constants of the V_{OFFSET} loop circuit 41C may be configured to improved stability, increase a responsiveness of the control loop governing the generation of the switching voltage, V_{SW}, or configured the switch mode power supply converter 872 to pre-charge the modulated power supply voltage, V_{CC}, prior to commencement of a data transmission. As depicted in Figure 46D, in some embodiments of the V_{OFFSET} loop circuit 41C, may receive a single-ended version of the V_{RAMP} signal. And the V_{OFFSET} loop circuit 41C may be further configured to pre-distort the V_{RAMP} signal to provide a frequency response compensated target voltage derived from the differential V_{RAMP} signal. In some alternative embodiments, the V_{OFFSET} loop circuit 41C may receive a compensated V_{RAMP} signal, V_{RAMP_C}, which may be used as a frequency

compensated target voltage of the modulated power supply voltage, V_{CC}. The threshold offset current 42, $I_{THRESHOLD_TARGET}$, generated with either the V_{RAMP} signal or the compensated V_{RAMP} signal may represent an average error in the modulated power supply voltage, V_{CC}, generated at the modulated power supply output 876.

[001168] In some embodiments, the switcher control circuit 52S may be configured to operate in the average power tracking "buck-buck" mode or the average power tracking "buck-boost" mode as a function of the envelope characteristics of the modulated radio frequency input signal to be transmitted and the battery voltage, V_{BAT}. For example, in some embodiments, the controller 50 may be configured to determine a maximum expected power amplifier supply voltage, V_{CC_MAX}, for the modulated power supply voltage, V_{CC}, based on the expected envelope characteristics of the modulated radio frequency input signal to be transmitted in a data transmission. Referring to Figure 40C and 46B, the controller 50 may obtain a measurement of battery voltage, V_{BAT} from the battery level sense circuit 264. Based on the maximum expected power amplifier supply voltage, V_{CC_MAX}, the battery voltage, V_{BAT}, and a maximum target duty cycle of the switch mode power supply converter 872, the controller 50 may select to operate the switch mode power supply converter 872 in either the average power tracking "buck-buck" mode or the "average power tracking "buck-boost" mode." In some embodiments, the maximum target duty cycle may be based on a maximum desired ripple voltage generated at the modulated power supply output 876.

[001169] As an example, in the case where the battery voltage, V_{BAT}, is sufficient to generate the maximum expected power amplifier supply voltage, V_{CC_MAX}, using a duty cycle that is no greater than the target duty cycle, the controller 50 may configure the switcher control circuit 880 to generate the switching voltage, V_{SW}, in the average power tracking "buck-buck" mode. In the case where the battery voltage is insufficient to generate the maximum expected power amplifier supply voltage, V_{CC_MAX}, using a duty cycle that is no greater than the target duty cycle, the controller 50 may configure the switcher control

circuit 880 to generate the switching voltage, V_{SW}, in the average power tracking "buck-boost" mode. In addition, in some embodiments, the minimum target duty cycle may be determined as a function of the stability of the switch mode power supply converter 872.

[001170] In the "bang-bang" mode of operation, the switch mode power supply converter 872 may be configured switch between a first bang-bang switching voltage, $V_{SW_BB1,}$ and a second bang-bang switching voltage, V_{SW_BB2}. For example, in a first "buck-buck" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to ground and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 1 x V_{BAT}. Alternatively, in a second "buck-buck" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to 1/2 x V_{BAT}, and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 1 x V_{BAT}. And in a third "buck-buck" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to ground and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 1 x V_{BAT}. In the case where the switch mode power supply converter 872 is configured to generate the switching voltage, V_{SW}, by a switch between the battery voltage, V_{BAT}, and ground, the switcher control circuit 880 may disable the multi-level charge pump 882.

[001171] In the "buck-boost" average power tracking mode, the switch mode power supply converter 872 may be configured to generate a first "bang-bang" switching voltage, V_{SW_BB1}, that is no greater than the battery voltage, V_{BAT}, and second "bang-bang" switching voltage, V_{SW_BB2}, that is greater than the battery voltage, V_{BAT}. Because the switch mode power supply converter 872 is configured to generate at least one "boost" voltage in the "buck-boost" average power tracking mode, the switcher control circuit 880 may not disable the multi-level charge pump 882.

[001172] For example, in a first "buck-boost" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching

voltage, V_{SW_BB1}, substantially equal to ground and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 3/2 x V_{BAT}. Alternatively, in a second "buck-boost" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to 1/2 x V_{BAT}, and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 3/2 x V_{BAT}. In a third "buck-boost" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to 1 x V_{BAT}, and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 3/2 x V_{BAT}. In a fourth "buck-boost" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to ground and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 2 x V_{BAT}. In a fifth "buck-boost" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to 1/2 x V_{BAT}, and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 2 x V_{BAT}. And in a sixth "buck-boost" average power tracking mode, the switch mode power supply converter may generate a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to 1 x V_{BAT}, and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to 2 x V_{BAT}.

[001173] In some embodiments of the multi-level charge pump 882, the multi-level charge pump 882 may be further configured to generate other fractions of the battery voltage, V_{BAT}. For example, in the "buck-buck" average power tracking mode, the switch mode power supply converter 872 may be configured to generate a first "bang-bang" switching voltage, V_{SW_BB1}, substantially equal to m_1/n_1 x V_{BAT}, and a second "bang-bang" switching voltage, V_{SW_BB2}, substantially equal to m_2/n_2 x V_{BAT}, where $m_1/n_1 \leq 1 < m_2/n_2$. Alternatively, may have a first bang-bang voltage level generated as the switching voltage, V_{SW}, at the switching voltage output 26 such that m/n is substantially m_1/n_1 x $V_{BAT} < V_{SW} \leq m_2/n_2$ x V_{BAT}, where $m_1/n_1 < m_2/n_2 \leq 1$.

[001174] The controller 50 may configure the propagation delay period provided by the programmable delay circuitry 432C, 432C', and 432C" as a function of the power level modulation mode. For example, referring briefly to Figure 40B, the switcher propagation delay may include the time period between a change in an operational state of the switcher control circuit 880 to generate a switching voltage, V_{SW}, and the application or generation of the switching voltage, V_{SW} at the switching voltage output 26. As depicted in Figure 40B, the switcher propagation delay of the switch mode power supply converter 872 may be related to both the signal propagation from the switcher control circuit 880 to a multi-level charge pump 882 and a switching circuit 884 and the delay associated with transitioning between a present value of the switching voltage, V_{SW}, and the to be generated switching voltage, V_{SW}. As an example, the segmentation mode of the switching circuit 884 may impact the switcher propagation delay because the current driving and sinking capacity of the switching circuit 884 may be reduced as a function of segmentation mode. In addition, in the average power tracking mode, the switcher propagation delay may vary depending on whether the switcher control circuit 880 is configured to operate in an average power tracking "buck-buck" mode or the average power tracking "buck-boost" mode due to the operation of the multi-level charge pump 882. For example, switcher propagation delay of the switch mode power supply converter 872 may be substantially less when the switcher control circuit 880 is configured to operated in the average power tracking "buck-buck" mode to switch between a first bang-bang switching voltage, V_{SW_BB1}, substantially equal to ground and a second bang-bang switching voltage, V_{SW_BB2}, substantially equal to V_{BAT}.

[001175] Accordingly, in some embodiments, the controller 50 may configure the programmable delay period of the programmable delay circuitry 432 as a function of the segmentation mode of the switching circuit 884. In addition, the controller 50 may configure the programmable delay period of the programmable delay circuitry 432 as a function of the average power tracking "buck-buck" mode.

[001176] First embodiment of the PARALLEL AMPLIFIER CIRCUIT

[001177] Figure 40C depicts an embodiment of the parallel amplifier circuit 874 that includes a differential filter 924 configured to generate a control signal 926 based on the differential V_{RAMP} signal. The differential filter 924 may provide degrees of frequency response correction as a function of the expected output power of the radio frequency power amplifier 869. For example, the controller 50 may determine or obtain the expected output power to be generated by the radio frequency power amplifier 869 during a data transmission in an upcoming data transmission slot. For example, the controller 50 may obtain the expected output power of the radio frequency power amplifier 869 from the digital baseband processing portion of a transceiver or modem that provides the differential V_{RAMP} signal.

[001178] Based on a determination that the expected output power of the radio frequency power amplifier 869 is at least equal to the high power modulation mode threshold, the controller 50 may configure the differential filter 924 to provide maximum peaking of the differential V_{RAMP} signal. Alternatively, in some embodiments, either the controller 50 or the power management system 870 may receive an indication to configure the power management system to operate in the high power modulation mode. In this case, the differential filter 924 may be configured to provide a maximum level of frequency response compensation or correction.

[001179] Alternatively, based on a determination that the output power to be generated by the radio frequency power amplifier 869 is less than the high power modulation mode threshold but greater than the low power modulation mode threshold, the power management system 870 may configure the differential filter 924 to provide a medium level of frequency response correction. In other words, based on a determination that the expected output power of the radio frequency power amplifier 869 is less than the high power modulation mode threshold, the controller 50 or the power management system 870 may configured configure the differential filter 924 to provide less frequency response compensation as a function of the expected output power of the radio frequency power amplifier 869.

[001180] As another example, based on a determination that the radio frequency power amplifier will generate an expected output power less than the low power modulation mode threshold, the controller 50 may configure the differential filter 924 to provide either minimum or no frequency response correction as a function of a tracking mode of the power management system 870. As an alternative example, the power management system 870 may have a slow tracking mode and a no tracking mode of operation. In the slow tracking mode of operation, the differential V_{RAMP} signal slowly tracks the envelope of the modulate radio frequency input signal having an input power P_{IN}, which is provided to the radio frequency power amplifier input. In the no tracking mode of operation, the differential the V_{RAMP} signal generates a substantially fixed output voltage as the control signal 926. In other words, the differential filter 924 may be configured to provide no frequency compensation when the power management system 870 is configured to not track the envelope of the modulate radio frequency input signal to be transmitted by the radio frequency power amplifier 869. However, in the slow tracking mode of operation, the differential filter 924 may be configured to provide some minimal frequency response compensation or correction. As an example, based on the tracking mode and set to the slow tracking mode, the differential filter 924 may provide the lease on frequency response correction to compensate for parasitic inductances and parasitic capacitances associated with either the radio frequency power amplifier 869 or the signal traces the couple the collector voltage supply input 869A to the modulated power supply output 876. In some embodiments, the degree of frequency response correction or compensation may be based on a relative scale of tracking. In this case, the jury a frequency response correction of competition in a function of the rate at which the differential V_{RAMP} signal tracks the envelope of the modulated radio frequency input signal.

[001181] Some embodiments of the differential filter 924 may be similar in form and function to the previously described embodiments of a digital V_{RAMP} pre-distortion filter circuit 812 and the analog V_{RAMP} pre-distortion filter circuit 844

depicted in Figure 37A and Figure 37C, respectively. The differential filter 924 may be configured to pre-distortion the received differential V_{RAMP} signal to compensate for frequency response of the parallel amplifier 928. In addition, the differential filter 924 may be further configured to compensate for parasitic impedances of the radio frequency power amplifier 869 in a similar fashion as previously described with respect to the analog V_{RAMP} pre-distortion filter circuit 844 and digital V_{RAMP} pre-distortion filter circuit 812.

[001182] The parallel amplifier 928 may be similar in form and function to as embodiments of the parallel amplifiers 35, 35A, 35D, and 35G and the embodiments of the rechargeable parallel amplifiers 35B, 35C, 35E, 35F, 35H, and 35I, depicted in the Figures 12A-I. As will be discussed below, some embodiments of the parallel amplifier 928 may be similar to the parallel amplifier 2200, depicted in Figure 46C. The parallel amplifier 928 may include a non-inverting input 928A configured to receive the control signal 926. In some embodiments, the control signal 926 may be a compensated V_{RAMP} signal, V_{RAMP_C}. The parallel amplifier 928 may also include an inverting input 928B in communication with the modulated power supply output 876. Based on the difference between the control signal and the modulated power supply voltage, V_{CC}, the parallel amplifier 928 generate a parallel amplifier output current, I_{PARA_AMP}, at the parallel amplifier output 928C in order to generate the parallel amplifier output voltage, V_{PARA_AMP}. The parallel amplifier 928 may generate a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, which is a fractional representation of the parallel amplifier output current, I_{PARA_AMP}, from the parallel amplifier feedback output 928E. The parallel amplifier 928 may include a parallel amplifier supply voltage input 928D configured to receive a μC charge pump output voltage, $V_{\mu C_OUT}$, from the μC charge pump circuit 262. Alternatively, as previously described, in some embodiments the parallel amplifier supply voltage input 928D may be switchably configured to be powered by the μC charge pump output voltage, $V_{\mu C_OUT}$, or a supply voltage provided by the multi-level charge pump 882 of the switch mode power supply converter 872, depicted in Figure 40B. As an example, some embodiments of the switch mode

power supply converter 872 may be configured to provide a parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, generated from the internal charge pump node parallel amplifier supply 294 or the charge pump output voltage, V_{CP_OUTPUT}, as depicted in Figures 7B-D, to power the parallel amplifier circuit 874 and/or the linear regulator 930, LDO.

[001183] As previously described above most respected Figure 18A-D, the μC charge pump circuit 262, may be configured to provide various power supply voltage levels to power the parallel amplifier 928 as a function of the battery voltage, V_{BAT}, the offset voltage across the coupling capacitor 18A, and the an expected envelope characteristics of signal to be transmitted.

[001184] For example, in some embodiments, the μC charge pump circuit 262 may generate the μC charge pump output voltage, $V_{\mu C_OUT}$, as a function of the battery voltage and the modulation mode of operation. For example, in the high power modulation mode, the power management system 870 may configure the μC charge pump circuit 262 to operate in the 1 x V_{BAT} mode or the 4/3 x V_{BAT} mode to generate the μC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to either the battery voltage, 1 x V_{BAT}, or 4/3 x V_{BAT}, respectively. In the medium power modulation mode, the power management system 870 may configure the μC charge pump circuit 262 to operate in the 1 x V_{BAT} mode or the 2/3 x V_{BAT} mode to generate the μC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to either the battery voltage, V_{BAT}, or 2/3 x V_{BAT}, respectively. In some embodiments, in the low power modulation mode, the power management system 870 may configure the μC charge pump circuit 262 to operate in the 1/4 x V_{BAT} mode, 1/3 x V_{BAT} mode, or the 1/2 x V_{BAT} mode to generate the μC charge pump output voltage, $V_{\mu C_OUT}$, substantially equal to 1/4 x V_{BAT}, 1/3 x V_{BAT}, or 1/2 x V_{BAT}, respectively.

[001185] Figure 40C further depicts that the μC charge pump circuit 262 may be configured to receive a μC charge pump clock 276 from a clock management circuit 260. As previously discussed relative to Figure 19A-B, the clock management circuit 260 to generate the μC charge pump clock 276 based on the oscillator 270 or the switching frequency of the switch mode power supply

converter 872. For example, in some embodiments, the switching frequency of the switch mode power supply converter 872 may be controlled by a frequency locked loop circuit, as described with respect to Figure 40B. In some embodiments, the clock management circuit 260 may power down the oscillator 270 when the switch mode power supply converter 872 is enabled. For example, in the high power modulation mode and the medium power modulation mode, the clock management circuit 260 may provide a µC charge pump clock 276 based on the switching frequency of the switch mode power supply converter 872 and disable the oscillator 270 . However, in the low power modulation mode, the clock management circuit 260 may enable the oscillator 270 to generate the µC charge pump clock 276.

[001186] The power management system 870 may configure the clock management circuit 260 to provide a µC charge pump clock 276 that maximizes the efficiency of the power management system 870 as a function of the expected output power of the radio frequency power amplifier 869. For example, the power management system 870 may configure the clock management circuit 260 to provide a µC charge pump clock 276 between about 0.5 MHz and 3 MHz when operating in the low power modulation mode. In the case where the clock management circuit provides the µC charge pump clock 276 based on the switching frequency of the switch mode power supply converter 872, the clock management circuit may be configured to disable the oscillator 270 to conserve energy drawn from the battery 20.

[001187] In some embodiments, the parallel amplifier 928 may be configured as a parallel amplifier similar to the parallel amplifiers 35A, 35D, and 35G, depicted in Figures 12A, 12D, and 12G. In other embodiments, the parallel amplifier 928 may be configured as a rechargeable parallel amplifier similar to the rechargeable parallel amplifiers 35B-C, 35E-F, and 35H-I, depicted in Figures 12B-C, 12E-F, and 12H-I. In some embodiments, the parallel amplifier 928 may include a segmented parallel amplifier output stage similar to those of parallel amplifiers 35G-I, depicted in Figure 12G-I. For example, some embodiments of the parallel amplifiers 35G-I may include segmented parallel

amplifier output stage dived into two or more segments. In some embodiments, the parallel amplifier 928 may be similar to the parallel amplifier 2200, depicted in Figure 46C.

[001188] In some embodiments, the segmented parallel amplifier output stage of the parallel amplifier 928 may be configured based upon the expected output power of the radio frequency power amplifier 869. As an example, the segmentation configuration of the parallel amplifier 928 may be a function of the maximum instantaneous output power, P_{INST_MAX}, to be generated by the radio frequency power amplifier 869 during the data transmission and the expected load line, $R_{RF_AMP_EXP}$, of the radio frequency power amplifier 869 during the data transmission. As an example, in some embodiments, the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to be provided by the parallel amplifier 928 during the data transmission may be substantially equal to $(P_{INST_MAX} / R_{RF_AMP_EXP})^{1/2}$. In some embodiments, the parallel amplifier 928 may include a maximum parallel amplifier output current, I_{PARA_MAX}, which is the maximum output current to be generated by the parallel amplifier 928. In some embodiments, the power management system 870 may configure the segmentation configuration of the parallel amplifier 928 based on the maximum parallel amplifier output current, I_{PARA_MAX}, and the maximum instantaneous output current, $I_{MAX_PARA_AMP}$. For example, in some embodiments, the controller may determine the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, based on the envelope characteristics of the modulated radio frequency input signal to be transmitted and the expected load line, $R_{RF_AMP_EXP}$, of the radio frequency power amplifier 869 during the data transmission. The power management system 870 may determine the maximum instantaneous output power, P_{INST_MAX}, based on the envelope characteristics of the modulated radio frequency input signal. Based on the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, the power management system 870 may determine an estimated percentage of output current generation capacity of the parallel amplifier 928 that may be used during the data transmission. For example, the power management system 870 may calculate the percentage of the output current generation capacity based on

the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to the maximum parallel amplifier output current, I_{PARA_MAX}. The power management system 870 may determine the number of output stage segments of the parallel amplifier 928 to enable based on the estimated percentage of output current generation capacity of the parallel amplifier 928 to be used. For example, in the case where the parallel amplifier 928 includes two output stage segments that are configured to have a substantially equal output current generation capacity, the power management system 870 may set the segmentation configuration to be 100% when the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to the maximum parallel amplifier output current, I_{PARA_MAX}, is substantially equal to or near at least 50%. The power management system 870 may set the segmentation configuration to be 50% when the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to the maximum parallel amplifier output current, I_{PARA_MAX}, is at least less than 50%. In the case where the output stage segments of the parallel amplifier 928 are not substantially equal, the controller 50 may determine which of the output stage segments to enable based on the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, and the current generation capacity of each of the output stage segments.

[001189] In some alternative embodiments, the segmentation configuration of the parallel amplifier 928 may be based on the expected peak-to-peak swing of the modulated power supply voltage, V_{CC_PKPK}, and the expected load line, $R_{RF_AMP_EXP}$, of the radio frequency power amplifier 869 and 869' during the data transmission.

[001190] For example, when operating in the high power modulation mode, the power management system 870 may set the segmentation configuration to be 100%. Alternatively, the power management system 870 may configure the parallel amplifier 928 to use only the first output stage segment or only the second output stage segment while operating in the medium power modulation mode depending on the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to the maximum parallel amplifier output current, I_{PARA_MAX}. And in

the low power modulation mode, the power management system 870 may disable the parallel amplifier 928 to place the parallel amplifier output 928C a high impedance mode.

[001191] As previously described with respect to Figure 40A, Figure 40C depicts that the parallel amplifier circuit 874 may provide the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, from an embodiment of the V_{OFFSET} loop circuit 41 to regulate the offset voltage, V_{OFFSET}, across the coupling capacitor 18A. For example, and not by way of limitation, in some embodiments of the parallel amplifier circuit 874, the embodiments of the V_{OFFSET} loop circuit 41 may be similar to the embodiments of the V_{OFFSET} loop circuit 41, depicted in Figures 2A-B and Figure 8, and the V_{OFFSET} loop circuit 41A, depicted in Figures 18A and Figure 18C, and the V_{OFFSET} loop circuit 41C, depicted in Figure 46D. In addition, some embodiments of the V_{OFFSET} loop circuit 41, depicted in Figures 2A-B, Figures 23A-D, and Figures 34A-E, the V_{OFFSET} loop circuit 41E, depicted in Figure 15, the V_{OFFSET} loop circuit 41F, depicted in Figure 16, the V_{OFFSET} loop circuit 41A, depicted in Figure 18A and Figure 18C, and the V_{OFFSET} loop circuit 41B, depicted in Figure 18B and Figure 18D, may be further configured to include the features, forms, techniques, circuitry, interfaces, functions, and/or combinations thereof of the various embodiments of the V_{OFFSET} loop circuit 41C depicted in Figure 46D. Accordingly, in some modes of operation, the V_{OFFSET} loop circuit 41 may be configured to pre-charge the coupling capacitor 18A prior to a data transmission.

[001192] In some embodiments, V_{OFFSET} loop circuit 41 may be configured to generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, that represents an average or integrated error between the modulated power supply voltage, V_{CC}, and a V_{RAMP} signal when the switch mode power supply converter 872 is configured to operate in an average power tracking mode of operation. Some embodiments of the V_{OFFSET} loop circuit 41 may be configured to pre-charge the bypass capacitor 19 and the coupling capacitor 18A while the switch mode power supply converter 872 is configured to operate in the average power tracking mode of operation.

[001193] For the sake of simplicity, and not by way of limitation, Figure 40C depicts that the parallel amplifier 928 may provide a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, as the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. Although not depicted, for the sake of simplicity and not by way of limitation, some alternative embodiments of the switcher control circuit 880 may also receive a feedback delay compensation signal 854, $I_{FEEDBACK_TC}$, from an embodiment of the feedback delay compensation circuit 852, depicted in Figures 38A-B and Figure 39A, and the differential feedback delay compensation circuit 852A, depicted in Figure 39B. In addition, for the sake of simplicity of description and not by way of limitation, Figure 40C depicts that the parallel amplifier 928 is configured to provide the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, as the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$. Although not depicted in Figure 40C for the sake of simplicity, other example embodiments of the parallel amplifier circuit 874 may include active noise reduction circuit configured to reduce high frequency ripple current and high frequency ripple voltage at the modulated power supply output 876.

[001194] One example of an active noise reduction circuit may include an open loop ripple compensation assist circuit 414, depicted in Figures 23A-23D. As previously described, the open loop ripple compensation assist circuit 414 may generate a high frequency ripple compensation current 416, I_{COR}, to substantially reduce high frequency ripple currents present at the modulated power supply output 876. For example, the high frequency ripple currents at the modulated power supply output 876 may induce some embodiments of a parallel amplifier 928 to generate high frequency ripple voltages in modulated power supply voltage, V_{CC}, due to a non-ideal output impedance of the parallel amplifier 928. The open loop ripple compensation assist circuit 414 may apply the high frequency ripple compensation current 416, I_{COR}, to the modulated power supply output 876 to reduce the electronic noise generated in a receiver band in response to the high frequency ripple currents. The scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, may be added to

the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, to provide the switch mode power supply feedback signal 40A.

[001195] In some embodiments, the controller 50 may configure the active noise reduction circuitry to provide a high level of active noise reduction in the high power modulation mode, a medium level of active noise reduction in the medium power modulation mode, and no active noise reduction in the low power modulation mode. Illustratively, some embodiments of the open loop ripple compensation assist circuit 414 may include programmable I_{COR} transconductance value, Gm_{ICOR}, that may be configured based on a power level modulation mode of operation. As an example, the open loop ripple compensation assist circuit 414 may include a high power modulation mode I_{COR} transconductance value, $Gm_{ICOR_HIGH_POWER}$, and a medium power modulation mode I_{COR} transconductance value, $Gm_{ICOR_MEDIUM_POWER}$. In the high power modulation mode, the controller 50 may set the programmable I_{COR} transconductance, Gm_{ICOR}, to the high power modulation mode I_{COR} transconductance value, $Gm_{ICOR_HIGH_POWER}$. In contrast, the controller 50 may set the programmable I_{COR} transconductance, Gm_{ICOR}, to a medium power modulation mode I_{COR} transconductance value, $Gm_{ICOR_MEDIUM_POWER}$, in the medium power modulation mode. And, in the low power modulation mode, the controller 50 may disable the open loop ripple compensation assist circuit 414.

[001196] The parallel amplifier circuit 874 may further include a linear regulator 930, LDO. The linear regulator 930, LDO, may be a low dropout voltage linear regulator. The parallel amplifier circuit 874 may also include a parallel amplifier output bypass switch 936, a linear regulator output selection switch 938, and feedback selection switch 940. The parallel amplifier output bypass switch 936 includes a first terminal 936A coupled to the parallel amplifier output 928C and a second terminal 936B coupled to ground. The power management system 870 may configure the parallel amplifier output bypass switch 936 to close when the parallel amplifier 928 is disabled. For example, the power management system 870 may configure the parallel amplifier output bypass switch 936 too close based on a determination that the expected output

power of the radio frequency power amplifier 869' is less than the low half power modulation mode threshold or the parallel amplifier output 928C is disabled and configured to provide a high impedance. Alternatively, the power management system 870 may configure the parallel amplifier output bypass switch 936 to be open when the parallel amplifier 928 is enabled.

[001197] The linear regulator output selection switch 938 may include an input terminal 938A coupled to a linear regulator output 930C of the linear regulator 930, a first output terminal 938B in communication with the modulated power supply output 876, and a second output terminal 938C in communication with the second linear regulator output 874D, LDO_2 OUTPUT, in communication with the CMOS logic supply input 869C of the radio frequency power amplifier 869.

[001198] The feedback selection switch 940 includes an output terminal 940A in communication with a inverting input 930B of the linear regulator 930, a first input terminal 940B in communication with the modulated power supply output 876, and the second input terminal 940C in communication with the second linear regulator output 874D, LDO_2 OUTPUT, of the parallel amplifier circuit 874. The linear regulator ninth rate also includes a linear regulator power supply input 930D configured to receive the μC charge pump output voltage, $V_{\mu C_OUT}$. The μC charge pump output voltage, $V_{\mu C_OUT}$, may be configured provide a voltage level to the linear regulator power supply input 930D as a function of the battery voltage, V_{BAT}, and the expected output power of the radio frequency power amplifier 869.

[001199] The linear regulator 930, LDO, may also include a non-inverting input 930A may be in communication with the non-inverting input 928A of the parallel amplifier. The non-inverting input 930A of the linear regulator 930, LDO, may also be in communication with the differential filter 924, and configured to receive the control signal 926 at the non-inverting input 930A. The linear regulator 930 may also receive a linear regulator feedback signal, LDO FEEDBACK, from the output terminal 940A of the feedback selection switch 940. Based on the difference between the control signal 926 and the linear regulator

feedback signal, LDO FEEDBACK, the linear regulator 930 may generate a linear regulator output voltage at the linear regulator output 930C. Based on the switch states of the linear regulator output selection switch 938 and feedback selection switch 940, the linear regulator 930, LDO, may generate a linear regulator output voltage to apply the first linear regulator output current 878A, I_{LDO}, to the modulated power supply output 876.

[001200] Alternatively, the linear regulator 930, LDO, may generate the second linear regulator output voltage, V_{LDO2}, at the second linear regulator output 874D, LDO_2 OUTPUT. Although not depicted in Figure 40C, some alternative embodiments of the parallel amplifier circuit 874 may be configured to allow the linear regulator 930 to simultaneously apply the first linear regulator output current 878A, I_{LDO}, to the modulated power supply output 876 and generate the second linear regulator output voltage, V_{LDO2}. For example, in this case, the controller 50 may configure the linear regulator 930, LDO, to provide a second linear regulator output voltage, V_{LDO2}, at least equal to the minimum CMOS logic supply voltage based on a determination by the controller that the battery voltage, V_{BAT}, is about or less than the minimum CMOS logic supply voltage. For example, in some embodiments, the controller 50 may obtain a measurement of the battery voltage, V_{BAT}, from the battery level sense circuit 264. Based on a determination that the battery voltage, V_{BAT} is less than a minimum CMOS logic supply voltage threshold, the controller 50 may configure the linear regulator 930, LDO, and the µC charge pump circuit 262 to cooperative generate a second linear regulator output voltage, V_{LDO2}, at least equal to the minimum CMOS logic supply voltage. In other alternative embodiments, the battery level sense circuit 264 may be configured to automatically detect that the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage threshold, and configure the linear regulator 930, LDO, and the µC charge pump circuit 262 to cooperatively generate a second linear regulator output voltage, V_{LDO2}, at least equal to the minimum CMOS logic supply voltage.

[001201] Some embodiments of the radio frequency power amplifier 869 may include a CMOS logic 869E. As an example, the embodiment of the radio

frequency power amplifier 869' depicted in Figure 46B. The CMOS logic 869E may control the operation of the radio frequency power amplifier 869. In some embodiments, the CMOS logic 869E may be powered by the battery voltage, V_{BAT}, received from the battery 20. The CMOS logic 869E may have a minimum CMOS logic supply voltage that corresponds to a minimum CMOS logic supply voltage threshold. Some embodiments of the radio frequency power amplifier 869 may have a minimum CMOS logic supply voltage substantially equal to 2.7 volts. Other embodiments of the radio frequency power amplifier 869 may have a minimum CMOS logic supply voltage substantially equal to 2.5 volts.

[001202] In some embodiments, the controller 50 may obtain a measurement of the battery voltage, V_{BAT}, from the battery level sense circuit 264 to determine whether the battery voltage, V_{BAT}, is at least equal to the minimum CMOS logic supply voltage threshold. In the case where the battery voltage, V_{BAT}, drops below the minimum CMOS logic supply voltage threshold, the power management system 870 may be configured to provide the second linear regulator output voltage 878D, V_{LDO2}, to the CMOS logic supply input 869C that is at least equal to the minimum CMOS logic supply voltage. Because the linear regulator 930 may be power the µC charge pump circuit 262, the operational ratio of the µC charge pump, μBB_{RATIO}, may be configured to boost the battery voltage, V_{BAT}, to provide a µC charge pump output voltage, $V_{\mu C_OUT}$. In this case, the µC charge pump circuit 262 may generate a µC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to a headroom voltage of the linear regulator 930 plus a minimum CMOS logic supply voltage.

[001203] For example, in some embodiments of the high power modulation mode and the medium power modulation mode, the controller 50 may obtain a measurement of the battery voltage, V_{BAT}, from the battery level sense circuit 264, which is configured to receive and measure the battery voltage, V_{BAT}. Based on the minimum CMOS logic supply voltage threshold and the battery voltage, $V_{BAT,}$ the controller 50 may determine an operational ratio of the µC charge pump, μBB_{RATIO}, from among the available operational ratios of the µC

charge pump, μBB_{RATIO}, that may provide a μC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum CMOS logic supply voltage threshold plus the headroom voltage of the linear regulator 930, LDO.

[001204] In addition, in some embodiments, the controller 50 may further determine the operational ratio of the μC charge pump, μBB_{RATIO}, to permit the parallel amplifier 928 to regulate the modulated power supply output 876 to provide a maximum expected power amplifier supply voltage, V_{CC_MAX}, and maintain the expected target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, across the coupling capacitor 18A. The controller 50 may select the operational ratio of the μC charge pump, μBB_{RATIO}, that results in the lowest value of the μC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum CMOS logic power supply voltage plus the headroom voltage of the linear regulator 930, LDO, and maintains the target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, across the coupling capacitor 18A. For those embodiments of the parallel amplifier circuit 874 that do not include a V_{OFFSET} loop circuit 41 and in those power level modulation modes in which the V_{OFFSET} loop circuit 41 is disabled, the controller 50 may be further configured to not determine the target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$, prior to configuring the μC charge pump circuit 262. For example, in the low power modulation mode, the controller 50 may disable the V_{OFFSET} loop circuit 41.

[001205] Figure 41 depicts an equivalent circuit of the power management system 870 when configured to operate in a low power modulation mode. The combination of the coupling capacitor 18A with the closed parallel amplifier output bypass switch 936 may be modeled as an impedance having an offset capacitance, C_{OFFSET}, and an equivalent series resistance (ESR), R_{ESR}. In addition, in the disabled state, the switch mode power supply converter 872 has an effective off state capacitance, C_{OFF}, which the linear regulator 930, LDO, must drive when the power management system 870 operates in the low power modulation mode.

[001206] For the sake of convenience, and not by way of limitation, a method 1300, a method 1400, a method 1500, and a method 1600, depicted in Figure 42, Figures 43A-B, Figures 44A-B, and Figure 45, may describe various

operations, tasks, functions, firmware, logic operations, hardware, analog logic or digital logic, a digital base band processing circuit, firmware, and/or software, a transceiver/communication device, and/or some combination thereof in terms of the controller 50 and/or the power management system 870. However, this is by way of description and not intended to limit the scope of the method 1300, the method 1400, the method 1500, and the method 1600. In addition, in some embodiments, the operations of the controller 50 and/or various selected portions of the power management system 870 may be incorporated into the hardware, software, and/or firmware of various components or portions of a transceiver/communication device.

[001207] Figure 42 depicts the method 1300 for configuring the operation of the pseudo-envelope tracking modulated power supply system 868 that depends upon the expected output power to be generated by the radio frequency power amplifier 869 during a data transmission. The method 1300 is described with continuing reference to the pseudo-envelope tracking modulated power supply system 868 and the power management system 870, depicted in Figures 40A, 40B, 40C, and 41.

[001208] Initially, the pseudo-envelope tracking modulated power supply system 868 may determine an expected output power to be generated by a radio frequency power amplifier 869 during a data transmission. (Step 1302). For example, in some embodiments, the controller 50 may determine the expected output power to be generated by the radio frequency power amplifier 869 based upon the envelope characteristics of data signal to be transmitted during a data transmission slot. In other embodiments, the digital baseband processing portion of the transceiver or modem that provides the differential V_{RAMP} signal to the parallel amplifier circuit 874 and the modulated radio frequency inpu signal to be transmitted to the radio frequency power amplifier 869 may determine the expected output power to be generated by the radio frequency power amplifier 869. Based on the expected output power to be generated by the radio frequency power amplifier 869 during the data transmission, the power management system 870 may select a power modulation mode of operation from

among a number of power modulation modes of operation. (Step 1304). For example, the power management system 870 depicted in Figure 42 includes a high power modulation mode, a medium power modulation mode, and a low power modulation mode. In the case where the expected output power to be generated by the radio frequency power amplifier 869 is greater than or equal to a high power modulation mode threshold, the power management system 870 configures the pseudo-envelope tracking modulated power supply system 868 to operate in a high power modulation mode. (Step 1306). Alternatively, in the case where the expected output power to be generated by the radio frequency power amplifier 869 is less than the high power modulation mode threshold but greater than a low power modulation mode threshold, the power management system 870 configures the pseudo-envelope tracking modulated power supply system 868 to operate in a medium power modulation mode. (Step 1308). In the case where the expected output power to be generated by the radio frequency power amplifier 869 is less than or equal to the low power modulation mode threshold, the power management system 870 may configure the pseudo-envelope tracking modulated power supply system 868 to operate in the low power modulation mode. (Step 1310).

[001209] Figures 43A-B depict the method 1400 for configuring the operation of the pseudo-envelope tracking modulated power supply system 868 to operate in a high power modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869 during a data transmission is greater than the high power modulation mode threshold. The method 1400 is described with continuing reference to the pseudo-envelope tracking modulated power supply system 868 depicted in Figures 40A, 40B, 40C, 41, 44A-B, and 45.

[001210] Prior to commencement of the data transmission, in response to the determination that the expected output power of the radio frequency power amplifier 869 will be less than the high power modulation mode threshold, the controller 50 may configure the power management system to operate in the high power modulation mode. (Step 1402). The controller 50 may configure the

operation of the linear regulator 930, LDO. (Step 1404). For example, the controller 50 may configure the linear regulator output selection switch 938 and feedback selection switch 940 to disconnect the linear regulator output 930C from the modulated power supply output 876. Based on the battery voltage, V_{BAT}, and the minimum CMOS logic supply voltage, the controller 50 may configure the linear regulator 930, LDO, to provide a second linear regulator output voltage, V_{LDO2}, to the CMOS logic supply input 869C of the radio frequency power amplifier 869. In addition, the controller 50 may configure the μC charge pump circuit 262 to provide a μC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum CMOS logic supply voltage plus the headroom voltage of the linear regulator 930, LDO. For example, the controller 50 may configure the μC charge pump circuit 262 to provide a μC charge pump output voltage, $V_{\mu C_OUT}$, at least sufficient for the linear regulator 930, LDO, to provide a second linear regulator output voltage, V_{LDO2}, to the CMOS logic supply input 869C that is substantially equal to the minimum CMOS supply voltage threshold. The controller 50 may determine an operation ratio of the μC charge pump, μBB_{RATIO}, from among the available operation ratios of the μC charge pump, μBB_{RATIO}, that produces a smallest μC charge pump output voltage, $V_{\mu C_OUT}$, to permit generation of the second linear regulator output voltage, V_{LDO2}, substantially equal to the minimum CMOS supply voltage threshold.

[001211] In addition, the controller 50 may determine an operation ratio of the μC charge pump, μBB_{RATIO}, from among the available operation ratios of the μC charge pump, μBB_{RATIO}, based on the maximum expected power amplifier supply voltage, V_{CC_MAX}. Based on the maximum expected power amplifier supply voltage, V_{CC_MAX}, the controller 50 determines a minimum μC output voltage, $V_{\mu C_OUT_MIN}$, based on the maximum expected power amplifier supply voltage, V_{CC_MAX}, and any losses between the μC charge pump circuit 262 and the parallel amplifier 928. For example, in some embodiments, the parallel amplifier supply voltage input 928D may be switchably coupled to either the battery voltage, V_{BAT}, or the μC charge pump output voltage, $V_{\mu C_OUT}$.

[001212] Based on the minimum µC output voltage, $V_{\mu C_OUT_MIN}$, and the battery voltage, V_{BAT}, the controller 50 may determine an operation ratio of the µC charge pump, μBB_{RATIO}, from among the available operation ratios of the µC charge pump, μBB_{RATIO}, that generates a µC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum µC output voltage, $V_{\mu C_OUT_MIN}$. The controller 50 determines an operation ratio of the µC charge pump, μBB_{RATIO}, having the smallest magnitude from among the available operation ratios of the µC charge pump, μBB_{RATIO}, that permits the µC charge pump circuit 262 to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum µC output voltage, $V_{\mu C_OUT_MIN}$. The controller may configure the µC charge pump circuit 262 to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, sufficient to power both the parallel amplifier 928, and the CMOS logic circuit of the radio frequency power amplifier 869. In some embodiments, the controller 50 may further determine whether the minimum µC output voltage, $V_{\mu C_OUT_MIN}$, is no more than the battery voltage, V_{BAT}. If the minimum µC output voltage, $V_{\mu C_OUT_MIN}$, is no greater than the battery voltage, V_{BAT}, and the battery voltage, V_{BAT}, is less than the minimum CMOS supply voltage threshold, the controller 50 may configure the parallel amplifier 928 to be powered by the battery voltage, V_{BAT}. In this case, the controller 50 may then configure the µC charge pump circuit 262 to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum CMOS supply voltage threshold plus the headroom voltage of the linear regulator 930, LDO. However, if the minimum µC output voltage, $V_{\mu C_OUT_MIN}$, is greater than the battery voltage, V_{BAT}, and the minimum CMOS supply voltage threshold plus the headroom voltage of the linear regulator 930, LDO, the controller 50 may configure the µC charge pump circuit 262 to generate a µC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum µC output voltage, $V_{\mu C_OUT_MIN}$.

[001213] The controller 50 may configure the differential filter 924 to pre-distort the differential V_{RAMP} signal to provide a compensated V_{RAMP} signal to the parallel amplifier 928 based on the magnitude of the expected output power to be generated by the radio frequency power amplifier 869. (Step 1406). The

controller may configure the differential filter 924 to provide a maximum level of frequency compensation while operating in the high power modulation mode.

[001214] The controller 50 may configure the μC charge pump circuit 262 to provide a supply voltage to the parallel amplifier 928 as a function of the battery voltage. (Step 1408). The controller 50 may configure the μC charge pump circuit 262 to operate in the 4/3 x V_{BAT} mode or the 1 x V_{BAT} mode.

[001215] The controller 50 may configure the parallel amplifier output bypass switch 936 to be in an open state. (Step 1410). The controller 50 may configure the operation of the switch mode power supply converter 872 as a function of the expected high output power of the signal to be transmitted by the radio frequency power amplifier 869. (Step 1412). The controller 50 may compare the expected output power of the radio frequency power amplifier 869 to the maximum average power, P_{MAX_AVE}, to determine the number of sets of series and shunt switches to enable. Based upon determination, the controller 50 configures the switcher control circuit 880. In some embodiments, the controller 50 may configure the switcher control circuit 880 to enable all of the sets of series and shunt switches while operating in the high power modulation mode.

[001216] The controller 50 may configure the segmentation configuration of the parallel amplifier 928 based on the expected parallel amplifier output current, I_{PARA_AMP}. (Step 1414). For example, in the high power modulation mode, the controller 50 may set the segmentation configuration of the parallel amplifier 928 to enable all the output stage segments of the segmented parallel amplifier output stage.

[001217] The controller 50 may configure the active noise reduction circuit for the high power modulation mode. (Step 1416). The controller 50 may configure the active noise reduction circuit to provide a high level of noise reduction. For example, the controller 50 may set the programmable I_{COR} transconductance value, Gm_{ICOR}, of the open loop ripple compensation assist circuit 414 to a high power modulation mode I_{COR} transconductance value, $Gm_{ICOR_HIGH_POWER}$.

[001218] For example, in the case where the active noise reduction circuit is an open loop ripple compensation assist circuit 414, the controller 50 may configure

the open loop ripple compensation assist circuit 414 to generate and apply a high frequency ripple compensation current 416, I_{COR}, based on the high power modulation mode I_{COR} transconductance value, $Gm_{ICOR_HIGH_POWER}$, to the modulated power supply output 876 to reduce the noise present in the receive channel of a band of operation.

[001219] The controller 50 may configure the operation of the V_{OFFSET} loop circuit 41. (Step 1418). The controller 50 may determine the target offset voltage parameter, V_{OFFSET_TARGET}, of the V_{OFFSET} loop circuit 41 based on the battery voltage, V_{BAT}, the expected envelope characteristics of the modulated radio frequency input signal to be transmitted, and the minimum offset voltage, V_{OFFSET_MIN}. In addition, the controller 50 may configure the V_{OFFSET} loop circuit 41 to operate in a pre-charge mode of operation as a function of the target offset voltage parameter, V_{OFFSET_TARGET}, and the offset voltage, V_{OFFSET}, across the coupling capacitor 18A.

[001220] The controller 50 may configure the operation of the feedback delay compensation circuit 852 as a function of the expected output power of the radio frequency power amplifier 869. (Step 1420). As an example, the controller 50 may enable the feedback delay compensation circuit 852 and set the apparent gain of the feedback delay compensation circuit 852 as a function of the expected output power. For example, as the expected output power of the radio frequency power amplifier 869 increases, the controller may increase the apparent gain of the feedback delay compensation circuit 852.

[001221] After the power management system 870 is configured to operate in the medium power modulation mode, the data transmission is commenced. (Step 1422).

[001222] Figures 44A-B depict a method 1500 for configuring the operation of the pseudo-envelope tracking modulated power supply system 868 to operate in a medium power modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869 during a data transmission is less than the high power modulation mode threshold but greater than a low power modulation mode threshold. The method 1500 is

described with continuing reference to the pseudo-envelope tracking modulated power supply system 868 depicted in Figures 40A, 40B, 40C, 41, 43A-B, and 45. For the sake of convenience, and not by way of limitation, description of the method 1500 may refer to the controller 50. However, as discussed above, a digital base band processing portion of the transceiver/communication device and/or a combination of hardware and firmware associated with the power management system 870 may likewise operate in conjunction with the controller 50. In addition, the operations of controller 50 may be incorporated into the hardware and/or firmware of various components or portions of a transceiver/ communication device.

[001223] The controller 50 may configure the power management system 870 to operate in a medium power modulation mode based on the determination that the expected output power of the radio frequency power amplifier 969 is less than a high power modulation mode threshold and greater than a low power modulation mode threshold. (Step 1502).

[001224] The controller 50 may configure the operation of the linear regulator 930, LDO, to operate in the medium power modulation mode. As in the case where the battery voltage, V_{BAT}, is sufficient to power the CMOS logic circuit of the radio frequency power amplifier 869, the controller 50 may disable the linear regulator 930, LDO. Alternatively, in the event the battery voltage, V_{BAT}, is insufficient to power the CMOS logic circuit of the radio frequency power amplifier 869, the controller 50 may configure the linear regulator output selection switch 938 and feedback selection switch 940 to disconnect the linear regulator output 930C from the modulated power supply output 876. Based on the battery voltage, V_{BAT}, and the minimum operational voltage of the CMOS logic circuit, the controller 50 may configure the linear regulator 930, LDO, to provide the second linear regulator output voltage, V_{LDO2}, to the CMOS logic supply input 869C. In addition, the controller 50 may configure the µC charge pump circuit 262 to provide a sufficient charge pump output voltage, $V_{\mu C_OUT}$, to permit operation of the radio frequency power amplifier 869. In the case where the battery voltage, V_{BAT}, is sufficient to provide the minimum operational voltage and the CMOS

logic circuit, the controller 50 may disable the linear regulator 930, LDO, and configure the linear regulator output 930C to provide a high impedance load.

[001225] The controller 50 may configure the differential filter 924 to pre-distort the differential V_{RAMP} signal used to provide a compensated V_{RAMP} signal as the control signal 926 to the non-inverting input 928A, of the parallel amplifier 928. (Step 1506). The controller 50 may configure the differential filter 924 to provide a medium level of pre-distortion filtering to compensate for the frequency response of the parallel amplifier 928 and the parasitic impedances associated with of the radio frequency power amplifier 869.

[001226] The controller 50 may configure the µC charge pump circuit 262 to provide a supply voltage to the parallel amplifier 928 as a function of the battery voltage, V_{BAT}. (Step 1508). For example, the controller 50 may configure the µC charge pump circuit 262 to operate in the 1 x V_{BAT} mode or the 2/3 x V_{BAT} mode of operation.

[001227] The controller 50 may configure the parallel amplifier output bypass switch 936 to be in an open state. (Step 1510). The controller 50 may configure the operation of the switch mode power supply converter 872 as a function of the expected medium level output power of the signal to be transmitted by the radio frequency power amplifier 869. (Step 1512). The controller 50 may compare the expected output power of the radio frequency power amplifier 869 to the maximum average power, P_{MAX_AVE}, to determine the number of sets of series switch and shunt switch pairs to enable. Based upon determination, the controller 50 may configure the switcher control circuit 880 to enable the determined number of sets of series switches and shunt switches. In some embodiments, the controller 50 may configure the switcher control circuit 880 to enable either 75% or 50% of the sets of series switches and shunt switches while operating in the medium power modulation mode as a function of the expected output power of the radio frequency power amplifier 869. In addition, in some embodiments of the medium power modulation mode, the controller 50 may configure the switcher control circuit 880 to disabled the 2 x V_{BAT} boost mode of the multi-level charge pump 882. In other embodiments, the controller 50 may

configure the switcher control circuit 880 to configure the switch mode power supply converter 872 to further provide a switching voltage, V_{SW}, substantially equal to one of 3/2 x V_{BAT}, 1 x V_{BAT}, 1/2 x V_{BAT}, or 0 volts. In addition, in some embodiments, the controller 50 may configure the switcher control circuit 880 to decrease the number of sets of series and shunt switch pairs used to generate the switching voltage, V_{SW}, as a function of the magnitude of the expected output power of the radio frequency power amplifier 869 with respect to the maximum average power, P_{MAX_AVE}.

[001228] The controller 50 may configure the parallel amplifier output stage segmentation of the parallel amplifier 928 based on the expected parallel amplifier output current, I_{PARA_AMP}. (Step 1514). For example, in the medium power modulation mode, the controller 50 may determine the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to the maximum parallel amplifier output current, I_{PARA_MAX}. Based on the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to the maximum parallel amplifier output current, I_{PARA_MAX}, the controller 50 sets the segmentation configuration of the segmented parallel amplifier output stage of the parallel amplifier 928. For example, for the case where the parallel amplifier 928 includes two output stage segments with substantially equal current generation capacity, the controller 50 may set the segmentation configuration to 50% provided the ratio of the maximum instantaneous output current, $I_{MAX_PARA_AMP}$, to the maximum parallel amplifier output current, I_{PARA_MAX}, is less than 50%. Otherwise, the controller 50 may set the segmentation configuration to be 100%.

[001229] The controller 50 may configure the active noise reduction circuit for the medium power modulation mode. (Step 1516). The controller 50 may configure the active noise reduction circuit to provide a medium level of noise reduction. For example, the controller 50 may set the programmable I_{COR} transconductance value, Gm_{ICOR}, of the open loop ripple compensation assist circuit 414 to a medium power modulation mode I_{COR} transconductance value, $Gm_{ICOR_MEDIUM_POWER}$.

[001230] For example, in the case where the active noise reduction circuit is an open loop ripple compensation assist circuit, the controller 50 may configure the open loop ripple compensation assist circuit 414 to generate and apply a high frequency ripple compensation current 416, I_{COR}, to the modulated power supply output 876 to reduce the noise present in the receive channel of a band of operation due to high frequency ripple current. The controller 50 may reduce the programmable I_{COR} transconductance of the open loop ripple compensation assist circuit 414 as the expected output power of the radio frequency power amplifier 869 decreases to reduce the degree of active noise reduction.

[001231] The controller 50 may configure the operation of the V_{OFFSET} loop circuit 41. (Step 1518). Based on the battery voltage, V_{BAT}, the expected envelope characteristics of the modulated radio frequency input signal to be transmitted, and the minimum offset voltage, V_{OFFSET_MIN}, the controller 50 may configure the target offset voltage parameter, V_{OFFSET_TARGET}, of the V_{OFFSET} loop circuit 41. In addition, the controller 50 may configure the V_{OFFSET} loop circuit 41 to operate a pre-charge mode of operation as a function of the target offset voltage parameter, V_{OFFSET_TARGET}, and the offset voltage, V_{OFFSET}, across the coupling capacitor 18A.

[001232] The controller 50 may configure the operation of the feedback delay compensation circuit 852 as a function of the expected output power of the radio frequency power amplifier 869. (Step 1520). As an example, the controller 50 may enable the feedback delay compensation circuit 852 and set the apparent gain of the feedback delay compensation circuit 852 as a function of the expected output power. For example, as the expected output power of the radio frequency power amplifier 869 decreases, the controller 50 may decrease the apparent gain the feedback delay compensation circuit 852. After the power management system 870 is configured to operate in the medium power modulation, the data transmission is commenced. (Step 1522).

[001233] Figure 45 depicts the method 1600 for configuring the operation of the pseudo-envelope tracking modulated power supply system 868 to operate in a low power modulation mode based on a determination that the expected output

power to be generated by the radio frequency power amplifier 869 during a data transmission is less than the high power modulation mode threshold but greater than a low power modulation mode threshold. The method 1600 is described with continuing reference to the pseudo-envelope tracking modulated power supply system 868 depicted in Figures 40A, 40B, 40C, 41, 43A-B, and 44A-B. For the sake of convenience, and not by way of limitation, description of the method 1600 may refer to the controller 50. However, as discussed above, a digital base band processing portion of the transceiver/communication device and/or a combination of hardware and firmware associated with the power management system 870 may likewise operate in conjunction with the controller 50. In addition, the operations of controller 50 may be incorporated into the hardware and/or firmware of various components or portions of a transceiver/ communication device.

[001234] The controller 50 may configure the power management system to operate in a low power modulation mode in response to a determination that the expected output power of the radio frequency power amplifier 869 is less than the low power modulation mode threshold. (Step 1602). The controller 50 may disable the parallel amplifier 928 and configure the parallel amplifier output 928C to be a high impedance load with respect to the parallel amplifier circuit output 874A. (Step 1604). In addition, the controller 50 may enable the parallel amplifier output bypass switch 936 to be in a closed state. (Step 1606). As a result, the negative terminal of the coupling capacitor 18A may short to ground.

[001235] The controller 50 may disable the switch mode power supply converter 872. For example, the switching circuit 884 may be disabled and configured to provide a high impedance path to ground at the switching voltage output 26. In addition, in some embodiments, the multi-level charge pump 882 may be disabled and configured to provide a high impedance path to ground at the charge pump output 64. In some alternative embodiments, as discussed above, the multi-level charge pump 882 may be configured to provide a high impedance path to ground at the charge pump output 64, but may be configured to generate a charge pump output voltage, V_{CP_OUTPUT}, described with respect to

Figure 7D, or generate the parallel amplifier supply voltage, $V_{SUPPLY_PARA_AMP}$, with the internal charge pump node parallel amplifier supply 294, described with respect to Figures 7B-C. (Step 1608). The controller 50 may also disable the active noise reduction circuit while the power management system 870 is configured to operate in low power modulation mode. For example, the controller 50 may disable the open loop ripple compensation assist circuit 414. In addition, the controller 50 may disable the V_{OFFSET} loop circuit 41 and the feedback delay compensation circuit 852 while in the low power modulation mode. (Step 1610). The controller 50 may obtain an estimate of the battery voltage, V_{BAT}, from the battery level sense circuit 264. In addition, the controller 50 may obtain or determine the maximum expected power amplifier supply voltage, V_{CC_MAX}, based on an envelope characteristic of the modulated radio frequency signal to be transmitted by the radio frequency power amplifier 869. Based on the maximum expected power amplifier supply voltage, V_{CC_MAX}, the battery voltage, V_{BAT}, and the maximum headroom voltage of the linear regulator 930, LDO, the controller 50 may select a minimum value of the operational ratio of the μC charge pump, μBB_{RATIO}, to permit the linear regulator 930, LDO, to generate the maximum expected power amplifier supply voltage, V_{CC_MAX}, during the data transmission. For example, the μC charge pump circuit 262 may typically operate in one of the 1/4 x V_{BAT} mode, 1/3 x V_{BAT} mode, or the 1/2 x V_{BAT} mode when the power management system 870 is configured to operate in the low power modulation mode. (Step 1612).

[001236] In some alternative embodiments, not depicted in Figure 40C, the linear regulator 930, LDO, may also switchably provide a supply voltage to the CMOS logic supply input 869C. In this case, the controller 50 may further determine whether the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage. Based on a determination that the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage, the controller 50 may determine a minimum value of the operational ratio of the μC charge pump, μBB_{RATIO}, necessary to generate a second linear regulator output voltage, V_{LDO2}, at least equal to the minimum CMOS logic supply voltage. Thereafter, the

controller 50 may configure the μC charge pump circuit 262 to generate a μC charge pump output voltage, $V_{\mu C_OUT}$, having the lowest voltage level that is sufficient to generate the maximum expected power amplifier supply voltage, V_{CC_MAX}, and at least equals the minimum CMOS logic supply voltage plus the headroom voltage of the linear regulator 930. In some embodiments, the controller 50 may configure the μC charge pump circuit 262 to provide a second linear regulator output voltage, V_{LDO2}, to provide at least a second linear regulator output voltage, V_{LDO2}, at least equal to the minimum CMOS logic supply voltage.

[001237] The controller 50 may select the linear regulator mode of operation based on the tracking mode of the power management system 870. (Step 1614). In response to an indication that the to be transmitted modulated radio frequency input signal will produce a substantially fixed DC reference voltage, the power management system 870 may be configured for a no tracking mode of operation. In the no tracking mode of operation, the power management system may configure the differential filter 924 to provide no frequency response compensation. (Step 1616). Thereafter, the data transmission commences. (Step 1622). However, based on a determination that the tracking mode of the power management system 870 is set to operate in a slow tracking mode, the digital base band processing portion of a transceiver/communication device may be configured to provide a differential V_{RAMP} signal that provides for a slow tracking mode (Step 1618). The controller may configure the differential filter 924 to provide a low amount of frequency response compensation or correction based on the expected output power of the radio frequency power amplifier 869. (Step 1620). Thereafter, the data transmission commences. (Step 1622).

[001238] Figures 46A-B depict an embodiment of a pseudo-envelope tracking modulated power supply system 868A that includes a radio frequency power amplifier 869'. The radio frequency power amplifier 869' may be powered by various embodiments of a power management system 870A. The various embodiments of the pseudo-envelope tracking modulated power supply system 868A and the power management system 870A may be similar to the

respective embodiments of the pseudo-envelope tracking modulated power supply system 868 and the power management system 870, which are depicted in Figures 40A-B and Figure 41. An example embodiment of a number of power level modulation modes of the power management system 870 are depicted in Figures 42, 43-43B, 44A-B, and 45.

[001239] The power management system 870A may include the switch mode power supply converter 872 and a parallel amplifier circuit 874'. In addition to the parallel amplifier circuit output 874A, the first linear regulator output 874B, LDO_1 OUTPUT, and the second linear regulator output 874D, LDO_2 OUTPUT, the embodiments of a pseudo-envelope tracking modulated power supply system 868A may include a radio frequency power amplifier 869'. The power management system 870A may be configured to power the radio frequency power amplifier 869' as a function of the expected output power to be generated by the radio frequency power amplifier 869' in a data transmission of a modulated radio frequency input signal provided to the radio frequency power amplifier for transmission. Figure 47, Figures 48A-B, Figures 49A-B, Figures 50A-B, and Figure 51 depict embodiments of a number of power level modulation modes of the power management system 870A.

[001240] Some embodiments of the power management system 870A may include a parallel amplifier circuit 874'. Similar to the parallel amplifier circuit 874, depicted in Figure 40C, the parallel amplifier circuit 874' may include the parallel amplifier circuit output 874A, the first linear regulator output 874B, LDO_1 OUTPUT, and the second linear regulator output 874D, LDO_2 OUTPUT, the switch mode power supply converter control output 874E, and the modulated power supply voltage feedback input 874F. In addition, the parallel amplifier circuit 874' may further include a V_{CMOS} output 874C configured provide a CMOS logic supply voltage 878C, V_{CMOS}, to the CMOS logic supply input 869C of the radio frequency power amplifier 869' as a function of the battery voltage, V_{BAT}.

[001241] The parallel amplifier circuit output 874A may be in communication with the modulated power supply output 876. In some embodiments, the parallel amplifier circuit output 874A may be coupled to the modulated power supply

output 876 via the coupling capacitor 18A. The first linear regulator output 874B, LDO_1 OUTPUT, may be in communication with the modulated power supply output 876. The V_{CMOS} OUTPUT, 874C may be in communication with the CMOS logic supply input 869C of the radio frequency power amplifier 869'. The second linear regulator output 874D, LDO_2 OUTPUT, may be in communication with the driver supply voltage input 869D of the radio frequency power amplifier 869'. The switch mode power supply converter control output 874E may be in communication with the switch mode power supply converter 872, and configured to provide a switch mode power supply feedback signal 40A to the switcher control circuit 880. The modulated power supply voltage feedback input 874F may be in communication with the modulated power supply output 876. In some embodiments, the parallel amplifier circuit 874' may also provide the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to the switch mode power supply converter 872 as a function of the power level modulation mode to govern the operation of the switch mode power supply converter 872.

[001242] Some embodiments of the power management system 870A may be configured to operate in a number of power level modulation modes. In addition, in some embodiments, the power management system 870A may be configured to operate based on various sets of the number of power level modulation. For example, in some embodiments, the power management system 870A may be configured to operate in a set of power level modulation modes that includes a high power modulation mode, a medium power modulation mode, a medium power average power tracking modulation mode, and a low power average power tracking modulation mode, depicted in Figure 47, Figure 48A-B, Figure 49A-B, Figure 50A-B, and Figure 51. In addition, the power management system 870 may be configured to operate in a set of power level modulation modes that include a high power modulation mode, a medium power modulation mode, and a low power average power tracking modulation mode that may be similar to the operation of the power management system 870 and the low power modulation mode, described with respect to the Figures 40A-C, 41, 42, and 45.

[001243] In the high power modulation mode and the medium power modulation, the power management system 870A may configure the parallel amplifier circuit 874' to generate a parallel amplifier output current, I_{PAWA_OUT}, from the parallel amplifier circuit output 874A to regulate the modulated power supply voltage, V_{CC}. The parallel amplifier output current, I_{PAWA_OUT}, may be applied to the modulated power supply output 876 to regulate generation of the modulated power supply voltage, V_{CC}, as a function of the differential V_{RAMP} signal. The modulated power supply voltage, V_{CC}, may be provided to the collector voltage supply input 869A to power the final output stage 869G of the radio frequency power amplifier 869'. In the medium power average power tracking modulation mode and the low power average power tracking modulation mode, the power management system 870A may configure the parallel amplifier circuit 874' to provide a low impedance path to ground at the parallel amplifier circuit output 874A in order to provide additional bypass capacitance for the modulated power supply output 876. For example, configuring the parallel amplifier circuit output 874A to provide a low impedance path to ground effectively puts the coupling capacitor 18A in parallel with the bypass capacitor 19.

[001244] In the high power modulation mode and the medium power modulation mode, the power management system 870A may configure the parallel amplifier circuit 874' to apply the parallel amplifier output current, I_{PAWA_OUT} to the modulated power supply output 876.

[001245] In some embodiments, in the high power modulation mode, the medium power modulation mode, and the medium power average power modulation mode, the power management system may configure the first linear regulator output 874B to provide a high impedance path to ground. In the low power average power tracking modulation mode, the power management system 870A may configure the parallel amplifier circuit 874' to generate a first linear regulator output current 878B, I_{LDO}, at the first linear regulator output 874B, LDO_1 OUTPUT, a function of the differential V_{RAMP} signal. The first linear regulator output current 878B, I_{LDO}, may be applied to the modulated power

supply output 876 to generate the modulated power supply voltage, V_{CC}. The modulated power supply voltage, V_{CC}, generated by the first linear regulator output current 878B, I_{LDO}, may be provided to the collector voltage supply input 869A to power the final output stage 869G of the radio frequency power amplifier 869'.

[001246] In each of the high power modulation mode, the medium power modulation mode, the medium power average power tracking modulation mode and the low power average power tracking modulationmode , the power management system 870A may configure the parallel amplifier circuit 874' generate a CMOS logic circuit supply voltage, V_{CMOS}, at the V_{CMOS} OUTPUT, 874C as a function of the battery voltage, V_{BAT}.

[001247] In some embodiments, the parallel amplifier circuit 874' may selectively provide a CMOS logic circuit supply voltage, V_{CMOS}, substantially equal to the battery voltage, V_{BAT}, based on a determination that the battery voltage, V_{BAT}, is at least equal to a minimum CMOS logic supply voltage threshold. Based on a determination that the battery voltage, V_{BAT}, is near or below the minimum CMOS logic supply voltage threshold, the parallel amplifier circuit 874' may provide a CMOS logic circuit supply voltage, V_{CMOS}, at least equal to the minimum CMOS logic supply voltage as a function of the battery voltage, V_{BAT}, and the minimum CMOS logic supply voltage threshold. In some alternative embodiments, the power management system 870A may configure the parallel amplifier circuit 874' to generate the CMOS logic circuit supply voltage, V_{CMOS}, at least equal to the minimum CMOS logic supply voltage only based on the determination that the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage threshold.

[001248] In the high power modulation mode, the medium power modulation mode, the medium power average power tracking modulation mode, and the low power modulation mode, the power management system 870A may configure the parallel amplifier circuit 874' to generate a second linear regulator output voltage, V_{LDO2}, at the second linear regulator output 874D, LDO_2 OUTPUT. The second linear regulator output voltage, V_{LDO2}, may be provided to the driver

supply voltage input 869D of the radio frequency power amplifier 869'. In some embodiments, the power management system 870A may configure the parallel amplifier circuit 874' to generate the second linear regulator output voltage, V_{LDO2}, as a function of the differential V_{RAMP} signal in the medium power average power tracking modulation mode and the low power average power tracking mode.

[001249] In the high power modulation mode and the medium power modulation mode, the power management system 870A may configure the parallel amplifier circuit 874' to generate the switch mode power supply feedback signal 40A to govern the generation of the switching voltage, V_{SW}, as a function of the parallel amplifier circuit output current, I_{PAWA_AMP}.

[001250] In the medium power average power tracking modulation mode, the power management system 870A may configure the parallel amplifier circuit 874' to generate the switch mode power supply feedback signal 40A to govern the generation of the switching voltage, V_{SW}, as a function of the differential V_{RAMP} voltage. The switcher control circuit 880 may use the switch mode power supply feedback signal 40A when configured to generate the switching voltage, V_{SW}, in the average power tracking "bang-bang" mode of operation.

[001251] In the embodiments of a pseudo-envelope tracking modulated power supply system 868A that include the coupling capacitor 18A, the power management system 870A may configure the parallel amplifier circuit 874' to generate a threshold offset current, $I_{THRESHOLD_OFFSET}$, to regulate an offset voltage, V_{OFFSET}, across the coupling capacitor 18A when configured to operate in the high power modulation mode and the medium power modulation mode. For some alternative embodiments of the parallel amplifier circuit 874', the power management system 870A may configure the parallel amplifier circuit 874' to generate a threshold offset current, $I_{THRESHOLD_OFFSET}$, to govern generation of the switching voltage, $V_{SW,}$ and regulate the modulated power supply voltage, V_{CC}. In this case, the power management system 870A may configure the parallel amplifier circuit 874' to generate the threshold offset current, $I_{THRESHOLD_OFFSET}$, to govern the generation of the switching voltage, V_{SW}, as a function of the

differential V_{RAMP} voltage. In some embodiments, the switcher control circuit 880 may use the threshold offset current, $I_{THRESHOLD_OFFSET}$, when operating in the average power tracking "buck-boost" mode of operation to generate the switching voltage, V_{SW}, at the switching voltage output. In some embodiments, the switcher control circuit 880 may also use the threshold offset current, $I_{THRESHOLD_OFFSET}$, to generate the switching voltage, V_{SW}, when configured to operate in the average power tracking "buck-buck" mode of operation.

[001252] Figure 46B depicts a parallel amplifier circuit 874' that is similar in form and function to the parallel amplifier circuit 874 depicted in Figure 40C. However, the parallel amplifier circuit 874' may further include a low power differential to single-ended converter 942, an average power tracking controller circuit 944, a first parallel amplifier feedback impedance 946 having a first impedance, Z_1, and a second parallel amplifier feedback impedance 948 having a second impedance, Z_2.

[001253] Figure 46B depicts that the low power differential to single-ended converter 942 including a non-inverting input that is configured to receive the differential V_{RAMP} signal. Operationally, the non-inverted V_{RAMP} signal component, V_{RAMP+}, is provided to the non-inverting input 942A and the inverted V_{RAMP} signal component, V_{RAMP-}, is provided to the inverting input 942B of the low power differential to single ended converter 942. Based on the difference between the non-inverting input 942A and the inverting input 942B, the low power differential to single ended converter 942 generates the V_{RAMP} signal at the single ended output 942C. In the medium power average power tracking mode and the low power average power tracking mode, some embodiments of the power management system 870A may disable the differential filter 924 and enable the low power differential to single-ended converter 942 to generate the V_{RAMP} signal as a function of the differential V_{RAMP} signal.

[001254] The average power tracking controller circuit 944 may include a non-inverting input 944A configured to receive the V_{RAMP} signal from the single ended output 942C, an inverting input 944B configured to receive the modulated power supply voltage, V_{CC}, and an average power tracking control signal output 944C

configured to generate an average power tracking control signal 966. The average power tracking controller circuit 944 may be configured to generate the average power tracking control signal at the average power tracking controller signal output 944C as a function of a difference between the V_{RAMP} signal and the modulated power supply voltage, V_{CC}.

[001255] For example, some embodiments of the average power tracking controller circuit 944 may include a front-end stage (not depicted) that is similar in form and/or function to a differential amplifier. As an example, in some embodiments, the average power tracking controller circuit 994 may use a front-end stage similar to the parallel amplifier front-end stage. The average power tracking controller circuit 944 may generate a current substantially equal to the product of the difference between the V_{RAMP} signal and the modulated power supply voltage, V_{CC}, multiplied by a programmable average power tracking transconductance, Gm_{APT}, as the average power tracking control signal 966. For example, in some embodiments, the average power tracking control signal 966 may be a current substantially equal to $Gm_{APT} \times (V_{RAMP} - V_{CC})$.

[001256] Accordingly, in some embodiments, the magnitude of the average power tracking control signal 966 may represent a difference between a target output voltage for the modulated power supply voltage, V_{CC}, provided by the V_{RAMP} signal and the modulated power supply voltage, V_{CC}, at the modulated power supply output 876. The average power tracking control signal 966 may provide an indication of an instantaneous error voltage between a target voltage for the modulated power supply output 876 and the modulated power supply voltage, V_{CC}.

[001257] In the case where the power management system 870A is configured to operate in an average power tracking modulation mode, the average power tracking control signal 966 may be provided to the switcher control circuit 880, depicted in Figure 40B, as an error signal to control the generation of the switching voltage, V_{SW}, at the switching voltage output 26. In the case where the switcher control circuit 880 uses the average power tracking control signal 966 as a composite control signal while operating in an average power tracking mode,

the controller 50 may configure a magnitude of the programmable average power tracking transconductance, Gm_{APT}, to adjust the frequency of operation of the switch mode power supply converter 872 in the average power tracking modes of operation. In addition, the controller 50 may also adjust the programmable average power tracking transconductance, Gm_{APT}, as a function of a ripple voltage at the modulated power supply output 876.

[001258] For example, in some embodiments, the controller 50 may increase the magnitude of the programmable average power tracking transconductance, Gm_{APT}, to increase a loop gain of the switch mode power supply converter 872 when operating in the average power tracking mode in order to reduce the ripple voltage at the modulated power supply output 876.

[001259] As another example, in some embodiments, the controller 50 may increase the magnitude of the programmable average power tracking transconductance, Gm_{APT}, as a function of the average expected output power, P_{OUT_AVE}. For example, as the average expected output power, P_{OUT_AVE}, increases, the controller 50 may increase the magnitude of the programmable average power tracking transconductance, Gm_{APT}, in order to minimize the ripple voltage generated at the modulated power supply output 876. In other words, as the load placed on the switch mode power supply converter 872 is increased, the loop gain may be increased to minimize the ripple voltage at the modulated power supply output 876. Similarly, the controller 50 may decrease the magnitude of the programmable average power tracking transconductance, Gm_{APT}, as the average expected power, P_{OUT_AVE}, decreases to ensure stablility of the switch mode power supply converter 872 and minimize the ripple voltage generated at the modulated power supply output 876.

[001260] In some embodiments, the power management system 870A may further adjust the programmable average power tracking transconductance, Gm_{APT}, as a function of the expected output power to be generated by the radio frequency power amplifier 869' to adjust the gain of the control loop of the switch mode power supply converter 872. In addition, the average power tracking controller circuit 944 may include a number of expected output power thresholds

that may be used to adjust the programmable average power tracking transconductance, Gm_{APT}, as a function of the expected output power of the radio frequency power amplifier 869'.

[001261] For example, as the expected output power of the radio frequency power amplifier 869' increases, the power management system 870A may increase the magnitude of the programmable average power tracking transconductance, Gm_{APT}, to increase switching frequency of the switch mode power supply converter 872. As a result, the modulated power supply output 876 may provide additional current to the collector voltage supply input 869A of the radio frequency power amplifier 869' while maintaining a target voltage for the modulated power supply voltage, V_{CC}, determined by the differential V_{RAMP} signal.

[001262] In some embodiments, when the expected output power of the radio frequency power amplifier 869' decreases below an output power threshold level, the power management system 870A may decrease the magnitude of the programmable average power tracking transconductance, Gm_{APT}, to decrease the gain of the control system and ensure stability of the switch mode power supply converter 872 or reduce the switching frequency of the switch mode power supply converter 872. In some embodiments, the power management system 870A may increase the programmable average power tracking transconductance, Gm_{APT}, for an initial period of time to pre-charge the modulated power supply voltage, V_{CC}, to a desired level and then decrease the programmable average power tracking transconductance, Gm_{APT}, to a normal operational level to ensure system stability.

[001263] The power management system 870A may enable the average power tracking controller circuit 944 when the expected output power of the radio frequency power amplifier 869' is less than the medium power modulation mode threshold. In the case where the expected output power of the radio frequency power amplifier 869' is least equal to the medium power modulation mode threshold, the low power differential to single ended converter 942 and the average power tracking controller circuit 944 may be disabled. In addition, the

power management system 870A may disable the average power tracking controller circuit 944 when the switch mode power supply converter 872 is disabled. For example, in some embodiments of the low power average power tracking modulation mode, the power management system 870A may disable the switch mode power supply converter and the average power tracking controller circuit 944.

[001264] The first parallel amplifier feedback impedance 946, Z_1, may be coupled between the inverting input 928B of the parallel amplifier 928 and the modulated power supply voltage feedback input 874F. The second parallel amplifier feedback impedance 948, Z_2, may be coupled between the inverting input 928B of the parallel amplifier 928 and ground. The impedance of the first parallel amplifier feedback impedance 946, Z_1, and the impedance of the second parallel feedback impedance 948, Z_2, may be programmable impedances. For example, the first parallel amplifier feedback impedance 946, Z_1, may include a programmable resistor array, a programmable capacitor array, and/or a combination thereof. In addition, the impedance of the second parallel feedback impedance 948, Z_2, may include a programmable resistor array, a programmable capacitor array, and/or a combination thereof. The controller 50 may be configured to adjust the programmable impedances of the first parallel amplifier feedback impedance 946, Z_1, and the second parallel feedback impedance 948, Z_2, to adjust the gain and the frequency response of the parallel amplifier 928. For example, in some embodiments, the controller 50 may adjust the first parallel amplifier feedback impedance 946, Z_1, and the second parallel feedback impedance 948, Z_2, to configure the frequency response or the gain of the parallel amplifier 928 as a function of the expected output power of the radio frequency power amplifier 869'. For example, the controller 50 may configure the first parallel amplifier feedback impedance 946, Z_1, and the second parallel feedback impedance 948, Z_2, to provide additional frequency compensation based on a determination to configure the power management system 870A is operating in a high power modulation mode. Alternatively, the controller 50 may configure the first parallel amplifier feedback impedance 946, Z_1, and the second

parallel feedback impedance 948, Z_2, to provide less frequency compensation based on a determination to configure the power management system 870A in the medium power modulation mode of operation.

[001265] The parallel amplifier circuit 874' may include a first linear regulator 950, LDO_1, configured to provide the linear regulator output current 878B, I_{LDO}, to the first linear regulator output 874B, LDO_1 OUTPUT, and a second linear regulator 952, LDO_2, configured to generate the second linear regulator output voltage, V_{LDO2}, at the second linear regulator output 874D, LDO_2 OUTPUT. In some embodiments, the first linear regulator 950, LDO_1, and the second linear regulator 952, LDO_2, may be low drop out voltage linear regulators. In addition, the parallel amplifier circuit 874' may further include a (DAC) programmable digital to analog converter 954, and a second signal control multiplexer 956 configured to provide a second linear regulator control voltage, $V_{CONTROL_LDO2}$, to the second linear regulator 952, LDO_2.

[001266] The first linear regulator 950, LDO_1, may include a non-inverting input 950A configured to receive the V_{RAMP} signal, an inverting input 950B coupled to the first regular regulator output 950C, which is configured to provide a first linear regulator output, LDO_1 Output, to the modulated power supply output 876. The first linear regulator 950, LDO_1, further includes a power supply input 950D configured to receive the μC charge pump output voltage, $V_{\mu C_OUT}$, from the μC charge pump circuit 262. The μC charge pump output voltage, $V_{\mu C_OUT}$, is also provided to a noise filter 958. The noise filter 958 may be a passive low pass filter configured to remove switching noise on the μC charge pump output voltage, $V_{\mu C_OUT}$.

[001267] The second signal control multiplexer 956 may include a first input 956A configured to receive the V_{RAMP} signal, a second input 956B configured to receive a programmable reference voltage from a programmable digital to analog converter 954, and a multiplexer output 954C configured to provide a second linear regulator control voltage, $V_{CONTROL_LDO2}$, to the non-inverting input 952A of a second linear regulator 952, LDO_2. In the high power modulation mode and the medium power modulation mode, the power

management system 870A may configure the programmable digital to analog converter (DAC) 954 to provide the programmable reference voltage as a target voltage to be generated by the second linear regulator 952, LDO_2. The second signal control multiplexer 956 may be configured to provide the programmable reference voltage as the second linear regulator control voltage, $V_{CONTROL_LDO2}$, to the non-inverting input 952A of a second linear regulator 952, LDO_2. In the medium power average power tracking modulation mode, the low power modulation mode modulation mode, and the low power modulation mode, the power management system 870A may configure the second signal control multiplexer 956 to provide the V_{RAMP} signal as the second linear regulator control voltage, $V_{CONTROL_LDO2}$, to the non-inverting input 952A of a second linear regulator 952, LDO_2.

[001268] The second linear regulator 952 further includes an inverting input 952B coupled to the second linear regulator output 952C of the second linear regulator 952, LDO_2. The second linear regulator 952, LDO_2 may be configured to provide a second linear regulator output, LDO_2 OUTPUT, to the radio frequency power amplifier 869' as a function of the battery voltage, V_{BAT}. The controller 50 may configure the programmable digital to analog converter (DAC) 954 to provide the target voltage to be generated by the second linear regulator 952, LDO_2. In response to receipt of the second linear regulator control voltage, $V_{CONTROL_LDO2}$, the second linear regulator 952, LDO_2, provides a second linear regulator output voltage, V_{LDO2}, to the driver supply voltage input 869D to power the driver 869F.

[001269] The parallel amplifier circuit 874' may further include a noise filter 958 including an input terminal configured to receive the μC charge pump output voltage, $V_{\mu C_OUT}$, and an output terminal configured to provide a filtered μC charge pump output voltage, $V_{\mu C_FILTERED}$, to a first input terminal 960A of a first power supply selection switch 960. In some embodiments, the noise filter 958 includes a PI network filter. In some embodiments, the PI network filter may be a PI LC filter or a PI CLC Filter. In some alternative embodiments, the noise filter 958 may include one or more bypass capacitors coupled between the input

terminal of the noise filter 958 and ground, one or more bypass capacitor coupled between the output terminal of the noise filter 958 and ground, and the inductor or inductive having a first terminal in communication with the input terminal of the noise filter 958 and a second terminal in communication with the output terminal of the noise filter 958. Some embodiments of the noise filter 958 may be implemented in an integrated circuit (IC) while other portions of the noise filter 958 are external to the integrated circuit. For example, the noise filter 958 may include one or more of a discrete inductive component and one or more of a discrete capacitor that are external to the integrated circuit and couple to or between the input terminal and the output terminal of the noise filter 958.

[001270] The first power supply selection switch 960 may include a second input terminal 960B configured to receive the battery voltage, V_{BAT}, and an output terminal 960C configured to provide a selected supply voltage, $V_{DD_SELECTED}$, to the second linear regulator power supply input 952D.

[001271] Depending on the minimum driver supply voltage, the power supply selection switch 960 may be configured to provide either the filtered µC charge pump output voltage, $V_{\mu C_FILTERED}$, or the battery voltage, V_{BAT}, to the second linear regulator power supply input 952D. For example, as described above, the controller 50 may determine the minimum driver supply voltage threshold as a function of the expected output power to be generated by the radio frequency power amplifier 869'. If the minimum driver supply voltage threshold is more than the battery voltage, V_{BAT}, less the headroom of the power supply selection switch 960 and headroom of the second linear regulator 952, LDO_2, the controller 50 configures the power supply selection switch 960 to provide the filtered µC charge pump output voltage, $V_{\mu C_FILTERED}$, to the second linear regulator power supply input 952D. In addition, the controller 50 may configure the µC charge pump output voltage, $V_{\mu C_OUT}$, to be at least equal to the headroom of the power supply selection switch 960 and headroom of the second linear regulator 952, LDO_2, plus the minimum driver supply voltage threshold and any voltage drop that occurs in the noise filter 958. However, in the case where the minimum driver supply voltage threshold is less than the battery voltage, V_{BAT}, the

controller 50 may configure the power supply selection switch 960 to provide the lesser of the filtered μC charge pump output voltage, $V_{\mu C_FILTERED}$, and the battery voltage, V_{BAT}, that permits the second linear regulator 952, LDO_2, to provide a second linear regulator output voltage, V_{LDO2}, at least equal to the minimum driver supply voltage threshold to the driver supply voltage input 869D in order to power the driver 869F.

[001272] The parallel amplifier circuit 874' may include an embodiment of the open loop ripple compensation assist circuit 414 as an active noise reduction circuit. In the high power modulation mode and the medium power modulation mode, the open loop ripple compensation assist circuit 414 may generate a high frequency ripple compensation current 416, I_{COR}. The high frequency ripple compensation current 416, I_{COR}, may be applied to the modulated power supply output 876 to reduce the voltage ripple generated at the modulated power supply output 876 by the switching action of switch mode power supply converter 872. In the high power modulation mode, the controller 50 may configure the open loop ripple compensation assist circuit 414 to generate the high frequency ripple compensation current 416, I_{COR}, as a function of a high power modulation mode I_{COR} transconductance value, $Gm_{ICOR_HIGH_POWER}$. In the medium power modulation mode, the controller 50 may configure the open loop ripple compensation assist circuit 414 to generate the high frequency ripple compensation current 416, I_{COR}, as a function of a medium power modulation mode I_{COR} transconductance value, $Gm_{ICOR_MEDIUM_POWER}$. In the high power modulation mode, the controller 50 may set the programmable I_{COR} transconductance, Gm_{ICOR}, to the high power modulation mode I_{COR} transconductance value, $Gm_{ICOR_HIGH_POWER}$. The open loop ripple compensation assist circuit 414 may generate the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}, that is proportional to the high frequency ripple compensation current 416, I_{COR}.

[001273] In contrast, the controller 50 may disable the open loop ripple compensation assist circuit 414 in the low power modulation mode, the medium power average power tracking modulation mode, and the low power average

power tracking modulation mode. Instead, the power management system 870A may depend on the additional decoupling capacitance of the relatively large capacitance value of the coupling capacitor 18A, which is switchably couple between the modulated power supply output 876 and ground in the medium power average power tracking modulation mode and the low power average power tracking modulation mode.

[001274] Also, in some modes of operation in the medium power modulation mode, the power management system 870A may disable all active noise reduction circuits as a function of the expected output power to be generated by the radio frequency power amplifier 869' during a data transmission, a band of operation in which the data transmission will take place, a bandwidth of the band of operation in which the data transmission will take place, the of modulation used in the data transmission, the peak-to-average ratio characteristic of the waveform to be generated, and/or some combination thereof that provides an indication that the electronic noise generated at the modulated power supply output 876 is within acceptable limits. For example, the power management system may disable the open loop ripple compensation assist circuit 414 based on a determination that the data transmission does not require active noise reduction as a function of the expected output power to be generated by the radio frequency power amplifier 869'.

[001275] The parallel amplifier circuit 874' may also include a first signal control multiplexer 964 having a first input 964A configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, which is generated by summing the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the scaled high frequency ripple compensation current estimate 418, I_{COR_SENSE}. The first signal control multiplexer 964 also includes a second input configured to receive an average power tracking control signal 966 from the average power tracking controller circuit 944. The first signal control multiplexer 964 also includes a multiplexer output 964C in communication with the switch mode power supply converter control output 874E. The first signal control multiplexer 964 may provide the switch mode power supply feedback

signal 40A to the switch mode power supply converter 872 as a function of the expected output power to be generated by the radio frequency power amplifier 869' in a data transmission.

[001276] For example, in the high power modulation mode and the medium power modulation mode, the first signal control multiplexer 964 may be configured to provide the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, as the switch mode power supply feedback signal 40A. In the medium power average power tracking mode, first signal control multiplexer may provide the average power tracking control signal 966 as the switch mode power supply feedback signal 40A.

[001277] The power management system 870A may configure the parallel amplifier circuit 874' to use the V_{RAMP} single at the single ended output 942C or the control signal 926 as a function of the expected output power to be generated by the radio frequency power amplifier 869' during the data transmission. As an example, in the medium power average power tracking modulation mode and the low power average power tracking modulation mode, some embodiments of the power management system 870A may disabled the differential filter 924 and enable the differential to single ended converter 942 to reduce the battery current, I_{BAT}, drawn from the battery 20. In the high power modulation mode and the medium power modulation mode, the power management system 870A may enable the differential filter 924 and disable the differential to single ended converter 942 to provide a desired level of frequency response compensation or correction to the differential V_{RAMP} signal. The differential filter 924 may generate the control signal 926 that is to the non-inverting input of the parallel amplifier 928 as a function of the expected output power to be generated by the radio frequency power amplifier 869' during a data transmission. The differential filter 924 may provide a compensated V_{RAMP} signal to the parallel amplifier 928 as the control signal 926 to compensate for the non-ideal output impedance of the parallel amplifier 928 and the parasitic impedances associated with the modulated power supply output 876 and the radio frequency power amplifier 869'.

[001278] In the high power modulation mode, the differential filter 924 may be configured to provide a maximum level of frequency response compensation or correction. In the medium power modulation mode, the differential filter 924 may be configured to provide a medium level of frequency response compensation or correction. In some embodiments of the medium power average power tracking modulation mode and the low power average power tracking mode, the power management system 870A may disable the differential filter 924.

[001279] As an example, in the high power envelope power tracking modulation mode, the power management system 870A may configure to differential filter 924 to apply maximum peaking to the differential V_{RAMP} signal to generate the control signal 926. Alternatively, in the medimum power envelope tracking power modulation mode, the power management system 870A may configure the differential filter 924 to apply a medium level peaking to the differential $_{VRAMP}$ signal to generate the control signal 926. In other words, based on a determination that the expected output power of the radio frequency power amplifier 869' is less than the high power modulation mode threshold, the power management system 870A may configure the differential filter 924 to provide less frequency response compensation as a function of the expected output power of the radio frequency power amplifier 869'.

[001280] The parallel amplifier circuit 874' further includes a first signal control multiplexer 964. The first signal control multiplexer 964 may be configured to receive the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, at a first input 964A and the average power tracking controller signal 966 at a second input 964B. The controller 50 configures the first signal control multiplexer 964 to provide the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, to the switch mode power supply converter 872 as a switch mode power supply feedback signal 40A when the expected output power of the radio frequency power amplifier 869' is greater than the medium power modulation mode threshold. Otherwise, the controller 50 configures the first signal control multiplexer 964 to provide the average power tracking control signal 966 to the

switch mode power supply converter 872 as the switch mode power supply control signal.

[001281] In the medium power average power tracking modulation mode, the controller 50 disables the parallel amplifier 928, the feedback delay compensation circuit 852, and the V_{OFFSET} loop circuit 41. In addition, as a non-limiting example, the controller 50 also disables any active noise reduction circuit of the parallel amplifier circuit 874'. For example, as depicted in Figure 46B, the controller 50 may disable the open loop ripple compensation assist circuit 414. In addition, the switch mode power supply feedback signal 40A is provided by the average power tracking controller circuit 944. Thus, the switcher control circuit 880 may be configured to operate in a manner similar to the first mode of operation depicted in Figure 5D, where the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, is substantially equal to the switch mode power supply feedback signal 40A. Referring to Figure 5A, Figure 40B, and Figures 46A-B, the controller 50 may configure the switcher control circuit 880 to toggle between the first boost output mode 192A and the shunt output mode 188A to generate a boosted switching voltage and a bucked switching voltage as a function of the compensated parallel amplifier circuit output current estimate, $I_{PAWA_OUT_EST}$, where $I_{PAWA_OUT_EST}$ is the substantially equal to the average power tracking control signal 966.

[001282] The first power supply selection switch 960 may provide either the battery voltage, V_{BAT}, or the µC charge pump output voltage, $V_{\mu C_FILTERED}$, the second linear regulator power supply input 952D. An optional second power supply selection switch 962 may be configured to provide either the battery voltage, V_{BAT}, or the µC charge pump output voltage, $V_{\mu C_OUT}$, to the V_{CMOS} Output, which is configured to provide a CMOS logic supply voltage 878C, V_{CMOS}, to the CMOS logic supply input 869C as a function of the battery voltage, V_{BAT}. For example, in some embodiments, the controller 50 obtains a measurement of the battery voltage, V_{BAT}, from the battery level sense circuit 264. The controller 50 compares the measured voltage level of the battery 20 to the CMOS logic supply voltage threshold. Based on a

determination that the battery voltage, V_{BAT}, is less than the CMOS logic supply voltage threshold, the controller 50 configures the second supply selection switch 962 to provide the μC charge pump output voltage, $V_{\mu C_OUT}$, to the CMOS logic supply voltage 878C, V_{CMOS}. In addition, the controller 50 configures the μC charge pump circuit 262 to generate a μC charge pump output voltage, $V_{\mu C_OUT}$, at least equal to the minimum CMOS logic circuit supply plus any voltage loss across the supply selection switch 962. In addition,

[001283] Similar to the power management system 870, depicted in Figures 40A-C, Figures 46A-B depict the power management system 870A to operate in various radio frequency output power level modulation modes. For example, some embodiments of the power management system 870A may be configured by the controller 50 to operate in a high power modulation mode, a medium power modulation mode, a medium power average power tracking modulation mode, a lower power average power tracking modulation mode, and/or some combination thereof.

[001284] Returning to the description of Figure 46B, while operating in either the high power modulation mode or the medium power modulation mode, the power management system 870A may be configured to generate the modulated power supply voltage, V_{CC}, as a function of the envelope characteristics of the modulate radio frequency input signal to the radio frequency power amplifier 869'. And other words, the power management system 870A generates the modulated power supply voltage, V_{CC}, by substantially tracking the envelope of the modulate radio frequency input signal to be transmitted is a function of the differential V_{RAMP} signal during a data transmission in a data transmission slot. The power management system 870A may configure the parallel amplifier 928 to regulate the modulated power supply voltage, V_{CC}, based on the compensated V_{RAMP} signal, V_{RAMP_C}, generated by the differential filter 924. In addition, the power management system 870A may configure the switch mode power supply converter 872 to generate the switching voltage, V_{SW}, as a function of the switch mode power supply feedback signal 40A is generated by an embodiment of the parallel amplifier circuit 874', the threshold offset current 42, $I_{THRESHOLD_OFFSET}$,

generated by an embodiment of the V_{OFFSET} loop circuit 41, the differential V_{RAMP} signal, and/or some combination thereof.

[001285] Based on a determination of an expected output power to be generated by the radio frequency power amplifier 869', the controller 50 may configure the power management system 870A to operate in one of the high power modulation mode, the medium power modulation mode, the medium power average power tacking modulation mode, and the low power average power tracking mode. As an example, the controller 50 may configure the power management system 870A to operate in the high power modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' is at least equal to a high power modulation mode threshold. The controller 50 may configure the power management system 870A to operate in the medium power modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' is less than the high power modulation mode threshold and at least equal to a medium power modulation mode threshold. The controller 50 may configure the power management system 870A to operate in a medium power average power tracking modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' is less than the medium power modulation mode threshold and either greater than a low power average power tracking mode threshold or at least equal to a medium power modulation average power tracking mode threshold. The controller 50 may configured the power management system 870A to operate in the low power average power tracking modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' is less than the low power average tracking modulation mode threshold.

[001286] Similar to the power management system 870, depicted in Figures 40A-C, the some embodiments of the power management system 870A may be configured to operate in a tracking mode. For example, in some embodiments, the power management system 870A may be configured to

operate in a no tracking mode of operation. In addition, in some embodiments, the power management system 870A may be configured to operate in a slow tracking mode of operation. While operating in a slow tracking mode, some embodiments of the power management system 870A may provide a minimum amount of frequency response compensation sufficient to compensate for parasitic capacitances and parasitic inductances between the modulated power supply output 876 and the collector voltage supply input 869A of the radio frequency power amplifier 869'. However, while operating in the no tracking mode, the power management system 870A may be configured to provide no frequency response compensation to the differential V_{RAMP} signal or the V_{RAMP} signal generated by the low power differential to single ended converter 942.

[001287] In some embodiments of the high power modulation mode, the power management system 870A may configure the switch mode power supply converter 872 and the parallel amplifier circuit 874' to operate in the pseudo-envelope power tracking mode. In mode, the multi-level charge pump 882 may be enabled and configured to generate either a first boost output voltage substantially equal to 3/2 x V_{BAT} or a second boost output voltage substantially equal to 2 x V_{BAT}. In addition, the power management system 870A may enable the differential filter 942, the feedback delay compensation circuit 852, and an embodiment of an active noise reduction circuit. For example, in some embodiments of the power management system 870A, the active noise reduction circuit may be an open loop ripple compensation assist circuit 414 configured to apply the high frequency ripple compensation current 416, I_{COR}, to the modulated power supply output 876. In addition, the µC charge pump circuit 262 may be configured to provide a µC charge pump output voltage, $V_{\mu C_OUT}$, to the parallel amplifier supply voltage input 928D as a function of the battery voltage, V_{BAT}. In some embodiments, the power management system 870A determine the operational ratio of the µC charge pump, μBB_{RATIO}, based on the battery voltage, V_{BAT}, the minimum CMOS logic supply voltage threshold, and the peak to peak swing of the power amplifier supply voltage, V_{CC_PKPK}. For example, the power management system 870A may obtain a measurement of the battery voltage,

V_{BAT}, from the battery level sense circuit 264. The power management system 870A may compare the measured value of the battery voltage, V_{BAT}, to the minimum CMOS logic voltage supply threshold to determine whether the battery voltage, V_{BAT}, is sufficient to power the CMOS logic 869C of the radio frequency power amplifier 869'. Based on the determination that the battery voltage is less than the minimum CMOS logic voltage supply threshold, a smallest available value of the operational ratios of the μC charge pump, μBB_{RATIO}, sufficient to provide a CMOS logic circuit supply voltage, V_{CMOS}, may be determined. The power management system 870A may also determine a smallest available value of the operational ratios of the μC charge pump, μBB_{RATIO}, that generates a μC charge pump output voltage, $V_{\mu C_OUT}$, sufficient to generate the maximum expected power amplifier supply voltage, V_{CC_MAX}, with the parallel amplifier 928 as a function of the peak to peak swing of the power amplifier supply voltage, V_{CC_PKPK}, the battery voltage, V_{BAT}, and minimum offset voltage, V_{OFFSET_MIN}, to be maintained across the coupling capacitor 18A. Based on the predefined operational ratios of the μC charge pump, the power management system 870A configures the μC charge pump circuit 262 to generate the μC charge pump output voltage, $V_{\mu C_OUT}$, that is sufficient to power the parallel amplifier 928, and provide a CMOS logic supply voltage, V_{CMOS}, that is at least equal to the minimum CMOS logic supply voltage. Based on the μC charge pump output voltage, $V_{\mu C_OUT}$, and the peak to peak swing of the power amplifier supply voltage, V_{CC_PKPK}, the power management system 870A configures the V_{OFFSET} loop circuit 41 to generates a target offset voltage, V_{OFFSET_TARGET}, across the coupling capacitor 18A.

[001288] The clock management circuit 260 may disable the oscillator 270 and generate the μC charge pump clock 276 based on the switching frequency of the switch mode power supply converter 872 in the high power modulation mode, the medium power modulation mode, and the medium power average power tracking modulation mode. In the low power modulation mode and the low power average power tracking mode, the clock management system may enable the oscillator 270 to generate the μC charge pump clock 276.

[001289] In some embodiments of the high power modulation mode and the medium power modulation mode, the power management system 870A may enable the V_{OFFSET} loop circuit 41 to regulate the offset voltage, V_{OFFSET}, between the parallel amplifier circuit output 874A and the modulated power supply output 876. In some embodiments of the medium power average power tracking modulation mode, the low power average power tracking modulation mode, and the low power modulation mode, the power management system 870A may be configured to disable the V_{OFFSET} loop circuit 41. When the V_{OFFSET} loop circuit 41 is enabled, some embodiments of the V_{OFFSET} loop circit 41 may be configured to pre-charge the coupling capacitor 18A prior to commencement of a data transmission for a predetermined time.

[001290] While operating in either the medium power average power tracking modulation mode or the low power average power tracking mode, the power management system 870A may be configured to generate the modulated power supply voltage, V_{CC}, substantially based on a function of the average power generated by the radio frequency power amplifier 869' during a data transmission in a data transmission slot. The power management system 870A may be configured to generate the modulated power supply voltage, V_{CC}, as a function of the V_{RAMP} signal generated by the low power differential to single ended converter 942. In some alternative embodiments, the power management system 870A may be further configured to generate the modulated power supply voltage, V_{CC}, as a function of the V_{RAMP} signal generated by the low power differential to single ended converter 942 and the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, generated by some alternative embodiments of the V_{OFFSET} loop circuit 41.

[001291] For example, and not by way of limitation, in some embodiments of the parallel amplifier circuit 874', the embodiments of the V_{OFFSET} loop circuit 41 may be similar to or include the embodiments of the V_{OFFSET} loop circuits 41, 41A-B, and 41C, which are depicted in Figures 2A-B, Figure 8, Figures 18A-B, and Figure 46D. In addition, some embodiments of the V_{OFFSET} loop circuits 41, 41A, and 41B may be configured to include the features, forms, techniques, circuitry,

interfaces, functions, of the V_{OFFSET} loop circuit 41C, which is depicted in Figure 46D. In this case, some embodiments of the medium power modulation mode may enable the V_{OFFSET} loop circuit 41 to provide a threshold offset signal 42, $I_{THRESHOLD_OFFSET}$. Otherwise, various embodiments of the medium power average power tracking modulation mode, the V_{OFFSET} loop circuit 41 may be disabled.

[001292] In the medium power average power tracking mode, the average power tracking control circuit 944 may be enabled to generated the average power tracking control signal 966 based on a V_{RAMP} signal generated by the low power differential to signal ended conveter 942. In addititon, the power management system 870A may disable the parallel amplifier 928 and the differential filter 924 in order to save energy stored in the battery 20. the power management system 870A may regulate the modulated power supply voltage, Vcc, generated by the switch mode power supply converter 872 as a function of the average power tracking control signal 966.

[001293] In the medium power aveage power tracking modulation mode, the first control signal multiplexer 964 may be configured to provide the average power tracking control signal 966 as the switch mode power supply feedback signal 40A. Otherwise, the first control signal multiplexer 964 may be configured to provide the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST}$, as the switch mode power supply feedback signal 40A.

[001294] As an alternative embodiment, the parallel amplifier 928 may be configured in a similar fashion as the parallel amplifier 2200 depicted in Figure 46C. In this case, the parallel amplifier 928 may be configured to operate in the medium power average power tracking mode to generate a modulation mode feedback signal that is substantially similar or equivalent to the average power tracking control signal 966. For example, the parallel amplifier output 928C may be disabled while the parallel amplifier feedback output 928E is configured to generate the average power tracking control signal as a function of the difference voltage between the V_{RAMP} signal and the modulated power supply

voltage, V_{CC}. In these embodiments, the average power tracking control circuit 944 may be removed.

[001295] Figures 12G-I depict embodiments of a parallel amplifier 35G, a rechargeable parallel amplifier 35H, and a rechargeable parallel amplifier 35I that include a segmented output driver stage configured to generate the parallel amplifier output current, I_{PARA_AMP}. Some embodiments of the segmented output driver stage may include two or more push-pull output stages that are coupled in parallel to form the parallel amplifier output. Each of the two or more push-pull output stages may be independently controlled. Alternatively, in some embodiments, only a subset of the two or more push-pull output stages may be independently controlled based on a segmentation configuration.

[001296] In some embodiments of the parallel amplifier 35G, rechargeable parallel amplifier 35H, and rechargeable parallel amplifier 35I, the segmentation configuration of the two or more push-pull output stages may be based the modulation modes of operation of a power management system. For example, Figures 40A-C and Figures 46A-B depict the power management systems 870 and 870A, which are configured to adjust the segmentation configuration of the parallel amplifier 928 as a function of an expected output power to be generated by the radio frequency power amplifiers 869 and 869', respectively, during a data transmission. For example, in some embodiments of the power management systems 870 and 870A may include one of the several embodiments of pseudo-envelope tracking modulation modes of operation, where each pseudo-envelope tracking modulation mode includes a segmentation configuration for the parallel amplifier 928. For example, some embodiments of the parallel amplifier 928 may include a maximum parallel amplifier output current, I_{PARA_MAX}, and configured to generate a fractional amount of the of the maximum parallel amplifier output current, I_{PARA_MAX}, based on a segmentation configuration. For example, some embodiments of the parallel amplifier 928 may include segmentation configurations to set the output current generation capacity of the parallel amplifier 928 substantially equal to 100%, 75%, 66%, 50%, 33%, 25%, 0%, and/or some combination thereof of the maximum parallel amplifier output

current, I_{PARA_MAX}. In this case, each of the two or more segmented push-pull output stages may be weighted proportionally to support the segmentation configurations of the various embodiments of the parallel amplifier 928.

[001297] Although not depicted in Figures 12G-I, as an example, some embodiments of the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I may each include a first push-pull output stage, a second push-pull output stage, and a third push-pull output stage coupled in parallel to form the parallel amplifier output. In some embodiments of the parallel amplifiers 35G-I, the first push-pull output stage may have twice the current generation capacity of the second push-pull output stage and twice the current carrying capacity of the third push-pull output stage. In this case, the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I may include segmentation configurations of 100%, 75%, 50%, 25%, and 0% (OFF). However, in some embodiments the current generation capacity of each of the first push-pull output stage, the second push-pull output stage, and the third push-pull output stage may be substantially equal to provide segmentation configurations of 100%, 66.6%, 33%, and 0%, (OFF). As another example, similar the embodiment of the operational amplifier 442 depicted in Figure 31A, some embodiments of the parallel amplifiers 35G-I may include a number of binary weighted push-pull output stages coupled in parallel to form a binary weighted output driver stage.

[001298] Similar to some embodiments of the parallel amplifier 35J, depicted in Figure 46C and described below, some embodiments of the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I may further include a feedback output stage configured to generate a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, that is proportional to the parallel amplifier output current, I_{PARA_AMP}. Similar to the previously described embodiments of the operational amplifier 442, depicted in Figures 31A and 32A-C, some embodiments of the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I may include a segmented feedback output stage that is proportionally weighted to match the

proportional weighting of the segmented output stage that forms the parallel amplifier output. In this case, the feedback segmentation configuration of the feedback output stage may be configured to match the segmentation configuration of the segmented output stage of the parallel amplifier output.

[001299] In still other embodiments, the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I may be configured to generate a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, that is scaled proportionally to the maximum parallel amplifier output current, $I_{PARA_AMP_MAX}$. For example, the parallel amplifier output current may be generated by a single push-pull output stage configured to generate a In this case, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, may be weighted or divided as a function of the segmentation configuration of the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I to maintain a desired fractional relationship with the parallel amplifier output current, I_{PARA_AMP}. As another example, in some embodiments, the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, may be provided to a resistor array to generate a feedback voltage. The resistance of the resistor array may be configured to track the segmentation configuration of the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I. For example, the resistor array may include a number of weighted resistors that may be configured to track the segmentation configuration of the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and the parallel amplifier 35I. As an example, the resistor array may include a number of binary weighted resistors that may be switchably coupled in parallel, and configured to track the segmentation configuration of the two or more push-pull output stages of the segmented output driver stage.

[001300] Figure 12G depicts an embodiment of a parallel amplifier 35G that is similar in form and function to the parallel amplifier 35A and the parallel amplifier 35D, depicted in Figures 12A and 12D, respectively. The description of the parallel amplifier 35G will be carried out with continuing reference to the embodiments of the parallel amplifiers 35A and 35D. Because the operation of

the parallel amplifiers 35A and 35D are described above, a description of the in common elements and operations will not be repeated.

[001301] Briefly referring to Figure 12A and Figure 12D, the parallel amplifiers 35A and 35D each include a first output stage 210 configured to source current or sink current to a parallel amplifier output node 218 based on a voltage difference between the parallel amplifier input voltage 204 and the amplifier feedback node 212. The amplifier feedback node 212 is coupled to the power amplifier supply voltage, V_{CC}, which may also be referred to as a modulated power supply voltage, V_{CC}. For example, Figures 40A-C and Figures 46A-B depict a modulated power supply output 876 having a modulated power supply voltage, V_{CC}.

[001302] Returning to Figure 12G, the following description of the parallel amplifier 35G will be carried out with continuing reference to the modulated power supply voltage, V_{CC}, and the modulated power supply output 876, depicted in Figures 40A-C and Figure 46A-B, and the parallel amplifier 35A, depicted in Figure 12A, and the parallel amplifier 35D, depicted in Figure 12D. The parallel amplifier 35G may be operationally similar to the parallel amplifiers 35A and 35D. Similar to the parallel amplifiers 35A and 35D, the parallel amplifier 35G includes a first amplifier 206, AMP_A, configured to generate a first amplifier output voltage, V_A, and second amplifier 208, AMP_B, configured to generate a second amplifier output voltage, V_B. The parallel amplifiers 35A and 35D provide the first amplifier output voltage, V_A, and the second amplifier output voltage, V_B, to the first output stage 210 to source and sink current to the parallel amplifier output node 218 based on the difference between the parallel amplifier input voltage 204 (either V_{RAMP} or V_{RAMP_C}) and the modulated power supply voltage, V_{CC}.

[001303] Figure 12 depicts that some embodiments of the parallel amplifier 35G may divide the first output stage 210 into driver segments to form a segmented parallel amplifier output stage having two or more output stage segments. For example, in some embodiments, the parallel amplifier 35G may include a segemented parallel amplifier output stage including a first segmented output driver stage 970 having two or more output stage segments. As an example, in

some embodiments, the first segmented output driver stage 970 may include a first push-pull output stage 972A and a second push-pull output stage 972B coupled at the parallel amplifier output node 218 to form a parallel amplifier output of the parallel amplifier 35G. In some embodiments, the first push-pull output stage 972A and the second push-pull output stage 972B may be balanced. Alternatively, in some embodiments, the first push-pull output stage 972A and the second push-pull output stage 972B may be binary weighted push-pull output stages.

[001304] The controller 50 may enable the first push-pull output stage 972A and the second push-pull output stage 972B to generate a parallel amplifier output current, I_{PARA_OUT}, as a function of the first amplifier output voltage, V_A, and the second amplifier output voltage, V_B, generated by the first amplifier 206, AMP_A, and the second amplifier 208, AMP_B. The first amplifier 206, AMP_A, and the second amplifier 208, AMP_B, may generate the first amplifier output voltage, V_A, and the second amplifier output voltage, V_B, in response to a voltage difference between the parallel amplifier input voltage 204 appearing at the positive input terminal 206A and the power amplifier supply voltage, V_{CC}.

[001305] The controller 50 may assert the first segment control signal 980A to enable the first push-pull output stage 972A. Similarly, the controller 50 may assert the second segment control signal 980B to enable the second push-pull output stage 972B. The controller 50 may de-assert the first segment control signal 980A to disable the first push-pull output stage 972A, and place the first push-pull output stage 972A into a high impedance state. The controller 50 may de-assert the second segment control signal 980B to disable the second push-pull output stage 972B, and place the second push-pull output stage 972B in a high impedance state.

[001306] The first push-pull output stage 972A may include a first segment first switching element 974', SW_{1A}', and a first segment second switching element 976', SW_{1B}'. The second push-pull output stage 972B may include a second segment first switching element 974", SW_{1A}", and a second segment second switching element 976", SW_{1B}". The first segment first switching

element 974', SW_{1A}', and the first segment second switching element 974", SW_{1A}", may be similar in form and function to the first switching element 214, SW_{1A}, depicted in Figures 12A and 12D. The first segment second switching element 976', SW_{1B}', and the second segment second switching element 976", SW_{1B}", may be similar in function and in form to the second switching element 216, SW_{1B}, depicted in Figures 12A and 12D.

[001307] The first segment first switching element 974', SW_{1A}', may include a gate 974G' in communication with a first voltage supply, V_{DD1}, a source 974S' in communication with an output of a power supply selection switch 971. The power selections switch 971 may receive the battery voltage, V_{BAT}, or the µC charge pump output voltage, $V_{\mu C_OUT}$, from the µC charge pump circuit 262. In addition, first segment first switching element 974', SW_{1A}', may include a drain 974D' in communication with the parallel amplifier output node 218. The first segment second switching element 976', SW_{1B}', may include a gate 976G', a source 976S' in communication ground, and a drain 976D' in communication with the parallel amplifier output node 218. The second segment first switching element 974", SW_{1A}", may include a gate 974G", a source 974S" also in communication with the output of the power supply selection switch 971. The second segment first switching element 974", SW_{1A}", may include a drain 974D" in communication with the parallel amplifier output node 218. The controller 50 may configure the power supply selection switcy 971 via a power supply selection signal to selectively power the first segmented output driver stage 970 with either the battery voltage, V_{BAT}, or the µC charge pump output voltage, $V_{\mu C_OUT}$, as a function of the battery voltage, V_{BAT}, and the maximum expected parallel amplifier supply voltage, V_{CC_MAX}. The second segment second switching element 976", SW_{1B}", may include a gate 976G", a source 976S" in communication ground, and a drain 976D" in communication with the parallel amplifier output node 218. The second segment first switching element 974", SW_{1A}", and the second segment second switching element 976", SW_{1B}", may be substantially similar in form and function to the first switching element 214, SW_{1A}, and the second switching element 216, SW_{1B}, depicted in Figures 12A and 12D.

[001308] In addition, the first segmented output driver stage 970 may further include an embodiment of an output control circuit 978 that is similar to the output control circuit 230A and the output control circuit 230B of the rechargeable parallel amplifiers 35B-C and 35E-F, depicted in Figures 12B-C and 12E-F, respectively. Figure 12G depicts an embodiment of the output control circuit 978 configured to control a first segmented output driver stage 970. However, to simplify the description of the rechargeable parallel amplifiers 35H-I depicted in Figures 12H-I, the description of the output control circuit 978 will substantially adopt the nomenclature and naming convention used to previously described the output control circuit 230A and the output control circuit 230B.

[001309] Illustratively, Figures 12B-C and Figures 12E-F depict that the output control circuit 230A and the output control circuit 230B may be configured to control the first output stage 210 with a first switch control output, V_{SW1A}, and a fourth switch control output, V_{SW1B}. The first switch control output, V_{SW1A}, may be configured to control the gate 214G of the first switching element 214, SW_{1A}, which may source a current to the parallel amplifier output node 218. The fourth switch control output, V_{SW1B}, may be configured to control the gate 216G of the second switching element 216, SW_{1B}, which may sink a current from the parallel amplifier output node 218.

[001310] Similarly, Figure 12G depicts that the output control circuit 978 may include a first amplifier output voltage V_A input 978A, V_{A_IN}, a second amplifier output voltage V_B input 978B, V_{B_IN}. The first amplifier output voltage V_A input 978A, V_{A_IN}, may be configured to receive the first amplifier output voltage, V_A. The second amplifier output voltage V_B input 978B, V_{B_IN}, may be configured to receive the second amplifier output voltage, V_B.

[001311] In addition, the output control circuit 978 may also include a first segment control input, SEG1, configured to receive a first segment control 980A and a second segment control input, SEG2, configured to receive a second segment control 980B. In addition, unlike the output control circuit 230A that controls the second output stage 220A of the rechargeable parallel amplifiers 35B, Figure 12G depicts an embodiment of the output control

circuit 978 without a V_{CC} input, V_{CC_IN}, configured to receive the modulated power supply voltage, V_{CC}, or a V_{AB} input, V_{AB_IN}, configured to receive a saved charge voltage, V_{AB}.

[001312] The output controller circuit 978 may also include a first segment first switch control output 978C', V_{SW1A}', a second segment first switch control output 978C", V_{SW1A}", a first segment second switch control output 978D', V_{SW1B}', and a second segment second switch control output 978D", V_{SW1B}".

[001313] To enable the first push-pull output stage 972A, the controller 50 may assert the first segment control signal 980A. In response to the assertion of the first segment control signal 980A, the output control circuit 978 enables the operation of the first push-pull output stage 972A. For example, the output control circuit 978 may be configured to provide the first amplifier output voltage, V_A, to the first segment first switch control output 978C', V_{SW1A}', and the second amplifier output voltage, V_B, to the first segment second switch control output 978D', V_{SW1B}', in response to the assertion of the first segmented control signal 980A.

[001314] To disable the first push-pull output stage 972A, the controller 50 may de-assert the first segment control signal 980A. In response to a de-assertion of the first segment control signal 980A, the output control circuit 978 may disable the operation of the second push-pull output stage 972B. For example, the output control circuit 978 may configure the first segment first switch control output 978C', V_{SW1A}', and the first segment second switch control output 978D', V_{SW1B}', to turn off the first segment first switching element 974', SW_{1A}', and the first segment second switching element 976', SW_{1B}', to place the first push-pull output stage 972A in a high impedance state.

[001315] As an example, in some embodiments, the output control circuit 978 may switchably couple the first amplifier output voltage V_A input 978A, V_{A_IN}, to the first segment first switch control output 978C', V_{SW1A}', and the second amplifier output voltage V_B input 978B, V_{B_IN}, to the first segment second switch control output 978D', V_{SW1B}', in response to the assertion of the first segmented control signal 980A. In response to de-assertion of the first segmented control

signal 980B, the output control circuit 978 may switchably decouple the first amplifier output voltage V_A input 978A, V_{A_IN}, from the first segment first switch control output 978C', V_{SW1A}', and decouple the second amplifier output voltage V_B input 978B, V_{B_IN}, from the first segment second switch control output 978D', V_{SW1B}'.

[001316] Similarly, to enable the second push-pull output stage 972B, the control circuit 978 may assert the second segment control signal 980B. In response to the assertion of the second segment control signal 980B, the output control circuit 978 may enable the operation of the second push-pull output stage 972B. For example, the output control circuit 978 may provide the first amplifier output voltage, V_A, to the second segment first switch control output 978C", V_{SW1A}", and the second amplifier output voltage, V_B, to the second segment second switch control output 978D", V_{SW1B}". To disable the second push-pull output stage 972B, the controller 50 may de-assert the second segment control signal 980B. In response to the de-assertion of the second segment control signal 980B, the output control circuit 978 may disable the second push-pull output stage 972B. For example, the output control circuit 978 may configure the second segment first switch control output 978C", V_{SW1A}", to turn off the second segment first switching element 974", SW_{1A}", and the second segment second switch control output 978D", V_{SW1B}", to provide a high impedance at the parallel amplifier output node 218.

[001317] A As an example, in some embodiments, the output control circuit 978 may switchably couple the first amplifier output voltage V_A input 978A, V_{A_IN}, to the second segment first switch control output 978C", V_{SW1A}", and the second amplifier output voltage V_B input 978B, V_{B_IN}, to the second segment second switch control output 978D", V_{SW1B}", in response to the assertion of the second segmented control signal 980B. In response to de-assertion of the second segmented control signal 980B, the output control circuit 978 may switchably decouple the first amplifier output voltage V_A input 978A, V_{A_IN}, from the second segment first switch control output 978C", V_{SW1A}", and decouple the second

amplifier output voltage V_B input 978B, V_{B_IN}, from the second segment second switch control output 978D", V_{SW1B}".

[001318] Accordingly, each of the first push-pull output stage 972A and the second push-pull output stage 972B may source current or sink current to the parallel amplifier output node 218 as a function of the first segment control signal 980, the second segment control signal 980B, and a difference between the difference between the parallel amplifier input voltage 204 (either V_{RAMP} or V_{RAMP_C}) and the modulated power supply voltage, V_{CC}, at the modulated power supply output 876.

[001319] Figure 12H depicts one of several embodiments of a rechargeable parallel amplifier 35H. The rechargeable parallel amplifier 35H may include a segmented parallel amplifier output, which is described with continuing reference to the embodiments of the rechargeable parallel amplifier 35B and the parallel amplifier 35G, depicted in Figures 12B and 12G. The rechargeable parallel amplifier 35H is similar to the rechargeable parallel amplifier 35B and the rechargeable parallel amplifier 35E, depicted in Figures 12B and 12E. In addition, the rechargeable parallel amplifier 35H may include an embodiment of an output control circuit 978' that is similar to the output control circuit 978, depicted in Figure 12G. However the output control circuit 978' is further configured to operate in a similar fashion as the output control circuit 230A of the rechargeable parallel amplifier 35B and rechargeable parallel amplifier 35E in order to control a second segmented output driver stage 982. The second segmented output driver stage is functionally similar to the second output stage 210A. However, the second segmended output driver stage 982 may include a first rechargeable push-pull output stage 984A and a second rechargeable push-pull output stage 984B.

[001320] For example, the first rechargeable push-pull output stage 984A may include a first segment third switching element 986', SW_{2A}', and a first segment fourth switching element 988', SW_{2B}'. The first segment third switching element 986', SW_{2A}', may include a source 986S' coupled to positive terminal of the charge conservation capacitor 228, C_{AB}, a drain 986D' coupled to the parallel

amplifier output node 218, and a gate 986G' coupled to the first segment third switch control output 978E', V_{SW2A}'. The first segment fourth switching element 988', SW_{2B}', may include a source 988S' coupled to the parallel amplifier output node 218, a drain 988D' coupled to the positive terminal of the charge conservation capacitor 228, C_{AB}, and a gate 988G' coupled to the first segment fourth switch control output 978F', V_{SW2B}'.

[001321] Similarly, the second rechargeable push-pull output stage 984B may include a second segment third switching element 986", SW_{2A}", and a second segment fourth switching element 988", SW_{2B}". The second segment third switching element 986", SW_{2A}", may include a source 986S" coupled to positive terminal of the charge conservation capacitor 228, C_{AB}, a drain 986D" coupled to the parallel amplifier output node 218, and a gate 986G" coupled to the second segment third switch control output 978E", V_{SW2A}". The second segment fourth switching element 988", SW_{2B}", may include a source 988S" coupled to the parallel amplifier output node 218, a drain 988D" coupled to the positive terminal of the charge conservation capacitor 228, C_{AB}, and a gate 988G" coupled to the second segment fourth switch control output 978F", V_{SW2B}".

[001322] The rechargeable parallel amplifier 35H further includes the first push-pull output stage 972A and the second output push-pull stage 972B of the first segmented output driver stage 970, depicted in Figure 12G. The output control circuit 978' further includes the first segment first switch control output 978C', V_{SW1A}', coupled to the gate 974G' of the first segement first switching element 974', SW_{1A}', the first segment second switch control output 978D', V_{SW1B}', coupled to the gate 976G' of the first segement second switching element 976', SW_{1B}', the second segment first switch control output 978C", V_{SW1A}", coupled to the gate 974G" of the second segment first switching element 974", SW_{1A}", and the second segment second switch control output 978D", V_{SW1B}", coupled to the gate 976G" of the second segment second switching element 976", SW_{1B}".

[001323] The output control circuit 978' further includes a V_{AB} input 978G, V_{AB_IN}, configured to receive a saved charge voltage, V_{AB}, a parallel amplifier output

voltage V_{PARA_AMP} input 978H, $V_{PARA_AMP_IN}$, configured to receive the parallel amplifier output voltage, V_{PARA_AMP}, and a modulated power supply voltage V_{CC} input 978I, V_{CC_IN}, configured to receive the modulated power supply voltage, V_{CC}, generated at the modulated power supply output 876, as depicted in Figures 40A-C, and 46A-B.

[001324] In some embodiments, the rechargeable parallel amplifier 35H may be configured to operate in a similar manner as the parallel amplifier 35G by only enabling the operation of the first push-pull output stage 972A and the second output push-push pull output stage 972B, as previously described with respect to the parallel amplifier 35G, depicted in Figure 12G. In addition, similar the parallel amplifier 35G, the controller 50 may selectively power the rechargeable parallel amplifier 35H from either the battery voltage, V_{BAT}, or the µC charge pump output voltage, $V_{\mu C_OUT}$, from the µC charge pump circuit 262.

[001325] To enable the rechargeable parallel amplifier 35H to operate as a rechargeable parallel amplifier, the output control circuit 978' may enable the operation of the first rechargeable push-pull output stage 984A and the second rechargeable push-pull output stage 972A in response to the assertion of the first segment control signal 980A. Alternatively, or in addition, the output control circuit 978' may enable the operation of the second rechargeable push-pull output stage 984B and the second push-pull output stage 972B in response to the assertion of the second segment control signal 980B.

[001326] To enable the first rechargeable push-pull output stage 984A, the output control circuit 978' may enable the operation of the first segment third switch control output 978E', V_{SW2A}', and the first segment fourth switch control output 978F', V_{SW2B}', in response to assertion of the first segment control signal 980A. To enable the second rechargeable push-pull output stage 984B, the output control circuit 978' may enable the operation of the second segment third switch control output 978E", V_{SW2A}", and the second segment fourth switch control output 978F", V_{SW2B}", in response to assertion of the first segment control signal 980B.

[001327] To operate in the linear mode of operation when enabled to operate as a rechargeable parallel amplifier, the rechargeable parallel amplifier 35H configures the output control circuit 978' to control the gates 974G' and 974G" in a similar fashion as the output control circuit 230A controls the gate 214G, control the gates 976G' and 976G" in a similar fashion as the output control circuit 230A controls the gate 216G, control the gates 986G' and 986G", in a similar fashion as the output control circuit 230A controls the gate 222G, and control the gates 988G', and 988G' in as similar fashion as the output control circuit 230A controls the gate 224G. Accordingly, in a similar fashion, the rechargeable parallel amplifier 35H may be configured to operate as a rechargeable parallel amplifier as a function of the first segment control signal 980A and the second segment control signal 980B.

[001328] Figure 12I depicts another embodiment of a rechargeable parallel amplifier 35I that is similar to the rechargeable parallel amplifier 35H. The description of the rechargeable parallel amplifier 35I will be carried out with continuing reference to the rechargeable parallel amplifier 35C, the rechargeable parallel amplifier 35F, and the rechargeable parallel amplifier 35H depicted in Figures 12C, 12F, and 12H. The output control circuit 978' is further configured to control a second segmented output driver stage 982' that is functionally similar to the second output stage 210B of the rechargeable parallel amplifier 35C and the rechargeable parallel amplifier 12F, depicted in Figures 12C and 12F.

[001329] Similar to the rechargeable parallel amplifier 35H, the second segmented output driver stage 982' may include a first rechargeable push-pull output stage 984A' and a second rechargeable push-pull output stage 984B'. The first rechargeable push-pull output stage 984A' is similar to the first rechargeable push-pull output stage 984A except the drain 988D' of the first segment fourth switching element 988', SW_{2B}', is coupled to the modulated power supply output 876. Similarly, the second rechargeable push-pull output stage 984A' is similar to the second rechargeable push-pull output stage 984B' except the drain 988D" of the second segment fourth switching element 988", SW_{2B}", is coupled to the modulated power supply output 876.

[001330] In some embodiments, the rechargeable parallel amplifier 35I may be configured to operate in a similar manner as the parallel amplifier 35G by only enabling the operation of the first push-pull output stage 972A and the second output push-push pull output stage 972B in response to the assertion of the respective first segment control signal 980A and the second segment control signal 980B, as previously described with respect to the parallel amplifier 35G, depicted in Figure 12G. In addition, similar the parallel amplifier 35G, the controller 50 may selectively power the rechargeable parallel amplifier 35I from either the battery voltage, V_{BAT}, or the µC charge pump output voltage, $V_{\mu C_OUT}$, from the µC charge pump circuit 262.

[001331] To enable the rechargeable parallel amplifier 35I to operate as a rechargeable parallel amplifier, the output control circuit 978' may enable the operation of the first rechargeable push-pull output stage 984A' and the first push-pull output stage 972A in response to the assertion of the first segment control signal 980A. Alternatively, or in addition, the output control circuit 978' may enable the operation of the second rechargeable push-pull output stage 984B and the second push-pull output stage 972B in response to the assertion of the second segment control signal 980B.

[001332] To enable the first rechargeable push-pull output stage 984A', the output control circuit 978' may enable the operation of the first segment third switch control output 978E', V_{SW2A}', and the first segment fourth switch control output 978F', V_{SW2B}', in response to assertion of the first segment control signal 980A. To enable the second rechargeable push-pull output stage 984B', the output control circuit 978' may enable the operation of the second segment third switch control output 978E", V_{SW2A}", and the second segment fourth switch control output 978F", V_{SW2B}", in response to assertion of the first segment control signal 980B.

[001333] To operate in the linear mode of operation when enabled to operate as a rechargeable parallel amplifier, the rechargeable parallel amplifier 35I may configure the output control circuit 978' to further control the gates 974G' and 974G" in a similar fashion as the output control circuit 230B controls the

gate 214G, control the gates 976G' and 976G" in a similar fashion as the output control circuit 230B controls the gate 216G, control the gates 986G' and 986G", in a similar fashion as the output control circuit 230B controls the gate 222G, and control the gates 988G', and 988G' in as similar fashion as the output control circuit 230B controls the gate 224G. Accordingly, in a similar fashion, the rechargeable parallel amplifier 35l may be configured to operate as a rechargeable parallel amplifier as a function of the first segment control signal 980A and the second segment control signal 980B.

[001334] Figure 46C depicts an embodiment of a parallel amplifier 2200 configured to combine the functionality of the average power tracking control circuit 944 and the parallel amplifier 928, depicted in Figure 46B. The embodiments of the parallel amplifier 2200 may be configured to operate in a number of modulation mode feedback signal modes as a function of the expected output power to be generated by the embodiments of the radio frequency power amplifiers 869 and 869'. As a non-limiting example, the modulation mode feedback signal modes may include a parallel amplifier mode and an average power tracking controller mode.

[001335] Some embodiments of the parallel amplifier 2200 may effectively combine the functionality of the parallel amplifier 928, the average power tracking control circuit 944, and the first signal control multiplexer 946. As described below in further detail, the parallel amplifier 2200 may include a parallel amplifier feedback output 928E' configured to provide a modulation mode feedback signal. The parallel amplifier feedback output 928E' may generate a modulation mode feedback signal substantially equivalent to one of a scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the average power tracking control signal 966 as a function of the power level modulation mode in which the power management system 870A is configured to operate. For example, in a pseudo-envelope tracking mode, the parallel amplifier 2200 may generate the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. In the medium power average power tracking mode, the parallel amplifier 2200 may generate the average power tracking control signal 966 at the parallel amplifier feedback

output 928E', and disable the parallel amplifier output 928C. For example, when disabled, the parallel amplifier 2200 may configure the parallel amplifier output 928C to provide a high impedance path to ground.

[001336] In addition, the parallel amplifier 2200 may also include a feedback transconductance, $Gm_{FEEBACK}$. In some embodiments, the controller 50 or the power management system 870A may configure the magnitude of the average power tracking control signal 966. In the medium power average power tracking modulation mode, the power management system 870A may set the feedback transconductance, $Gm_{FEEDBACK}$, to substantially equal the programmable average power tracking transconductance, Gm_{APT}, that average power tracking controller circuit 944 may use to generate the average power tracking control signal 966.

[001337] The parallel amplifier 2200 may configure the parallel amplifier feedback output 928E to provide a modulation mode feedback signal substantially equal to a product of the programmable average power tracking transconductance, Gm_{APT}, and a difference voltage substantially equal to the V_{RAMP} signal less the modulated power supply voltage, V_{CC}: The modulation mode feedback signal may substantially equal Gm_{APT} x (V_{RAMP} – V_{CC}).

The controller 50 may configure the parallel amplifier 2200 to generate the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, in response to the differential V_{RAMP} signal when the power management system 870A operates in either the high power modulation mode or the medium power envelope tracking modulation. In addition, the feedback transconductance, $Gm_{FEEBACK}$, may be configured to set the fractional relationship between the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, and the parallel amplifier output current, I_{PARA_AMP}.

[001338] Figure 46C depicts an example embodiment of a parallel amplifier 2200 that includes a segmented parallel amplifier output driver stage. Some embodiments of the parallel amplifier 2200 may include various segmentation configurations. Some of the embodiments of the parallel amplifier 2200 may be configured in a similar fashion as the embodiments of the rechargeable parallel amplifiers 35B-C, 35E-F, and 35H-I, depicted in

Figures 12B-C, 12E-F, and 12H-I, and/or the parallel amplifiers 35G-I that may include a segmented output driver stage, depicted in Figures 12G-I, and/or the parallel amplifiers 35A, 35D, and 35G, depicted in Figure 12A, 12D, and 12G. The description of the parallel amplifier 2200 will be carried out with continuing reference to the embodiments of the power management system 870, the power management system 870A, the parallel amplifier circuit 874, the parallel amplifier circuit 874', and the embodiments of the parallel amplifier 928, 928' and 928", which are depicted in Figures 40A-E and 46A-C and 46E-H.

[001339] Similar to the parallel amplifier 928, the parallel amplifier 2200 may include a non-inverting input 928A configured to receive a first control signal, an inverting input 928B, a parallel amplifier output 928C, a parallel amplifier supply voltage input 928D configured to receive a supply voltage to power the parallel amplifier 2200, and a parallel amplifier feedback output 928E' configured to provide a modulation mode feedback signal. Some embodiments of the parallel amplifier 2200 may further include a parallel amplifier front-end stage 2202 and a parallel amplifier output stage 2204. The parallel amplifier output stage 2204 may include a segmented output stage 2206 and a feedback output stage 2208. In some embodiments, the segmented output stage 2206 may include two or more segments. For example, the segmented output stage may include a first output driver segment 2206D including a first output driver segment output and a second output driver segment 2206E including a second output driver segement segment operablely coupled to the first output driver segment output to form the parallel amplifier output 928C. In some embodiments of the parallel amplifier 2200, the first output driver segment 2206D may be enabled or disabled by a first segment control signal 980A. The second output driver segment 2206E may be enabled or disabled by a second segment control signal 980B. In addition, in some embodiments of the parallel amplifier 2200, the feedback output stage 2208 may also be divided into two or more segments, where each of the two or more segments of the feedback output stage 2208 correspond to a respective one of the two or more segments of the segmented output stage 2206. As an example, the feedback output stage 2208 may include a first

feedback output driver segment 2208D having a first feedback output driver segment output and a second feedback output driver segment 2208E having a second feedback output driver segment output operably coupled to the first output driver segment output to form the parallel amplifier feedback output 928E'. The first feedback output driver segment and the second feedback output driver segment may be enabled or disabled by the first segment control signal 980A and the second segment control signal 980B, respectively. The first feedback output driver segment 2208D corresponds to the first output driver segment 2206D and the second feedback output driver segment 2208E corresponds to the second output driver segment 2206E. For example, in the parallel amplifier mode of operation, the first feedback output driver segment 2208D may generate an output current that is fractionally related to an output current generated by the first output driver segment 2206D, and the second feedback output driver segment 2208E may generate an output current that is fractionally related to an output current generated by the second output driver segment 2206E. The parallel amplifier 2200 may be configured to generate a modulation mode feedback signal that is substantially equivalent to the sense parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, which is fractionally related to the parallel amplifier output current, I_{PARA_AMP}.

[001340] In addition, the parallel amplifier 2200 may include a parallel amplifier mode of operation and an average power tracking controller mode of operation. In the parallel amplifier mode of operation, the parallel amplifier 2200 may be configured to generate a parallel amplifier output current, I_{PARA_AMP} to generate a parallel amplifier output voltage, V_{PARA_AMP} at the parallel amplifier output 928C. In addition, the parallel amplifier 2200 may configure the parallel amplifier feedback output 928E' to provide a modulation mode feedback signal that is substantially the same as the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. In the average power tracking controller mode of operation, the parallel amplifier 2200 may disable the parallel amplifier output 928C to provide a high impedance load. In addition, in the average power tracking controller mode of operation, the parallel amplifier 2200 may configure the parallel amplifier

feedback output 928E' to provide a modulation mode feedback output signal that is substantially the same as the average power tracking control signal 966, depicted in Figure 46B.

[001341] The parallel amplifier 2200 may be in communication with the controller 50 via a control bus 44. The controller 50 may configure various parameters or control signal to configure the parallel amplifier 2200 to operate in either the parallel amplifier mode of operation or the average power tracking mode of operation. As an example, Figure 46C depicts an embodiment of the parallel amplifier 2200 that includes a segmented output stage 2206 divided into a first output driver segment 2206D and a second output driver segment 2206E. The parallel amplifier 2200 may receive a first segment control signal 980A and a second segment control signal 980B from the controller 50. As an example, the first segment control signal 980A may be asserted to enable the first output driver segment 2206D and the second segment control signal 980B may be asserted to enable the second output driver segment 2206E. As further depicted in Figure 46G, some embodiments of the parallel amplifier 2200 may include an embodiment of the feedback output stage 2208 that is segmented into a first feedback output driver segment 2208D and a second feedback output driver segment 2208E. As an example, the first segment control signal 980A may be asserted to enable the first feedback output driver segment 2208D and the second segment control signal 980B may be asserted to enable the second feedback output driver segment 2208E. In some embodiments, the parallel amplifier may be further configured to receive a feedback stage enable 2214 and a feedback transconductance signal 2216 from the controller 50. The controller 50 may configure the feedback stage enable 2214 to enable and disable the feedback output stage 2208. As an example, the controller 50 may de-assert the feedback stage enable 2214 to disable the feedback output stage 2208.

[001342] As an example, the controller 50 may assert the feedback stage enable 2214 to enable the feedback output stage 2208. In some embodiments, the feedback output stage 2208 may switch into the average power tracking

controller mode of operation when the first segment control signal 980A and the second segment control signal 980B are disabled and the feedback stage enable 2214 is asserted. In this case, the feedback output stage 2208 may enable the first feedback output driver segment 2208D and the second feedback output driver segment 2208E to operate in the average power tracking mode of operation. In addition, in some embodiments, the controller 50 may provide a feedback transconductance signal 2216 to the parallel amplifier 2200 to configure the transconductance of the feedback output stage as a function of being in either the parallel amplifier mode of operation or the average power tracking mode of operation. As an example, the controller 50 may assert the feedback transconductance signal 2216 to configure the feedback output stage 2208 to use the programmable average power tracking transconductance, Gm_{APT}, to generate the modulation mode feedback signal. The controller 50 may de-assert the feedback transconductance signal 2216 to configure the feedback output stage 2208 to use the feedback output stage transconductance, Gm_{FBS}, in the parallel amplifier mode of operation.

[001343] Alternatively, some embodiments of the parallel amplifier 2200 may include one or more control registers that may receive and store an operational mode parameter, a segmentation configuration parameter, a feedback output stage enable parameter, a segmented output stage transconductance, Gm_{SEG}, parameter, and a feedback output stage transconductance, Gm_{FBS}, parameter. The operational mode parameter may be set to configure the parallel amplifier 2200 to operate in either parallel amplifier mode of operation or the average power tracking mode of operation. The feedback output stage enable parameter may be set to enable or disable the operation of the feedback output stage. The controller 50 may set the segmented output stage transconductance, Gm_{SEG}, parameter to configure a segmented output stage transconductance, Gm_{SEG}, of the segmented output stage 2206. The controller 50 may set the feedback output stage transconductance, Gm_{FBS}, parameter to configure a feedback output stage transconductance, $Gm_{FBS,}$ of the feedback output stage 2208.

[001344] As an alternative non-limiting example, in still other embodiments of the parallel amplifier 2200, a segmention configuration parameter may be used to configure the operation of each of the segments of the segmented output stage 2206. The segmentation configuration parameter may also be used to configure the operation of each of the segments of the feedback output stage 2208. As a non-limiting example, the segmentation configuration parameter may be used to set the first segment control signal 980A and the second segment control signal 980B provided to the segmented output stage 2206 and the feedback output stage 2208. The parallel amplifier 2200 may enable or disable the first output driver segment 2206D and the second output driver segment 2206E of the segmented output stage 2206 as a function of the segmention configuration parameter. Similarly, the parallel amplifier 2200 may enable or disable the first feedback output driver segment 2208D and the second feedback output driver segment 2208E of the feedback output stage 2208 as a function of the segmention configuration parameter. Some embodiments of the parallel amplifier 2200 may include a parallel amplifier disable parameter to disable the parallel amplifier 2200 and /or place the parallel amplifier 2200 into low power standby state of operation. The segmented output stage 2206 may be disabled and provide a high impedance load when the parallel amplifier parameter is set to disable the parallel amplifier 2200.

[001345] The parallel amplifier front-end stage 2202 may include a non-inverting input 2202A in communication with the non-inverting input 928A, and configured to receive a first input signal. The parallel amplifier front-end stage 2202 may also include an inverting input 2202B configured to receive a second input signal from the inverting input 928B. the parallel amplifier front-end stage 2202 may further include a PFET control output 2202C configured to generate a PFET control signal and a NFET control output 2202D. The parallel amplifier front-end stage 2202 may be configured as a high impedance diffierential input configured to drive the segmented output stage 2206 and the feedback output stage 2208 as a function of a voltage difference between the non-inverting input 2202A and the inverting input 2202B. In response to the difference voltage developed

across the non-inverting input 2202A and the inverting input 2202B, the parallel amplifier front-end stage 2202 may be configured to generate the PFET control signal 2210 from the PFET control output 2202C and a NFET control signal 2212 from the NFET control output 2202D to drive the segmented output stage 2206 and the feedback output stage 2208. The PFET control signal 2210 and the NFET control signal 2212 may be provided to the segmented output stage 2206 to generate the parallel amplifier output current, I_{PARA_AMP}, and the feedback output stage 2208 to generate a modulation mode feedback signal from the parallel amplifier feedback output 928E'. In some embodiments, the PFET control signal 2210 and the NFET control signal 2212 may be further configured to independently drive each segment of the segmented output stage 2206. In some embodiments described below, embodiments of the feedback output stage 2208 may also be divided into segments substantially proportional to the segments of the segmented output stage 2206. In this case, the PFET control signal 2210 and the NFET control signal 2212 may be further configured to independently drive each segment of the feedback output stage 2208.

[001346] In the case where the voltage difference between the non-inverting input 2202A and the inverting input 2202B is substantially equal to zero, the PFET control signal 2210 and the NFET control signal 2212 may provided a balanced output to the segmented output stage 2206 such that the parallel amplifier output current, I_{PARA_AMP}, is substantially equal to zero. Similarly, in some embodiments, the PFET control signal 2210 and the NFET control signal 2212 may be configured to provide a balance output to the feedback output stage 2208 such that the modulation mode feedback signal generated at the parallel amplifier feedback output 928E' is substantially equal to zero when the voltage difference between the non-inverting input 2202A and the inverting input 2202B is substantially equal to zero.

[001347] Figure 46C further depicts an alternative embodiment of the parallel amplifier 2200 as a parallel amplifier 928' that includes a second non-inverting input 928F configured to receive a second control signal. The alternative configuration of parallel amplifier 928' will be described with respect to the

operation of the parallel amplifier 2200 with reference to Figure 46B. The parallel amplifier 2200 may further include a control signal selection switch 2220 having a first input 2220A configured to receive the first input signal from the non-inverting input 928A, a second input 2220B configured to receive a second input signal from the second non-inverting input 928F, and a control signal output 2220C in communication with the non-inverting input 2202A of the parallel amplifier front-end stage 2202. In some embodiments, the parallel amplifier 2200 configure the control signal selection switch 2220 to select the first input 2220A in the parallel amplifier mode of operation and the second input 2220B in the average power tracking controller mode of operation.

As an example, referring to Figure 46B, in the average power tracking controller mode, the parallel amplifier 2200 may be configured to select the V_{RAMP} signal generated by the low power differential to signal ended converter 952 at the second non-inverting input 928F. In the parallel amplifier mode of operation, the parallel amplifier 2200 may be configured to select the control signal 926 generated by the differential filter 924.

[001348] Returning to Figure 46C, as a non-limiting example, in some embodiments, the segmented output stage 2206 may be configured to in a similar fashion as the first segmented output driver stage 970, depicted in Figure 12G. Alternatively, as another non-limiting example, the segmented output stage 2206 may be configured to further include a second segmented output driver similar to the second segmented output driver 982, depicted in Figure 12H, or the second segmented output driver 982' depicted in Figure 12I.

[001349] For example, the segmented output stage 2206 may have a segmented output stage transconductance, Gm_{SEG}, which may be adjusted by the controller 50. The segmented output stage transconductance, Gm_{SEG}, may also be a function of the segmentation configuration of the parallel amplifier 2200. For example, the segmented output stage transconductance, Gm_{SEG}, may have a maximum value in the case where all the segments of the segmented output driver are enabled. Also, the segmented output stage transconductance may depend on the relative current carrying capacity of each

segment that is enabled. In addition, in some embodiments, the feedback output stage 2208 may also be divided into the same number of segments as the segmented output stage. In this case, the similar to the embodiments of the operational amplifier 442A, depicted in Figures 31A-B and Figures 32A-D, each segment of the feedback output stage 2208 may be substantially matched to a corresponding segment in the segmented output stage 2206 with respect to current carrying capacity to maintain a fractional relationship between the parallel amplifier output current, I_{PARA_AMP}, and the modulation mode feedback signal generated at the parallel amplifier feedback output 928E'.

[001350] For example, in the parallel amplifier mode of operation, the parallel amplifier 2200 may be configured to generate a parallel amplifier output current, I_{PARA_AMP}, from the parallel amplifier output 928C to produce a parallel amplifier output voltage, V_{PARA_AMP}. In addition, the parallel amplifier 2200 may be configured to generate a modulation mode feedback signal that is fractionally related to the parallel amplifier output current, I_{PARA_AMP}. In this case, the parallel amplifier generates the modulation mode feedback signal to be substantially equivalent to the sense parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$. In some embodiments, the fractional ratio between the modulation mode feedback signal and the parallel amplifier output current, I_{PARA_AMP}, may be programmable. In other embodiments, the fractional ratio between the modulation mode feedback signal and the parallel amplifier output current, I_{PARA_AMP}, may be fixed. In still other embodiments, the fractional ratio between the modulation mode feedback signal and the parallel amplifier output current, I_{PARA_AMP}, is based on a maximum parallel amplifier output current, I_{PARA_MAX}. In still other embodiments, the fractional ratio between the modulation mode feedback signal and the parallel amplifier output current, I_{PARA_AMP}, may be automatically adjusted based on the segmentation configuration of the parallel amplifier 2200.

[001351] In the average power tracking controller mode of operation, the parallel amplifier 2200 may be configured to generate a modulation mode feedback signal that is substantially the equivalent to the average power tracking control

signal. For example, referring briefly to Figure 46B, the various embodiments of the parallel amplifier 2200 may be configured in a similar fashion as the average power tracking controller circuit 944 to generate the modulation mode feedback signal based on a difference between the V_{RAMP} signal generated by the low power differential to single ended converter 942 and the modulated power supply voltage, V_{CC}. In this case, the feedback output stage transconductance, Gm_{FBS}, parameter may be adjusted to equal the programmable average power tracking transconductance, Gm_{APT}, of the average power tracking controller circuit 944. In some embodiments, the parallel amplifier 2200 may include a programmable average power tracking transconductance, Gm_{APT}, parameter that may be configured by the controller 50. In this case, parallel amplifier 2200 may selectively configure the feedback output stage 2208 to use the programmable average power tracking transconductance, Gm_{APT}, parameter in the average power tracking mode of operation and the feedback output stage transconductance, Gm_{FBS}, in the parallel amplifier mode of operation.

[001352] In addition, in the average power tracking control mode of operation, the parallel amplifier 2200 may be configured to place the parallel amplifier output 928C in a high impedance mode by disabling each of the segments of the segmented output stage 2206. For example, the controller may de-assert the first segment control signal 980A and the second segment control signal 980B to place the segmented output stage 2206 in a high impedance mode. The controller 50 may enable the feedback output stage 2208 by asserting the feedback stage enable 2214. In some embodiments, in the case where the first segment control signal 980A and the second segment control signal 980B are de-asserted and the feedback stage enable 2216 is enabled, the parallel amplifier 2200 may be configured to operate in the average power tracking controller mode of operation.

[001353] In some alternative embodiments, the parallel amplifier circuits 974 and 974' may further include an multiplexer, switch, or shared signaling configuration (not depicted) to selectively provide the V_{RAMP} signal generated by the low power differential to single ended converter 942 or the control signal 926

generated by the differential filter 924 to the non-inverting input 928A of the parallel amplifier 2200.

[001354] A non-inverting input 928A may receive a first input signal. An inverting input 928B may receive a second input signal. A parallel amplifier output 928C may generate the parallel amplifier output current, I_{PARA_AMP}, as a function of a difference between the first input signal and the second input signal. A parallel amplifier supply voltage input 928D may receive a μC charge pump output voltage, $V_{\mu C_OUT}$. The parallel amplifier feedback output 928E' However, unlike the parallel amplifier 928, the parallel amplifier 2200 is configured to provide a modulation mode feedback signal from the parallel amplifier feedback output 928E'. In addition, some embodiments of the parallel amplifier 2200 may further include a second non-inverting input 928F.

[001355] Figure 46D depicts an embodiment of a V_{OFFSET} loop circuit 41C that is similar to the embodiments the V_{OFFSET} loop circuit 41, depicted in Figure 8, and the embodiments of the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B, depicted in Figures 18A-D. The description of the V_{OFFSET} loop circuit 41C will be carried out with continuing reference to the V_{OFFSET} loop circuit 41A and V_{OFFSET} loop circuit 41B, depicted in the Figures 18A-D, and the parallel amplifier circuit 874, depicted in Figure 40C, and the parallel amplifier circuit 874', as depicted in Figure 46B, the switch mode power supply converter 872, depicted in Figures 40A-B and Figure 46A, the power management systems 870A-B and the respective parallel amplifier circuits 872B'-872C', depicted in Figures 40D-E, the power management systems 870E-H and the respective parallel amplifier circuits 872E'-872H', depicted in Figures 46E-H, and the switcher control circuit 52S, depicted in Figure 5S.

[001356] The V_{OFFSET} loop circuit 41C may be configured to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the high power modulation mode and the low power modulation mode of the power level modulation modes to regulate an offset voltage, V_{OFFSET}, across a coupling circuit configured to operably couple a parallel amplifier circuit output 874A to the modulated power supply output 876. In addition, the V_{OFFSET} loop circuit 41C may be further

configured to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the medium power average power modulation mode to regulate the modulated power supply voltage, V_{CC}, as a function of the diffential V_{RAMP} signal. In the medium power aveage power tracking modulation mode, the power management systems 870, 870A-870C, and 870E-870H may selectively configure the some embodiments of the V_{OFFSET} loop circuit 41C to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to provide an indication of an instantaneous error voltage between a target voltage for the modulated power supply output 876 and the modulate power supply voltage, V_{CC}, and/or an indication of a weighted error voltage between a target voltage for the modulated power supply output 876 and the modulate power supply voltage, V_{CC}. In medium power aveage power tracking modulation mode, some embodiments of the V_{OFFSET} loop circuit 41 may receive the target voltage for the modulated power supply output 876 from differential filter 924 and/or the low power differential to single ended converter 942. For example, the target voltage for the modulated powr supply output 876 may be the V_{RAMP} signal generated by the low power differential to single ended converter 942. As another example, the target voltage for the modulated power supply output 876 may be the control signal 926 generated by the differential filter 924 with either no frequency response compensation or correction or a low level of frequency response compensation or correction. For example, in some average power tracking "bang-bang" modes of operation, the target voltage may be selected between the V_{RAMP} signal or the control signal 926.

[001357] The V_{OFFSET} loop circuit 41C may include an offset multiplexer 2222, a target multiplexer 2224, and a summing circuit 2226 in cooperative communication with a threshold offset generation circuit 2228 to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$. Some embodiments of the V_{OFFSET} loop circuit 41C may further include a programmable reference 2230 configured to generate a reference voltage, V_{REF}. The controller 50 may be configured to control and configure the V_{OFFSET} loop circuit 41C via control bus 44. For example, the controller 50 may be in operable communication with the offset

multiplexer 2222, the target multiplexer 2224, the summing circuit 2226, the threshold offset generation circuit 2228, and the programmable reference 2230 via the control bus 44.

[001358] The summing circuit 2226 may include a non-inverting input 2226A, a first inverting input 2226B, and a second inverting input 2226C. In some embodiments, the summing circuit 2226 may be configured as summing amplifier. The non-inverting input 2226A may receive the modulated power supply voltage, V_{CC}, from the modulated power supply output 876. In addition, the first inverting input 2226B may receive an offset signal 2234 from an offset multiplexer output 2222D of the offset multiplexer 2222. The second inverting input 2226C may receive a target signal 2236 from a target multiplexer output 2224D of the target multiplexer 2224. The summing circuit 2226 subtracts the offset signal 2234 and target signal 2236 from the modulated power supply voltage, V_{CC}, to generate a loop circuit error signal 2238. The summing circuit 2226 may provide the loop circuit error signal 2238 to the threshold offset generation circuit 2228. In response to the loop circuit error signal 2238, the threshold offset generation circuit 2228 generates the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, based on the loop circuit error signal 2238 as a function of the power level modulation mode.

[001359] In some embodiments of the V_{OFFSET} loop circuit 41C, threshold offset generation circuit 2228 may be configured to function in as similar manner as the integrator with zero compensation 314, depicted in Figures 18B and 18D. Alternatively, in some embodiments of the V_{OFFSET} loop circuit 41C, the threshold offset generation circuit 2228 may be configured to function in a similar manner as the previously described K_{ERROR_GAIN} circuit 306, depicted in Figures 18B and 18D. In some alternative embodiments, the V_{OFFSET} loop circuit 41C be selectively configured to function in a similar manner as the integrator with zero compensation 314, the K_{ERROR_GAIN} circuit 306, and/or a combination thereof.

[001360] The offset multiplexer 2222 may include a first input 2222A configured to receive a parallel amplifier output voltage, V_{PARA_AMP}, a second input 2222B coupled to a ground reference, and a third input 2222C configured to receive a

reference voltage signal 2232, V_{REF}, from the programmable reference 2230. The controller 50 may configure the offset multiplexer 2222 to provide an offset signal 2234 from the offset multiplexer output 2222D to the first inverting input 2226B of the summing circuit 2226, which is selected from among the parallel amplifier output voltage, V_{PARA_AMP}, the ground reference, and the reference voltage signal, V_{REF}.

[001361] The target multiplexer 2224 may include a first input 2224A configured to receive a target offset voltage, V_{TARGET_OFFSET}, a second input 2224B configured to receive a V_{RAMP} signal, and a third input configured to receive a filtered V_{RAMP} signal from a pre-filter 313. The pre-filter 313 is previously described above with respect to the operation of the V_{OFFSET} loop circuit 41A and the V_{OFFSET} loop circuit 41B, depicted in Figures 18A-D. The pre-filter 313 may be configured to provide a degree of frequency compensation or pre-distortion to compensate for the frequency response of the V_{OFFSET} loop circuit 41C and the switch mode power supply converter 872. As an example, the pre-filter may include the programmable pole time constant, Tau_P, and the programmable zero time constant, Tau_Z. The controller 50 may adjust the values of the programmable pole time constant, Tau_P, and the programmable zero time constant, Tau_Z, to adjust the frequency response of the pre-filter 313. The filtered V_{RAMP} signal generated by the pre-filter 313 may be similar to a compensated V_{RAMP} signal, V_{RAMP_C}, where the pre-filter 313 has applied a degree of signal pre-distortion or frequency response compensation or correction to the V_{RAMP} signal to compensate for the frequency response of the control loop of the switch mode power supply converter 872 in the medium power average power tracking mode.

[001362] For example, in medium power average power tracking modulation mode, the controller 50 may configure the V_{OFFSET} loop circuit 41C to regulate the modulated power supply voltage, V_{CC}, as a function of the V_{RAMP} signal, where the V_{RAMP} signal provides a target voltage for the modulated power supply output 876. The controller 50 may configure the values of the programmable pole time constant, Tau_P, and the programmable zero time constant, Tau_Z, to

pre-distort the V_{RAMP} signal to provide a selected amount of frequency response compensation to improve the response or stability of the control loop of the switch mode power supply converter 872.

[001363] As an example, the controller 50 may configure the target multiplexer 2224 to provide a target signal 2236 from the target multiplexer output 2224D to the second inverting input 2226C of the summing circuit 2226. The target signal 2236 may be selected from among the target offset voltage, $V_{TARGET_TRESHOLD}$, the V_{RAMP} signal, and the filtered V_{RAMP} signal. In some alternative embodiments, the V_{OFFSET} loop circuit 41C may be configured to receive the control signal 926 from the differential filter 924. The differential filter 924 may apply a level of frequency response compensation, peakinig, or signal distortion to the differential V_{RAMP} signal to generate a compensated V_{RAMP} signal as a function of the power level modulation mode.

[001364] Referring to Figures 40A-E and Figures 46A-H, Figure 40D depicts an embodiment of a power management system 870B that is similar to the embodiments of the power management system 870, depicted in Figures 40A-C. The power management system 870A includes an embodiment of a parallel amplifier circuit 874B' having an embodiment of the V_{OFFSET} loop circuit 41C. The V_{OFFSET} loop circuit 41C may be configured to receive the control signal 926 from differential filter 924 in the medium power average power tracking mode of operation.

[001365] In this case, the third input 2224C may receive the control signal 926 from the differential filter 924. In the medium power average power tracking mode, the differential filter 924 may be configured to provide the V_{RAMP} signal to the second input 2224B of the target multiplexer 2224 in the medium power average power tracking modulation mode. As another alternative, in some embodiments, the second input 2224B may selectively receive the V_{RAMP} signal from either the single ended output 942C of the low power differential to single ended converter 942 or the control signal 926 from the differential filter 924. As still another alternative, some embodiments of the target multiplexer 2224 may

further include a fourth input 2224E configured to receive the control signal 926 from the differential filter 924.

[001366] In the high power modulation mode and the medium power envelope tracking mode, the controller 50 may configure the target multiplexer 2224 and the offset multiplexer to operate in a V_{OFFSET} loop control configuration to regulate the offset voltage, V_{OFFSET}, between the parallel amplifer circuit output 874A and the modulated power supply output 876.

[001367] In the V_{OFFSET} loop control configuration, the controller 50 may configure the target multiplexer 2224 to provide the target offset voltage, V_{TARGET_OFFSET}, as the target signal 2236. In addition, the controller 50 may configure the offset multiplexer 2222 to provide the parallel amplifier output voltage, V_{PARA_AMP}, as the offset signal 2234. The summing circuit 2226 may generate a loop circuit error signal 2238 substantially equal to the modulated power supply voltage, V_{CC}, less a sum of the target offset voltage, V_{TARGET_OFFSET}, and the parallel amplifier output voltage, V_{PARA_AMP}, which may be expressed mathematically as $Error_{LOOP_CIRCUIT} = [V_{CC} - V_{TARGET_OFFSET} - V_{PARA_AMP}]$.

[001368] Thus, referring briefly to Figures 18A-D, some embodiments of the V_{OFFSET} loop circuit 41C configured to operate in the V_{OFFSET} loop configuration may configure the offset multiplexer 2222 and the target multiplexer 2224 such that the summing circuit 2226 may generate a loop circuit error signal 2238 substantially similar to the V_{OFFSET} error signal 304 generated by the summing circuit 300. As previously described, the V_{OFFSET} loop circuits 41A-B may generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to regulate the offset voltage, V_{OFFSET}, across the coupling circuit 18 as a function of the V_{OFFSET} error signal 304. Returning to Figure 46D, the threshold offset generation circuit 2228 may use the loop circuit error signal 2238 to generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to regulate the offset voltage, V_{OFFSET}, across the coupling capacitor 18A.

[001369] In the medium power average power tracking modulation mode, the controller 50 may configure to the V_{OFFSET} loop circuit 41C to regulate the generation of the switching voltage, V_{SW}, as a function of the differential V_{RAMP}

signal. In this case, the controller 50 may configure the parallel amplifier circuit 874' to disable the generation of the switch mode power supply feedback signal 40A. In addition, the controller may configure the offset multiplexer 2222 and the target multiplexer 2224 to operate in a switch mode power supply converter control loop configuration.

[001370] As an example, the controller 50 may configure the target multiplexer 2224 to provide the V_{RAMP} signal as the target signal 2236. In some alternative embodiments, the controller 50 may configure the target multiplexer 2224 to provide the control signal 926 as a target signal 2236. The controller 50 may configure the offset multiplexer 2222 to provide the ground voltage from the second input 2222B as a target signal 2236. In response, the summing circuit 2226 may generate a loop circuit error signal 2238 that is substantially equal to the modulated power supply voltage, V_{CC}, less the V_{RAMP} signal. Referring to Figures 3A, 3I, 4B-C, and 4J-L, the composite control signal provided to the inverting inputs of the first comparator 140, the second comparator 142, the third comparator 144, and the fourth comparator 146 by subtracting the threshold offset current 42, $I_{THRESHOLD_OFFSET}$. Thus, in the switch mode power supply converter control loop configuration, the composite control signal may be substantially equal to a negative value of the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, as the composite control signal.

[001371] Because the switch mode power supply feedback signal 40A is disabled, the composite control signal may be a function of the V_{RAMP} signal less the modulated power supply voltage, V_{CC}, which may be expressed mathematically as a switch mode power supply converter control loop error, $Error_{SWITCHER_LOOP_CIRCUIT} = (V_{RAMP} - V_{CC})$. In the case where the threshold offset generation circuit 2228 is configured to operate in a substantially similar manner as the integrator with zero compensation 314, depicted in Figures 18B and 18D, the composite control signal is an indication of a weighted error voltage between a target voltage for the modulated power supply output 876 and the modulate power supply voltage, V_{CC}.

[001372] As described above, the integrator with zero compensation 314 may have a filter response that is equivalent to a Laplace transfer function equal to $[(1+Tau_{0^*} s)/(Tau_1 *s)]$. Thus, in the medium power average power tracking modulation mode, the composite control signal may be an average power tracking weighted error voltage signal, $I_{APT_WEV}(t)$ as shown in equation (23) as follows:

$$(23)\quad I_{APT_WEV}(t) = \frac{Tau_0}{Tau_1}[V_{RAMP}(t) - V_{CC}(t)] + \frac{1}{Tau_1}\int_0^t [V_{RAMP}(\tau) - V_{CC}(\tau)]\,\partial\tau,$$

for $t \geq 0$. The weighted error voltage signal may include an instantaneous error voltage component and an average error voltage component.

[001373] Some embodiments of the switcher control circuit 880 may use the composite control signal that is a measure of the average error voltage of the modulated power supply voltage, V_{CC}, to regulate generation of the switching voltage, V_{SW}, in the average power tracking "buck-buck" mode of operation. In the average power tracking modes of operation, some embodiments of the switcher control circuit 880 may use only the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, as the composite control signal for both the average power tracking "buck-buck" mode and the average power tracking "buck-boost" mode.

[001374] Alternatively, in the case where the threshold offset generation circuit 2228 is configured to operate in a substantially similar manner as the previously described K_{ERROR_GAIN} circuit 306, depicted in Figures 18B and 18D. For example, the threshold offset current 42 $I_{THRESHOLD_OFFSET}$, may be substantially equal to a product of the offset voltage gain, K_{ERROR_GAIN}, and a difference voltage substantially equal to the V_{RAMP} signal less the modulate power supply voltage, V_{CC}, which may be expressed mathematically as $I_{THRESHOLD_OFFSET} = K_{ERROR_GAIN} \times (V_{RAMP} - V_{CC})$. The controller 50 may configure the offset voltage gain, K_{ERROR_GAIN}, to be substantially equal to the average power tracking transconductance, Gm_{AMP}, in order to generate a threshold offset current 42 $I_{THRESHOLD_OFFSET}$, that is substantially equal to the average power tracking control signal 966. Thus, in the medium power average power tracking

modulation mode, the composite control signal may be an average power tracking instantanesous error voltage signal, $I_{APT_INST_EV}(t)$ as shown in equation (24) as follows:

(24) $$I_{ATP_INST_EV}(t) = Gm_{APT}[V_{RAMP}(t) - V_{CC}(t)].$$

[001375] In some alternative embodiments, the V_{OFFSET} loop circuit 41C be selectively configured to function in a similar manner as the integrator with zero compensation 314, the K_{ERROR_GAIN} circuit 306, and/or a combination thereof. In addition, in some embodiments, the V_{OFFSET} loop circuit 41C may be further configured to operate in a pre-charge mode of operation for a predetermined period of time to pre-charge the modulated power supply voltage, V_{CC}, prior to commencement of a data transmission in a substantially manner as the embodiments of the V_{OFFSET} loop circuit 41A or V_{OFFSET} loop circuit 41B may pre-charge the coupling capacitor 18A prior to commencement of a data transmission.

[001376] For the sake of convenience, and not by way of limitation, a method 1700, a method 1800, a method 1900, a method 2000, and method 2100, depicted inb Figure 47, Figures 48A-B, Figures 49A-B, Figures 50A-B, and Figure 51, may describe various operations, tasks, functions, firmware, logic operations, hardware, analog logic or digital logic, a digital base band processing circuit, firmware, and/or software, a transceiver/communication device, and/or some combination thereof in terms of the controller 50 and/or the power management system 870. However, this is by way of description and not intended to limit the scope of the method 1700, the method 1800, the method 1900, the method 2000, and the method 2100. In addition, in some embodiments, the operations of the controller 50 and/or various selected portions of the power management system 870 may be incorporated into the hardware, software, and/or firmware of various components or portions of a transceiver/ communication device.

[001377] Figure 47 depicts the method 1700 for configuring of the operation of the pseudo-envelope tracking modulated power supply system 868A that depends upon the expected output power to be generated by the radio frequency power amplifier 869' during a data transmission. The method 1700 is described with continuing reference to the pseudo-envelope tracking modulated power supply system 868A depicted in Figures 46A-B, 48A-B, 49A-B, 50A-B, and 51A. In addition, method 1700 is further described with continuing reference to Figures 40A-C, 41, 42, 43A-B, 44A-B, and 45.

[001378] The pseudo-envelope tracking modulated power supply system 868A may determine an expected output power to be generated by a radio frequency power amplifier 869' during a data transmission. (Step 1702). For example, in some embodiments, the controller 50 may determine the expected output power to be generated by the radio frequency power amplifier 869' a based upon the envelope characteristics of data signal to be transmitted during a data transmission slot. In other embodiments, the digital baseband processing portion of the transceiver or modem that provides the differential V_{RAMP} signal to the parallel amplifier circuit 874' may determine the expected output power to be generated by the radio frequency power amplifier 869'. Based on the expected output power to be generated by the radio frequency power amplifier 869' during the data transmission, the power management system 870A may select a power modulation mode of operation from among a number of power level modulation modes of operation. (Step 1704). For example, the power management system 870 depicted in Figure 42 includes a high power modulation mode, a medium power modulation mode, and a low power modulation mode. In the case where the expected output power to be generated by the radio frequency power amplifier 869 is greater than or equal to a high power modulation mode threshold, the power management system 870 configures the pseudo-envelope tracking modulated power supply system 868A to operate in a high power modulation mode. (Step 1706). Alternatively, in the case where the expected output power to be generated by the radio frequency power amplifier 869 is less than the high power modulation mode threshold but greater than a low power

modulation mode threshold, the power management system 870 configures the pseudo-envelope tracking modulated power supply system 868A to operate in a medium power modulation mode. (Step 1708). In the case where the expected output power to be generated by the radio frequency power amplifier 869 is less than or equal to the low power modulation mode threshold, the power management system 870 may configure the pseudo-envelope tracking modulated power supply system 868A to operate in the medium power average power tracking modulation mode. (Step 1710). In the case where the expected output power to be generated by the radio frequency power amplifier 869 is less than or equal to the low power modulation mode threshold, the power management system 870 may configure the pseudo-envelope tracking modulated power supply system 868A to operate in the low power average power tracking modulation mode. (Step 1712).

[001379] Figures 48A-B depict a method 1800 for configuring the pseudo-envelope tracking modulated power supply system 868A to operate in a high power modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' to during a data transmission at least equal to the high power modulation mode threshold. Some aspect of the method 1800 may be similar to the method 1400, depicted in Figures 43A-B. Figure 43A-B depict the method 1400 for configuring the pseudo-envelope tracking modulated power supply system 868 and the power management system 870 to operate in a high power modulation mode. Accordingly, without intent to limit the scope of the method 1800, the description of the method 1800 may be described with continuing reference to the method 1400. In addition, the method 1800 is described with continuing reference to the various embodiments of the pseudo-envelope tracking modulated power supply system 868A, the power management system 870A, the switch mode power supply converter 872, and parallel amplifier circuit 874', depicted in Figures 46A-B, Figure 47, Figure 48A-B, Figure 49A-B, Figure 50A-B, and Figure 51. For the sake of convenience, and not by way of limitation, description of the method 1800 may refer to the controller 50. However, as

discussed above, a digital base band processing portion of the transceiver/communication device and/or a combination of hardware and firmware associated with the power management system 870A may likewise operate in conjunction with the controller 50. In addition, the operations of controller 50 may be incorporated into the hardware and/or firmware of various components or portions of a transceiver/ communication device.

[001380] To configure the power management system 870A to operate in the high power modulation mode, the controller 50 may determine or receive envelope characteristics data that describe the modulated radio frequency signal to be transmitted by the radio frequency power amplifier 869'. In other embodiments, the envelope characteristics data may further include parameters to configure the μC charge pump circuit 262 and the V_{OFFSET} control circuit 41. In some embodiments the power management system 870A or the controller 50 may receive a segmentation mode for configuring the switching circuit 884, a segmentation configuration for configuring the parallel amplifier 928, an average expected output power, P_{OUT_AVE}, to be generated by the radio frequency power amplifier 869', and the segmentation mode for the switching circuit 884. For example, a digial modem or a digital baseband circuit configured to operate with the power management system 870A may have a look-up table, LUT, that maps the average expected output power, P_{OUT_AVE}, to segmentation mode of the switching circuit 884 and the segmentation configuration for the parallel amplifier 928. Based on the mapping between the average expected output power, P_{OUT_AVE}, to the segmentation mode of the switching circuit 884 and the segmentation configuration for the parallel amplifier 928, the digital modem or the digital baseband circuit may provide the segmentation mode and segmentation configuration information the power management system 870A. For example, in some embodiments, the control 50 may provide the segmentation mode and segmentation configuration information via the data bus 44. Based on the envelope characteristic data, the controller 50 may configure the power management system 870A to operate in a high power modulation mode. (Step 1802).

[001381] In the high power modulation mode, the controller 50 may disable the first linear regulator 952, the low power differential to single ended converter 942, and the average power tracking controller circuit 944. (Step 1804).

[001382] The controller 50 may enable the programmable digital to analog converter 954 to generate a programmable reference voltage. The second linear regulator 952 may generate a second linear amplifier output voltage, V_{LDO2}, as a function of the programmable reference voltage and the battery voltage, V_{BAT}. (Step 1806).

[001383] The controller 50 may enable the digital filter 824 to generate the control signal 926. The controller 50 may configure the predistortion characteristics of a differential filter 824 to apply a maxium level of frequency response compensation to the differential V_{RAMP} signal to generate the control signal 926. (Step 1808).

[001384] The controller 50 may configure a switch mode power supply converter 872 based on expected high output power of the radio frequency power amplifier 869' to be transmitted. In the high power modulation mode, the switcher control circuit 880 enables the multi-level charge pump 882 and the driving circuit 842 to generate the switching voltage, V_{SW}. In some embodiments, the switcher control circuit 880 configures the multi-level charge pump 882 to generate all available "buck" level voltages and all available "boost" voltage levels. To improve efficiency in the high power modulation mode, the switcher control circuit 880 may inhibit the generation of "buck" voltage levels that are between the battery voltage, V_{BAT}, and ground to preserve the charge stored on a first flying capacitor 100 and a second flying capacitor 102 of the multi-level charge pump 882 for generation of the first boost voltage and the second boost voltage. average expected output power, P_{OUT_AVE}, the switcher control circuit 880 may determine a segmentation mode for the switching circuit 884. In some embodiments, the power management system 870A may receive a segmentation mode from a digital baseband processing portion of the transceiver or modem that provides the differential V_{RAMP} signal. The switcher control circuit 880 may generate a segmentation control signal 880A to enable operation

of all the sets of series switch and shunt switch pairs of the switching circuit 884 as a function of the segmentation mode. In some embodiments, the switcher control circuit may adjust the programmable delay period of the programmable delay circuitry 432 to offset at least a portion of any change in the temporal relationship between application of a current induced by the switching voltage, V_{SW}, and application of the high frequency ripple compensation current 416, I_{COR}, to the modulated power supply output 876. (Step 1810).

[001385] The power management system 870A may adjust the segmentation of a parallel amplifier output 928C and enable the parallel amplifier circuit output 872A. The power management system 870A may determine the segmentation configuration for the parallel amplifier 928. If the parallel amplifier includes an unsegmented output driver stage, the power management system 870A may not determine the segmentation configuration. To enable the parallel amplifier circuit output, the power management system 870A may set a parallel amplifier bypass switch 936 to open state. As a result, the coupling capacitor is decoupled from the ground. In addition, in some embodiments, the power management system 870A may set a first impedance, Z_1, of a first parallel amplifier feedback impedance 946 and a second impedance, Z_2 of a second parallel amplifier feedback impedance 948 to adjust a gain and a frequency response of the parallel amplifier 928 in order to compensate for the frequency response of the parallel amplifier 928 in the high power modulation mode. (Step 1812).

[001386] The power management system 870A may configure a μC charge pump circuit 262 to generate μC charge pump output voltage, $V_{\mu C_OUT}$, as a function of the battery voltage, V_{BAT}, the peak-to-peak swing of the power amplifier supply voltage, V_{CC_PKPK}. (Step 1914). In addition, the power management system 870A may configure the μC charge pump circuit 262 to generate μC charge pump output voltage, $V_{\mu C_OUT}$, to generate a target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$. If the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage threshold, the power management system 870A may further configure the μC charge pump circuit 262 to generate a

μC charge pump output voltage, $V_{\mu C_OUT}$, sufficient to provide a minimum CMOS logic supply voltage threshold, the power management system 870 may be configured to provide a CMOS logic circuit supply voltage, V_{CMOS}, to the CMOS logic supply input 869C that is at least equal to the minimum CMOS logic supply voltage. The controller may configure the supply selection switch 962 to provide the μC charge pump output voltage, $V_{\mu C_OUT}$, to the CMOS logic supply input 869C. In some embodiments, the controller 50 may configure the supply selection switch 962 to provide the battery voltage to the CMOS logic supply input 869C when the battery voltage, V_{BAT} is at least equal to the minimum CMOS logic supply voltage threshold. (Step 1814).

[001387] The power management system 870A may configure a first signal control signal multiplexer 964 to prove the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST,}$ to the switch mode power supply converter 876 as the switch mode power supply feedback signal 40A. (Step 1816).

[001388] The power management system 870A may configure a feedback delay compensation circuit 862 and active noise reduction circuit for the high power modulation mode. (Step 1818). As an example, in the high power modulation mode, the power management system 870A may configure the feedback delay compensation circuit 852 to operate as a function of a high power mode apparent gain to increase the aggressiveness of the feedback compensation provided by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. In addition, in some embodiments, the power management system may configure the active noise reduction circuit to provide a maximum level of noise reduction. As an example, the controller 50 may configure the open loop ripple compensation assist circuit 414 to generate and apply a medium frequency ripple compensation current 416, I_{COR}, based on the high power modulation mode I_{COR} transconductance value, $Gm_{ICOR_HIGH_POWER}$, to the modulated power supply output 876 to reduce the noise present in the receive channel of a band of operation. (Step 1820).

[001389] The V_{OFFSET} loop circuit 41 may be configured to determine whether the coupling capacitor 18A to operate in a pre-charge mode of operation prior to

the commencement of the data transmission. The V_{OFFSET} loop circuit 41 may compare the V_{OFFSET} error signal 304 to a maximum V_{OFFSET} error threshold parameter to determine whether the to operate in a pre-charge mode for a predetermined period of time. (Step 1822).

[001390] After the power management system 870A is configured to operate in the high power modulation mode, the modulated radio frequency input signal is provided to the radio frequency power amplifier 869' and the differential V_{RAMP} signal is provide to the switch mode power supply converter 872 and the parallel amplifier circuit 784'. In response to the differential V_{RAMP} signal and the modulated radio frequency input signal, the data transmission commences. The data may be transmitted in a data transmission slot. (Step 1824).

[001391] Figures 49A-B depict a method 1900 for configuring the pseudo-envelope tracking modulated power supply system 868A to operate in a medium power modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' to during a data transmission at less than the high power modulation mode threshold and at least substantially equal to a medium power modulation mode threshold. Some aspect of the method 1900 may be similar to the method 1500, depicted in Figures 44A-B, which depict a method for configuring the pseudo-envelope tracking modulated power supply system 868 and the power management system 870 to operate in a medium power modulation mode. Accordingly, an without intent to limit the scope of the method 1900, the description of the method 1900 may be described with continuing reference to the method 1500. In addition, the method 1900 is described with continuing reference to the various embodiments of the pseudo-envelope tracking modulated power supply system 868A, the power management system 870A, the switch mode power supply converter 872, and parallel amplifier circuit 874', depicted in Figures 46A-B, Figure 47, Figure 48A-B, Figure 49A-B, Figure 50A-B, and Figure 51.

[001392] Controller 50 may configure the power management system 870A to operate in a medium power modulation mode based on the determination that the expected output power of the radio frequency power amplifier 869' is less

than a high power modulation mode threshold and low power modulation mode threshold.

[001393] To configure the power management system 870A to operate in the medium power modulation mode, the controller 50 may determine or receive envelope characteristics data that describe the modulated radio frequency signal to be transmitted by the radio frequency power amplifier 869'. In other embodiments, the envelope characteristics data may further include parameters to configure the μC charge pump circuit 262 and the V_{OFFSET} control circuit 41. In some embodiments the power management system 870A or the controller 50 may receive a segmentation mode for configuring the switching circuit 884, a segmentation configuration for configuring the parallel amplifier 928, an average expected output power, P_{OUT_AVE}, to be generated by the radio frequency power amplifier 869'. In addition, based on the expected average expected output power, P_{OUT_AVE}, the power management system 870A determine whether to inhibit the operation of the multi-level charge pump 882 to only generate a first boost mode output voltage substantially equal to 3/2 x V_{BAT}. In addition, in some embodiments, the power management system 870A may further determine whether to inhibit the generation of the first buck mode output voltage substantially equal to 1/2 x V_{BAT} based on the average expected output power, P_{OUT_AVE}. Based on the envelope characteristic data, the power management system 870A may further determine whether to configure the power management system 870A to operate in the medium power modulation mode. (Step 1902).

[001394] The power management system 870A may enable the programmable digital to analog converter 954 to generate a programmable reference voltage. The second linear regulator 952 may generate a second linear amplifier output voltage, V_{LDO2}, as a function of the programmable reference voltage and the battery voltage, V_{BAT}. (Step 1904)

[001395] In the medium power modulation mode, the controller may disable the first linear regulator 952, the low power differential to single ended converter 942, and the average power tracking controller circuit 944. (Step 1906)

[001396] The power management system 870A may enable the digital filter 824 to generate the control signal 926. The power management system 870A may configure the predistortion characteristics of a differential filter 824 to apply a medium level of frequency response compensation to the differential V_{RAMP} signal to generate the control signal 926. (Step 1908).

[001397] The power management system 870A may configure the switch mode power supply converter 872 based on the expected medium output power to be generated by the radio frequency amplifier during the data transmission. (Step 1910). As an example, in the medium power modulation mode, the switcher control circuit 880 may enable the multi-level charge pump 882 and the driving circuit 842 to generate the switching voltage, V_{SW}. In some embodiments, the switcher control circuit 880 may only operate the multi-level charge pump 882 to generate a first boost level voltage substantially equal to 3/2 x V_{BAT} based on the average expected output power, P_{OUT_AVE}. In addition, the switcher control circuit 880 may configure the segmentation mode of the switching circuit 884 as a function of the average expected output power, P_{OUT_AVE}. In some embodiments, the power management system 870A may receive a segmentation mode from a digital baseband processing portion of the transceiver or modem that provides the differential V_{RAMP} signal. As an example, in some embodiments, the power management system 870A may compare the average expected output power, P_{OUT_AVE}, to set of switcher output power thresholds to determine the segmentation mode. The switcher control circuit 880 may generate a segmentation control signal 880A to enable operation of some or all of the sets of series switch and shunt switch pairs of the switching circuit 884 as a function of the segmentation mode. In some embodiments, the switcher control circuit may adjust the programmable delay period of the programmable delay circuitry 432 to offset at least a portion of any change in the temporal relationship between application of a current induced by the switching voltage, V_{SW}, and application of the high frequency ripple compensation current 416, I_{COR}, to the modulated power supply output 876 as a function of the segmentation mode. In some embodiments, the power management system 870A may

configure the switcher control circuit 880 to enable either 75% or 50% of the sets of series switches and shunt switches while operating in the medium power modulation mode as a function of the expected output power of the radio frequency power amplifier 869'.

[001398] The power management system 870A may adjust the segmentation of a parallel amplifier output 928C and enable the parallel amplifier circuit output 872A. (Step 1912). For example, the power management system 870A may determine the segmentation configuration for the parallel amplifier 928. If the parallel amplifier includes an unsegmented output driver stage, the power management system 870A may not determine the segmentation configuration. To enable the parallel amplifier circuit output, the power management system 870A may set a parallel amplifier bypass switch 936 to open state. As a result, the coupling capacitor is decoupled from the ground. In addition, in some embodiments, the power management system 870A may set a first impedance, Z_1, of a first parallel amplifier feedback impedance 946 and a second impedance, Z_2 of a second parallel amplifier feedback impedance 948 to adjust a gain and a frequency response of the parallel amplifier 928 in order to compensate for the frequency response of the parallel amplifier 928 in the high power modulation mode.

[001399] The power management system 870A may configure a μC charge pump circuit 262 to generate μC charge pump output voltage, $V_{\mu C_OUT}$, as a function of the battery voltage, V_{BAT}, the peak-to-peak swing of the power amplifier supply voltage, V_{CC_PKPK}. (Step 1914). In addition, the power management system 870A may configure the μC charge pump circuit 262 to generate μC charge pump output voltage, $V_{\mu C_OUT}$, to generate a target offset voltage, $V_{OFFSET_TARGET_EXPECTED}$. If the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage threshold, the power management system 870A may further configure the μC charge pump circuit 262 to generate a μC charge pump output voltage, $V_{\mu C_OUT}$, sufficient to provide a minimum CMOS logic supply voltage threshold, the power management system 870 may be configured to provide a CMOS logic circuit supply voltage, V_{CMOS}, to the CMOS

logic supply input 869C that is at least equal to the minimum CMOS logic supply voltage. The controller may configure the supply selection switch 962 to provide the μC charge pump output voltage, $V_{\mu C_OUT}$, to the CMOS logic supply input 869C. In some embodiments, the power management system 870A may configure the supply selection switch 962 to provide the battery voltage to the CMOS logic supply input 869C when the battery voltage, V_{BAT} is at least equal to the minimum CMOS logic supply voltage threshold.

[001400] The power management system 870A may configure a first signal control signal multiplexer 964 to prove the parallel amplifier circuit output current estimate 40, $I_{PAWA_OUT_EST,}$ to the switch mode power supply converter 876 as the switch mode power supply feedback signal 40A. (Step 1916).

[001401] The power management system 870A may configure a feedback delay compensation circuit 862 and active noise reduction circuit for the medium power modulation mode. (Step 1918). As an example, in the medium power modulation mode, the power management system 870A may configure the feedback delay compensation circuit 852 to operate as a function of a medium power mode apparent gain to increase the aggressiveness of the feedback compensation provided by the feedback delay compensation signal 854, $I_{FEEDBACK_TC}$. In addition, in some embodiments, the power management system may configure the active noise reduction circuit to provide a maximum level of noise reduction. As an example, the power management system 870A may configure the open loop ripple compensation assist circuit 414 to generate and apply a medium frequency ripple compensation current 416, I_{COR}, based on the medium power modulation mode I_{COR} transconductance value, $Gm_{ICOR_MEDIUM_POWER}$, to the modulated power supply output 876 to reduce the noise present in the receive channel of a band of operation.

[001402] The V_{OFFSET} loop circuit 41 may be configured to determine whether the coupling capacitor 18A to operate in a pre-charge mode of operation prior to the commencement of the data transmission. The V_{OFFSET} loop circuit 41 may compare the V_{OFFSET} error signal 304 to a maximum V_{OFFSET} error threshold

parameter to determine whether the to operate in a pre-charge mode for a predetermined period of time. (Step 1920).

[001403] After the power management system 870A is configured to operate in the medium power modulation mode, the modulated radio frequency input signal is provided to the radio frequency power amplifier 869' and the differential V_{RAMP} signal is provide to the switch mode power supply converter 872 and the parallel amplifier circuit 784'. In response to the differential V_{RAMP} signal and the modulated radio frequency input signal, the data transmission commences. The data may be transmitted in a data transmission slot. (Step 1922).

[001404] Figures 50A-B depict a method 2000 for configuring the pseudo-envelope tracking modulated power supply system 868A to operate in a medium power average power tracking modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' to during a data transmission at less than the medium power modulation mode threshold and at least substantially equal to a medium power average power tracking modulation mode threshold. The method 2000 is described with continuing reference to the various embodiments of the pseudo-envelope tracking modulated power supply system 868A, the power management system 870A, the switch mode power supply converter 872, and parallel amplifier circuit 874',depicted in Figures 46A-B, Figure 47, Figure 48A-B, Figure 49A-B, Figure 50A-B, and Figure 51. For the sake of convenience, and not by way of limitation, description of the method 2000 may refer to the power management system 870A.

[001405] To configure the power management system 870A to operate in the medium power average power tracking modulation mode, the power management system 870A may determine or receive envelope characteristics data that describe the modulated radio frequency signal to be transmitted by the radio frequency power amplifier 869'. In other embodiments, the envelope characteristics data may further include parameters to configure the μC charge pump circuit 262. For example, the envelope characteristics data may include the maximum expected power amplifier supply voltage, V_{CC_MAX}. Based on the

envelope characteristic data, the power management system 870A may further determine whether to configure the power management system 870A to operate in the medium power average power tracking modulation mode. (Step 2002).

[001406] The power management system 870A may disable the first linear regulator 950, LDO_1, and configure the first linear regulator output 874B to provide a high impedance path to ground. (Step 2004).

[001407] The power management system 870A may disable the programmable digital to analog converter 954. The power management system 870A may configure the second signal control multiplexer 956 to provide the V_{RAMP} signal to the non-inverting input of the second linear regulator 952, LDO_2. In response to the V_{RAMP} signal, the second linear regulator 952, LDO_2, may generate a second linear amplifier output voltage, V_{LDO2}, that is at least equal to the minimum driver supply voltage threshold as a function of the battery voltage, V_{BAT}, as described above. (Step 2006).

[001408] In the medium power average power tracking modulation mode, the power management system 870A may disable differential filter 942 and the parallel amplifier 928. The power management system 870A may configure the parallel amplifier output 928C to provide a high impedance path to ground. The power management system 870A may also enable the low power differential to single ended converter 942 to generate the V_{RAMP} signal as a function of the differential V_{RAMP} signal. (Step 2008)

[001409] The power management system 870A may configure the µC charge pump circuit 262 to generate µC charge pump output voltage, $V_{\mu C_OUT}$, as a function of the battery voltage, V_{BAT}. The power management system 870A may determine whether the battery voltage, V_{BAT}, is greater than a minimum CMOS logic supply voltage threshold. In response to a determination that the battery voltage, V_{BAT}, is at least equal to the minimum CMOS logic supply voltage threshold, the power management system 870A may configure the supply selection switch 962 to provide the battery voltage, V_{BAT}, to the CMOS logic supply input 869C. In response to a determination that the battery voltage, V_{BAT}, is near or less than the minimum CMOS logic supply voltage threshold, the

power management system 870A may configure the supply selection switch 962 to provide the μC charge pump output voltage, $V_{\mu C_OUT}$, to the CMOS logic supply input 869C. Based on the battery voltage, V_{BAT}, and the minimum CMOS logic supply voltage threshold, the power management system 870A configures the μC charge pump circuit 262 to generate μC charge pump output voltage, $V_{\mu C_OUT}$, having a lowest possible voltage that is at least equal to the minimum CMOS logic supply voltage threshold after accounting for losses between the μC charge pump circuit 262 and the CMOS logic supply input 869C. The clock management circuit 260 may disable the oscillator 270 , and generate a μC charge pump clock 276 based on the switching frequency of the switch mode power supply converter. (Step 2010).

[001410] The power management system 870A may set a parallel amplifier bypass switch 936 to a closed state to provide a low impedance path to ground. (Step 2012).

[001411] The power management system 870A may be configured to average power tracking circuit to control the switch mode power supply converter 2014. The power management system 870 may set the average power tracking transconductance, Gm_{APT}. (Step 2014).

[001412] The power management system 870A may set the average power tracking mode of operation as a function of the battery voltage, V_{BAT}, and the expected output power to be generated by the radio frequency power amplifier 869'. As an example, the power management system 879A may determine the maximum power amplifier supply voltage, V_{CC_MAX}, is expected to be generated based on the envelope characteristics of the modulate radio frequency input signal to be transmitted by the radio frequency power amplifier 869'. Based on a determination that the maximum power amplifier supply voltage, V_{CC_MAX}, is not greater than the battery voltage, V_{BAT}, less the headroom of the switching circuit 884, the power management system 870 may select an average power tracking "buck-buck" mode of operation to provide the modulated power supply voltage, V_{CC}, at the modulate power supply output 876. As an example, the head room of the headroom of the switching circuit 884 may be

between 100mV and 300mV. On the other hand, based on a determination that the maximum power amplifier supply voltage, V_{CC_MAX}, is greater than the battery voltage, V_{BAT}, less the headroom of the switching circuit 884, but maximum power amplifier supply voltage, V_{CC_MAX}, is does not exceed the battery voltage, V_{BAT}. The power management system 870 may select an average power tracking "buck-boost" mode of operation to provide the modulated power supply voltage, V_{CC}, at the modulate power supply output 876. As an example, the power management system 870 may select the First "Buck-Boost" Mode, where the first "bang-bang" switching voltage, V_{SW_BB1}, is substantially equal to zero volts and the second "bang-bang" switching voltage, V_{SW_BB2}, is substantially equal to 3/2 x V_{BAT}. In this case, the power management system 870 to operate in a low duty cycle. Yet, as another example, based on a determination that the maximum power amplifier supply voltage, V_{CC_MAX}, is exceeds the battery voltage, V_{BAT}, the power management system 870 may select the second "buck-boost" mode in order to benefit from a lower voltage change between the first "bang-bang" switching voltage, V_{SW_BB1}, and the second "bang-bang" switching voltage, V_{SW_BB2}, which will tend to reduce the ripple voltage or ripple currents generated at the modulated power supply output 867 and improve efficiency of the switch mode power supply coverter 872. (Step 2016)

[001413] The power management system 870A configure the first control signal multiplexer 964 to provide the average power tracking control signal 966 as the switch mode power supply feedback signal 40A. (Step 2018).

[001414] The power management system 870A configure the switch mode power supply converger 872 to operate in the selected average power tracking mode of operation. The power management system 870A may configure the switcher control circuit 880 to operate in a segmentation mode as a function of the average expected output power, P_{OUT_AVE}, a set of switcher output power thresholds. The set of switcher output power thresholds may be a function of the expected load line, $R_{RF_AMP_EXP}$, of the radio frequency power amplifier 869' and the selected the average power tracking mode of operation. In response, the switch mode power supply converter 872 may generate the switching voltage,

V_{SW}, in one of the average power tracking "buck-buck" modes and the average power tracking "buck-boost" modes based on the selected average power tracking "bang-bang" mode of operation. (Step 2020).

[001415] The power management system 870A may disable the V_{OFFSET} loop circuit 41 and any active noise reduction circuitry. (Step 2022).

[001416] After the power management system 870A is configured to operate in the medium power average power tracking modulation mode, the modulated radio frequency input signal may be provided to the radio frequency power amplifier 869', the switch mode power supply converter 872, and the parallel amplifier circuit 784'. In response to the differential V_{RAMP} signal and the modulated radio frequency input signal, the data transmission commences. The data may be transmitted in a data transmission slot. (Step 2024).

[001417] Figures 51 depict a method 2100 for configuring the pseudo-envelope tracking modulated power supply system 868A to operate in a low power average power tracking modulation mode based on a determination that the expected output power to be generated by the radio frequency power amplifier 869' to during a data transmission at less than the high power modulation mode threshold and at least substantially equal to a medium power modulation mode threshold. The method 2100 is described with continuing reference to the various embodiments of the pseudo-envelope tracking modulated power supply system 868A, the power management system 870A, the switch mode power supply converter 872, and parallel amplifier circuit 874', depicted in Figures 46A-B, Figure 47, Figure 48A-B, Figure 49A-B, Figure 50A-B, and Figure 51.

[001418] The power management system 870A may configure the power management system to operate in a low power average power tracking modulation mode in response to a determination that the expected output power of the radio frequency power amplifier 869 is less than the low power average power tracking modulation mode threshold. To configure the power management system 870A to operate in the low power modulation mode, the power managemen system 870A may determine or receive envelope

characteristics data that describe the modulated radio frequency signal to be transmitted by the radio frequency power amplifier 869'. In other embodiments, the envelope characteristics data may further include parameters to configure the μC charge pump circuit 262. (Step 2102).

[001419] The power management system 870A may enable the first parallel amplifier 950, LDO_1, to regulate the modulated power supply voltage, V_{CC}, as a function of the differential V_{RAMP} signal. The power management system 870A may configure the second signal control multiplexer 956 to provide the V_{RAMP} signal to the non-inverting input of the second linear regulator 952, LDO_2. In response to the V_{RAMP} signal, the second linear regulator 952, LDO_2, may generate a second linear amplifier output voltage, V_{LDO2}, as a function of the battery voltage, V_{BAT}. (Step 2104).

[001420] The power management system 870A may disable the parallel amplifier 928, and configure the parallel amplifier output 928C to provide a high impedance mode to ground. (Step 2106).

[001421] The power management system 870A may set the parallel amplifier output bypass switch 936 to be in a closed state. As a result, the negative terminal of the coupling capacitor 18A as short to ground. (Step 2108).

[001422] The power management system 870A may disable the switch mode power supply converter 872. For example, the switcher control circuit 880 may disable the multi-level charge pump 882 and the switching circuit 884. The switching voltage output 26 may provide a high impedance path to ground. (Step 2110).

[001423] The power management system 870A may also disabled any active noise reduction circuit while the power management system 870A is configured to operate in low power average power tracking modulation mode. For example, the power management system 870A may disable the open loop ripple compensation assist circuit 414. In addition, the power management system 870A may disable the V_{OFFSET} loop circuit 41 and the feedback delay compensation circuit 852 while in the low power average power tracking modulation mode. (Step 2112).

[001424] The power management system 870A may obtain an estimate of the battery voltage, V_{BAT}, from the battery level sense circuit 264. In addition, the power management system 870A may obtain or determine the maximum expected power amplifier supply voltage, V_{CC_MAX}, based on an envelope characteristic of the modulated radio frequency signal to be transmitted by the radio frequency power amplifier 869'. Based on the maximum expected power amplifier supply voltage, V_{CC_MAX}, the battery voltage, V_{BAT}, and the maximum headroom voltage of the first linear regulator 950, LDO_1, the power management system 870A may select a minimum value of the operational ratio of the μC charge pump, μBB_{RATIO}, to permit the first linear regulator 950, LDO_1, to generate the maximum expected power amplifier supply voltage, V_{CC_MAX}, during the data transmission. For example, the μC charge pump circuit 262 may typically operate in one of the 1/4 x V_{BAT} mode, 1/3 x V_{BAT} mode, or the 1/2 x V_{BAT} mode when the power management system 870A is configured to operate in the low power average power tracking modulation mode. (Step 2112). In addition, the power management system 870A may further determine whether the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage. Based on a determination that the battery voltage, V_{BAT}, is less than the minimum CMOS logic supply voltage, power management system 870A may determine a minimum value of the operational ratio of the μC charge pump, μBB_{RATIO}, from among the available operational ratios of the μC charge pump, μBB_{RATIO}, that would be at least equal to any losses through the power supply selection switch 962 to the CMOS logic supply input 869C plus the minimum CMOS logic supply voltage threshold. Thereafter, the power management system 870A configures the μC charge pump circuit 262 to generate a μC charge pump output voltage, $V_{\mu C_OUT}$, having the lowest voltage level that is sufficient to generate the maximum expected power amplifier supply voltage, V_{CC_MAX}, and at least equals the minimum CMOS logic supply voltage threshold plus any losses through the power supply selection switch 962 to the CMOS logic supply input 869C. The power management system 870A configures the power supply selection switch 962 to provide the μC charge pump output voltage, $V_{\mu C_OUT}$, to the CMOS

logic supply input 869C. The clock management system may enable the oscillator 270 to generate the μC charge pump clock 276. (Step 2114).

[001425] The power management system 870A may disable the differential filter 924, and configure the low power differential to single ended converter 942 to generate a V_{RAMP} signal configured for a no tracking mode of operation. (Step 2116). The digital base band processing portion of a transceiver/communication device may be configured to provide a differential V_{RAMP} signal that is substantially fixed direct current (DC) reference voltage to the power management system 870A. (Step 2118). Thereafter, the data transmission commences. (Step 2122). However, in some alternative embodiments of the power management system, such as those depicted in Figures 40D-E, and Figures 46H, the power management system 870A may enable the differential filter 924 to provide the control signal 926 with a low level of frequency response compensation or correction in the low power average tracking modulation mode. In this case, the power management system 870A may configure the differential filter 924 to provide the control signal 926, (Alternate Step 2116). The digital base band processing portion of a transceiver/communication device may be configured to provide a differential V_{RAMP} signal that provides for a slow tracking mode substantially fixed direct current (DC) reference voltage to the power management system 870A. (Step 2118). Thereafter, the data transmission commences. (Step 2122).

[001426] Figure 40D depicts an embodiment of a power management system 870B that is similar the power mangagement system 870A. For example, Figure 40D depicts an embodiment of a power management system 870B that includes the switch mode power suppy converter 872, an embodiment of the radio frequency power amplifier 869, a bypass capacitor array 19A, and an embodiment of a parallel amplifier circuit 874B'. The parallel amplifier circuit 874B' may be similar to the parallel amplifier circuit 874, depicted in Figure 40C. The parallel amplifier circuit 874B' may include an embodiment of a V_{OFFSET} loop circuit 41C and a grounding switch 937. The grounding

switch 937 may include a ground terminal coupled to ground and a switched terminal in communication with a bypass capacitor switch interface 984G.

[001427] The bypass capacitor array 19A may include a number of bypass capacitors. At least one of the number of bypass capacitors may be switchably coupled between the modulated power supply output 876 and ground. In some embodiments, at least one of the number of the bypass capacitors may be a switchably coupled bypass capacitor configured to be switchably coupled between the modulated power supply output 876 and ground. In some embodiments, the switchably coupled bypass capacitor may include a supply side terminal switchably coupled to the modulated power supply output 876 and a ground terminal coupled to ground. As an example, the bypass capacitory array may include a low resistance switch interposed between the supply side terminal and the modulated power supply output 876. The power management system 870B may configure the bypass capacitor array 19A to switchable couple the supply side terminal of the switchably coupled bypass capacitor to the modulated power supply output 876 as a function of the expected output power to be generated by the radio frequency power amplifier 869 to provide addition bypass capacitance in order to reduce a magnitude of a ripple voltage or noise at the collector voltage supply input 869A. In other embodiments, the switchably coupled bypass capacitor may include a supply side terminal switchably coupled to the modulated power supply output 876 and a ground terminal switchable coupled to ground. The power management system 870B may configure the bypass capacitor array 19A to switchable couple the ground terminal of the switchably coupled bypass capacitor to ground as a function of the expected output power to be generated by the radio frequency power amplifier 869 to provide addition bypass capacitance in order to reduce a magnitude of a ripple voltage or noise at the collector voltage supply input 869A. In other embodiments of the power management system 870B, the switchably coupled bypass capacitor may include a supply side terminal coupled to the modulated power supply output 876 and a ground terminal in communication with a bypass capacitor switch interface 984G. The power management system 870B may

configure the parallel amplifier circuit 874B' to close the grounding switch 937 as a function of the expected output power to be generated by the radio frequency power amplifier 869 to provide addition bypass capacitance in order to reduce a magnitude of a ripple voltage or noise at the collector voltage supply input 869A. In some embodiments, the bypass capacitor switch input 984G may be further configured couple two or more switchably coupled capacitor in the bypass capacitor array 19A. In addition, the grounding switch 937 may include a corresponding number of switched terminals that may each be independently controlled to couple each switchably coupled bypass capacitor to ground as a function of the expected output power to be generated by the radio frequency power amplifier 869.

[001428] The embodiments of a V_{OFFSET} loop circuit 41C may be configured to generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, in the medium power average power modulation mode to govern the generatation of the switching voltage, V_{SW}, by the switch mode power supply converter 872 in the medium power average power tracking mode.

[001429] In the medium power average power tracking mode, the V_{OFFSET} loop circuit 41C may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, as a function of the differential V_{RAMP} signal and the modulated power supply voltage, V_{CC}. For example, in the medium power average power tracking mode and the low power modulation mode, the power management system 870B' may enable the differential filter 842 to generate the control signal 926. In some embodiments, the control signal 926 may generate a V_{RAMP} signal without frequency response compensation or correction. The control signal 926 may be provided to the V_{OFFSET} loop circuit 41C.

[001430] In response to the control signal 926, the V_{OFFSET} loop circuit 41C may generate the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, when the switch mode power supply converter 872 is configured to operate in an averge power tracking "bang-bang" mode. For example, in some embodiments, the threshold offset current 42, $I_{THRESHOLD_OFFSET}$, may generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, substantially equivalent to the average power tracking control

signal 966. When the switch mode power supply converter is configured to operate in the average power tracking "buck-boost" mode, the V_{OFFSET} loop circuit 41C may generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, that is a measure of the average error voltage of the modulated power supply voltage, V_{CC}. In some embodiments of the power management system 870B, the V_{OFFSET} loop circuit 41C may generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, that is the measure of the average error voltage of the modulated power supply voltage, V_{CC}, when the switch mode power supply converter 872 is configured to operate in the average power tracking "buck-buck" mode.

[001431] As another alternative example, Figure 46E depicts an embodiment of a power management system 870E that is similar to the power management system 870A, depicted in Figures 46A-B. The power management system 870E may include an embodiment of the parallel amplifier circuit 874E that is similar to the embodiments of the parallel amplifier circuit 874', depicted in Figure 46B. The parallel amplifier circuit 874E' may include a V_{OFFSET} loop circuit 41C configured to govern generation of the switching voltage, V_{SW}, in a response to a determination to operate the power management system 870E in the medium power average power tracking modulation mode during a data transmission.

[001432] The low power differential to single ended converter 942 may be configured to generate a V_{RAMP} signal as a function of the differential V_{RAMP} signal in the medium power average power tracking mode, the low power average tracking mode, and the low power modulation mode. In the low power average power tracking modulation mode, the V_{OFFSET} loop circuit 41C may be configured to receive a V_{RAMP} signal from the low power differential to single ended converter 942. In response to the V_{RAMP} signal, the V_{OFFSET} loop circuit 41C may generate a threshold offset current 42, $I_{THRESHOLD_OFFSET}$, to govern generation of the switching voltage, V_{SW}, and regulate

[001433] Alternatively, as depicted in Figure 40E and Figures 46F-G, in the medium power average power tracking modulation mode, some embodiments of the parallel amplifier circuits 874C', 874F', and 874G' may disable any active noise reduction circuitry, and provide a modulation mode feedback signal from

the parallel amplifier feedback output 928E' as the switch mode power supply feedback signal 40A to regulate the operation of the switch mode power supply converter 872 in the average power tracking "buck-buck" mode of operation. As described below with respect to Figure 46C, the embodiments of a parallel amplifier 928' and a parallel amplifier 928" may be configured to generate the modulation mode feedback signal as a function of the differential V_{RAMP} signal and the modulated power supply voltage, V_{CC}, to control the generation of the switching voltage, V_{SW}, in the average power tracking "buck-buck" mode of operation. In the average power tracking "buck-buck" mode of operation, the controller 50 may configure the embodiments of the parallel amplifier 928' and a parallel amplifier 928" to generate a modulation mode feedback signal that is substantially equivalent to the averge power tracking control signal 966. In addition, the controller 50 may configure the embodiments of the parallel amplifier 928' and the parallel amplifier 928" to provide a high impedance path to ground at the parallel amplifier output 928C. The controller 50 may further configure the parallel amplifier circuit output 874A to provide a low impedance path to ground to provide additional filtering capacitance at the modulated power supply output 876 from the coupling capacitor 18A. Advantageously, the additional filtering capacitance may reduce the ripple voltage generated at the modulated power supply output 876 as a function of the switching voltage, V_{SW}. In the high power modulation mode and the medium power modulation mode, the controller 50 may configure the parallel amplifier 928' and the parallel amplifier 928" to generate the scaled parallel amplifier output current estimate, $I_{PARA_AMP_SENSE}$, from the parallel amplifier feedback output 928E'. Embodiments of the parallel amplifier 928' and the parallel amplifier 928" are described below with respect to Figure 46C.

[001434] Figure 52A, Figure 52B, Figure 52C, and Figure 52D depict a number of embodiments of a parallel amplifier 2300 operably disposed in a number of embodiments of the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A, depicted in Figure 30A, Figures 23A-D, Figure 24, Figures 34A-E,

Figures 40A-E, and Figures 46A-H. Each of the various embodiments of the parallel amplifier 2300 may include a segmented output driver stage having two or more output stage segments. Each of the two or more output stage segments may receive one of a set of supply voltages provided to the parallel amplifier 2300. In addition, some embodiments of the parallel amplifier 2300 may include three or more output stage segments.

[001435] The various embodiments of the parallel amplifier 2300 may include a parallel amplifier 2300A, depicted in Figure 52A, a parallel amplifier 2300B, depicted in Figure 52B, a parallel amplifier 2300C, depicted in Figure 52C, and a parallel amplifier 2300D, depicted in Figure 52D. The example embodiments of the parallel amplifier 2300A, 2300B, 2300C, and 2300D are described with continuing reference to the embodiments of the power management systems 870, 870A-870C, and 870E-870H, depicted in Figures 40A-E, Figures 46A-B, and Figures 46E-H, and the parallel amplifier 35G, depicted in Figure 12G.

[001436] Example embodiments of the parallel amplifier 2300 may include a parallel amplifier 2300A, depicted in Figure 52A, a parallel amplifier 2300B, depicted in Figure 52B, a parallel amplifier 2300C, depicted in Figure 52C, and a parallel amplifier 2300D, depicted in Figure 52D. The example embodiments of the parallel amplifier 2300A, 2300B, 2300C, and 2300D are described with continuing reference to the embodiments of the power management systems 870, 870A-870C, and 870E-870H, depicted in Figures 40A-E, Figures 46A-B, and Figures 46E-H, and the parallel amplifier 35G, depicted in Figure 12 G.

[001437] Figure 52A depicts an embodiment of the parallel amplifier 2300A that is similar to embodiment of the parallel amplifier 35G. Advantageously, the parallel amplifier 2300A may further provide a separate supply voltage for each of the output stage segments in order to reduce the overall energy drained from the battery 20 during a data transmission.

[001438] Figure 52B depicts an example embodiment of a parallel amplifier 2300B having two output stage segments. Each of the two or more

output segments may receive a respective supply voltage from a set of supply voltages provided to the parallel amplifier by a charge pump 2390B configured to provide two output voltages derived from the battery voltage, V_{BAT}. In some embodiments, the charge pump 2390B may further provide the battery voltage, V_{BAT}, as the voltage level for one of the two output voltages or as a third output voltage. Similarly, Figure 52C depicts a parallel amplifier 2300C having two output stage segments, where each output stage segment of the two output segments is in communication with one of the two output voltages provided by the charge pump 2390B. Figure 52C depicts the parallel amplifier 2300C having one output stage segment configured to receive a supply voltage form the µC charge pump circuit 262' and a second output stage segment configured to receive the battery voltage, V_{BAT}. The µC charge pump circuit 262' is substantially similar in form and function to the embodiments of the µC charge pump circuit 262 depicted in Figures 19A-B, Figures 40C-E, Figure 46B, and Figures 46E-H. For the sake of description, the µC charge pump circuit 262' is substantially the same as the operation of the µC charge pump circuit 262 except the µC charge pump output voltage generated by µC charge pump circuit 262' is labeled $V_{FIRST-OUTPUT}$, whereas the µC charge pump output voltage for the µC charge pump circuit 262 is labled $V_{\mu C_OUT}$. The changes in names for the µC charge pump output voltage is by way of conventinence and not by limitation and to provide the reader with a consistent correspondence between the various embodiments of the charge pump 2390A, the charge pump 2390B, and the µC charge pump circuit 262'.

[001439] Returning to Figure 52A, the parallel amplifier 2300A may include a first control input 2302, a second control input 2304, a parallel amplifier output 2306, and a control interface 2308. The controller 50 may be configured to interface with the control interface 2308 to configure and control the operation of the parallel amplifier 2300A. As an example, in some embodiments, the controller 50 may communicate with the control interface 2308 via a control bus 44. The controller 50 may provide control settings, configuration parameters, and threshold parameters to the parallel amplifier 2300A. In addition, the

controller 50 may be configured to both read and write the control settings, configuration parameters, and threshold parameters from the control interface 2308. For example, the controller 50 may provide one or more configuration parameters to the control interface 2308, which may store the control parameters in local parameter registers. As an example, based on the control parameters, the control interface 2308 may generate a configuration signal 2310 and a threshold signal 2312. Alternatively, in some embodiments, the controller 50 may generate the configuration signal 2310 and a threshold signal 2312. The parallel amplifier 2300A may further include a supply voltage interface 2314 configured to receive two or more supply voltages. In addition, in some embodiments, the first control input 2302 and the second control input 2304 provide a high input impedance input. For example, the first control input 2302 and the second control input 2304 may be a differential input configured to provide a high impedance input. For example, the first control input 2302 may be a non-inverting input. The second control input 2304 may be an inverting input. As a further example, the first control input 2302 and the second control input 2304 may be a non-inverting input and an inverting input of a class AB amplifier, respectively.

[001440] As an example, in some embodiments, the first control input 2302 may receive a target voltage for the modulated power supply voltage, V_{CC}. The target voltage for the modulated power supply voltage, V_{CC}, may be a V_{RAMP} signal. For example, the low power differential to signal-ended converter 942 may generate the V_{RAMP} signal in response to a differential V_{RAMP} signal. As another example, the first control input 2302 may receive the control signal 926 generated by the differential filter 924 in response to the differential V_{RAMP} signal. The second control input 2304 may be in communication with the modulated power supply output 876, and configured to receive the modulated power supply voltage, V_{CC}. The parallel amplifier 2300 may generate the parallel amplifier output current, I_{PARA_AMP}, as a function a difference voltage between the first control input 2302 and the second control input 2304. The parallel amplifier 2300A may apply the

parallel amplifier output current, I_{PARA_AMP}, to the parallel amplifier output 2306 to generate a parallel amplifier output voltage, V_{PARA_AMP}.

[001441] As depicted in Figures 52A-D, each of the two or more output stage segments may receive a number of supply voltages from a variety of voltage sources. As a non-limiting example, embodiments of the voltage sources may include some combination of a battery voltage, V_{BAT}, from a battery 20, boost supply voltages generated by various embodiments of charge pumps as a function of the battery voltage, V_{BAT}, and a number of buck supply voltages generated by various embodiments of charge pumps as a function of the battery voltage, V_{BAT}. In addition, the supply voltages provided to each of the two or more output stage segments may change as a function of the expected output power to be generated by a radio frequency power amplifier 869' and the battery voltage, V_{BAT}. The supply voltages provided to each of the two or more output stage segments may change for each data transmission as a function of an expected output power to be generated by the radio frequency power amplifier 869'.

[001442] Each of the two or more output stage segments may include a first transistor in communication with a respective one of the supply voltages, and a parallel amplifier output of the parallel amplifier 2300, and configured to source current from the respective one of the supply voltages to the parallel amplifier output of the parallel amplifier 2300 to generate a parallel amplifier output current, I_{PARA_AMP}, as a function of the parallel amplifier output voltage, V_{PARA_AMP}, a headroom voltage of the first transistor, a voltage level of the respective one of the supply voltages, and a relative magnitude of the voltage level of the respective one of the supply voltage to the other supply voltages. For example, the parallel amplifier 2300 may be configured to compare the parallel amplifier output voltage, V_{PARA_AMP}, to one or more threshold levels to determine which of the two or more output stage segments to enable to generate the parallel amplifier output current, I_{PARA_AMP}.

[001443] To determine the one or more thresholds, a controller 50 may determine a relative magnitude of each supply voltage of the supply voltages

associated with a respective one of the two or more output stage segments. The controller 50 sets a first threshold level of the one or more threshold levels to substantially equal a smallest supply voltage of the one of the supply voltages having the smallest magnitude less the headroom of the first transistor of the respective one of the two or more output stage segments that receives the smallest supply voltage. The parallel amplifier 2300 may enable the respective one of the one of the two or more output stage segments that receives the smallest supply voltage to generate the parallel amplifier output current, I_{PARA_AMP}, so long as the parallel amplifier output voltage, V_{PARA_AMP}, is less than the first threshold. The controller 50 may set a second threshold level of the one or more threshold levels to substantially equal the second smallest supply voltage of the two or more output stage segments less the headroom of the first transistor of output stage segment of the two or more output stage segments communication with the second smallest supply voltage. The parallel amplifier 2300 may enable the respective one of two or more output stage segments that receives the second smallest supply voltage to generate the parallel amplifier output current, I_{PARA_AMP}, so long as the parallel amplifier output voltage, V_{PARA_AMP}, is at least substantially equal to the first threshold and less than the second threshold. Similarly, the controller 50 may set a third threshold level of the one or more threshold levels to substantially equal the third smallest supply voltage of the two or more output stage segments less the headroom of the first transistor of the output stage segment of the two or more output stage segments in communication with the third smallest supply voltage. The parallel amplifier 2300 may enable the respective one of the two or more output stage segments that receives the third smallest supply voltage to generate the parallel amplifier output current, I_{PARA_AMP}, so long as the parallel amplifier output voltage, V_{PARA_AMP}, is at least substantially equal to the second threshold and less than the third threshold. Subsequent threshold levels may be determined by the controller 50 for each of the two or more output stage segments. The parallel amplifier 2300 may enable the respective one of the two or more output stage segments that receives the largest supply voltage to generate the parallel

amplifier output current, I_{PARA_AMP}, so long as the parallel amplifier output voltage, V_{PARA_AMP}, is at least equal to the n^{th} threshold where the two or more output stage segments include (n+1) segments configured to receiver (n+1) supply voltages.

[001444] In some embodiments of the parallel amplifier 2300, each of the two or more output stage segments may include a second transistor in communication with the parallel amplifier output of the parallel amplifier 2300 and a common voltage level, such as ground. For each of the two or more output stage segments, the second transistor may be configured to sink current to generate the parallel amplifier output current, I_{PARA_AMP}, as a function of the parallel amplifier output voltage, V_{PARA_AMP}, the headroom voltage of the first transistor of the respective segment, the voltage level of the respective one of the supply voltages received by the first transistor of the respective segment, and the relative magnitude of the voltage level of the respective one of the supply voltages received by the first transistor of the respective segment to the other supply voltages. The parallel amplifier 2300 may enable each of the two or more output stage segments to generate the parallel amplifier output current, I_{PARA_AMP}, in a mutually exclusive manner such that only one of the two or more output stage segments is enabled at any one time. The second transistor of a respective output stage segment of the two or more output stage segments may sink a bias current associated with the respective segment while the segment is in a standby mode of operation. The segment may be in a standby mode of operation when not configured to generate parallel amplifier output current, I_{PARA_AMP}.

[001445] Other embodiments of the parallel amplifier 2300 may include a shared or common transistor in communication with the parallel amplifier output of the parallel amplifier 2300 and the common voltage level. The shared or common transistor may sink current to generate the parallel amplifier output current, I_{PARA_AMP}, for each of two or more output stage segments. In other words, because the parallel amplifier 2300 may enable each of the two or more output stage segments to generate the parallel amplifier output current, I_{PARA_AMP}, in a

mutually exclusive manner such that only one of the two or more output stage segments is a enabled at any one time, a shared or common transistor may sink current to generate the parallel amplifier output current, I_{PARA_AMP}, for each of the two or more output stage segments. In addition, the shared or common transistor may sink a respective bias current for each of the two or more output stage segments that are in a standby mode of operation.

[001446] For example, Figure 52A depicts a parallel amplifier 2300A having three or more output stage segments. Each of the three or more output stage segments may receive a respective supply voltage from a set of supply voltages provided to the parallel amplifier by a charge pump 2390A configured to provide three output voltages derived from the battery voltage, V_{BAT}. In some operational configurations, the charge pump 2390A may provide the battery voltage, V_{BAT}, as one of the three output voltages. The controller 50 may configure the charge pump 2390A to generate specific output voltages depending on the battery voltage, V_{BAT}, the maximum expected parallel amplifier supply voltage, V_{CC_MAX}, to be generated by the modulated power supply output 876, the minimum CMOS logic power supply threshold, and the minimum driver supply voltage of the driver 869F provided to the driver supply voltage input 869D of the radio frequency power amplifier 869'. In some embodiments, the charge pump 2390A may provide a fourth output voltage substantially equal to the battery voltage, V_{BAT}. Furthermore, depending on the various supply voltages needed by the parallel amplifier 2300 to regulate the modulated power supply output 876, the battery voltage, V_{BAT}, and the minimum supply voltage for the driver supply voltage input 869D, the controller 50 may configure the charge pump 2390A to generate a set of supply voltages that minimizes the overall expected energy drawn from the battery 20 during a data transmission. Some embodiments of the charge pump 2390A receive a µC charge pump clock 276 from the clock management circuit 260. In some embodiments, the µC charge pump clock 276 may be derived from the switching frequency of the switch mode power supply converter 872. In other embodiments or configurations, the µC charge pump clock 276 may be derived from an oscillator 270, which is enabled when the

switch mode power supply converter 872 is disabled. Based on the μC charge pump clock 276, the charge pump 2390A may operate in a number of phases, described below in further detail, to generate a first output voltage $V_{FIRST-OUTPUT}$ provided at the first output 2394 of the charge pump 2390A, the second output voltage $V_{SECOND-OUTPUT}$ provided at the second output 2396 of the charge pump 2390A, and the third output voltage $V_{THIRD-OUTPUT}$ at the third output 2398. The controller 50 may determine a first threshold level and a second threshold level to be used by the comparator circuitry 2318A to control the operation of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350.

[001447] During operation, the controller 50 may enable the pre-amplifier 2316 and the comparator circuitry 2318A. The pre-amplifier 2316 may generate a first amplifier output voltage, V_A, and a second amplifier output voltage, V_B, in response to the difference voltage between the first input 2324 and the second input 2326 of the pre-amplifier 2316. The comparator circuitry 2318A compares the parallel amplifier output voltage, V_{PARA_AMP}, to the first threshold and the second threshold. If the parallel amplifier output voltage, V_{PARA_AMP}, is less than the first threshold, the comparator circuitry 2318A determines which to the first supply voltage 2376, the second supply voltage 2378, and the third supply voltage 2380 has the least magnitude. Comparator circuitry 2318A may enable the one of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 that is associated with the one of the first supply voltage 2376, the second supply voltage 2378, and the third supply voltage 2380 having the least magnitude so long as the parallel amplifier output voltage, V_{PARA_AMP}, is less than the first threshold. The comparator circuitry 2318A enables the one of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 that is associated with the one of the first supply voltage 2376, the second supply voltage 2378, and the third supply voltage 2380 having the maximum magnitude so long as the parallel amplifier output voltage, V_{PARA_AMP}, is greater than the third threshold. Otherwise, the comparator circuitry 2318A

enables the one of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 that is associated with the one of the first supply voltage 2376, the second supply voltage 2378, and the third supply voltage 2380 having the middle range magnitude so long as the parallel amplifier output voltage, V_{PARA_AMP}, is at least equal to the first threshold and not more than the second threshold level.

[001448] The parallel amplifier 2300A may further include a pre-amplifier 2316, comparator circuitry 2318A, and a segmented output driver stage 2320A. The pre-amplifier 2316 may include a first input 2324 in communication with the first control input 2302, a second input 2326 in communication with the second control input 2304, and a control input 2328 in communication with a control interface 2308. The control input 2328 may receive the configuration signal 2310 from the control interface 2308. The pre-amplifier 2316 may further include a first pre-amplifier output 2330 and a second pre-amplifier output 2332 configured to respectively generate a first amplifier output voltage, V_A, and a second amplifier output voltage, V_B, in response to the difference in voltage between the first input 2324 and the second input 2326 of the pre-amplifier 2316. The first pre-amplifier output 2330 and the second pre-amplifier output 2332 may drive the segmented output driver stage 2320.

[001449] The comparator circuitry 2318A may include a control input 2334 configured to receive the configuration signal 2310 and a threshold input 2336 configured to receive the threshold signal 2312 from the control interface 2308. The comparator circuitry 2318 may further include a parallel amplifier output voltage input 2338 configured to receive the parallel amplifier output voltage, V_{PARA_AMP}, from the parallel amplifier output 2306. The comparator circuitry 2318A may include a first segment control output 2340, a second segment control output 2342, and a third segment control output 2344. As described below, the comparator circuitry 2318A may be configured to control the generation of the parallel amplifier output current, I_{PARA_AMP}, as a function of the parallel amplifier output voltage, V_{PARA_AMP}, a first threshold level, and a second threshold level.

[001450] The segmented output driver stage 2320 may include the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350. The first push-pull output stage 2346 may include a first PFET transistor 2352 and a first NFET transistor 2354. The second push-pull output stage 2348 may include a second PFET transistor 2356 and a second NFET transistor 2358. The third push-pull output stage 2350 may include a third PFET transistor 2360 and a third NFET transistor 2362. The drains of the first PFET transistor 2352, the first NFET transistor 2354, the second PFET transistor 2356, the second NFET transistor 2358, the third PFET transistor 2360, and the third NFET transistor 2362 may be operably coupled or combined to form the parallel amplifier output 2306. The sources of the first NFET transistor 2354, the second NFET transistor 2358, and the third NFET transistor 2362 may be operably coupled to ground.

[001451] The segmented output driver stage 2320 may further include a first switch element 2364, a second switch element 2366, a third switch element 2368, a fourth switch element 2370, a fifth switch element 2372, and a sixth switch element 2374. Each of the first switch element 2364, the second switch element 2366, the third switch element 2368, the fourth switch element 2370, the fifth switch element 2372, and the sixth switch element 2374 may include a first terminal, a second terminal and a control terminal, and configured to have an on state and an off state. The first pre-amplifier output 2330 may be in communication with the first terminal of the first switch element 2364, the third switch element 2368, and the fifth switch element 2372. The first segment control output 2340 may be in communication with the control terminal of the first switch element 2364 and the control terminal of the second switch element 2366. The second segment control output 2342 may be in communication with the third switch element 2368 and the fourth switch element 2370. The third segment control output 2344 may be in communication with the fifth switch element 2372 and the sixth switch element 2374. The gate of the first PFET transistor 2352 may be in communication with the second terminal of the first switch element 2364. The gate of the first NFET transistor 2354 may

be in communication with the second terminal of the second switch element 2366. The gate of the second PFET transistor 2356 may be in communication with second terminal of the third switch element 2368. The gate of the second NFET transistor 2358 may be in communication with the second terminal of the fourth switch element 2370. The gate of the third PFET transistor 2360 may be in communication with the second terminal of the fifth switch element 2372. The gate of the third NFET transistor 2362 may be in communication with the second terminal of the sixth switch element 2374.

[001452] The control interface 2308 may be in communication with the controller 50. The control interface 2308 may include a configuration signal 2310 and a threshold signal 2312. As an example, the control input of the pre-amplifier 2316 may receive a configuration signal 2310. The configuration signal 2310 may include a pre-amplifier enable signal and a comparator circuitry control signal. The controller 50 may assert the comparator circuitry control signal to enable the comparator circuitry 2318A. The controller 50 may de-assert the comparator circuitry control signal to disable the comparator circuitry 2318A. In the disabled state, the comparator circuitry 2318 may default to an output state that configures each of the first switch element 2364, the second switch element 2366, the third switch element 2368, the fourth switch element 2370, the fifth switch element 2372, and the sixth switch element 2374 to disable the first PFET transistor 2352, the first NFET transistor 2354, the second PFET transistor 2356, the second NFET transistor 2358, the third PFET transistor 2360, and the NFET transistor 2362. As a result, the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 are each disabled and provide a high impedance path to ground. Accordingly, the parallel amplifier output 2306 presents a high impedance path to ground.

[001453] The source of the first PFET transistor 2352 may receive a first supply voltage 2376. The source of the second PFET transistor 2356 may receive a second supply voltage 2378. The source of the third PFET transistor 2360 may receive a third supply voltage 2380. As an example, in some embodiments, the supply voltage interface 2314 may receive the first supply voltage 2376, the

second supply voltage 2378, and a third supply voltage 2380 from the charge pump 2390A.

[001454] Some embodiments of the charge pump 2390A may receive the battery voltage, V_{BAT}, from the battery 20. The charge pump 2390A may include a first output 2394 configured to provide the first supply voltage 2376, a second output 2396 configured to provide the second supply voltage 2378, and a third output 2398 configured to provide the third supply voltage 2380 to the supply voltage interface 2314. In addition, the charge pump 2390A may be in communication with a controller 50 via the control bus 44. The controller 50 may provide a set of programming parameters 2392 to the charge pump 2390A. The controller 50 may generate the programming parameters 2392 as a function of the battery voltage, V_{BAT}, and the maximum expected parallel amplifier supply voltage, V_{CC_MAX}. In response to receipt of the programming parameters, the charge pump 2390A may generate a set of output voltages based on the programming parameters 2392.

[001455] For example, based on the programming parameters 2392, the charge pump 2390A may generate a first output voltage, $V_{FIRST\text{-}OUTPUT}$, at the first output 2394, a second output voltage, $V_{SECOND\text{-}OUTPUT}$, at the second output 2396, and a third output voltage, $V_{THIRD\text{-}OUPUT}$, at the third output 2398.

[001456] Based on the first output voltage $V_{FIRST\text{-}OUTPUT}$ provided at the first output 2394, the second output voltage $V_{SECOND\text{-}OUTPUT}$ provided at the second output 2396, and the third output voltage $V_{THIRD\text{-}OUPUT}$ at the third output 2398, the controller 50 may determine a first threshold level and a second threshold level to be used by the comparator circuitry 2318A to control the operation of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350.

[001457] Some embodiments of the charge pump 2390A may be configured to generate a buck output voltage, or a boost voltage that is greater than the battery voltage, V_{BAT}, and/or some combination thereof. In the case where the operational ratio of the µC charge pump, μBB_{RATIO}, results in one of the first output voltage, $V_{FIRST\text{-}OUTPUT}$, the second output voltage, $V_{SECOND\text{-}OUTPUT}$, and

the third output voltage, $V_{THIRD-OUPUT}$, being below the minimum expected power amplifier supply voltage, V_{CC_MIN}, the controller 50 may configure the charge pump 2390A to bypass the switching network 2412 to provide an output voltage substantially equal to the battery voltage, V_{BAT}.

[001458] The controller 50 may set the voltage levels of the output voltage $V_{FIRST-OUTPUT}$, the second output voltage $V_{SECOND-OUTPUT}$, and the third charge pump output voltage $V_{THIRD-OUTPUT}$ based on the envelope characteristic of the modulated radio frequency input signal provided to the radio frequency power amplifier 869' such that the parallel amplifier 2300A may generate a maximum power amplifier supply voltage, V_{CC_MAX}. In addition, referring to Figure 42, the controller 50 may further determine whether the battery voltage is greater than the minimum CMOS supply voltage threshold. In the case where the battery voltage, V_{BAT}, is less than the minimum CMOS supply voltage threshold, the controller 50 may configure the charge pump 2390A to generate at least one of the first output voltage $V_{FIRST-OUTPUT}$, the second output voltage $V_{SECOND-OUTPUT}$, and the third output voltage $V_{THIRD-OUTPUT}$ that is greater than the minimum CMOS supply voltage threshold, which is provided to the radio frequency power amplifier 869 or 869' as previously described. Similarly, based on the expected output power to be generated by the radio frequency power amplifier 869 or 869', the controller 50 may configure one of the first output voltage $V_{FIRST-OUTPUT}$, the second output voltage $V_{SECOND-OUTPUT}$, and the third output voltage $V_{THIRD-OUTPUT}$ to provide a supply voltage to the second linear regulator, V_{LDO2}, at least equal to the minimum driver supply voltage threshold of the driver 869F of the radio frequency power amplifier 869'.

[001459] As an example, and not by way of limitation, the following description of the operation of the comparator circuit assumes that the $V_{FIRST-OUTPUT} < V_{SECOND-OUTPUT} < V_{THIRD-OUTPUT}$. As depicted in Figure 52A, the first output voltage $V_{FIRST-OUTPUT}$ is received by the first PFET transistor 2352, the second output voltage $V_{SECOND-OUTPUT}$ is received by the second PFET transistor 2356, and the third output voltage $V_{THIRD-OUTPUT}$ is received by the third PFET transistor 2360. The controller 50 may set the first threshold level substantially

equal to the $V_{FIRST-OUTPUT}$ less the headroom voltage of the first PFET transistor 2352, $V_{HEADROOM-FIRST-PFET}$. The controller 50 may set the second threshold level substantially equal to the second output voltage $V_{SECOND-OUTPUT}$ less the headroom voltage of the second PFET transistor 2356, $V_{HEADROOM-SECOND-PFET}$.

[001460] The controller 50 may communicate the first threshold level and the second threshold level to the comparator circuitry 2318A via the control bus 44. In addition, in some embodiments, the controller 50 may configure the comparator circuitry 2318A to compare the parallel amplifier output voltage, V_{PARA_AMP} to the first threshold and the second threshold to govern the operation of the first segment control output 2340, the second segment control output 2342, and the third segment control output 2344.

[001461] Because the first output voltage $V_{FIRST-OUTPUT}$ has the least magnitude, the comparator circuitry 2318A may activate the first segment control output 2340 to enable the first PFET transistor 2352 and the first NFET transistor 2354 to generate the parallel amplifier output current, I_{PARA_AMP}, so long as the parallel amplifier output voltage, V_{PARA_AMP}, is less than the first threshold. For example, the first segment control output 2340 may generate a control signal to configure the first switch element 2364 to provide the first amplifier output voltage, V_A, to the gate of the first PFET transistor 2352, and a second switch element 2366 to provide a second amplifier output voltage, V_B, to the gate of the first NFET transistor 2354. When the parallel amplifier output voltage, V_{PARA_AMP}, rises above the first threshold, the comparator circuitry 2318A may configure the first segment control output 2340 to place the first switch element 2364 and the second switch element 2366 in a standy mode or bias mode of operation. In addition, the comparator circuitry 2318A may activate the second segment control output 2342 to enable the second PFET transistor 2356 and the first NFET transistor 2354 to generate the parallel amplifier output current, I_{PARA_AMP}, so long as the parallel amplifier output voltage, V_{PARA_AMP}, is between the first threshold and the second threshold. For example, the second segment control output 2342 may generate a control signal to configure the third switch element

2368 to provide the first amplifier output voltage, V_A, to the gate of the second PFET transistor 2356, and a fourth switch element 2370 to provide the second amplifier output voltage, V_B, to the gate of the second NFET transistor 2358.

[001462] When the parallel amplifier output voltage, V_{PARA_AMP}, rises above the second threshold, the comparator circuitry 2318A may configure the second segment control output 2342 to place the third switch element 2368 and the fourth switch element 2370 in a standy mode or bias mode of operation. In addition, the comparator circuitry 2318A activate the third segment control output 2342 to enable the third PFET transistor 2360 and the third NFET transistor 2362 to generate the parallel amplifier output current, I_{PARA_AMP}, so long as the parallel amplifier output voltage, V_{PARA_AMP}, is at least equal to the second threshold. For example, the third segment control output 2344 may generate a control signal to configure the fifth switch element 2372 to provide the first amplifier output voltage, V_A, to the gate of the third PFET transistor 2360, and a third switch element 2374 to provide the second amplifier output voltage, V_B, to the gate of the third NFET transistor 2362. When the parallel amplifier output voltage, V_{PARA_AMP}, is less than equal to the second threshold, the comparator circuitry 2318A may configure the third segment control output 2344 to place the fifth switch element 2372 and the sixth switch element 2374 in a standy mode or bias mode of operation. In a standby mode or bias mode of operation, the first switch element 2364 and the second switch element 2366 may provide a gate voltage to the first PFET transistor 2352 and a gate voltage to the first NFET transistor 2354 to generate a first bias current through the first PFET transistor 2352 and the first NFET transistor 2354. In a standby mode or bias mode of operation, the third switch element 2368 and the fourth switch element 2370 may provide a gate voltage to the second PFET transistor 2356 and a gate voltage to the second NFET transistor 2358 to generate a second bias current through the second PFET transistor 2356 and the second NFET transistor 2358. Likewise, in a standby mode or bias mode of operation, the fifth switch element 2372 and the sixth switch element 2374 may provide a gate voltage to the third PFET transistor 2360 and a gate voltage to the third NFET

transistor 2362 to generate a third bias current through the third PFET transistor 2360 and the third NFET transistor 2362.

[001463] The magnitude of the first bias current may be a function of a source voltage on the source of the first PFET transistor 2352. The magnitude of the second bias current may be a function of a source voltage on the source of the second PFET transistor 2356. The magnitude of the third bias current may be a function of a source voltage on the source of the third PFET transistor 2360.

[001464] In the example case where the first output voltage $V_{FIRST-OUTPUT}$ is less than the second output voltage $V_{SECOND-OUTPUT}$, and the second output voltage $V_{SECOND-OUTPUT}$ is less than the third output voltage $V_{THIRD-OUTPUT}$, the bias current through the first PFET transistor 2352 may be less than a second bias current generated by the second PFET transistor 2356. Similarly, the second bias current generated by the second PFET transistor 2356 may be less than a third bias current generated by the third PFET transistor 2360.

[001465] In addition, in some embodiments, the comparator circuitry 2318A may configure the first segment control output 2340 to turn off first PFET transistor 2352 and the first NFET transistor 2354. For example, the first segment control output 2340 may provide a control signal to configure the first switch element 2364 and the second switch element 2366 to put the first PFET transistor 2352 and the first NFET transistor 2354 in a non-conducting state. The first PFET transistor 2352 and the first NFET transistor 2354 may provide a high impedance path to ground in the non-conducting state. Likewise, the comparator circuitry 2318A may configure the second segment control output 2342 to turn off second PFET transistor 2356 and the second NFET transistor 2358. For example, the second segment control output 2342 may provide a control signal to configure the third switch element 2368 and the fourth switch element 2370 to put the second PFET transistor 2356 and the second NFET transistor 2358 in a non-conducting state. The second PFET transistor 2356 and the second NFET transistor 2358 may provide a high impedance path to ground in the non-conducting state. The comparator circuitry 2318A may further configure the third segment control output 2344 to turn off third PFET transistor 2360 and the third

NFET transistor 2362. For example, the third segment control output 2344 may provide a control signal to configure the fifth switch element 2372 and the sixth switch element 2374 to put the third PFET transistor 2360 and the third NFET transistor 2362 in a non-conducting state. The third PFET transistor 2360 and the third NFET transistor 2362 may provide a high impedance path to ground in the non-conducting state.

[001466] In addition, in some embodiments of the parallel amplifier 2300A, the comparator circuitry 2318A may be configured to receive and use the target voltage for the modulated power supply voltage, V_{CC}, received by the first control input 2302 to determine when to enable each of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 to generate the parallel amplifier output current, I_{PARA_AMP}. As discussed above, the first control input 2302 may receive the V_{RAMP} signal or the control signal 926 generated in response to the differential V_{RAMP} signal. Advantageously, both the V_{RAMP} signal and the control signal 926 may provide a time advanced control signal that may be used to determine which of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 to enable to generate the parallel amplifier output current, I_{PARA_AMP}. Because both the V_{RAMP} signal and the control signal 926 are time advance relative to the parallel amplifier output voltage, V_{PARA_AMP}, the comparator circuitry 2318A may determine earlier in time when to switich between the the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 to ensure linear operation of the parallel amplifier 2300. As an example, the various embodiments of the V_{OFFSET} loop control circuit 41 may regulate the threshold voltage, $V_{THRESHOLD}$, across the coupling capacitor 18A to be substantially constant based on a target offset voltage parameter, V_{OFFSET_TARGET}. Thus, the comparator circuitry 2318A may generate a time advanced estimate of the parallel amplifier output voltage, V_{PARA_AMP}, by subtracting a target offset voltage, V_{OFFSET_TARGET}, represented by the target offset voltage parameter, V_{OFFSET_TARGET}, from the V_{RAMP} signal. Similarly, the comparator circuitry 2318A

may generate a time advanced estimate of the parallel amplifier output voltage, V_{PARA_AMP}, by subtracting the target offset voltage, V_{OFFSET_TARGET}, represented by the target offset voltage parameter, V_{OFFSET_TARGET}, from control signal 926. The comparator circuitry 2318A may compare the time advance estimate of the parallel amplifier output voltage, V_{PARA_AMP}, to the first threshold and the second threshold to control the generation of the parallel amplifier output current, I_{PARA_AMP}. Equivalently, the controller 50 may calculate the first threshold and the second threshold to take into account the target offset voltage, V_{OFFSET_TARGET}, represented by the target offset voltage parameter, V_{OFFSET_TARGET}. For example, referring to the above example where the $V_{FIRST\text{-}OUTPUT} < V_{SECOND\text{-}OUTPUT} < V_{THIRD\text{-}OUTPUT}$, the first threshold may be substantially equal to sum of the target offset voltage, V_{OFFSET_TARGET}, and the first output voltage $V_{FIRST\text{-}OUTPUT}$ less the headroom voltage of the first PFET transistor 2352, $V_{HEADROOM\text{-}FIRST\text{-}PFET}$. Similarly, the the second threshold may be substantially equal to sum of the target offset voltage, V_{OFFSET_TARGET}, and the second output voltage $V_{SECOND\text{-}OUTPUT}$ less the headroom voltage of the second PFET transistor 2356, $V_{HEADROOM\text{-}SECOND\text{-}PFET}$.

[001467] In addition, in some power level modulation modes, the controller 50 may configure the comparator circuitry 2318A to disable at least one of the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 to reduce the bias current used by the parallel amplifier 2300A. For example, in some embodiments of the medium power modulation mode, the controller 50 may configured the comparator circuitry 2318A to not use one of the the first push-pull output stage 2346, the second push-pull output stage 2348, and the third push-pull output stage 2350 by either setting the first threshold to be less than the minimum expected power amplifier supply voltage, V_{CC_MIN}, plus the target offset voltage, V_{OFFSET_TARGET}, or setting the second threshold to be greater than the maximum power amplifier supply voltage, V_{CC_MAX}, plus the target offset voltage, V_{OFFSET_TARGET}, less the headroom voltage of the respective one of the first PFET transistor 2352, the second PFET transistor 2356, or the third PFET transistor 2360 to be disabled.

The controller 50 may then configure the one charge pump 2390A to not provide an output voltage to the respective one of the first PFET transistor 2352, the second PFET transistor 2356, or the third PFET transistor 2360 to be disabled. As a result, the parallel amplifier 2300A may be configured to decrease the energy consumed by generation of the additional charge pump output voltage as well as the bias current associated with the disabled push-pull output stage.

[001468] Figure 52B depicts an embodiment of a parallel amplifier 2300B that is similar to the parallel amplifier 2300A. The parallel amplifier 2300B is configured to operate with a charge pump 2390B that includes a first output 2394 configured to provide the first supply voltage 2376 and a second output 2396 configured to provide the second supply voltage 2378 to the supply voltage interface 2314. The charge pump 2390B may be similar in form and function to the various embodiments of the various multiple output µC charge pump systems described and depicted in the international patent application PCT/US2011/054106, entitled "SINGLE µC-BUCKBOOST CONVERTER WITH MULTIPLE REGULATED SUPPLY OUTPUTS," filed September 29, 2011. As an example, the charge pump 2390B may be similar in form and function to the dual output µC charge pump circuit 12A, the dual output µC charge pump circuit 12B, the dual output µC charge pump circuit 12C, the dual output µC charge pump circuit 12D, and/or some combination thereof, depicted in the respective Figure 2A, Figure 2B, Figure 2C, and Figure 2D, of the international patent application PCT/US2011/054106. As an example, some embodiments of the charge pump 2390B may be similar in form and function to the µC charge pump 2410 depicted in Figure 53A.

[001469] Similar to the parallel amplifier 2300A, the controller 50 may be in communication with the charge pump 2390B via the control bus 44. The controller 50 may provide the programming parameters 2392 to configure the charge pump 2390B. Based on the programming parameters 2392, the charge pump 2390B may generate a a first output voltage $V_{FIRST\text{-}OUTPUT}$ at the first output 2394 and a second output voltage $V_{SECOND\text{-}OUTPUT}$ at the second output 2396.

[001470] The parallel amplifier 2300B may include a control interface 2308. The parallel amplifier 2300B is similar in form and function to the parallel amplifier 2300A depicted in Figure 52A. However, the parallel amplifier 2300B may not include the third push-pull output stage 2350, the fifth switch element 2372 and the sixth switch element 2374. In addition, the parallel amplifier 2300B may include an embodiment of the comparator circuitry 2318B. The comparator circuitry 2318B may be similar to the comparator circuitry 2318A depicted in Figure 52A. However, the comparator circuitry 2318B does not include a third segment control output 2344 configured to control the fifth switch element 2372 and the sixth switch element 2374.

[001471] The comparator circuitry 2318B may operate in substantially the same manner as the comparator circuitry 2318A depicted in Figure 52A, except that the controller 50 only calculates a first threshold. When the parallel amplifier voltage, V_{PARA_AMP}, is less that the first threshold, the one of the first push-pull output stage 2346 and the second push-pull output stage 2348 that receives a first supply voltage 2376 and a second supply voltage 2378 having the least magnitude is enabled. When the parallel amplifier voltage, V_{PARA_AMP}, is greater than the first threshold, the other of the first push-pull output stage 2346 and the second push-pull output stage 2348 is enabled.

[001472] Figure 52C depicts an embodiment of a parallel amplifier 2300C that is substantially similar in form and function to the parallel amplifier 2300B. The parallel amplifier 2300C combines the first NFET transistor 2354 and the second NFET transistor 2358 into a shared NFET transistor 2382. The parallel amplifier 2300C operates substantially the same as the parallel amplifier 2300B except that the shared NFET transistor 2382 is always enabled. The shared NFET transistor 2382 may be configured to provide a bias current for the one of the first PFET transistor 2352 and the second PFET transistor 2356 that is not configured to generate the parallel amplifier output current, I_{PARA_AMP}.

[001473] Figure 52D depicts an embodiment of a parallel amplifier 2300D. The difference is that the first supply voltage 2376 is provided by the μC charge pump circuit 262 and the second supply voltage 2378 is substantially equal to the

battery voltage, V_{BAT}. Accordingly, for the case where the first supply voltage 2376 is greater than the battery voltage, V_{BAT}, the first threshold is substantially equal to the battery voltage less the headroom voltage of the second PFET transistor 2356. In the case where the first supply voltage 2376 is less than the battery voltage, the first threshold is substantially equal to the first supply voltage 2376 less the headroom voltage of the first PFET transistor 2352.

[001474] Figure 53A depicts an example embodiment of a µC charge pump system 2400 including a µC charge pump 2410, which uses only two flying capacitors to generate multiple output voltages. The µC charge pump 2410 may be similar in form and function to the various embodiments of µC charge pumps described and depicted in the international patent application PCT/US2011/054106, filed September 29, 2011, and entitled, "SINGLE µC-BUCKBOOST CONVERTER WITH MULTIPLE REGULATED SUPPLY OUTPUTS." Some embodiments of the µC charge pump 2410 may be similar to the charge pumps depicted in Figures 2A-D, of the international patent application PCT/US2011/054106. The µC charge pump system 2400 and the µC charge pump 2410 will be described with continuing reference to the embodiments of the power management systems 870, 870A-870C, and 870E-870H, depicted in Figures 40A-E, Figures 46A-B, and Figures 46E-H, the parallel amplifier 35G, depicted in Figure 12G, and the various embodiments of the parallel amplifier 2300, depicted in Figures 52A-D. As described herein, some or all of the various embodiments and combinations thereof of the µC charge pump system 2400 and the µC charge pump 2410 may be incorporated into various embodiments of the parallel amplifier circuits 874, 874', 874B', 874C', 874D', 874E', 874F', 874G', and 874H' depicted in Figure 40A, Figures 40B-E, Figures 46A-B, and Figures 46E-H.

[001475] The embodiments of the µC charge pump reduce or eliminate the need for inductors, large numbers of capacitors, more than two flying capacitors, and complex switching techniques to transform an available voltage level from a system power source, such as a battery 20, to more desirable power supply voltages. Some described embodiments of the µC charge pump 2410 may only

include two flying capacitors. The μC charge pump 2410 may use the only two flying capacitors to simultaneously generate multiple supply outputs. Each of the multiple supply outputs may provide either the same or a different output voltage level. The described embodiments also include efficient power management systems that flexibly provide highly accurate voltage levels that are substantially insensitive to the voltage level provided by a system power source, such as the battery voltage, V_{BAT}. In some embodiments, the μC charge pump 2410 may provide the battery voltage, V_{BAT}, as one of the different output voltages.

[001476] The μC charge pump system 2400 may be configured to provide multiple supply voltages to various circuits of an electronic system. The μC charge pump system 2400 may include a μC charge pump 2410 having a μC charge pump control circuit 2414A cooperatively coupled to a switching network 2412. The switching network 2412 may include a first output 2416 and a second output 2418. A first output capacitor 2420 may be coupled between the first output 2416 and ground, and configured to store charge transferred from the battery 20 by the switching network 2412 to generate a first output voltage $V_{FIRST-OUTPUT}$ 2416VO. As second output capacitor 2422 may be coupled between the second output 2418 and ground, and configured to store charge transferred from the battery 20 by the switching network 2412 to generate a second output voltage $V_{SECOND-OUTPUT}$ 2418VO. The first output 2416 may be coupled to a first output capacitor 2420, having a capacitance substantially equal to $C_{\mu C1}$. The first output 2416 may be coupled to a second output capacitor 2422 having a capacitance substantially equal to $C_{\mu C2}$. The switching network 2412 and the μC charge pump control circuit 2414A may receive a battery voltage, V_{BAT}, from the battery 20. Similar to the μC charge pump circuit 262, the μC charge pump control circuit 2414A may receive a μC charge pump clock 276 from a clock management circuit 260. Depending on a power level modulation mode of operation, the μC charge pump clock 276 may be generated based on a switching frequency of the switch mode power supply converter 872. Alternatively, the μC charge pump clock 276 may be generated based on a frequency of an oscillator 270.

[001477] The switching network 2412 and the µC charge pump control circuit 2414A may cooperatively transfer charge from the battery 20 to the first output capacitor 2420 and the second output capacitor 2422 as a function of a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC developed across a first flying capacitor 2424 and a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC developed across a second flying capacitor 2426. The first flying capacitor 2424 may have a first terminal 2424A and a second terminal 2424B. The first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC is developed across the first terminal 2424A and the second terminal 2424B of the first flying capacitor 2424. The first flying capacitor 2424 may have a capacitance substantially equal to C_{FLY1}. The second flying capacitor 2426 may have a first terminal 2426A and a second terminal 2426B. The second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC is developed across the first terminal 2426A and the second terminal 2426B of the second flying capacitor 2426. The second flying capacitor 2426 may have a capacitance substantially equal to C_{FLY2}.

[001478] As a non-limiting example, Figure 53A may depict an embodiment of the charge pump 2390B, depicted in Figures 52B-C, as a µC charge pump 2410. Each of the at least two output voltage levels may be provided to one or more different components, sub-assemblies, and devices of electronic devices, sub-systems, and systems. As an example, the µC charge pump 2410 may include first flying capacitor 2424 having a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC, and a second flying capacitor 2426 having a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC . The µC charge pump 2410 may generate the two or more output voltages as a function of a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC developed across a first flying capacitor 2424 and a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC developed across the second flying capacitor 2426. As an example, the µC charge pump 2410 may include a switching network 2412 in communication with the µC charge pump control circuit 2414A. The switching network 2412 may include a number of switch elements and a first flying capacitor 2424 and a second flying capacitor 2426.

[001479] Figure 53A depicts an example embodiment of the µC charge pump control circuit 2414A configured to control the switching network 2412. The µC charge pump control circuit 2414A may actuate various switches of the switching network 2412 based on a phase of operation to switchably couple the first flying capacitor 2424 and the second flying capacitor 2426 in various relationships between the battery voltage, V_{BAT}, the ground, the first output 2416, and the second output 2418 to simultaneously generate multiple output voltages.

[001480] As a first example, the µC charge pump system 2400 may include a non-limiting example of a µC charge pump 2410 and a controller 50 coupled to the µC charge pump 2410 via the control bus 44. In some embodiments, the controller 50 may be coupled to a battery level sense circuit 264 via the control bus 44. The battery level sense circuit 264 may be configured to provide the controller 50 a measured or estimated voltage of the battery 20. As an example, the battery voltage, V_{BAT}, may be derived from a battery 20.

[001481] The µC charge pump 2410 may also be coupled to the battery 20, and be configured to receive the battery voltage, V_{BAT}. The µC charge pump 2410 may generate a first output 2416 and a second output 2418. As an example, the controller 50 may configure the µC charge pump 2410 to generate a first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO on the first output 2416 and a second output voltage $V_{SECOND\text{-}OUTPUT}$ 2418VO on the second output 2418.

[001482] In some embodiments of the µC charge pump system 2400, the controller 50 may configure the µC charge pump 2410 such that the first output 2416 operates in a "buck mode" of operation. In the case where the µC charge pump 2410 operates the first output 2416 in the buck mode of operation, the first output 2416 provides a "bucked" output voltage level relative to the battery voltage, V_{BAT}, as the first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO . As an example, neglecting losses in the signal paths between the battery voltage, V_{BAT}, and the first output 2416, when the µC charge pump 2410 is configured to operate the first output 2416 in the buck mode of operation, the first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO may have a magnitude that is equal to or less than the battery voltage, V_{BAT} In a similar fashion, in some embodiments of the

µC charge pump system 2400, the controller 50 may configure the µC charge pump 2410 such that the second output 2418 operates in a buck mode of operation. In the buck mode of operation, the second output 2418 may provide a bucked output voltage level relative as the second output voltage $V_{SECOND-OUTPUT}$ 2418VO. As an example, in the buck mode of operation, the second output voltage $V_{SECOND-OUTPUT}$ 2418VO may have a magnitude that is equal to or less than the $batt_{ery}$ voltage, V_{BAT}.

[001483] In other embodiments of the µC charge pump system 2400, the controller 50 may configure the µC charge pump 2410 such that the first output 2416 operates in a "boost mode" of operation. In the boost mode of operation, the first output 2416 may provide a "boosted" output voltage level relative to the battery voltage, V_{BAT}, as the first output voltage $V_{FIRST-OUTPUT}$ 2416VO . As an example in the boost mode of operation, the first output voltage $V_{FIRST-OUTPUT}$ 2416VO may have a magnitude that is greater than the battery voltage, V_{BAT}.

[001484] Likewise, in some embodiments of the µC charge pump system 2400, the controller 50 may configure the µC charge pump 2410 to operate the second output 2418 operates in a boost mode of operation. In the boost mode of operation, the second output 2418 may provide the boosted output voltage level as the second output voltage$V_{SECOND-OUTPUT}$ 2418VO. As an example, in the boost mode of operation, the second output voltage $V_{SECOND-OUTPUT}$ 2418VO may have a magnitude that is greater than the battery voltage, V_{BAT}.

[001485] The controller 50 may configure the µC charge pump 2410 to operate in various modes of operation. As a non-limiting example of these modes of operation, the controller 50 may configure the µC charge pump 2410 to operate in a "buck / buck mode" of operation, a "buck / boost mode" of operation, and/or a "boost / buck mode" of operation. As one example, when the controller 50 configures the µC charge pump 2410 to operate in the buck / buck mode of operation, the µC charge pump 2410 operates the first output 2416 in a buck mode of operation and the second output 2418 in a buck mode of operation. As another example, when the controller 50 configures the µC charge pump 2410 to

operate in the buck / boost mode of operation, the µC charge pump 2410 operates the first output 2416 in a buck mode of operation and the second output 2418 in a boost mode of operation. As yet another example, when the controller 50 configures the µC charge pump 2410 to operate in the boost / buck mode of operation, the µC charge pump 2410 operates the first output 2416 in a boost mode of operation and the second output 2418 in a buck mode of operation. In still other embodiments, the µC charge pump 2410 may also operated in a boost/boost mode of operation to simultaneously generate two boosted output voltages.

[001486] In some embodiments, the controller 50 may be configured to control the modes of operation of the µC charge pump 2410 based upon the measured or estimated voltage of the battery voltage, V_{BAT}. Alternatively, the controller 50 may be configured to control the operation of the µC charge pump 2410 based upon an operational mode of a system or an integrated chip in which the µC charge pump system 2400 is being used. For example, the controller 50 may configure the µC charge pump 2410 based on a power level modulation mode, as discussed above with respect to Figures 40A-51.

[001487] In some embodiments, similar to Figures 18A-D, the µC charge pump system 2400 may further include the clock management circuit 260. The µC charge pump control circuit 2414A may use the µC charge pump clock 276 to govern the operation of the µC charge pump 2410. For example, the µC charge pump control circuit 2414A may use the µC charge pump clock 276 to determine the length and timing of each of the phases of operation, the duration of each of the phases of operation, and the order in which the switches of the switching network 2412 change state.

[001488] As previously described with respect to the µC charge pump circuit 262, depicted in Figures 18A-D, Figures 40C-E, Figure 41, and Figures 46B and 46E-H, the controller 50 may configure the clock management circuit 260 to provide the µC charge pump clock 276 in various operational modes. As a non-limiting list of examples, the various refence clock sources used to generate the µC charge pump clock 276 may include a frequency locked

loop (FLL) circuit, a reference clock from a sub-system of an integrated chip, a power supply system, the switching frequency of the switch mode power supply converter 872 in Figure 40B. In some embodiments, the µC charge pump clock 276 is derived from the switching frequency of the switch mode power supply converter while the switch mode power supply converter 872 is enabled. In some embodiments, the switching frequency of the switch mode power supply converter 872 is free running and substantially determined by the one or more threshold levels used by the switcher control circuit 880 to determine an operational state of the switcher control circuit 880. As an example, in the free running state of operation, decreasing the shunt level threshold 124 may increase the switching frequency of the switch mode power supply converter 872. Conversely, increasing the shunt threshold level may decrease the switching frequency of the switch mode power supply converter 872. In some embodiments of the switch mode power supply converter 872, the controller 50 may be configure one or more of the shunt level threshold 124, the first buck level threshold 125, the series level threshold 126, the first boost level threshold 128, and the second boost level threshold 130 to obtain a target switching frequency. For example, in some embodiments, the controller 50 may adjust one or more threshold level parameters to obtain a desired switching frequency in order to place harmonics of the switching frequency outside a particular band of operation or receiver channel within a band of operation. Also, the controller 50 may turn on the oscillator 270 to provide the µC charge pump clock 276 when the switch mode power supply converter 872 is disabled. Otherwise, the controller 50 may power down the oscillator 270.

[001489] Figure 53A depicts one of several embodiments of the µC charge pump 2410. For the sake of convenience, and not by way of limitation, the µC charge pump 2410 is described with continuing reference to various elements of the controller 50, control bus 44, the battery level sense circuit 264, the battery voltage, V_{BAT}, the battery 20, the clock management circuit 260, and the µC charge pump clock 276, the first flying capacitor 2424, and the second flying capacitor 2426.

[001490] The µC charge pump 2410 may include a switching network 2412and a µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may communicate with the controller 50 via the control bus 44. The controller 50 may configure the µC charge pump 2410 to operate in various modes of operation via the control bus 44. As a non-limiting example, the µC charge pump 2410 may be configured by the controller 50 to operate in a "buck / buck mode" of operation, a "buck / boost mode" of operation, and/or a "boost / buck mode" of operation. In addition, the µC charge pump control circuit 2414A may be further configured to receive the µC charge pump clock 276 . Furthermore, the controller 50 may configure the µC charge pump 2410 to operate in a boost/boost mode of operation.

[001491] The switching network 2412 may be configured by the µC charge pump control circuit 2414A to generate the first output voltage $V_{FIRST-OUTPUT}$ 2416VO on the first output 2416 and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO on the second output 2418 based on a selected mode of operation of the µC charge pump 2410.

[001492] To simplify the description of the operation of the µC charge pump 2410 and the operation of the switching network 2412, Figure 53A depicts the first flying capacitor 2424 and the second flying capacitor 2426 as being incorporated into the switching network 2412. Some embodiments of the µC charge pump 2410 may include and use more than two flying capactiors to generate the first output voltage $V_{FIRST-OUTPUT}$ 2416VO on the first output 2416 and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO on the second output 2418. However, advantageously, the µC charge pump 2410 may be configured to simultaneously generate the first output voltage $V_{FIRST-OUTPUT}$ 2416VO on the first output 2416 and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO on the second output 2418 using only the first flying capacitor 2424 and the second flying capacitor 2426.

[001493] In other words, as will be described below, some embodiments of the µC charge pump 2410 may generate the variously described output voltage levels corresponding to a "buck / buck mode" of operation, a "buck / boost mode"

of operation, a "boost / buck mode" of operation, a "boost / boost" mode of operation, and/or some combination thereof using only the first flying capacitor 2424 and the second flying capacitor 2426. It may be appreciated that those embodiments of the µC charge pump 2410 that only use the first flying capacitor 2424 and the second flying capacitor 2426 to generate the desired output voltage levels on the first output 2416 and the second output 2418 may provide improved technical performance due to reduced complexity and reduced response time verses embodiments that include more than two flying capacitors.

[001494] The switching network 2412 may include a first flying capacitor 2424, a second flying capacitor 2426, a first switch 2432, (SW1), a second switch 2436, (SW2), a third switch 2440, (SW3), a fourth switch 2444, (SW4), a fifth switch 2448, (SW5), a sixth switch 2452, (SW6), a seventh switch 2456, (SW7), an eighth switch 2460, (SW8), a ninth switch 2464, (SW9), a tenth switch 2468, (SW10), an eleventh switch 2472, (SW11), a twelfth switch 2476, (SW12), a thirteenth switch 2480, (SW13), a fourteenth switch 2484, (SW14), a fifteenth switch 2488, (SW15), a sixteenth switch 2492, (SW16), and a seventeenth switch 2496, (SW17).

[001495] In some embodiments of the switching network 2412, the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17), may be solid state based switches, micro-electromechanical systems (MEMS) contact based switches, or combinations thereof.

[001496] Illustratively, as a non-limiting example, solid state based switches may include field effect transistors, insulator-on-semiconductor based transistors, bipolar based transistors, and/or a combination thereof. The example solid state

based switches may be fabricated using various semiconductor device fabrication processes, techniques, and materials. As an example, some solid state based switches may be based on a gallium nitride (GaN) process. In some embodiments, gallium nitride metal/oxide semiconductor field-effect transistors may be used to create the solid state switches. In still other embodiments, the gallium nitride metal/oxide semiconductor field-effect transistors may be a gallium nitride field effect transistor. As an example, the gallium nitride field effect transistor may be an enhancement mode gallium nitride metal–oxide–semiconductor field-effect transistor (MOSFET).

[001497] Returning to the description of the μC charge pump control circuit 2414A, the μC charge pump control circuit 2414A may further include;

- a first switch control configured to provide a first switch control signal 2430 to the first switch 2432, (SW1), to control the operation of the first switch 2432, (SW1);
- a second switch control configured to provide a second switch control signal 2434 to the second switch 2436, (SW2), to control the operation of the second switch 2436, (SW2);
- a third switch control configured to provide a third switch control signal 2438 to the third switch 2440, (SW3), to control the operation of the third switch 2440, (SW3);
- a fourth switch control configured to provide a fourth switch control signal 2442 to the fourth switch 2444, (SW4), to control the operation of the fourth switch 2444, (SW4);
- a fifth switch control configured to provide a fifth switch control signal 2446 to the fifth switch 2448, (SW5), to control the operation of the fifth switch 2448, (SW5);
- a sixth switch control configured to provide a sixth switch control signal 2450 to the sixth switch 2452, (SW6), to control the operation of the sixth switch 2452, (SW6);

- a seventh switch control configured to provide a seventh switch control signal 2454 to the seventh switch 2456, (SW7), to control the operation of the seventh switch 2456, (SW7);
- an eighth switch control configured to provide an eighth switch control signal 2458 to the eighth switch 2460, (SW8), to control the operation of the eighth switch 2460, (SW8);
- a ninth switch control configured to provide a ninth switch control signal 2462 to the ninth switch 2464, (SW9), to control the operation of the ninth switch 2464, (SW9);
- a tenth switch control configured to provide a tenth switch control signal 2466 to the tenth switch 2468, (SW10), to control the operation of the tenth switch 2468, (SW10);
- an eleventh switch control configured to provide an eleventh switch control signal 2470 to the eleventh switch 2472, (SW11), to control the operation of the eleventh switch 2472, (SW11);
- a twelfth switch control configured to provide a twelfth switch control signal 2474 to the twelfth switch 2476, (SW12), to control the operation of the twelfth switch 2476, (SW12);
- a thirteenth switch control configured to provide a thirteenth switch control signal 2478 to the thirteenth switch 2480, (SW13), to control the operation of the thirteenth switch 2480, (SW13);
- a fourteenth switch control configured to provide a fourteenth switch control signal 2482 to the fourteenth switch 2484, (SW14), to control the operation of the fourteenth switch 2484, (SW14);
- a fifteenth switch control configured to provide a fifteenth switch control signal 2486 to the fifteenth switch 2488, (SW15), to control the operation of the fifteenth switch 2488, (SW15);
- a sixteenth switch control configured to provide a sixteenth switch control signal 2490 to the sixteenth switch 2492, (SW16), to control the operation of the sixteenth switch 2492, (SW16); and

- a seventeenth switch control configured to provide a seventeenth switch control signal 2494 to the seventeenth switch 2496, (SW17), to control the operation of the seventeenth switch 2496, (SW17).

[001498] The first switch 2432, (SW1), may be coupled between the battery voltage, V_{BAT}, and the first terminal 2424A of the first flying capacitor 2424. The first switch 2432, (SW1), may include a first switch control input configured to receive the first switch control signal 2430 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the first switch control signal 2430 to operably open and close the first switch 2432, (SW1), based upon the various modes of operation of the µC charge pump 2410.

[001499] The second switch 2436, (SW2), may be coupled between the first terminal 2424A of the first flying capacitor 2424 and the first output 2416. The second switch 2436, (SW2), may include a second switch control input configured to receive the second switch control signal 2434 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the second switch control signal 2434 to operably open and close the second switch 2436, (SW2), based upon the various modes of operation of the µC charge pump 2410.

[001500] The third switch 2440, (SW3), may be coupled between the second terminal 2424B of the first flying capacitor 2424 and ground. The third switch 2440, (SW3), may include a third switch control input configured to receive the third switch control signal 2438 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the third switch control signal 2438 to operably open and close the third switch 2440, (SW3), based upon the various modes of operation of the µC charge pump 2410.

[001501] The fourth switch 2444, (SW4), may be coupled between the second terminal 2424B of the first flying capacitor 2424 and the first output 2416. The fourth switch 2444, (SW4), may include a fourth switch control input configured to receive the fourth switch control signal 2442 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the fourth switch control signal 2442 to operably open and close the fourth

switch 2444, (SW4), based upon the various modes of operation of the µC charge pump 2410.

[001502] The fifth switch 2448, (SW5), may be coupled between the second terminal 2424B of the first flying capacitor 2424 and the first terminal 2426A of the second flying capacitor 2426 The fifth switch 2448, (SW5), may include a fifth switch control input configured to receive the fifth switch control signal 2446 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the fifth switch control signal 2446 to operably open and close the fifth switch 2448, (SW5), based upon the various modes of operation of the µC charge pump 2410.

[001503] The sixth switch 2452, (SW6), may be coupled between the first terminal 2426A of the second flying capacitor 2426 and the battery voltage, V_{BAT}. The sixth switch 2452, (SW6), may include a sixth switch control input configured to receive the sixth switch control signal 2450 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the sixth switch control signal 2450 to operably open and close the sixth switch 2452, (SW6), based upon the various modes of operation of the µC charge pump 2410.

[001504] The seventh switch 2456, (SW7), may be coupled between the first terminal 2426A of the second flying capacitor 2426 and the first output 2416. The seventh switch 2456, (SW7), may include a seventh switch control input configured to receive the seventh switch control signal 2454 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the seventh switch control signal 2454 to operably open and close the seventh switch 2456, (SW7), based upon the various modes of operation of the µC charge pump 2410.

[001505] The eighth switch 2460, (SW8), may be coupled between the second terminal 2426B of the second flying capacitor 2426 and ground. The eighth switch 2460, (SW8), may include an eighth switch control input configured to receive the eighth switch control signal 2458 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the eighth switch control signal 2458 to operably open and close the eighth

switch 2460, (SW8), based upon the various modes of operation of the µC charge pump 2410.

[001506] The ninth switch 2464, (SW9), may be coupled between the second terminal 2426B of the second flying capacitor 2426 and the first output 2416. The ninth switch 2464, (SW9), may include a ninth switch control input configured to receive the ninth switch control signal 2462 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the ninth switch control signal 2462 to operably open and close the ninth switch 2464, (SW9), based upon the various modes of operation of the µC charge pump 2410.

[001507] The tenth switch 2468, (SW10), may be coupled between the first terminal 2424A of the first flying capacitor 2424 and the first terminal 2426A of the second flying capacitor 2426. The tenth switch 2468, (SW10), may include a tenth switch control input configured to receive the tenth switch control signal 2466 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the tenth switch control signal 2466 to operably open and close the tenth switch 2468, (SW10), based upon the various modes of operation of the µC charge pump 2410.

[001508] The eleventh switch 2472, (SW11), may be coupled between the second terminal 2426B of the second flying capacitor 2426 and the battery voltage, V_{BAT}. The eleventh switch 2472, (SW11), may include an eleventh switch control input configured to receive the eleventh switch control signal 2470 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the eleventh switch control signal 2470 to operably open and close the eleventh switch 2472, (SW11), based upon the various modes of operation of the µC charge pump 2410.

[001509] The twelfth switch 2476, (SW12), may be coupled between the second terminal 2426B of the second flying capacitor 2426 and the second output 2418. The twelfth switch 2476, (SW12), may include a twelfth switch control input configured to receive the twelfth switch control signal 2474 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may

configure the twelfth switch control signal 2474 to operably open and close the twelfth switch 2476, (SW12), based upon the various modes of operation of the µC charge pump 2410.

[001510] The thirteenth switch 2480, (SW13), may be coupled between the first terminal 2426A of the second flying capacitor 2426 and the second output 2418. The thirteenth switch 2480, (SW13), may include a thirteenth switch control input configured to receive the thirteenth switch control signal 2478 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the thirteenth switch control signal 2478 to operably open and close the thirteenth switch 2480, (SW13), based upon the various modes of operation of the µC charge pump 2410.

[001511] The fourteenth switch 2484, (SW14), may be coupled between the second terminal 2424B of the first flying capacitor 2424 and the second output 2418. The fourteenth switch 2484, (SW14), may include a fourteenth switch control input configured to receive the fourteenth switch control signal 2482 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the fourteenth switch control signal 2482 to operably open and close the fourteenth switch 2484, (SW14), based upon the various modes of operation of the µC charge pump 2410.

[001512] The fifteenth switch 2488, (SW15), may be coupled between the second terminal 2424B of the first flying capacitor 2424 and the battery voltage, V_{BAT}. The fifteenth switch 2488, (SW15), may include a fifteenth switch control input configured to receive the fifteenth switch control signal 2486 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the fifteenth switch control signal 2486 to operably open and close the fifteenth switch 2488, (SW15), based upon the various modes of operation of the µC charge pump 2410.

[001513] The sixteenth switch 2492, (SW16), may be coupled between the battery voltage, V_{BAT}, and the first output 2416. The sixteenth switch 2492, (SW16), may include a sixteenth switch control input configured to receive the sixteenth switch control signal 2490 from the µC charge pump control

circuit 2414A. The µC charge pump control circuit 2414A may configure the sixteenth switch control signal 2490 to operably open and close the sixteenth switch 2492, (SW16), based upon the various modes of operation of the µC charge pump 2410.

[001514] The seventeenth switch 2496, (SW17), may be coupled between the battery voltage, V_{BAT}, and the second output 2418. The seventeenth switch 2496, (SW17), may include a seventeenth switch control input configured to receive the seventeenth switch control signal 2494 from the µC charge pump control circuit 2414A. The µC charge pump control circuit 2414A may configure the seventeenth switch control signal 2494 to operably open and close the seventeenth switch 2496, (SW17), based upon the various modes of operation of the µC charge pump 2410.

[001515] Numerous example embodiments of the modes of operation of the µC charge pump 2410 will now be described. These example embodiments of the modes of operation of the µC charge pump 2410 are by illustration and not by way of limitation. For example, various other modes of operation of the µC charge pump 2410 may be used to generate different magnitudes of the first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO on the first output 2416 and the second output voltage $V_{SECOND\text{-}OUTPUT}$ 2418VO on the second output 2418. These additional various other modes of operation of the µC charge pump 2410, as would be evident to one of ordinary skill in the art, are thereby included herein. In addition, for the sake of clarity and brevity, the foregoing description of the modes of operation of the µC charge pump 2410 will be accomplished by describing a configuration where a supply voltage for the µC charge pump 2410 is powered by a battery voltage, V_{BAT}, derived from the battery 20.

[001516] The description of the modes of operation of the µC charge pump 2410 based on the battery voltage, V_{BAT}, is derived from the battery 20 and is not by way of limitation and only meant to aid the understanding of the modes of operation of the µC charge pump 2410 and the ratios between the first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO to voltage level of the battery voltage, V_{BAT}, and

the ratios between the second output voltage $V_{SECOND-OUTPUT}$ 2418VO to the voltage level of the battery voltage, V_{BAT}.

[001517] A non-limiting set of example operational modes of the µC charge pump 2410 will now be discussed with reference to various tables, provided herein. Example operational modes of the µC charge pump 2410 may include one or more buck / buck modes of operation, one or more buck / boost modes of operation, and/or one or more boost / buck modes of operation. In addition, those of ordinary skill in the art may recognize that various other modes of operation may be achive by the µC charge pump 2410 including a number of boost / boost modes of operation. In addition, additional modes of operation may be achieved such that the first output voltage $V_{FIRST-OUTPUT}$ 2416VO and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO are substantially equal.

[001518] TABLE 1A, entitled "MODES OF OPERATION TABLE FOR BUCK / BUCK OPERATION OF A DUAL OUTPUT µC CHARGE PUMP CIRCUIT," describes, in tablulated form, several, non-limiting, example modes of operation of the µC charge pump 2410 configured to operate in a buck / buck mode of operation. The described non-limiting example modes of Buck /Buck modes of operation include: a First (1st) Buck / Buck Mode, a Second (2nd) Buck / Buck Mode, a Third (3rd) Buck / Buck Mode, a Fourth (4th) Buck / Buck Mode, a Fifth (5th) Buck / Buck Mode, a First (1st) Bypass Mode, a Second (2nd) Bypass Mode, a Third (3rd) Bypass Mode, and an OFF Mode. In addition, although not described in detail below, it will be understood that the µC charge pump 2410 may be further configured to operate in additional buck / buck modes of operation, as described in TABLE 1B, entitled "MODES OF OPERATION TABLE FOR BUCK / BUCK OPERATION OF A DUAL OUTPUT µC CHARGE PUMP CIRCUIT." These addition, non-limiting examples, of Buck /Buck modes of operation may include: a Sixth (6th) Buck / Buck Mode, a Seventh (7th) Buck / Buck Mode, an Eighth (8th) Buck / Buck Mode, a Ninth (9th) Buck / Buck Mode, a Tenth (10th) Buck / Buck Mode, a Fifth (5th) Bypass Mode, a Fifth (5th) Bypass Mode, and a Sixth (6th) Bypass Mode.

[001519] As depicted in TABLE 1A, each example mode of operation corresponds to an operational ratio, (μBB_{RATIO}), of the µC charge pump 2410, where the operational ratio, (μBB_{RATIO}), may provide a relationship between the first output voltage $V_{FIRST-OUTPUT}$ 2416VO generated by the first output 2416 and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO generated by the second output 2418. The operational ratio, (μBB_{RATIO}), may be an operational ratio parameter that is configured by the controller 50 and stored locally in the µC charge pump control circuit 2414A.

[001520] As described in Table 1A, the µC charge pump 2410 is configured to generate a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to (μBB_{RATIO}) x V_{BAT}. In addition, the µC charge pump 2410 is further configured to generate a second output $V_{SECOND-OUTPUT}$ substantially equal to (1-μBB_{RATIO}) x V_{BAT}.

[001521] Accordingly, in the First Buck / Buck Mode of operation of the µC charge pump 2410, the controller 50 may configure the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/4 x V_{BAT}.

[001522] In the Second Buck / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 2/3 x V_{BAT}.

[001523] In the Third Buck / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO

substantially equal to 1/2 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/2 x V_{BAT}.

[001524] In the Fourth Buck / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/3 x V_{BAT}.

[001525] In the Fifth Buck / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT}. In the OFF Mode of operation of the µC charge pump 2410, the controller 50 configures the first output 2416 to float and the second output 2418 to float.

[001526] In the First Bypass Mode of operation of the µC charge pump 2410, the controller 50 may configure the µC charge pump control circuit 2414A to use any number of available operational ratios, (μBB_{RATIO}), to generate the second output voltage $V_{SECOND-OUTPUT}$ 2418VO. The controller 50 further configures the sixteenth switch 2492, (SW16) to be closed. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to V_{BAT}.

[001527] The controller 50 may also configure the second switch 2416, (SW2), the fourth switch 2444, (SW4), the seven switch 2456, (SW7), and the ninth switch 2496, (SW9), to be open in order to decouple the second output 2416 from the internal switching of the switching network 2412. Alternatively, in some additional modes of operation, the controller 50 may selectively configure the

second switch 2416, (SW2), the fourth switch 2444, (SW4), the seven switch 2456, (SW7), and the ninth switch 2496, (SW9), to be closed during a mode of operaton to obtain a desired output voltage level on the second output voltage $V_{SECOND-OUTPUT}$ 2418VO.

[001528] For example, because the first flying capacitor 2424 and the second flying capacitor 2426 are not used to generate the first output voltage $V_{FIRST-OUTPUT}$ 2416VO, the controller 50 may at least generate a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to $(1-\mu BB_{RATIO}) \times V_{BAT}$, $(\mu BB_{RATIO}) \times V_{BAT}$. In addition, as described further below, the controller 50 may at least generate a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to $(1+ \mu BB_{RATIO}) \times V_{BAT}$.

[001529] In the OFF Mode of operation of the µC charge pump 2410, the controller 50 configures the first output 2416 to float and the second output 2418 to float.

MODES OF OPERATION TABLE FOR BUCK / BUCK OPERATION OF A µC CHARGE PUMP CIRCUIT			
MODES OF OPERATION	OPERATIONAL RATIOS, (μBB_{RATIO})	$V_{FIRST\text{-}OUTPUT}$ $V_{FIRST\text{-}OUTPUT} = (\mu BB_{RATIO}) \times V_{BAT}$	$V_{SECOND\text{-}OUTPUT}$ $= (1 - \mu BB_{RATIO}) \times V_{BAT}$
First Buck / Buck Mode	1/4	1/4 x V_{BAT}	3/4 x V_{BAT}
Second Buck / Buck Mode	1/3	1/3 x V_{BAT}	2/3 x V_{BAT}
Third Buck / Buck Mode	1/2	1/2 x V_{BAT}	1/2 x V_{BAT}
Fourth Buck / Buck Mode	2/3	2/3 x V_{BAT}	1/3 x V_{BAT}
Fifth Buck / Buck Mode	3/4	3/4 x V_{BAT}	1/4 x V_{BAT}
First Bypass Mode	μBB_{RATIO}	V_{BAT}	$(1\text{-}\mu BB_{RATIO}) \times V_{BAT}$ or FLOATING
Second Bypass Mode	μBB_{RATIO}	$(\mu BB_{RATIO}) \times V_{BAT}$ or FLOATING	V_{BAT}
Third Bypass Mode	μBB_{RATIO}	V_{BAT}	V_{BAT}
OFF Mode	OFF	FLOATING	FLOATING

TABLE 1A

MODES OF OPERATION TABLE FOR BUCK / BUCK OPERATION OF A µC CHARGE PUMP CIRCUIT			
MODES OF OPERATION	OPERATIONAL RATIOS, (μBB_{RATIO})	$V_{FIRST\text{-}OUTPUT}$ $V_{FIRST\text{-}OUTPUT} = (1\text{-}\mu BB_{RATIO}) \times V_{BAT}$	$V_{SECOND\text{-}OUTPUT}$ $= (\mu BB_{RATIO}) \times V_{BAT}$
Sixth Buck / Buck Mode	1/4	3/4 x V_{BAT}	1/4 x V_{BAT}
Seventh Buck / Buck Mode	1/3	2/3 x V_{BAT}	1/3 x V_{BAT}
Eighth Buck / Buck Mode	1/2	1/2 x V_{BAT}	1/2 x V_{BAT}
Ninth Buck / Buck Mode	2/3	1/3 x V_{BAT}	2/3 x V_{BAT}
Tenth Buck / Buck Mode	3/4	1/4 x V_{BAT}	3/4 x V_{BAT}
Fourth Bypass Mode	μBB_{RATIO}	V_{BAT}	(μBB_{RATIO}) x V_{BAT} or FLOATING
Third Bypass Mode	μBB_{RATIO}	(1-μBB_{RATIO}) x V_{BAT} or FLOATING	V_{BAT}
Foruth Bypass Mode	μBB_{RATIO}	V_{BAT}	V_{BAT}
OFF MODE	0	FLOATING	FLOATING

TABLE 1B

[001530] Based on the mode of operation of the µC charge pump 2410, the controller 50 may configure the µC charge pump control circuit 2414A to control the switch state (open or closed) of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17) based upon the µC charge pump clock 68.

[001531] For example, in some embodiments of the µC charge pump 2410, the µC charge pump control circuit 2414A may be configured to divide the operation of the µC charge pump 2410 into phases of operation. For example, µC charge pump control circuit 2414A may be configured to operate in a first phase, a second phase, a third phase, a fourth phase, and so forth. During each phase of operation of the µC charge pump 2410, the µC charge pump control circuit 2414A may be configured to change the switch state (open or closed) of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17), for a period of time.

[001532] In some embodiments of the µC charge pump 2410, depicted in Figure 53A, the µC charge pump control circuit 2414A may configure the period of time for each phase of operation of the µC charge pump 2410 to be substantially equal. For example, the µC charge pump 2410 may remain in each

phase of operation for the same number of clock cycles of the µC charge pump clock 68.

[001533] In other embodiments of the µC charge pump 2410, depicted in Figure 53A, the µC charge pump control circuit 2414A may configure the period of time for each phase of operation of the µC charge pump 2410 to be different to optimize the effeciency of the µC charge pump 2410 when operating in a particular mode of operation. For example, in some modes of operation, the µC charge pump control circuit 2414A may configure the µC charge pump 2410 to remain in a first phase of operation for a first number of clock cycles of the µC charge pump clock 68 and remain in a second phase of operation for a second number of clock cycles of the µC charge pump clock 68. The period of time for each phase of operation may be based upon one or more of the various factors including, but not limited to, the size of each of the µC charge pump switches, the current load associated with each of the first output 2416 and the second output 2418, the combination of the first output voltage $V_{FIRST-OUTPUT}$ 2416VO and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO generated at the respective first output 2416 and the second output 2418.

[001534] The maximum switching frequency between the phases of operation may be a function of the setting times of the first output voltage $V_{FIRST-OUTPUT}$ 2416VO and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO generated at the respective first output 2416 and the second output 2418. The settling times may be a function of the series resistance of the µC charge pump switches used to generate each of the first output voltage $V_{FIRST-OUTPUT}$ 2416VO and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO. The setting time may also depend on the capacitance values of the first output capacitor 2420 and the second output capacitor 2422.

[001535] In addition, to minimize switching noise and interference signals, in some embodiments of the µC charge pump 2410, the µC charge pump control circuit 2414A may align the phases of operation of the µC charge pump 2410 such that the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5),

the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17), may switch states based on or in alignment with the switching frequency of the switch mode power supply converter 872.

[001536] Continuing with the description of the various example embodiments of the modes of operation of the µC charge pump 2410 described in TABLE 1A, TABLE 1B-1, TABLE 1B-2, and TABLE 1B-3, entitled "SWITCH OPERATION TABLES FOR BUCK / BUCK OPERATION OF A µC CHARGE PUMP," describe the switch state (open or closed) of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17), of the µC charge pump 2410 when the µC charge pump 2410 is configured to operate in an identifed buck / buck mode of operation. In addition, TABLE 1B-1 and TABLE 1B-2 also provide the corresponding operational ratio, (μBB_{RATIO}), of the µC charge pump 2410, used in the identified buck / buck mode of operation. Also, TABLE 1B-1, TABLE 1B-2, and Table 1B-3 describe the switch state of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth

switch 2496, (SW17), relative to a particular phase of operation of the µC charge pump 2410.

[001537] As used in TABLE 1B-1, TABLE 1B-2, and TABLE 1B-3, "PHASE 1" indicates that the µC charge pump 2410 is configured to operate in a first phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the first phase of operation. "PHASE 2" indicates that the µC charge pump 2410 is configured to operate in a second phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the second phase of operation. "PHASE 3" indicates that the µC charge pump 2410 is configured to operate in a third phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the third phase of operation. "PHASE 4" indicates that the µC charge pump 2410 is configured to operate in a fourth phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the fourth phase of operation. "OPEN" indicates that the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified switch to be closed during all the phases of operation of the µC charge pump 2410.

SWITCH OPERATION TABLE FOR BUCK / BUCK MODE OF OPERATION OF A µC CHARGE PUMP			
See, TABLE 1A	MODES OF OPERATION FOR BUCK / BUCK OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	First Buck / Buck Mode, (μBB_{RATIO} = 1/4), where $V_{FIRST\text{-}OUTPUT}$ = 1/4 x V_{BAT} and $V_{SECOND\text{-}OUTPUT}$ = 3/4 x V_{BAT}	Second Buck / Buck Mode, (μBB_{RATIO} = 1/3), where $V_{FIRST\text{-}OUTPUT}$ = 1/3 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 2/3 x V_{BAT}	Third Buck / Buck Mode, (μBB_{RATIO} = 1/2), where $V_{FIRST\text{-}OUTPUT}$ = 1/2 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 1/2 x V_{BAT}
SW1	Phase 1	Phase 1 and Phase 3	Phase 1 and Phase 3
SW2	OPEN	Phase 2	Phase 2
SW3	Phase 3	Phase 2	Phase 2
SW4	OPEN	OPEN	Phase 1
SW5	Phase 1	Phase 1	OPEN
SW6	OPEN	Phase 3	Phase 1
SW7	Phase 2	Phase 2	Phase 2
SW8	Phase 2	Phase 2	Phase 2
SW9	Phase 1 and Phase 3	Phase 1	Phase 1
SW10	Phase 3 and Phase 4	OPEN	Phase 3
SW11	Phase 4	OPEN	OPEN
SW12	OPEN	Phase 3	Phase 3
SW13	OPEN	OPEN	OPEN
SW14	Phase 4	Phase 3	Phase 3
SW15	OPEN	OPEN	OPEN

TABLE 1B-1

SW16	OPEN	OPEN	OPEN
SW17	OPEN	OPEN	OPEN

SWITCH OPERATION TABLE FOR BUCK / BUCK MODE OF OPERATION OF A µC CHARGE PUMP			
See, TABLE 1A	MODES OF OPERATION FOR BUCK / BUCK OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	Fourth Buck / Buck Mode, (μBB_{RATIO} = 2/3), where $V_{FIRST\text{-}OUTPUT}$ = 2/3 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 1/3 x V_{BAT}	Fifth Buck / Buck Mode, (μBB_{RATIO} = 3/4), where $V_{FIRST\text{-}OUTPUT}$ = 3/4 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 1/4 x V_{BAT}	OFF Mode where $V_{FIRST\text{-}OUTPUT}$ = FLOAT $V_{SECOND\text{-}OUTPUT}$ = FLOAT
SW1	Phase 1 and Phase 3	Phase 4	OPEN
SW2	Phase 2	Phase 3	OPEN
SW3	OPEN	OPEN	OPEN
SW4	Phase 1	Phase 1	OPEN
SW5	Phase 2 and Phase 3	Phase 3 and Phase 4	OPEN
SW6	Phase 1	Phase 2	OPEN
SW7	OPEN	OPEN	OPEN
SW8	Phase 2	Phase 3	OPEN
SW9	Phase 1	Phase 2	OPEN
SW10	OPEN	Phase 1	OPEN
SW11	OPEN	Phase 1	OPEN
SW12	Phase 3	Phase 4	OPEN
SW13	OPEN	OPEN	OPEN
SW14	OPEN	OPEN	OPEN
SW15	OPEN	OPEN	OPEN
SW16	OPEN	OPEN	OPEN
SW17	OPEN	OPEN	OPEN

TABLE 1B-2

SWITCH OPERATION TABLE FOR BUCK / BUCK MODE OF OPERATION OF A µC CHARGE PUMP			
See, TABLE 1A	MODES OF OPERATION FOR BUCK / BUCK OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	First Bypass Mode, (μBB_{RATIO} = permissible value), where $V_{FIRST\text{-}OUTPUT} = V_{BAT}$, and $V_{SECOND\text{-}OUTPUT} = \mu BB_{RATIO} \times V_{BAT}$	Second Bypass Mode, (μBB_{RATIO} = permissible value), where $V_{FIRST\text{-}OUTPUT} = \mu BB_{RATIO} \times V_{BAT}$, and $V_{SECOND\text{-}OUTPUT} = \mu BB_{RATIO} \times V_{BAT}$	Third Bypass Mode where $V_{FIRST\text{-}OUTPUT} = V_{BAT}$ $V_{SECOND\text{-}OUTPUT} = V_{BAT}$
SW1	X	X	CLOSED ALL PHASES
SW2	OPEN	X	CLOSED ALL PHASES
SW3	X	X	OPEN
SW4	OPEN	X	OPEN
SW5	X	X	OPEN
SW6	X	X	CLOSED ALL PHASES
SW7	OPEN	X	CLOSED ALL PHASES
SW8	X	X	OPEN
SW9	OPEN	X	OPEN
SW10	X	X	OPEN
SW11	X	X	OPEN
SW12	X	OPEN	OPEN
SW13	X	OPEN	CLOSED ALL PHASES
SW14	X	OPEN	OPEN

SW15	X	OPEN	OPEN
SW16	CLOSED ALL PHASES	X	CLOSED ALL PHASES
SW17	X	CLOSED ALL PHASES	CLOSED ALL PHASES

TABLE 1B-3

[001538] TABLE 1B-1 describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the First (1st) Buck / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/4 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 3/4 x V_{BAT}.

[001539] In the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the ninth switch 2464, (SW9), to place the first flying capacitor 2424 and the second flying capacitor 2426 in series between the battery voltage, V_{BAT}, and the first output 2416. Charge is transferred from the battery voltage, V_{BAT}, (V_{BAT}), to the first output capacitor 2420 via the first flying capacitor 2424 and the second flying capacitor 2426. The first flying capacitor voltage VFIRST-FLYCAP 2424FC and the second flying capacitor voltage VSECOND-FLYCAP 2426FC are subtracted from the battery voltage, V_{BAT}, to provide a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/4 x V_{BAT}, on the first output 2416. Also, during the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A configures the remaining µC charge pump switches to be open, which disconnects the second output 2418 from the first flying capacitor 2424 and the second flying capacitor 2426. In this case, the second output 2418 provides a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 3/4 x V_{BAT}, from the charge already stored on the second output capacitor 2422.

[001540] In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8), to place the second flying capacitor 2426 between

the first output 2416 and ground. The charge stored on the second flying capacitor 2426 and first output capacitor 2420 is sourced to the first output 2416 to provide the first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/4 x V_{BAT}. Similar to the first phase of operation, (Phase 1), the second output 2418 continues to provide the second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/4 x V_{BAT}, from the charge already stored on the second output capacitor 2422.

[001541] In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the ninth switch 2464, (SW9), and the tenth switch 2468, (SW10). As a result, the second terminal 2424B of the first flying capacitor 2424 is tied to ground, the first terminal 2424A of the first flying capacitor 2424 is coupled to the first terminal 2426A of the second flying capacitor 2426 and the second terminal 2426B of the second flying capacitor 2426 is coupled to the first output 2416.

[001542] Accordingly, charge stored on the first flying capacitor 2424 and the second flying capacitor 2426 is sourced to the first output 2416 to maintain the first output voltage $V_{FIRST-OUTPUT}$ 2416VO at a voltage level substantially equal to 1/4 x V_{BAT}. The a first output voltage $V_{FIRST-OUTPUT}$ 2416VO remains substantially equal to 1/4 x V_{BAT}, where the magnitude of the first output voltage $V_{FIRST-OUTPUT}$ 2416VO is determined by subtracting the second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC from the first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC. Similar to the first phase of operation, (Phase 1), and the second phase of operation, (Phase 2), the second output 2418 continues to provide the second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/4 x V_{BAT}, from the charge previously stored on the second output capacitor 2422.

[001543] In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), and the fourteenth switch 2484, (SW14). During the fourth phase of operation, (Phase 4), charge is transferred from the battery voltage,

V_{BAT}, to the second output capacitor 2422 via the first flying capacitor 2424 and the second flying capacitor 2426. The magnitude of the second output voltage VSECOND-OUTPUT 2418VO is determined by subtracting the second flying capacitor voltage VSECOND-FLYCAP 2426FC from the first flying capacitor voltage VFIRST-FLYCAP 2424FC and the battery voltage, V_{BAT}, (V_{BAT}). Accordingly, the second output 2418 provides a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 3/4 x V_{BAT}. During the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A configures the remaining µC charge pump switches to be open, which disconnects the first output 2416 from the first flying capacitor 2424 and the second flying capacitor 2426. As a result, the first output 2416 provides the first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/4 x V_{BAT}, from the charge stored on the first output capacitor 2420 during the other phases of operation.

[001544] Otherwise, the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17), remain open while the µC charge pump 2410 is configured to operate in the First (1^{st}) Buck / Buck Mode.

[001545] Having described the basic operation of the µC charge pump control circuit 2414A and the phases of operation of the µC charge pump 2410 in detail with respect to the case where the µC charge pump 2410 is configured to operate in the First (1st) Buck / Buck Mode, the remaining modes of operation of the µC charge pump 2410 will now be briefly described.

[001546] TABLE 1B-1 describes, and Figure 4 depicts, the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Second (2^{nd}) Buck / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}),

set to 1/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 2/3 x V_{BAT}.

[001547] As described in TABLE 1B-1 in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the third switch 2440, (SW3), the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the sixth switch 2452, (SW6), the twelfth switch 2476, (SW12), and the fourteenth switch 2484, (SW14). Otherwise, the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17), remain open while the µC charge pump 2410 is configured to operate in the Second (2^{nd}) Buck / Buck Mode.

[001548] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/3 x V_{BAT}, and the second output 2418 generates a

second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 2/3 x V_{BAT}.

[001549] TABLE 1B-1 describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Third (3^{rd}) Buck / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/2 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/2 x V_{BAT}.

[001550] As described in TABLE 1B-1, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fourth switch 2444, (SW4), the sixth switch 2452, (SW6), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the third switch 2440, (SW3), the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), tenth switch 2468, (SW10), the twelfth switch 2476, (SW12), and the fourteenth switch 2484, (SW14). As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/2 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/2 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/2 x V_{BAT} on the second output capacitor 2422.

[001551] TABLE 1B-2 describes, and Figure 6 depicts, the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Fourth (4^{th}) Buck / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND\text{-}OUTPUT}$ 2418VO substantially equal to 1/3 x V_{BAT}.

[001552] As described in TABLE 1B-2, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fourth switch 2444, (SW4), the sixth switch 2452, (SW6), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the twelfth switch 2476, (SW12).

[001553] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST\text{-}FLYCAP}$ 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND\text{-}FLYCAP}$ 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND\text{-}OUTPUT}$ 2418VO substantially equal to 1/3 x V_{BAT} on the second output capacitor 2422.

[001554] TABLE 1B-2 describesthe operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the

Fifth (5^{th}) Buck / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT}.

[001555] As described in TABLE 1B-2, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the fourth switch 2444, (SW4), the tenth switch 2468, (SW10), and the eleventh switch 2472, (SW11). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the sixth switch 2452, (SW6), and the ninth switch 2464, (SW9). As further described in TABLE 1B-2,in the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eighth switch 2460, (SW8). In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the twelfth switch 2476, (SW12).

[001556] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 3/4 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/4 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT} on the second output capacitor 2422.

[001557] As further described in TABLE 1B-2, the controller 50 may also configure the µC charge pump 2410 to operate in the OFF Mode of operation.

As described in Table 1A, when the µC charge pump 2410 is configured in the OFF Mode of operation, both the first output 2416 and second output 2418 float. As described in TABLE 1B-2, when the controller 50 configures the µC charge pump 2410 to be in the OFF Mode of operation, the µC charge pump control circuit 2414A may operablely open the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeent switch 2496, (SW17). As a result, the first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO on the first output 2416 floats relative to ground.

[001558] Likewise, the second output voltage $V_{SECOND\text{-}OUTPUT}$ 2418VO on the second output 2418 floats relative to ground. It will be appreciated, by those skilled in the art, that the configurations and phases of operation of the µC charge pump 2410 to achive thedditional buck / buck modes of operation, as described in TABLE 1B, including the Sixth (6^{th}) Buck / Buck Mode, the Seventh (7^{th}) Buck / Buck Mode, the Eighth (8^{th}) Buck / Buck Mode, the Ninth (9^{th}) Buck / Buck Mode, and the Tenth (10^{th}) Buck / Buck Mode, may be understood based on the foregoing description of the operation of the µC charge pump 2410 to operate in either a buck / boost mode of operation or a boost /buck mode of operation, as described below. Accordingly, a detailed description of the configurations and phases of operation of the µC charge pump 2410 to achive the additional buck / buck modes of operation, as described in TABLE 1B, are omitted for the sake of brevity andn not by way of limitation. In addition, as previously described with respect to the First Bypass Mode, the Second Bypass Mode, the Third Bypass Mode, the Fourth Bypass Mode, the Fifth Bypass Mode, and the Sixth Bypass Mode, the µC charge pump 2410 may buck or boost the battery voltage, (V_{BAT}), to obtain either a buck voltage output level or a boost

output voltage level on the non-bypassed output; the bypassed output may have an output voltage substantially equal to the battery voltage, (V_{BAT}).

[001559] A non-limiting set of example operational modes of the µC charge pump 2410 configured to operate in a buck / boost mode of operation will now be discussed. As an example, TABLE 2A-1 and TABLE 2A-2, entitled "MODES OF OPERATION TABLE FOR BUCK / BOOST OPERATION OF A DUAL OUTPUT µC CHARGE PUMP CIRCUIT," describe, in tablulated form, several, non-limiting, example modes of operation of the µC charge pump 2410 configured to operate in a buck / boost mode of operation. As an example, the non-limiting example modes of buck / boost modes of operation described in TABLE 2A-1 include: a First (1^{st}) Buck / Boost Mode, a Second (2^{nd}) Buck / Boost Mode, a Third (3^{rd}) Buck / Boost Mode, a Fourth (4^{th}) Buck / Boost Mode, a Fifth (5^{th}) Buck / Boost Mode, and an OFF Mode. As another example, the non-limiting example modes of buck / boost modes of operation described in TABLE 2A-2 include: a Sixth (6^{th}) Buck / Boost Mode, a Seventh (7^{th}) Buck / Boost Mode, an Eighth (8^{th}) Buck / Boost Mode, a Ninth (9^{th}) Buck / Boost Mode, a Tenth (10^{th}) Buck / Boost Mode, and an OFF Mode. Additional bypass modes are not described for the sake of brevity, but fall within the scope of the operation of the described embodiment of the µC charge pump 2410.

[001560] As depicted in TABLE 2A-1 and TABLE 2A-2, each example buck / boost mode of operation of the µC charge pump 2410 corresponds to an operational ratio, (μBB_{RATIO}), where the operational ratio, (μBB_{RATIO}), may provide a relationship between the first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO generated by the first output 2416 and the second output voltage $V_{SECOND\text{-}OUTPUT}$ 2418VO generated by the second output 2418. The operational ratio, (μBB_{RATIO}), may be an operational ratio parameter that is configured by the controller 50 and stored locally in the µC charge pump control circuit 2414A.

[001561] For example, TABLE 2A-1 describes example buck / boost modes of operation of the µC charge pump 2410 where the first output 2416 is configured to generate a first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO such that $V_{FIRST\text{-}OUTPUT} = (\mu BB_{RATIO}) \times V_{BAT}$. The second output 2418 is configured to generate a

second output voltage $V_{SECOND-OUTPUT}$ 2418VO such that $V_{SECOND-OUTPUT} = (1+\mu BB_{RATIO}) \times V_{BAT}$, where V_{BAT} is used to represent the magnitude of the voltage on the battery voltage, V_{BAT}.

[001562] Accordingly, as described in TABLE 2A-1, in the First Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/4 x V_{BAT}.

[001563] In the Second Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 4/3 x V_{BAT}.

[001564] In the Third Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/2 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/2 x V_{BAT}.

[001565] In the Fourth Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/3 x V_{BAT}.

[001566] In the Fifth Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 7/4 x V_{BAT}.

[001567] In the OFF Mode of operation of the µC charge pump 2410, the controller 50 configures the first output 2416 to float and the second output 2418 to float.

[001568] In contrast, TABLE 2A-2 describes other example buck / boost modes of operation of the µC charge pump 2410 where the first output 2416 is configured to generate a first output voltage $V_{FIRST-OUTPUT}$ 2416VO such that $V_{FIRST-OUTPUT} = (1-\mu BB_{RATIO}) \times V_{BAT}$. The second output 2418 is configured generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO such that $V_{SECOND-OUTPUT} = (1+\mu BB_{RATIO}) \times V_{BAT}$.

[001569] Accordingly, as described in TABLE 2A-2, in the Sixth Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/4 x V_{BAT}.

[001570] In the Seventh Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 4/3 x V_{BAT}.

[001571] In the Eighth Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/2 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/2 x V_{BAT}.

[001572] In the Ninth Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/3 x V_{BAT}.

[001573] In the Tenth Buck / Boost Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to1/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 7/4 x V_{BAT}.

[001574] In the OFF Mode of operation of the µC charge pump 2410, the controller 50 configures the first output 2416 to float and the second output 2418 to float.

[001575] TABLE 2B-1A and TABLE 2B-1B, entitled "SWITCH OPERATION TABLES FOR BUCK / BOOST OPERATION OF A µC CHARGE PUMP," describe the switch state (open or closed) of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the

fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17) of the µC charge pump 2410 when the µC charge pump 2410 is configured to operate in the buck / boost modes of operation described in TABLE 2A-1. In addition, TABLE 2B-1A and TABLE 2B-1B also provide the corresponding operational ratio, (μBB_{RATIO}), used by the µC charge pump 2410 when operating in the buck / boost modes of operation described in TABLE 2A-1. TABLE 2B-1A and TABLE 2B-1B further describe the switch state of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17) relative to the particular phases of operation used by the µC charge pump 2410 when operating in the buck / boost modes of operation described in TABLE 2A-1.

[001576] TABLE 2B-2A and TABLE 2B-2B, also entitled "SWITCH OPERATION TABLES FOR BUCK / BOOST OPERATION OF A µC CHARGE PUMP," describe the switch state (open or closed) of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17) of the µC charge pump 2410 when the µC charge pump 2410 is configured to operate in the buck / boost modes of operation described in TABLE 2A-2.

[001577] In addition, TABLE 2B-2A and TABLE 2B-2B also provide the corresponding operational ratio, (μBB_{RATIO}), used by the µC charge pump 2410 when operating in the buck / boost modes of operation described in TABLE 2A-2. TABLE 2B-2A and TABLE 2B-2B further describe the switch state of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17) relative to the particular phases of operation used by the µC charge pump 2410 when operating in the buck / boost modes of operation described in TABLE 2A-2.

[001578] As used in TABLE 2B-1A, TABLE 2B-1B, TABLE 2B-2A, and TABLE 2B-2A, "PHASE 1" indicates that the µC charge pump 2410 is configured to operate in a first phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the first phase of operation. "PHASE 2" indicates that the µC charge pump 2410 is configured to operate in a second phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the second phase of operation. "PHASE 3" indicates that the µC charge pump 2410 is configured to operate in a third phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the third phase of operation. "PHASE 4" indicates that the µC charge pump 2410 is configured to operate in a fourth phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the fourth phase of

operation. "OPEN" indicates that the μC charge pump control circuit 2414A configures the switch state (open or closed) of the identified switch to be closed during all the phases of operation of the μC charge pump 2410.

MODES OF OPERATION TABLE FOR BUCK / BOOST OPERATION OF A DUAL OUTPUT µC CHARGE PUMP CIRCUIT			
MODES OF OPERATION	OPERATIONAL RATIOS, (μBB_{RATIO})	$V_{FIRST\text{-}OUTPUT} = (\mu BB_{RATIO}) \times V_{BAT}$	$V_{SECOND\text{-}OUTPUT} = (1+ \mu BB_{RATIO}) \times V_{BAT}$
First Buck / Boost Mode	1/4	1/4 x V_{BAT}	5/4 x V_{BAT}
Second Buck / Boost Mode	1/3	1/3 x V_{BAT}	4/3 x V_{BAT}
Third Buck / Boost Mode	1/2	1/2 x V_{BAT}	3/2 x V_{BAT}
Fourth Buck / Boost Mode	2/3	2/3 x V_{BAT}	5/3 x V_{BAT}
Fifth Buck / Boost Mode	3/4	3/4 x V_{BAT}	7/4 x V_{BAT}
OFF Mode	OFF	FLOATING	FLOATING

TABLE 2A-1

MODES OF OPERATION TABLE FOR BUCK / BOOST OPERATION OF A DUAL OUTPUT µC CHARGE PUMP CIRCUIT			
MODES OF OPERATION	OPERATIONAL RATIOS, (μBB_{RATIO})	$V_{FIRST\text{-}OUTPUT} = (1 - \mu BB_{RATIO}) \times V_{BAT}$	$V_{SECOND\text{-}OUTPUT} = (1 + \mu BB_{RATIO}) \times V_{BAT}$
Sixth Buck / Boost Mode	1/4	$3/4 \times V_{BAT}$	$5/4 \times V_{BAT}$
Seventh Buck / Boost Mode	1/3	$2/3 \times V_{BAT}$	$4/3 \times V_{BAT}$
Eigth Buck / Boost Mode	1/2	$1/2 \times V_{BAT}$	$3/2 \times V_{BAT}$
Ninth Buck / Boost Mode	2/3	$1/3 \times V_{BAT}$	$5/3 \times V_{BAT}$
Tenth Buck / Boost Mode	3/4	$1/4 \times V_{BAT}$	$7/4 \times V_{BAT}$
OFF Mode	OFF	FLOATING	FLOATING

TABLE 2A-2

SWITCH OPERATION TABLE FOR BUCK / BOOST MODE OF OPERATION OF DUAL OUTPUT µC CHARGE PUMP			
See, TABLE 2A-1	MODES OF OPERATION FOR BUCK / BOOST OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	First Buck / Boost Mode, (μBB_{RATIO} = 1/4), where Vfirst-output = 1/4 x V_{BAT} and $V_{SECOND-OUTPUT}$ = 5/4 x V_{BAT}	Second Buck / Boost Mode, (μBB_{RATIO} = 1/3), where $V_{FIRST-OUTPUT}$ = 1/3 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 4/3 x V_{BAT}	Third Buck / Boost Mode, (μBB_{RATIO} = 1/2), where $V_{FIRST-OUTPUT}$ = 1/2 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 3/2 x V_{BAT}
SW1	Phase 1	Phase 1	Phase 1
SW2	OPEN	Phase 2	Phase 2
SW3	Phase 3	Phase 2	Phase 2
SW4	OPEN	OPEN	Phase 1
SW5	Phase 1	Phase 1	OPEN
SW6	OPEN	OPEN	Phase 1
SW7	Phase 2	Phase 2	Phase 2
SW8	Phase 2	Phase 2	Phase 2
SW9	Phase 1 and Phase 3	Phase 1	Phase 1
SW10	Phase 3 and Phase 4	Phase 3	Phase 3
SW11	OPEN	Phase 3	Phase 3
SW12	Phase 4	OPEN	OPEN
SW13	OPEN	Phase 3	Phase 3
SW14	OPEN	OPEN	OPEN
SW15	Phase 4	Phase 3	Phase 3
SW16	OPEN	OPEN	OPEN

TABLE 2B-1A

SW17	OPEN	OPEN	OPEN

SWITCH OPERATION TABLE FOR BUCK / BOOST MODE OF OPERATION OF DUAL OUTPUT µC CHARGE PUMP			
See, TABLE 2A-1	MODES OF OPERATION FOR BUCK / BOOST OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	Fourth Buck / Boost Mode, (μBB_{RATIO} = 2/3), where $V_{FIRST\text{-}OUTPUT}$ = 2/3 x V_{BAT} and $V_{SECOND\text{-}OUTPUT}$ = 5/3 x V_{BAT}	Fifth Buck / Boost Mode, (μBB_{RATIO} = 3/4), where $V_{FIRST\text{-}OUTPUT}$ = 3/4 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 7/4 x V_{BAT}	OFF Mode where $V_{FIRST\text{-}OUTPUT}$ = FLOAT $V_{SECOND\text{-}OUTPUT}$ = FLOAT
SW1	Phase 1	OPEN	OPEN
SW2	Phase 2	Phase 3	OPEN
SW3	OPEN	OPEN	OPEN
SW4	Phase 1	Phase 1	OPEN
SW5	Phase 2 and Phase 3	Phase 3 and Phase 4	OPEN
SW6	Phase 1	Phase 2	OPEN
SW7	OPEN	OPEN	OPEN
SW8	Phase 2	Phase 3	OPEN
SW9	Phase 1	Phase 2	OPEN
SW10	Phase 3	Phase 1 and Phase 4	OPEN
SW11	Phase 3	Phase 1 and Phase 4	OPEN
SW12	OPEN	OPEN	OPEN
SW13	Phase 3	Phase 4	OPEN
SW14	OPEN	OPEN	OPEN
SW15	OPEN	OPEN	OPEN

TABLE 2B-1B

SW16	OPEN	OPEN	OPEN
SW17	OPEN	OPEN	OPEN

SWITCH OPERATION TABLE FOR BUCK / BOOST MODE OF OPERATION OF DUAL OUTPUT µC CHARGE PUMP			
See, TABLE 2A-2	MODES OF OPERATION FOR BUCK / BOOST OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	Sixth Buck / Boost Mode, (μBB_{RATIO} = 1/4), where $V_{FIRST-OUTPUT}$ = 3/4 x V_{BAT} and $V_{SECOND-OUTPUT}$ = 5/4 x V_{BAT}	Seventh Buck / Boost Mode, (μBB_{RATIO} = 1/3), where $V_{FIRST-OUTPUT}$ = 2/3 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 4/3 x V_{BAT}	Eighth Buck / Boost Mode, (μBB_{RATIO} = 1/2), where $V_{FIRST-OUTPUT}$ = 1/2 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 3/2 x V_{BAT}
SW1	OPEN	Phase 1	Phase 1
SW2	Phase 3	Phase 2	Phase 2
SW3	OPEN	OPEN	Phase 2
SW4	Phase 1	Phase 1	Phase 1
SW5	Phase 3	Phase 2	OPEN
SW6	Phase 2	Phase 1	Phase 1
SW7	OPEN	OPEN	Phase 2
SW8	Phase 3	Phase 2	Phase 2
SW9	Phase 2	Phase 1	Phase 1
SW10	Phase 1 and Phase 4	Phase 3	Phase 3
SW11	Phase 1	Phase 3	Phase 3
SW12	Phase 4	OPEN	OPEN
SW13	OPEN	Phase 3	Phase 3
SW14	OPEN	OPEN	OPEN
SW15	Phase 4	Phase 3	Phase 3
SW16	OPEN	OPEN	OPEN

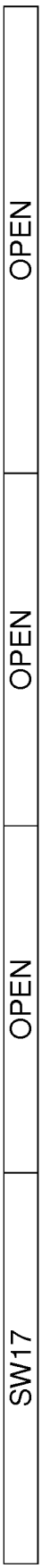


TABLE 2B-2A

SWITCH OPERATION TABLE FOR BUCK / BOOST MODE OF OPERATION OF DUAL OUTPUT µC CHARGE PUMP			
See, TABLE 2A-2	MODES OF OPERATION FOR BUCK / BOOST OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	Ninth Buck / Boost Mode, (μBB_{RATIO} = 2/3), where $V_{FIRST-OUTPUT}$ = 1/3 x V_{BAT} and $V_{SECOND-OUTPUT}$ = 5/3 x V_{BAT}	Tenth Buck / Boost Mode, (μBB_{RATIO} = 3/4), where $V_{FIRST-OUTPUT}$ = 1/4 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 7/4 x V_{BAT}	OFF Mode where $V_{FIRST-OUTPUT}$ = FLOAT $V_{SECOND-OUTPUT}$ = FLOAT
SW1	Phase 1	Phase 1	OPEN
SW2	Phase 2	OPEN	OPEN
SW3	Phase 2	Phase 3	OPEN
SW4	OPEN	OPEN	OPEN
SW5	Phase 1 and Phase 3	Phase 1 and Phase 4	OPEN
SW6	OPEN	OPEN	OPEN
SW7	Phase 2	Phase 2	OPEN
SW8	Phase 2	Phase 2	OPEN
SW9	Phase 1	Phase 1 and Phase 3	OPEN
SW10	Phase 3	Phase 3 and Phase 4	OPEN
SW11	Phase 3	Phase 4	OPEN
SW12	OPEN	OPEN	OPEN
SW13	Phase 3	Phase 4	OPEN
SW14	OPEN	OPEN	OPEN
SW15	OPEN	OPEN	OPEN
SW16	OPEN	OPEN	OPEN
SW17	OPEN	OPEN	OPEN

TABLE 2B-2B

[001579] The configurations and operations of the µC charge pump 2410 when the µC charge pump 2410 operates in the various buck / boost modes, described in the TABLE 2A-1 and the TABLE 2A-2, will now be discussed with reference to the TABLE 2B-1A, the TABLE 2B-1B, the TABLE 2B-2A, and the TABLE 2B-2B.

[001580] TABLE 2B-1A describes, and Figures 8A-B depicts, the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the First Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/4 x V_{BAT}.

[001581] As described in TABLE 2B-1A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the ninth switch 2464, (SW9), and the tenth switch 2468, (SW10). In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the twelfth switch 2476, (SW12), and the fifteenth switch 2488, (SW15).

[001582] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO

substantially equal to 1/4 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/4 x V_{BAT} on the second output capacitor 2422.

[001583] TABLE 2B-1A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Second Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 4/3 x V_{BAT}.

[001584] As described in TABLE 2B-1A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the third switch 2440, (SW3), the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the thirteenth switch 2480, (SW13), and the fifteenth switch 2488, (SW15).

[001585] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/3 x V_{BAT}, on the first output capacitor 2420 and the

second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 4/3 x V_{BAT} on the second output capacitor 2422.

[001586] TABLE 2B-1A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Third Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/2 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/2 x V_{BAT}.

[001587] As further described in TABLE 2B-1A and depicted in Figure 10, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6),and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the third switch 2440, (SW3), the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the thirteenth switch 2480, (SW13), and the fifteenth switch 2488, (SW15).

[001588] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/2 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 1/2 x V_{BAT}, on the first output capacitor 2420 and the

second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/2 x V_{BAT} on the second output capacitor 2422.

[001589] TABLE 2B-1B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Fourth Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/3 x V_{BAT}.

[001590] As further described in TABLE 2B-1B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fourth switch 2444, (SW4), the sixth switch 2452, (SW6), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), and the thirteenth switch 2480, (SW13).

[001591] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-}$

OUTPUT 2418VO substantially equal to 5/3 x V_{BAT} on the second output capacitor 2422.

[001592] TABLE 2B-1B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Fifth Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 3/4 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 7/4 x V_{BAT}.

[001593] As further described in TABLE 2B-1B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the fourth switch 2444, (SW4), the tenth switch 2468, (SW10), and the eleventh switch 2472, (SW11). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the sixth switch 2452, (SW6), and the ninth switch 2464, (SW9). As further depicted in Figure 12B, in the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eighth switch 2460, (SW8). In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), and the thirteenth switch 2480, (SW13).

[001594] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 3/4 x V_{BAT}, on the first output capacitor 2420 and the

second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 7/4 x V_{BAT} on the second output capacitor 2422.

[001595] TABLE 2B-2A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Sixth Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/4 x V_{BAT}.

[001596] As described in TABLE 2B-2A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the fourth switch 2444, (SW4), the tenth switch 2468, (SW10), and the eleventh switch 2472, (SW11). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the sixth switch 2452, (SW6), and the ninth switch 2464, (SW9). As further depicted in Figure 13B, in the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eighth switch 2460, (SW8). In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the twelfth switch 2476, (SW12), and the fifteenth switch 2488, (SW15).

[001597] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/4 x V_{BAT}, on the first output capacitor 2420 and the

second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 5/4 x V_{BAT} on the second output capacitor 2422.

[001598] TABLE 2B-2A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Seventh Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 4/3 x V_{BAT}.

[001599] As described in TABLE 2B-2A , in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fourth switch 2444, (SW4), the sixth switch 2452, (SW6), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the thirteenth switch 2480, (SW13), and the fifteenth switch 2488, (SW15).

[001600] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 2/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-}$

OUTPUT 2418VO substantially equal to 4/3 x V_{BAT} on the second output capacitor 2422.

[001601] TABLE 2B-2A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Eighth Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/2 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 3/2 x V_{BAT}.

[001602] As further described in TABLE 2B-2A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6),and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the third switch 2440, (SW3), the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the thirteenth switch 2480, (SW13), and the fifteenth switch 2488, (SW15).

[001603] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/2 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/2 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage VSECOND-

OUTPUT 2418VO substantially equal to 3/2 x V_{BAT} on the second output capacitor 2422.

[001604] TABLE 2B-2B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Ninth Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/3 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 5/3 x V_{BAT}.

[001605] As further described in TABLE 2B-2B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the third switch 2440, (SW3), the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), and the thirteenth switch 2480, (SW13).

[001606] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage VSECOND-

OUTPUT 2418VO substantially equal to 5/3 x V_{BAT} on the second output capacitor 2422.

[001607] TABLE 2B-2B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Tenth Buck / Boost Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/4 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 7/4 x V_{BAT}.

[001608] As further described in TABLE 2B-2B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the ninth switch 2464, (SW9). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the seventh switch 2456, (SW7), and the eighth switch 2460, (SW8). As further depicted in Figure 16B, in the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the ninth switch 2464, (SW9), and the tenth switch 2468, (SW10). In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), and the thirteenth switch 2480, (SW13).

[001609] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 1/4 x V_{BAT}, on the first output capacitor 2420 and the

second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 7/4 x V_{BAT} on the second output capacitor 2422.

[001610] Both the TABLE 2B-1B and the TABLE 2B-2B describe the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the OFF Mode. As described in both the TABLE 2B-1B and the TABLE 2B-2B, when the controller 50 configures the µC charge pump 2410 to be in the OFF Mode of operation, the µC charge pump control circuit 2414A may operablely open the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), and the fifteenth switch 2488, (SW15). As a result, the first output voltage $V_{FIRST-OUTPUT}$ 2416VO on the first output 2416 floats relative to ground. Likewise, the second output voltage $V_{SECOND-OUTPUT}$ 2418VO on the second output 2418 floats relative to ground.

[001611] A non-limiting set of example operational modes of the µC charge pump 2410 configured to operate in a boost / buck mode of operation will now be discussed. As an example, TABLE 3A-1 and TABLE 3A-2, entitled "MODES OF OPERATION TABLE FOR BOOST / BUCK OPERATION OF A DUAL OUTPUT µC CHARGE PUMP CIRCUIT," describe, in tablulated form, several, non-limiting, example modes of operation of the µC charge pump 2410 configured to operate in a boost / buck mode of operation. As an example, the non-limiting example modes of boost / buck modes of operation described in TABLE 3A-1 include: a First (1^{st}) Boost / Buck Mode, a Second (2^{nd}) Boost / Buck Mode, a Third (3^{rd}) Boost / Buck Mode, a Fourth (4^{th}) Boost / Buck Mode, a Fifth (5^{th}) Boost / Buck Mode, and an OFF Mode. As another example, the non-limiting example modes of boost / buck modes of operation described in TABLE 3A-2 include: a Sixth (6^{th}) Boost / Buck Mode, a Seventh (7^{th}) Boost / Buck Mode, an Eighth (8^{th}) Boost /

Buck Mode, a Ninth (9th) Boost / Buck Mode, a Tenth (10th) Boost / Buck Mode, and an OFF Mode.

[001612] As depicted in TABLE 3A-1 and TABLE 3A-2, each example boost / buck mode of operation of the µC charge pump 2410 corresponds to an operational ratio, (μBB_{RATIO}), where the operational ratio, (μBB_{RATIO}), may provide a relationship between the first output voltage $V_{FIRST-OUTPUT}$ 2416VO generated by the first output 2416 and the second output voltage $V_{SECOND-OUTPUT}$ 2418VO generated by the second output 2418. The operational ratio, (μBB_{RATIO}), may be an operational ratio parameter that is configured by the controller 50 and stored locally in the µC charge pump control circuit 2414A.

[001613] For example, TABLE 3A-1 describes example boost / buck modes of operation of the µC charge pump 2410 where the first output 2416 is configured to generate a first output voltage $V_{FIRST-OUTPUT}$ 2416VO such that $V_{FIRST-OUTPUT} = (1+ \mu BB_{RATIO}) \times V_{BAT}$. The second output 2418 is configured to generate a second output voltage $V_{SECOND-OUTPUT}$ 2418VO such that $V_{SECOND-OUTPUT} = (\mu BB_{RATIO}) \times V_{BAT}$.

[001614] Accordingly, as described in TABLE 3A-1, in the First Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to $5/4 \times V_{BAT}$, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to $1/4 \times V_{BAT}$.

[001615] In the Second Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to $4/3 \times V_{BAT}$, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to $1/3 \times V_{BAT}$.

[001616] In the Third Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/2 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/2 x V_{BAT}.

[001617] In the Fourth Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 5/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 2/3 x V_{BAT}.

[001618] In the Fifth Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 7/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/4 x V_{BAT}.

[001619] In the OFF Mode of operation of the µC charge pump 2410, the controller 50 configures the first output 2416 to float and the second output 2418 to float.

[001620] In contrast, TABLE 3A-2 describes other example boost / buck modes of operation of the µC charge pump 2410 where the first output 2416 is configured to generate a first output voltage $V_{FIRST-OUTPUT}$ 2416VO such that $V_{FIRST-OUTPUT} = (1+ \mu BB_{RATIO}) \times V_{BAT}$. The second output 2418 is configured to generate a second output voltage $V_{SECOND-OUTPUT}$ 2418VO such that $V_{SECOND-OUTPUT} = (1 - \mu BB_{RATIO}) \times V_{BAT}$.

[001621] Accordingly, as described in TABLE 3A-2, in the Sixth Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 5/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/4 x V_{BAT}. In the Seventh Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 4/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 2/3 x V_{BAT}. In the Eighth Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 3/2 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/2 x V_{BAT}. In the Ninth Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 5/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/3 x V_{BAT}. In the Tenth Boost / Buck Mode of operation of the µC charge pump 2410, the controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. As a result, the first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 7/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT}. In the OFF Mode of operation of the µC charge pump 2410, the

controller 50 configures the first output 2416 to float and the second output 2418 to float.

[001622] TABLE 3B-1A and TABLE 3B-1B, entitled "SWITCH OPERATION TABLE FOR BUCK / BOOST OPERATION OF DUAL OUTPUT µC CHARGE PUMP," describe, in tabular form, the switch state (open or closed) of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), and the fifteenth switch 2488, (SW15), of the µC charge pump 2410 when the µC charge pump 2410 is configured to operate in the boost / buck modes of operation described in TABLE 3A-1. In addition, TABLE 3B-1A and TABLE 3B-1B also provide the corresponding operational ratio, (μBB_{RATIO}), used by the µC charge pump 2410 when operating in the boost / buck modes of operation described in TABLE 3A-1. TABLE 3B-1A and TABLE 3B-1B further describe the switch state of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), and the fifteenth switch 2488, (SW15), relative to the particular phases of operation used by the µC charge pump 2410 when operating in the boost / buck modes of operation described in TABLE 3A-1.

[001623] TABLE 3B-2A and TABLE 3B-2B, also entitled "SWITCH OPERATION TABLE FOR BUCK / BOOST OPERATION OF A µC CHARGE PUMP," describe the switch state (open or closed) of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth

switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17) of the µC charge pump 2410 when the µC charge pump 2410 is configured to operate in the boost / buck modes of operation described in TABLE 3A-2. In addition, TABLE 3B-2A and TABLE 3B-2B also provide the corresponding operational ratio, (μBB_{RATIO}), used by the µC charge pump 2410 when operating in the boost / buck modes of operation described in TABLE 3A-2. TABLE 3B-2A and TABLE 3B-2B further describe the switch state of each of the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15), the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17) relative to the particular phases of operation used by the µC charge pump 2410 when operating in the boost / buck modes of operation described in TABLE 3A-2.

[001624] As used in TABLE 3B-1A, TABLE 3B-1B, TABLE 3B-2A, and TABLE 3B-2A, "PHASE 1" indicates that the µC charge pump 2410 is configured to operate in a first phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the first phase of operation. "PHASE 2" indicates that the µC charge pump 2410 is configured to operate in a second phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the second phase of operation. "PHASE 3" indicates that the µC charge pump 2410 is configured to

operate in a third phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the third phase of operation. "PHASE 4" indicates that the µC charge pump 2410 is configured to operate in a fourth phase of operation, where the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified µC charge pump switch to be closed during the time period of the fourth phase of operation. "OPEN" indicates that the µC charge pump control circuit 2414A configures the switch state (open or closed) of the identified switch to be closed during all the phases of operation of the µC charge pump 2410.

MODES OF OPERATION TABLE FOR BOOST/ BUCK OPERATION OF A µC CHARGE PUMP CIRCUIT			
MODES OF OPERATION	OPERATIONAL RATIOS, (μBB_{RATIO})	$V_{FIRST\text{-}OUTPUT} = (1+\mu BB_{RATIO}) \times V_{BAT}$	$V_{SECOND\text{-}OUTPUT} = (\mu BB_{RATIO}) \times V_{BAT}$
First Boost / Buck Mode	1/4	5/4 x V_{BAT}	1/4 x V_{BAT}
Second Boost / Buck Mode	1/3	4/3 x V_{BAT}	1/3 x V_{BAT}
Third Boost / Buck Mode	1/2	3/2 x V_{BAT}	1/2 x V_{BAT}
Fourth Boost / Buck Mode	2/3	5/3 x V_{BAT}	2/3 x V_{BAT}
Fifth Boost / Buck Mode	3/4	7/4 x V_{BAT}	3/4 x V_{BAT}
OFF Mode	OFF	FLOATING	FLOATING

TABLE 3A-1

MODES OF OPERATION TABLE FOR BOOST / BUCK OPERATION OF A µC CHARGE PUMP CIRCUIT			
MODES OF OPERATION	OPERATIONAL RATIOS, (μBB_{RATIO})	$V_{FIRST\text{-}OUTPUT} = (1 + \mu BB_{RATIO}) \times V_{BAT}$	$V_{SECOND\text{-}OUTPUT} = (1 - \mu BB_{RATIO}) \times V_{BAT}$
Sixth Boost / Buck Mode	1/4	5/4 x V_{BAT}	3/4 x V_{BAT}
Seventh Boost / Buck Mode	1/3	4/3 x V_{BAT}	2/3 x V_{BAT}
Eighth Boost / Buck Mode	1/2	3/2 x V_{BAT}	1/2 x V_{BAT}
Ninth Boost / Buck Mode	2/3	5/3 x V_{BAT}	1/3 x V_{BAT}
Tenth Boost / Buck Mode	3/4	7/4 x V_{BAT}	1/4 x V_{BAT}
OFF Mode	OFF	FLOATING	FLOATING

TABLE 3A-2

SWITCH OPERATION TABLE FOR BOOST / BUCK MODE OF OPERATION OF A µC CHARGE PUMP			
See, TABLE 3A-1	MODES OF OPERATION FOR BOOST / BUCK OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	First Boost / Buck Mode, (μBB_{RATIO} = 1/4), where $V_{FIRST\text{-}OUTPUT}$ = 5/4 x V_{BAT} and $V_{SECOND\text{-}OUTPUT}$ = 1/4 x V_{BAT}	Second Boost / Buck Mode, (μBB_{RATIO} = 1/3), where $V_{FIRST\text{-}OUTPUT}$ = 4/3 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 1/3 x V_{BAT}	Third Boost / Buck Mode, (μBB_{RATIO} = 1/2), where $V_{FIRST\text{-}OUTPUT}$ = 3/2 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 1/2 x V_{BAT}
SW1	Phase 1	Phase 1	Phase 1
SW2	OPEN	Phase 3	Phase 3
SW3	Phase 3	Phase 2	Phase 2
SW4	OPEN	OPEN	OPEN
SW5	Phase 1	Phase 1	OPEN
SW6	OPEN	OPEN	Phase 1
SW7	OPEN	Phase 3	Phase 3
SW8	Phase 2	Phase 2	Phase 2
SW9	Phase 4	OPEN	OPEN
SW10	Phase 3 and Phase 4	Phase 2	Phase 2
SW11	OPEN	Phase 3	Phase 3
SW12	Phase 1 and Phase 3	Phase 1	Phase 1
SW13	Phase 2	Phase 2	Phase 2
SW14	OPEN	OPEN	Phase 1
SW15	Phase 4	Phase 3	Phase 3
SW16	OPEN	OPEN	OPEN

TABLE 3B-1A

SW17	OPEN	OPEN	OPEN

SWITCH OPERATION TABLE FOR BOOST / BUCK MODE OF OPERATION OF A µC CHARGE PUMP			
See, TABLE 3A-1	MODES OF OPERATION FOR BOOST / BUCK OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	Fourth Boost / Buck Mode, (μBB_{RATIO} = 2/3), where $V_{FIRST\text{-}OUTPUT}$ = 5/3 x V_{BAT} and $V_{SECOND\text{-}OUTPUT}$ = 2/3 x V_{BAT}	Fifth Boost / Buck Mode, (μBB_{RATIO} = 3/4), where $V_{FIRST\text{-}OUTPUT}$ = 7/4 x V_{BAT}, and $V_{SECOND\text{-}OUTPUT}$ = 3/4 x V_{BAT}	OFF Mode where $V_{FIRST\text{-}OUTPUT}$ = FLOAT $V_{SECOND\text{-}OUTPUT}$ = FLOAT
SW1	Phase 1	OPEN	OPEN
SW2	Phase 3	Phase 4	OPEN
SW3	OPEN	OPEN	OPEN
SW4	OPEN	OPEN	OPEN
SW5	Phase 2 and Phase 3	Phase 3 and Phase 4	OPEN
SW6	Phase 1	Phase 2	OPEN
SW7	OPEN	OPEN	OPEN
SW8	Phase 2	Phase 3	OPEN
SW9	OPEN	OPEN	OPEN
SW10	Phase 2	Phase 1 and Phase 3	OPEN
SW11	Phase 3	Phase 1 and Phase 4	OPEN
SW12	Phase 1	Phase 2	OPEN
SW13	Phase 2	Phase 3	OPEN
SW14	Phase 1	Phase 1	OPEN
SW15	OPEN	OPEN	OPEN
SW16	OPEN	OPEN	OPEN

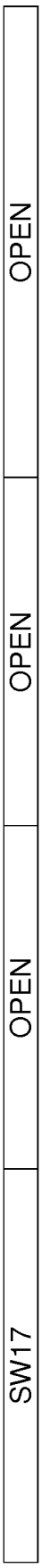


TABLE 3B-1B

SWITCH OPERATION TABLE FOR BOOST / BUCK MODE OF OPERATION OF A µC CHARGE PUMP			
See, TABLE 3A-2	MODES OF OPERATION FOR BOOST / BUCK OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	Sixth Boost / Buck Mode, (μBB_{RATIO} = 1/4), where $V_{FIRST-OUTPUT}$ = 5/4 x V_{BAT} and $V_{SECOND-OUTPUT}$ = 3/4 x V_{BAT}	Seventh Boost / Buck Mode, (μBB_{RATIO} = 1/3), where $V_{FIRST-OUTPUT}$ = 4/3 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 2/3 x V_{BAT}	Eighth Boost / Buck Mode, (μBB_{RATIO} = 1/2), where $V_{FIRST-OUTPUT}$ = 1/2 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 3/2 x V_{BAT}
SW1	OPEN	Phase 1	Phase 1
SW2	OPEN	Phase 3	Phase 3
SW3	OPEN	OPEN	Phase 2
SW4	OPEN	OPEN	OPEN
SW5	Phase 3	Phase 2	OPEN
SW6	Phase 2	Phase 1	Phase 1
SW7	OPEN	Phase 3	Phase 3
SW8	Phase 3	Phase 2	Phase 2
SW9	Phase 4	OPEN	OPEN

SW10	Phase 1, Phase 3 and Phase 4	Phase 2	Phase 2
SW11	Phase1	Phase 3	Phase 3
SW12	Phase 2	Phase 1	Phase 1
SW13	Phase 3	Phase 2	Phase 2
SW14	Phase 1	Phase 1	Phase 1
SW15	Phase 4	Phase 3	Phase 3
SW16	OPEN	OPEN	OPEN
SW17	OPEN	OPEN	OPEN

TABLE 3B-2A

SWITCH OPERATION TABLE FOR BOOST / BUCK MODE OF OPERATION OF A µC CHARGE PUMP			
See, TABLE 3A-2	MODES OF OPERATION FOR BOOST / BUCK OPERATION OF DUAL OUTPUT µC CHARGE PUMP WITH CORRESPONDING OPERATIONAL RATIOS, (μBB_{RATIO})		
µC CHARGE PUMP SWITCHES	Ninth Boost / Buck Mode, (μBB_{RATIO} = 2/3), where $V_{FIRST-OUTPUT}$ = 5/3 x V_{BAT} and $V_{SECOND-OUTPUT}$ = 1/3 x V_{BAT}	Tenth Boost / Buck Mode, (μBB_{RATIO} = 3/4), where $V_{FIRST-OUTPUT}$ = 7/4 x V_{BAT}, and $V_{SECOND-OUTPUT}$ = 1/4 x V_{BAT}	OFF Mode where $V_{FIRST-OUTPUT}$ = FLOAT $V_{SECOND-OUTPUT}$ = FLOAT
SW1	Phase 1	Phase 1	OPEN
SW2	Phase 3	Phase 4	OPEN
SW3	Phase 2	Phase 3	OPEN
SW4	OPEN	OPEN	OPEN
SW5	Phase 1 and Phase 3	Phase 1 and Phase 4	OPEN
SW6	OPEN	OPEN	OPEN
SW7	OPEN	OPEN	OPEN
SW8	Phase 2	Phase 2	OPEN
SW9	OPEN	OPEN	OPEN
SW10	Phase 2	Phase 3	OPEN
SW11	Phase 3	Phase 4	OPEN
SW12	Phase 1	Phase 1 and Phase 3	OPEN
SW13	Phase 2	Phase 2	OPEN
SW14	OPEN	OPEN	OPEN
SW15	OPEN	OPEN	OPEN
SW16	OPEN	OPEN	OPEN

SW17	OPEN	OPEN	OPEN

TABLE 3B-2B

[001625] The configurations and operations of the μC charge pump 2410 when the μC charge pump 2410 operates in the various boost / buck modes, described in the TABLE 3A-1 and the TABLE 3A-2, will now be discussed with reference to the TABLE 3B-1A, the TABLE 3B-1B, the TABLE 3B-2A, and the TABLE 3B-2B.

[001626] TABLE 3B-1A describes the operation of the μC charge pump 2410 when the controller 50 configures the μC charge pump 2410 to operate in the First Boost / Buck Mode. The controller 50 configures the μC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. The μC charge pump control circuit 2414A operably divides the operation of the μC charge pump 2410 into four phases of operation. The μC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 5/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT}.

[001627] As described in TABLE 3B-1A, in the first phase of operation, (Phase 1), the μC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the twelfth switch 2476, (SW12). In the second phase of operation, (Phase 2), the μC charge pump control circuit 2414A operably closes the eighth switch 2460, (SW8) and the thirteenth switch 2480, (SW13). As further depicted in Figure 17B, in the third phase of operation, (Phase 3), the μC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the tenth switch 2468, (SW10), and the twelfth switch 2476, (SW12). In the fourth phase of operation, (Phase 4), the μC charge pump control circuit 2414A operably closes the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), and the fifteenth switch 2488, (SW15).

[001628] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially

equal to 5/4 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT} on the second output capacitor 2422.

[001629] TABLE 3B-1A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Second Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 4/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/3 x V_{BAT}.

[001630] As described in TABLE 3B-1A , in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the tenth switch 2468, (SW10). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the seventh switch 2456, (SW7), the eleventh switch 2472, (SW11), and the fifteenth switch 2488, (SW15).

[001631] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 4/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-}$

OUTPUT 2418VO substantially equal to 1/3 x V_{BAT} on the second output capacitor 2422.

[001632] TABLE 3B-1A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Third Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 3/2 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 1/2 x V_{BAT}.

[001633] As further described in TABLE 3B-1A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the sixth switch 2452, (SW6), the twelfth switch 2476, (SW12), and the fourteenth switch 2484, (SW14). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the seventh switch 2456, (SW7), the eleventh switch 2472, (SW11), and the fifteenth switch 2488, (SW15).

[001634] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/2 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 3/2 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage VSECOND-

OUTPUT 2418VO substantially equal to 1/2 x V_{BAT} on the second output capacitor 2422.

[001635] TABLE 3B-1B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Fourth Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 5/3 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 2/3 x V_{BAT}.

[001636] As further described in TABLE 3B-1B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the sixth switch 2452, (SW6), the twelfth switch 2476, (SW12), and the fourteenth switch 2484, (SW14). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eleventh switch 2472, (SW11).

[001637] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 5/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage VSECOND-

OUTPUT 2418VO substantially equal to 2/3 x V_{BAT} on the second output capacitor 2422.

[001638] TABLE 3B-1B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Fifth Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 7/4 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 3/4 x V_{BAT}.

[001639] As further described in TABLE 3B-1B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), and the fourteenth switch 2484, (SW14). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the sixth switch 2452, (SW6), and the twelfth switch 2476, (SW12). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13). In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eleventh switch 2472, (SW11).

[001640] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 7/4 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage VSECOND-

OUTPUT 2418VO substantially equal to 3/4 x V_{BAT} on the second output capacitor 2422.

[001641] TABLE 3B-2A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Sixth Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 5/4 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 3/4 x V_{BAT}.

[001642] As described in TABLE 3B-2A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), and the fourteenth switch 2484, (SW14). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the sixth switch 2452, (SW6), and the twelfth switch 2476, (SW12). As further depicted in Figure 22B, in the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13).. In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), and the fifteenth switch 2488, (SW15).

[001643] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 5/4 x V_{BAT}, on the first output capacitor 2420 and the

second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 3/4 x V_{BAT} on the second output capacitor 2422.

[001644] TABLE 3B-2A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Seventh Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 4/3 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 2/3 x V_{BAT}.

[001645] As described in TABLE 3B-2A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the sixth switch 2452, (SW6), the twelfth switch 2476, (SW12), and the fourteenth switch 2484, (SW14). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the fifth switch 2448, (SW5), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the seventh switch 2456, (SW7), the eleventh switch 2472, (SW11), and the fifteenth switch 2488, (SW15).

[001646] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 4/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-}$

OUTPUT 2418VO substantially equal to 2/3 x V_{BAT} on the second output capacitor 2422.

[001647] TABLE 3B-2A describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Eighth Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 1/2. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 3/2 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 1/2 x V_{BAT}.

[001648] As further described in TABLE 3B-2A, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the sixth switch 2452, (SW6), the twelfth switch 2476, (SW12), and the fourteenth switch 2484, (SW14). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the seventh switch 2456, (SW7), the eleventh switch 2472, (SW11), and the fifteenth switch 2488, (SW15).

[001649] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/2 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 3/2 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage VSECOND-

OUTPUT 2418VO substantially equal to 1/2 x V_{BAT} on the second output capacitor 2422.

[001650] TABLE 3B-2B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Ninth Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 2/3. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into three phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 5/3 x V_{BAT}, and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 1/3 x V_{BAT}.

[001651] As further described in TABLE 3B-2B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the twelfth switch 2476, (SW12). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the eighth switch 2460, (SW8), the tenth switch 2468, (SW10), and the thirteenth switch 2480, (SW13). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eleventh switch 2472, (SW11).

[001652] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage VFIRST-FLYCAP 2424FC substantially equal to 1/3 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage VSECOND-FLYCAP 2426FC substantially equal to 1/3 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage VFIRST-OUTPUT 2416VO substantially equal to 5/3 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage VSECOND-OUTPUT 2418VO substantially equal to 1/3 x V_{BAT} on the second output capacitor 2422.

[001653] TABLE 3B-2B describes the operation of the µC charge pump 2410 when the controller 50 configures the µC charge pump 2410 to operate in the Tenth Boost / Buck Mode. The controller 50 configures the µC charge pump control circuit 2414A to use an operational ratio, (μBB_{RATIO}), set to 3/4. The µC charge pump control circuit 2414A operably divides the operation of the µC charge pump 2410 into four phases of operation. The µC charge pump control circuit 2414A operably configures the switching network 2412 such that first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 7/4 x V_{BAT}, and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT}.

[001654] As further described in TABLE 3B-2B, in the first phase of operation, (Phase 1), the µC charge pump control circuit 2414A operably closes the first switch 2432, (SW1), the fifth switch 2448, (SW5), and the twelfth switch 2476, (SW12). In the second phase of operation, (Phase 2), the µC charge pump control circuit 2414A operably closes the eighth switch 2460, (SW8), and the thirteenth switch 2480, (SW13). In the third phase of operation, (Phase 3), the µC charge pump control circuit 2414A operably closes the third switch 2440, (SW3), the tenth switch 2468, (SW10), and the twelfth switch 2476, (SW12). In the fourth phase of operation, (Phase 4), the µC charge pump control circuit 2414A operably closes the second switch 2436, (SW2), the fifth switch 2448, (SW5), and the eleventh switch 2472, (SW11).

[001655] As a result, the first flying capacitor 2424 develops a first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC substantially equal to 1/2 x V_{BAT}, and the second flying capacitor 2426 develops a second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC substantially equal to 1/4 x V_{BAT}. Accordingly, first output 2416 generates a first output voltage $V_{FIRST-OUTPUT}$ 2416VO substantially equal to 7/4 x V_{BAT}, on the first output capacitor 2420 and the second output 2418 generates a second output voltage $V_{SECOND-OUTPUT}$ 2418VO substantially equal to 1/4 x V_{BAT} on the second output capacitor 2422.

[001656] Both the TABLE 3B-1B and the TABLE 3B-2B describe the operation of the μC charge pump 2410 when the controller 50 configures the μC charge pump 2410 to operate in the OFF Mode. As described in both the TABLE 3B-1B and the TABLE 3B-2B, when the controller 50 configures the μC charge pump 2410 to be in the OFF Mode of operation, the μC charge pump control circuit 2414A may operably open the first switch 2432, (SW1), the second switch 2436, (SW2), the third switch 2440, (SW3), the fourth switch 2444, (SW4), the fifth switch 2448, (SW5), the sixth switch 2452, (SW6), the seventh switch 2456, (SW7), the eighth switch 2460, (SW8), the ninth switch 2464, (SW9), the tenth switch 2468, (SW10), the eleventh switch 2472, (SW11), the twelfth switch 2476, (SW12), the thirteenth switch 2480, (SW13), the fourteenth switch 2484, (SW14), the fifteenth switch 2488, (SW15) the sixteenth switch 2492, (SW16), and the seventeenth switch 2496, (SW17). As a result, the first output voltage $V_{FIRST\text{-}OUTPUT}$ 2416VO on the first output 2416 floats relative to ground. Likewise, the second output voltage $V_{SECOND\text{-}OUTPUT}$ 2418VO on the second output 2418 floats relative to ground.

[001657] Returning briefly to Figure 53A, in some operational modes of the µC charge pump system 2400, the µC charge pump 2410 may be configured to provide various "floating" modes of operation, as depicted in TABLE 5.

FLOATING MODES OF OPERATION FOR A MULTIPLE OUTPUT µC CHARGE PUMP		
MODES OF OPERATION	$V_{FIRST-OUTPUT}$	$V_{SECOND-OUTPUT}$
OFF Mode	$V_{FIRST-OUTPUT}$ = FLOATING (PRESENTS HIGH IMPEDANCE PATH TO GROUND)	$V_{SECOND-OUTPUT}$ = FLOATING (PRESENTS HIGH IMPEDANCE PATH TO GROUND)
1st Floating Mode	$V_{FIRST-OUTPUT}$ = FLOATING	Permissible Modes of Operation
2nd Floating Mode	Permissible Mode of Operation	$V_{SECOND-OUTPUT}$ = FLOATING

TABLE 5

[001658] Figure 53B depicts an embodiment of a µC charge pump system 2640 configured to generated the charge a first output voltage $V_{FIRST-OUTPUT}$ 2412VO at the first output 2414, a second output voltage $V_{SECOND-OUTPUT}$ 2418VO at the second output 2418, and a third output voltage $V_{THIRD-OUTPUT}$ 2644VO at the third output 2544. The µC charge pump system 2640 may be substantially the same in form and function as the µC charge pump system 2400 depicted in Figure 53A. However, the µC charge pump system 2640 includes a µC charge pump 2650. The µC charge pump 2650 is substantially similar in form and function as the µC charge pump 2410 except the µC charge pump 2650 includes a µC charge pump control circuit 2414A configured to cooperatively operate with a switching network 2651 to generate the third output voltage $V_{THIRD-OUTPUT}$ 2644VO at the third output 2644. As depicted in Figure 53B, the third output voltage $V_{THIRD-OUTPUT}$ 2644VO at the third output 2644 may be implemented by the µC charge pump control circuit 2414A further including of an eighteenth switch control configured to generate an eighteenth switch control signal 2652 to control an eighteenth switch 2653 of the switching network 2651. The eighteenth switch 2653 may be coupled between the first terminal 2424A of

the first flying capacitor 2424 and the third output 2644. In addition, the μC charge pump control circuit 2414A may further include a nineteenth switch control configured to generate an nineteenth switch control signal 2654 to control a nineteenth switch 2655 of the switching network 2651. The nineteenth switch 2655 may be coupled between the second terminal 2424B of the first flying capacitor 2424 and the third output 2644. In addition, the μC charge pump control circuit 2414A may further include a twentieth switch control configured to generate a twentieth switch control signal 2656 to control a twentieth switch 2658. The twentieth switch 2658 may be coupled between the first terminal 2426A of the second flying capacitor 2426 and the third output 2644. In addition, the μC charge pump control circuit 2414A may further include a twenty first switch control configured to generate a twenty first switch control signal 2658 to control a twenty first switch 2660. The twenty first switch 2660 may be coupled between the second terminal 2426B of the second flying capacitor 2426 and the third output 2644. Also, the μC charge pump control circuit 2414A may further include a twenty second switch control configured to generate a twenty second switch control signal 2662 to control a twenty second switch 2664. The twenty second switch 2664 may be coupled between the battery voltage, V_{BAT}, and third output 2644 to provide a bypass mode. In the bypass mode, the third output provides a third output voltage $V_{THIRD-OUTPUT}$ 2644VO substantially equal to the battery voltage,V_{BAT}.

[001659] The μC charge pump 2650 may be configured to generate various combinations of buck output voltages and boost put voltage as a function of the combinations of the first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC and the second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC with the battery voltage, V_{BAT}. In addition, the μC charge pump 2650 may be futher configured to generate various buck output voltage as a function of the combinations of the first flying capacitor voltage $V_{FIRST-FLYCAP}$ 2424FC and the second flying capacitor voltage $V_{SECOND-FLYCAP}$ 2426FC with the ground voltage.

[001660] For example, the third output 2424 may be coupled to the first terminal 2424A of the first flying capacitor 2424 by closing the eighteenth

switch 2653. The third output 2424 may be coupled to the second terminal 2424B of the first flying capacitor 2424 by closing the twenty first switch 2660. The third output 2424 may be coupled to the first terminal 2426B of the second flying capacitor 2426 by closing the nineteenth switch 2655. The third output 2424 may be coupled to the second terminal 2426B of the second flying capacitor 2426 by closing the twentieth switch 2658. The third output 2644 maybe couple to the battery voltage, V_{BAT}, by closing the twenty second switch 2664 in orde to provide a bypass mode. In addition, the third output 2644 may be coupled to ground by selectively closing the twenty first switch 2660 and the third switch 2440.

[001661] Thus, the µC charge pump 2650 may operate in a simiar fastion as the µC charge pump 2510 except an extra phase of operation may be added to provide a charge to the third output capacitor 2646 coupled between the third output 2424 and ground. Accordingly, the the third output voltage $V_{THIRD-OUTPUT}$ 2644VO may be configure to have the following output voltages by charging the third output capacitor 2646 during an extra phase of operation substantially similar to the operation of the a simiar fastion as the µC charge pump 2510:

- $V_{THIRD-OUTPUT}$ = 0 volts;
- $V_{THIRD-OUTPUT} = V_{BAT}$;
- $V_{THIRD-OUTPUT} = V_{BAT} \pm V_{First\ FLY_CAP}$;
- $V_{THIRD-OUTPUT} = V_{BAT} \pm V_{SECOND-\ FLY_CAP}$;
- $V_{THIRD-OUTPUT} = V_{BAT} \pm V_{First\ FLY_CAP} \pm V_{SECOND}$;
- $V_{THIRD-OUTPUT} = \pm V_{First\ FLY_CAP} \pm V_{SECOND}$, where $V_{THIRD-OUTPUT} > 0$ or $V_{THIRD-OUTPUT} < 0$;
- $V_{THIRD-OUTPUT} = \pm V_{First\ FLY_CAP}$
- $V_{THIRD-OUTPUT} = \pm V_{SECOND}$, where $V_{THIRD-OUTPUT} > 0$ or $V_{THIRD-OUTPUT} < 0$

[001662] Figure 55 depicts a portion of a communication device including various embodiments of an envelope tracking modulated power supply system 2500 with transceiver power control loop compensation. For the purposes of illustration and not by way of limitation, the envelope tracking modulated power

supply system 2500 with transceiver power control loop compensation may be described with continuing reference to a number of the embodiments the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A, depicted in Figures 40A-E, and Figures 46A-B and Figure 46E-H, the embodiments of the parallel amplifier 2200 depicted in Figure 46C, the embodiments of the parallel amplifier 2300, depicted in Figure 52A-D as the parallel amplifier 2300A, the parallel amplifier 2300B, the parallel amplifier 2300C, the parallel amplifier 35A, the rechargeable parallel amplifier 35B, the rechargeable parallel amplifier 35C, the parallel amplifier 35D, the rechargeable parallel amplifier 35E, the rechargeable parallel amplifier 35F, the parallel amplifier 35G, the rechargeable parallel amplifier 35H, and rechargeable parallel amplifier 35I, depicted in Figures 12A-H, respectively,

[001663] The envelope tracking modulated power supply system 2500 with transceiver power control loop compensation may include a transceiver power control loop 2502 and an envelope tracking control system 2503. The transceiver power control loop 2502 may include a transmit-target power setting parameter 2502A and a transmit-gain setting parameter 2502B. The transceiver power control loop 2502 may adjust a drive level or an input power P_{IN} of a modulated radio frequency input signal 2504 provided to the radio frequency power amplifier 2540 based on the values of the transmit-target power setting parameter 2502A and a transmit-gain setting parameter 2502B as a function of the output power P_{OUT} generated by the radio frequency power amplifier 2540.

[001664] In some embodiments, the modulated radio frequency input signal 2504, P_{IN}, may be a test signal. As an example, the modulated radio frequency input signal 2504, P_{IN}, may be a carrier wave having a desired frequency.

[001665] In some embodiments of the communication device, the transmit-target power setting parameter 2502A may be based on network control information provided by a communication network in which the communication device is configured to operate. For example, the communication network may provide the communication device with network control information to configure the operation of the communication device within the communication network. In some

embodiments, a transmit-target power setting parameter 2502A used by a communication device may be a function of the different wireless transmissions generated by the communication device. The transmit-target power setting parameter 2502A of the communication device may also be based on a data rate of the transmission, the resource blocks to be used during the transmission, a frequency band allocated for the transmission, the relative location of the transmission band to other bands of operation in the communication network, and/or a combination thereof. As another example, the transmit-target power setting parameter 2502A may be a function of the distance between the communication device and a nearest base station of the communication network. For example, the communication device may use an initial value of the transmit-target power setting parameter 2502A based on a target base station to receive an initial transmission. Thereafter, the communication network may configure the communication device to use a new value of a transmit-target power setting parameter 2502A based on a serving base station.

[001666] In some embodiments, the transceiver power control loop 2502 may adjust the transmit-gain setting parameter 2502B in response to changes in bias settings of the transceiver circuitry 2512, a temperature change of the digital baseband circuit 2510, and/or changes in the voltage standing wave ratio, VSWR, for a particular transmit frequency.

[001667] As an example, the transceiver power control loop 2502 may be configured to adjust a transmit-gain setting parameter 2502B to provide a modulated radio frequency input signal 2504 to a radio frequency power amplifier 2540. In some embodiments, the transmit-gain setting may be adjusted as a function of the output power P_{OUT} of the amplified radio frequency output signal 2548 provided to the antenna 2544 and a transmit-target power setting parameter 2502A.

[001668] For example, in some embodiments, the transceiver power control loop 2502 may increase the transmit-gain setting parameter 2502B used to set the input power P_{IN} of the modulated radio frequency input signal 2504 provided to the radio frequency power amplifier 2540 in response to a decrease in the output

power P_{OUT} of an amplified radio frequency output signal 2548 provided to the antenna 2544. In response to the increase of the transmit-gain setting parameter 2502B, the transceiver circuitry 2512 may increase the drive level of the modulated radio frequency input signal 2504 provided to the radio frequency power amplifier 2540. In other words, the transceiver circuitry 2512 may increase the input power P_{IN} of the modulated radio frequency input signal 2504 to increase the output power P_{OUT} of the amplified radio frequency output signal 2548. To avoid gain compression due to the increase drive level of the modulated radio frequency input signal 2504, the envelope tracking control system 2503 may be configured to increase the amplitude of the modulated power supply voltage, V_{CC}, provided to the collector of the radio frequency power amplifier 2540. Otherwise, the modulated power supply voltage, V_{CC}, may be insufficient to support the increased output power P_{OUT} to be generated by the radio frequency power amplifier 2540. Gain compression may result in degradation of the spectrum performance and the error vector magnitude (EVM) performance of the transmitted signal as measured at the output of the radio frequency power amplifier 2540.

[001669] For example, Figure 54 depicts a set of iso-gain contours of the radio frequency power amplifier 2540 that may be stored in a V_{CC} look up table 2586, and used to generate the modulated power supply voltage, V_{CC}, provided to the collector of the radio frequency power amplifier 2540. For example, the sets iso-gain contours may depict an iso-gain curve for the power gains 28dBm, 27dBm, 26dBm, and 25dBm. In addition, Figure 54 depicts an original input power P_{IN} or drive level of a modulated radio frequency input signal provided as an input to the radio frequency power amplifier 2540 to transmit a data signal. Figure 54 further depicts an original range of the modulated power supply voltage, V_{CC}, generated by the envelope tracking power converter system 2530 as a function of the digital I/Q signal 2506 provided to a digital baseband circuit 2510 for transmission. The modulated radio frequency input signal may also be generated based on the digital I/Q signal 2506. The Figure 54 further depicts a new range of the modulated power supply voltage, V_{CC}, that should be generated by the envelope

tracking power converter system 2530 in response to the input power P_{IN} of the a modulated radio frequency input signal being increased by 1dBm while maintaining the same modulation range. As shown in Figure 54, if the envelope tracking power converter system 2530 is not configured to generate a modulated power supply voltage, V_{CC}, greater than 3.75 volts, the modulated radio frequency input signal may cause the radio frequency power amplifier 2540 to change from the iso-gain contour for 27dBm of power gain to the iso- gain contour for 26dBm for an input power P_{IN} or drive level above 6dBm. As a result, the radio frequency power amplifier 2540 may operate in a non-linear mode an jump from one iso-gain contour to another during the data transmission. This may result in gain compression. To avoid this problem, the envelope tracking control system 2503 may determine whether the transceiver power control loop 2502 has increased the drive level of the modulated radio frequency input signal such that the envelope tracking power converter system 2530 may not be able to provide a sufficient range for the modulated power supply voltage, V_{CC}, to support the increase in drive level. In that case, the envelope tracking control system 2503 may configure the digital baseband circuit 2510 to generate a control signal 2508 that will support the new range of the modulated power supply voltage, V_{CC}, necessary to prevent gain compression.

[001670] As an example, to avoid gain compression, the transceiver power control loop 2502 may be further configured to cooperative operate with the envelope tracking control system 2503. The envelope tracking control system 2503 may provide a control signal 2508 to an envelope tracking power converter system 2530 as a function of the digital I/Q signal 2506 provided to a digital baseband circuit 2510 for transmission. The digital I/Q signal 2506 may include a digital in-phase component $I_{DIGITAL}$ 2506A and a digital quadrature component $Q_{DIGITAL}$ 2506B. In addition, the envelope tracking control system 2503 may be configured to adjust the control signal 2508 as a function of the transmit-gain setting parameter 2502B, the transmit-target power setting parameter 2502A, a temperature measurement of the digital baseband circuit 2510, and/or some combination thereof. In still other embodiments, the envelope tracking control

system 2503 may be further configured to adjust the control signal 2508 as a function of the transmit frequency of the transmitter channel for the band of operation in which the communication device is configured to operate. As an example, in some embodiments, the envelope tracking control system 2503 may adjust the generation of a modulated power supply voltage, $V_{CC,}$ as a function of a transmit-target power setting parameter 2502A and a transmit-gain setting parameter 2502B, and a transmit frequency of the transmitter channel.

[001671] The Figures 55 may further depict embodiments of a system, circuitry, and methods for providing a transceiver power control loop 2502 configured to regulate the output power P_{OUT} of an amplified radio frequency output signal 2548 provided to the antenna 2544 in response to the modulated radio frequency input signal 2504.

[001672] Figure 55 depicts the envelope tracking modulated power supply system 2500 with transceiver power control loop compensation including a digital baseband circuit 2510, an envelope tracking power converter system 2530, a radio frequency power amplifier 2540, a radio frequency switch 2542 in combination with an antenna 2544 and power coupler 2546. The digital baseband circuit 2510, the envelope tracking power converter system 2530, the radio frequency power amplifier 2540, and radio frequency switch 2542 may be in communication with a controller 50 via a control bus 44. The controller 50 may control and/or provide parameters to govern the function of the digital baseband circuit 2510, the envelope tracking power converter system 2530, the radio frequency power amplifier 2540, and the radio frequency switch 2542 by selectively setting parameters and settings in the various devices. In addition, as will be discussed, the controller 50 may also provide a transmit-target power setting parameter 2502A to the digital baseband circuit 2510 as a function output power level control information received by the communication device from a base station of communication network in which the communication device is configured to operate. The transmit-target power setting parameter 2502A may configure the digital baseband circuit 2510 to provide a modulated radio frequency input signal 2504 having an input power P_{IN} to the radio frequency

power amplifier 2540. The digital baseband circuit 2510 may be configured to receive the digital I/Q signal 2506 to be transmitted by the radio frequency power amplifier 2540 during a data transmission The digital I/Q signal 2506 may include a digital in-phase component $I_{DIGITAL}$ 2506A and a digital quadrature component $Q_{DIGITAL}$ 2506B. The digital baseband circuit 2510 may include transceiver circuitry 2512 and the configuration-feedback circuitry 2520. The transceiver circuitry 2512 may include a front-end control interface circuit 2514 configured to communicate via a front-end control interface 2514A to the envelope tracking power converter system 2530. In addition, the digital baseband circuit 2510 may also configure various operational parameters of the envelope tracking power converter system 2530 via the front-end control interface 2514A. As an example, in some embodiments, the digital baseband circuit 2510 may provide various operational parameters via the front-end control interface 2514A to the envelope tracking power converter system 2530 as a function of a regulated time period.

[001673] In addition, the transceiver circuitry 2512 may provide a control signal 2508 to the envelope tracking power converter 2430. In some embodiments, control signal 2508 may be a differential control signal having a non-inverted control signal component 2508A and an inverted control signal component 2508B. For example, the control signal 2508 may be a differential V_{RAMP} signal having a non-inverted V_{RAMP} signal component and an inverted V_{RAMP} signal component. The control signal 2508 may provide a target voltage for the modulated power supply voltage, V_{CC}, at the modulated power supply output 876. Based on the control signal 2508, the envelope tracking power converter system 2530 may generate a modulated power supply voltage, V_{CC}, at the modulated power supply output 876.

[001674] The transceiver circuitry 2512 may further include a temperature sensor 2516 configured to provide a temperature measurement of the digital baseband circuit 2510. In some embodiments, the envelope tracking control system 2503 may use the temperature measurement of the digital baseband circuit 2510 to adjust the

[001675] The transceiver circuitry 2512 may also include a feedback analog-to-digital converter 2518 configured to receive a measurement signal 2532 from the envelope tracking power converter system 2530. The measurement signal 2532 in combination with the feedback analog-to-digital converter 2518 may provide information such as the temperature and supply voltage of the envelope tracking power converter system 2530.

[001676] The feedback analog-to-digital converter 2518 may receive the measurement signal 2532 from the envelope tracking power converter system 2530. The feedback analog-to-digital converter 2518 may convert the measurement signal 2532 into digital data, which may be provided to the controller 50 or other portions of the digital baseband circuit 2510. For example, in some embodiments, the envelope tracker power converter 16 may provide various types of measurements, including an analog temperature signal, an analog power supply voltage signal, and a measurement of the battery voltage, V_{BAT}.

[001677] For example, via the front-end control interface 2514A, the digital baseband circuit 2510 may request the envelope tracking power converter system 2530 to provide a measurement of the battery voltage, V_{BAT}, from a battery 20. In response, the envelope tracking power converter system 2530 may provide a measurement of the battery voltage, $V_{BAT,}$ to the feedback analog-to-digital converter 2518 via the measurement signal 2532. In a similar fashion, the digital baseband circuit 2510 may obtain a measurement of the temperature of the envelope tracking power converter system 2530 via the measurement signal 2532.

[001678] Based on the digital in-phase component $I_{DIGITAL}$ 2506A and the digital quadrature component $Q_{DIGITAL}$ 2506B, the transceiver circuitry 2512 may generate a control signal 2508 to provide a target voltage for generation of a modulated power supply voltage, V_{CC}. As previously described, in some embodiments that control signal 2508 may be a differential V_{RAMP} signal. The envelope tracking control system 2503 may configured to the digital baseband circuit 2510 to generate the control signal 2508 as a function of the modulated

radio frequency input signal 2504 provided to the radio frequency power amplifier 2540 for transmission. The envelope tracking power converter system 2530 may generate the modulated power supply voltage, V_{CC}, at the modulated power supply output 876 in response to the control signal 2508. The envelope tracking power converter system 2530 may provide the modulated power supply voltage, V_{CC}, to the radio frequency power amplifier 2540.

[001679] The radio frequency power amplifier 2540 may generate an amplified radio frequency output signal 2548 as a function of the input power P_{IN} of the modulated radio frequency input signal 2504 and the modulated power supply voltage V_{CC}. The radio frequency power amplifier 2540 may provide the amplified radio frequency output signal 2548 to the antenna 2544 via a radio frequency switch 2542.

[001680] In response to the amplified radio frequency output signal 2548, the power coupler 2546 may obtain a measurement of the amplified radio frequency output signal 2548. In some embodiments, the power coupler 2546 may also obtain a measurement of the output power of the amplified radio frequency output signal 2548, present at the antenna 2544. In other embodiments of the transceiver power control loop 2502, the power coupler 2546 may be located at the output of the radio frequency power amplifier 2540 and configured to obtain a measurement of the amplified radio frequency output signal 2548 before passing through the radio frequency switch 2542. Some embodiments of the power coupler 2546 may include a power detector configured to measure the output power P_{OUT} of the amplified radio frequency output signal 2548 at the output of the radio frequency power amplifier 2540. The power coupler 2546 may provide a measured amplified radio frequency output signal 2550 to the digital baseband circuit 2510. For example, the power coupler 2546 may provide a measured amplified radio frequency output signal 2550 to the configuration-feedback circuitry 2520 of the digital baseband circuit 2510.

[001681] The I/Q feedback system 2522 may receive the measured amplified radio frequency output signal 2550. The I/Q feedback system 2522 may demodulate the measured amplified radio frequency output signal 2550 to obtain

digitized in-phase feedback component $I_{MEASURED}$ 2570 and a measured quadrature component $Q_{MEASURED}$ 2572 as a function of the measured amplified radio frequency output signal 2550.

[001682] The digitized in-phase feedback component $I_{MEASURED}$ 2570 and measured quadrature phase signal, $Q_{MEASURED}$, may be provided to the fast calibration iso-gain and delay alignment circuitry 2524 and the transceiver power control loop circuitry 2526. The transceiver power control loop circuitry 2526 also receives the transmit-target power setting parameter 2502A. Based on digitized in-phase feedback component $I_{MEASURED}$ 2570 and a measured quadrature component $Q_{MEASURED}$ 2572, the transceiver power control loop circuitry 2526 may determine whether to increase or decrease the power level of the modulated radio frequency input signal 2504 as a function of the transmit-target power setting parameter 2502A.

[001683] For example, the transceiver power control loop circuitry 2526 may determine that the output power P_{OUT} of the measured amplified radio frequency output signal 2550 is less than the transmit-target power setting parameter 2502A. In response to the determination that the output power P_{OUT} of the measured amplified radio frequency output signal 2550 is less than the transmit-target power setting parameter 2502A, the the transceiver power control loop circuitry 2526 may configure the transceiver circuitry 2512 to increase the input power P_{IN} of the modulated radio frequency input signal 2504 provided to the radio frequency power amplifier 2540. For example, in some embodiments, the transceiver power control loop circuitry 2526 may increase the magnitude of the transmit-gain setting parameter 2502B. The transceiver power control loop circuitry 2526 may generate a transmit-gain setting signal 2526A based on the transmit-gain setting parameter 2502B. In some embodiments, the transceiver power control loop circuitry 2526 may provide the transmit-gain setting signal 2526A to a baseband controller 2511. The baseband controller 2511 may be configured to adjust various parameters and settings of the transceiver circuitry 2512 to increase the drive level or input power P_{IN} of the modulated radio frequency input signal 2504 to compensate for the difference between the

transmit-target power setting parameter 2502A and the output power P_{OUT} of the measured amplified radio frequency output signal 2550.

[001684] In addition, the transceiver power control loop circuitry 2526 may provide the transmit-gain setting signal 2526A and the transmit-target power setting signal 2526B to a pseudo-envelope follower gain controller 2574, which for the sake of convenience may be abbreviated as the PEF gain controller. Alternatively, in some embodiments, the baseband controller 2511 may provide the transmit-gain setting parameter and the transmit-target output power parameter to the pseudo-envelope follower gain controller 2574. For example, in some alternative embodiments, the baseband controller 2511 may configure the pseudo-envelope follower gain controller 2574 to generate gain control signal 2574A having a gain control magnitude substantially equal to $G_{CONTROL}$.

[001685] On the other hand, the transceiver power control loop circuitry 2526 may determine that the output power P_{OUT} of the measured amplified radio frequency output signal 2550 exceeds the transmit-target power setting parameter 2502A. Based on a determination that the output power P_{OUT} of the measured amplified radio frequency output signal 2550 exceeds the transmit-target power setting parameter 2502A, the transceiver power control loop circuitry 2526 may decrease the magnitude of the transmit-gain setting parameter 2502B.

[001686] The transceiver power control loop circuitry 2526 may generate a transmit-gain setting signal 2526A based on the reduced magnitude of the transmit-gain setting parameter 2502B. In some embodiments, the baseband controller 2511 may be configured to adjust various parameters and settings of the transceiver circuitry 2512 to reduce the drive level or input power P_{IN} of the modulated radio frequency input signal 2504 to decrease the output power P_{OUT} of the measured amplified radio frequency output signal 2550. In addition, the transceiver power control loop circuitry 2526 may provide the transmit-gain setting signal 2526A to the pseudo-envelope follower gain controller 2574.

[001687] In some embodiments the power coupler 2546 may include a detector. The detector may include a sensor in communication with an output of the radio

frequency power amplifier 2540. The detector may measure an output power generated by the radio frequency power amplifier 2540. As an example, after accounting for losses in the radio frequency switch 2542, the power coupler 2546 may provide a measured output power, P_{OUT}, of the amplified radio frequency output signal 2548. The measured output power may provide an average power measurement. The power coupler 2546 may also provide an average power measurement based on various averaging techniques. In some embodiments, the power coupler 2546 may be configured to provide a peak power measurement. In some embodiments, the power coupler 2546 may be configured as a linear power detector. In other embodiments, the power coupler 2546 may be a logarithmic power detector. In still other embodiments, the power coupler 2546 may be a non-linear power detector.

[001688] The radio frequency switch 2542 includes a closed state of operation and open state of operation. In the closed state of operation, the radio frequency switch 2542 may couple the radio frequency power amplifier 2540 to the antenna 2544, which permits the amplified radio frequency output signal 2548 to pass through the radio frequency switch 2542 to the antenna 2544 to transmit the amplified radio frequency output signal 2548. In the open state of operation, the radio frequency switch 2542 substantially attenuates the amplified radio frequency output signal 2548 to minimize or prevent a transmission of the amplified radio frequency output signal 2548. Ideally, in the open state of operation, the radio frequency switch 2542 has infinite impedance. In some embodiments, the radio frequency switch 2542 may provide antenna switch isolation around +25 dBm.

[001689] In some embodiments, the communication device may include a controller 50 configured to coordinate the functions of the various components and operations of the embodiments of the envelope tracking modulated power supply system 2500 with transceiver power control loop compensation. In some embodiments, the controller 50 may include a number of distributed processors, ditributed microcontrollers, controllers, local control units, memory mapped local memory for various components, functions, and features of the various

embodiments of a power management system 870, the various embodiments of a switch mode power supply converter 872, the various embodiments of a parallel amplifier circuit 874, firmware circuitry, reconfigurable digital logic circutiry, state machines, analog logic circuitry, a number of communication interfaces and busses, various forms of memory, data registers, control registers, cache memory, distributed memory, memory mappings, register mappings, various types of sensors and inputs for receiving sensory data or information, one or more digital-to-analog converters, one or more analog-to-digital converters, various types and numbers of output drivers, various types and numbers of digital input buffers and analog input buffers, various processor cores and arithmetic operation units, sub-processors, read only memory, random access memory, flash memory circuitry, electronically fuseable memory, interrupt handlers, interrupt handling management systems, and controls signals. For the sake of simplicity of description, and not by way of limitation, the controller 50 may be described as performing various functions and features to govern the operation of the communication device, the various embodiments of the envelope tracking modulated power supply system 2500 with transceiver power control loop compensation, the digital baseband circuit 2510, the envelope tracking power converter system 2530, the radio frequency power amplifier 2540, the radio frequency switch 2542, the power coupler 2546. As an example, and not by way of limitation, the controller 50 may include a control bus 44 in communication with the digital baseband circuit 2510, the envelope tracking power converter system 2530, the radio frequency power amplifier 2540, the radio frequency switch 2542, and the power coupler 2546. For the sake of simplicity, and not by way of limitation, the control bus 44 is only depicted as being in communication with each component depicted in Figure 1. Even so, one of ordinary skill in the art will understand that this is by way of example and not by way of limitation.

[001690] For example, the controller 50 may be in communication with various other elements to be described in the digital baseband circuit 2510, the embodiments of the switch mode power supply converter 872, and the

embodiments of the parallel amplifier circuit 874 of the envelope tracking power converter system 2530. As an example, the controller 50 may be in communication with and cooperatively operate with the various embodiments of the power management system 870.

[001691] The controller 50 may include a processor, a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A processor may be a microprocessor. In the alternative, the processor may be any conventional processor, controller, microcontroller, a state machine and/or a combination thereof. A processor may also be implemented as a combination of computing devices. As an example, a combination of computing devices may include a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. The processor 28 may further include or be embodied in hardware and in computer executable instructions that are stored in memory, and may reside, for example, in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, hard disk, a removable disk, a CD-ROM, or any other form of computer readable medium known in the art. An exemplary storage medium may be coupled to the processor such that a processor can read information from, and write information to, the storage medium. In the alternative, the storage medium or a portion of the storage medium may be integral to the processor. The processor and the storage medium may reside in an Application Specific Integrated Circuit (ASIC).

[001692] The front-end control interface circuit 2514 is in communication with the envelope tracking power converter system 2530 via a front-end control interface 2536. In some embodiments, the front-end control interface circuit 2514 may operate with a Mobile Industry Processor Interface® standard based device via the front-end control interface 2536. As an example, the front-end

control interface circuit 2514 and the front-end control interface 2536 may be configured to control devices based on a Radio Frequency Front-End control interface specification.

[001693] In some embodiments, the controller 50 may cooperatively interoperate the front-end control interface circuit 2514 to configure and control the envelope tracking power converter system 2530. In still other embodiments, the controller 50 may be a supervisory processor that governs other controller s. The baseband controller 2511 may include configurable firmware, a processor, sub-controllers, control logic, control circuitry, one or more state machines, a Digital Signal Processor (DSP), an ASIC, a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. The baseband controller 2511 may include firmware, executable program code, read only memory, fusible memory, a memory processor, a microprocessor, conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices. As an example, a combination of computing devices may include a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. The controller 32 may further include or be embodied in hardware and in computer executable instructions that are stored in memory, and may reside, for example, in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, hard disk, a removable disk, a CD-ROM, or any other form of computer readable medium known in the art. An exemplary storage medium may be coupled to the processor such that a processor can read information from, and write information to, the storage medium. In the alternative, the storage medium or a portion of the storage medium may be integral to the processor. The processor and the storage medium may reside in an Application Specific Integrated Circuit (ASIC).

[001694] The digital baseband circuit 2510 may receive a digital I/Q signal 2506 to be transmitted by the radio frequency power amplifier 2540. For example, the digital I/Q signal 2506 include a digital data signal. Alternatively, the digital I/Q signal 2506 may be a test signal for calibrating various parts of the envelope tracking modulated power supply system 2500 with transceiver power control loop compensation. In some embodiments, the digital I/Q signal 2506 may include a digital in-phase component $I_{DIGITAL}$ 2506A and a digital quadrature component $Q_{DIGITAL}$ 2506B. The digital in-phase component $I_{DIGITAL}$ 2506A and the digital quadrature component $Q_{DIGITAL}$ 2506B where the digital in-phase component $I_{DIGITAL}$ 2506A and the digital quadrature component $Q_{DIGITAL}$ 2506B represent the in-phase and quadrature components of a signal to be transmitted. The digital I/Q signal 2506 may receive various types of test signals to generate a modulated radio frequency input signal 2504 having a desired envelope characteristic. In addition, the digital I/Q signal 2506 may inlcude a test signal that generates the modulated radio frequency input signal 2504 having a desired frequency characteristic or periodicity. For example, dependent upon a band of operation of a communication network to which a communication device is assigned or a wideband modulation technique associated with the band of operation, the test signal received by the digital I/Q signal 2506 may include various frequency characteristics. As an example, for the case where a wideband modulation technique includes a particular modulation bandwidth, the digital I/Q signal 2506 may generate a modulated radio frequency input signal 2504 that has a bandwidth substantially similar to bandwidth associated with the wideband modulation technique or the band of operation assigned to the communication device.

[001695] The digital baseband circuit 2510 may further include a pseudo-envelope follower gain controller 2574 configured to provide a gain control signal 2574A having a gain control magnitude substantially equal to $G_{CONTROL}$. The pseudo-envelope follower gain controller 2574 may adjust the magnitude of the gain control signal 2574A based as a function of a measured temperature of the transceiver circuitry 2512, the transmit-gain setting signal 2526A, a carrier

frequency for the band of operation in which the communication device is configured to operate, and/or a combination there of to generate the V_{CC} look up table index signal 2584 at the input of the V_{CC} look up table 2586. The pseudo-envelope follower gain controller 2574 may adjust the gain control magnitude, $G_{CONTROL}$, such that the V_{CC} look up table index signal 2584 provides an index signal into the V_{CC} look up table 2586 that substantially emulates the drive level or input power P_{IN} of the modulated radio frequency input signal 2504 provided to the radio frequency power amplifier 2540. In other words, the pseudo-envelope follower gain controller 2574 may adjust the magnitude of the gain control magnitude, $G_{CONTROL}$, such that the V_{CC} look up table compensated envelope signal 2588 may provide a target voltage for the modulated power supply voltage, V_{CC}, as a function of the iso-gain curve that corresponds to the transmit-target power setting parameter 2502A. As a result, the gain control signal 2574A may compensate for an increase in the input power of the modulated radio frequency input signal provided to the radio frequency power amplifier 2540 to prevent or minimize gain compression.

[001696] The envelope tracking power converter system 2530 may include various circuits to generate a modulated power amplifier supply voltage, VCC, at the modulated power supply output 876 . As a non-limiting example, some embodiments of the envelope tracking power converter system 2530 may include a switch mode power supply converter 872 and the parallel amplifier circuit 874. In some embodiments, the switch mode power supply converter 872 may be a buck converter. In other embodiments, the switch mode power supply converter 872 may include a multi-level charge pump buck converter configured to buck and/or boost a supply voltage to provide a switching voltage at different voltages dependent upon the control signal 2508. As a non-limiting example, in some embodiments, the envelope tracking power converter system 2530 may operate in various power level modulation modes depending on the expected ouput power to be generated by the radio frequency power amplifier 2540 in a data transmission.

[001697] As depicted in Figure 56, the transceiver circuitry 2512 may include an AM/PM compensation circuit 2573, a digital gain control circuit 2576, an envelope magnitude calculation circuit 2578, and an envelope tracking digital/analog section 2580. The envelope magnitude calculation circuit 2578 may receive the digital in-phase component $I_{DIGITAL}$ 2506A and the digital quadrature component $Q_{DIGITAL}$ 2506B. The envelope magnitude calculation circuit 2578 may calculate an envelope magnitude, $\zeta_{MAGNITUDE}$, of an expected envelope of the modulated radio frequency input signal 2504, P_{IN}. As an example, the envelope magnitude calculation circuit 2578 may generate the envelope magnitude, $\zeta_{MAGNITUDE}$, based on the digital in-phase component $I_{DIGITAL}$ 2506A and the digital quadrature component $Q_{DIGITAL}$ 2506B. In some embodiments, the envelope magnitude, $\zeta_{MAGNITUDE}$, may be proportional to the magnitude of the envelope of the modulated radio frequency input signal 2504, P_{IN}. As a non-limiting example, the envelope magnitude, $\zeta_{MAGNITUDE}$, may be described by equation (25) as follows:

$$(25)\ \zeta_{\mathrm{MAGNITUDE}} = \sqrt{I_{DIGITAL}{}^2 + Q_{DIGITAL}{}^2}$$

The envelope magnitude calculation circuit 2578 provides the envelope magnitude, $\zeta_{MAGNITUDE}$, to the envelope tracking digital/analog section 2580.

[001698] The AM/PM compensation circuit 2573 may be configured to receive the digital in-phase component $I_{DIGITAL}$ 2506A and the digital quadrature component $Q_{DIGITAL}$ 2506B. In some embodiments, the AM/PM compensation circuit 2573 may be configured to provide amplitude modulation and phase modulation compensation for the radio frequency power amplifier. For example, some embodiments of the AM/PM compensation circuit 2573 may adjust the digital in-phase component $I_{DIGITAL}$ 2506A and the digital quadrature component $Q_{DIGITAL}$ 2506B to compensate for any phase shift due to the modulated power supply voltage, V_{CC}, the input power, P_{IN}, of the modulated radio frequency input signal 2504 to be transmitted by the radio frequency power amplifier 2540, and/or a combination thereof.

[001699] For example, some embodiments of the AM/PM compensation circuit 2573 may receive the V_{CC} look up table index signal 2584 and the V_{CC} look up table compensated envelope signal 2588. The V_{CC} look up table index signal 2584 may be substantially equivalent to a digital representation of the envelope of the modulated radio frequency input signal 2504 provided to the radio frequency power amplifier for transmission. The the V_{CC} look up table compensated envelope signal 2588 may be substantially equivalent to a digital representation of a target envelope for the envelope tracking power converter system 2530 to track or follow to generate a modulated power supply voltage, V_{CC}, that substantially corresponds to the modulated radio frequency input signal 2504. In other words, the V_{CC} look up table 2586 may translate the V_{CC} look up table index signal 2584 into a desired target voltage for the modulated power supply voltage, V_{CC}.

[001700] As will be described, pseudo-envelope follower gain controller 2574 may generate the gain control, $G_{CONTROL}$, signal as a function of a temperate of the digital baseband circuit 2510, the transmit-target power setting signal 2526B, a transmit-gain setting signal 2526A, and/or a combination thereof to adjust the magnitude of the envelope magnitude, $\zeta_{MAGNITUDE}$, signal. As a result, the V_{CC} look up table index signal 2584 may include a transceiver gain adjusted envelope magnitude $\zeta_{TGA\text{-}MAGNITUDE}$, substantially equal to the product of the envelope magnitude, $\zeta_{MAGNITUDE}$, signal and the gain control, $G_{CONTROL}$, signal. The gain control, $G_{CONTROL}$, adjusts the envelope magnitude, $\zeta_{MAGNITUDE}$, signal to reflect a change in the transceiver gain such that the V_{CC} look up table index signal is not solely based on the expected output power to be generated by the radio frequency power amplifier 2540 in response to the modulated radio frequency input signal 2504. Transceiver gain adjusted envelope magnitude, $\zeta_{TGA\text{-}MAGNITUDE}$, is provided by the equation (26) as follows:

$$\zeta_{TGA-MAGNITUDE} = \zeta_{MAGNITUDE} \times G_{CONTROL}, \quad (26)$$

where the gain control, $G_{CONTROL}$, may be a function of the transceiver temperature, $T_{TRANCEIVER}$, and the transceiver gain settings, $G_{TRANSCEIVER}$. In some embodiments, the gain control, $G_{CONTROL}$, may also be a function of the transceiver transmit frequency, $F_{TRANSMIT}$.

[001701] Accordingly, the V_{CC} look up table index signal 2584 substantially compensates for a change in the gain of the digital transceiver to reflect the input drive level to the radio frequency power amplifier. Thus, the V_{CC} look up table index signal 2584 provides an emulated "Pin drive level of the power amplifier" rather using as index the output power of the radio frequency power amplifier 2540 to generate the control signal 2508.

[001702] Because the gain control, $G_{CONTROL}$, provided by the pseudo-envelope follower gain controller 2574 compensates for changes in the transmit gain setting used to set the power level of the modulated radio frequency input signal 2504, the V_{CC} look up table index signal 2584 may index into the V_{CC} look up table 2586 to generate a V_{CC} look up table compensated envelope signal 2588 that is adjusted for a change in the transmit-gain setting signal 2526A used to set the power level of the modulated radio frequency input signal 2504 provided to the radio frequency power amplifier 2540.

[001703] The AM/PM compensation circuit 2573 may compensate for any phase shift due to the drive level change in of the modulated radio frequency input signal 2504 provided to the radio frequency power amplifier 2540.

[001704] In some embodiments, the AM/PM compensation circuit 2573 may either the V_{CC} look up table index signal 2584 or the V_{CC} look up table compensated envelope signal 2588 as a scaled version of the digital envelope of the modulated radio frequency input signal 2504. In other words, the AM/PM compensation circuit 2573 may use either the V_{CC} look up table index signal 258, the V_{CC} look up table compensated envelope signal 2588, and/or a combination thereof to represent the modulated radio frequency input signal 2504. Based on the representation of the represent the modulated radio frequency input signal 2504, the AM/PM compensation circuit 2573 may calculate a phase correction as a function of the input power P_{IN}. The AM/PM compensation circuit 2573 may

apply the phase correction to generate a phase corrected digital in-phase component $I_{DIGITAL}$ 2573I and a phase corrected digital in-phase component $I_{DIGITAL}$ 2527Q, which are provide to the digital gain control circuit 2576. In response to the phase corrected digital in-phase component $I_{DIGITAL}$ 2573I and the phase corrected digital in-phase component $I_{DIGITAL}$ 2527Q, the digital gain control circuit 2576 may generate a gain adjusted digital in-phase, $I_{DIGITAL_GAIN_ADJUSTED}$, component and the gain adjusted digital quadrature, $Q_{DIGITAL_GAIN_ADJUSTED}$, based on the transmit-gain setting parameter.

[001705] The envelope tracking digital/analog section 2580 may include the pseudo-envelope follower gain controller 2574, a multiplier 2582, the V_{CC} look up table 2586, a fine tuning delay circuit 2590, a digital pre-distortion compensation filter 2592, a differential digital-to-analog converter 2598, and a fixed delay circuit 2600. The multiplier 2582 may include a first input in communication with the output of the pseudo-envelope follower gain controller 2574 and a second input in communication with the envelope magnitude calculation circuit 2578. The first input of the multiplier 2582 may receive the gain control, $G_{CONTROL}$, from the pseudo-envelope follower gain controller 2574. The second input of the multiplier 2582 may receive the envelope magnitude, $\zeta_{MAGNITUDE}$. The multiplier 2582 multiplies the envelope magnitude, $\zeta_{MAGNITUDE}$, by the gain control, $G_{CONTROL}$, to generate the V_{CC} look up table index signal 2584. In some embodiments, the gain control, $G_{CONTROL}$, is adjusted to compensate for variations in a setup of the digital baseband circuit 2510. For example, the value of the gain control, $G_{CONTROL}$, may be adjusted to increase or decrease the modulated power supply voltage, V_{CC}, generated by the envelope tracking power converter system 2530 as a function of the input power P_{IN} or drive level of the modulated radio frequency input signal provided to the radio frequency power amplifier 2540.

[001706] The multiplier 2582 provides a V_{CC} look up table index signal 2584 to the V_{CC} look up table 2586 based on the product of the envelope magnitude, $\zeta_{MAGNITUDE}$, and the gain control, $G_{CONTROL}$.

[001707] The V_{CC} look up table 2586 may include one or more tables to translate the V_{CC} look up table index signal 2584 into a V_{CC} look up table compensated envelope signal 2588. The V_{CC} look up table compensated envelope signal 2588 may provide a target voltage for the modulated power supply voltage, V_{CC}, to be generated by the envelope tracking power converter system 2530 based on the envelope of the modulated radio frequency input signal 2504. For example, depending upon a band of operation, a power level modulation mode of operation of the communication device, a spectrum target, and/or an error vector magnitude target, the baseband controller 2511 or the controller 50 may configure the V_{CC} look up table 2586 to select a particular set of look up values as a function of an operational mode of the communication device, the digital baseband circuit 2510, the envelope tracking power converter system 2530, the envelope tracking digital/analog section 2580, and/or a combination thereof. The V_{CC} look up table 2586 provides a V_{CC} look up table compensated envelope signal 2588 to the fine tuning delay circuit 2590.

[001708] The fine tuning delay circuit 2590 may be configured to delay propagation of the V_{CC} look up table compensated envelope signal 2588 based on a programmable delay parameter. The programmable delay parameter may be controlled by the controller 50 the baseband controller 2511 and/or a combination thereof. Depending upon the programmable delay parameter, the fine tuning delay circuit 2590 may provide a delay propagation of the V_{CC} look up table compensated envelope signal 2588 based on a programmable delay parameter by a fine tuning delay time, T_{FINE_TUNING}. The granularity of the fine tuning delay time, T_{FINE_TUNING}, may depend upon a clock of the digital baseband circuit 2510. As a non-limiting example, various embodiments an open loop envelope tracking system calibration technique and circuitry are described in the U.S. Patent Application Number 13/367,973, entitled, "Group Delay Calibration Method For Power Amplifier Envelope Tracking," filed on February 7, 2012, which is also filed as the international patent application, PCT/US2012/02414. Both the U.S. Patent Application Number 13/367,973 and the international patent application, PCT/US2012/02414 claim priority to U.S. provisional patent

application number 61/440,089, filed February 7, 2011. In addition, as another non-limiting example, various embodiments of a fine tuning delay circuit 2590 may be described in the United States Patent Application Number 13/423,649, filed of March 19, 2012, and entitled, "Apparatuses And Methods For Rate Conversion And Fractional Delay Calculation Using A Coefficient Look Up Table," which is filed as a continuation-in-part application of, and claims the benefit of, U.S. patent application number 13/367,973, filed February 7, 2012, entitled “Group Delay Calibration Method for Power Amplifier Envelope Tracking,” and also claims the benefit of U.S. provisional patent application number 61/454,141, filed March 18, 2011, and U.S. provisional patent application number 61/454,226, filed March 18, 2011.

[001709] In some embodiments, the propagation delay of the fine tuning delay circuit 2590 may be provided by an interpolator. In other embodiments, the propagation delay of the fine tuning delay circuit 2590 may be provided by a tapped delay line or other delay circuit. The fine tuning delay circuit 2590 provdes a digitally delayed control signal without pre-distortion compensation 84 to the digital pre-distortion compensation filter 2594. The digitally delayed control signal without pre-distortion compensation 84 may be provided to the digital pre-distortion compensation filter 2594.

[001710] The digital pre-distortion compensation filter 2594 may be either an infinite impulse response filter (IIR) or a finite impulse response filter (FIR). In some embodiments, the coefficients of the digital pre-distortion compensation filter 2594 may be configured by the controller 50 baseband controller 2511 and/or a combination thereof. In addition, the propagation delay through the digital pre-distortion compensation filter 2594 may vary depending upon the various modes of operation of the communication device.

[001711] For example, the propagation delay through the digital pre-distortion compensation filter 2594 may depend on various factors including a band of operation, a channel bandwidth, a wideband modulation bandwidth, channel conditions, a location of the communication device relative to communication hubs, points, towers, and hot-spots, signal modulation techniques, expected

envelope characteristics, the peak-to-average ratio of the envelope of the signal to be transmitted, the data rate, the bandwidth of the channel, error vector magnitude, desired transmit spectrum characteristics, and/or some combination thereof.

[001712] As an example application, the digital pre-distortion compensation filter 2594 may be configured to equalize the frequency response of the modulated power supply voltage, V_{CC}, relative to the differential V_{RAMP} signal. The digital pre-distortion compensation filter 2592 may provide a digital control signal 2596 to the differential digital-to-analog converter 2598. In some embodiments, the digital control signal 2596 may be a digital V_{RAMP} signal, $V_{RAMP_DIGITAL}$. The differential digital-to-analog converter 2598 may convert the digital control signal 2596 into the control signal 2508. In some embodiments, the control signal 2508 may be a differential control signal. For example, as described above, the control signal 2508 may include the non-inverted control signal component 2508A and the inverted control signal component 2508B. In some embodiments, the non-inverted control signal component 2508A may be the non-inverted V_{RAMP} signal component, $V_{RAMP}+$, and the inverted control signal component 2508B may be the inverted V_{RAMP} signal component, $V_{RAMP}-$. Although not depicted in Figure 56, the differential digital-to-analog converter 2598 may further include anti-aliasing filters to accomplish proper image rejection after converting digital data into an analog signal.

[001713] The fixed delay circuit 2600 may provide a fixed delay to offset the propagation delay of the of the envelope magnitude, $\zeta_{MAGNITUDE}$, signal through the envelope tracking digital/analog section 2580 and provide a range of delay for the fine tuning delay circuit 2590. The fixed delay circuit 2600 receives the gain adjusted digital in-phase, $I_{DIGITAL_GAIN_ADJUSTED}$, component and the gain adjusted digital quadrature, $Q_{DIGITAL_GAIN_ADJUSTED}$, component from the digital gain control circuit 2576. The fixed delay circuit 2600 provides a delay adjusted digital in-phase component 2604 and a delay adjusted quadrature component 2618 as outputs.

[001714] The first digital-to-analog converter circuit 2606 is configured to receive the delay adjusted digital in-phase component 2604. The first digital-to-analog converter circuit 2606 converts the delay adjusted digital in-phase component 2604 into an analog signal to generate a pre-reconstruction in-phase component 2608, which is provided to the first anti-aliasing filter 2610. The first anti-aliasing filter 2610 filters the pre-reconstruction in-phase component 2608 to provide an analog in-phase component 2612 to be mixed.

[001715] Similarly, the second digital-to-analog converter circuit 2620 may receive the delay adjusted quadrature component 2618. The second digital-to-analog converter circuit 2620 converts the delay adjusted quadrature component 2618 into a pre-reconstruction quadrature component 2622, which is provided to the second anti-aliasing filter 2624. The second anti-aliasing filter 2624 filters the pre-reconstruction quadrature component 2622 to provide an analog quadrature component 2626 to be mixed.

[001716] The digital baseband circuit 2510 may further include an oscillator 2558, an in-phase component mixer 2614, I-Mixer, and a quadrature component mixer 2628, Q-Mixer. The oscillator 2558 is configured to generate a carrier signal 2558A having a transmit carrier frequency for a band of operation, which is provided to the quadrature component mixer 112, Q-Mixer, and the in-phase component mixer 2614, I-Mixer. The quadrature component mixer 2628, Q-Mixer, mixes the analog quadrature component 2626 to generate a modulated quadrature component 2630. The in-phase component mixer 2614, I-Mixer, mixes the analog in-phase component 2612 to generate a modulated in-phase component 2616. The modulated quadrature component 2630 and the modulated in-phase component 2616 are provided to a radio frequency attenuator 2632. The controller 50 may adjust the radio frequency attenuator 2632 to provide a magnitude of the modulated quadrature component 2630 and the modulated in-phase component 2616 used to provide the modulated radio frequency input signal 2504 having an input power P_{IN} to the radio frequency power amplifier 2540. The radio frequency attenuator 2632 may be either a digital radio frequency attenuator or an analog radio frequency attenuator.

[001717] The fine tuning delay time, T_{FINE_TUNING}, of the fine tuning delay circuit 2590 may be configured to adjust the group delay relationship between the control signal 2508 provided to the envelope tracking power converter system 2530 and the modulated radio frequency input signal 2504, P_{IN}, provided to the radio frequency power amplifier 2540. The output power of the amplified radio frequency output signal 2548 may depend on the relative group delay mismatch between the control signal 2508 and the modulated radio frequency input signal 2504, P_{IN}.

[001718] Figure 56 depicts a more detailed view of the digital baseband circuit 2510 including the baseband controller 2511, the transceiver circuitry 2512, and the configuration-feedback circuitry 2520. Although Figure 56 depicts that the transceiver circuitry 2512 and the configuration-feedback circuitry 2520 are substantially separate portions of the digital baseband circuit 2510, in some embodiments, the features and the functions of the transceiver circuitry 2512 and the configuration-feedback circuitry 2520 may be cooperatively shared.

[001719] Figure 56 further depicts an I/Q feedback system 2522 having a buffer 2552 configured to receive the measured amplified radio frequency output signal 2550 from the power coupler 2546. The buffer 2552 provides the measured amplified radio frequency output signal 2550 to the in-phase component feedback mixer 2554 and the quadrature component feedback mixer 2556. The in-phase component feedback mixer 2554 and the quadrature component feedback mixer 2556 may receive a carrier signal 2558A having a transmit carrier frequency from an oscillator 2558. The in-phase component feedback mixer 2554 and the quadrature component feedback mixer 2556 may demodulate the measured amplified radio frequency output signal 2550 to recover an in-phase feedback component 2562 and a quadrature feedback component 2564. The in-phase component feedback mixer 2554 may provide the in-phase feedback component 2562 to an in-phase component analog-to-digital converter 2566 to generate a digitized in-phase feedback component $I_{MEASURED}$ 2570. The quadrature component feedback mixer 2556 may provide the quadrature feedback component 2564 to a quadrature component analog-to-digital converter

2568 to generate a digitized quadrature feedback component $Q_{MEASURED}$ 2572. The fast calibration iso-gain and delay alignment circuitry 2524 and the transceiver power control loop circuitry 2526 may each receive the digitized in-phase feedback component $I_{MEASURED}$ 2570 and the digitized quadrature feedback component $Q_{MEASURED}$ 2572.

[001720] As a non-limiting example, the V_{CC} look up table 2586 may store a plurality of calibrated iso-gain contours. The iso-gain contours may be calibrated by measuring the relationship between a range of drive levels or input power P_{IN} levels of a modulated radio frequency input signal 2504 versus an output power P_{OUT} generated by the radio frequency power amplifier 2540 at a given modulated power supply voltage, V_{CC}. For example, in the simplest form, the input power P_{IN} for a modulated radio frequency input signal 2504 may be sweep through 27dBn to + 7 dbm at a given modulated power supply voltage Vcc. The fast calibration iso-gain and delay alignment circuitry 2524 may determine the output power generated in response to the input power P_{IN} level. The process may then be repeated for different magnitudes of the modulated power supply voltage, V_{CC}. As another non-limiting example, some embodiments of the fast calibration iso-gain and delay alignment circuitry 2524 may be described in the international patent application number PCT/ US2012/023495 and the United States Patent Application No. 13/363,888, each entitled, "Fast Envelope System Calibration," and each file on February 1, 2012, and which each claim the benefit of provisional patent application serial number 61/438,755, filed February 2, 2011.

[001721] As depicted in the Figure 57B, the measured data for the iso-gain contours may have a saw-tooth characteristic. As depicted in Figure 57A, the saw-tooth effect may be due in part to various corruption sources that affect the accuracy of calibration including feedback noise sources that impact the measured amplified radio frequency output signal 2550, carrier leakage from the oscillator 2558, quadrature mismatch between the in-phase component feedback mixer 2554 and the quadrature component feedback mixer 2556, and/or some combination thereof. To correct for the saw-tooth effect, as depicted in Figure

57B and described in 57C, the initial measured data may be post-process either by the controller 50, the baseband controller 2511, or factor test equipment to remove or minimize the impact of the corruption sources. For example, Figure 57C depicts a method 2900 for reducing a saw tooth-effect.

[001722] At the factor, an initial calibration of each iso-gain contour of a number of iso-gain contours to be stored in the V_{CC} lookup table 2586 may be initiated. (Step 2902.)

[001723] For each iso-gain contour of the number of iso-gain contours, the fast calibration iso gain and delay alignment circuitry 2524 may store a calibrated transmit-gain setting of the transceiver circuitry 2512, a calibrated measured transceiver temperature, and a calibrated transmitter frequency . (Step 2904.)

[001724] Thereafter, one of the controller 50, the baseband controller 2511, fast calibration iso-gain and delay alignment circuitry 2524, and/or factor test equipment may post process the initial iso-gain contour data for each of the iso-gain contours to remove or substantially reduce a saw tooth-effect substantially related to various corruption sources in the transceiver power control loop 2502. As an example, a fit-post processing algorithm may be applied to the initial iso-gain contour data to remove the overall saw tooth effect and recalculate discrete points for the V_{CC} look up table 2586 base on an interpolation process. As an example, the controller 50 or a factory calibration computer may execute the fit-processing and then recalculate the new discrete point to define the iso-gain curves. For example, in some embodiments, N data point may be used to generate an M^{th} order polynomial that provide a polyfit with respect to the initial iso-gain contour data. Other advance filtering techniques may also be applied to remove the saw tooth-effect and provide clean post processed calibrated iso-gain contour data. (Step 2906).

[001725] For each iso-gain contours, one of the controller 50, the baseband controller 2511, fast calibration iso-gain and delay alignment circuitry 2524, and/or factor test equipment may the store the post-processed (smoothed/interpolated/ filtered) initial iso-gain contour calibration data as

calibrated iso-gain contour calibration data in the V_{CC} look up table 2586. (Step 2908).

[001726] In response to receipt of the in-phase feedback component 2562, the in-phase component analog-to-digital converter 2566 provides the digitized in-phase feedback component $I_{MEASURED}$ 2570 to the fast calibration iso-gain and delay alignment circuitry 2524 and the transceiver power control loop circuitry 2526. Similarly, the quadrature component feedback mixer 2556, provides a quadrature feedback component 2564 to the quadrature component analog-to-digital converter 2568. In response, the quadrature component analog-to-digital converter 2568 provides the digitized quadrature feedback component $Q_{MEASURED}$ 2572 to both the fast calibration iso-gain and delay alignment circuitry 2524 and the transceiver power control loop circuitry 2526.

[001727] The transceiver power control loop circuitry 2526 may determine a measured output power, $P_{OUT_MEASURED}$, generated by the radio frequency power amplifier 2540 in response to the modulated radio frequency input signal 2504 having an input power P_{IN} and the control signal 2508. For example, the transceiver power control loop circuitry may calculate the measured output power, $P_{OUT_MEASURED}$, as a function of the digitized in-phase feedback component $I_{MEASURED}$ 2570 and the digitized quadrature feedback component $Q_{MEASURED}$ 2572. Based on the measured output power, $P_{OUT_MEASURED}$, and the transmit-target power setting parameter 2502A, the transceiver power control loop circuitry 2526 may generate a transmit-gain setting signal 2526A to minimize a difference between the measured output power, $P_{OUT_MEASURED}$, and the transmit-target power setting parameter. The transceiver power control loop circuitry 2526 may also provide the transmit-gain setting signal 2526A to a baseband controller 2511. In addition, in some embodiments, transceiver power control loop circuitry 2526 may provide the measured output power, $P_{OUT_MEASURED}$, to the controller 50 via the control bus 44. In this case, the baseband controller 2511 may provide the transmit-target power setting parameter to the transceiver power control loop circuitry 2526. In some embodiments, the pseudo-envelope follower gain controller 2574 may receive an

indication of the transmit-gain setting parameter of the transceiver from and the configuration-feedback circuitry 2520 via the transmit-gain setting signal 2526A.

[001728] Figures 58A-D depict a method 2700 for compensating a control signal generated as part of an envelope tracking system for changes in the drive level or input power P_{IN} of a modulated radio frequency input signal 2504. The digital baseband circuit 2510 may provide the modulated radio frequency input signal 2504 to the radio frequency power amplifier 2540 to generate the amplified radio frequency output signal 2548. The radio frequency power amplifier 2540 may provide the amplified radio frequency output signal 2548 to the antenna 2544 for transmission. A previously discussed, the transceiver power control loop 2502 may adjust the drive level or input power P_{IN} of the modulated radio frequency input signal 2504 in response a determination that the output power P_{OUT} of the amplified radio frequency output signal 2548, measured at the antenna 2544, outside a threshold limit of a target-transmit output power parameter. For example, the configuration-feedback circuitry 2520 may determine whether an output power of a radio frequency power amplifier is outside of a threshold limit of a target-transmit output power parameter. Based on a determination that the output power of the radio frequency power amplifier is outside of the threshold limit of the target-transmit output power parameter, a transceiver circuit configured to generate a modulated radio frequency input signal based on a difference between the output power of the radio frequency power amplifier and the target-transmit output power parameter, and generate a control signal to regulate generation of a modulated supply voltage to maintain a linear gain characteristic of the radio frequency power amplifier through a new dynamic range of the modulated radio frequency input signal.

[001729] The envelope tracking control system 2503 may be configured to compensate for a change in the input power P_{IN} or drive level of the modulated radio frequency input signal provided to the radio frequency power amplifier 2540. (Step 2702).

As an example, the pseudo-envelope follower gain controller 2574 may receive an indication of the transmit-gain setting parameter of the transceiver circuit from

and the configuration-feedback circuitry 2520 via the transmit-gain setting signal 2526A. In addition the pseudo-envelope follower gain controller 2574 may receive an indication of the transmit-target power setting parameter from the configuration-feedback circuitry 2520 via the transmit-target power setting signal 2526B. (Step 2704).

[001730] In response to receipt of the indication of the transmit-gain setting parameter, the pseudo-envelope follower gain controller 2574 may obtain or receive a value of the calibration transmit-gain setting parameter used during calibration of the iso-gain contours based on the transmit-target power setting parameter. (Step 2706**.)**

[001731] The pseudo-envelope follower gain controller 2574 may determine a transmit gain setting delta as a function of the indication of the transmit-gain setting of the transceiver and the calibration transmit-gain setting parameter. The transmit gain setting delta may be calculated by subtracting calibration transmit-gain setting parameter from the transmit-gain setting parameter. (Step 2708).

[001732] The pseudo-envelope follower gain controller 2574 may determine a compensation value for the pseudo-envelop following gain control signal as a function of the temperature of the transceiver circuitry 2512, the transceiver frequency, and/or a combination thereof (Step 2712.)

[001733] The pseudo-envelope follower gain controller 2574 may determine a measured temperature for the transceiver circuitry 2512. To determine a compensation value for the pseudo-envelop following gain control signal 2574A, the pseudo-envelope follower gain controller 2574 may receive a measured temperature for the transceiver circuitry 2512 form the temperature sensor 2516 via the temperature signal 2516A. (Step 2714.)

[001734] The pseudo-envelope follower gain controller 2574 may determine the measured calibration temperature of the transceiver circuitry 2512 during the calibration of the iso-gain contours during calibration of the iso-gain contours stored in the V_{CC} look up table 2586. As an example, in some embodiments, the baseband receive 2511 may obtain or receive the measured calibration

temperature of the transceiver circuitry 2512 from the controller 50. Alternatively, the measured calibration temperature of the transceiver circuitry 2512 may be stored in a memory or register accessible by the baseband controller 2511. In some embodiments, the controller 50 may provide the measured calibration temperature of the transceiver circuitry 2512 to the pseudo-envelope follower gain controller 2574. In still other embodiments, the pseudo-envelope follower gain controller 2574 may request the measured calibration temperature of the transceiver circuitry 2512 from the baseband controller 2511 or the controller 50. In still other embodiments, the measured calibration temperature of the transceiver circuitry 2512 may be provided to the pseudo-envelope follower gain controller 2574 prior to commencement of a data transmission. (Step 2716.)

[001735] The pseudo-envelope follower gain controller 2574 may subtract the measured calibration temperature from the measured transceiver temperature to determine a transceiver temperature delta. (Step 2718.)

[001736] Thereafter, the pseudo-envelope follower gain controller 2574 may determine a temperature induced transceiver circuitry gain change based on the transceiver temperature delta and a known temperature dependent transceiver gain change characteristic / function for the transceiver circuitry 2512. (Step 2720.)

[001737] In some embodiments of the envelope tracking control system 2503, the pseudo-envelope follower gain controller 2574 may further compensate the transceiver frequency being used to generate the modulated radio frequency input signal 2504. In other embodiments, the envelope tracking control system 2503 may determine whether to compensate for the transceiver frequency. For example, the envelope tracking control system 2503 may determine whether the present transceiver frequency is substantially near a calibration transceiver frequency used during calibration of the iso-gain contours stored in the stored in the V_{CC} look up table 2586. Based on a determination that the present transceiver frequency is substantially near the calibration transceiver frequency, the pseudo-envelope follower gain controller 2574 may determine to dispense with determining a compensation factor for a difference between the present

transceiver frequency and the calibration transceiver frequency. In other embodiments, the pseudo-envelope follower gain controller 2574 may always generate a compensation factor for a difference between the present transceiver frequency and the calibration transceiver frequency. (Step 2722.)

[001738] Based on a determination to not to generate a compensation factor for a difference between the present transceiver frequency and the calibration transceiver frequency. the pseudo-envelope follower gain controller 2574 may subtract the temperature induced transceiver circuitry gain change from the transceiver gain delta to generate the pseudo-envelope follower gain control signal. (Step 2724.)

[001739] Otherwise, based on a determination to to generate a compensation factor for a difference between the present transceiver frequency and the calibration transceiver frequency, the pseudo-envelope follower gain controller 2574 may determine compensation value for transceiver frequency as a function of the transceiver frequency and the calibration transceiver frequency used during calibration of the iso-gain contours stored in the stored in the V_{CC} look up table 2586. (Step 2726.)

[001740] The pseudo-envelope follower gain controller 2574 may obtain the transceiver frequency to be used during the data transmission. For example, in some embodiments, the pseudo-envelope follower gain controller 2574 may obtain or receive the transceiver frequency to be used during the data transmission from the baseband controller 2511, the controller 50, or the digital baseband circuit 2510. For example, the transceiver frequency may be based on the band of operation of the communication device. The controller 50 or the baseband controller 2511 may configure the oscillator 2558 to generate a carrier signal 2558A having a transceiver frequency substantially equal to the transceiver frequency to be used during the data transmission. (Step 2728.)

[001741] The pseudo-envelope follower gain controller 2574 may obtain the calibration transceiver frequency used during calibration of the iso-gain contours stored in the V_{CC} look up table 2586. For example, the pseudo-envelope follower gain controller 2574 may obtain or receive the calibration transceiver frequency

used during calibration of the iso-gain contours from the controller 50, the baseband controller 2511, or from a memory local to the digital baseband circuit 2510. In some embodiments, the The pseudo-envelope follower gain controller 2574 may receive the calibration transceiver frequency used during calibration of the iso-gain contours prior to initiation of a data transmission. (Step 2730.) The pseudo-envelope follower gain controller 2574 may subtract the calibration transceiver frequency from the transceiver frequency to be used during transmission to determine a transceiver frequency delta. (Step 2732.)

[001742] Thereafter, the pseudo-envelope follower gain controller 2574 may determine a transceiver frequency induced gain change based on the transceiver frequency delta and a know transceiver gain change characteristic / function for the transceiver circuitry with respect to a change in the transceiver frequency. (Step 2734.) The pseudo-envelope follower gain controller 2574 may subtract the temperature induced transceiver circuitry gain change and the transceiver frequency induced gain change from the transmit-gain setting delta to generate the pseudo-envelope follower gain control signal. (Step 2736.)

[001743] The pseudo-envelope follower gain controller 2574 may scale the envelope magnitude as a function of the pseudo gain control signal to generate an index input signal for the V_{CC} look up table 2586 that provides an emulation of the input power pin of the modulated radio frequency input signal provided to the radio frequency power amplifier. (Step 2738.)

[001744] The pseudo-envelope follower gain controller 2574 may generate a control signal to substantially operate on a single iso-gain contour related to the transmit-target output power setting parameter to minimize distortion in response to an increase in the input power pin of the modulated radio frequency input signal provided to the radio frequency power amplifier (Step 2740.) Thereafter, the digital baseband circuit 2510 may commence the data transmission. (Step 2742.)

[001745] Figures 59-60 depict an embodiment of a switch mode power supply switching frequency control system 3000 that includes an embodiment of the

average frequency control circuit 885, depicted as the average frequency control circuit 3002.

[001746] Figure 59 depicts a switch mode power supply switching frequency control system 3000 configured to adjust the switching frequency of the switch mode power supply to strategically place harmonics of the switching frequency in a desired location of the frequency spectrum. In addition, the switch mode power supply switching frequency control system 3000 may be configured to move a first harmonic frequency of the switching frequency by a desired amount such that the first harmonic frequency falls outside a band of frequency and a second harmonic frequency of the switching frequency remains outside of the band of frequencies. The switch mode power supply switching frequency control system 3000 may be described with respect to the various embodiments of the pseudo-envelope tracking modulated power supply system 868 and the pseudo-envelope tracking modulated power supply system 868A, depicted in Figures 40A-E, and Figures 46A-B and Figure 46E-H, the various embodiments of the power management system 870, depicted in Figures 40A-C, the power management system 870A, depicted in Figures 46A-C, the power management system 870B and parallel amplifier circuit 874B', depicted in Figure 40D, the power management system 870C and parallel amplifier circuit 874C', depicted in Figure 40E, the power management system 870E and parallel amplifier circuit 874E', depicted in Figure 46E, power management system 870F and parallel amplifier circuit 874F', depicted in Figure 46F, the power management system 870G and parallel amplifier circuit 874G', depicted in Figure 46G, and the power management system 870H and parallel amplifier circuit 874H', depicted in Figure 46H.

[001747] The switch mode power supply switching frequency control system 3000 may include the average frequency control circuit 3002 in communication with a controller 50, trigger circuitry 3006 configured to provide a trigger signal 3010 to frequency control circuitry 3012 based on a master bus signal, and the switcher control circuit 52S. As depicted in Figure 61, the trigger signal 3010 may be generated in a periodic fashion in response to receipt of the master bus

signal. Referring to Figure 55-56, the master bus single may be associated with a digital modem or digital baseband circuit 2510 configured to control the operation of an envelope power tracker converter system 2540. For example, in some embodiments the master bus signal may be generated by the front-end control interface circuit 2514. The periodicity of the master bus signal may be generated basd on a master system clock of the communication device in a communication network. The master system clock may be locked to a time base related to providing time slots for transmitting data. For example, each time slot may have a time slot period, T_{SLOT}, which may be used to regulated the switching frequency of the switch mode power supply converter 872. As an example, a counter valude that may be pre-loaded into a counter or compared to a counter output may be calculated based on time slot period, T_{SLOT}. As an example, a target value for an average switching frequency of a switch mode power supply converter 872 may be multiplied by the time slot period, T_{SLOT}, to obtain a predeteremined counter value. The counter value may be used to determine whether the switch mode power supply converter 872 is operating at a switching frequency that is greater than or less than the target value for an average switching frequency by comparing a counter output of the counter 3016 to the predeteremined counter value.

[001748] Returning to Figures 59-60, if the counter output of the counter 3016 is greater than the predeteremined counter value, the switching frequency of the switch mode power supply converter 872 is too high. In response, the average frequency control circuit 3002 may increase the value of the adjusted shunt level threshold parameter 3048 to slow the switching frequency. Conversely, if the counter output of the counter 3016 is less than the predeteremined counter value, the switching frequency of the switch mode power supply converter 872 is too low. In response, the average frequency control circuit 3002 may decrease the value of the adjusted shunt level threshold parameter 3048 to slow the switching frequency.

[001749] The average frequency control circuit 3002 may include a the frequency controller circuitry 3012 configured to be enabled by the AVFC enable

signal, a divider 3014 configured to receive a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$, from the switcher control circuit 52S, and a counter 3016 configured to receive a counter clock 3022 from the divider 3014.

[001750] The frequency controller circuitry 3012 may configured the divider 3014 to divide by a ratio of 1, 2, 4 or 8 based on a divider setting signal provided by the divider setting output of the frequency controller circuitry 3012. The frequency controller circuitry 3012 may asset a counter enable signal 3024 to enable the counter 3016 to commence counting. The frequency controller circuitry 3012 may generate a counter reset signal 3026 to reset the counter 3016. The frequency controller circuitry 3012 may load the predetermined counter value into the coutner 3016 via the counter preload signal generated by the counter preload output. In response to receipt of a trigger signal 3010, the frequency control circuit may enable the coutner 3016 to begin counting down. Upon recipt of the next trigger signal 3010, the accumulator 3018 may sample the overflow indicator to determine whether the counter reached a value substantially equal to the predetermined counter value. Intially the accumulator loads the intial shunt level threshold level to generate the adjusted shunt threshold 3032. In the case where the overflow indicator is asserted, which means the switching frequency of the switch mode power supply converter 872 is above the target average switching frequency, the accumulator 3018 may be configured to add a step size to the adjusted shunt threshold 3032 to generate a new value of the adjusted shunt level threshold 3032. In the case where the overflow indicator is de-asserted, which means the switching frequency of the switch mode power supply converter 872 is below the target average switching frequency, the accumulator may subtract the step size from the adjusted shunt level threshold. The step size may be

[001751] The average frequency control circuit 3002 may also include an accumulator 3018 configured to receive a shunt level threshold parameter 3004 from a programmable threshold circuit 122A and an overflow indicator 3009 from the counter 3016, and the trigger signal 3010 from the trigger circuitry 3008.

[001752] The average frequency control circuit 3002 may further include a toggle circuit 3040 configured to receive the counter clock 3022 and a toggle enable signal from a toggle enable fo the frequency controller circuitry 3012.

[001753] The average frequency control circuit 3002 may also include a first adder 3034 configured to add a toggle signal 3044 generated by the toggle circuit 3040 to an adjusted shunt threshold 3032 generated by the accumulator 3018. The average frequency control circuit 3002 may also include a dither circuit 3042 configured to generate a dither signal 3046 as a function of a dither range signal and a dither enable signal provided by the dither range output and the dither range output of the frequency controller circuitry 3012. A second adder 3047 may add the dither signal 3046 to the sum of the toggle signal 3044 and the adjusted shunt level threshold 3032 generated by the first adder 3034 to generate an adjusted shunt level threshold parameter 3048 that is provide to the programmable threshold circuit 122A of the switcher control circuit 52S. The programmable threshold circuit 122A may include a shunt level threshold parameter select multiplxer or switch 124A configured to provide a shunt level threshold 124 to the non-inverting input of the first comparator 140. The shunt level threshold parameter select multiplxer or switch 124A may receive an average frequency control (AVFC) enable signal. When the average frequency control circuit 3002 is enabled to govern the switching frequency of the switch mode power supply converter 876, the average frequency control (AVFC) enable signal is asserted. In response, the shunt level threshold parameter select multiplxer or switch 124A may provide the adjusted shunt level threshold parameter to generate the shunt level threshold 124. In this case, the average frequency control circuit 3002 may provide a closed loop control mode for adjusting the average switching frequency of the switch mode power supply converter 872. Otherwise, when the average frequency control (AVFC) enable signal is de-asserted, the shunt level threshold parameter select multiplxer or switch 124A may provide shunt level threshold parameter to generate the shunt level threshold 124. When the average frequency control (AVFC) enable signal is de-asserted, the controller 50 may configure the shunt level threshold

parameter to control the switching frequency of the switch mode power supply converter 872 in an open loop control mode.

[001754] The average frequency control circuit 3002 may be configured to generate an adjusted shunt level threshold 3032 based on the shunt level threshold parameter stored in an embodiment of the programmable threshold circuit 122A of the switcher control circuit 52S, a pre-determined counter value 3006 provided as a counter preload to the counter 3016, and a counter clock that is derived from a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$. The pre-determined counter value 3006 may correspond to a target switching frequency, and a counter clock 3022 derived from a logic level indication of the switching voltage output, $V_{SW_EST_OUT}$.

[001755] The logic level indication of the switching voltage output, $V_{SW_EST_OUT}$ may effectively provide an indication of the switching frequency of the switch mode power supply converter 872. Depending on the overflow indicator 3009 of the counter 3016, the accumulator 3018 may either increase or decrease the value of the shunt level threshold parameter to provide an adjusted shunt level threshold 3032. In some embodiments, the average frequency control circuit 3002 may include a toggle circuit 3040. In some embodiments, the toggle circuit 3040 may be configured to toggle the magnitude of the adjusted shunt level threshold 3032 with a toggle signal 3044 generated based on a programmable toggle value. In other embodiments, the toggle circuit 3040 may be configured to toggle the magnitude of the adjusted shunt level threshold 3032 by one-half of a least significant bit of the adjusted shunt level threshold 3032. For example, in some embodiments, the toggle circuit 3040 may toggle the magnitude of the adjusted shunt level threshold 3032 on every transmission slot boundary to obtain an average switching frequency near or at the target switching frequency set by the pre-determined counter value. In doing so, the average frequency control circuit 3002 may effectively provide an additional effective resolution or granularity substantially equal to one-half of the least significant bit of the shunt level threshold parameter. Toggling the magnitude of the shunt level threshold 124 may tend to spread the energy present in any spurious emissions

across a band of frequencies, which may reduce the maximum peak energy level of the spurious emissions related to the switching frequency of the switch mode power supply converter as a function of how fast the switch mode power supply converter 872 changes the average switching frequency of the switch mode power supply converter 872. At the same time, toggling the magnitude of the shunt level threshold 124 may also have an effect similar to frequency hopping. In addition, some embodiments of the average frequency control circuit 3002 may further include a dither circuit 3042 configured to provide a dither signal 3046 having a programmable dither magnitude. The dither signal 3046 may be applied to the sum of the adjusted shunt level threshold 3032 and the toggle signal 3044 during a data transmission. The dither circuit 3044 may generate different degrees or magnitudes of dithering. The higher the magnitude of the dither signal 3046, the greater the spreading of the energy in the harmonic switching frequencies. As an example, in some embodiments, the dither signal 3044 may have a substantially random or pseudo-random magnitude. In some embodiments, the dither signal 3044 may have a mean value substantially equal to zero. The dither signal 3044 may either increase or decrease the switching frequency of the switch mode power supply converter 872. In some embodiments, dither signal 3046 may be generated based on a pseudo-random binary sequence having an auto correlation function substantially equal to zero and a duty cycle. In some embodiments, the controller 50 may configure the duty cycle of the pseudo-random binary sequence. In other embodiments, the duty cycle of the pseudo-random binary sequence may be fixed. When applied to the adjusted shunt level threshold 3032, the toggle signal 3044 and the dither signal 3046 generate an adjusted shunt level threshold parameter 3048 that may be selectively used by the switcher control circuit 52S to govern the generation of the switching frequency in a closed loop system while also spreading energy of the harmonics of the switching frequency to lower the magnitude of the peak energy in the harmonics of the switching frequency.

[001756] Figure 62 depicts an embodiment of a power supply selection system 3050 configured to provide a desired power supply voltage to the parallel

amplifier 928, the first linear regulator 950, the second linear regulator 952, and V_{CMOS} Output. Figure 62 is described with continuing reference to Figure Figures 40A-E, and Figures 46A-H, and Figure 52B.

[001757] A power supply selection system 3050 includes controller 50 in communication with a first supply select circuit 3052, a second supply select circuit 3054, a third supply select circuit 3056, and a fourth supply select circuit 3058. Each of the first supply select circuit 3052, the second supply select circuit 3054, the third supply select circuit 3056, and the fourth supply select circuit 3058 may receive a battery voltage, V_{BAT}, a first output voltage VFIRST-OUTPUT generated by the charge pump 2390B and a second output voltage VSECOND-OUTPUT provided at the second output 2396 of the charge pump 2390B, as depicted in Figure 52B.

[001758] The first supply select circuit 3052 may be configured to provide a paralle amplifer supply voltage 3070 to the parallel amplifier 928. The second supply select circuit 3054 may be configured to provide a seond linear regular supply voltage 3072 to the noise filter 952, which provide a filtered µC charge pump output voltage, $V_{\mu C_FILTERED}$, to the second linear regulator 952. The third supply select circuit 3056 is configured to provide a first linear regulator supply voltage 3074 to the first linear regulator 950. The fourth supply select circuit 3058 is configured to provide the CMOS logic supply voltage 878C, V_{CMOS}, to the the V_{CMOS} Output of the parallel amplifier circuit 874', as depicted in Figure 46B.

[001759] The controller 50 may provide a first supply select signal 3060 to the first supply select circuit 3052, a second supply select signal 3062 to the second supply select circuit 3054, a third supply select signal 3064 to the third supply select circuit 3056, and a fourth supply select signal 3066 to the fourth supply select circuit 3058. As previously described above, the controller 50 may determine the power supply needs of the parallel amplifer 928, the first linear regular 950, the second linear regular 952, and the CMOS logic 869E of the radio frequency power amplifier 869' based on the the maximum expected power amplifier supply voltage, V_{CC_MAX}, the minimum driver supply voltage threshold, and the minimum CMOS logic supply voltage threshold. In addition, the

controller 50 may obtain a measurement of the battery voltage, V_{BAT}. Based on the combination of supply requirements, the controller 50 may configure the charge pump 2390B to generate first output voltage $V_{FIRST-OUTPUT}$ and a second output voltage $V_{SECOND-OUTPUT}$ that will result in a minimum energy drain from the battery 20 in order to meet each of the supply voltage requirements of the parallel amplifier 928, the first linear regulator 950, the second linear regulator 952, and the CMOS logic 869E. The controller 50 may then selectively configure the first supply select circuit 3052, a second supply select circuit 3054, a third supply select circuit 3056, and a fourth supply select circuit 3058 to provide a minimum supply voltage necessary to power each of the circuits.

[001760] Figure 63 depicts a supply switching circuit 3100A configured to selective provide a selected supply voltage, VDD, to an IC circuit block 3638. The supply switching circuit 3100A may include a first first inverter level translator 3110 powered by a first supply voltage VDD1, a second inverter level translator 3112 powered by a second supply voltage VDD2, a third inverter level translator 3114 powered by the first supply voltage VDD1 and a fourth inverter level translator 3116 power by the second supply voltage VDD2.

[001761] The a first pfet transistor PFET1 3102 has a source coupled to the first supply voltage VDD1, a gate configured to be controlled by the first inverter level translator 3110, and a drain coupled to the source tof the third pfet transistor PFET3 3106. The second pfet transistor PFET2 3104 has a source coupled to the second supply volage VDD2, a gate configured to be controlled by the second inveterter level translator 3112, and a drain couple to the source of a fourth pfest transistor PFET4 3108. The drain of each of the third pfet transistor 3106 and the forth pfet transitor 3108 are coupled to a level translator with complementary output 3132. The controller 50 may control the first inverter level translator 3110, the second inverter level translator 3112, the third inveter level translator 3114, the fourth inverter translator 3116 and the level translator with complementary output 3132 to control a first power pfet PFETA 3134 coupled and a second power pfet PFETB 3136 to provide either the first supply voltage VDD1 or the second supply voltage VDD2 to the IC circuit block 3638.

[001762] Those skilled in the art will recognize improvements and modifications to the embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed:

Claims

1. A modulated power supply system comprising:

a parallel amplifier configured to: apply a parallel amplifier output current to a radio frequency power amplifier supply output based on a control signal and a power amplifier supply voltage voltage based on an expected output power of the radio frquency power amplifier being greater than a low power modulation mode threshold;

an low dropout regulator (LDO) configured to: apply an output current to a radio frequency power amplifier supply output based on the control signal and the power amplifier supply voltage based on the expected output power of the radio frequency amplifier being greater than the low power modulation mode threshold; and

a switching power supply converter configured to: generate a switching voltage at a switching voltage output to apply a switching current to radio frequency power amplifier supply output based on the expected output power of the radio frequency power amplifier being greater than the low power modulation mode threhold.

2. A selectable power source system for minimizing energy consumption from a battery comprising:

a charge pump configured to receive a battery voltage, and generate a charge pump output voltage as a function of the battery voltage, a maximum expected modulated power supply voltage, and a minimum first supply voltage parameter;

a parallel amplifier including:

a first selectable power supply input configured to:

receive the charge pump output voltage and the battery voltage, and

select one of the charge pump output voltage and the battery voltage having a least magnitude voltage that is at least equal to the maximum expected modulated power supply voltage and a headroom voltage of the parallel amplifier as a parallel amplifier supply voltage;

the parallel amplifier configured to:

generate a parallel amplifier output current from the parallel amplifier supply voltage as a function of a control signal to regulate a modulated power supply voltage to be provided to a radio frequency power amplifier during a data transmission;

a first supply output including:

a selectable power supply input configured to receive at least one of the at least one charge pump output voltage and the battery voltage; and

a supply output in communication with a first supply input of the radio frequency power amplifier, and configured to provide a first supply voltage to the first supply input of the radio frequency power amplifier as a function of the battery voltage and a minimum first supply voltage parameter.

3. An envelope tracking control system with power control loop compensation comprising:

- an output power control loop configured to:
  - determine an output power of an amplified modulated radio frequency output signal generated by a radio frequency power amplifier in response to a modulated radio frequency input signal and a modulated power supply voltage associated with the modulated radio frequency input signal;
  - generate an adjustment for a drive level of the modulated radio frequency input signal based on a difference between

the output power of the amplified modulated radio frequency output signal and a transmit-target output power level; and

- an envelope control loop configured to:
  - generate a gain control adjustment as a function of the adjustment for the drive level of the modulated radio frequency input signal;
  - generate a control signal having sufficient dynamic range to avoid gain compression due the adjustment of the drive level of the modulated radio frequency input signal based on a magnitude of an input signal used to generate the modulated radio frequency input signal and the gain control adjustment; and
  - provide the control signal to an envelope tracking power converter to govern generation of the modulated power supply voltage.

4.. The envelope tracking control system of claim 3 further comprising:

- the output power control loop further configured to generate a transmit-gain setting based on the adjustment for the drive level of the modulated radio frequency input signal; and
- a pseudo envelope tracking control circuit configured to
  - receive the transmit-gain setting; and
  - determine a transmit-gain setting difference between the transmit-gain setting and a calibration transmit-gain setting used during calibration of an iso-gain contour.

5. A method for providing a modulated power supply for a radio frequency power amplifier comprising:

prior to a data transmission, determining an expected output power of the radio frequency power amplifier to be generated by the radio frequency power amplifier during the data transmission; and

based on a determination that the expected output power of the radio frequency power amplifier is less than a low power modulation mode threshold, applying an output current from a linear regulator to generate a modulated power supply voltage at a modulated power supply output.

6. The method of claim 5 further comprising:

applying a parallel amplifier output current from a parallel amplifier to the modulated power supply output to generate the modulated power supply voltage based on a determination that the expected output power of the radio frequency power amplifier is greater than the low power modulation mode threshold.

7. The method of claim 6 wherein applying the parallel amplifier output current to the modulated power supply output from the parallel amplifier to the modulated power supply output comprises:

generating the parallel amplifier output current based on a control signal and the modulated power supply voltage.

8. The method of claim 7 wherein generating the parallel amplifier output current based on the control signal and the modulated power supply voltage comprises:

receiving a differential control signal to regulate generation of the modulated power supply voltage;

filtering the differential control signal to generate a compensated control signal based on the expected output power of the radio frequency power amplifier; and

providing the compensated control signal to the parallel amplifier as the control signal.

9. The method of claim 8 wherein filtering the differential control signal to generate the compensated control signal based on the expected output power of the radio frequency power amplifier further comprises:

applying a first level of frequency compensation based on a determinaion that the expected output power of the radio frequency power amplifier is less than a first power modulation mode threshold, wherein the first power modulation mode threshold is greater than the low power modulation mode threshold.

10. The method of claim 9 wherein filtering the differential control signal to generate the compensated control signal based on the expected output power of the radio frequency power amplifier further comprises:

applying a second level of frequency compensation based on a determination that the expected output power of the radio frequency power amplifier is greater than the first power modulation mode threshold.

11. The method of claim 10 wherein the first power modulation mode threshold is a high power modulation mode threshold.

12. The method of claim 10 wherein the second level of frequency compensation is greater than the first level of frequency compensation.

13. The method of claim 12 wherein applying the second level of frequency compensation that is greater than the first level of frequency compensation comprises:

appling a higher level of frequency peaking to the differential control signal to generate the compensated control signal.

14. The method of claim 1 wherein applying the parallel amplifier output current from the parallel amplifier to the modulated power supply output to generate the modulated power supply voltage based on the determination that the expected output power of the radio frequency power amplifier is greater than the low power modulation mode threshold further comprises:

based on a determination that the expected output power to be generated by the radio frequency power amplifier is less than a high power modulation

mode threshold, generating the parallel amplifier output current with less than all of a plurality of parallel amplifier output driver segments.

15. The method of claim 6 wherein applying the parallel amplifier output current from the parallel amplifier to the modulated power supply output to generate the modulated power supply voltage based on the determination that the expected output power of the radio frequency power amplifier is greater than the low power modulation mode threshold further comprises:

generating a switching voltage at a switching voltage output of a switch mode power supply converter to induce generation of a switching current applied to the modulated power supply output.

16. The method of claim 15 wherein generating the switching voltage at the switching voltage output of the switch mode power supply converter to induce generation of the switching current applied to the modulated power supply output comprises:

based on a determination that the expected output power to be generated by the radio frequency power amplifier is less than a high power modulation mode threshold, selecting less than all of a plurality of segmented series switches of the switch mode power supply converter to generate the switching voltage.

17. The method of claim 16 wherein based on the determination that the expected output power to be generated by the radio frequency power amplifier is less than the high power modulation mode threshold, selecting the less than all of the plurality of segmented series switches of the switch mode power supply converter to generate the switching voltage further comprises:

selecting less than all of a plurality of segmented shunt switches of the switch mode power supply converter to generate the switching voltage.

18. The method of claim 17 wherein generating the switching voltage at the switching voltage output of the switch mode power supply converter to induce generation of the switching current applied to the modulated power supply output further comprises:

receiving a battery voltage from a battery at the switch mode power supply converter; and

controlling an on state and an off state for each of the less than all of the plurality of segemented series switches and an on state and an off state for each of the less than all of the plurality of segmented shunt switches selected to generate the switching voltage at the switching voltage output of the switch mode power supply converter as a function of the expected output power to be generated by the radio frequency power amplifier during the data transmission to minimize a battery current drawn from the battery.

19. The method of claim 15 wherein generating the switching voltage at the switching voltage output of the switch mode power supply converter to induce generation of the switching current applied to the modulated power supply output comprises:

based on a determination that the expected output power to be generated by the radio frequency power amplifier is less than a high power modulation mode threshold, operating the switch mode power supply converter in only a bang-bang mode of operation to generate the switching voltage at the switching voltage output of the switch mode power supply converter.

20. The method of claim 15 wherein generating the switching voltage at the switching voltage output of the switch mode power supply converter to induce generation of the switching current applied to the modulated power supply output comprises:

based on a determination that the expected output power to be generated by the radio frequency power amplifier is less than a high power modulation

mode threshold, operating the switch mode power supply converter in a plurality of buck operational modes to generate the switching voltage.

21. The method of claim 20 wherein:

the plurality of buck operational modes further includes a first output mode of operation; and

operating the switch mode power supply converter in the plurality of buck operational modes to generate the switching voltage comprises:

receiving a supply voltage at the switch mode power supply converter; and

generating the switching voltage at the switching voltage output of the switch mode power supply converter that is between a reference voltage and the supply voltage of the switch mode power supply converter in the first output mode of operation.

22. The method of claim 21 wherein generating the switching voltage at the switching voltage output of the switch mode power supply converter that is between the reference voltage and the supply voltage in the first output mode of operation comprises:

controlling a switching network of the switch mode power supply converter to switchably connect only a first flying capacitor and a second flying capacitor of the switch mode power supply converter in communication with the switching voltage output to generate the switching voltage that is substantially equal to one-half the supply voltage at the switching voltage output.

23. The method of claim 21 wherein operating the switch mode power supply converter in the plurality of buck operational modes to generate the switching voltage comprises:

generating the switching voltage at the switching voltage output by operating the switch mode power supply converter in the plurality of buck operational modes and a first boost mode of operation to generate the switching voltage at the switching voltage output, wherein the switching voltage generated

by operating the switch mode power supply converter in the first boost mode of operation is less than twice the supply voltage.

24. The method of claim 23 wherein generating the switching voltage at the switching voltage output by operating the switch mode power supply converter in the first boost mode of operation comprises:

controlling a network of switches in the switch mode power supply converter to place only a first flying capacitor and a second flying capacitor in parallel and switchably coupling the first flying capacitor and the second flying capacitor between the supply voltage and the switching voltage output of the switch mode power supply converter to generate the switching voltage substantially equal to three-halves the supply voltage.

25. The method of claim 21 wherein receiving the supply voltage at the switch mode power supply converter comprises:

receiving the supply voltage derived from a battery.

26. The method of claim 25 wherein the supply voltage is substantially equal to a battery voltage of a battery in communication with the switch mode power supply converter.

27. The method of claim 6 wherein based on the determination that the expected output power to be generated by the radio frequency power amplifier is less than the low power modulation mode threshold, applying the output current from the linear regulator to generate the modulated power supply voltage at the modulated power supply output further comprises:

disabling a switching voltage output of a switch mode power supply converter and a parallel amplifier output of the parallel amplifier to provide a high impedance at the switching voltage output of the switch mode power supply converter and a high impedance at the parallel amplifier output of the parallel amplifier; and

switchably coupling the parallel amplifier output of the parallel amplifier to a reference voltage.

28. The method of claim 27 wherein based on the determination that the expected output power to be generated by the radio frequency power amplifier is less than the low power modulation mode threshold, applying the output current from the linear regulator to generate the modulated power supply voltage at the modulated power supply output further comprises:

disabling an active noise reduction circuit.

29. The method of claim 28 wherein disabling the active noise reduction circuit comprises;

disabling generation of an open loop ripple compensation current to be applied to the modulated power supply output.

30. The method of claim 28 wherein disabling the active noise reduction circuit comprises:

disabling an output impedance compensation circuit;

providing a control signal to the linear regulator that is uncompensated for an output impedance characteristic of the parallel amplifier; and

generating the output current from the linear regulator based on the control signal and the modulated power supply voltage.

31. The method of claim 6 wherein generating the modulated power supply voltage with the parallel amplifier based on the determination that the expected output power of the radio frequency power amplifier is greater than the low power modulation mode threshold further comprising:

generating the modulated power supply voltage with a switch mode power supply converter in combination with the parallel amplifier.

32. The method of claim 31 wherein generating the modulated power supply voltage with the switch mode power supply converter in combination with the parallel amplifier further comprises:

placing the linear regulator in a high impedance mode of operation.

33. The method of claim 5 further comprising:

disabling the linear regulator based on a determination that the expected output power of the radio frequency power amplifier is greater than the low power modulation mode threshold.

34. The method of claim 33 wherein disabling the linear regulator based on the determination that the expected output power of the radio frequency power amplifier is greater than the low power modulation mode threshold further comprises:

configuring the linear regulator to have a high output impedance.

35. The method of claim 5 further comprising:

based a determination that the expected output power of the radio frequency power amplifier is greater than the low power modulation mode threshold, switchably connecting a linear regulator output of the linear regulator to provide a communication path for applying a linear regulator supply voltage to a bias circuit of the radio frequency power amplifier.

36. The method of claim 5 further comprising:

determining a voltage level of the supply voltage;

based on the voltage level of the supply voltage, configuring a charge pump to generate a charge pump output voltage;

providing the charge pump output voltage to the linear regulator to

37. The method of claim 7 further comprising:

receiving a supply voltage at a switch mode power supply converter; and

based on the determination that the expected output power of the radio frequency power amplifier is greater than a low power modulation mode threshold, generating a switching voltage at a switching voltage output to induce a switching current applied to the modulated power supply output.

38. The method of claim 37 wherein generating a switching voltage at a switching voltage output to induce a switching current applied to the modulated power supply output comprises:

controlling a switching network of the switch mode power supply converter to switchably connect a first terminal of a first flying capacitor and a first terminal of a second flying capacitor of the switch mode power supply converter to the switching voltage output and a second terminal of the first flying capacitor and a second terminal of the second flying capacitor as a function of a composite feedback signal to generate the switching voltage at the switching voltage output.

39. The method of claim 38 wherein controlling the switching network of the switch mode power supply converter to switchably connect the first terminal of the first flying capacitor and the first terminal of the second flying capacitor of the switch mode power supply converter to the switching voltage output and the second terminal of the first flying capacitor and the second terminal of the second flying capacitor as a function of the composite feedback signal to generate the switching voltage at the switching voltage output comprises:

controlling the switching network of the switch mode power supply converter to switchably connect the second terminal of the first flying capacitor and the second terminal of the second flying capacitor to a reference voltage to provide the switching voltage at the switching voltage output.

40. The method of claim 38 wherein wherein controlling the switching network of the switch mode power supply converter to switchably connect the first terminal of the first flying capacitor and the first terminal of the second flying capacitor of the switch mode power supply converter to the switching voltage

output and the second terminal of the first flying capacitor and the second terminal of the second flying capacitor as the function of the composite feedback signal to generate the switching voltage at the switching voltage output comprises:

controlling the switching network of the switch mode power supply converter to switchably connect the second terminal of the first flying capacitor and the second terminal of the second flying capacitor to the supply voltage to provide the switching voltage, wherein the switching voltage is greater than the supply voltage.

41. The method of claim 38 wherein controlling the switching network of the switch mode power supply converter to switchably connect the first terminal of the first flying capacitor and the first terminal of the second flying capacitor of the switch mode power supply converter to the switching voltage output and the second terminal of the first flying capacitor and the second terminal of the second flying capacitor as the function of the composite feedback signal to generate the switching voltage further comprises:

generating the switching voltage that is greater than the supply voltage only based on a dermination that the expected output power of the radio frequency power amplifier is greater than a high power modulation mode threshold.

42. The method of claim 8 wherein generating a switching voltage at a switching voltage output to induce a switching current applied to the modulated power supply output comprises:

controlling a switching network of a switch mode power supply converter to switchably connect a first terminal of a first flying capacitor of the switch mode power supply converter to the switching voltage output, a second terminal of the first flying capacitor to a first terminal of a second flying capacitor of the switch mode power supply converter, and a second terminal of the second flying

capacitor to the supply voltage as a function of a composite feedback signal to generate the switching voltage at the switching voltage output.

43. The method of claim 37 wherein generating the switching voltage at the switching voltage output to induce the switching current applied to the modulated power supply output comprises:

based on a determination that the expected output power of the radio frequency power amplifier is greater than a medium power average power mode tracking mode threshold, generating the composite feedback signal based on a slope of the control signal.

44. The method of claim 43 wherein generating the composite feedback signal based on the slope of the control signal further comprises:

generating the composite feedback signal based on the slope of the control signal and the parallel amplifier output current.

45. The method of claim 44 wherein generating the composite feedback signal based on the slope of the control signal and the parallel amplifier output current further comprises:

generating the composite feedback signal based on the slope of the control signal, the parallel amplifier output current, and an noise reduction output current generated by an active noise reduction circuit.

46. The method of claim 45 wherein generating the noise reduction output current by the active noise reduction circuit comprises:

generating a switching voltage output estimate with the switch mode power supply converter based on an operational state of a switcher control circuit of the switch mode power supply converter;

generating a high frequency ripple compensation current based on the switching voltage output estimate and the control signal; and

applying the high frequency ripple compensation current to the modulated power supply output as the noise reduction output current.

47. The method of claim 6 further comprises:

receiving a supply voltage at a switch mode power supply converter; and

based on a determination that the expected output power of the radio frequency power amplifier is greater than a high power modulation mode threshold, boosting the supply voltage to generate a switching voltage at a switching voltage output of the switch mode power supply converter, wherein the switching voltage is greater than the supply voltage; and

applying the switching voltage at the switching voltage output of the switch mode power supply converter to induce generation of an inductor current applied to the modulated power supply output.

48. The method of claim 5 further comprising:

transmitting the data transmission in a data transmission slot.

49. The method of claim 5 further comprising;

deactivating a coupling circuit between the modulated power supply output and a parallel amplifier output of a parallel amplifier while generating the modulated power supply voltage with the linear regulator.

50. The method of claim 5 wherein the output current is based on a reference voltage and the modulated power supply output voltage.

51. The method of claim 5 wherein applying the output current from the linear regulator to generate the modulated power supply voltage at the modulated power supply output comprises:

generating the output current based on a difference between a V_{RAMP} signal and the modulated power supply voltage at the modulated power supply output.

52. The method of claim 51 further comprising:

transmitting the data transmission during a data transmission slot, wherein the V_{RAMP} signal is substantially constant throughout the data transmission.

53. The method of claim 5 wherein applying an output current from the linear regulator to generate the modulated power supply voltage at the modulated power supply output comprises providing the output current from a low drop out regulator.

54. The method of claim 6 further comprises:

receiving a control signal to govern generation of the modulated power supply voltage;

based on a determination that the expected output power to be generated by the radio frequency power amplifier is between a medium power modulation mode threshold and the low power modulation mode threshold, generating a switch mode power supply converter control signal based on the control signal;

generating a switching voltage at a switching voltage output of a switch mode power supply converter from a supply voltage based on the switch mode power supply converter control signal; and

applying the switching voltage at the switching voltage output to induce generation of an inductor current applied to the modulated power supply output.

55. The method of claim 54 wherein based on the determination that the expected output power to be generated by the radio frequency power amplifier is between the medium power modulation mode threshold and the low power modulation mode threshold, generating the switch mode power supply converter control signal based on the control signal further comprises:

disabling the parallel amplifier.

56. The method of claim 54 wherein generating the switch mode power supply converter control signal based on the control signal comprises:

receiving a control signal;

generating an error signal substantially equal to the modulated power supply voltage less the control signal; and

generating the switch mode power supply converter control signal based on the error signal and a programmable gain factor.

57. The method of claim 56 wherein receiving the control signal comprises:

disabling a differntial filter configured to generate a frequency compensated control signal;

receiving a differential control signal; and

converting the differential control signal into the control signal, wherein the control signal is a single ended control signal.

58. The method of claim 57 wherein receiving the differential control signal comprises receiving a differential V_{RAMP} signal.

59. The method of claim 58 wherein the control signal is a substantially constant voltage level during transmission of a data burst by the radio frequency power amplifier during a data transmission slot.

60. The method of claim 54 wherein generating the switching voltage at the switching voltage output of the switch mode power supply converter from the supply voltage based on the switch mode power supply converter control signal comprises:

determining a voltage level of the supply voltage;

based on an envelope characteristic of a data burst to be transmitted by the radio frequency power amplifier, determining a maximum voltage level of the modulated power supply voltage; and

selecting a selected bang-bang mode of operation of a plurality of bang-bang modes of operation of the switch mode power supply converter based on the voltage level of the supply voltage and the maximum voltage level of the modulated power supply voltage;

operating the switch mode power supply converter in the selected bang-bang mode of operation to generate the switching voltage based on the switch mode power supply converter control signal.

61. The method of claim 60 wherein operating the switch mode power supply converter in the selected bang-bang mode of operation to generate the switching voltage based on the switch mode power supply converter control signal comprises:

generating a composite feedback signal with a switcher control circuit of the switch mode power supply converter based on the switch mode power supply converter control signal;

determining whether the composite feedback signal is greater than a bang-bang threshold level;

generating the switching voltage that is greater than the supply voltage at the switching voltage output based on a determination that the composite feedback signal is greater than the bang-bang threshold level.

62. The method of claim 61 wherein operating the switch mode power supply converter in the selected bang-bang mode of operation to generate the switching voltage based on the switch mode power supply converter control signal further comprises:

generating the switching voltage having a voltage level that is between the supply voltage and a ground voltage based on a determination that the composite feedback signal is less than the bang-bang threshold level.

63. The method of claim 62 where generating the switching voltage that is between the supply voltage and the ground voltage based on the determination

that the composite feedback signal is less than the bang-bang threshold level comprises:

generating the switching voltage substantially equal to half the supply voltage.

64. The method of claim 62 where generating the switching voltage that is between the supply voltage and the ground voltage based on the determination that the composite feedback signal is less than the bang-bang threshold level comprises:

generating the switching voltage substantially equal to the supply voltage.

65. The method of claim 63 further comprising:

disabling an offset voltage loop circuit configured to regulate an offset voltage between the modulated power supply output and a parallel amplifier output of the parallel amplifier.

66. The method of claim 63 further comprising:

disabling an active noise reduction circuit.

67. The method of claim 66 wherein disabling the active noise reduction circuit comprises:

disabling an open loop ripple compensation circuit configured to apply a high frequency ripple compensation current to the modulated power supply output.

68. The method of claim 61 wherein operating the switch mode power supply converter in the selected bang-bang mode of operation to generate the switching voltage further comprises:

generating the switching voltage substantially equal to a reference voltage based on a determination that the composite feedback signal is less than the bang-bang threshold level.

69. The method of claim 61 wherein generating the switching voltage that is greater than the supply voltage at the switching voltage output based on the determination that the composite feedback signal is greater than the bang-bang threshold level comprises:

generating the switching voltage substantially equal to three-halves of the supply voltage.

70. The method of claim 61 wherein generating the switching voltage that is greater than the supply voltage at the switching voltage output based on the determination that the composite feedback signal is greater than the bang-bang threshold level comprises:

generating the switching voltage substantially equal to twice the supply voltage.

71. The method of claim 61 wherein generating the composite feedback signal with the switcher control circuit of the switch mode power supply converter based on the switch mode power supply converter control signal further comprises:

generating an offset voltage error signal substantially equal to only a difference between the modulated power supply voltage and a maximum offset voltage error threshold;

generating a threshold offset signal based on the offset voltage error signal to reguate an offset voltage between the modulated power supply output and a parallel amplifier output of the parallel amplifier;

subtacting the threshold offset signal from the switch mode power supply converter control signal to generate a composite feedback signal; and

comparing the composite feedback signal to the bang-bang threshold level to determine whether the composite feedback signal is greater than a bang-bang threshold level.

72. A switch mode power supply converter comprising:

a supply input configured to receive a supply voltage;

a switcher control circuit including a plurality of threshold levels and a plurality of operational states, wherein the plurality of operational states includes a shunt output mode, a series output mode, and one or more boost output modes, and the plurality of threshold levels includes a shunt level threshold, a series level threshold that is greater than the shunt level threshold, and a first boost level threshold that is greater than the series level threshold, and the switcher control circuit configured to:

receive at least one feedback signal from a parallel amplifier circuit;

generate a composite feedback signal based on the at least one feedback signal;

transition to the series output mode based on the composite feedback signal being at least equal to the series level threshold;

transition to the one or more boost output modes based on the composite feedback signal being at least equal to the first boost level threshold; and

transition to the shunt output mode based on the composite feedback signal being less than equal to the shunt level threshold; and

a switching voltage output configured to provide a switching voltage derived from the supply voltage based on each of the plurality of operational states of the switcher control circuit.

73. The switch mode power supply converter of claim 72 wherein the switcher control circuit is further configured to transition directly from the series output mode and the one or more boost output modes to the shunt output mode based on the composite feedback signal being less than equal to the shunt level threshold.

74. The switch mode power supply converter of claim 72 wherein:

the one or more boost output modes include a first boost output mode and a second boost output mode;

the plurality of threshold levels further includes a second boost level threshold that is greater than the first boost level threshold; and

the switcher control circuit is further configured to:

transition to the first boost output mode based on the composite feedback signal being at least equal to the first boost level threshold; and

transition to the second boost output mode based on the composite feedback signal being at least equal to the second boost level threshold.

75. The switch mode power supply converter of claim 74 wherein the switcher control circuit is further configured to transition directly from series output mode, the first boost output mode, and the second boost output mode to the shunt output mode based on the composite feedback signal being less than equal to the shunt level threshold.

76. The switch mode power supply converter of claim 74 wherein the switcher control circuit is further configured to:

transition from the series output mode to the first boost output mode based on the composite feedback signal being at least equal to the first boost level threshold.

77. The switch mode power supply converter of claim 76 wherein the switcher control circuit is further configured to:

transition from the first boost output mode to the second boost output mode based on the composite feedback signal being at least equal to the second boost level threshold.

78. The switch mode power supply converter of claim 77 wherein the switcher control circuit is further configured to:

enable the switcher control circuit to transition to the first boost output mode after the switcher control circuit transitions to the series output mode.

79. The switch mode power supply converter of claim 77 wherein the switcher control circuit is further configured to:

enable the switcher control circuit to transition to the second boost output mode after the switcher control circuit transitions to the first boost output mode.

80. The switch mode power supply converter of claim 79 wherein the switcher control circuit is further configured to:

enable the switcher control circuit to transition to the first boost output mode after the switcher control circuit transitions to the series output mode.

81. The switch mode power supply converter of claim 74 wherein the switcher control circuit is further configured to:

transition from the first boost output mode to the series output mode based on the composite feedback signal being less than least equal to the first boost level threshold.

82. The switch mode power supply converter of claim 81 wherein the switcher control circuit is further configured to:

transition from the second boost output mode to the series output mode based on the composite feedback signal being less than equal to the first boost level threshold.

83. The switch mode power supply converter of claim 82 wherein the switcher control circuit is further configured to:

transition from the series output mode to the shunt output mode based on the composite feedback signal being less than equal to the shunt level threshold.

84. The switch mode power supply converter of claim 74 further comprising a multi-level charge pump including a switching network and only two flying capacitors, and configure to:

generate an output voltage substantially equal to three-halves of a supply voltage in response to the switcher control circuit being in the first output mode;

generate the output voltage substantially equal to twice the supply voltage in response to the switcher control circuit being in the second output mode; and

provide the output voltage to switching voltage output as the switching voltage based on the switcher control circuit being the one or more boost output modes.

85. The switch mode power supply converter of claim 84 wherein:

the plurality of operational states further includes a first output mode, the plurality of threshold levels further includes a first threshold level that is greater than the shunt level threshold but less than the series level threshold, and the switcher control circuit is further configured to:

transition to the first output mode based on the composite feedback signal being less than equal to the series threshold level.

86. A method for controlling a voltage across a coupling device between a parallel amplifier circuit output and a power amplifier supply output in a pseudo-envelope follower power management system comprising:

determining an expected offset voltage between a power amplifier supply voltage and a parallel amplifier output voltage prior to a data transmission based an envelope characteristic of a signal to be transmitted and a supply voltage used to power a parallel amplifier;

setting a target offset voltage based on the expected offset voltage;

regulating an offset voltage between the power amplifier supply voltage and the parallel amplifier output voltage based on the target offset voltage.

87. The method for controlling the voltage across the coupling device between the parallel amplifier circuit output and the power amplifier supply output in a pseudo-envelope follower power management system of claim 86 wherein determining the expected offset voltage between the power amplifier supply voltage and the parallel amplifier output voltage prior to the data transmission

based the envelope characteristic of a signal to be transmitted and the supply voltage used to power a parallel amplifier;

comprises:

determining a peak-to-peak swing of the power amplifier supply voltage based on the envelope characteristic of the signal to be transmitted;

determining the parallel amplifier supply voltage based on the supply voltage and the peak-to-peak swing of the power amplifier supply voltage;

determining the expected offset voltage between the power amplifier supply voltage and the parallel amplifier circuit output voltage based on the parallel amplifier supply voltage, the peak-to-peak swing of the power amplifier supply voltage, and a minimum headroom voltage of a current sourcing transistor of a parallel amplifier output stage of the parallel amplifier.

88. The method for controlling the voltage across the coupling device between the parallel amplifier circuit output and the power amplifier supply output in a pseudo-envelope follower power management system of claim 87 wherein determining the parallel amplifier supply voltage based on the measurement of the supply voltage and the peak-to-peak swing of the power amplifier supply voltage comprises:

determining a minimum parallel amplifier supply voltage based on the peak-to-peak swing of the power amplifier supply voltage, the minimum headroom voltage of the current sourcing transistor, and a minimum headroom voltage of a current sinking transistor of the parallel amplifier output stage;

determining a minimum operational ratio of the charge pump based on the minimum parallel amplifier supply voltage and the supply voltage;

selecting an available operation ratio of the charge pump from among a plurality of available operational ratios of the charge pump that has a smallest value at least equal to the minimum operational ratio of the charge pump as a selected operational ratio of the charge pump.

89. The method for controlling the voltage across the coupling device between the parallel amplifier circuit output and the power amplifier supply output in a pseudo-envelope follower power management system of claim 87 further comprising:

generating a parallel amplifier supply voltage substantially equal to a product of the selected operational ratio of the charge pump and the supply voltage.

90. The method for controlling the voltage across the coupling device between the parallel amplifier circuit output and the power amplifier supply output in a pseudo-envelope follower power management system of claim 89 wherein the supply voltage is substantially equal to a battery voltage.

91. The method for controlling the voltage across the coupling device between the parallel amplifier circuit output and the power amplifier supply output in a pseudo-envelope follower power management system of claim 90 wherein the parallel amplifier circuit is a rechargeable parallel amplifier.

92. The method for controlling the voltage across the coupling device between the parallel amplifier circuit output and the power amplifier supply output in a pseudo-envelope follower power management system of claim 86 wherein regulating the offset voltage between the power amplifier supply voltage and the parallel amplifier output voltage based on the target offset voltage comprises:

generating an offset voltage error signal based on the power amplifier supply voltage less a sum of the target offset voltage and the parallel amplifier circuit output voltage;

generating an offset voltage feedback signal based on the offset voltage error signal; and

providing the offset voltage feedback signal to a switch mode power supply converter to regulate the offset voltage.

93. A pseudo-envelope follower power management system with an open loop parallel amplifier current assist system comprising:

a switch mode power supply converter configured to:

generate a switching voltage at a switching voltage output; and

generate a switching voltage output estimate;

an open loop assist circuit configured to:

receive the switching voltage output estimate and a target voltage for a power amplifier supply voltage;

generate an open loop assist current as a function of the switching voltage output estimate and the target voltage for the power amplifier supply voltage; and

apply the open loop assist current to a power amplifier supply output.

94. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 1 wherein the open loop assist circuit is further configure to:

generate an output current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage, wherein the output current estimate is an estimate of a power amplifier supply current provided to a radio frequency power amplifier;

generate a bypass capacitor current estimate based on the target voltage for the power amplifier supply voltage, wherein the bypass capacitor current estimate is an estimate of a bypass capacitor current provided by a bypass capacitor in communication with the power amplifier supply output;

generate a power inductor current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage, wherein the power inductor current estimate is an estimate of a power inductor current induced in a power inductor by the switching voltage and provided to the power amplifier supply output; and

generate an open loop assist current estimate based on the output current estimate less a sum of the bypass capacitor current estimate and the power inductor current estimate.

95. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 94 wherein the open loop assist circuit includes a controlled current source configured to generate the open loop assist current based on the open loop assist current estimate.

96. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 95 wherein the open loop assist circuit includes:

an output current estimator circuit configured to:

receive the target voltage for the power amplifier supply voltage;

subtract a minimum power amplifier turn on voltage of the radio frequency power amplifier from the target voltage for the power amplifier supply voltage to generate a difference signal; and

scale the difference signal by an estimated power amplifier transconductance of the radio frequency power amplifier to generate the output current estimate.

97. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 96 wherein the open loop assist circuit further includes:

a bypass capacitor current estimator circuit configured to:

differentiate the target voltage for the power amplifier supply voltage to generate a bypass capacitor voltage rate of change signal; and

scale the bypass capacitor voltage rate of change signal by an estimated bypass capacitor capacitance to generate the bypass capacitor current estimate.

98. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 97 wherein the open loop assist circuit further includes a power inductor current estimator circuit configured to generate the power inductor current estimate as a function of an estimated power inductor parameter and an integration of a difference voltage based on a difference between the switching voltage output estimate less the target voltage for the power amplifier supply voltage.

99. A switch mode power supply converter comprising:
a switching voltage output;
a supply input configured to receive a supply voltage; and
a switcher control circuit including:
a first boost mode operation during which the switcher controller configures the charge pump having only two flying capacitors to provide a first boost output voltage greater than the supply voltage as a switching voltage at the switching voltage output;
a second boost mode of operation during which the switcher controller configures a charge pump to provide a second boost output voltage that is greater than the first boost output voltage as the switching voltage at the switching voltage output;
a series output mode of operation during which the switcher controller configures the charge pump to charge the only two flying capacitor and a series switch to provide the switching voltage substantially equal to the supply voltage at the switching voltage output;
a shunt output mode of operation during which the switcher controller configures the charge pump to charge the only two flying capacitor and a shunt switch to provide the switching voltage substantially equal to a reference voltage at the switching voltage output; and

a plurality of threshold levels including a shunt level threshold, a series level threshold which is greater than the shunt level threshold, a first boost level threshold that is greater than the series level threshold, and a second boost level threshold that is greater than the first boost level threshold; and

configured to:

receive at least one feedback signal from a parallel amplifier circuit;

generate a composite feedback signal based on the at least one feedback signal;

detect the composite feedback signal being at least less than equal to a first set of thresholds of the plurality of threshold including the shunt level threshold; and

transition an operational state of the switcher control circuit directly from the first boost output mode and the second boost output mode upon detection that the composite feedback signal is at least less than equal to the shunt level threshold

100. A pseudo-envelope follower power management system with an open loop parallel amplifier current assist system comprising:

a switch mode power supply converter configured to:

generate a switching voltage at a switching voltage output; and

generate a switching voltage output estimate;

an open loop assist circuit configured to:

receive the switching voltage output estimate and a target voltage for a power amplifier supply voltage;

generate an open loop assist current as a function of the switching voltage output estimate and the target voltage for the power amplifier supply voltage; and

apply the open loop assist current to a power amplifier supply output.

101. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 100 wherein the open loop assist circuit is further configured to:

generate an output current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage, wherein the output current estimate is an estimate of a power amplifier supply current provided to a radio frequency power amplifier;

generate a bypass capacitor current estimate based on the target voltage for the power amplifier supply voltage, wherein the bypass capacitor current estimate is an estimate of a bypass capacitor current provided by a bypass capacitor in communication with the power amplifier supply output;

generate a power inductor current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage, wherein the power inductor current estimate is an estimate of a power inductor current induced in a power inductor by the switching voltage and provided to the power amplifier supply output; and

generate an open loop assist current estimate based on the output current estimate less a sum of the bypass capacitor current estimate and the power inductor current estimate.

102. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 101 wherein the open loop assist circuit includes a controlled current source configured to generate the open loop assist current based on the open loop assist current estimate.

103. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 102 wherein the target voltage for the power amplifier supply voltage is a V_{RAMP} signal.

104. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 102 wherein the switching

voltage output estimate is one of a scaled switching voltage and an estimated switching voltage output.

105. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 104 wherein the estimated switching voltage output provides an early indication of a future voltage level of the switching voltage.

106. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 102 wherein the open loop assist circuit includes:

an output current estimator circuit configured to:

receive the target voltage for the power amplifier supply voltage;

subtract a minimum power amplifier turn on voltage of the radio frequency power amplifier from the target voltage for the power amplifier supply voltage to generate a difference signal; and

scale the difference signal by an estimated power amplifier transconductance of the radio frequency power amplifier to generate the output current estimate.

107. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 106 wherein the output current estimator circuit includes:

an operational amplifier including a non-inverting input configured to receive the target voltage for the power amplifier supply voltage, an inverting input configured to receive the minimum power amplifier turn on voltage of the radio frequency power amplifier, and an operational amplifier output configured to generate the difference signal; and

a transconductance amplifier having a transconductance amplifier transconductance substantially equal to the estimated power amplifier transconductance of the radio frequency power amplifier, and configured to:

receive the difference signal; and

scale the difference signal by the transconductance amplifier transconductance to generate the output current estimate.

108. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 106 wherein the target voltage for the power amplifier supply voltage is a V_{RAMP} signal.

109. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 106 wherein the open loop assist circuit further includes:

a bypass capacitor current estimator circuit configured to:

differentiate the target voltage for the power amplifier supply voltage to generate a bypass capacitor voltage rate of change signal; and

scale the bypass capacitor voltage rate of change signal by an estimated bypass capacitor capacitance to generate a bypass capacitor current estimate.

110. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 109 wherein the bypass capacitor current estimator circuit includes:

a high pass filter having a high pass filter corner frequency and configured to:

receive the target voltage for the power amplifier supply voltage; and

high pass filter the target voltage for the power amplifier supply voltage to differentiate the target voltage for the power amplifier supply voltage.

111. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 110 wherein:

the high pass filter include a programmable high pass filter time constant substantially equal to between 8 nanoseconds and 16 nanoseconds; and

the high pass filter is further configured to set the high pass filter corner frequency based on the programmable high pass filter time constant.

112. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 109 wherein the open loop assist circuit further includes a power inductor current estimator circuit configured to generate the power inductor current estimate as a function of an estimated power inductor parameter and an integration of a difference voltage based on a difference between the switching voltage output estimate less the target voltage for the power amplifier supply voltage.

113. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 112 wherein the estimated power inductor parameter is one of a measured inductance of the power inductor between a range of frequencies and an estimated inductance of the power inductor between the range of frequencies.

114. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 113 wherein the range of frequencies is between 10 MHz and 30 MHz.

115. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 112 wherein:

the switching voltage output estimate is an estimated switching voltage output that provides an early indication of a future voltage level of the switching voltage; and

the target voltage for the power amplifier supply voltage is a V_{RAMP} signal.

116. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 115 wherein the power inductor current estimator circuit includes an integrator circuit configured to:

scale the estimated switching voltage output and the V_{RAMP} signal by a reciprocal of the estimated power inductor parameter to generate a scaled switching voltage output estimate and a scaled target voltage for the power amplifier supply voltage;

integrate a difference of the scaled switching voltage output estimate less the scaled target voltage for the power amplifier supply voltage to generate the power inductor current estimate.

117. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 116 wherein the integrator circuit has a bandwidth between 5 MHz and 45 MHz.

118. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 116 wherein the integrator circuit includes a programmable slope.

119. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 115 wherein the power inductor current estimator circuit includes an integrator circuit configured to:

integrate a difference of the estimated switching voltage output less the V_{RAMP} signal to generate an integrated difference; and

scale the integrated difference of the estimated switching voltage output less the V_{RAMP} signal by a reciprocal of the estimated power inductor parameter to generate the power inductor current estimate.

120. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 119 wherein the integrator circuit has a bandwidth between 5 MHz and 45 MHz.

121. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 119 wherein the integrator circuit includes a programmable slope.

122. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 112 further comprising a summing circuit configured to:

receive the output current estimate, the bypass capacitor current estimate, and the power inductor current estimate; and

subtract a sum of the bypass capacitor current estimate and the power inductor current estimate to generate the open loop assist current estimate.

123. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 100 wherein the switch mode power supply converter is a multi-level charge pump buck converter.

124. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 100 wherein the switch mode power supply converter is a buck converter.

125. The pseudo-envelope follower power management system with the open loop parallel amplifier current assist system of claim 100 wherein the open loop assist circuit is further configured to generate the open loop assist current to reduce a parallel amplifier output current generated by a parallel amplifier configured to regulate the power amplifier supply voltage at the power amplifier supply output.

126. A method for providing an open loop parallel amplifier current assist current in a pseudo-envelope follower power management system comprising:

receiving a switching voltage output estimate, wherein the switching voltage output estimate provides an indication of a switching voltage generated by a switch mode power supply converter;

receiving a target voltage for a power amplifier supply voltage;

generating an open loop assist current as a function of the switching voltage output estimate and the target voltage for the power amplifier supply voltage; and

applying the open loop assist current to a power amplifier supply output to reduce a parallel amplifier output current generated by a parallel amplifier configured to regulate the power amplifier supply voltage at the power amplifier supply output.

127. The method for providing the open loop parallel amplifier current assist current in the pseudo-envelope follower power management system of claim 126 wherein generating the open loop assist current as the function of the switching voltage output estimate and the target voltage for the power amplifier supply voltage comprising:

generating an output current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage, wherein the output current estimate is an estimate of a power amplifier supply current provided to a radio frequency power amplifier;

generating a bypass capacitor current estimate based on the target voltage for the power amplifier supply voltage, wherein the bypass capacitor current estimate is an estimate of a bypass capacitor current provided by a bypass capacitor in communication with the power amplifier supply output;

generating a power inductor current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage, wherein the power inductor current estimate is an estimate of a power inductor current induced in a power inductor by the switching voltage and provided to the power amplifier supply output; and

generating the open loop assist current based on the output current estimate less a sum of the bypass capacitor current estimate and the power inductor current estimate.

128. The method for providing the open loop parallel amplifier current assist current in the pseudo-envelope follower power management system of claim 127 wherein generating the power inductor current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage comprises:

generating the power inductor current estimate as a function of an estimated power inductor parameter and an integration of a difference voltage based on a difference of the switching voltage output estimate less the target voltage for the power amplifier supply voltage.

129. The method for providing the open loop parallel amplifier current assist current in the pseudo-envelope follower power management system of claim 128 wherein generating the bypass capacitor current estimate based on the target voltage for the power amplifier supply voltage comprises:

differentiating the target voltage for the power amplifier supply voltage to generate a bypass capacitor voltage rate of change signal; and

scaling the bypass capacitor voltage rate of change signal by an estimated bypass capacitor capacitance to generate the bypass capacitor current estimate.

130. The method for providing the open loop parallel amplifier current assist current in the pseudo-envelope follower power management system of claim 129 wherein generating the output current estimate based on the switching voltage output estimate and the target voltage for the power amplifier supply voltage comprises:

subtracting a minimum power amplifier turn on voltage of the radio frequency power amplifier from the target voltage for the power amplifier supply voltage to generate a difference signal; and

scaling the difference signal by an estimated power amplifier transconductance of the radio frequency power amplifier to generate the output current estimate.

131. The method for providing the open loop parallel amplifier current assist current in the pseudo-envelope follower power management system of claim 130 wherein:

the switching voltage output estimate is an estimated switching voltage output that provides an early indication of a future voltage level of the switching voltage; and

the target voltage for the power amplifier supply voltage is a V_{RAMP} signal.

132. The method for providing the open loop parallel amplifier current assist current in the pseudo-envelope follower power management system of claim 126 wherein the switch mode power supply converter is a multi-level charge pump buck converter.

133. A parallel amplifier output impedance compensation circuit comprising:

a first differentiator circuit configured to:

receive a V_{RAMP} signal; and

generate an estimate of a bypass capacitor current provided by a bypass capacitor coupled between a power amplifier supply output and a reference voltage as a function of the V_{RAMP} signal;

a second differentiator circuit configured to:

receive a dynamic current, wherein the dynamic current is a combination of the estimate of the bypass capacitor current and an estimate of a parallel amplifier output current that is provide by a parallel amplifier to regulate a power amplifier output voltage at the power amplifier supply output; and

generate a power amplifier supply ripple voltage estimate as a function of the dynamic current;

a frequency pre-distortion circuit configured to:

receive the V_{RAMP} signal; and

filter the V_{RAMP} signal to generate a peaked V_{RAMP} signal that compensates for a roll off of a modulation frequency response of the parallel amplifier; and

a summing circuit configured to:

subtract the power amplifier supply ripple voltage estimate from the peaked V_{RAMP} signal to generate a compensated V_{RAMP} signal; and provide the compensated V_{RAMP} signal to the parallel amplifier to regulate the power amplifier output voltage.

134. The parallel amplifier output impedance compensation circuit of claim 133 wherein the second differentiator circuit is configured to:

differentiate the dynamic current to generate a derivative of the dynamic current; and

generate the power amplifier supply ripple voltage estimate based on the derivative of the dynamic current.

135. The parallel amplifier output impedance compensation circuit of claim 134 wherein the second differentiator circuit is further configured to scale the derivative of the dynamic current by a parallel amplifier inductance estimate parameter to generate the power amplifier supply ripple voltage estimate.

136. The parallel amplifier output impedance compensation circuit of claim 135 wherein the parallel amplifier inductance estimate parameter is an estimate of an inductive characteristic of a parallel amplifier output impedance in a range of frequencies near or within an operational bandwidth of a linear radio frequency power amplifier powered by the power amplifier output voltage.

137. The parallel amplifier output impedance compensation circuit of claim 136 wherein the range of frequencies is between 10 MHz and 30 MHz.

138. The parallel amplifier output impedance compensation circuit of claim 135 wherein the second differentiator circuit includes a high pass filter having a high pass time constant for setting a corner frequency of the high pass filter, and configured to high pass filter the dynamic current to generate the derivative of the dynamic current.

139. The parallel amplifier output impedance compensation circuit of claim 138 wherein the high pass time constant of the second differentiator circuit has a range between 8 nanoseconds and 16 nanoseconds.

140. The parallel amplifier output impedance compensation circuit of claim 135 wherein the first differentiator circuit is further configured to:

differentiate the V_{RAMP} signal to generate a derivative of the V_{RAMP} signal; and

generate the estimate of the bypass capacitor current of the bypass capacitor based on the derivative of the V_{RAMP} signal.

141. The parallel amplifier output impedance compensation circuit of claim 140 wherein the first differentiator circuit is further configured to scale the derivative of the V_{RAMP} signal received by an estimated bypass capacitor capacitance parameter to generate the estimate of the bypass capacitor current of the bypass capacitor.

142. The parallel amplifier output impedance compensation circuit of claim 140 wherein the first differentiator circuit includes a high pass filter having a high pass time constant for setting a corner frequency of the high pass filter, and configured to high pass filter the V_{RAMP} signal to generate a derivative of the V_{RAMP} signal.

143. The parallel amplifier output impedance compensation circuit of claim 142 wherein the high pass time constant of the first differentiator circuit has a range between 8 nanoseconds and 16 nanoseconds.

144. The parallel amplifier output impedance compensation circuit of claim 135 wherein the frequency pre-distortion circuit includes a peaking filter configured to equalize a frequency response between a first control input configured to receive the V_{RAMP} signal and the power amplifier supply output.

145. The parallel amplifier output impedance compensation circuit of claim 144 wherein the frequency pre-distortion circuit is configured such that the frequency response between the first control input and the power amplifier supply output is substantially flat up to about 35 MHz.

146. The parallel amplifier output impedance compensation circuit of claim 135 wherein the frequency pre-distortion circuit includes a Laplace transfer function substantially equal to [1+Tau_Zero*s] / [1+Tau_Pole*s], where Tau_Zero is a zero time constant and Tau_Pole is a pole time constant.

147. The parallel amplifier output impedance compensation circuit of claim 146 wherein the zero time constant is substantially equal to about .192 microseconds and the pole time constant is substantially equal to about .4 microseconds.

148. A method for compensation for a non-ideal parallel amplifier output impedance comprising:

receiving a V_{RAMP} signal;

receiving an estimate of a parallel amplifier output current generated by a parallel amplifier configured to regulate a power amplifier supply voltage at a power amplifier supply output;

generating a compensated V_{RAMP} signal based on the V_{RAMP} signal and the estimate of the parallel amplifier output current; and

providing the compensated V_{RAMP} signal to the parallel amplifier.

149. The method for compensation for the non-ideal parallel amplifier output impedance of claim 148 wherein generating the compensated V_{RAMP} signal based on the V_{RAMP} signal and the estimate of the parallel amplifier output current comprises:

generating an estimate of a bypass capacitor current provided by a bypass capacitor coupled between the power amplifier supply output and a reference voltage as a function of the V_{RAMP} signal;

summing the estimate of the bypass capacitor current with the estimate of a parallel amplifier output current to generate a dynamic current; and

generating a power amplifier supply ripple voltage estimate as a function of the dynamic current.

150. The method for compensation for the non-ideal parallel amplifier output impedance of claim 149 wherein generating the power amplifier supply ripple voltage estimate as a function of the dynamic current comprises:

differentiating the dynamic current to generate a derivative of the dynamic current; and

scaling the derivative of the dynamic current by a parallel amplifier inductance estimate parameter to generate the power amplifier supply ripple voltage estimate.

151. The method for compensation for the non-ideal parallel amplifier output impedance of claim 150 wherein the parallel amplifier inductance estimate parameter is an estimate of an inductive characteristic of a parallel amplifier output impedance in a range of frequencies near or within an operational bandwidth of a linear radio frequency power amplifier powered by the power amplifier supply voltage.

152. The method for compensation for the non-ideal parallel amplifier output impedance of claim 151 wherein the range of frequencies is between 10 MHz and 30 MHz.

153. The method for compensation for the non-ideal parallel amplifier output impedance of claim 150 wherein differentiating the dynamic current to generate the derivative of the dynamic current comprises:

high pass filtering the dynamic current with a high pass filter to generate the derivative of the dynamic current.

154. The method for compensation for the non-ideal parallel amplifier output impedance of claim 153 wherein the high pass filter includes a high pass filter time constant having a range between 8 nanoseconds and 16 nanoseconds.

155. The method for compensation for the non-ideal parallel amplifier output impedance of claim 150 wherein generating the estimate of the bypass capacitor current provided by the bypass capacitor coupled between the power amplifier supply output and the reference voltage as the function of the V_{RAMP} signal comprises:

differentiating the V_{RAMP} signal to generate the derivative of the V_{RAMP} signal;

scaling the derivative of the V_{RAMP} signal received by an estimated bypass capacitor capacitance parameter to generate the estimate of the bypass capacitor current of the bypass capacitor.

156. The method for compensation for the non-ideal parallel amplifier output impedance of claim 155 wherein differentiating the V_{RAMP} signal to generate the derivative of the V_{RAMP} signal comprises:

high pass filtering the V_{RAMP} signal with a high pass filter to generate the derivative of the V_{RAMP} signal.

157. The method for compensation for the non-ideal parallel amplifier output impedance of claim 156 wherein the high pass filter includes a high pass filter time constant having a range between 8 nanoseconds and 16 nanoseconds.

158. The method for compensation for the non-ideal parallel amplifier output impedance of claim 155 wherein generating the compensated V_{RAMP} signal based on the V_{RAMP} signal and the estimate of the parallel amplifier output current further comprises:

filtering the V_{RAMP} signal with a filter to generate a peaked V_{RAMP} signal to compensate for a roll off of a modulation frequency response of the parallel amplifier; and

subtracting the power amplifier supply ripple voltage estimate from the peaked V_{RAMP} signal to generate a compensated V_{RAMP} signal.

159. The method for compensation for the non-ideal parallel amplifier output impedance of claim 158 wherein the filter includes a zero time constant substantially equal to about .192 microseconds and a pole time constant substantially equal to about .4 microseconds.

160. The method for compensation for the non-ideal parallel amplifier output impedance of claim 158 wherein filtering the V_{RAMP} signal to generate the peaked V_{RAMP} signal to compensate for the roll off of the modulation frequency response of the parallel amplifier comprises:

configuring a frequency response of the filter to equalize a frequency response between a first control input configured to receive the V_{RAMP} signal and the power amplifier supply output.

161. The method for compensation for the non-ideal parallel amplifier output impedance of claim 160 wherein configuring the frequency response of the filter to equalize the frequency response between the first control input configured to receive the V_{RAMP} signal and the power amplifier supply output comprises:

configuring the frequency response of the filter such that the frequency response between the first control input and the power amplifier supply output is substantially flat up to about 35 MHz.

162. An offset voltage control circuit for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output comprising:

a summing circuit configured to:

receive a power amplifier supply voltage provided to a linear radio frequency power amplifier, a parallel amplifier circuit output voltage generated by a parallel amplifier circuit to regulate the power amplifier supply voltage, and an offset voltage target signal; and

subtract a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal; and

an integrator circuit configured to:

integrate the offset voltage error signal to generate an offset voltage feedback signal; and

provide the offset voltage feedback signal to a switcher control circuit of a switch mode power supply converter to regulate a difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage.

163. The offset voltage control circuit of claim 162 wherein the offset voltage target signal is substantially equal to a target offset voltage parameter.

164. The offset voltage control circuit of claim 162 wherein the integrator circuit is an integrator with zero compensation.

165. The offset voltage control circuit of claim 164 wherein a bandwidth of the integrator with zero compensation is based on a first time constant and a second time constant.

166. The offset voltage control circuit of claim 165 wherein the integrator with zero compensation has a Laplace transfer function including $(1 + Tau_1 \times s) / (Tau_2 \times s)$, wherein Tau_1 is the first time constant and Tau_2 is the second time constant.

167. The offset voltage control circuit of claim 166 further comprising a local parameter storage circuit configured to store a first normal operation time constant and a second normal operation time constant.

168. The offset voltage control circuit of claim 167 further comprising:

a pre-charge time configured to generate a timer event after a predetermined time period;

a control circuit configured to:

determine prior to commencement of a transmission slot whether to configure the bandwidth of the integrator with zero compensation to be one of a pre-charge bandwidth for the predetermined time period and a normal operation bandwidth based on a magnitude of the offset voltage error signal, wherein the pre-charge bandwidth is greater than the normal operation bandwidth; and

in response to a determination prior to commencement of the transmission slot to configure the bandwidth of the integrator with zero compensation to be the pre-charge bandwidth for the predetermined time period:

set the first time constant equal to a first pre-charge time constant and the second time constant equal to a second pre-charge time constant to configure the bandwidth of the integrator with zero compensation to be the pre-charge bandwidth; and

enable the pre-charge time configured to generate the timer event after the predetermined time period; and

wherein the integrator with zero compensation is further configured to use the first normal operation time constant from the local parameter storage circuit as the first time constant and the second normal operation time constant from the local parameter storage circuit as the second time constant in response to the timer event.

169. The offset voltage control circuit of claim 168 wherein:

in response to a determination prior to commencement of the transmission slot, the control circuit is further configured to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth, configure the integrator with zero compensation to use the first normal operation time constant from the local parameter storage circuit as the first time constant and the second normal operation time constant from the local parameter storage circuit as the second time constant.

170. The offset voltage control circuit of claim 162 further comprising:

an offset target signal selection circuit configured to provide the offset voltage target signal based on one of a target offset voltage parameter, a V_{RAMP} signal, and a pre-filtered V_{RAMP} signal.

171. The offset voltage control circuit of claim 164 wherein:

the switcher control circuit includes a plurality of comparators, the switcher control circuit configured to:

generate a first composite feedback signal based on the offset voltage feedback signal;

generate a second composite feedback signal without the offset voltage feedback signal;

provide the first composite feedback signal to less than all of the plurality of comparators;

provide the second composite feedback signal to at least one of the plurality of comparators; and

control generation of a switching voltage by the switch mode power supply converter based on outputs generated by the plurality of comparators.

172. The offset voltage control circuit of claim 171 wherein the switch mode power supply converter is a multi-level charge pump buck converter.

173. A method for regulating a voltage across a coupling circuit between a power amplifier supply output and a parallel amplifier circuit output comprising:

receiving a power amplifier supply voltage provided to a linear radio frequency power amplifier, a parallel amplifier circuit output voltage generated by a parallel amplifier circuit to regulate the power amplifier supply voltage, and an offset voltage target signal;

subtracting a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal;

integrating the offset voltage error signal to generate an offset voltage feedback signal; and

providing the offset voltage feedback signal to a switch mode power supply converter to regulate a difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage.

174. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 173 wherein receiving the offset voltage target signal comprises providing the offset voltage target signal based on a target offset voltage parameter.

175. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim

173 wherein integrating the offset voltage error signal to generate the offset voltage feedback signal comprises:

integrating the offset voltage error signal with an integrator with zero compensation to generate the offset voltage feedback signal.

176. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 175 wherein integrating the offset voltage error signal with the integrator with zero compensation to generate the offset voltage feedback signal comprises:

controlling a bandwidth of the integrator with zero compensation based on a first time constant and a second time constant.

177. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 176 wherein controlling the bandwidth of the integrator with zero compensation based on the first time constant and the second time constant comprises:

determining prior to commencement of a data transmission whether to configure the bandwidth of the integrator with zero compensation to be one of a pre-charge operation bandwidth for a predetermined time period and a normal operation bandwidth based on a magnitude of the offset voltage error signal, wherein the pre-charge operation bandwidth is greater than the normal operation bandwidth; and

in response to a determination prior to commencement of the data transmission to configure the bandwidth of the integrator with zero compensation to be the pre-charge operation bandwidth for the predetermined time period:

setting the first time constant equal to a first pre-charge operation time constant and the second time constant equal to a second pre-charge operation time constant to configure the bandwidth of the integrator with zero compensation to be the pre-charge operation bandwidth; and

after the predetermined time period, setting the first time constant equal to a first normal operation time constant and the second time

constant equal to a second normal operation time constant to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth.

178. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 177 wherein controlling the bandwidth of the integrator with zero compensation based on the first time constant and the second time constant further comprises:

in response to a determination prior to commencement of the data transmission to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth, setting the first time constant equal to the first normal operation time constant and the second time constant equal to the second normal operation time constant to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth.

179. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 173 wherein receiving the offset voltage target signal comprises:

providing the offset voltage target signal based on one of an offset voltage target parameter, a V_{RAMP} signal, and a pre-filtered V_{RAMP} signal.

180. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 173 wherein providing the offset voltage feedback signal to the switch mode power supply converter to regulate the difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage comprises:

providing a composite feedback signal based on the offset voltage feedback signal to less than all of a plurality of comparators of a switcher control circuit of the switch mode power supply converter; and

determining an operational state of the switcher control circuit based on outputs generated by all of the plurality of comparators.

181. An offset voltage control circuit to regulate an offset voltage comprising:

a summing circuit configured to:

receive a power amplifier supply voltage from a power amplifier supply output, a parallel amplifier circuit output voltage from a parallel amplifier circuit output of a parallel amplifier circuit, and an offset voltage target signal; and

subtract a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal; and

an error gain circuit configured to:

receive the offset voltage error signal;

scale the offset voltage error signal by an error gain value to generate an offset voltage feedback signal; and

provide the offset voltage feedback signal to a switcher control circuit of a switch mode power supply converter to regulate a difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage.

182. The offset voltage control circuit to regulate the offset voltage of claim 181 wherein the error gain value is configured based on an operational mode of a linear radio frequency power amplifier.

183. The offset voltage control circuit to regulate the offset voltage of claim 182 wherein the offset voltage target signal is substantially equal to an offset voltage target parameter.

184. The offset voltage control circuit to regulate the offset voltage of claim 183 wherein the switcher control circuit includes a plurality of comparators used to control generation of a switching voltage by the switch mode power supply converter, and the switcher control circuit is configured to provide a composite

feedback signal based on the offset voltage feedback signal to less than all of the plurality of comparators.

185. The offset voltage control circuit to regulate the offset voltage of claim 184 wherein the switch mode power supply converter is a multi-level charge pump buck converter.

186. The offset voltage control circuit to regulate the offset voltage of claim 183 further comprising a control circuit configured to determine prior to commencement of a data transmission whether to pre-charge a coupling device between a parallel amplifier circuit output and the power amplifier supply output based on the offset voltage error signal; and

wherein:

in response to a determination to pre-charge the coupling device prior to commencement of the data transmission, the error gain circuit is configured to:

use a pre-charge error gain value as the error gain value for a predetermined time period; and

use a normal error gain value as the error gain value after the predetermined time period, wherein the pre-charge error gain value is greater than the normal error gain value.

187. The offset voltage control circuit to regulate the offset voltage of claim 181 further comprising:

an offset target signal selection circuit configured to provide one of an offset voltage target parameter, a V_{RAMP} signal, and a pre-filtered V_{RAMP} signal as the offset voltage target signal.

188. A method for controlling an offset voltage in a pseudo-envelope follower power management system comprising:

receiving a power amplifier supply voltage from a power amplifier supply output, a parallel amplifier circuit output voltage from a parallel amplifier output of a parallel amplifier circuit, and an offset voltage target signal; and

subtracting a sum of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal;

scaling the offset voltage error signal by an error gain value to generate an offset voltage feedback signal; and

providing the offset voltage feedback signal to a switcher control circuit of a switch mode power supply converter to regulate a difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage.

189. The method for controlling the offset voltage in the pseudo-envelope follower power management system of claim 188 further comprising:

selecting the error gain value based on an operational mode of a linear radio frequency power amplifier.

190. The method for controlling the offset voltage in the pseudo-envelope follower power management system of claim 189 further comprising:

providing the offset voltage target signal based on an offset voltage target parameter.

191. The method for controlling the offset voltage in the pseudo-envelope follower power management system of claim 190 further comprising:

generating a first composite feedback signal based on the offset voltage feedback signal;

generating a second composite feedback signal without the offset voltage feedback signal;

providing the first composite feedback signal to less than all of a plurality of comparators of the switcher control circuit to generate comparator outputs for the less than all of the plurality of comparators; and

providing the second composite feedback signal to at least one of the plurality of comparators of the switcher control circuit to generate a comparator output for the at least one of the plurality of comparators.

192. The method for controlling the offset voltage in the pseudo-envelope follower power management system of claim 191 wherein the switch mode power supply converter is a multi-level charge pump buck converter.

193. The method for controlling the offset voltage in the pseudo-envelope follower power management system of claim 190 further comprising:

determining prior to commencement of a data transmission whether to pre-charge a coupling device between the parallel amplifier output and the power amplifier supply output based on the offset voltage error signal;

in response to a determination to pre-charge the coupling device prior to commencement of the data transmission:

using a pre-charge error gain value as the error gain value for a predetermined time period; and

after the predetermined time period, using a normal error gain value as the error gain value, wherein the pre-charge error gain value is greater than the normal error gain value.

194. The method for controlling the offset voltage in the pseudo-envelope follower power management system of claim 188 further comprising:

selecting the offset voltage target signal from one of an offset voltage target parameter, a V_{RAMP} signal, and a pre-filtered V_{RAMP} signal.

195. An offset voltage control circuit of a pseudo-envelope follower power management system having automatic pre-charging comprising:

a summing circuit configured to generate an offset voltage error signal based on an offset voltage between a power amplifier supply voltage and a parallel amplifier output voltage and a target offset voltage;

an integrator having a plurality of modes of operation including a normal mode of operation and a pre-charge mode of operation, and configured to:

generate an offset voltage feedback signal based on the offset voltage error signal and one of the plurality of modes of operation; and

provide the offset voltage feedback signal to a switch mode power supply converter to regulate the offset voltage; and

a control circuit configured to:

determine prior to commencement of a transmission slot whether to set the integrator to operate in one of the pre-charge mode of operation and the normal mode of operation for a predetermined time period based on a magnitude of the offset voltage error signal; and

based on a determination to set the integrator to operate in the pre-charge mode of operation, configure the integrator to operate in the pre-charge mode of operation for the predetermined time period.

196. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 195 further comprising a pre-charge time configured to generate a timer event after the predetermined time period; and

wherein:

the integrator is further configured to transition from the pre-charge mode of operation to the normal mode of operation in response to the timer event; and

the control circuit is further configured to enable a pre-charge timer to generate the timer event after the predetermined time period.

197. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 196 wherein the integrator includes a first time constant and a second time constant and the integrator is further configured to integrate the offset voltage error signal as a function of the first time constant and the second time constant to generate the offset voltage feedback signal.

198. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 197 further comprising a parameter storage circuit configured to store a first startup time constant, a second startup time constant, a first normal operational time constant, and a second normal operational time constant; and wherein:

the integrator is further configured to:

in the pre-charge mode of operation, use the first startup time constant stored in the parameter storage circuit as the first time constant and the second startup time constant stored in the parameter storage circuit as the second time constant; and

in the normal mode of operation, use the first normal operational time constant stored in the parameter storage circuit as the first time constant and the second normal operational time constant stored in the parameter storage circuit as the second time constant.

199. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 198 wherein the control circuit is further configured to:

monitor a control signal provided to a parallel amplifier to regulate the power amplifier supply voltage; and

set the integrator to operate in the pre-charge mode of operation based on a lack of modulation on the control signal provided to the parallel amplifier.

200. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 199 wherein the control signal is based on a V_{RAMP} signal.

201. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 200 wherein the integrator has a Laplace transfer function including $(1 + Tau_1 \times s) / (Tau_2 \times s)$, wherein Tau_1 is the first time constant and Tau_2 is the second time constant.

202. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 195 wherein the integrator is further configured to:

generate the offset voltage feedback signal as a function of a pre-charge loop bandwidth in the pre-charge mode of operation; and

generate the offset voltage feedback signal as a function of a normal operational loop bandwidth in the pre-charge mode of operation.

203. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 202 wherein the pre-charge loop bandwidth is greater than the normal operational loop bandwidth.

204. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 203 wherein the pre-charge loop bandwidth is between three and seven times, inclusive, greater than the normal operational loop bandwidth.

205. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 204 wherein the pre-charge loop bandwidth is about five times greater than the normal operational loop bandwidth.

206. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 195 wherein the control circuit is further configured to set the integrator to operate in the normal mode of operation prior to commencement of the transmission slot based on the magnitude of the offset voltage error signal.

207. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 195 wherein the control circuit is configured to:

monitor a control signal provided to a parallel amplifier to regulate the power amplifier supply voltage; and

set the integrator to operate in the pre-charge mode of operation based on a lack of modulation on the control signal provided to the parallel amplifier.

208. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 207 wherein the control circuit is further configured to set the integrator to operate in the normal mode of operation prior to commencement of the transmission slot based on the magnitude of the offset voltage error signal.

209. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 207 wherein the control signal is based on a V_{RAMP} signal.

210. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 195 wherein the control circuit is a processor.

211. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 195 wherein the offset voltage is across a coupling device having a first node in communication with a power amplifier supply output and a second node in communication with the parallel amplifier.

212. The offset voltage control circuit of the pseudo-envelope follower power management system of claim 195 wherein the integrator is an integrator with a zero compensation circuit.

213. A method for pre-charging a coupling circuit between a power amplifier supply output and a parallel amplifier circuit output of a pseudo-envelope follower power management system comprising:

determining prior to initiation of a transmission of data whether to operate an offset voltage loop circuit in one of a normal mode of operation and a pre-charge mode of operation based on an offset voltage and a target offset voltage;

in response to a determination to operate the offset voltage loop circuit in the pre-charge mode of operation, configuring a bandwidth of the offset voltage loop circuit to have a pre-charge operational bandwidth for a predetermined time period; and

generating an offset voltage feedback signal with the offset voltage loop circuit based on a difference between the offset voltage and the target offset voltage to regulate the offset voltage.

214. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 213 further comprising:

in response to a determination to operate the offset voltage loop circuit in the normal mode of operation, configuring the bandwidth of the offset voltage loop circuit to have a normal operational bandwidth, wherein the normal operational bandwidth is less than the pre-charge operational bandwidth.

215. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 213 further comprising:

monitoring a V_{RAMP} signal to detect a lack of modulation; and

in response to detection of the lack of modulation on the V_{RAMP} signal, configuring the bandwidth of the offset voltage loop circuit to have the pre-charge operational bandwidth.

216. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 213 wherein configuring the bandwidth of the offset voltage loop circuit to have the pre-charge operational bandwidth for a predetermined time period comprises:

configuring an integrator of the offset voltage loop circuit to operate with a pre-charge time constant to integrate the difference between the offset voltage and the target offset voltage; and

after the predetermined time period, configuring the integrator to operate with a normal operational time constant to integrate the difference between the offset voltage and the target offset voltage.

217. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 216 wherein after the predetermined time period, configuring the integrator to operate with the normal operational time constant comprises:

generating a timer event after the predetermined time period in response to the determination to operate the offset voltage loop circuit in the pre-charge mode of operation; and

in response to the timer event, configuring the integrator to operate with the normal operational time constant.

218. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 216 wherein configuring in response to a determination to operate the offset voltage loop circuit in the normal mode of operation, comprises configuring the integrator of the offset voltage loop circuit to operate with the normal operational time constant such that the bandwidth of the offset voltage loop circuit is set to a normal operational bandwidth, wherein the normal operational bandwidth is less than the pre-charge operational bandwidth.

219. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 213 wherein configuring

the bandwidth of the offset voltage loop circuit to have the pre-charge operational bandwidth for a predetermined time period comprises:

configuring an integrator with a zero compensation circuit of the offset voltage loop circuit to operate with a first pre-charge time constant and a second pre-charge time constant from a local parameter storage circuit of the offset voltage loop circuit;

generate a timer event after the predetermined time period of configuring the integrator with the zero compensation circuit of the offset voltage loop circuit to operate with the first pre-charge time constant and the second pre-charge time constant; and

in response to the timer event, automatically configuring the integrator with the zero compensation circuit of the offset voltage loop circuit to operate with a first normal operational constant and a second normal operational time constant from the local parameter storage circuit.

220. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 219 wherein in response to a determination to operate the offset voltage loop circuit in the normal mode of operation, configuring the integrator with the zero compensation circuit to operate with the first normal operational constant and the second normal operational time constant from the local parameter storage circuit such that the bandwidth of the offset voltage loop circuit has a normal operational bandwidth, wherein the normal operational bandwidth is less than the pre-charge operational bandwidth.

221. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 220 wherein generating the offset voltage feedback signal with the offset voltage loop circuit based on the difference between the offset voltage and the target offset voltage to regulate the offset voltage comprises:

integrating the difference between the offset voltage and the target offset voltage to generate the offset voltage feedback signal.

222. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 213 further comprising providing the offset voltage feedback signal to a switch mode power supply configured to regulate the offset voltage.

223. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 222 wherein providing the offset voltage feedback signal to the switch mode power supply configured to regulate the offset voltage comprises:

generating a first composite feedback signal based on the offset voltage feedback signal;

generating a second composite feedback signal without the offset voltage feedback signal; and

generating a switching voltage of the switch mode power supply based on the first composite feedback signal and the second composite feedback signal.

224. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 223 wherein generating the switching voltage of the switch mode power supply based on the first composite feedback signal and the second composite feedback signal comprises:

providing the first composite feedback signal to at least one of a plurality of comparators of the switch mode power supply; and

providing the second composite feedback signal to at least one of the plurality of comparators of the switch mode power supply; and

generating the switching voltage based on outputs of the plurality of comparators.

225. A method for pre-charging a coupling circuit between a power amplifier supply output and a parallel amplifier circuit output of a pseudo-envelope follower power management system comprising:

receiving a parallel amplifier output voltage and a power amplifier supply voltage;

determining whether to pre-charge a coupling device prior to a data transmission based on an offset voltage substantially equal to a difference between the parallel amplifier output voltage and the power amplifier supply voltage;

generating an offset voltage signal substantially equal to the offset voltage less a target offset voltage;

in response to a determination to pre-charge the coupling device prior to the data transmission:

integrating an offset voltage error signal based on a pre-charge time constant to generate an offset voltage feedback signal; and

after a predetermined time period, integrating the offset voltage error signal based on a normal operational time constant to generate the offset voltage feedback signal; and

providing the offset voltage feedback signal to a switch mode power supply to regulate the offset voltage.

226. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 225, wherein integrating the offset voltage error signal based on the pre-charge time constant to generate the offset voltage feedback signal comprises configuring an integrator to have a pre-charge bandwidth.

227. The method for pre-charging the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of the pseudo-envelope follower power management system of claim 226, wherein integrating the offset voltage error signal based on the normal operational time constant to generate the offset voltage feedback signal comprises configuring the integrator to have a normal operational bandwidth that is less than the pre-charge bandwidth.

228. A feedback delay compensation system for a pseudo-envelope follower power management system comprising:

a feedback delay compensation circuit configured to:

generate an early indication of a change of a target voltage for a power amplifier supply voltage at a power amplifier supply output based on a V_{RAMP} signal; and

a switcher control circuit of a switch mode power supply converter configured to:

receive the early indication of the change of the target voltage for the power amplifier supply voltage from the feedback delay compensation circuit; and

govern generation of a switching voltage at a switching voltage output by the switch mode power supply converter as a function of the early indication of the change of the target voltage for the power amplifier supply voltage.

229. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 228 wherein the feedback delay compensation circuit is configured to:

generate a feedback delay compensation signal based on a derivative of the V_{RAMP} signal; and

provide the feedback delay compensation signal to the switch mode power supply converter as the early indication of the change of the target voltage for the power amplifier supply voltage.

230. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 229 wherein the V_{RAMP} signal is a differential V_{RAMP} signal and the derivative of the V_{RAMP} signal is a derivative of the differential V_{RAMP} signal.

231. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 230 wherein the feedback delay compensation circuit includes a differential high pass filter configured to high pass filter the differential V_{RAMP} signal to generate the derivative of the differential V_{RAMP} signal.

232. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 231 further comprising:

a differential transconductance circuit including a transconductance, the differential transconductance circuit configured to:

receive the derivative of the differential V_{RAMP} signal; and

generate the feedback delay compensation signal based on the derivative of the differential V_{RAMP} signal and the transconductance of the differential transconductance circuit.

233. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 232 wherein the transconductance of the differential transconductance circuit is programmable.

234. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 233 wherein the transconductance

of the differential transconductance circuit has a range between .7 Amps/Volt and 1.3 Amps/Volt.

235. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 231 wherein the differential high pass filter includes a programmable high pass time constant.

236. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 235 wherein an apparent gain of the feedback delay compensation circuit is a function of the programmable high pass time constant.

237. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 236 wherein the feedback delay compensation circuit is configured to adjust the apparent gain based on a band of operation of a communication device.

238. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 235 wherein the feedback delay compensation circuit includes a first programmable binary weighted capacitor having a first programmable capacitance and a second programmable binary weighted capacitor having a second programmable capacitance, and the feedback delay compensation circuit is configured to adjust the programmable high pass time constant of the differential high pass filter as a function of the first programmable capacitance and the second programmable capacitance.

239. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 229 wherein the switcher control circuit is further configured to:

receive a parallel amplifier circuit output current estimate from a parallel amplifier circuit;

generate a composite feedback signal based on a combination of the parallel amplifier circuit output current estimate and the feedback delay compensation signal;

compare the composite feedback signal to a plurality of threshold levels to determine a plurality of comparison outputs;

govern the switch mode power supply converter to generate the switching voltage based on the plurality of comparison outputs of the switcher control circuit.

240. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 239 wherein the parallel amplifier circuit output current estimate is based on a parallel amplifier output current applied to the power amplifier supply output.

241. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 239 wherein the parallel amplifier output current includes a parallel amplifier output current generated by a parallel amplifier configured to regulate the power amplifier supply voltage.

242. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 241 wherein the parallel amplifier output current further includes a high frequency ripple compensation current generated by an open loop compensation assist circuit.

243. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 242 wherein the switcher control circuit is further configured to:

receive a threshold offset signal generated by a V_{OFFSET} loop circuit of the parallel amplifier circuit to regulate an offset voltage between a parallel amplifier circuit output of the parallel amplifier circuit and the power amplifier supply output; and

subtract the threshold offset signal from the combination of the parallel amplifier circuit output current estimate and the feedback delay compensation signal to generate the composite feedback signal.

244. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 239, wherein the switch mode power supply converter is a buck converter.

245. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 243 wherein the plurality of threshold levels includes a shunt level threshold, a series level threshold, a first boost level threshold, and a second boost level threshold.

246. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 239 wherein the switch mode power supply converter is a multi-level charge pump buck converter configured to provide at least one boost voltage as the switching voltage at the switching voltage output.

247. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 229 wherein the switcher control circuit further includes a plurality of comparators including a first set of comparators and a second set of comparators; wherein:

the first set of comparators are configured to:

receive a first set of threshold levels;

receive a first composite feedback signal; and

generate a first set of comparator outputs based on the first set of threshold levels and the first composite feedback signal;

the second set of comparators are configured to:

receive a second set of threshold levels;

receive a second composite feedback signal; and

generate a second set of comparator outputs based on the second set of threshold levels and the second composite feedback signal; and the switcher control circuit is further configured to:

receive a parallel amplifier circuit output current feedback signal from a parallel amplifier circuit;

provide the first composite feedback signal based on a combination of the parallel amplifier circuit output current feedback signal and the feedback delay compensation signal to the first set of comparators;

provide the second composite feedback signal based on the parallel amplifier circuit output current feedback signal to the second set of comparators to generate the second set of comparator outputs to the second set of comparators; and

govern the switch mode power supply converter to generate the switching voltage based the first set of comparator outputs and the second set of comparator outputs.

248. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 247 wherein the parallel amplifier circuit output current feedback signal is based on a parallel amplifier output current generated by a parallel amplifier of the parallel amplifier circuit, a high frequency ripple compensation current generated by an open loop high frequency ripple compensation assist circuit of the parallel amplifier circuit, and/or a combination thereof.

249. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 248 wherein the switcher control circuit is further configured to:

receive a threshold offset signal generated by a V_{OFFSET} loop circuit of the parallel amplifier circuit to regulate an offset voltage between a parallel amplifier circuit output of the parallel amplifier circuit and the power amplifier supply output;

subtract the threshold offset signal from the combination of the parallel amplifier circuit output current feedback signal and the feedback delay compensation signal to generate the first composite feedback signal; and

subtract the threshold offset signal from the parallel amplifier circuit output current feedback signal to generate the second composite feedback signal.

250. The feedback delay compensation system for the pseudo-envelope follower power management system of claim 228 wherein the feedback delay compensation circuit is part of the switch mode power supply converter.

251. A method for compensating for feedback delay in a pseudo-envelope follower power management system comprising:

generating an early indication of a change of a target voltage for a power amplifier supply voltage at a power amplifier supply output based on a V_{RAMP} signal; and

generating a switching voltage with a switch mode power supply converter;

governing generation of the switching voltage by the switch mode power supply converter based on the early indication of the change of the target voltage for the power amplifier supply voltage.

252. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 251 wherein generating the early indication of the change of the target voltage for the power amplifier supply voltage at the power amplifier supply output based on the V_{RAMP} signal comprises:

generating a feedback delay compensation signal based on a derivative of a differential V_{RAMP} signal.

253. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 252 wherein generating the

feedback delay compensation signal based on the derivative of the differential V_{RAMP} signal comprises:

high pass filtering the differential V_{RAMP} signal to generate a high pass filtered differential V_{RAMP} signal; and

generating the feedback delay compensation signal based on the high pass filtered differential V_{RAMP} signal.

254. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 253 wherein generating the feedback delay compensation signal based on the high pass filtered differential V_{RAMP} signal comprises:

receiving the high pass filtered differential V_{RAMP} signal at a differential transconductance circuit; and

generating the feedback delay compensation signal based on the high pass filtered differential V_{RAMP} signal and a transconductance of the differential transconductance circuit.

255. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 253 further comprising:

adjusting a corner frequency of a differential high pass filter to control a magnitude of the feedback delay compensation signal.

256. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 253, wherein generating the feedback delay compensation signal based on the derivative of the differential V_{RAMP} signal further comprises:

adjusting a corner frequency of a differential high pass filter to maximize power efficiency of a parallel amplifier as based on a band of operation of a communication device.

257. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 256, wherein the parallel amplifier is configured to regulate the power amplifier supply voltage provided to a linear radio frequency power amplifier of the communication device.

258. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 253 wherein governing the generation of the switching voltage by the switch mode power supply converter further comprises:

receiving at least one of a parallel amplifier circuit output current feedback signal and an offset voltage control signal from a parallel amplifier circuit;

combining the at least one of the parallel amplifier circuit output current feedback signal and the offset voltage control signal with the feedback delay compensation signal to generate a composite feedback signal; and

controlling the generation of the switching voltage by the switch mode power supply converter based on the composite feedback signal.

259. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 258 wherein the switch mode power supply converter is one of a multi-level charge pump buck converter and a buck converter.

260. The method for compensating for feedback delay in the pseudo-envelope follower power management system of claim 251 wherein the switch mode power supply converter is one of a multi-level charge pump buck converter and a buck converter.

261. A parallel amplifier output impedance compensation system for a pseudo-envelope follower power management system comprising:

a switch mode power supply converter configured to:

generate a switching output voltage at a switching voltage output; and

generate an estimated switching voltage signal; and

a parallel amplifier output impedance compensation circuit in communication with the switch mode power supply converter, and configured to:

receive a V_{RAMP} signal and the estimated switching voltage signal;

generate a high frequency ripple compensation signal based on a difference between the V_{RAMP} signal and the estimated switching voltage signal;

generate a compensated V_{RAMP} signal based on the V_{RAMP} signal and the high frequency ripple compensation signal; and

provide the compensated V_{RAMP} signal to a parallel amplifier in order to regulate a power amplifier supply voltage at a power amplifier supply output.

262. The parallel amplifier output impedance compensation system of claim 261 wherein the parallel amplifier output impedance compensation circuit includes a subtraction circuit configured to generate an expected difference signal based on the V_{RAMP} signal and the estimated switching voltage signal.

263. The parallel amplifier output impedance compensation system of claim 262 wherein the switch mode power supply converter includes a programmable delay circuit configured to delay generation of the estimated switching voltage signal by an alignment period to temporally align the estimated switching voltage signal with the V_{RAMP} signal.

264. The parallel amplifier output impedance compensation system of claim 263 wherein the alignment period is set to minimize a peak-to-peak ripple voltage on the power amplifier supply voltage.

265. The parallel amplifier output impedance compensation system of claim 264 wherein the parallel amplifier output impedance compensation circuit further includes:

a high pass filter configured to:

receive the expected difference signal; and

high pass filter the expected difference signal to generate an estimated high frequency ripple signal; and

a scaling circuit in communication with the high pass filter, and configured to:

receive a scaling factor and the estimated high frequency ripple signal; and

scale the estimated high frequency ripple signal based on the scaling factor to generate the high frequency ripple compensation signal.

266. The parallel amplifier output impedance compensation system of claim 265 wherein the parallel amplifier output impedance compensation circuit further includes a scaling function circuit configured to generate the scaling factor based on a band of operation of a communication network.

267. The parallel amplifier output impedance compensation system of claim 265 wherein the parallel amplifier output impedance compensation circuit further includes a scaling function circuit configured to:

receive a scaled parallel amplifier output current from the parallel amplifier; and

generate the scaling factor to the scaling circuit based on the scaled parallel amplifier output current.

268. The parallel amplifier output impedance compensation system of claim 267 wherein the scaling function circuit is further configured to:

select a coefficient of a scaling function based on a band of operation of a communication network; and

generate the scaling factor with the scaling function based on the scaled parallel amplifier output current.

269. The parallel amplifier output impedance compensation system of claim 268 wherein the scaled parallel amplifier output current is fractionally related to a parallel amplifier output current applied to the power amplifier supply output by the parallel amplifier to regulate the power amplifier supply voltage.

270. The parallel amplifier output impedance compensation system of claim 267 wherein the scaling function circuit is further configured to select the scaling factor based on an estimate of an inductive characteristic of a parallel amplifier output impedance between frequencies of 10 MHz and 30 MHz.

271. The parallel amplifier output impedance compensation system of claim 265 wherein the parallel amplifier output impedance compensation circuit further includes a tune circuit configured to provide the scaling factor to the scaling circuit based on an operational mode of a linear radio frequency power amplifier.

272. The parallel amplifier output impedance compensation system of claim 271 wherein the tune circuit is further configured to dynamically provide the scaling factor to the scaling circuit on a block-by-block transmission basis.

273. The parallel amplifier output impedance compensation system of claim 265 wherein the parallel amplifier output impedance compensation circuit is configured to provide the scaling factor to the scaling circuit based on a band of operation of a communication network.

274. The parallel amplifier output impedance compensation system of claim 265 wherein the parallel amplifier output impedance compensation circuit further includes:

a pre-distortion filter circuit configured to pre-distort the V_{RAMP} signal to generate a pre-filtered V_{RAMP} signal based on a wideband modulation associated with a mode of operation of a communication device;

a summing circuit in communication with the pre-distortion filter circuit, and configured to combine the high frequency ripple compensation signal with the pre-filtered V_{RAMP} signal to generate the compensated V_{RAMP} signal.

275. The parallel amplifier output impedance compensation system of claim 274 wherein the pre-distortion filter circuit includes a pre-distortion frequency response, and is further configured to:

filter the V_{RAMP} signal to generate the pre-filtered V_{RAMP} signal based on the frequency response to substantially compensate for a parallel amplifier frequency response of the parallel amplifier.

276. The parallel amplifier output impedance compensation system of claim 275 wherein the frequency response of the pre-distortion filter circuit is further configured to provide frequency peaking to compensate for a power amplifier associated inductance, a power amplifier filter associated capacitance, and/or a combination thereof.

277. The parallel amplifier output impedance compensation system of claim 276 wherein the pre-distortion filter circuit includes a zero setting time constant and a pole setting time constant, and the zero setting time constant and the pole setting time constant of the pre-distortion filter circuit are configured such that the frequency response of the pre-distortion filter circuit has a real-zero at around 11MHz and a real pole at around 20 MHz.

278. The parallel amplifier output impedance compensation system of claim 274 wherein the parallel amplifier output impedance compensation circuit is configured to provide the scaling factor based on an estimate of an inductive characteristic of a parallel amplifier output impedance and a scaled parallel amplifier output current generated by the parallel amplifier.

279. The parallel amplifier output impedance compensation system of claim 274 wherein the parallel amplifier output impedance compensation circuit is configured to provide the scaling factor based on an operational mode of a linear radio frequency power amplifier.

280. The parallel amplifier output impedance compensation system of claim 274 wherein the parallel amplifier output impedance compensation circuit is configured to provide the scaling factor based on a ratio of a parallel amplifier inductance parameter and an estimated power inductor inductance parameter, wherein:

the parallel amplifier inductance parameter is based on an estimate of an inductive characteristic of a parallel amplifier output impedance in a band of frequencies between 10 MHz and 30 MHz; and

the estimated power inductor inductance parameter is based on an estimate of an inductance of a power inductor in a band of frequencies between 10 MHz and 30 MHz, where the power inductor is in communication with the switching voltage output and the power amplifier supply output.

281. The parallel amplifier output impedance compensation system of claim 267, wherein the parallel amplifier output impedance compensation circuit further includes:

a summing circuit configured to:

receive the high frequency ripple compensation signal and the V_{RAMP} signal; and

combine the high frequency ripple compensation signal and the V_{RAMP} signal to generate a summing circuit output signal; and

a post-distortion filter circuit having a frequency response, and configured to:

receive the summing circuit output signal; and

filter the summing circuit output signal to generate the compensated V_{RAMP} signal based on a wide-bandwidth modulation of a mode of operation of a communication device.

282. The parallel amplifier output impedance compensation system of claim 281 wherein the frequency response of the post-distortion filter circuit is configured to be based on a radio frequency bandwidth of a linear radio frequency power amplifier associated with the wide-band modulation of the mode of operation of the communication device.

283. The parallel amplifier output impedance compensation system of claim 282 wherein the frequency response of the post-distortion filter circuit is further configured to provide frequency peaking to compensate for a power amplifier associated inductance, a power amplifier filter associated capacitance, and/ or a combination thereof.

284. The parallel amplifier output impedance compensation system of claim 265 wherein the parallel amplifier output impedance compensation circuit further includes:

a digital pre-distortion filter circuit configured to:

receive a digital V_{RAMP} signal; and

generate a pre-filtered V_{RAMP} signal based on the digital V_{RAMP} signal to equalize a frequency response of the parallel amplifier; and

a summing circuit in communication with the digital pre-distortion filter circuit, and configured to combine the high frequency ripple compensation signal with the pre-filtered V_{RAMP} signal to generate the compensated V_{RAMP} signal.

285. The parallel amplifier output impedance compensation system of claim 284 wherein the digital pre-distortion filter circuit is configured to provide frequency peaking to compensate for a power amplifier associated inductance, a power amplifier filter associated capacitance, and/or a combination thereof.

286. The parallel amplifier output impedance compensation system of claim 284 wherein the digital pre-distortion filter circuit is located in a digital baseband processing portion of a communication device.

287. The parallel amplifier output impedance compensation system of claim 284 wherein the digital pre-distortion filter circuit is an IIR filter.

288. The parallel amplifier output impedance compensation system of claim 287 wherein the IIR filter is configured as a multiple order filter.

289. The parallel amplifier output impedance compensation system of claim 287 wherein the IIR filter includes both feed forward filter coefficients and feedback filter coefficients.

290. The parallel amplifier output impedance compensation system of claim 287 wherein the IIR filter is configured to operate at a clock rate of about 312 MHz.

291. The parallel amplifier output impedance compensation system of claim 284 wherein the digital pre-distortion filter circuit is an FIR filter.

292. The parallel amplifier output impedance compensation system of claim 284 wherein the digital pre-distortion filter circuit is configured to have a pole at approximately 14.5 MHz and a zero at approximately 20 MHz.

293. The parallel amplifier output impedance compensation system of claim 261 wherein the switch mode power supply converter is configured as a multi-level charge pump buck converter.

294. A method for compensating for non-ideal parallel amplifier output impedance comprising:

receiving a V_{RAMP} signal;

generating an estimated switching voltage signal based on an operational state of a switcher control circuit that governs generation of a switching voltage by a switch mode power supply converter; and

generating a high frequency ripple compensation signal based on a difference between the V_{RAMP} signal and the estimated switching voltage signal;

generating a compensated V_{RAMP} signal based on the V_{RAMP} signal and the high frequency ripple compensation signal; and

providing the compensated V_{RAMP} signal to a parallel amplifier in order to regulate a power amplifier supply voltage at a power amplifier supply output.

295. The method of claim 294 further comprising:

delaying generation of the estimated switching voltage signal by an alignment period to temporally align the estimated switching voltage signal with the V_{RAMP} signal.

296. The method of claim 295 further comprising:

adjusting the alignment period to minimize a peak-to-peak ripple voltage on the power amplifier supply voltage.

297. The method of claim 295 wherein generating the high frequency ripple compensation signal based on the difference between the V_{RAMP} signal and the estimated switching voltage signal comprises:

subtracting the estimated switching voltage signal from the V_{RAMP} signal to generate an expected difference signal;

high pass filtering the expected difference signal to generate an estimated high frequency ripple signal; and

scaling the estimated high frequency ripple signal with a scaling factor to generate the high frequency ripple compensation signal.

298. The method of claim 297 wherein generating the high frequency ripple compensation signal based on the difference between the V_{RAMP} signal and the estimated switching voltage signal further comprises:

receiving the V_{RAMP} signal with a pre-distortion filter;

pre-distorting the V_{RAMP} signal with the pre-distortion filter to generate a pre-filtered V_{RAMP} signal based on a wideband modulation associated with a mode of operation of a communication device; and

combining the high frequency ripple compensation signal with the pre-filtered V_{RAMP} signal to generate the compensated V_{RAMP} signal.

299. The method of claim 298 further comprising:

receiving a scaled parallel amplifier output current from the parallel amplifier, wherein the scaled parallel amplifier output current is fractionally related to a parallel amplifier output current applied to the power amplifier supply output by the parallel amplifier to regulate the power amplifier supply voltage; and

generating the scaling factor based on the scaled parallel amplifier output current.

300. The method of claim 299 wherein generating the scaling factor based on the scaled parallel amplifier output current comprises:

selecting a coefficient of a scaling function based on a band of operation of a communication network; and

calculating the scaling factor with the scaling function based on the scaled parallel amplifier output current.

301. The method of claim 298 further comprising:

generating the scaling factor based on a band of operation of a communication network.

302. The method of claim 298 further comprising:

generating the scaling factor on a block-by-block transmission basis.

303. The method of claim 302 wherein generating the scaling factor on the block-by-block transmission basis comprises selecting the scaling factor based on an operational mode of a linear radio frequency power amplifier.

304. The method of claim 298 wherein the pre-distortion filter is one of an FIR filter and an IIR filter, the V_{RAMP} signal received by the pre-distortion filter is a digital V_{RAMP} signal, and pre-distorting the V_{RAMP} signal with the pre-distortion filter to generate the pre-filtered V_{RAMP} signal based on the wideband modulation associated with the mode of operation of the communication device comprises generating the pre-filtered V_{RAMP} signal based on the digital V_{RAMP} signal to equalize a frequency response of the parallel amplifier.

305. The method of claim 304 wherein generating the pre-filtered V_{RAMP} signal based on the digital V_{RAMP} signal to equalize the frequency response of the parallel amplifier further comprises providing frequency peaking to compensate for a power amplifier associated inductance, a power amplifier filter associated capacitance, and/or a combination thereof.

306. An operational amplifier comprising:

an operational amplifier front-end having a non-inverting input and an inverting input, and configured to generate an output stage source current control signal and an output stage sink current control signal based on a difference between the non-inverting input and the inverting input;

a first push-pull output stage having a first stage transconductance and a first push-pull output, and configured to generate a first stage output current at the first push-pull output based on the first stage transconductance, the output stage source current control signal, and the output stage sink current control signal;

a second push-pull output stage having a first digitally programmable transconductance and a second push-pull output configured to generate a second output stage current at the second push-pull output based on the first digitally programmable transconductance, the output stage source current control signal, and the output stage sink current control signal; and

a control interface configured to:

receive at least one control input; and

set the first digitally programmable transconductance based on the at least one control input.

307. The operational amplifier of claim 306 wherein the second push-pull output stage includes:

an array of programmable mirrored source current elements in communication with the control interface; and

an array of programmable mirrored sink current elements in communication with the control interface, and configured to be in communication with the array of programmable mirrored sink current elements to form the second push-pull output.

308. The operational amplifier of claim 307 wherein:

the array of programmable mirrored source current elements includes a plurality of binary weighted programmable source current elements; and

the array of programmable mirrored sink current elements includes a plurality of binary weighted programmable sink current elements.

309. The operational amplifier of claim 308 wherein the first push-pull output stage further includes:

a first push-pull PFET transistor having a gate configured to receive the output stage source current control signal, a source in communication with a supply voltage, and a drain in communication with the first push-pull output; and

a first push-pull NFET transistor having a gate configured to receive the output stage sink current control signal, a source in communication with a reference voltage, and a drain in communication with the first push-pull output.

310. The operational amplifier of claim 309 wherein a channel width of the first push-pull PFET transistor and a channel width of the first push-pull NFET transistor are configured such that a current sourcing capacity of the first push-pull PFET transistor is substantially matched to a current sinking capacity of the first push-pull NFET transistor.

311. The operational amplifier of claim 309 wherein the second push-pull output stage further includes:

an offset current PFET transistor having an offset current sourcing capacity, and including a gate in communication with the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain in communication with the second push-pull output; and

an offset current NFET transistor having an offset current sinking capacity substantially matched to the offset current sourcing capacity of the offset current PFET transistor, and including a gate in communication with the first push-pull NFET transistor, a source in communication with the reference voltage, and a drain in communication with the second push-pull output.

312. The operational amplifier of claim 309 wherein:

each of the plurality of binary weighted programmable source current elements is current mirrored to the first push-pull PFET transistor; and

each of the plurality of binary weighted programmable sink current elements is current mirrored to the first push-pull NFET transistor.

313. The operational amplifier of claim 312 wherein:

each of the plurality of binary weighted programmable source current elements and each of the plurality of binary weighted programmable sink current elements are in communication with the control interface; and

each of the plurality of binary weighted programmable source current elements and each of the plurality of binary weighted programmable sink current elements are configured to be in one of an on state and an off state as a function of the first digitally programmable transconductance.

314. The operational amplifier of claim 313 wherein each binary weighted programmable source current element of the plurality of binary weighted programmable source current elements is associated with a respective binary weighted programmable sink current element of the plurality of binary weighted programmable sink current elements.

315. The operational amplifier of claim 314 wherein the binary weighted programmable source current element and the respective binary weighted programmable sink current element associated with the binary weighted programmable source current element are configured such that a current sourcing capacity of the binary weighted programmable source current element is substantially equivalent to a current sinking capacity of the respective binary weighted programmable sink current element.

316. The operational amplifier of claim 309 wherein:

the plurality of binary weighted programmable source current elements includes "N" number of binary weighted programmable source current elements such that

for "n" having an integer value between 1 and "N", inclusive, each of an n^{th} binary weighted programmable source current element of the plurality of binary weighted programmable source current elements includes:

an n^{th} binary weighted PFET transistor having a channel width, a gate in communication with the gate of the first push-pull PFET transistor,

a source in communication with the supply voltage, and a drain, and configured to provide a current sourcing capacity based on the channel width of the n^{th} binary weighted PFET transistor; and

an n^{th} control PFET transistor having a gate in communication with the control interface, a source in communication with the drain of the n^{th} binary weighted PFET transistor, and a drain in communication with the second push-pull output, and configured to be in one of an on state and an off state as based on the first digitally programmable transconductance.

317. The operational amplifier of claim 316 wherein:

the channel width of each n^{th} binary weighted programmable source current element of the plurality of binary weighted programmable source current elements is interrelated such that for "n" having an integer value between 2 and "N", inclusive, the channel width of the n^{th} binary weighted PFET transistor and the channel width of the $(n-1)^{th}$ binary weighted PFET transistor are configured such that the current sourcing capacity of the n^{th} binary weighted PFET transistor of the n^{th} binary weighted programmable source current element is substantially equal to twice the current sourcing capacity of the $(n-1)^{th}$ binary weighted PFET transistor of an $(n-1)^{th}$ binary weighted programmable source current element.

318. The operational amplifier of claim 316 wherein:

the plurality of binary weighted programmable sink current elements includes "N" number of binary weighted programmable sink current elements such that for "n" having an integer value between 1 and "N", inclusive, each n^{th} binary weighted programmable sink current element of the plurality of binary weighted programmable sink elements includes:

an n^{th} binary weighted NFET transistor having a channel width, a gate in communication with the gate of the first push-pull NFET transistor, a source in communication with the supply voltage, and a drain, and configured to provide a current sinking capacity based on the channel width of the n^{th} binary weighted NFET transistor;

an n^{th} control NFET transistor having a gate in communication with the control interface, a source in communication with the drain of the n^{th} binary weighted NFET transistor, and a drain in communication with the second push-pull output, and configured to be in one of an on state and an off state as based on the first digitally programmable transconductance.

319. The operational amplifier of claim 318 wherein:

the channel width of each n^{th} binary weighted programmable sink current element of the plurality of binary weighted programmable sink current elements is interrelated such that for "n" having the integer value between 2 and N, inclusive, the channel width of the n^{th} binary weighted NFET transistor and a channel width of an $(n-1)^{th}$ binary weighted NFET transistor are configured such that the current sourcing capacity of the n^{th} binary weighted NFET transistor of the n^{th} binary weighted programmable sink current element is substantially equal to twice the current sourcing capacity of the $(n-1)^{th}$ binary weighted NFET transistor of the $(n-1)^{th}$ binary weighted programmable sink current element.

320. The operational amplifier of claim 319 wherein for "n" having the integer value between 1 and "N", inclusive, the channel width of the n^{th} binary weighted PFET transistor and the channel width of the n^{th} binary weighted NFET transistor are configured such that the current sourcing capacity of the n^{th} binary weighted PFET transistor is substantially equal to the current sourcing capacity of the n^{th} binary weighted NFET transistor.

321. The operational amplifier of claim 318 wherein for "n" having the integer value between 1 and "N", inclusive, the gate of the n^{th} control PFET transistor is configured to receive an n^{th} control PFET transistor signal from the control interface and the gate of the n^{th} control NFET transistor is configured to receive an n^{th} control NFET transistor signal from the control interface based on the first digitally programmable transconductance.

322. The operational amplifier of claim 321 further comprising a third push-pull output stage in communication with the control interface and including:

a second digitally programmable transconductance;

a plurality of binary weighted programmable sense source current elements in communication with the gate of the first push-pull PFET transistor; and

a plurality of binary weighted programmable sense sink current elements in communication with the gate of the first push-pull NFET transistor; and

wherein the plurality of binary weighted programmable sense source current elements are configured to be in communication with the plurality of binary weighted programmable sense sink current elements to form a third push-pull output.

323. The operational amplifier of claim 322 wherein each of the plurality of binary weighted programmable sense source current elements and each of the plurality of binary weighted programmable sense sink current elements are configured to be in one of an on state and an off state as a function of the second digitally programmable transconductance.

324. The operational amplifier of claim 323 wherein the control interface is further configured to set the second digitally programmable transconductance based on at least a portion of the at least one control input.

325. The operational amplifier of claim 322 wherein each binary weighted programmable sense source current element of the plurality of binary weighted programmable sense source current elements is associated with a respective binary weighted programmable sense sink current element of the plurality of binary weighted programmable sense sink current elements.

326. The operational amplifier of claim 325 wherein the binary weighted programmable sense source current element and the respective binary weighted

programmable sense sink current element associated with the binary weighted programmable sense source current element are configured such that a current sourcing capacity of the binary weighted programmable sense source current element is substantially equivalent to a current sinking capacity of the respective binary weighted programmable sense sink current element.

327. The operational amplifier of claim 322 wherein:

the plurality of binary weighted programmable sense source current elements includes "M" number of binary weighted programmable sense source current elements such that for "m" having an integer value between 1 and "M", inclusive, each m^{th} binary weighted programmable sense source current element of the plurality of binary weighted programmable sense source current elements includes:

an m^{th} binary weighted sense PFET transistor having a channel width, a gate in communication with the gate of the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain, and configured to provide a current sourcing capacity based on the channel width of the m^{th} binary weighted sense PFET transistor;

an m^{th} control sense PFET transistor having a gate in communication with the control interface, a source in communication with the drain of the m^{th} binary weighted sense PFET transistor, and a drain in communication with the third push-pull output, and configured to be in one of an on state and an off state as based on the second digitally programmable transconductance.

328. The operational amplifier of claim 327 wherein:

the channel width of each m^{th} binary weighted programmable sense source current element of the plurality of binary weighted programmable sense source current elements is interrelated such that for "m" having an integer value between 2 and "M", inclusive, the channel width of the m^{th} binary weighted sense PFET transistor and the channel width of an $(m-1)^{th}$ binary weighted sense PFET

transistor are configured such that the current sourcing capacity of the m^{th} binary weighted sense PFET transistor of the m^{th} binary weighted programmable sense source current elementis substantially equal to twice the current sourcing capacity of the $(m-1)^{th}$ binary weighted sense PFET transistor of an $(m-1)^{th}$ binary weighted programmable sense source current element.

329. The operational amplifier of claim 328 wherein:

the plurality of binary weighted programmable sense sink current elements includes "M" number of binary weighted programmable sense sink current elements such that for "m" having an integer value between 1 and "M", inclusive, each m^{th} binary weighted programmable sense sink current element of the plurality of binary weighted programmable sense sink current elements includes:

an m^{th} binary weighted sense NFET transistor having a channel width, a gate in communication with the gate of the first push-pull NFET transistor, a source in communication with the supply voltage, and a drain, and configured to provide a current sinking capacity based on the channel width of the m^{th} binary weighted sense NFET transistor;

an m^{th} control sense NFET transistor having a gate in communication with the control interface, a source in communication with the drain of the m^{th} binary weighted sense NFET transistor, and a drain in communication with the third push-pull output, and configured to be in one of an on state and an off state as based on the second digitally programmable transconductance.

330. The operational amplifier of claim 329 wherein:

for "m" having the integer value between 1 and "M", inclusive, the gate of the m^{th} control sense PFET transistor is configured to receive an m^{th} control sense PFET transistor signal from the control interface and the gate of the m^{th} control sense NFET transistor is configured to receive an m^{th} control sense NFET transistor signal from the control interface based on the second digitally programmable transconductance.

331. The operational amplifier of claim 329 wherein for "m" having the integer value between 2 and "M", inclusive, the channel width of the m^{th} binary weighted sense NFET transistor of an m^{th} binary weighted programmable sense sink current element and the channel width of an $(m-1)^{th}$ binary weighted sense NFET transistor of an $(m-1)^{th}$ binary weighted programmable sense sink current element are configured such that the current sourcing capacity of the m^{th} binary weighted sense NFET transistor is substantially equal to twice the current sourcing capacity of the $(m-1)^{th}$ binary weighted sense NFET transistor.

332. The operational amplifier of claim 329 wherein for "m" having the integer value between 1 and "M", inclusive, the channel width of the m^{th} binary weighted sense PFET transistor of the m^{th} binary weighted programmable sense source current element and the channel width of the m^{th} binary weighted sense NFET transistor of the m^{th} binary weighted programmable sense sink current element are configured such that the current sourcing capacity of the m^{th} binary weighted sense PFET transistor is substantially equal to the current sourcing capacity of the m^{th} binary weighted sense NFET transistor.

333. The operational amplifier of claim 332 wherein for "m" equal to "M" and "n" equal to N, the channel width of the m^{th} binary weighted sense PFET transistor and the channel width of the m^{th} binary weighted sense NFET transistor are further configured such that the current sourcing capacity of the m^{th} binary weighted sense PFET transistor and the current sinking capacity of the m^{th} binary weighted sense NFET transistor are fractionally related by a sense scaling factor to the current sourcing capacity of the n^{th} binary weighted PFET transistor and the current sinking capacity of the n^{th} binary weighted NFET transistor, respectively.

334. The operational amplifier of claim 332 wherein "N" > "M".

335. The operational amplifier of claim 334 wherein:

the second digitally programmable transconductance is a function of the first digitally programmable transconductance; and

for "m" having the integer value between 1 and "M", inclusive, "n" equals "m" plus "N" - "M", the gate of the m^{th} control sense PFET transistor is configured to receive the n^{th} control PFET transistor signal from the control interface and the gate of the m^{th} control sense NFET transistor is configured to receive the n^{th} control NFET transistor signal from the control interface.

336. The operational amplifier of claim 334 wherein "M" = 5 and "N" = 6.

337. The operational amplifier of claim 322 further comprising an operational amplifier output isolation circuit including a high impedance input in communication with the first push-pull output and an isolated feedback node configured to provide a feedback voltage based on a first push-pull output voltage generated at the first push-pull output, wherein the isolated feedback node is configured to substantially isolate the first push-pull output from a feedback network impedance.

338. The operational amplifier of claim 337 wherein the operational amplifier output isolation circuit includes:

a first NFET transistor having a gate in communication with the high impedance input, a drain in communication with the supply voltage, and a source in communication with the isolated feedback node; and

a second NFET transistor having a gate in communication with a bias voltage, a drain in communication with the isolated feedback node, and a source in communication with the reference voltage.

339. The operational amplifier of claim 338 further comprising a transconductance bias circuit having a transconductance setting impedance and coupled between the first push-pull output and the reference voltage.

340. The operational amplifier of claim 339 wherein the transconductance bias circuit includes a bias resistor having a bias resistor resistance and a bias capacitor having a bias capacitor capacitance coupled in series, wherein the transconductance setting impedance is substantially equal to the bias resistor resistance plus a bias capacitor impedance based on the bias capacitor capacitance.

341. The operational amplifier of claim 322 wherein:

the second push-pull output stage further includes:

an offset current PFET transistor having a channel width, and including agate in communication with the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain in communication with the second push-pull output;

an offset current NFET transistor having a channel width, a gate in communication with the first push-pull NFET transistor, a source in communication with the reference voltage, and a drain in communication with the second push-pull output; and

wherein the channel width of the offset current PFET transistor and the channel width of the offset current NFET transistor are configured such that a current sinking capacity of the offset current PFET transistor is substantially matched to a current sinking capacity of the offset current NFET transistor;

the third push-pull output stage further includes:

an offset sense current PFET transistor having a channel width, a gate in communication with the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain in communication with the second push-pull output; and

an offset sense current NFET transistor having a channel width, a gate in communication with the first push-pull NFET transistor, a source in

communication with the reference voltage, and a drain in communication with the second push-pull output; and

wherein the channel width of the offset sense current PFET transistor and the channel width of the offset sense current NFET transistor are configured such that the current sinking capacity of the offset sense current PFET transistor and the current sourcing capacity of the offset sense current NFET transistor are fractionally related by a sense scaling factor to the current sourcing capacity of the offset current PFET transistor and the offset current NFET transistor, respectively.

342. The operational amplifier of claim 341 wherein the third push-pull output stage is configured such that the second digitally programmable transconductance has a minimum transconductance value that is fractionally related by the sense scaling factor to a minimum transconductance value of the first digitally programmable transconductance.

343. The operational amplifier of claim 306 wherein the second push-pull output stage is configured such that the first digitally programmable transconductance has a minimum transconductance value.

344. The operational amplifier of claim 343 wherein the first digitally programmable transconductance may be configured to provide at least 64 transconductance values.

345. The operational amplifier of claim 306 further comprising:

a third push-pull output stage including a second digitally programmable transconductance, a third push-pull output, and configured to generate a third output stage current at the third push-pull output based on the second digitally programmable transconductance, the output stage source current control signal, and the output stage sink current control signal.

346. The operational amplifier of claim 345 wherein the control interface is in communication with the third push-pull output stage, and configured to set the second digitally programmable transconductance based on at least a portion of the at least one control input.

347. The operational amplifier of claim 346 wherein the second digitally programmable transconductance is substantially related to the first digitally programmable transconductance by a sense scaling factor.

348. The operational amplifier of claim 347 wherein:

the second push-pull output stage is configured such that the first digitally programmable transconductance has a minimum transconductance value; and

the third push-pull output stage is configured such that the second digitally programmable transconductance has a minimum transconductance value that is substantially related to the minimum transconductance value of the first digitally programmable transconductance by a sense scaling factor.

349. The operational amplifier of claim 348 wherein:

the first digitally programmable transconductance may be configured to provide 64 transconductance values; and

the second digitally programmable transconductance may be configured to provide 32 transconductance values.

350. The operational amplifier of claim 345 further comprising an operational amplifier output isolation circuit including a high impedance input in communication with the first push-pull output and an isolated feedback node configured to provide a feedback voltage based on a first push-pull output voltage generated at the first push-pull output, wherein the isolated feedback node is configured to substantially isolate the first push-pull output from a feedback network impedance.

351. The operational amplifier of claim 350 wherein the operational amplifier output isolation circuit includes:

a first NFET transistor having a gate in communication with the high impedance input, a drain in communication with a supply voltage, and a source in communication with the isolated feedback node; and

a second NFET transistor having a gate in communication with a bias voltage, a drain in communication with the isolated feedback node, and a source in communication with a reference voltage.

352. The operational amplifier of claim 351 further comprising a transconductance bias circuit having a transconductance setting impedance and coupled between the first push-pull output and the reference voltage.

353. A programmable delay circuit with minimize jitter comprising:

a variable capacitor having a variable capacitance and including a first node and a second node in communication with a reference voltage;

a first transistor including a control node configured to receive a digital logic level signal to be delayed, a first node, and a second node coupled to the first node of the variable capacitor, and configured to source a first bias current to the variable capacitor in response to the digital logic level signal being below a logic low threshold voltage to charge the variable capacitor; and

a second transistor including a control node in communication with the control node of the first transistor and configured to receive the digital logic level signal to be delayed, a first node, and a second node in communication with the variable capacitor and the second node of the first transistor, and configured to sink a second bias current from the variable capacitor in response to the digital logic level signal to be delayed being above a logic high threshold voltage to discharge the variable capacitor;

a third transistor including a control node in communication with the control node of the first transistor and the control node of the second transistor, and configured to receive the digital logic level signal to be delayed, a first node

in communication with a first known voltage level, and a second node in communication with the first node of the first transistor, and configured to provide a conductive path based on a voltage level of the digital logic level signal; and

a fourth transistor including a control node in communication with the control node of the first transistor and the control node of the second transistor, and configured to receive the digital logic level signal to be delayed, a first node in communication with a second known voltage level, and a second node in communication with the first node of the second transistor, and configured to provide a conductive path based on the voltage level of the digital logic level signal.

354. The programmable delay circuit with minimize jitter of claim 353 wherein:

the third transistor is further configured to pull the first node of the first transistor to the first known voltage level at least while the first transistor is in a non-conducting mode of operation; and

the fourth transistor is further configured to pull the first node of the second transistor to the second known voltage level at least while the second transistor is in a non-conducting mode of operation.

355. The programmable delay circuit with minimize jitter of claim 354 wherein:

the variable capacitor has a variable capacitor voltage on the first node of the variable capacitor;

the variable capacitor voltage is substantially equal to the first known voltage level after the variable capacitor is discharged; and

the variable capacitor voltage is substantially equal to the second known voltage level after the variable capacitor is charged.

356. The programmable delay circuit with minimize jitter of claim 355 further comprising:

a fifth transistor including a first node in communication with a supply voltage, a second node in communication with the first node of the first transistor,

the fifth transistor configured to source the first bias current to the first node of the first transistor as a function of the supply voltage; and

a sixth transistor including a first node in communication with ground, a second node in communication with the first node of the second transistor, the sixth transistor configured to sink the second bias current from the first node of the second transistor as a function of the supply voltage.

357. The programmable delay circuit with minimize jitter of claim 355 further comprising:

an output buffer stage including an output buffer output, an output buffer input having a logic low threshold voltage and a logic high threshold voltage; and configured to:

generate a logic high output voltage at the output buffer output in response to the variable capacitor voltage falling below the logic low threshold voltage of the output buffer stage; and

generate a logic low output voltage at the output buffer output in response to the variable capacitor voltage exceeding the logic high threshold voltage of the output buffer stage.

358. The programmable delay circuit with minimize jitter of claim 357 wherein a programmable propagation delay between the control node of the first transistor and the output buffer output is based on the variable capacitance, the first bias current, and the second bias current.

359. The programmable delay circuit with minimize jitter of claim 358 wherein the first bias current is substantially equal to the second bias current.

360. A programmable delay circuit with minimize jitter comprising:

a variable capacitor including a programmable capacitance, a first node, and a second node, and having a variable capacitor voltage on the first node of the variable capacitor;

a first PFET transistor including gate, a source in communication with a supply voltage, and a drain, and configured to source a first bias current from the drain;

a second PFET transistor including a gate configured to receive a digital logic signal have a signal voltage, a source in communication with the drain of the first PFET transistor, and a source in communication with the first node of the variable capacitor, and configured to charge the variable capacitor with a capacitor current substantially equal to the first bias current in response to the signal voltage of the digital logic signal falling below a logic low threshold voltage;

a first NFET transistor including a gate, a source in communication with a reference voltage, and a drain, and configured to sink a second bias current into the drain;

a second NFET transistor including a gate in communication with the gate of the second PFET transistor, a source in communication with the drain of the first NFET transistor, and a source in communication with the first node of the variable capacitor, and configured to discharge the variable capacitor with the capacitor current substantially equal to the second bias current in response to the signal voltage of the digital logic signal rising above a logic high threshold voltage;

a third PFET transistor including a gate in communication with the gate of the second PFET transistor and the gate of the second NFET transistor, a source in communication with a first known voltage, and a drain in communication with the source of the second NFET transistor and the drain of the first NFET transistor;

a third NFET transistor including a gate in communication with the gate of the second PFET transistor, the gate of the second NFET transistor, and the gate of the third PFET transistor, a source in communication with a second known voltage, and a drain in communication with the source of the second NFET transistor and the drain of the first NFET transistor; and

an output buffer stage including an output buffer output, an output buffer input having a logic low threshold voltage and a logic high threshold voltage; and configured to:

generate a logic high output voltage at the output buffer output in response to the variable capacitor voltage falling below the logic low threshold voltage of the output buffer stage; and

generate a logic low output voltage at the output buffer output in response to the variable capacitor voltage exceeding the logic high threshold voltage of the output buffer stage.

361. The programmable delay circuit with minimize jitter of claim 360 wherein:

the variable capacitor voltage is substantially equal to the first known voltage after the variable capacitor is discharged; and

the variable capacitor voltage is substantially equal to the second known voltage after the variable capacitor is charged.

362. The programmable delay circuit with minimize jitter of claim 361 wherein the first known voltage is substantially equal to the supply voltage and the second known voltage is substantially equal to the reference voltage.

363. The programmable delay circuit with minimize jitter of claim 361 wherein a programmable delay between the gate of the second PFET transistor and the output buffer output of the output buffer stage while the variable capacitor is being charged is a function of the programmable capacitance and the first bias current.

364. The programmable delay circuit with minimize jitter of claim 363 wherein a programmable delay between the gate of the second NFET transistor and the output buffer output of the output buffer stage while the variable capacitor is being discharged is a function of the programmable capacitance and the second bias current.

365. The programmable delay circuit with minimize jitter of claim 364 wherein the first bias current is substantially equal to the second bias current.

366. The programmable delay circuit with minimize jitter of claim 360 wherein:

the third PFET transistor is configured to pull the source of the second NFET transistor and the drain of the first NFET transistor to the first known voltage at least while the second NFET transistor is in a non-conducting mode of operation; and

the third NFET transistor is configured to pull the source of the second PFET transistor and the drain of the first PFET transistor to the second known voltage at least while the second PFET transistor is in a non-conducting mode of operation.

367. The programmable delay circuit with minimize jitter of claim 366 wherein:

the variable capacitor voltage is substantially equal to the first known voltage after the variable capacitor is discharged; and

the variable capacitor voltage is substantially equal to the second known voltage after the variable capacitor is charged.

368. A method for minimizing jitter of a programmable delay period provided by a programmable delay circuit comprising:

providing a first current source configured to provide a first bias current to a source of a first PFET transistor and a second current source configured to sink a second bias current from a source of a first NFET transistor;

placing the first PFET transistor in a conducting mode based on a signal voltage of a digital signal to be delayed falling below a logic low threshold voltage to charge a variable capacitor with a capacitor current substantially equal to the first bias current;

placing the first NFET transistor in a conducting mode based on the signal voltage of the digital signal to be delayed rising above a logic high threshold

voltage to discharge the variable capacitor with the capacitor current substantially equal to the second bias current;

placing the first PFET transistor in a non-conducting mode based on the signal voltage of the digital signal to be delayed rising above the logic high threshold voltage;

placing the first NFET transistor in a non-conducting mode based on the signal voltage of the digital signal to be delayed falling below the logic low threshold voltage;

pulling the source of the first PFET transistor to a first known voltage based on the first PFET transistor transitioning into the non-conducting mode; and

pulling the source of the first NFET transistor to a second known voltage based on the first PFET transistor transitioning to the non-conducting mode.

369. The method for minimizing jitter of the programmable delay period provided by the programmable delay circuit of claim 368 wherein pulling the source of the first PFET transistor to the first known voltage based on the first PFET transistor transitioning into the non-conducting mode comprises:

preventing charge build up at the source of the first PFET transistor while the first PFET transistor is in the non-conducting mode.

370. The method for minimizing jitter of the programmable delay period provided by the programmable delay circuit of claim 369 wherein pulling the source of the first NFET transistor to the first known voltage based on the first NFET transistor transitioning into the non-conducting mode comprises:

preventing charge build up at the source of the first NFET transistor while the first NFET transistor is in the non-conducting mode.

371. The method for minimizing jitter of the programmable delay period provided by the programmable delay circuit of claim 368 wherein placing the first PFET transistor in the conducting mode based on the signal voltage of the digital

signal to be delayed falling below the logic low threshold voltage to charge the variable capacitor with the capacitor current substantially equal to the first bias current comprises:

charging the variable capacitor to provide a charging delay period based on a programmable capacitance of the variable capacitor and the first bias current.

372. The method for minimizing jitter of the programmable delay period provided by the programmable delay circuit of claim 371 wherein placing the first NFET transistor in the conducting mode based on the signal voltage of the digital signal to be delayed rising above the logic high threshold voltage to charge the variable capacitor with the capacitor current substantially equal to the second bias current comprises:

discharging the variable capacitor to provide a discharging delay period based on the programmable capacitance of the variable capacitor and the second bias current.

373. The method for minimizing jitter of the programmable delay period provided by the programmable delay circuit of claim 372 wherein the first bias current is substantially equal to the second bias current.

374. The method for minimizing jitter of the programmable delay period provided by the programmable delay circuit of claim 372 wherein:

a variable capacitor voltage across the variable capacitor is substantially equal to the first known voltage after the variable capacitor is fully discharged; and

the variable capacitor voltage across the variable capacitor is substantially equal to the second known voltage after the variable capacitor is fully charged.

375. A programmable delay circuit comprising:

a bias reference and mirror circuit configured to generate a bias reference current that is substantially proportional to a supply voltage;

a variable delay circuit including:

a variable capacitor having a variable capacitor voltage; and

an output buffer stage including an output buffer output, an output buffer input having a logic low threshold voltage that is substantially proportional to the supply voltage and a logic high threshold voltage that is substantially proportional to the supply voltage; and configured to:

generate a logic high output voltage at the output buffer output in response to the variable capacitor voltage falling below the logic low threshold voltage; and

generate a logic low output voltage at the output buffer output in response to the variable capacitor voltage exceeding the logic high threshold voltage; and

the variable delay circuit configured to generate a capacitor current in the variable capacitor based on the bias reference current to provide a programmable delay period that is substantially insensitive to a change in the supply voltage.

376. The programmable delay circuit of claim 375 wherein the variable delay circuit is configured such that a sensitivity of the capacitor current to a change in the supply voltage is substantially offset by a sensitivity of the logic low threshold voltage to the supply voltage and a sensitivity of the logic high threshold voltage to the supply voltage.

377. The programmable delay circuit of claim 375 wherein the variable delay circuit is further configured to generate the capacitor current that is substantially proportional to the bias reference current.

378. The programmable delay circuit of claim 375 wherein the variable delay circuit is further configured to:

source a first bias current that is substantially proportional to the bias reference current to the variable capacitor in order to charge the variable capacitor; and

sink a second bias current that is substantially proportional to the bias reference current to the variable capacitor in order to discharge the variable capacitor.

379. The programmable delay circuit of claim 378 wherein the first bias current is substantially equal to the second bias current.

380. The programmable delay circuit of claim 378 wherein:

the variable capacitor includes a first terminal configured to provide the variable capacitor voltage and a second terminal in communication with a reference voltage; and

the variable delay circuit includes:

a first PFET transistor having a gate, a source in communication with the supply voltage, and a drain, and configured to generate a drain current from the drain of the first PFET transistor substantially equal to the first bias current; and

a second PFET transistor having a gate configured to receive an input signal voltage, a source in communication with the drain of the first PFET transistor, and a drain in communication with the first terminal of the variable capacitor, and configured to source the first bias current to generate the capacitor current of the variable capacitor in response to the input signal voltage falling below the logic low output voltage.

381. The programmable delay circuit of claim 380 wherein the variable delay circuit includes:

a first NFET transistor having a gate, a source in communication with the reference voltage, and a drain, and configured to generate a drain current at the drain of the first NFET transistor substantially equal to the second bias current; and

a second NFET transistor having a gate configured to receive the input signal voltage, a source in communication with the drain of the first NFET transistor, and a drain in communication with the first terminal of the variable capacitor, and configured to sink the second bias current to generate the capacitor current of the variable capacitor in response to the input signal voltage rising above the logic high output voltage.

382. The programmable delay circuit of claim 381 wherein the bias reference and mirror circuit includes:

a third NFET transistor having a source in communication with the reference voltage, and a drain, and a gate in communication with the drain of the third NFET transistor and the gate of the first NFET transistor, and configured to sink a drain current into the drain of the third NFET transistor;

a fourth NFET transistor having a gate in communication with the drain and the gate of the third NFET transistor, a source in communication with the reference voltage, and a drain configured to generate a drain current into the drain of the fourth NFET transistor that is substantially proportional to the drain current of the third NFET transistor;

and a third PFET transistor having a source in communication with the supply voltage, a gate in communication with the gate of the first PFET transistor, and a drain in communication with the gate of the third PFET transistor and the drain of the fourth NFET transistor, and configured to generate a drain current from the drain of the third PFET transistor substantially equal to the drain current of the fourth NFET transistor;

wherein the bias reference and mirror circuit is further configured to generate the drain current into the drain of the third NFET transistor substantially equal to the bias reference current.

383. The programmable delay circuit of claim 382 wherein the first NFET transistor is configured to generate the drain current at the drain of the first NFET

transistor that is substantially proportional to the drain current of the third NFET transistor.

384. The programmable delay circuit of claim 383 further comprising:

a voltage divider circuit including:

a first resistor having a first resistance, a first terminal in communication with the supply voltage and a second terminal;

a second resistor having a second resistance substantially equal to the first resistance of the first resistor, a first terminal and a second terminal in communication with the reference voltage;

a fourth PFET transistor having a source in communication with the second terminal of the second resistor, a gate, and a drain in communication with the gate of the fourth PFET transistor;

a fifth PFET transistor having a source in communication with the gate and the drain of the fourth PFET transistor, a gate, and a drain in communication with the gate of the fifth PFET transistor and the first terminal of the second resistor; and wherein a source voltage on the source of the second PFET transistor is substantially equal to one-half the supply voltage; and

wherein the bias reference and mirror circuit includes:

a sixth PFET transistor having a gate in communication with the gate of the fifth PFET transistor, a drain in communication with the drain and the gate of the third NFET transistor, and a source, and configured to have a source voltage on the source of the sixth PFET transistor substantially equal to the source voltage on the source of the second PFET transistor; and

a third resistor having a third resistance, a first terminal in communication with the supply voltage and a second terminal in communication with the source of the sixth PFET transistor; and

wherein the bias reference current is substantially equal to the supply voltage less the source voltage on the source of the sixth PFET transistor divided by the third resistance.

385. The programmable delay circuit of claim 384 wherein the bias reference current is substantially equal to the supply voltage divided by twice the third resistance.

386. The programmable delay circuit of claim 375 wherein the bias reference and mirror circuit includes a first resistor having a first resistance, a first terminal coupled to the supply voltage and a second terminal, and is configured to generate the bias reference current based on a voltage on the second terminal of the first resistor and the first resistance;

a voltage divider circuit in communication with the second terminal of the first resistor, and configured to set the voltage on the second terminal of the first resistor to be substantially equal to one-half the supply voltage.

387. The programmable delay circuit of claim 386 wherein the voltage divider circuit includes:

a second resistor having a second resistance, a first terminal in communication with the supply voltage and a second terminal;

a third resistor having a third resistance substantially equal to the second resistance of the second resistor, a first terminal and a second terminal in communication with a reference voltage;

a first PFET transistor having a source in communication with the second terminal of the second resistor, a gate, and a drain in communication with the gate of the first PFET transistor;

a second PFET transistor having a source in communication with the gate and the drain of the first PFET transistor, a gate, and a drain in communication with the gate of the second PFET transistor and the first terminal of the third resistor; and

wherein a voltage on the source of the second PFET transistor is substantially equal to one-half the supply voltage.

388. The programmable delay circuit of claim 387 wherein the bias reference and mirror circuit further includes a third PFET transistor having a gate in communication with the gate and drain of the second PFET transistor, a source in communication with the second terminal of the first resistor, and a drain, wherein the second PFET transistor and the third PFET transistor are configured such that the voltage on the second terminal of the first resistor is substantially equal to one-half the supply voltage.

389. The programmable delay circuit of claim 387 wherein the bias reference current is substantially equal to twice the first resistance divided by the supply voltage.

390. The programmable delay circuit of claim 375 wherein the variable delay circuit is configured to provide the programmable delay period based on a variable capacitance of the variable capacitor.

391. The programmable delay circuit of claim 390 wherein the variable capacitor is a programmable capacitor array including a plurality of binary weighted capacitors.

392. A method for variably delaying a signal comprising:

receiving a digital logic level input signal having a digital logic input signal voltage to be variably delayed;

generating a bias reference current that is proportional to a supply voltage;

generating a capacitor current in a variable capacitor based on the bias reference current and the digital logic input signal voltage to produce a variable capacitor voltage on the variable capacitor;

adjusting a logic high threshold voltage and a logic low threshold voltage of an output buffer proportionally to the supply voltage; and

changing an output voltage of the output buffer in response to the variable capacitor voltage being one of above the logic high threshold voltage of the output buffer and below the logic low threshold voltage of the output buffer.

393. The method for variably delaying the signal of claim 392 wherein generating the bias reference current that is proportional to the supply voltage comprises:

generating a reference voltage substantially equal to one-half the supply voltage; and

generating the bias reference current substantially based on a difference between the supply voltage and the reference voltage.

394. The method for variably delaying the signal of claim 393 wherein generating the capacitor current in the variable capacitor based on the bias reference current and the digital logic input signal voltage to produce the variable capacitor voltage on the variable capacitor comprises:

current mirroring the bias reference current to generate a first bias current and a second bias current;

sourcing the first bias current to the variable capacitor to generate the capacitor current in response to the digital logic input signal voltage being substantially equal to at most the logic low threshold voltage to discharge the variable capacitor; and

sinking the second bias current from the variable capacitor to generate the capacitor current based in response to the digital logic input signal voltage being substantially equal to at least the logic high threshold voltage to discharge the variable capacitor.

395. The method for variably delaying the signal of claim 394 further comprising:

delaying the digital logic level input signal by a programmable delay period based on a variable capacitance of the variable capacitor and the capacitor current; and

adjusting the variable capacitance of the variable capacitor to change the programmable delay period.

396. An offset voltage control circuit for regulating an offset voltage between a power amplifier supply output and a parallel amplifier circuit output comprising:

a summing circuit configured to:

receive a power amplifier supply voltage provided to a linear radio frequency power amplifier, a parallel amplifier circuit output voltage generated by a parallel amplifier circuit to regulate the power amplifier supply voltage, and an offset voltage target signal; and

subtract a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal; and

an integrator circuit configured to:

integrate the offset voltage error signal to generate an offset voltage feedback signal; and

provide the offset voltage feedback signal to a switcher control circuit of a switch mode power supply converter to regulate a difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage.

397. The offset voltage control circuit of claim 396 wherein the offset voltage target signal is substantially equal to a target offset voltage parameter.

398. The offset voltage control circuit of claim 396 wherein the integrator circuit is an integrator with zero compensation.

399. The offset voltage control circuit of claim 398 wherein a bandwidth of the integrator with zero compensation is based on a first time constant and a second time constant.

400. The offset voltage control circuit of claim 399 wherein the integrator with zero compensation has a Laplace transfer function including $(1 + Tau_1 \times s) / (Tau_2 \times s)$, wherein Tau_1 is the first time constant and Tau_2 is the second time constant.

401. The offset voltage control circuit of claim 400 further comprising a local parameter storage circuit configured to store a first normal operation time constant and a second normal operation time constant.

402. The offset voltage control circuit of claim 401 further comprising:

a pre-charge time configured to generate a timer event after a predetermined time period;

a control circuit configured to:

determine prior to commencement of a transmission slot whether to configure the bandwidth of the integrator with zero compensation to be one of a pre-charge bandwidth for the predetermined time period and a normal operation bandwidth based on a magnitude of the offset voltage error signal, wherein the pre-charge bandwidth is greater than the normal operation bandwidth; and

in response to a determination prior to commencement of the transmission slot to configure the bandwidth of the integrator with zero compensation to be the pre-charge bandwidth for the predetermined time period:

set the first time constant equal to a first pre-charge time constant and the second time constant equal to a second pre-charge time constant to configure the bandwidth of the integrator with zero compensation to be the pre-charge bandwidth; and

enable the pre-charge time configured to generate the timer event after the predetermined time period; and

wherein the integrator with zero compensation is further configured to use the first normal operation time constant from the local parameter storage circuit as the first time constant and the second normal operation time constant from the local parameter storage circuit as the second time constant in response to the timer event.

403. The offset voltage control circuit of claim 402 wherein:

in response to a determination prior to commencement of the transmission slot, the control circuit is further configured to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth, configure the integrator with zero compensation to use the first normal operation time constant from the local parameter storage circuit as the first time constant and the second normal operation time constant from the local parameter storage circuit as the second time constant.

404. The offset voltage control circuit of claim 396 further comprising:

an offset target signal selection circuit configured to provide the offset voltage target signal based on one of a target offset voltage parameter, a V_{RAMP} signal, and a pre-filtered V_{RAMP} signal.

405. The offset voltage control circuit of claim 398 wherein:

the switcher control circuit includes a plurality of comparators, the switcher control circuit configured to:

generate a first composite feedback signal based on the offset voltage feedback signal;

generate a second composite feedback signal without the offset voltage feedback signal;

provide the first composite feedback signal to less than all of the plurality of comparators;

provide the second composite feedback signal to at least one of the plurality of comparators; and

control generation of a switching voltage by the switch mode power supply converter based on outputs generated by the plurality of comparators.

406. The offset voltage control circuit of claim 405 wherein the switch mode power supply converter is a multi-level charge pump buck converter.

407. A method for regulating a voltage across a coupling circuit between a power amplifier supply output and a parallel amplifier circuit output comprising:

receiving a power amplifier supply voltage provided to a linear radio frequency power amplifier, a parallel amplifier circuit output voltage generated by a parallel amplifier circuit to regulate the power amplifier supply voltage, and an offset voltage target signal;

subtracting a combination of the parallel amplifier circuit output voltage and the offset voltage target signal from the power amplifier supply voltage to generate an offset voltage error signal;

integrating the offset voltage error signal to generate an offset voltage feedback signal; and

providing the offset voltage feedback signal to a switch mode power supply converter to regulate a difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage.

408. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 407 wherein receiving the offset voltage target signal comprises providing the offset voltage target signal based on a target offset voltage parameter.

409. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 407 wherein integrating the offset voltage error signal to generate the offset voltage feedback signal comprises:

integrating the offset voltage error signal with an integrator with zero compensation to generate the offset voltage feedback signal.

410. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 409 wherein integrating the offset voltage error signal with the integrator with zero compensation to generate the offset voltage feedback signal comprises:

controlling a bandwidth of the integrator with zero compensation based on a first time constant and a second time constant.

411. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 410 wherein controlling the bandwidth of the integrator with zero compensation based on the first time constant and the second time constant comprises:

determining prior to commencement of a data transmission whether to configure the bandwidth of the integrator with zero compensation to be one of a pre-charge operation bandwidth for a predetermined time period and a normal operation bandwidth based on a magnitude of the offset voltage error signal, wherein the pre-charge operation bandwidth is greater than the normal operation bandwidth; and

in response to a determination prior to commencement of the data transmission to configure the bandwidth of the integrator with zero compensation to be the pre-charge operation bandwidth for the predetermined time period:

setting the first time constant equal to a first pre-charge operation time constant and the second time constant equal to a second pre-charge operation time constant to configure the bandwidth of the integrator with zero compensation to be the pre-charge operation bandwidth; and

after the predetermined time period, setting the first time constant equal to a first normal operation time constant and the second time constant equal to a second normal operation time constant to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth.

412. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 411 wherein controlling the bandwidth of the integrator with zero compensation based on the first time constant and the second time constant further comprises:

in response to a determination prior to commencement of the data transmission to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth, setting the first time constant equal to the first normal operation time constant and the second time constant equal to the second normal operation time constant to configure the bandwidth of the integrator with zero compensation to be the normal operation bandwidth.

413. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 407 wherein receiving the offset voltage target signal comprises:

providing the offset voltage target signal based on one of an offset voltage target parameter, a V_{RAMP} signal, and a pre-filtered V_{RAMP} signal.

414. The method for regulating the voltage across the coupling circuit between the power amplifier supply output and the parallel amplifier circuit output of claim 407 wherein providing the offset voltage feedback signal to the switch mode power supply converter to regulate the difference between the power amplifier supply voltage and the parallel amplifier circuit output voltage comprises:

providing a composite feedback signal based on the offset voltage feedback signal to less than all of a plurality of comparators of a switcher control circuit of the switch mode power supply converter; and

determining an operational state of the switcher control circuit based on outputs generated by all of the plurality of comparators.

415. An operational amplifier comprising:

an operational amplifier front-end having a non-inverting input and an inverting input, and configured to generate an output stage source current control signal and an output stage sink current control signal based on a difference between the non-inverting input and the inverting input;

a first push-pull output stage having a first stage transconductance and a first push-pull output, and configured to generate a first stage output current at the first push-pull output based on the first stage transconductance, the output stage source current control signal, and the output stage sink current control signal;

a second push-pull output stage having a first digitally programmable transconductance and a second push-pull output configured to generate a second output stage current at the second push-pull output based on the first digitally programmable transconductance, the output stage source current control signal, and the output stage sink current control signal; and

a control interface configured to:

receive at least one control input; and

set the first digitally programmable transconductance based on the at least one control input.

416. The operational amplifier of claim 415 wherein the second push-pull output stage includes:

an array of programmable mirrored source current elements in communication with the control interface; and

an array of programmable mirrored sink current elements in communication with the control interface, and configured to be in communication with the array of programmable mirrored sink current elements to form the second push-pull output.

417. The operational amplifier of claim 416 wherein:

the array of programmable mirrored source current elements includes a plurality of binary weighted programmable source current elements; and

the array of programmable mirrored sink current elements includes a plurality of binary weighted programmable sink current elements.

418. The operational amplifier of claim 417 wherein the first push-pull output stage further includes:

a first push-pull PFET transistor having a gate configured to receive the output stage source current control signal, a source in communication with a supply voltage, and a drain in communication with the first push-pull output; and

a first push-pull NFET transistor having a gate configured to receive the output stage sink current control signal, a source in communication with a reference voltage, and a drain in communication with the first push-pull output.

419. The operational amplifier of claim 418 wherein a channel width of the first push-pull PFET transistor and a channel width of the first push-pull NFET transistor are configured such that a current sourcing capacity of the first push-pull PFET transistor is substantially matched to a current sinking capacity of the first push-pull NFET transistor.

420. The operational amplifier of claim 418 wherein the second push-pull output stage further includes:

an offset current PFET transistor having an offset current sourcing capacity, and including a gate in communication with the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain in communication with the second push-pull output; and

an offset current NFET transistor having an offset current sinking capacity substantially matched to the offset current sourcing capacity of the offset current PFET transistor, and including a gate in communication with the first push-pull

NFET transistor, a source in communication with the reference voltage, and a drain in communication with the second push-pull output.

421. The operational amplifier of claim 418 wherein:

each of the plurality of binary weighted programmable source current elements is current mirrored to the first push-pull PFET transistor; and

each of the plurality of binary weighted programmable sink current elements is current mirrored to the first push-pull NFET transistor.

422. The operational amplifier of claim 421 wherein:

each of the plurality of binary weighted programmable source current elements and each of the plurality of binary weighted programmable sink current elements are in communication with the control interface; and

each of the plurality of binary weighted programmable source current elements and each of the plurality of binary weighted programmable sink current elements are configured to be in one of an on state and an off state as a function of the first digitally programmable transconductance.

423. The operational amplifier of claim 422 wherein each binary weighted programmable source current element of the plurality of binary weighted programmable source current elements is associated with a respective binary weighted programmable sink current element of the plurality of binary weighted programmable sink current elements.

424. The operational amplifier of claim 423 wherein the binary weighted programmable source current element and the respective binary weighted programmable sink current element associated with the binary weighted programmable source current element are configured such that a current sourcing capacity of the binary weighted programmable source current element is substantially equivalent to a current sinking capacity of the respective binary weighted programmable sink current element.

425. The operational amplifier of claim 418 wherein:

the plurality of binary weighted programmable source current elements includes "N" number of binary weighted programmable source current elements such that

for "n" having an integer value between 1 and "N", inclusive, each of an n^{th} binary weighted programmable source current element of the plurality of binary weighted programmable source current elements includes:

an n^{th} binary weighted PFET transistor having a channel width, a gate in communication with the gate of the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain, and configured to provide a current sourcing capacity based on the channel width of the n^{th} binary weighted PFET transistor; and

an n^{th} control PFET transistor having a gate in communication with the control interface, a source in communication with the drain of the n^{th} binary weighted PFET transistor, and a drain in communication with the second push-pull output, and configured to be in one of an on state and an off state as based on the first digitally programmable transconductance.

426. The operational amplifier of claim 425 wherein:

the channel width of each n^{th} binary weighted programmable source current element of the plurality of binary weighted programmable source current elements is interrelated such that for "n" having an integer value between 2 and "N", inclusive, the channel width of the n^{th} binary weighted PFET transistor and the channel width of the $(n-1)^{th}$ binary weighted PFET transistor are configured such that the current sourcing capacity of the n^{th} binary weighted PFET transistor of the n^{th} binary weighted programmable source current element is substantially equal to twice the current sourcing capacity of the $(n-1)^{th}$ binary weighted PFET transistor of an $(n-1)^{th}$ binary weighted programmable source current element.

427. The operational amplifier of claim 425 wherein:

the plurality of binary weighted programmable sink current elements includes "N" number of binary weighted programmable sink current elements such that for "n" having an integer value between 1 and "N", inclusive, each n^{th} binary weighted programmable sink current element of the plurality of binary weighted programmable sink elements includes:

an n^{th} binary weighted NFET transistor having a channel width, a gate in communication with the gate of the first push-pull NFET transistor, a source in communication with the supply voltage, and a drain, and configured to provide a current sinking capacity based on the channel width of the n^{th} binary weighted NFET transistor;

an n^{th} control NFET transistor having a gate in communication with the control interface, a source in communication with the drain of the n^{th} binary weighted NFET transistor, and a drain in communication with the second push-pull output, and configured to be in one of an on state and an off state as based on the first digitally programmable transconductance.

428. The operational amplifier of claim 427 wherein:

the channel width of each n^{th} binary weighted programmable sink current element of the plurality of binary weighted programmable sink current elements is interrelated such that for "n" having the integer value between 2 and N, inclusive, the channel width of the n^{th} binary weighted NFET transistor and a channel width of an $(n-1)^{th}$ binary weighted NFET transistor are configured such that the current sourcing capacity of the n^{th} binary weighted NFET transistor of the n^{th} binary weighted programmable sink current element is substantially equal to twice the current sourcing capacity of the $(n-1)^{th}$ binary weighted NFET transistor of the $(n-1)^{th}$ binary weighted programmable sink current element.

429. The operational amplifier of claim 428 wherein for "n" having the integer value between 1 and "N", inclusive, the channel width of the n^{th} binary weighted PFET transistor and the channel width of the n^{th} binary weighted NFET transistor are configured such that the current sourcing capacity of the n^{th} binary weighted

PFET transistor is substantially equal to the current sourcing capacity of the n^{th} binary weighted NFET transistor.

430. The operational amplifier of claim 427 wherein for "n" having the integer value between 1 and "N", inclusive, the gate of the n^{th} control PFET transistor is configured to receive an n^{th} control PFET transistor signal from the control interface and the gate of the n^{th} control NFET transistor is configured to receive an n^{th} control NFET transistor signal from the control interface based on the first digitally programmable transconductance.

431. The operational amplifier of claim 430 further comprising a third push-pull output stage in communication with the control interface and including:

a second digitally programmable transconductance;

a plurality of binary weighted programmable sense source current elements in communication with the gate of the first push-pull PFET transistor; and

a plurality of binary weighted programmable sense sink current elements in communication with the gate of the first push-pull NFET transistor; and

wherein the plurality of binary weighted programmable sense source current elements are configured to be in communication with the plurality of binary weighted programmable sense sink current elements to form a third push-pull output.

432. The operational amplifier of claim 431 wherein each of the plurality of binary weighted programmable sense source current elements and each of the plurality of binary weighted programmable sense sink current elements are configured to be in one of an on state and an off state as a function of the second digitally programmable transconductance.

433. The operational amplifier of claim 432 wherein the control interface is further configured to set the second digitally programmable transconductance based on at least a portion of the at least one control input.

434. The operational amplifier of claim 431 wherein each binary weighted programmable sense source current element of the plurality of binary weighted programmable sense source current elements is associated with a respective binary weighted programmable sense sink current element of the plurality of binary weighted programmable sense sink current elements.

435. The operational amplifier of claim 434 wherein the binary weighted programmable sense source current element and the respective binary weighted programmable sense sink current element associated with the binary weighted programmable sense source current element are configured such that a current sourcing capacity of the binary weighted programmable sense source current element is substantially equivalent to a current sinking capacity of the respective binary weighted programmable sense sink current element.

436. The operational amplifier of claim 431 wherein:

the plurality of binary weighted programmable sense source current elements includes "M" number of binary weighted programmable sense source current elements such that for "m" having an integer value between 1 and "M", inclusive, each m^{th} binary weighted programmable sense source current element of the plurality of binary weighted programmable sense source current elements includes:

an m^{th} binary weighted sense PFET transistor having a channel width, a gate in communication with the gate of the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain, and configured to provide a current sourcing capacity based on the channel width of the m^{th} binary weighted sense PFET transistor;

an m^{th} control sense PFET transistor having a gate in communication with the control interface, a source in communication with the drain of the m^{th} binary weighted sense PFET transistor, and a drain in communication with the third push-pull output, and configured to be in one of an on state and an off state as based on the second digitally programmable transconductance.

437. The operational amplifier of claim 436 wherein:

the channel width of each m^{th} binary weighted programmable sense source current element of the plurality of binary weighted programmable sense source current elements is interrelated such that for "m" having an integer value between 2 and "M", inclusive, the channel width of the m^{th} binary weighted sense PFET transistor and the channel width of an $(m-1)^{th}$ binary weighted sense PFET transistor are configured such that the current sourcing capacity of the m^{th} binary weighted sense PFET transistor of the m^{th} binary weighted programmable sense source current elementis substantially equal to twice the current sourcing capacity of the $(m-1)^{th}$ binary weighted sense PFET transistor of an $(m-1)^{th}$ binary weighted programmable sense source current element.

438. The operational amplifier of claim 437 wherein:

the plurality of binary weighted programmable sense sink current elements includes "M" number of binary weighted programmable sense sink current elements such that for "m" having an integer value between 1 and "M", inclusive, each m^{th} binary weighted programmable sense sink current element of the plurality of binary weighted programmable sense sink current elements includes:

an m^{th} binary weighted sense NFET transistor having a channel width, a gate in communication with the gate of the first push-pull NFET transistor, a source in communication with the supply voltage, and a drain, and configured to provide a current sinking capacity based on the channel width of the m^{th} binary weighted sense NFET transistor;

an m^{th} control sense NFET transistor having a gate in communication with the control interface, a source in communication with the drain of the m^{th} binary

weighted sense NFET transistor, and a drain in communication with the third push-pull output, and configured to be in one of an on state and an off state as based on the second digitally programmable transconductance.

439. The operational amplifier of claim 438 wherein:

for "m" having the integer value between 1 and "M", inclusive, the gate of the m^{th} control sense PFET transistor is configured to receive an m^{th} control sense PFET transistor signal from the control interface and the gate of the m^{th} control sense NFET transistor is configured to receive an m^{th} control sense NFET transistor signal from the control interface based on the second digitally programmable transconductance.

440. The operational amplifier of claim 438 wherein for "m" having the integer value between 2 and "M", inclusive, the channel width of the m^{th} binary weighted sense NFET transistor of an m^{th} binary weighted programmable sense sink current element and the channel width of an $(m-1)^{th}$ binary weighted sense NFET transistor of an $(m-1)^{th}$ binary weighted programmable sense sink current element are configured such that the current sourcing capacity of the m^{th} binary weighted sense NFET transistor is substantially equal to twice the current sourcing capacity of the $(m-1)^{th}$ binary weighted sense NFET transistor.

441. The operational amplifier of claim 438 wherein for "m" having the integer value between 1 and "M", inclusive, the channel width of the m^{th} binary weighted sense PFET transistor of the m^{th} binary weighted programmable sense source current element and the channel width of the m^{th} binary weighted sense NFET transistor of the m^{th} binary weighted programmable sense sink current element are configured such that the current sourcing capacity of the m^{th} binary weighted sense PFET transistor is substantially equal to the current sourcing capacity of the m^{th} binary weighted sense NFET transistor.

442. The operational amplifier of claim 441 wherein for "m" equal to "M" and "n" equal to N, the channel width of the m^{th} binary weighted sense PFET transistor and the channel width of the m^{th} binary weighted sense NFET transistor are further configured such that the current sourcing capacity of the m^{th} binary weighted sense PFET transistor and the current sinking capacity of the m^{th} binary weighted sense NFET transistor are fractionally related by a sense scaling factor to the current sourcing capacity of the n^{th} binary weighted PFET transistor and the current sinking capacity of the n^{th} binary weighted NFET transistor, respectively.

443. The operational amplifier of claim 441 wherein "N" > "M".

444. The operational amplifier of claim 443 wherein:

the second digitally programmable transconductance is a function of the first digitally programmable transconductance; and

for "m" having the integer value between 1 and "M", inclusive, "n" equals "m" plus "N" - "M", the gate of the m^{th} control sense PFET transistor is configured to receive the n^{th} control PFET transistor signal from the control interface and the gate of the m^{th} control sense NFET transistor is configured to receive the n^{th} control NFET transistor signal from the control interface.

445. The operational amplifier of claim 443 wherein "M" = 5 and "N" = 6.

446. The operational amplifier of claim 431 further comprising an operational amplifier output isolation circuit including a high impedance input in communication with the first push-pull output and an isolated feedback node configured to provide a feedback voltage based on a first push-pull output voltage generated at the first push-pull output, wherein the isolated feedback node is configured to substantially isolate the first push-pull output from a feedback network impedance.

447. The operational amplifier of claim 446 wherein the operational amplifier output isolation circuit includes:

a first NFET transistor having a gate in communication with the high impedance input, a drain in communication with the supply voltage, and a source in communication with the isolated feedback node; and

a second NFET transistor having a gate in communication with a bias voltage, a drain in communication with the isolated feedback node, and a source in communication with the reference voltage.

448. The operational amplifier of claim 447 further comprising a transconductance bias circuit having a transconductance setting impedance and coupled between the first push-pull output and the reference voltage.

449. The operational amplifier of claim 448 wherein the transconductance bias circuit includes a bias resistor having a bias resistor resistance and a bias capacitor having a bias capacitor capacitance coupled in series, wherein the transconductance setting impedance is substantially equal to the bias resistor resistance plus a bias capacitor impedance based on the bias capacitor capacitance.

450. The operational amplifier of claim 431 wherein:

the second push-pull output stage further includes:

an offset current PFET transistor having a channel width, and including a gate in communication with the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain in communication with the second push-pull output;

an offset current NFET transistor having a channel width, a gate in communication with the first push-pull NFET transistor, a source in communication with the reference voltage, and a drain in communication with the second push-pull output; and

wherein the channel width of the offset current PFET transistor and the channel width of the offset current NFET transistor are configured such that a current sinking capacity of the offset current PFET transistor is substantially matched to a current sinking capacity of the offset current NFET transistor;

the third push-pull output stage further includes:

an offset sense current PFET transistor having a channel width, a gate in communication with the first push-pull PFET transistor, a source in communication with the supply voltage, and a drain in communication with the second push-pull output; and

an offset sense current NFET transistor having a channel width, a gate in communication with the first push-pull NFET transistor, a source in communication with the reference voltage, and a drain in communication with the second push-pull output; and

wherein the channel width of the offset sense current PFET transistor and the channel width of the offset sense current NFET transistor are configured such that the current sinking capacity of the offset sense current PFET transistor and the current sourcing capacity of the offset sense current NFET transistor are fractionally related by a sense scaling factor to the current sourcing capacity of the offset current PFET transistor and the offset current NFET transistor, respectively.

451. The operational amplifier of claim 450 wherein the third push-pull output stage is configured such that the second digitally programmable transconductance has a minimum transconductance value that is fractionally related by the sense scaling factor to a minimum transconductance value of the first digitally programmable transconductance.

452. The operational amplifier of claim 415 wherein the second push-pull output stage is configured such that the first digitally programmable transconductance has a minimum transconductance value.

453. The operational amplifier of claim 452 wherein the first digitally programmable transconductance may be configured to provide at least 64 transconductance values.

454. The operational amplifier of claim 415 further comprising:

a third push-pull output stage including a second digitally programmable transconductance, a third push-pull output, and configured to generate a third output stage current at the third push-pull output based on the second digitally programmable transconductance, the output stage source current control signal, and the output stage sink current control signal.

455. The operational amplifier of claim 454 wherein the control interface is in communication with the third push-pull output stage, and configured to set the second digitally programmable transconductance based on at least a portion of the at least one control input.

456. The operational amplifier of claim 455 wherein the second digitally programmable transconductance is substantially related to the first digitally programmable transconductance by a sense scaling factor.

457. The operational amplifier of claim 456 wherein:

the second push-pull output stage is configured such that the first digitally programmable transconductance has a minimum transconductance value; and

the third push-pull output stage is configured such that the second digitally programmable transconductance has a minimum transconductance value that is substantially related to the minimum transconductance value of the first digitally programmable transconductance by a sense scaling factor.

458. The operational amplifier of claim 457 wherein:

the first digitally programmable transconductance may be configured to provide 64 transconductance values; and

the second digitally programmable transconductance may be configured to provide 32 transconductance values.

459. The operational amplifier of claim 454 further comprising an operational amplifier output isolation circuit including a high impedance input in communication with the first push-pull output and an isolated feedback node configured to provide a feedback voltage based on a first push-pull output voltage generated at the first push-pull output, wherein the isolated feedback node is configured to substantially isolate the first push-pull output from a feedback network impedance.

460. The operational amplifier of claim 459 wherein the operational amplifier output isolation circuit includes:

a first NFET transistor having a gate in communication with the high impedance input, a drain in communication with a supply voltage, and a source in communication with the isolated feedback node; and

a second NFET transistor having a gate in communication with a bias voltage, a drain in communication with the isolated feedback node, and a source in communication with a reference voltage.

461. The operational amplifier of claim 460 further comprising a transconductance bias circuit having a transconductance setting impedance and coupled between the first push-pull output and the reference voltage.

462. A rechargeable parallel amplifier circuit comprising:

a charge storage capacitor including a first node configured to provide a charge storage capacitor voltage and a second node in communication with a reference voltage;

a parallel amplifier output configured to provide a parallel amplifier output voltage;

a first PFET transistor having a minimum PFET headroom voltage and including a source in communication with the first node of the charge storage capacitor, a drain in communication with the parallel amplifier output, and a gate, and configured to discharge the charge storage capacitor as a function of the parallel amplifier output voltage, the charge storage capacitor voltage, and the minimum PFET headroom voltage to generate a parallel amplifier output current; and

a first NFET transistor having a minimum NFET headroom voltage and including a source in communication with the first node of the charge storage capacitor, a drain in communication with the parallel amplifier output, and a gate, and configured to charge the charge storage capacitor as a function of the parallel amplifier output voltage, the charge storage capacitor voltage, and the minimum NFET headroom voltage to generate the parallel amplifier output current.

463. The rechargeable parallel amplifier circuit of claim 462 further comprising:

an output control circuit configured to:

receive the parallel amplifier output voltage and the charge storage capacitor voltage;

determine whether the charge storage capacitor voltage is at least greater than a sum of the parallel amplifier output voltage and the minimum PFET headroom voltage; and

enable the first PFET transistor to generate the parallel amplifier output voltage based on a determination that the charge storage capacitor voltage is at least greater than the sum of the parallel amplifier output voltage and the minimum PFET headroom voltage.

464. The rechargeable parallel amplifier circuit of claim 463 wherein the output control circuit is further configured to:

determine whether the parallel amplifier output voltage is at least greater than a sum of the minimum NFET headroom voltage and the charge storage capacitor voltage; and

enable the first NFET transistor to generate the parallel amplifier output current based on a determination that the parallel amplifier output voltage is at least greater than the sum of the minimum NFET headroom voltage and the charge storage capacitor voltage.

465. The rechargeable parallel amplifier circuit of claim 464 further comprising:

a first amplifier including a first amplifier non-inverting input configured to receive an input signal, a first amplifier inverting configured to receive a feedback signal, and a first amplifier output in communication with the gate of the first PFET transistor; and

a second amplifier including a second amplifier non-inverting input configured to receive an input signal, a second amplifier inverting input configured to receive a feedback signal, and a second amplifier output in communication with the gate of the first NFET transistor.

466. The rechargeable parallel amplifier circuit of claim 465 wherein the first PFET transistor is further configured to generate the parallel amplifier output current based on the first amplifier output of the first amplifier; and

the first NFET transistor is further configured to generate the parallel amplifier output current based on the second amplifier output of the second amplifier.

467. The rechargeable parallel amplifier circuit of claim 466 wherein the parallel amplifier output stage further comprises a second PFET transistor including a source in communication with a supply voltage, a drain in communication with the parallel amplifier output, and a gate in communication with the first amplifier output of the first amplifier, and configured to generate the parallel amplifier output current based on the first amplifier output of the first amplifier; and

wherein the output control circuit is further configured to disable the second PFET transistor from generating the parallel amplifier output current based on the determination that the charge storage capacitor voltage is at least greater than the sum of the parallel amplifier output voltage and the minimum PFET headroom voltage.

468. The rechargeable parallel amplifier circuit of claim 467 further comprising:

a second NFET transistor including a source in communication with the reference voltage, a drain in communication with the parallel amplifier output, and a gate in communication with the second amplifier output of the second amplifier, and configured to generate the parallel amplifier output current based on the second amplifier output of the second amplifier; and

wherein the output control circuit is further configured to disable the second NFET transistor from generating the parallel amplifier output current based on the determination that the parallel amplifier output voltage is at least greater than the sum of the minimum NFET headroom voltage and the charge storage capacitor voltage.

469. A rechargeable parallel amplifier circuit for governing a power supply voltage for a linear radio frequency power amplifier comprising:

a parallel amplifier output having a parallel amplifier output voltage;

a charge storage capacitor including a first node configured to provide a charge storage capacitor voltage and a second node in communication with a reference voltage;

a first NFET transistor having a minimum NFET headroom voltage and including a source in communication with the first node of the charge storage capacitor, a drain configured to receive a power amplifier supply voltage from a power amplifier supply output, and a gate, and configured to charge the charge storage capacitor from the power amplifier supply output as a function of the power amplifier supply voltage, the charge storage capacitor voltage, and the

minimum NFET headroom voltage to regulate the power amplifier supply voltage; and

a first PFET transistor having a minimum PFET headroom voltage and including a source in communication with the first node of the charge storage capacitor, a drain in communication with the parallel amplifier output, and a gate, and configured to discharge the charge storage capacitor as a function of the parallel amplifier output voltage, the charge storage capacitor voltage, and the minimum PFET headroom voltage to generate a parallel amplifier output current.

470. The rechargeable parallel amplifier circuit of claim 469 further comprising an output control circuit is further configured to:

receive the power amplifier supply voltage and the charge storage capacitor voltage;

determine whether the power amplifier supply voltage is at least greater than a sum of the minimum NFET headroom voltage and the charge storage capacitor voltage; and

enable the first NFET transistor to charge the charge storage capacitor from the power amplifier supply voltage based on a determination that the power amplifier supply voltage is at least greater than the sum of the minimum NFET headroom voltage and the charge storage capacitor voltage.

471. The rechargeable parallel amplifier circuit of claim 470 further comprising:

a first amplifier including a first amplifier non-inverting input configured to receive an input signal, a first amplifier inverting configured to receive the power amplifier supply voltage, and a first amplifier output in communication with the gate of the first PFET transistor; and

a second amplifier including a second amplifier non-inverting input configured to receive an input signal, a second amplifier inverting input configured to receive the power amplifier supply voltage, and a second amplifier output in communication with the gate of the first NFET transistor.

472. The rechargeable parallel amplifier circuit of claim 471 wherein the first NFET transistor is further configured to sink a current from the power amplifier supply voltage based on the second amplifier output of the second amplifier to regulate the power amplifier supply voltage.

473. The rechargeable parallel amplifier circuit of claim 471 further comprising:

an output control circuit further configured to:

receive the parallel amplifier output voltage; and

determine whether the charge storage capacitor voltage is at least greater than a sum of the parallel amplifier output voltage and the minimum PFET headroom voltage; and

enable the first PFET transistor to generate the parallel amplifier output voltage based on a determination that the charge storage capacitor voltage is at least greater than the sum of the parallel amplifier output voltage and the minimum PFET headroom voltage.

474. The rechargeable parallel amplifier circuit of claim 473 wherein the first PFET transistor is further configured to apply the parallel amplifier output current to the power amplifier supply output from the charge storage capacitor based on the first amplifier output of the first amplifier to regulate the power amplifier supply voltage.

475. The rechargeable parallel amplifier circuit of claim 473 further comprising:

a second NFET transistor including a source in communication with the reference voltage, a drain in communication with the parallel amplifier output, and a gate in communication with the second amplifier output of the second amplifier, and configured to generate the parallel amplifier output current as a function of the second amplifier output of the second amplifier; and

wherein the output control circuit is further configured to disable the second NFET transistor from generating the parallel amplifier output current based on the determination that the power amplifier supply voltage is at least

greater than the sum of the minimum NFET headroom voltage and the charge storage capacitor voltage.

476. The rechargeable parallel amplifier circuit of claim 475 further comprising a second PFET transistor including a source in communication with a supply voltage, a drain in communication with the parallel amplifier output, and a gate in communication with the first amplifier output of the first amplifier, and configured to generate the parallel amplifier output current as a function of the first amplifier output of the first amplifier; and

wherein the output control circuit is further configured to disable the second PFET transistor from generating the parallel amplifier output current based on the determination that the charge storage capacitor voltage is at least greater than the sum of the parallel amplifier output voltage and the minimum PFET headroom voltage.

477. The rechargeable parallel amplifier circuit of claim 476 wherein the second PFET transistor and the second NFET transistor apply the parallel amplifier output current to the power amplifier supply output to regulate the power amplifier supply voltage.

478. A programmable delay circuit comprising:

- a bias reference and mirror circuit configured to generate a bias reference current that tracks a change in a propagation delay between a switcher control circuit and a switching voltage output of a switch mode power supply converter as a function of temperature; and
- a variable delay circuit including:
  - a variable capacitor having a variable capacitor voltage; and
  - an output buffer stage including an output buffer output, an output buffer input having a logic low threshold voltage that is substantially proportional to a supply voltage and a logic

high threshold voltage that is substantially proportional to the supply voltage; and configured to:

- generate a logic high output voltage at the output buffer output in response to the variable capacitor voltage falling below the logic low threshold voltage; and
- generate a logic low output voltage at the output buffer output in response to the variable capacitor voltage exceeding the logic high threshold voltage; and

▪ the variable delay circuit configured to generate a capacitor current in the variable capacitor based on the bias reference current to provide a programmable delay period that substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as the function of temperature.

479. The programmable delay circuit of claim 478 further comprising:

a voltage reference circuit configured to generate a bias reference voltage that substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as the function of temperature; and

wherein the bias reference and mirror circuit is further configured to generate the bias reference current based on the bias reference voltage.

480. The programmable delay circuit of claim 479 wherein:

the voltage reference circuit is further configured to generate the bias reference voltage that also substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as a function of the supply voltage.

481. The programmable delay circuit of claim 478 wherein the variable delay circuit is further configured to:

source a first bias current that is substantially proportional to the bias reference current to the variable capacitor in order to charge the variable capacitor; and

sink a second bias current that is substantially proportional to the bias reference current to the variable capacitor in order to discharge the variable capacitor.

482. The programmable delay circuit of claim 481 wherein the first bias current is substantially equal to the second bias current.

483. The programmable delay circuit of claim 481 wherein:

the variable capacitor includes a first node configured to provide the variable capacitor voltage and a second node in communication with a reference voltage; and

the variable delay circuit includes:

a first PFET transistor having a gate, a source in communication with the supply voltage, and a drain, and configured to generate a first PFET drain current from the drain of the first PFET transistor substantially equal to the first bias current; and

a second PFET transistor having a gate configured to receive an input signal voltage, a source in communication with the drain of the first PFET transistor, and a drain in communication with the first node of the variable capacitor, and configured to source the first bias current to generate the capacitor current of the variable capacitor in response to the input signal voltage falling below a logic low output voltage.

484. The programmable delay circuit of claim 483 wherein the variable delay circuit further includes:

a first NFET transistor having a gate, a source in communication with the reference voltage, and a drain, and configured to generate a first NFET drain current at the drain of the first NFET transistor substantially equal to the second bias current; and

a second NFET transistor having a gate configured to receive the input signal voltage, a source in communication with the drain of the first NFET transistor, and a drain in communication with the first node of the variable capacitor, and configured to sink the second bias current to generate the capacitor current of the variable capacitor in response to the input signal voltage rising above a logic high output voltage.

485. The programmable delay circuit of claim 484 wherein the bias reference and mirror circuit further includes:

a third NFET transistor having a source in communication with the reference voltage, and a drain, and a gate in communication with the drain of the third NFET transistor and the gate of the first NFET transistor, and configured to sink a third NFET drain current into the drain of the third NFET transistor;

a fourth NFET transistor having a gate in communication with the drain and the gate of the third NFET transistor, the source in communication with the reference voltage, and a drain configured to generate a fourth NFET drain current into the drain of the fourth NFET transistor that is substantially proportional to the drain current of the third NFET transistor;

and a third PFET transistor having a source in communication with the supply voltage, a gate in communication with the gate of the first PFET transistor, and a drain in communication with the gate of the third PFET transistor and the drain of the fourth NFET transistor, and configured to generate a third PFET drain current from the drain of the third PFET transistor substantially equal to the fourth NFET drain current of the fourth NFET transistor; and

wherein the bias reference and mirror circuit is further configured to generate the third NFET drain current into the drain of the third NFET transistor substantially equal to the bias reference current.

486. The programmable delay circuit of claim 485 wherein the first NFET transistor is configured to generate the first NFET drain current at the drain of the first NFET transistor that is substantially proportional to the third NFET drain current of the third NFET transistor.

487. The programmable delay circuit of claim 486 further comprising:

the voltage reference circuit including:

a first resistor having a first resistance, a first node in communication with the supply voltage and a second node;

a second resistor having a second resistance substantially equal to the first resistance of the first resistor, a first node and a second node in communication with the reference voltage;

a fourth PFET transistor having a source in communication with the second node of the second resistor, a gate, and a drain in communication with the gate of the fourth PFET transistor;

a fifth PFET transistor having a source in communication with the gate and the drain of the fourth PFET transistor, a gate, and a drain in communication with the gate of the fifth PFET transistor and the first node of the second resistor; and wherein a source voltage on the source of the second PFET transistor is substantially equal to one-half the supply voltage; and

a compensation current source having a first node coupled to the drain of the fourth PFET transistor, and configured to generate a compensation current proportional to the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as the function of temperature and the function of the supply voltage to generate the bias reference voltage on the source of the fifth PFET transistor;

wherein:

the bias reference and mirror current circuit includes:

a sixth PFET transistor having a gate in communication with the gate of the fifth PFET transistor, a drain in communication with the drain and the gate of

the third NFET transistor, and a source, and configured to have a source voltage on the source of the sixth PFET transistor substantially equal to the bias reference voltage on the source of the second PFET transistor; and

a third resistor having a third resistance, a first node in communication with the supply voltage and a second node in communication with the source of the sixth PFET transistor; and

the bias reference current is substantially equal to the supply voltage less the bias reference voltage on the source of the sixth PFET transistor divided by the third resistance.

488. The programmable delay circuit of claim 487 wherein the compensation current source is configured to increase the compensation current proportional to an increase in temperature.

489. The programmable delay circuit of claim 487 wherein the compensation current source includes a proportional to absolute temperature current source.

490. The programmable delay circuit of claim 489 wherein the compensation current source includes a programmable resistor array to adjust a proportional to absolute temperature current generated by the proportional to absolute temperature current source.

491. The programmable delay circuit of claim 488 wherein the compensation current source is further configured to generate a portion of the compensation current proportional to an increase in the supply voltage.

492. The programmable delay circuit of claim 491 wherein the compensation current source further includes a programmable resistor array to adjust the current proportional to voltage current source circuit as the function of the supply voltage.

493. The programmable delay circuit of claim 487 wherein the compensation current source includes a current proportional to voltage current source circuit configured to generate a portion of the compensation current as the function of the supply voltage.

494. The programmable delay circuit of claim 493 wherein the current proportional to voltage current source circuit includes a band gap circuit.

495. The programmable delay circuit of claim 478 wherein the variable delay circuit is configured to provide the programmable delay period based on a variable capacitance of the variable capacitor.

496. The programmable delay circuit of claim 495 wherein the variable capacitor is a programmable capacitor array including a plurality of binary weighted capacitors.

497. The programmable delay circuit of claim 478 wherein the bias reference and mirror circuit is further configured to generate the bias reference current to track a change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as a function of a supply voltage.

498. The programmable delay circuit of claim 478 wherein the bias reference and mirror circuit is further configured to substantially track a change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as a function of a supply voltage.

499. A method for variably delaying a signal comprising:

receiving a digital logic level input signal having a digital logic input signal voltage to be variably delayed;

generating a bias reference current that substantially tracks a change in a propagation delay between a switcher control circuit and a switching voltage output of a switch mode power supply converter as a function of temperature;

generating a capacitor current in a variable capacitor based on the bias reference current and the digital logic input signal voltage to produce a variable capacitor voltage on the variable capacitor; and

changing an output voltage of an output buffer in response to the variable capacitor voltage being one of above a logic high threshold voltage of the output buffer and below a logic low threshold voltage of the output buffer.

500. The method for variably delaying the signal of claim 499 wherein generating the bias reference current that substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as the function of temperature comprises generating a compensation current with a current proportional to absolute temperature circuit.

501. The method for variably delaying the signal of claim 499 wherein generating the bias reference current that substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as the function of temperature comprises:

generating the bias reference current that substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as the function of temperature and a function of a supply voltage.

502. The method for variably delaying the signal of claim 501 wherein generating the bias reference current that substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage

output of the switch mode power supply converter as the function of temperature and the function of the supply voltage comprises:

generating a portion of the bias reference current with a band gap circuit.

503. The method for variably delaying the signal of claim 501 further comprising:

delaying the digital logic level input signal by a programmable delay period based on a variable capacitance of the variable capacitor and the bias reference current, wherein the programmable delay period substantially tracks the change in the propagation delay between the switcher control circuit and the switching voltage output of the switch mode power supply converter as the function of temperature and the function of the supply voltage.

504. The method for variably delaying the signal of claim 503 further comprising:

adjusting the variable capacitance of the variable capacitor to change the programmable delay period.

505. The envelope tracking control system of claim 4 further comprising:

- the pseudo envelope tracking control circuit further configured to
  - determine the gain control adjustment based on the transmit-gain setting difference; and
  - scale the magnitude of the input signal used to generate the modulated radio frequency input signal by the gain control adjustment to generate a gain control adjusted envelope magnitude signal.

506. The envelope tracking control system of claims 4-5 further comprising:

- a look up table including an index input, and output, and calibrated iso-gain contour data associated with the iso-gain contour, and configured to:
  - receive the gain control adjusted envelope magnitude signal

- provide a target voltage for the modulated power supply voltage as a function of the gain control adjusted envelope magnitude signal.

507. The envelope tracking control system of claim 3 further comprising:

- the pseudo envelope tracking control circuit further configured to:
  - obtain a temperature measurement of a transceiver configured to generate the modulated radio frequency input signal;
  - determine a calibrated temperature measurement of the transceiver during calibration of the iso-gain contour.
  - subtract calibrated temperature measurement from the temperature measurement to obtain a temperature difference;
  - based on the temperature difference, adjust the control signal to provided to the envelope tracking power converter.

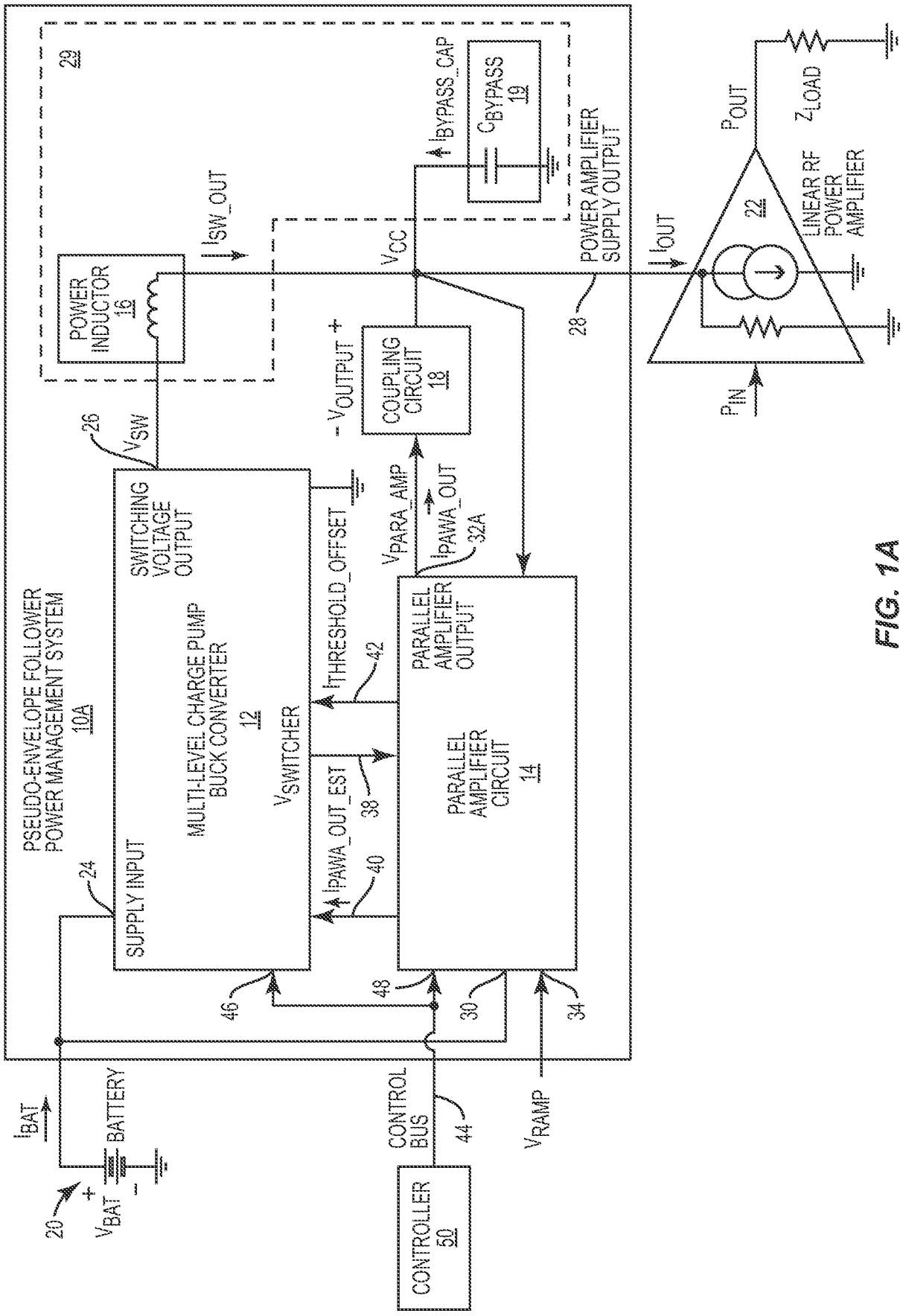

PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM
10A
SUPPLY INPUT
24
SWITCHING VOLTAGE OUTPUT
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER
12
VSWITCHER
26
VSW
POWER INDUCTOR
16
ISW_OUT
29
VCC
IBYPASS_CAP
CBYPASS
19
POWER AMPLIFIER SUPPLY OUTPUT
28
IOUT
POUT
ZLOAD
LINEAR RF POWER AMPLIFIER
22
PIN
- VOUTPUT +
COUPLING CIRCUIT
18
VPARA_AMP
IPAWA_OUT
32A
ITHRESHOLD_OFFSET
42
PARALLEL AMPLIFIER OUTPUT
IPAWA_OUT_EST
38
40
PARALLEL AMPLIFIER CIRCUIT
14
46
48
30
34
IBAT
BATTERY
20
VBAT
CONTROL BUS
44
CONTROLLER
50
VRAMP

FIG. 1A

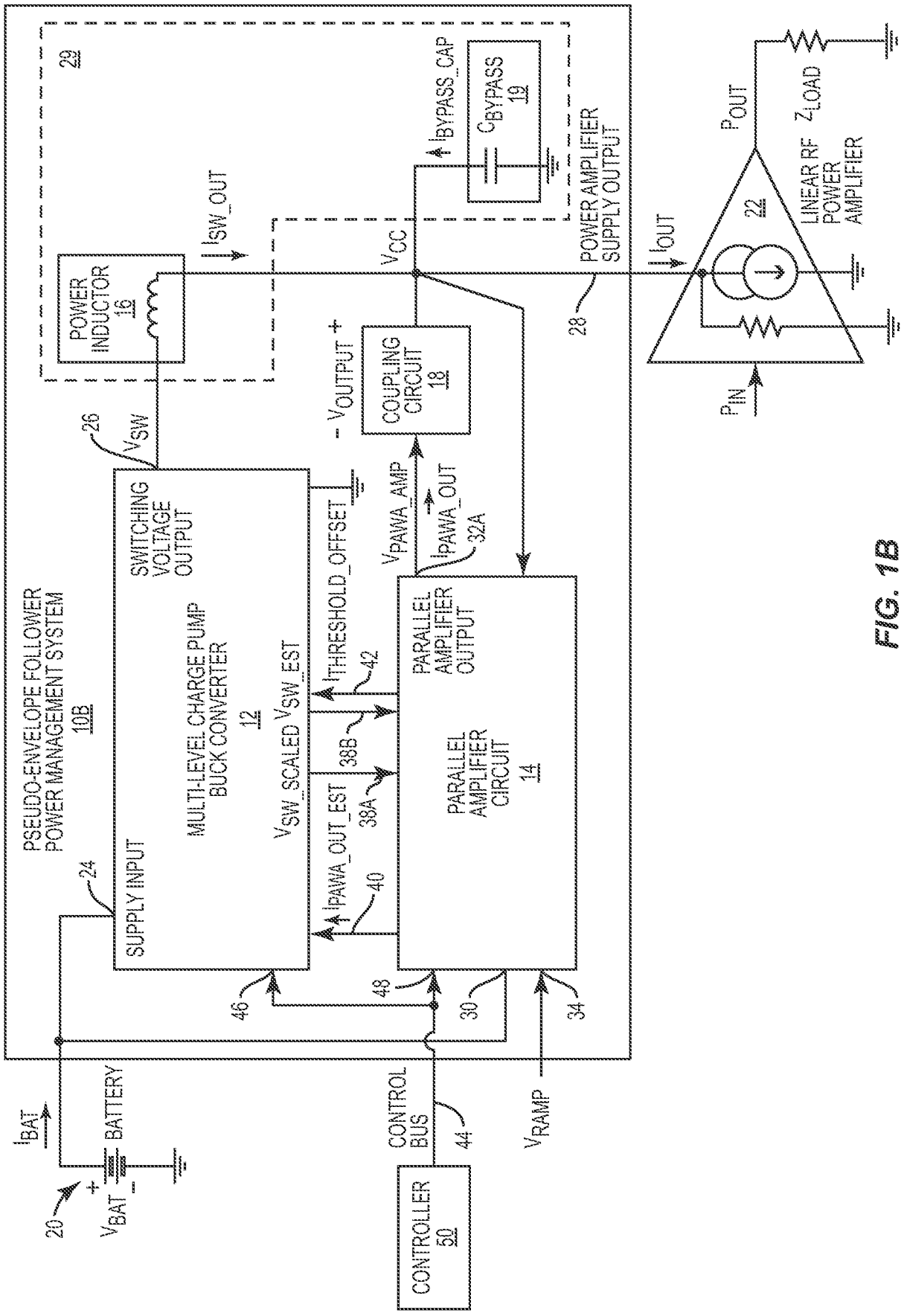

PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM
10B
SUPPLY INPUT
24
SWITCHING VOLTAGE OUTPUT
26
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER
12
PARALLEL AMPLIFIER CIRCUIT
14
PARALLEL AMPLIFIER OUTPUT
POWER INDUCTOR
16
COUPLING CIRCUIT
18
CBYPASS
19
POWER AMPLIFIER SUPPLY OUTPUT
29
28
LINEAR RF POWER AMPLIFIER
22
CONTROLLER
50
CONTROL BUS
44
BATTERY
20
IBAT
VBAT
ISW_OUT
VCC
IBYPASS_CAP
IOUT
POUT
ZLOAD
PIN
VSW
VSW_SCALED
VSW_EST
IPAWA_OUT_EST
38A
38B
40
ITHRESHOLD_OFFSET
42
VPAWA_AMP
IPAWA_OUT
32A
VOUTPUT
VRAMP
46
48
30
34

FIG. 1B

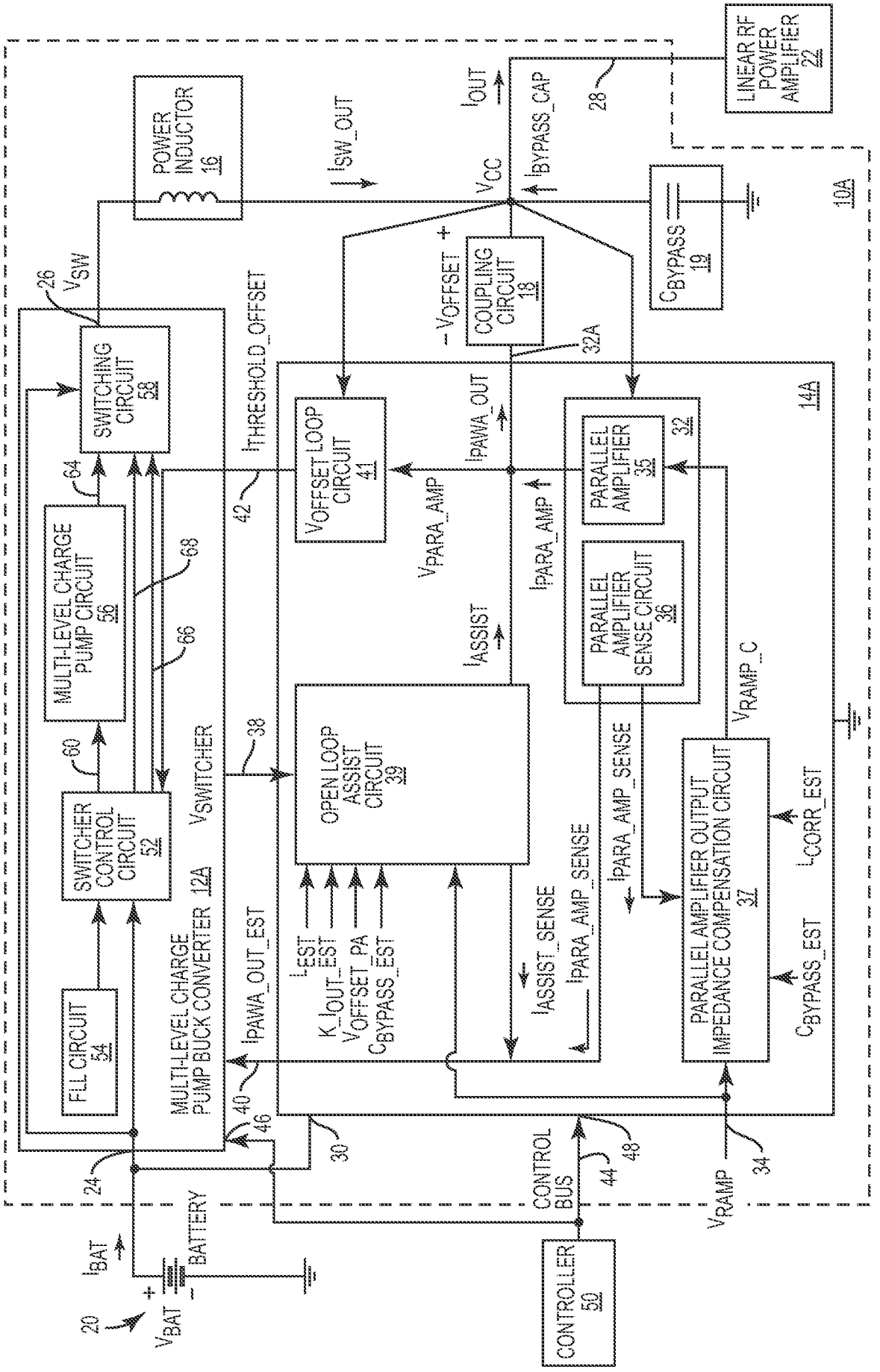

20
VBAT
BATTERY
IBAT
24
CONTROLLER 50
CONTROL BUS
44
48
VRAMP
34
30
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12A
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 52
60
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
66
68
SWITCHING CIRCUIT 58
26
VSW
POWER INDUCTOR 16
ISW_OUT
VSWITCHER
38
IPAWA_OUT_EST
40
46
LEST
K_IOUT_EST
VOFFSET_PA
CBYPASS_EST
OPEN LOOP ASSIST CIRCUIT 39
IASSIST_SENSE
IPARA_AMP_SENSE
IASSIST
VPARA_AMP
IPARA_AMP
PARALLEL AMPLIFIER SENSE CIRCUIT 36
PARALLEL AMPLIFIER 35
32
PARALLEL AMPLIFIER OUTPUT IMPEDANCE COMPENSATION CIRCUIT 37
VRAMP_C
LCORR_EST
CBYPASS_EST
14A
10A
VOFFSET LOOP CIRCUIT 41
42
ITHRESHOLD_OFFSET
IPAWA_OUT
VOFFSET
COUPLING CIRCUIT 18
32A
VCC
IOUT
IBYPASS_CAP
28
CBYPASS 19
LINEAR RF POWER AMPLIFIER 22

FIG. 2A

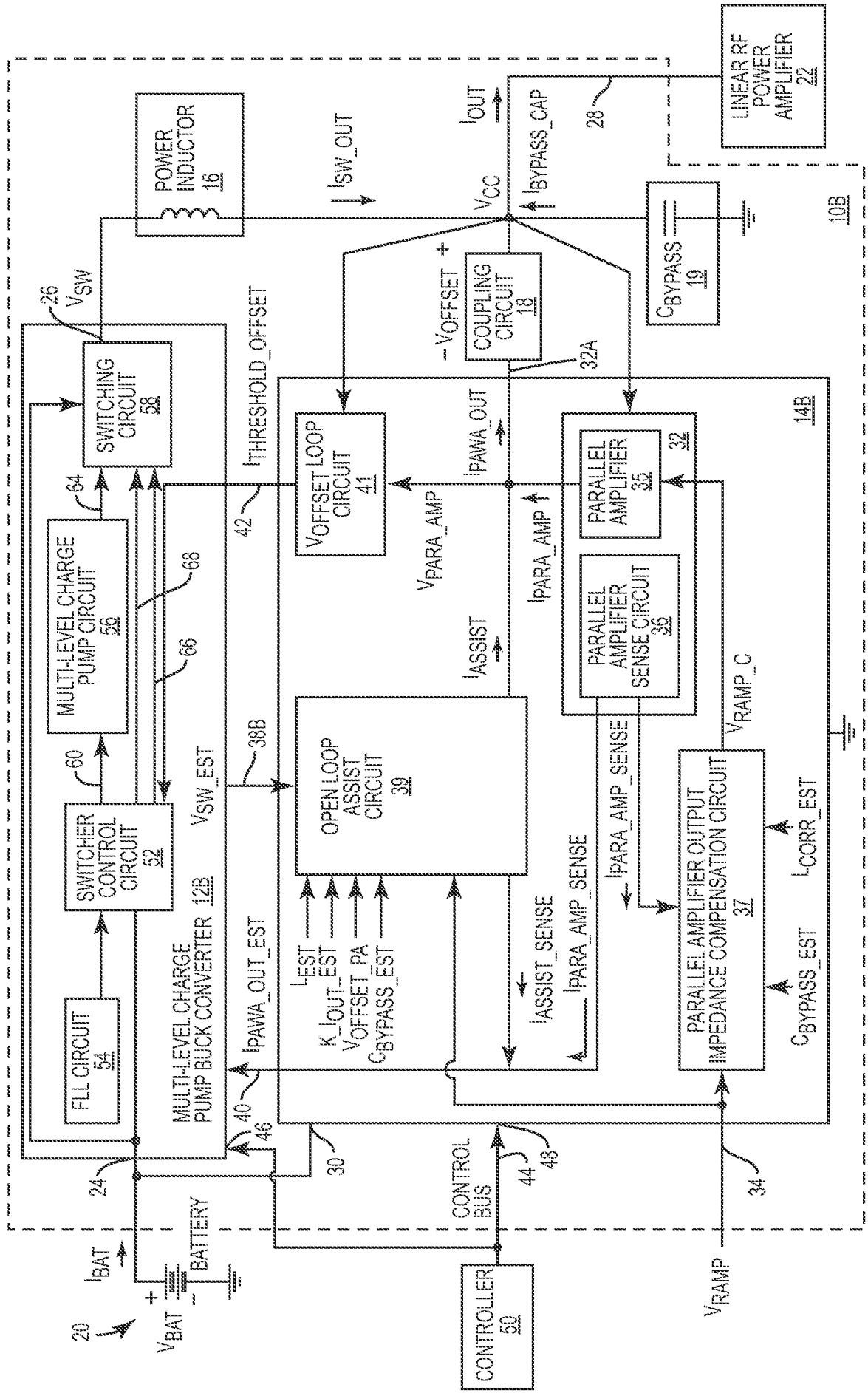

20
VBAT
BATTERY
IBAT
24
CONTROLLER 50
CONTROL BUS
44
48
30
46
40
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12B
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 52
60
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
SWITCHING CIRCUIT 58
26
VSW
68
66
VSW_EST
38B
OPEN LOOP ASSIST CIRCUIT 39
LEST
K_IOUT_EST
VOFFSET_PA
CBYPASS_EST
IPAWA_OUT_EST
IASSIST_SENSE
IPARA_AMP_SENSE
42
ITHRESHOLD_OFFSET
VOFFSET LOOP CIRCUIT 41
VPARA_AMP
IASSIST
IPAWA_OUT
IPARA_AMP
PARALLEL AMPLIFIER 35
32
PARALLEL AMPLIFIER SENSE CIRCUIT 36
14B
VRAMP_C
IPARA_AMP_SENSE
PARALLEL AMPLIFIER OUTPUT IMPEDANCE COMPENSATION CIRCUIT 37
LCORR_EST
CBYPASS_EST
34
VRAMP
POWER INDUCTOR 16
ISW_OUT
VCC
IOUT
IBYPASS_CAP
28
LINEAR RF POWER AMPLIFIER 22
10B
-VOFFSET +
COUPLING CIRCUIT 18
32A
CBYPASS 19

FIG. 2B

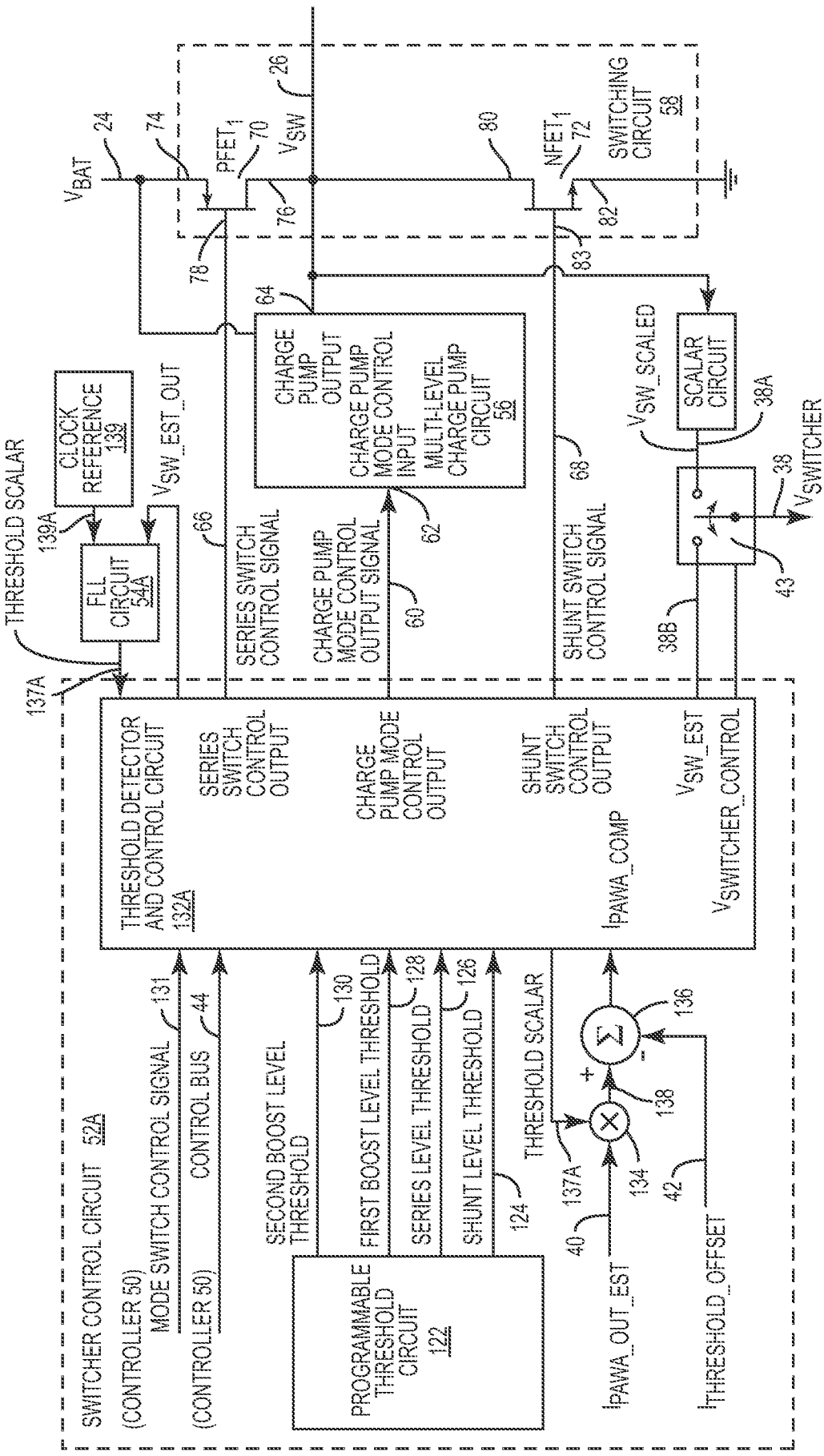

SWITCHER CONTROL CIRCUIT 52A
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD SCALAR
137A
139A
CLOCK REFERENCE 139
FLL CIRCUIT 54A
VSW_EST_OUT
66
SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
60
62
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
SHUNT SWITCH CONTROL SIGNAL
68
VSW_SCALED
SCALAR CIRCUIT
38A
38B
43
38
VSWITCHER
VBAT
24
74
PFET1
70
VSW
26
78
76
80
NFET1
72
SWITCHING CIRCUIT 58
82
83
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132A
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
IPAWA_COMP
VSWITCHER_CONTROL
PROGRAMMABLE THRESHOLD CIRCUIT 122
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
THRESHOLD SCALAR
137A
40
IPAWA_OUT_EST
134
138
136
42
ITHRESHOLD_OFFSET

FIG. 3A

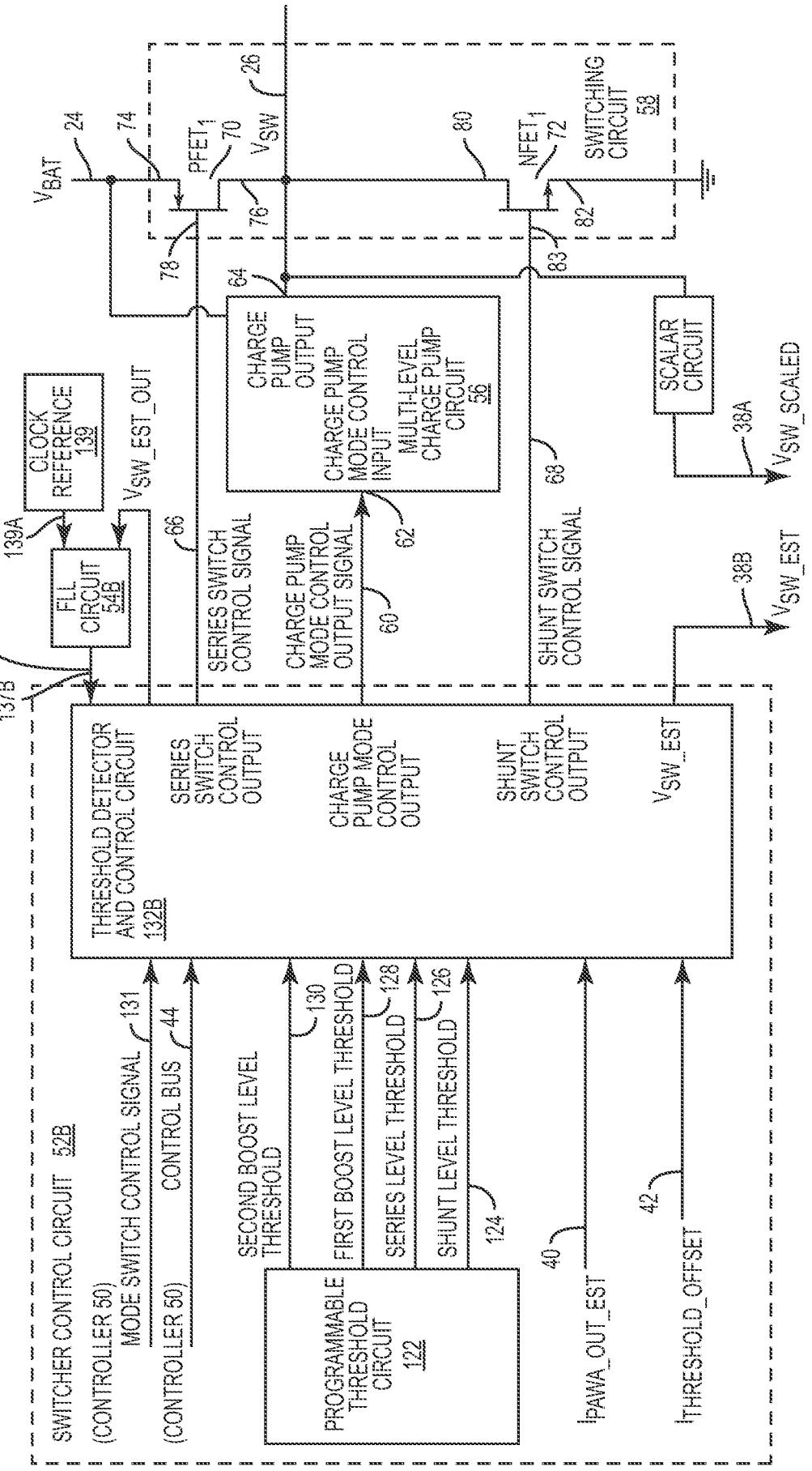

SWITCHER CONTROL CIRCUIT 52B
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD SCALAR'
137B
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132B
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
V_{SW_EST}
PROGRAMMABLE THRESHOLD CIRCUIT 122
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
40
$I_{PAWA_OUT_EST}$
42
$I_{THRESHOLD_OFFSET}$
CLOCK REFERENCE 139
139A
FLL CIRCUIT 54B
$V_{SW_EST_OUT}$
66
SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
60
62
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
SHUNT SWITCH CONTROL SIGNAL
68
SCALAR CIRCUIT
38A
V_{SW_SCALED}
38B
V_{SW_EST}
V_{BAT}
24
74
78
$PFET_1$
70
V_{SW}
26
76
80
$NFET_1$
72
82
83
SWITCHING CIRCUIT 58

FIG. 3B

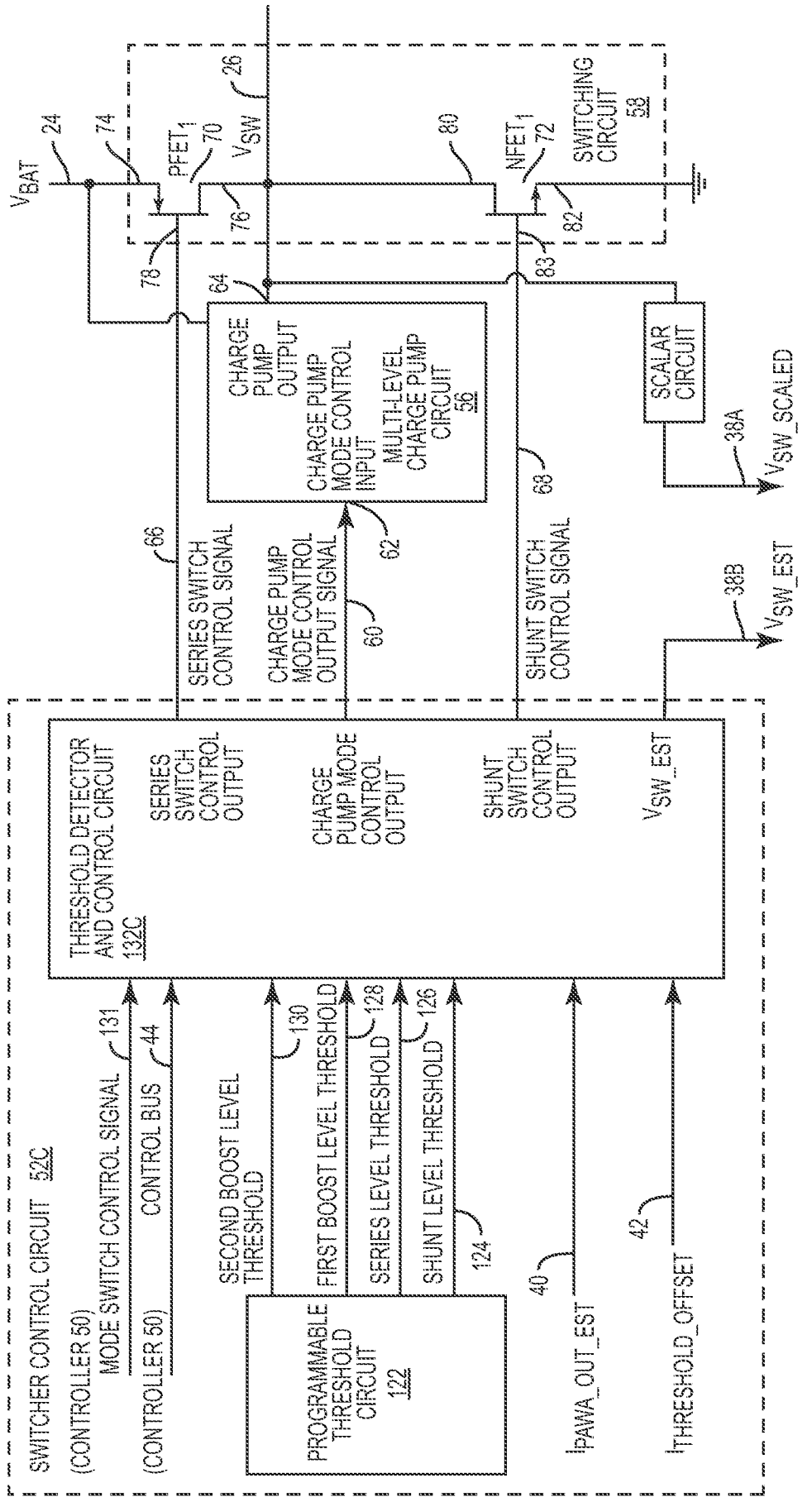

SWITCHER CONTROL CIRCUIT 52C
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132C
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
PROGRAMMABLE THRESHOLD CIRCUIT 122
40
IPAWA_OUT_EST
42
ITHRESHOLD_OFFSET
SERIES SWITCH CONTROL SIGNAL
66
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
60
62
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
SHUNT SWITCH CONTROL SIGNAL
68
SCALAR CIRCUIT
38A
VSW_SCALED
38B
VSW_EST
VBAT
24
74
PFET1
70
VSW
26
78
64
76
80
NFET1
72
SWITCHING CIRCUIT 58
82
83

FIG. 3C

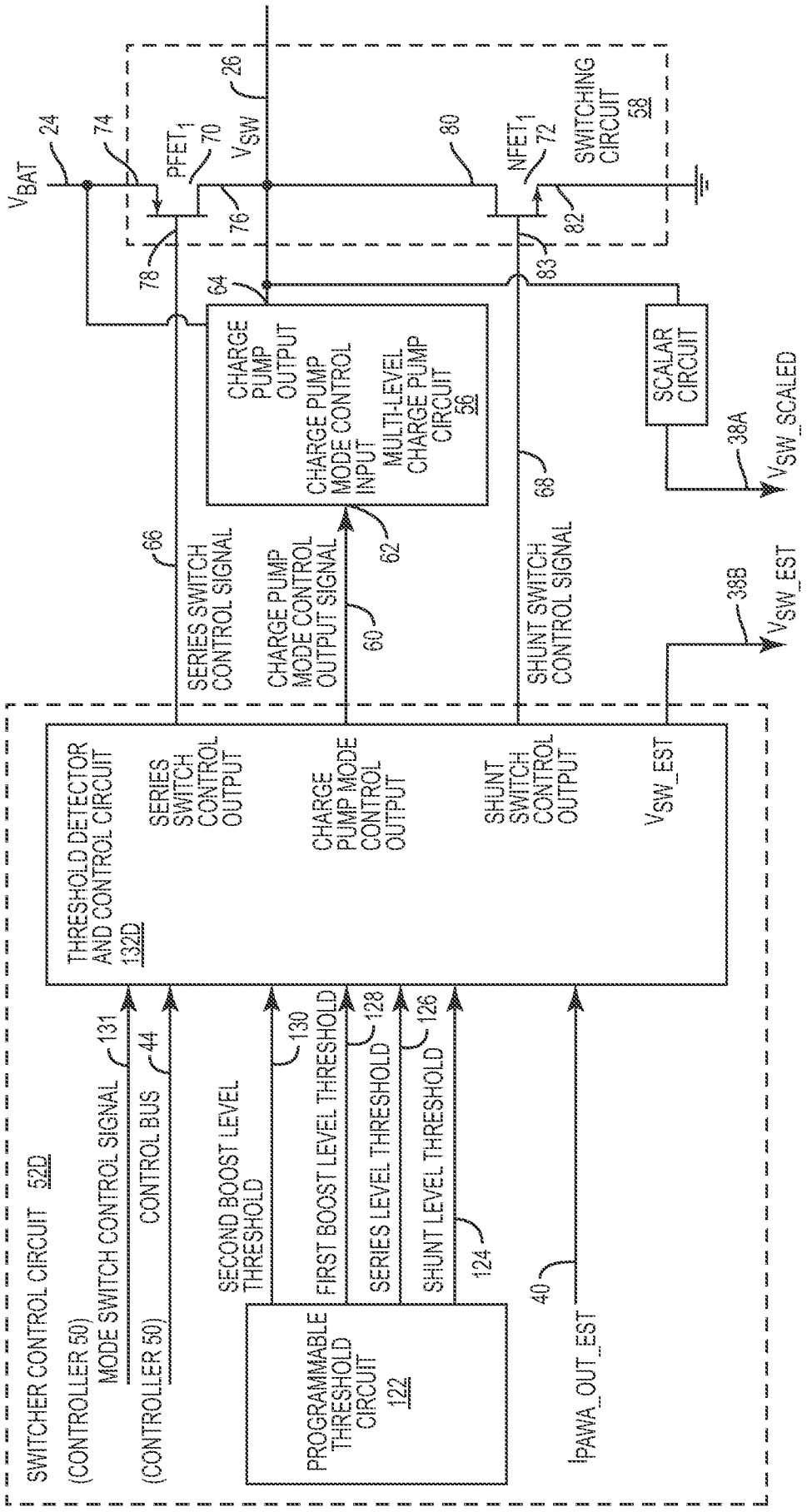

SWITCHER CONTROL CIRCUIT 52D
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132D
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
PROGRAMMABLE THRESHOLD CIRCUIT 122
40
IPAWA_OUT_EST
VBAT
24
74
PFET1
70
VSW
26
76
78
80
NFET1
72
SWITCHING CIRCUIT 58
82
83
64
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
62
66
SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
60
SHUNT SWITCH CONTROL SIGNAL
68
SCALAR CIRCUIT
38A
VSW_SCALED
38B
VSW_EST

FIG. 3D

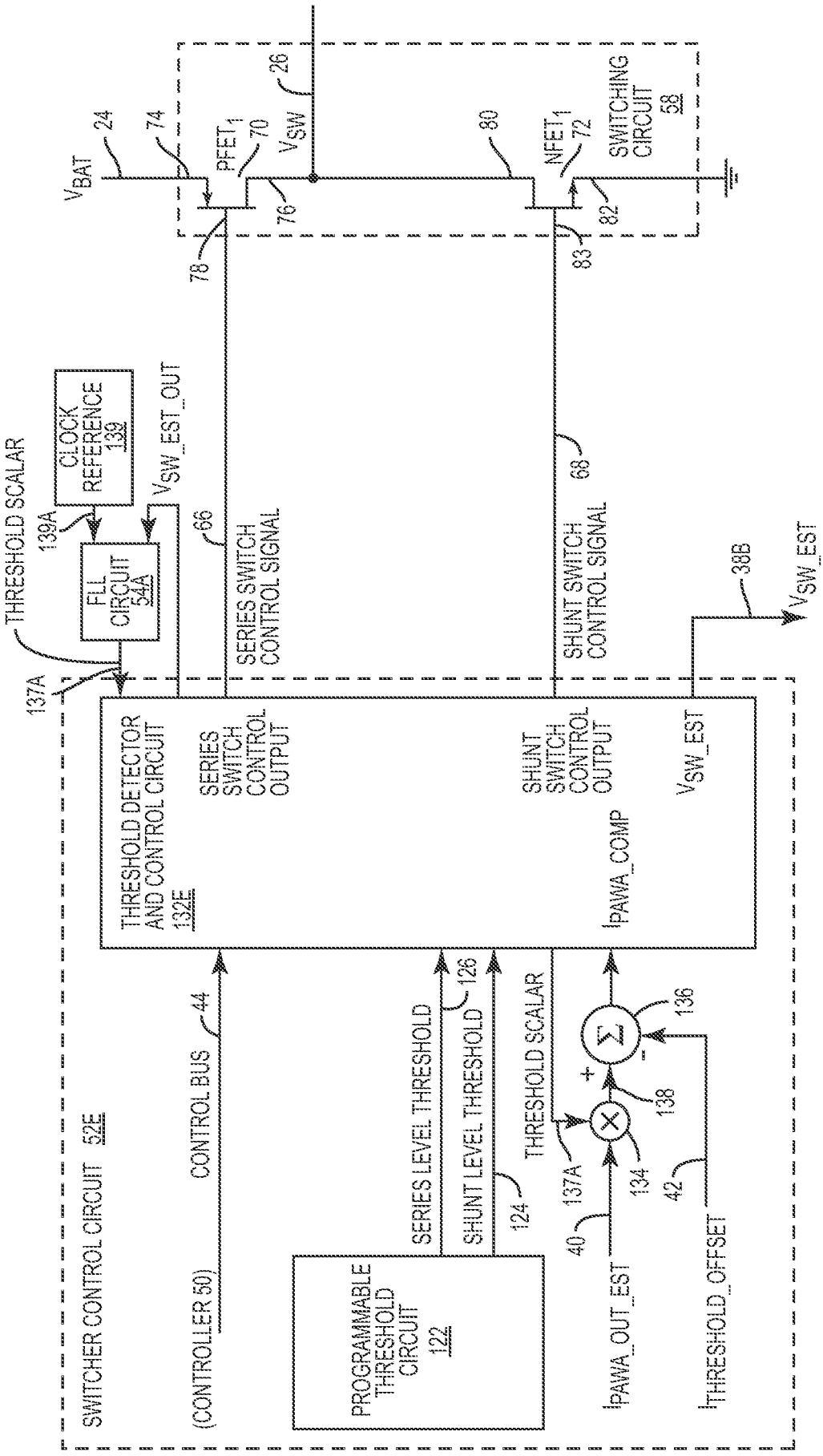

SWITCHER CONTROL CIRCUIT 52E
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132E
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
IPAWA_COMP
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
THRESHOLD SCALAR
IPAWA_OUT_EST
ITHRESHOLD_OFFSET
THRESHOLD SCALAR
137A
FLL CIRCUIT 54A
CLOCK REFERENCE 139
VSW_EST_OUT
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
VBAT
PFET1
VSW
NFET1
SWITCHING CIRCUIT 58
38B
VSW_EST

FIG. 3E

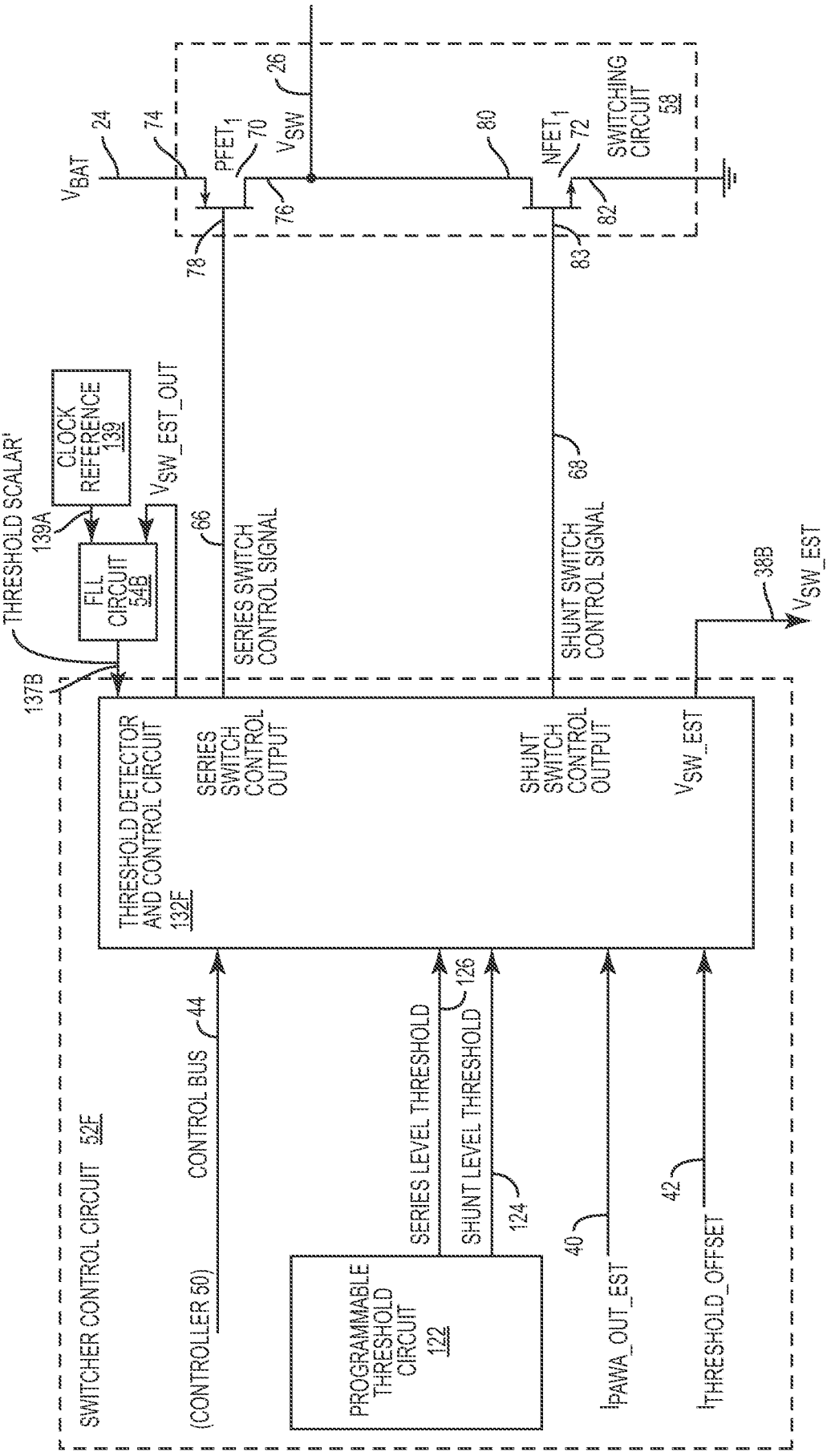

SWITCHER CONTROL CIRCUIT 52E
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132E
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
126
124
40
IPAWA_OUT_EST
42
ITHRESHOLD_OFFSET
THRESHOLD SCALAR'
139A
137B
CLOCK REFERENCE 139
FLL CIRCUIT 54B
VSW_EST_OUT
66
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
68
38B
VSW_EST
VBAT
24
74
PFET1
70
VSW
26
76
78
80
NFET1
72
82
83
SWITCHING CIRCUIT 59

FIG. 3F

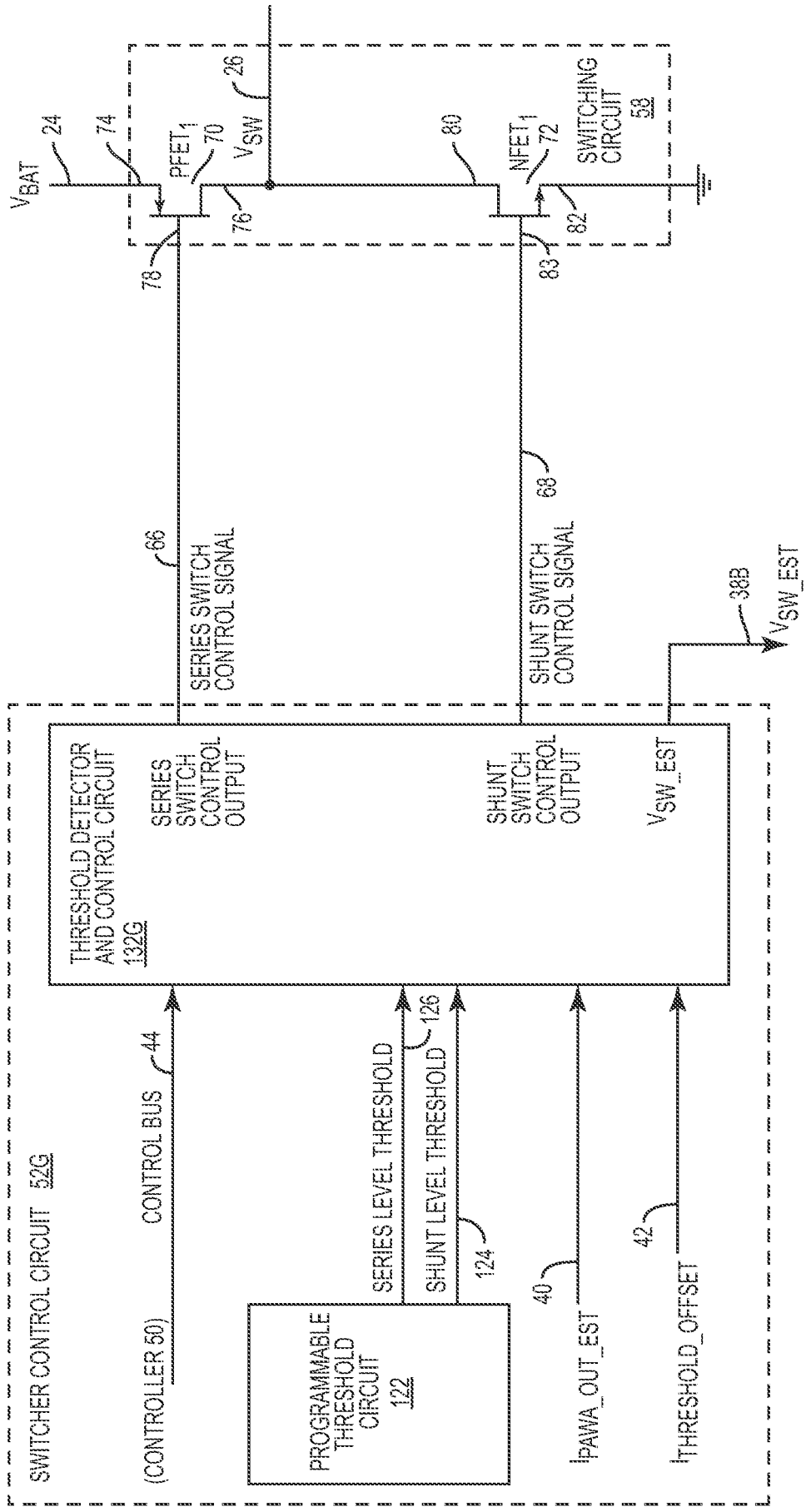

SWITCHER CONTROL CIRCUIT 52G
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132G
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
126
124
40
IPAWA_OUT_EST
42
ITHRESHOLD_OFFSET
66
SERIES SWITCH CONTROL SIGNAL
68
SHUNT SWITCH CONTROL SIGNAL
38B
VSW_EST
VBAT
24
74
PFET1
70
VSW
26
80
NFET1
72
SWITCHING CIRCUIT 59
76
78
82
83

FIG. 3G

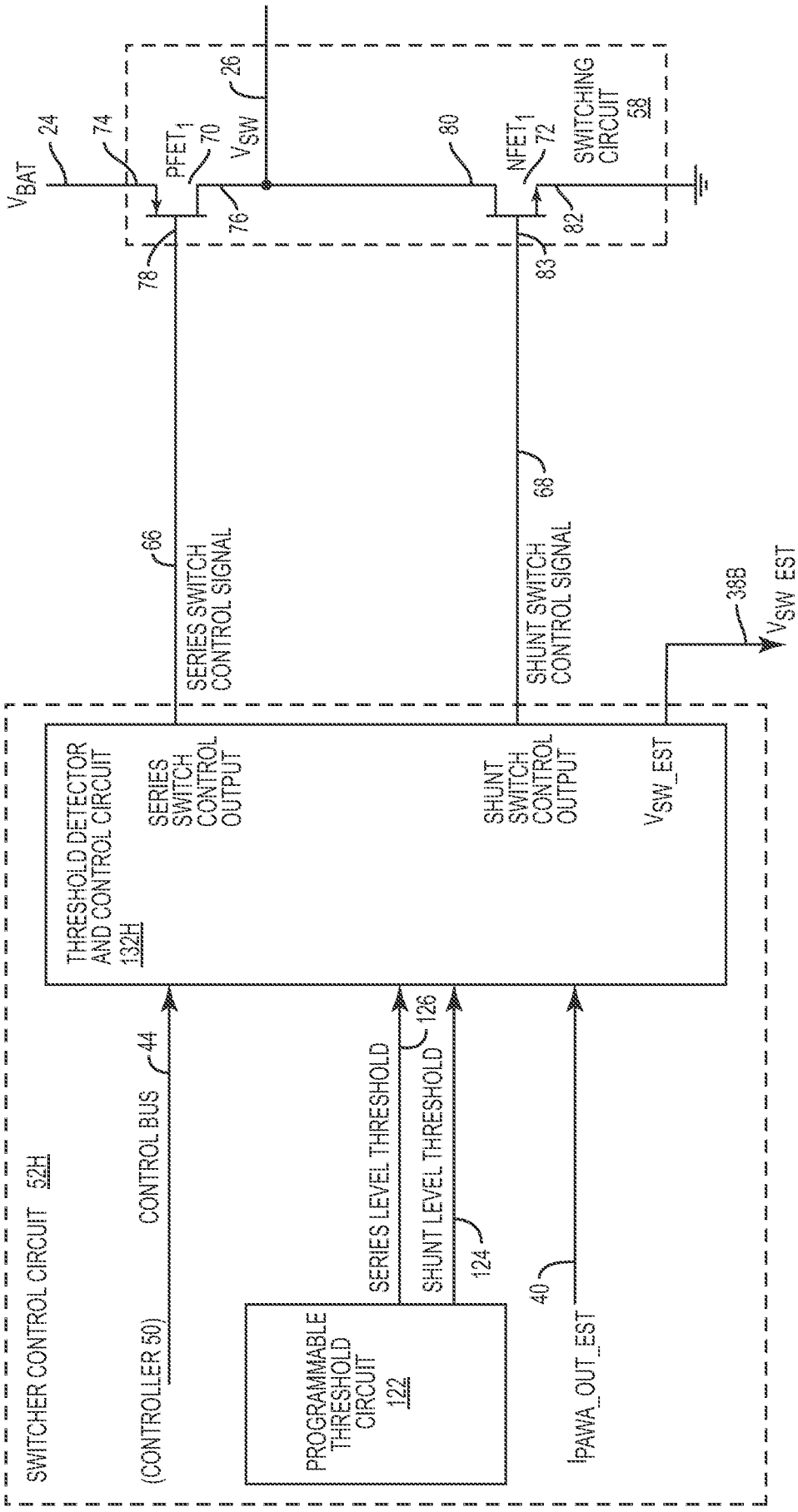

SWITCHER CONTROL CIRCUIT 52H
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132H
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
126
124
40
IPAWA_OUT_EST
66
SERIES SWITCH CONTROL SIGNAL
68
SHUNT SWITCH CONTROL SIGNAL
38B
VSW_EST
VBAT
24
74
PFET1
70
VSW
26
76
78
80
NFET1
72
82
83
SWITCHING CIRCUIT 58

FIG. 3H

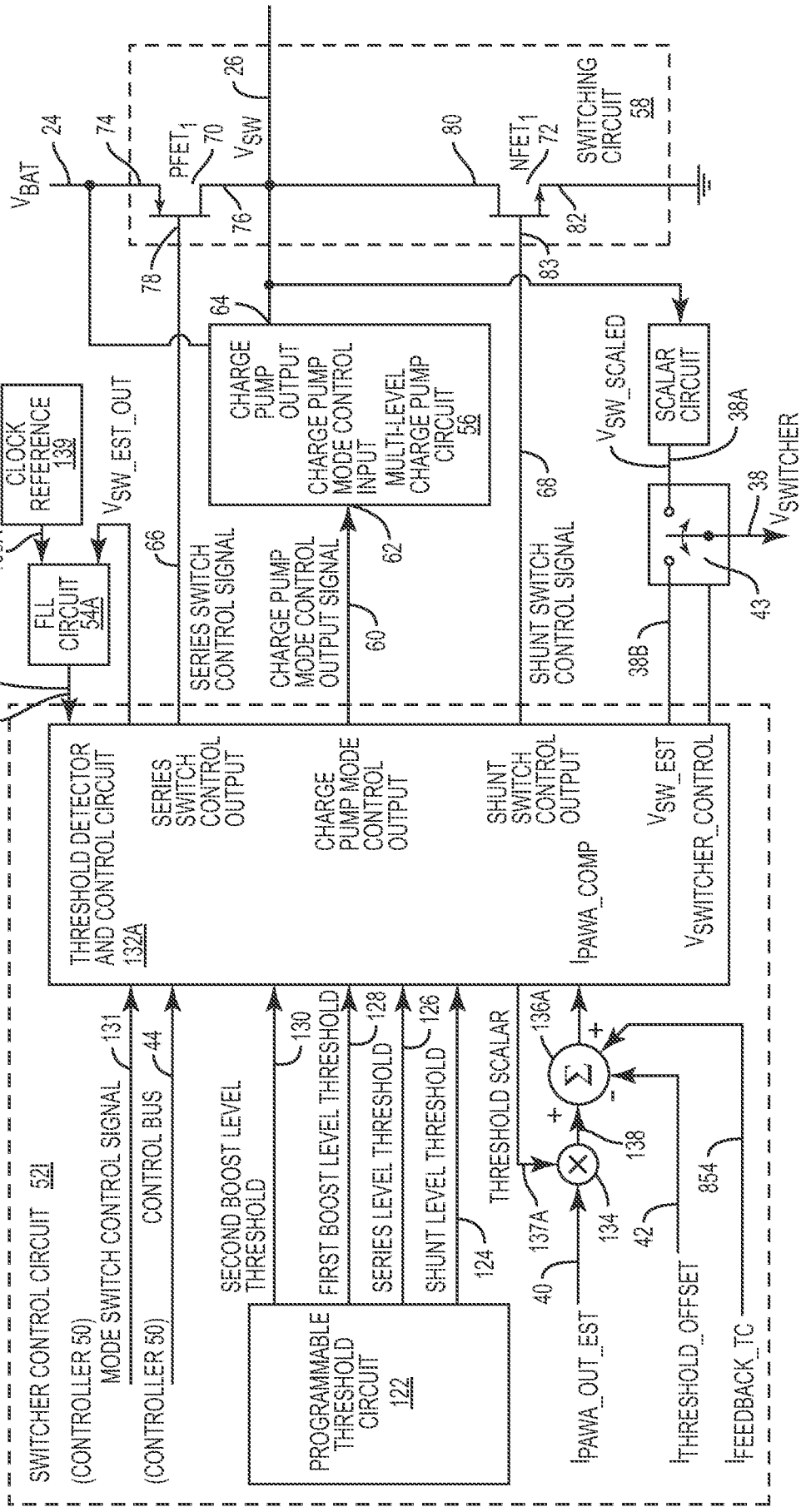

SWITCHER CONTROL CIRCUIT 52
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD SCALAR
137A
139A
CLOCK REFERENCE 139
FLL CIRCUIT 54A
VSW_EST_OUT
66
SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
60
62
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
SHUNT SWITCH CONTROL SIGNAL
68
VSW_SCALED
SCALAR CIRCUIT
38A
38B
43
38
VSWITCHER
VBAT
24
74
PFET1
70
VSW
26
78
76
80
NFET1
72
SWITCHING CIRCUIT 58
82
83
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132A
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
IPAWA_COMP
VSW_EST
VSWITCHER_CONTROL
PROGRAMMABLE THRESHOLD CIRCUIT 122
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
THRESHOLD SCALAR
136A
137A
138
134
40
42
854
IPAWA_OUT_EST
ITHRESHOLD_OFFSET
IFEEDBACK_TC

FIG. 3I

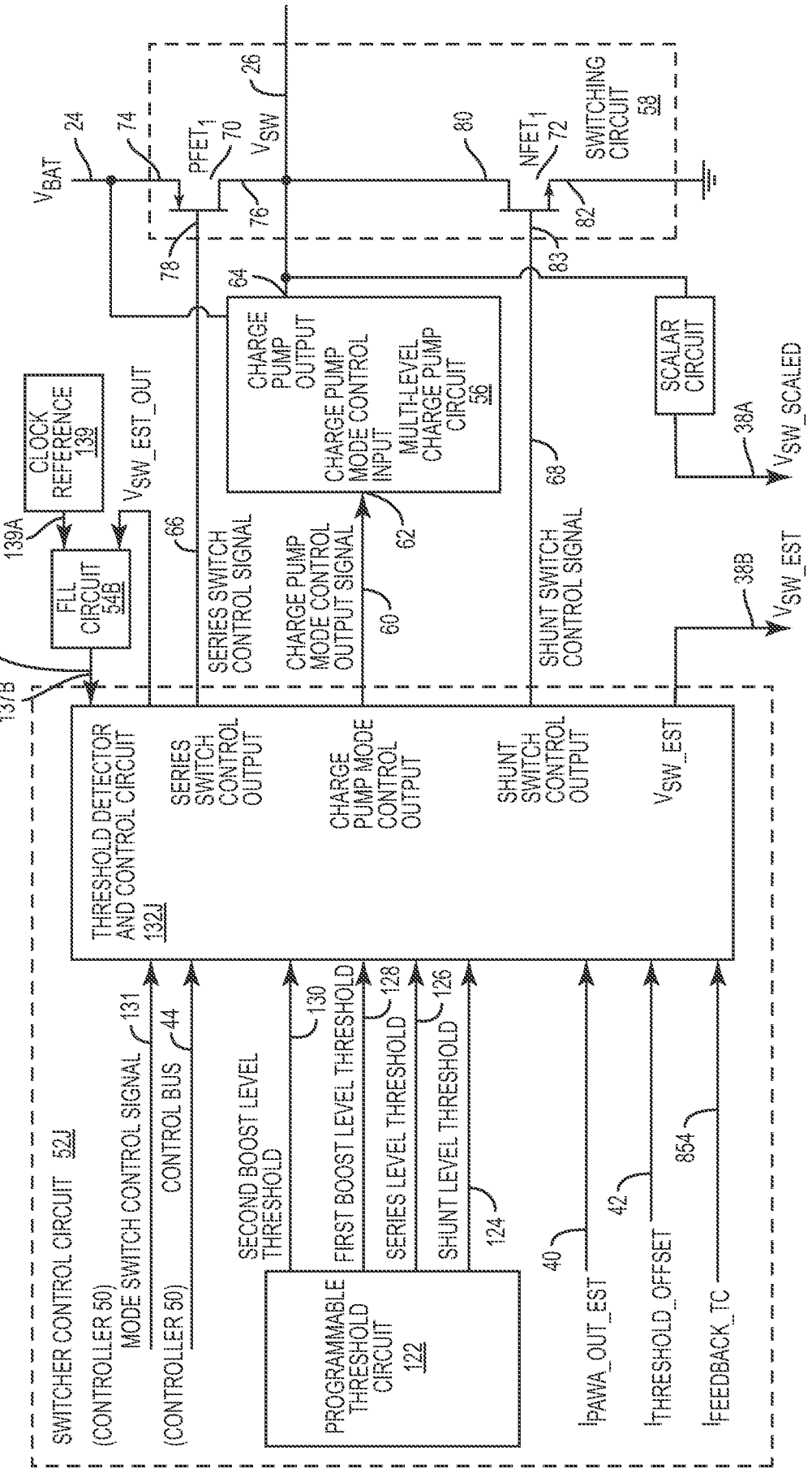

SWITCHER CONTROL CIRCUIT 52J
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD SCALAR'
137B
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132J
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
PROGRAMMABLE THRESHOLD CIRCUIT 122
40
IPAWA_OUT_EST
42
ITHRESHOLD_OFFSET
854
IFEEDBACK_TC
CLOCK REFERENCE 139
139A
FLL CIRCUIT 54B
VSW_EST_OUT
66
SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
60
62
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
SHUNT SWITCH CONTROL SIGNAL
68
SCALAR CIRCUIT
38A
VSW_SCALED
38B
VSW_EST
VBAT
24
74
78
64
PFET1
70
VSW
26
76
80
NFET1
72
82
83
SWITCHING CIRCUIT 59

FIG. 3J

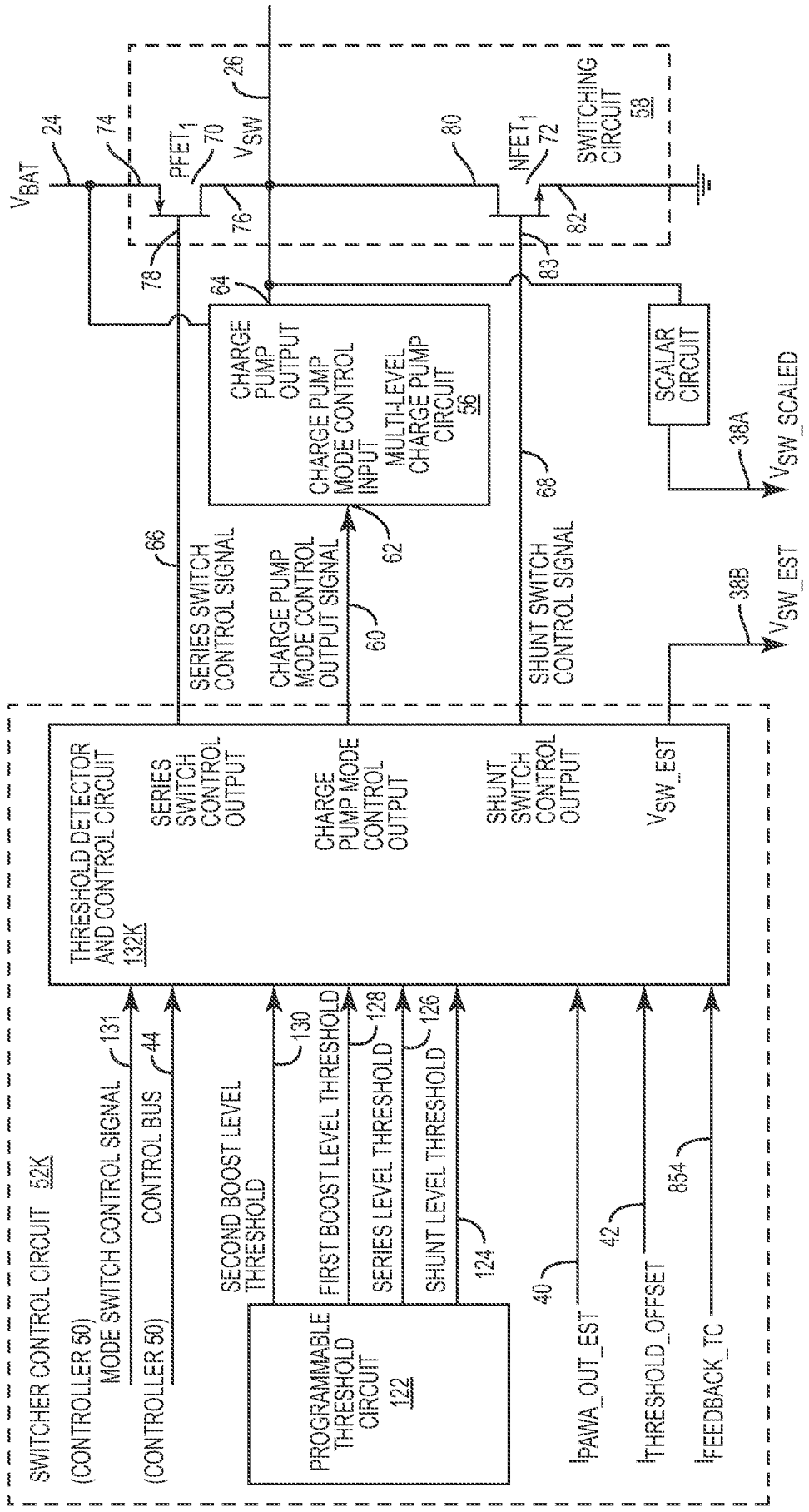

SWITCHER CONTROL CIRCUIT 52K
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL
131
(CONTROLLER 50)
CONTROL BUS
44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132K
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
PROGRAMMABLE THRESHOLD CIRCUIT 122
40
IPAWA_OUT_EST
42
ITHRESHOLD_OFFSET
854
IFEEDBACK_TC
SERIES SWITCH CONTROL SIGNAL
66
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
60
62
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
SHUNT SWITCH CONTROL SIGNAL
68
38B
VSW_EST
SCALAR CIRCUIT
38A
VSW_SCALED
VBAT
24
74
PFET1
70
VSW
26
80
NFET1
72
SWITCHING CIRCUIT 59
78
64
76
82
83

FIG. 3K

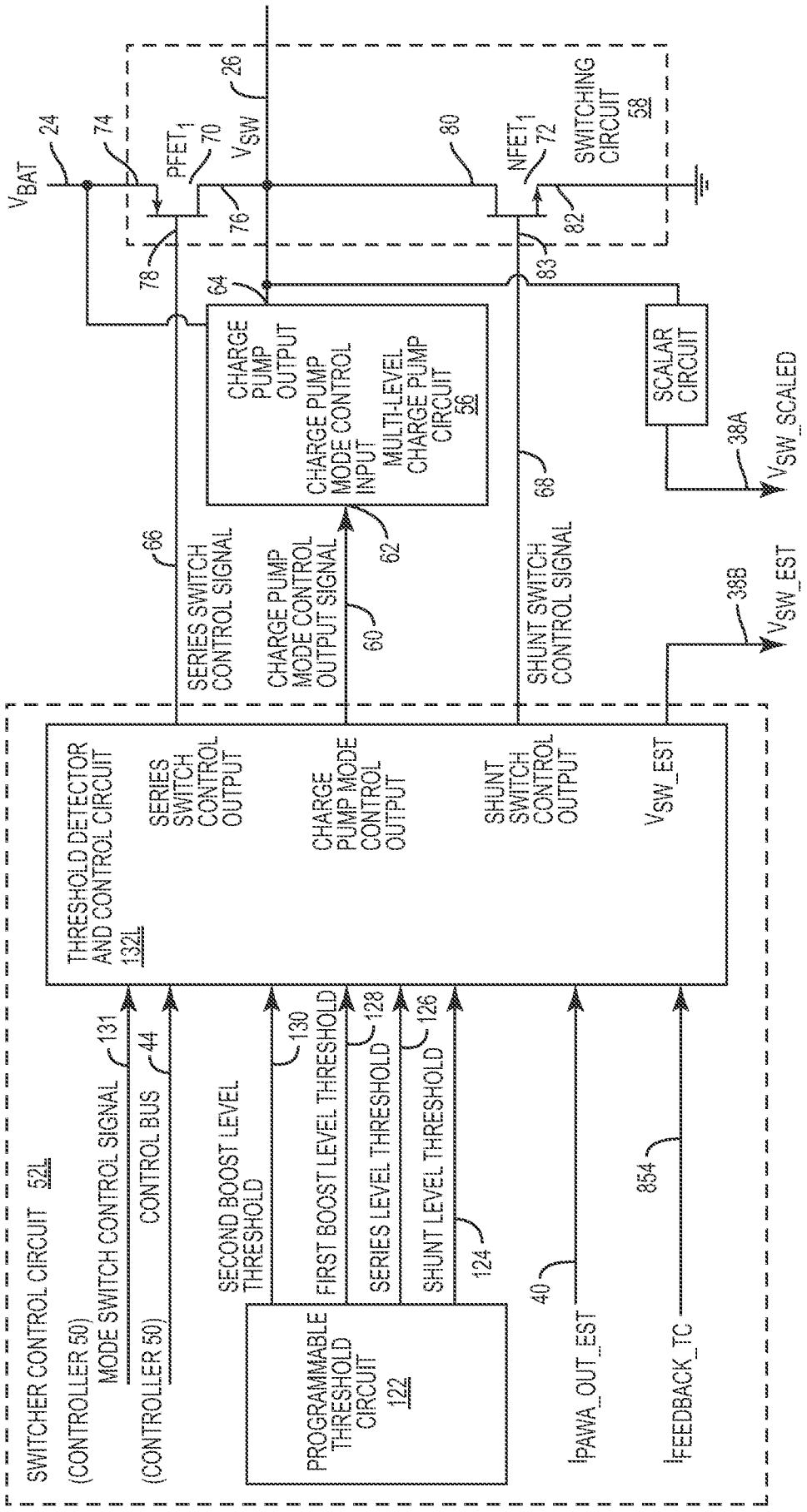

SWITCHER CONTROL CIRCUIT 52L
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132L
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
PROGRAMMABLE THRESHOLD CIRCUIT 122
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
130
128
126
124
40
IPAWA_OUT_EST
854
IFEEDBACK_TC
SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
SHUNT SWITCH CONTROL SIGNAL
66
60
68
62
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
SCALAR CIRCUIT
38A
VSW_SCALED
38B
VSW_EST
VBAT
24
74
78
PFET1
70
76
VSW
26
80
NFET1
72
82
83
SWITCHING CIRCUIT 58

FIG. 3L

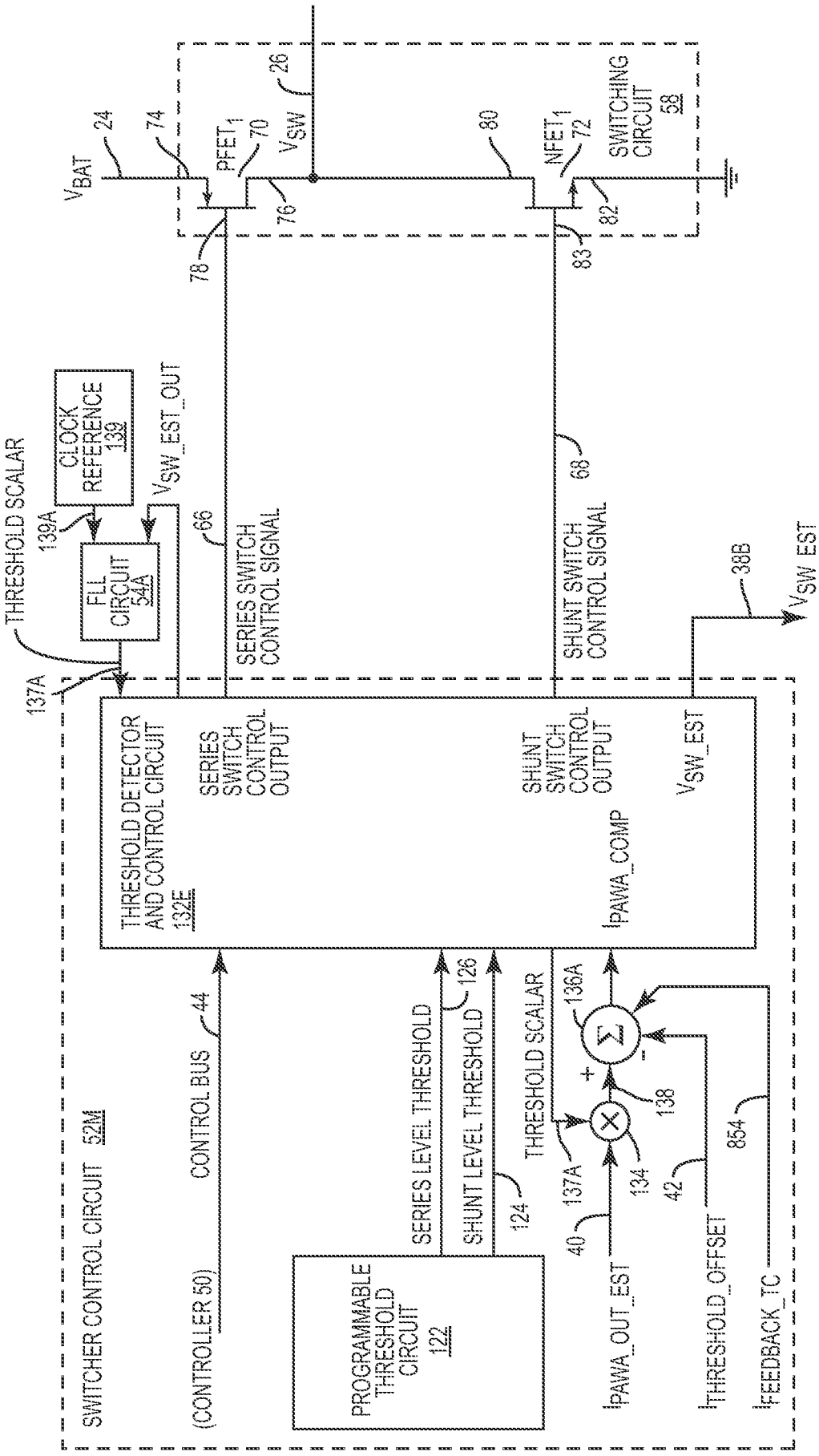

SWITCHER CONTROL CIRCUIT 52M
(CONTROLLER 50)
CONTROL BUS 44
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD 126
SHUNT LEVEL THRESHOLD 124
THRESHOLD SCALAR
137A
136A
138
134
40
42
854
IPAWA_OUT_EST
ITHRESHOLD_OFFSET
IFEEDBACK_TC
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132E
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
IPAWA_COMP
38B
VSW_EST
SERIES SWITCH CONTROL SIGNAL 66
SHUNT SWITCH CONTROL SIGNAL 68
THRESHOLD SCALAR
137A
CLOCK REFERENCE 139
139A
FLL CIRCUIT 54A
VSW_EST_OUT
VBAT 24
74
PFET1 70
VSW 26
76
78
80
NFET1 72
82
83
SWITCHING CIRCUIT 58

FIG. 3M

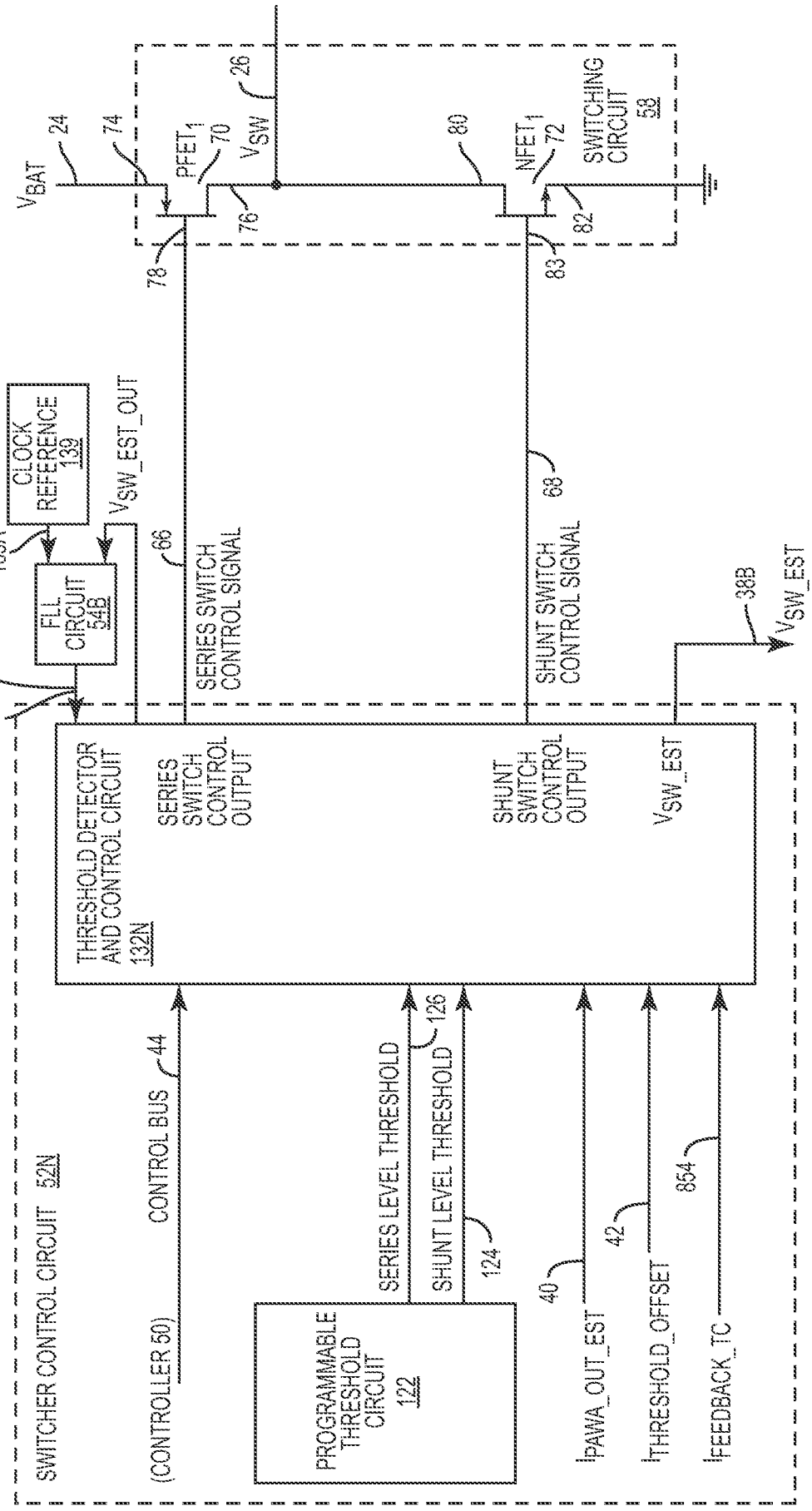

SWITCHER CONTROL CIRCUIT 52N
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132N
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
126
124
40
42
854
IPAWA_OUT_EST
ITHRESHOLD_OFFSET
IFEEDBACK_TC
THRESHOLD SCALAR'
139A
137B
CLOCK REFERENCE 139
FLL CIRCUIT 54B
VSW_EST_OUT
66
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
68
38B
VSW_EST
VBAT
24
74
PFET1
70
VSW
26
76
78
80
NFET1
72
82
83
SWITCHING CIRCUIT 59

FIG. 3N

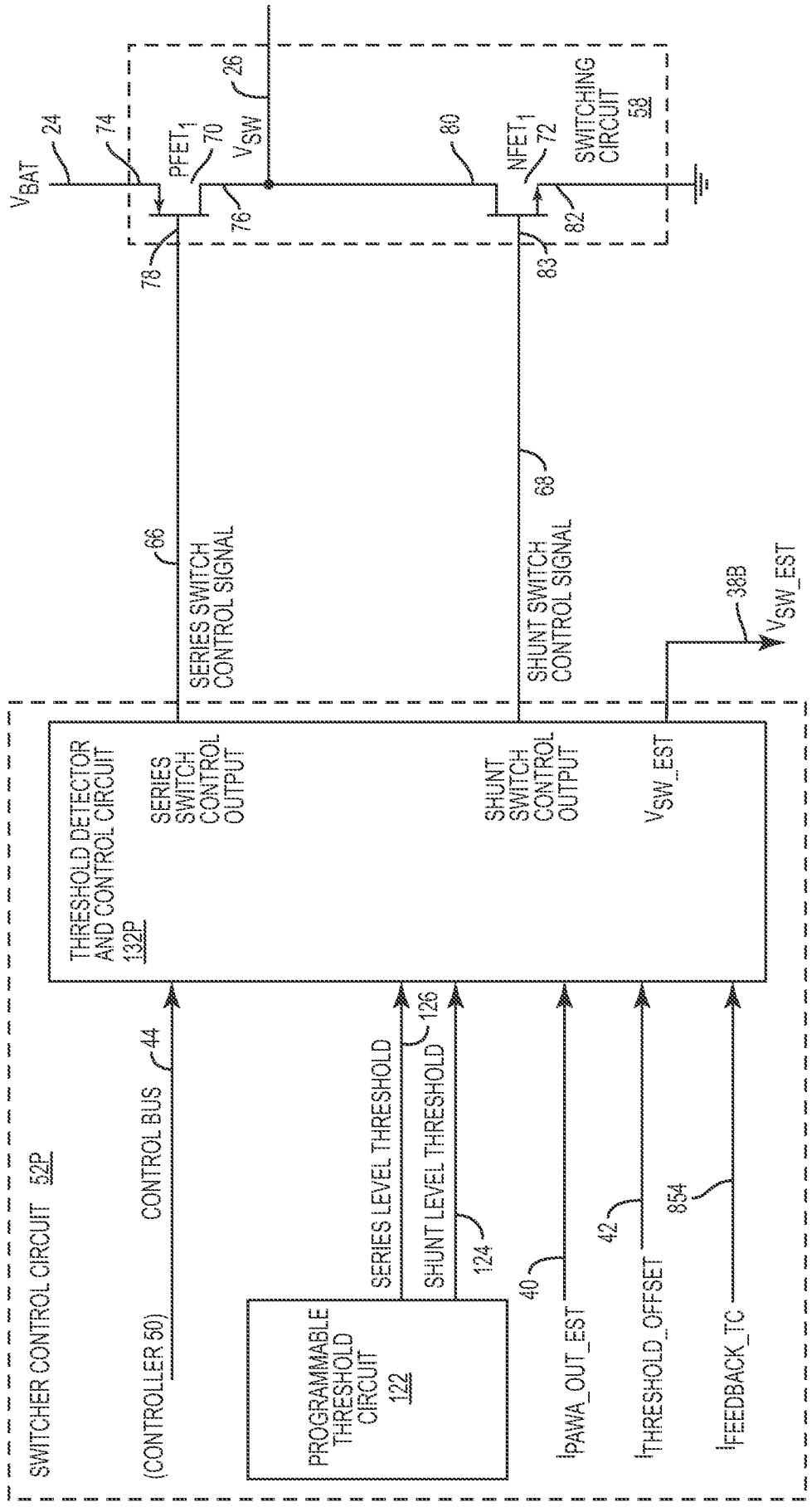

SWITCHER CONTROL CIRCUIT 52P
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132P
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD 126
124
40
IPAWA_OUT_EST
42
ITHRESHOLD_OFFSET
854
IFEEDBACK_TC
66
SERIES SWITCH CONTROL SIGNAL
68
SHUNT SWITCH CONTROL SIGNAL
38B
VSW_EST
VBAT 24
74
PFET1 70
VSW 26
80
NFET1 72
SWITCHING CIRCUIT 58
76
78
82
83

FIG. 3P

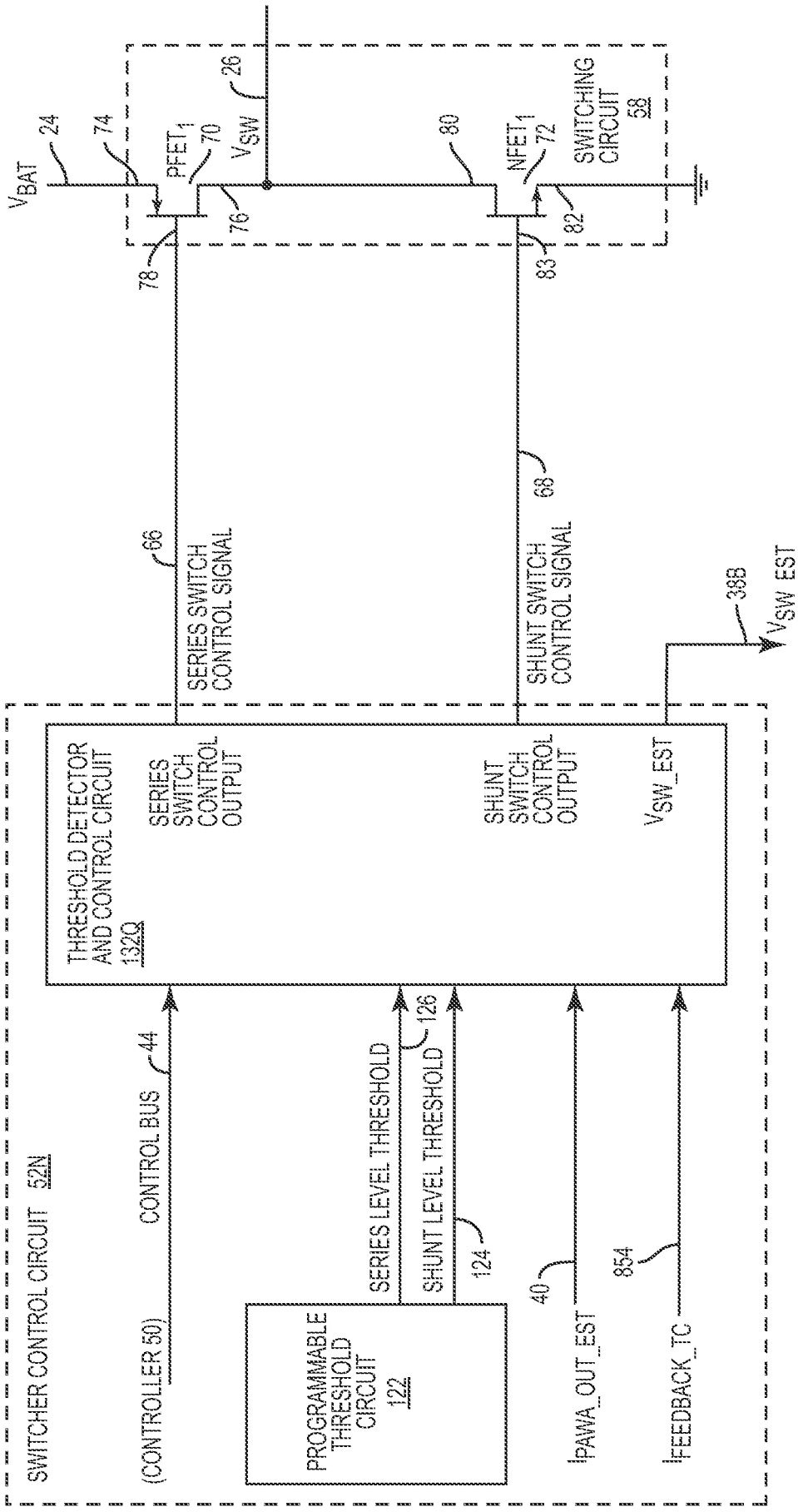

SWITCHER CONTROL CIRCUIT 52N
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132Q
SERIES SWITCH CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
PROGRAMMABLE THRESHOLD CIRCUIT 122
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
126
124
40
IPAWA_OUT_EST
854
IFEEDBACK_TC
66
SERIES SWITCH CONTROL SIGNAL
68
SHUNT SWITCH CONTROL SIGNAL
38B
VSW_EST
VBAT
24
74
PFET1
70
VSW
26
76
78
80
NFET1
72
82
83
SWITCHING CIRCUIT 58

FIG. 3Q

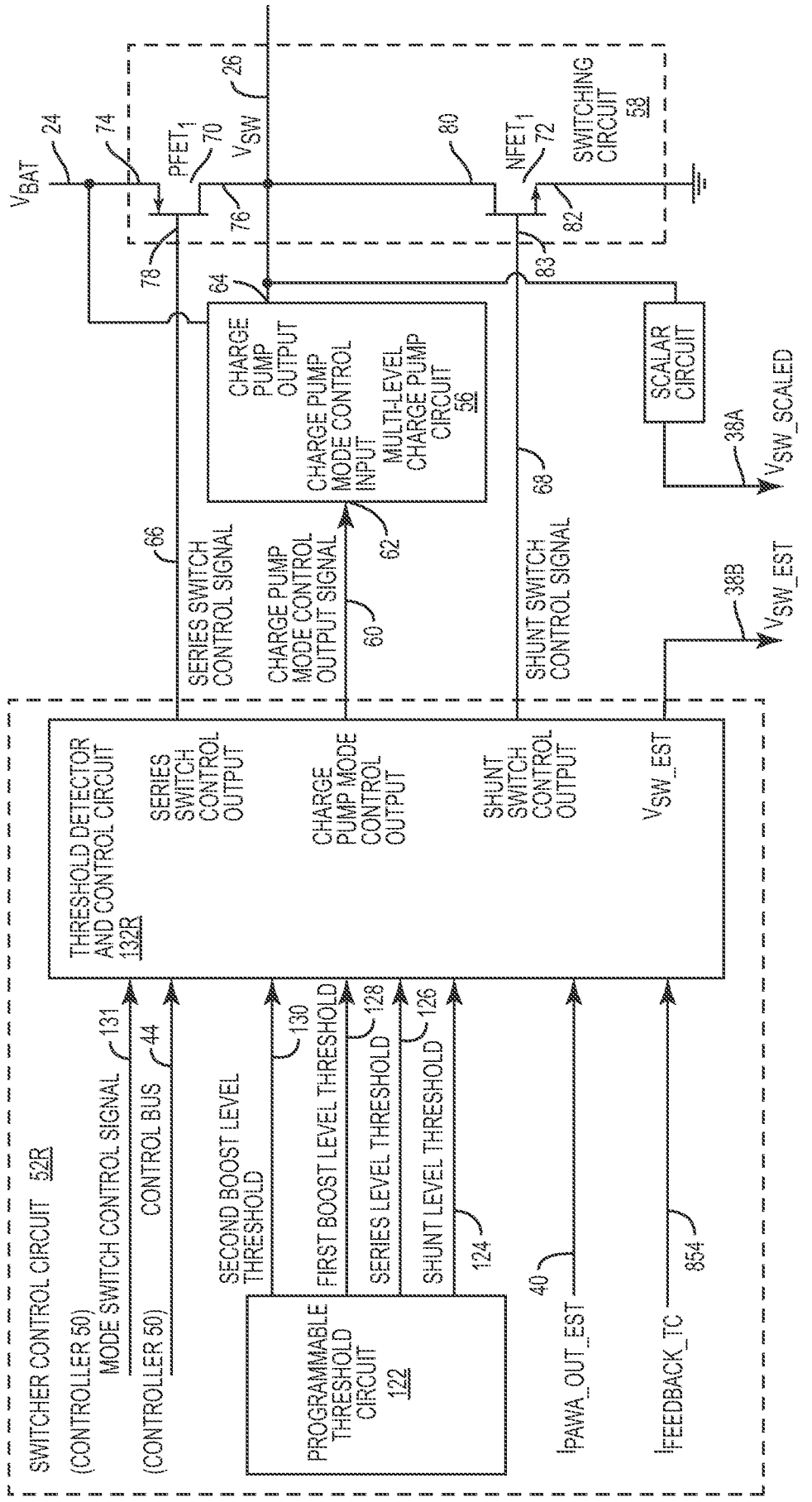

SWITCHER CONTROL CIRCUIT 52R
(CONTROLLER 50)
MODE SWITCH CONTROL SIGNAL 131
(CONTROLLER 50)
CONTROL BUS 44
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132R
SERIES SWITCH CONTROL OUTPUT
CHARGE PUMP MODE CONTROL OUTPUT
SHUNT SWITCH CONTROL OUTPUT
VSW_EST
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
PROGRAMMABLE THRESHOLD CIRCUIT 122
IPAWA_OUT_EST
IFEEDBACK_TC
SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP MODE CONTROL OUTPUT SIGNAL
SHUNT SWITCH CONTROL SIGNAL
CHARGE PUMP OUTPUT
CHARGE PUMP MODE CONTROL INPUT
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
SCALAR CIRCUIT
VSW_SCALED
VSW_EST
VBAT
PFET1
VSW
NFET1
SWITCHING CIRCUIT 59
24
74
70
26
80
72
76
82
78
64
83
66
60
62
68
38A
38B
130
128
126
124
40
854

FIG. 3R

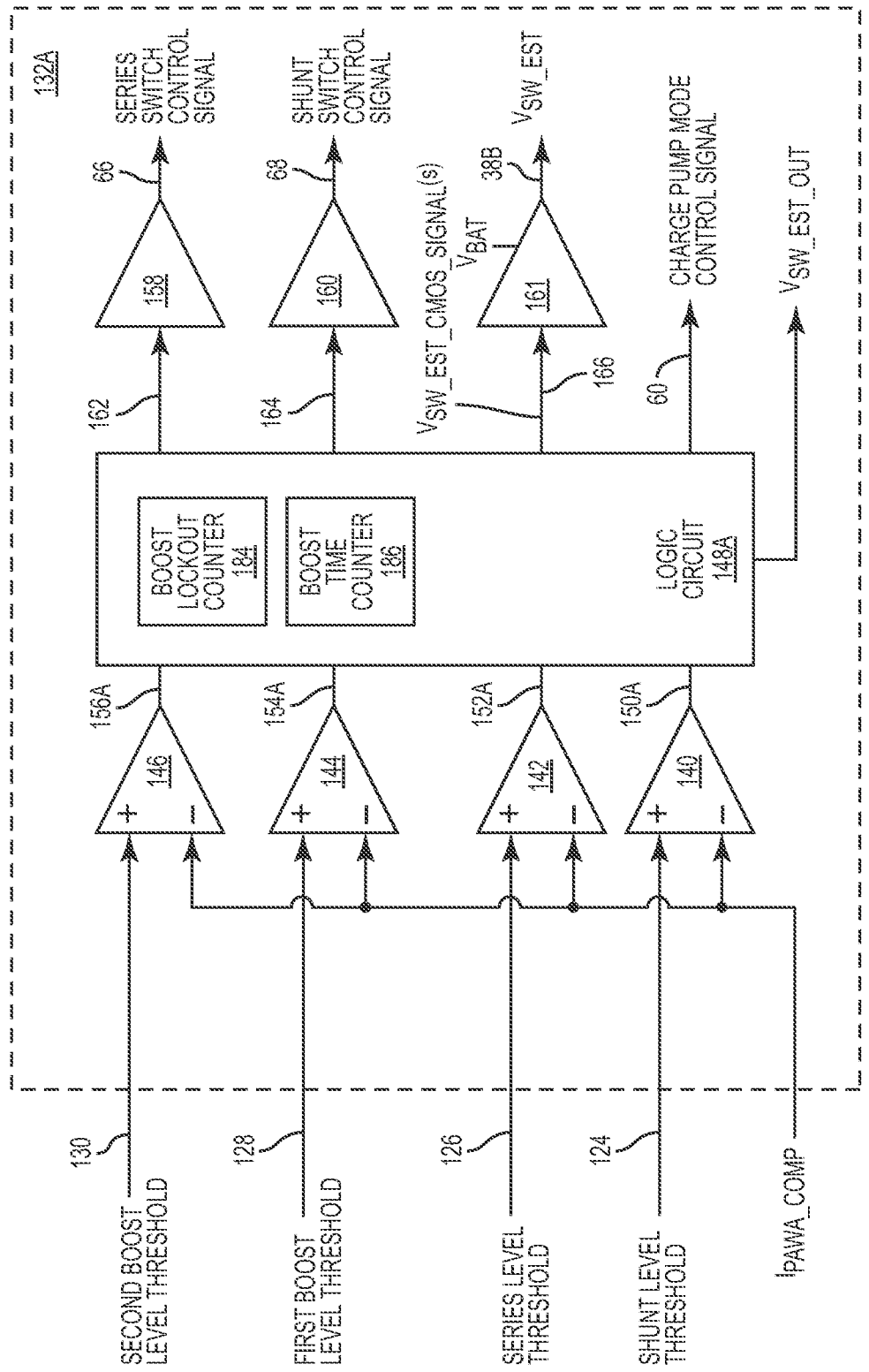

132A
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
V_{SW_EST}
CHARGE PUMP MODE CONTROL SIGNAL
$V_{SW_EST_OUT}$
66
68
38B
158
160
161
162
164
166
60
$V_{SW_EST_CMOS_SIGNAL(s)}$
V_{BAT}
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148A
156A
154A
152A
150A
146
144
142
140
130
128
126
124
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
I_{PAWA_COMP}

FIG. 4A

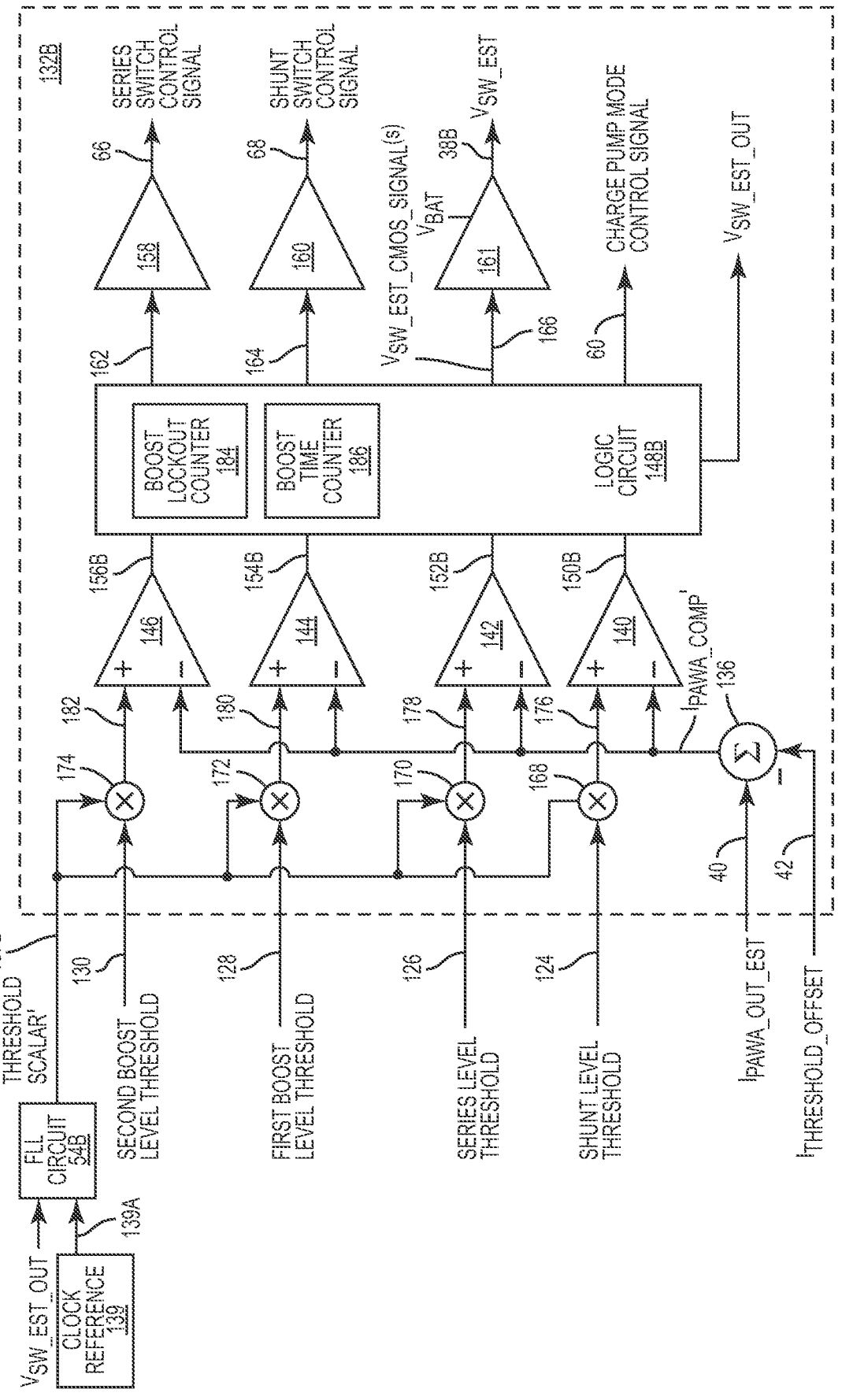

VSW_EST_OUT
CLOCK REFERENCE 139
139A
FLL CIRCUIT 54B
THRESHOLD SCALAR'
137B
132B
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
IPAWA_OUT_EST
40
ITHRESHOLD_OFFSET
42
156B
154B
152B
150B
146
144
142
140
182
180
178
176
174
172
170
168
IPAWA_COMP'
136
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148B
162
164
166
60
158
160
161
66
68
38B
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
VSW_EST_CMOS_SIGNAL(s)
VBAT
VSW_EST
CHARGE PUMP MODE CONTROL SIGNAL
VSW_EST_OUT

FIG. 4B

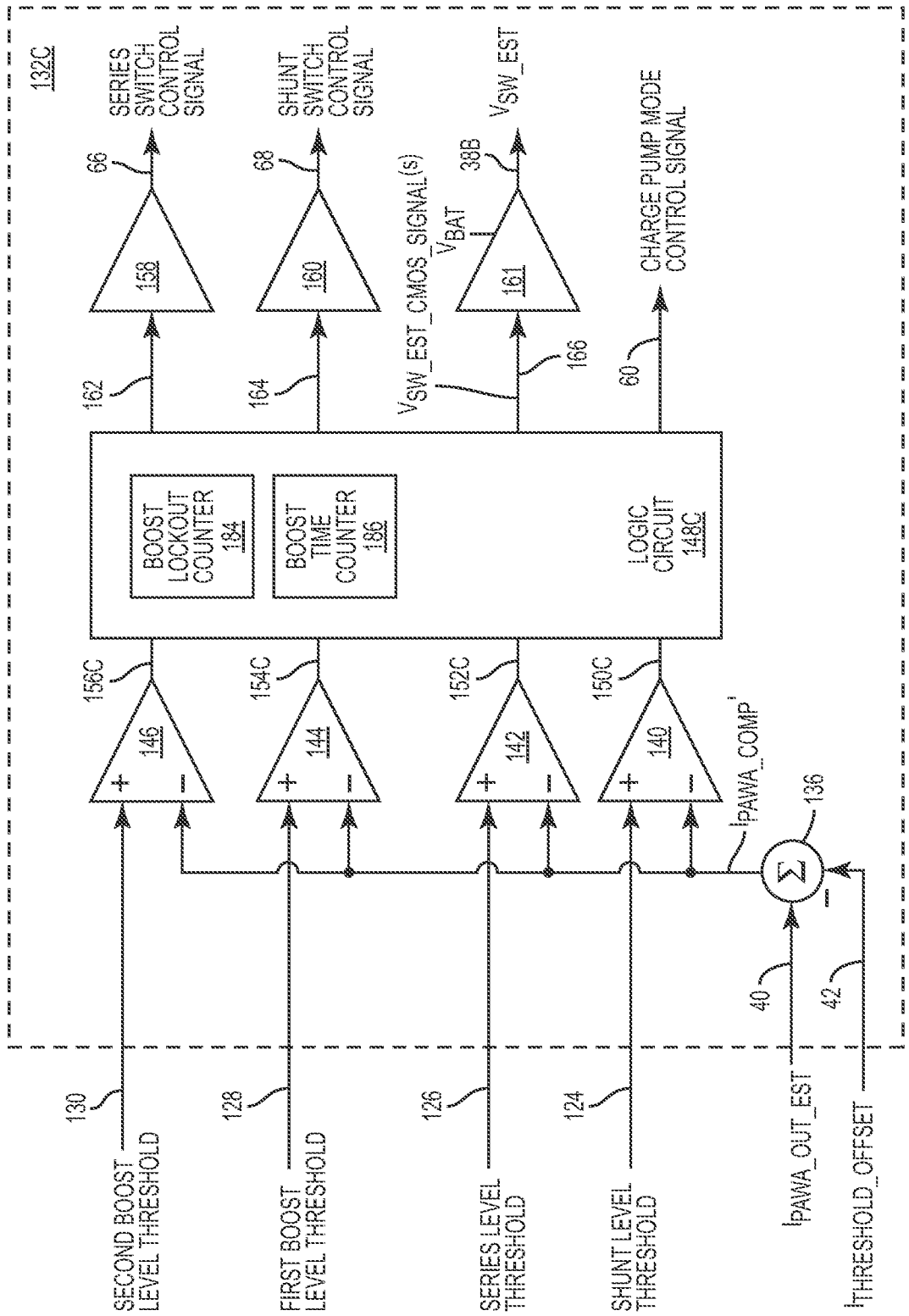

132C
SERIES SWITCH CONTROL SIGNAL
66
158
SHUNT SWITCH CONTROL SIGNAL
68
160
V_{SW_EST}
38B
V_{BAT}
161
CHARGE PUMP MODE CONTROL SIGNAL
60
162
164
$V_{SW_EST_CMOS_SIGNAL(S)}$
166
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148C
156C
154C
152C
150C
146
144
142
140
I_{PAWA_COMP}'
136
40
42
130
128
126
124
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$
$I_{THRESHOLD_OFFSET}$

FIG. 4C

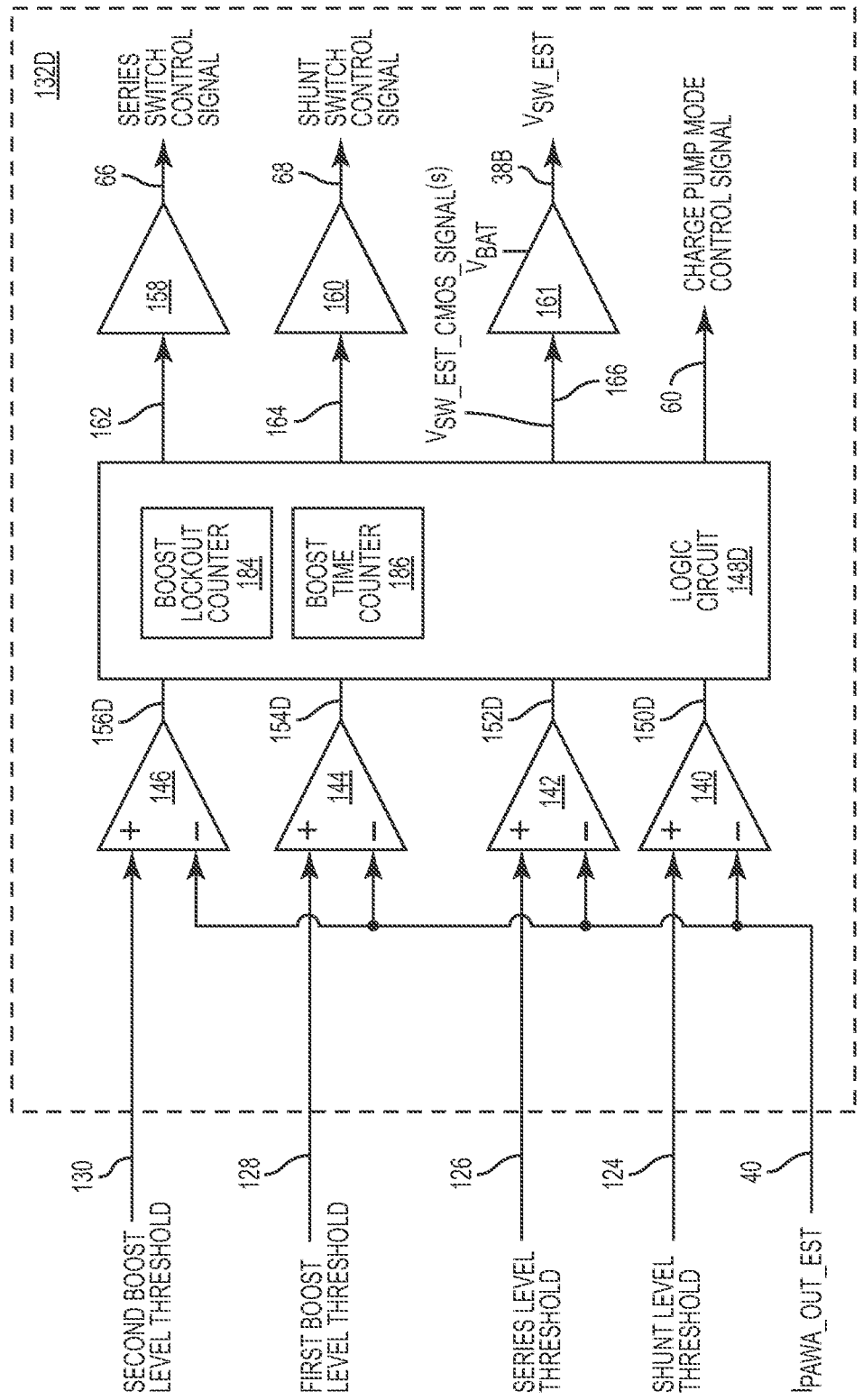

132D
SERIES SWITCH CONTROL SIGNAL
66
158
SHUNT SWITCH CONTROL SIGNAL
68
160
V_{SW_EST}
38B
V_{BAT}
161
$V_{SW_EST_CMOS_SIGNAL(S)}$
CHARGE PUMP MODE CONTROL SIGNAL
60
162
164
166
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148D
156D
154D
152D
150D
146
144
142
140
130
128
126
124
40
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$

FIG. 4D

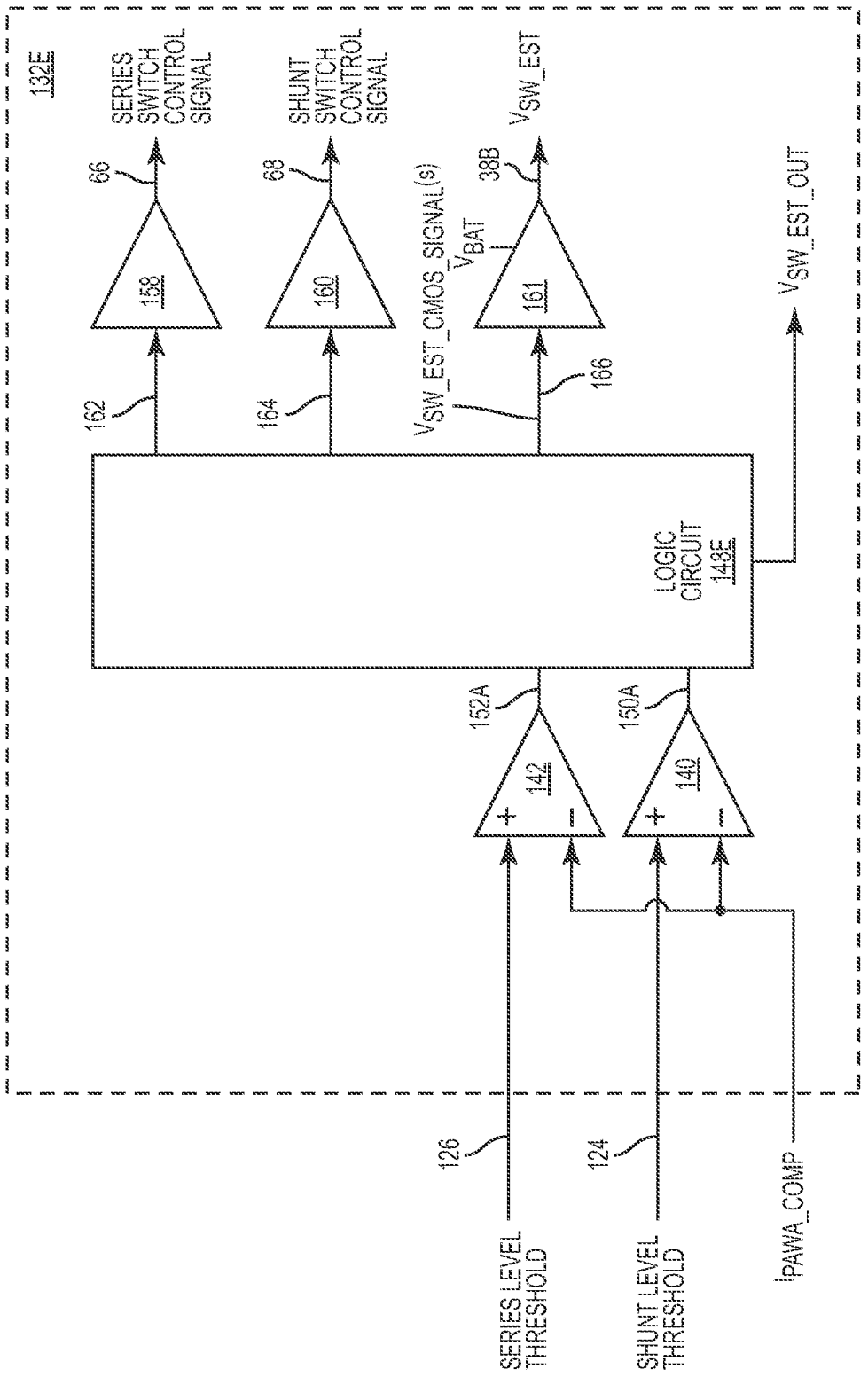

132E
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
V_{SW_EST}
66
68
38B
158
160
161
V_{BAT}
$V_{SW_EST_CMOS_SIGNAL(s)}$
162
164
166
$V_{SW_EST_OUT}$
LOGIC CIRCUIT 148E
152A
150A
142
140
126
124
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
I_{PAWA_COMP}

FIG. 4E

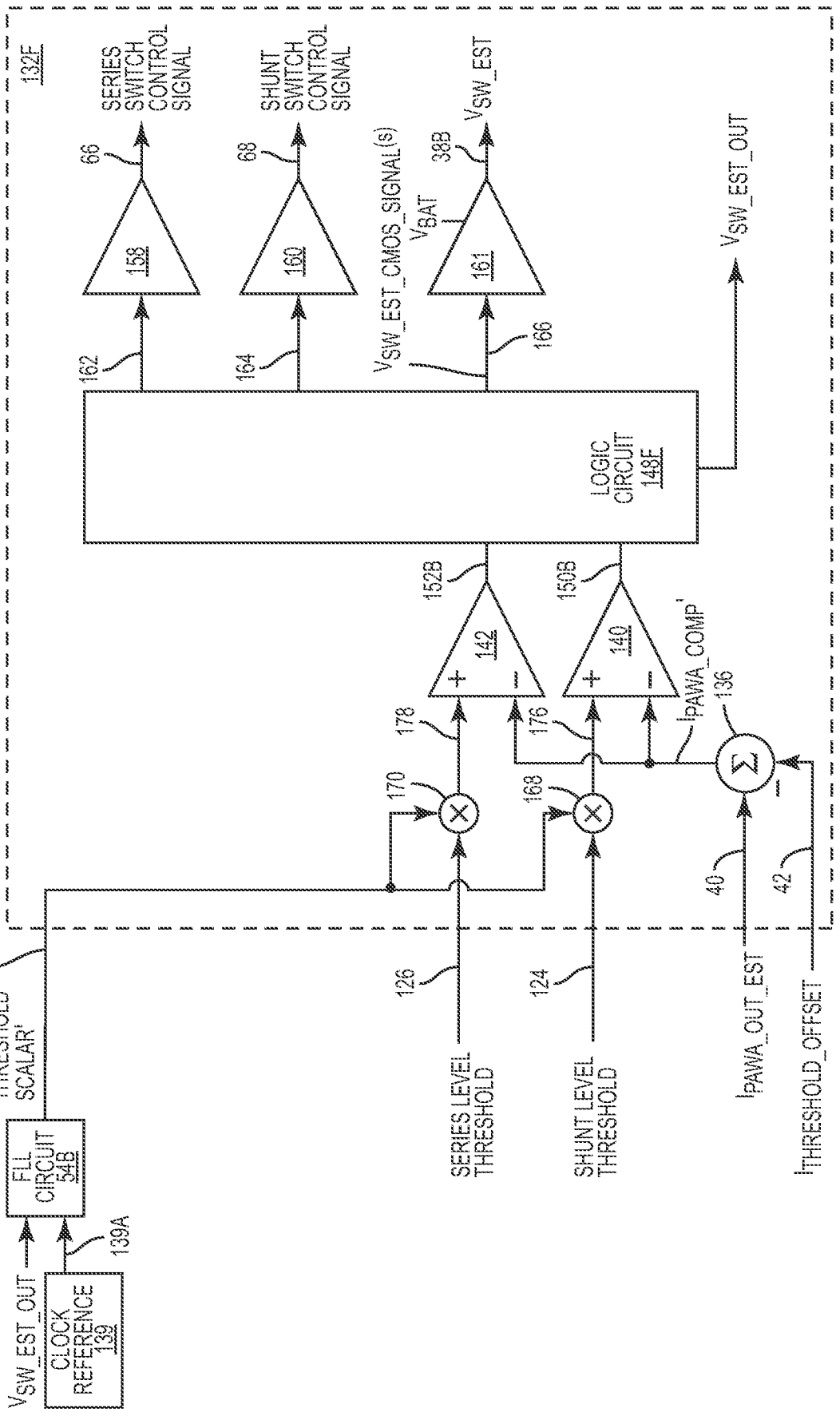

132F
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
VSW_EST
VSW_EST_OUT
66
68
38B
158
160
161
VSW_EST_CMOS_SIGNAL(s)
VBAT
162
164
166
LOGIC CIRCUIT 148F
152B
150B
142
140
178
176
170
168
IPAWA_COMP'
136
137B
THRESHOLD SCALAR'
FLL CIRCUIT 54B
126
124
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
40
42
IPAWA_OUT_EST
ITHRESHOLD_OFFSET
VSW_EST_OUT
CLOCK REFERENCE 139
139A

FIG. 4F

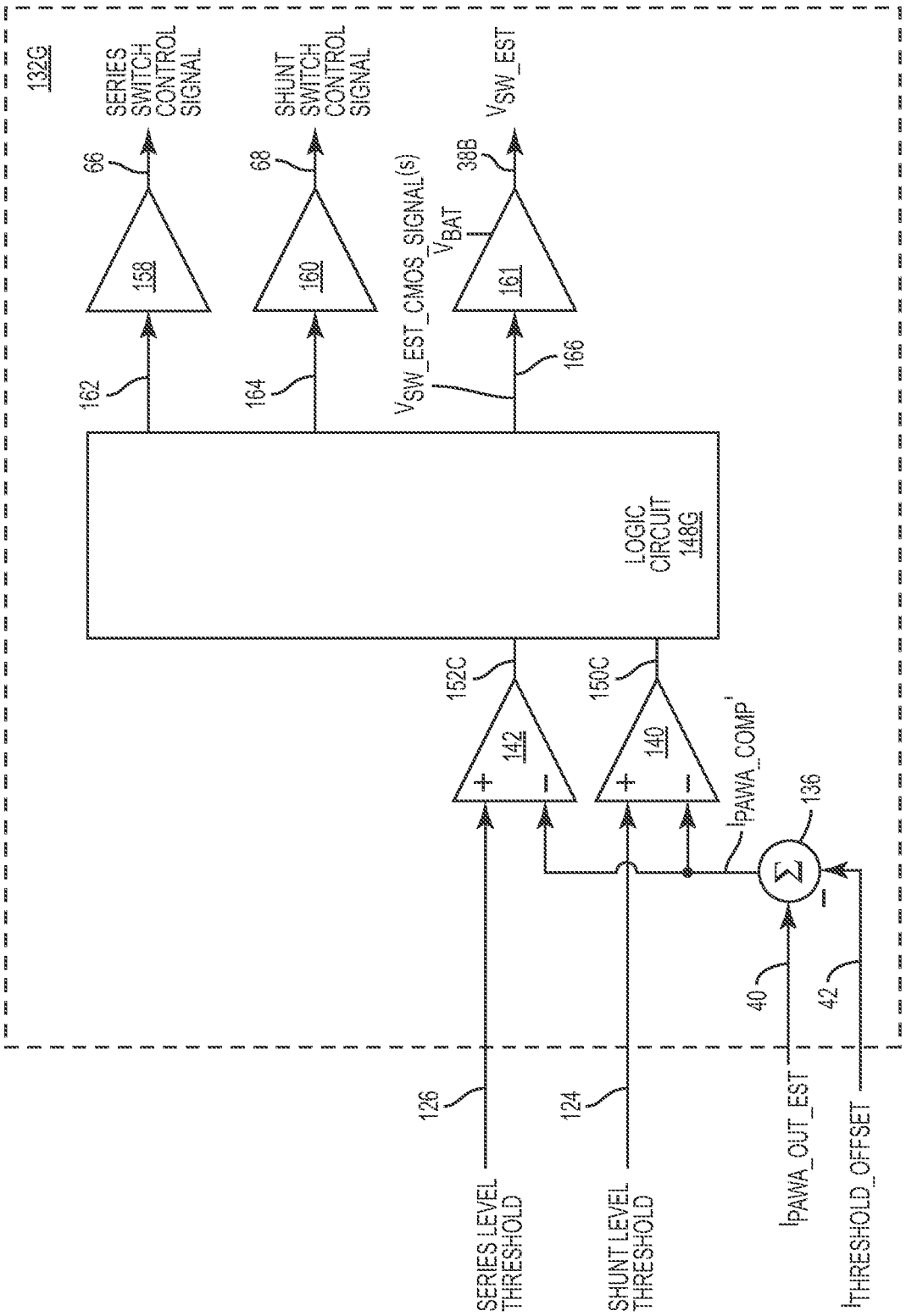

132G
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
V_{SW_EST}
66
68
38B
158
160
161
V_{BAT}
$V_{SW_EST_CMOS_SIGNAL(S)}$
162
164
166
LOGIC CIRCUIT 148G
152C
150C
142
140
I_{PAWA_COMP}'
136
40
42
126
124
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$
$I_{THRESHOLD_OFFSET}$

FIG. 4G

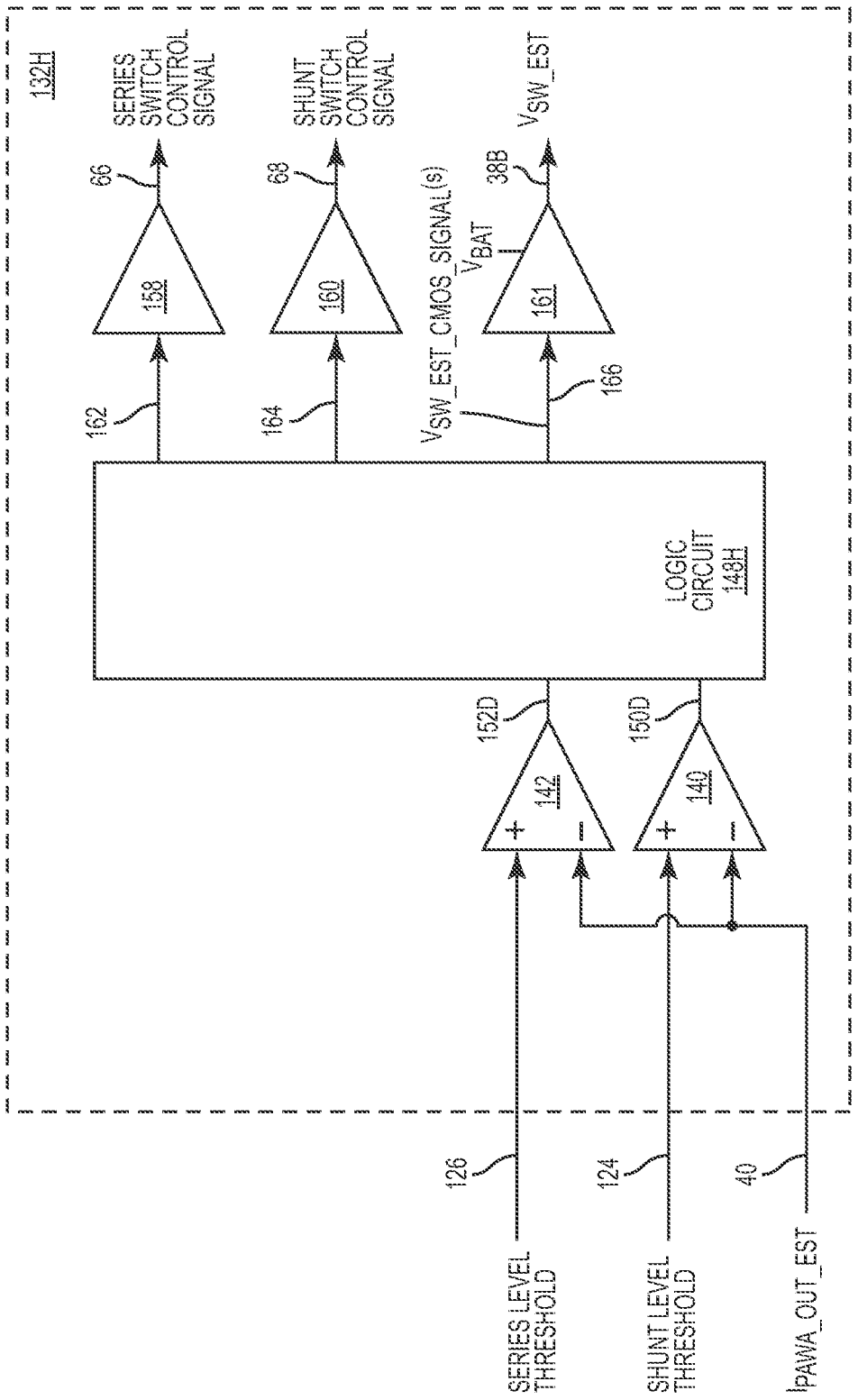

132H
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
V_{SW_EST}
66
68
38B
158
160
161
V_{BAT}
$V_{SW_EST_CMOS_SIGNAL(s)}$
162
164
166
LOGIC CIRCUIT 148H
152D
150D
142
140
126
124
40
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$

FIG. 4H

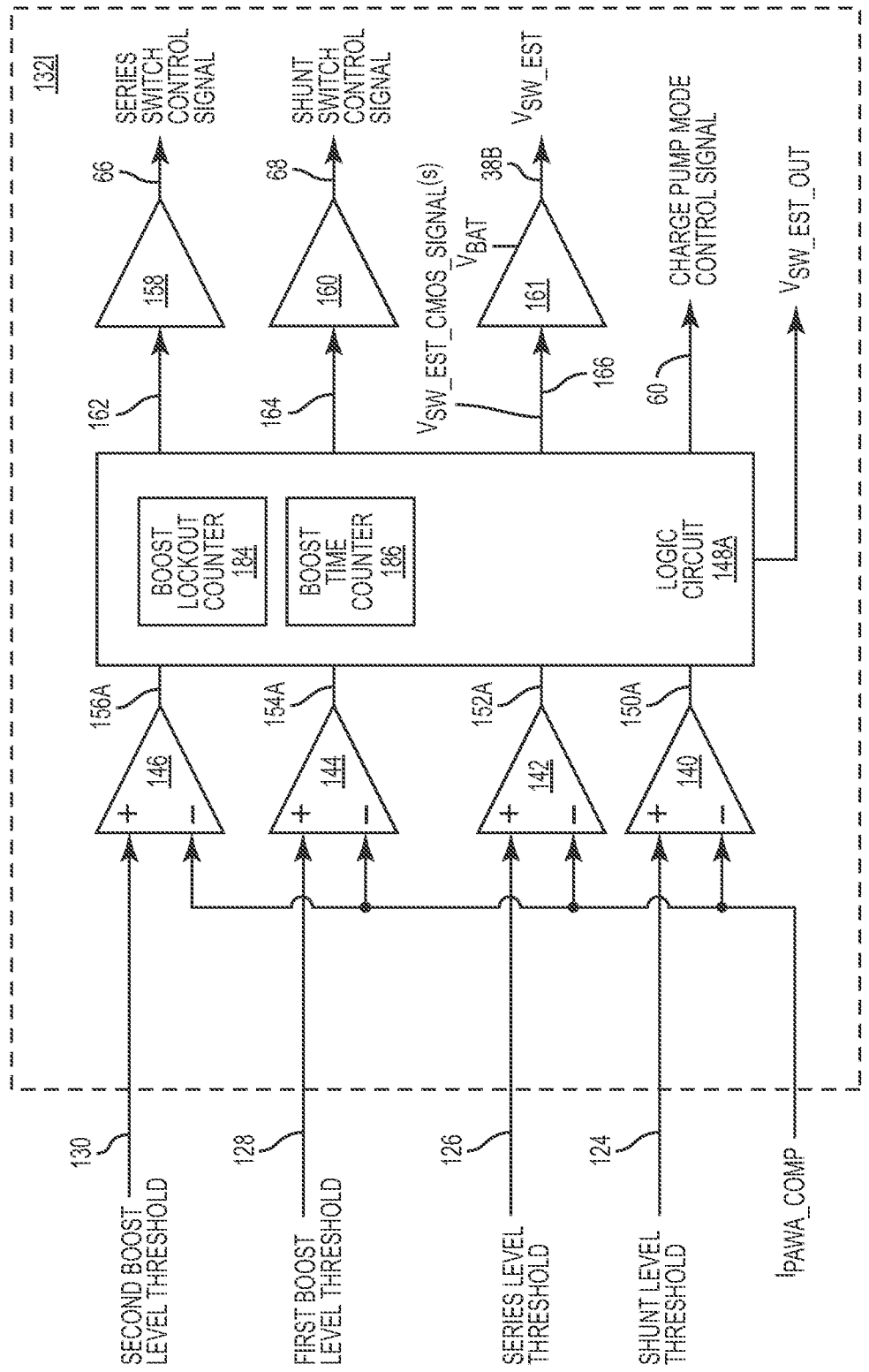

152A
SERIES LEVEL THRESHOLD
126
150A
SHUNT LEVEL THRESHOLD
124
IPAWA_COMP
LOGIC CIRCUIT 148A
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
VSW_EST_CMOS_SIGNAL(s)
VBAT
38B
VSW_EST
166
60
CHARGE PUMP MODE CONTROL SIGNAL
VSW_EST_OUT
162
164
66
SERIES SWITCH CONTROL SIGNAL
68
SHUNT SWITCH CONTROL SIGNAL
158
160
161
146
144
142
140

FIG. 4I

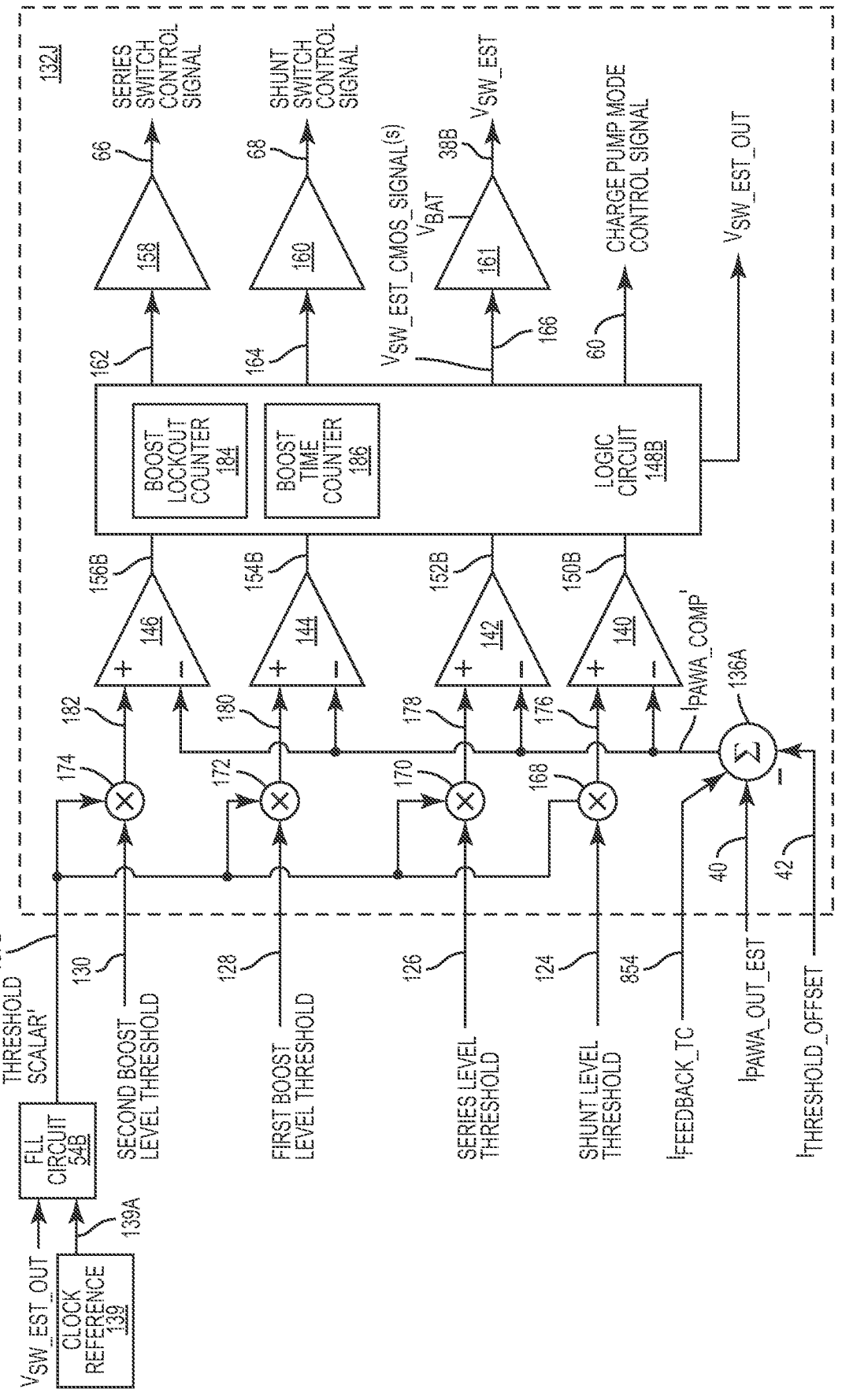

$V_{SW_EST_OUT}$
CLOCK REFERENCE 139
139A
FLL CIRCUIT 54B
THRESHOLD SCALAR'
137B
SECOND BOOST LEVEL THRESHOLD
130
FIRST BOOST LEVEL THRESHOLD
128
SERIES LEVEL THRESHOLD
126
SHUNT LEVEL THRESHOLD
124
$I_{FEEDBACK_TC}$
854
$I_{PAWA_OUT_EST}$
40
$I_{THRESHOLD_OFFSET}$
42
136A
I_{PAWA_COMP}'
146
144
142
140
156B
154B
152B
150B
182
180
178
176
174
172
170
168
132J
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148B
158
160
161
162
164
166
66
68
38B
60
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
$V_{SW_EST_CMOS_SIGNAL(S)}$
V_{BAT}
V_{SW_EST}
CHARGE PUMP MODE CONTROL SIGNAL
$V_{SW_EST_OUT}$

FIG. 4J

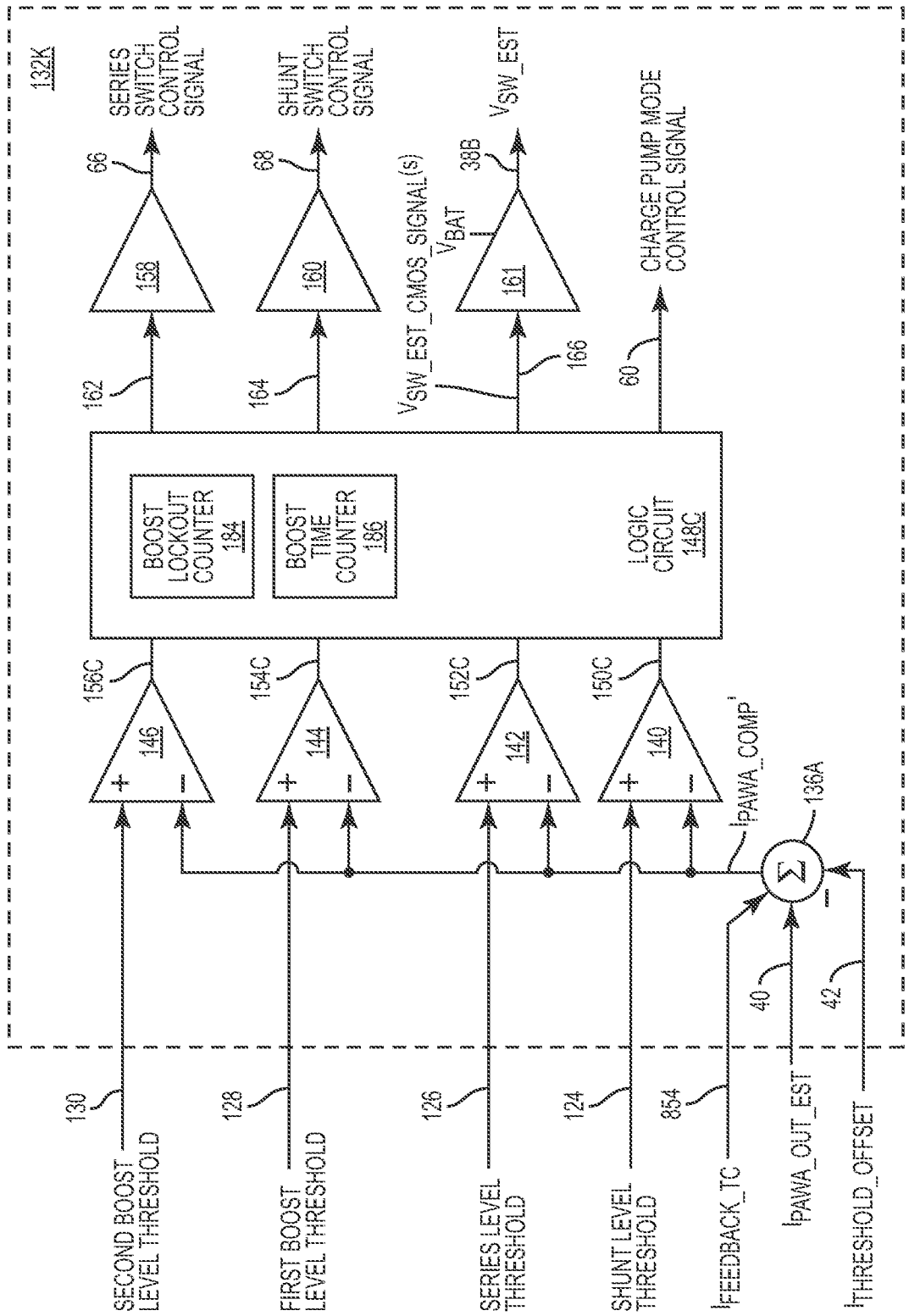

132K
SERIES SWITCH CONTROL SIGNAL
66
158
SHUNT SWITCH CONTROL SIGNAL
68
160
V_{SW_EST}
38B
161
V_{BAT}
$V_{SW_EST_CMOS_SIGNAL(S)}$
CHARGE PUMP MODE CONTROL SIGNAL
60
162
164
166
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148C
156C
154C
152C
150C
146
144
142
140
I_{PAWA_COMP}
136A
130
128
126
124
854
40
42
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{FEEDBACK_TC}$
$I_{PAWA_OUT_EST}$
$I_{THRESHOLD_OFFSET}$

FIG. 4K

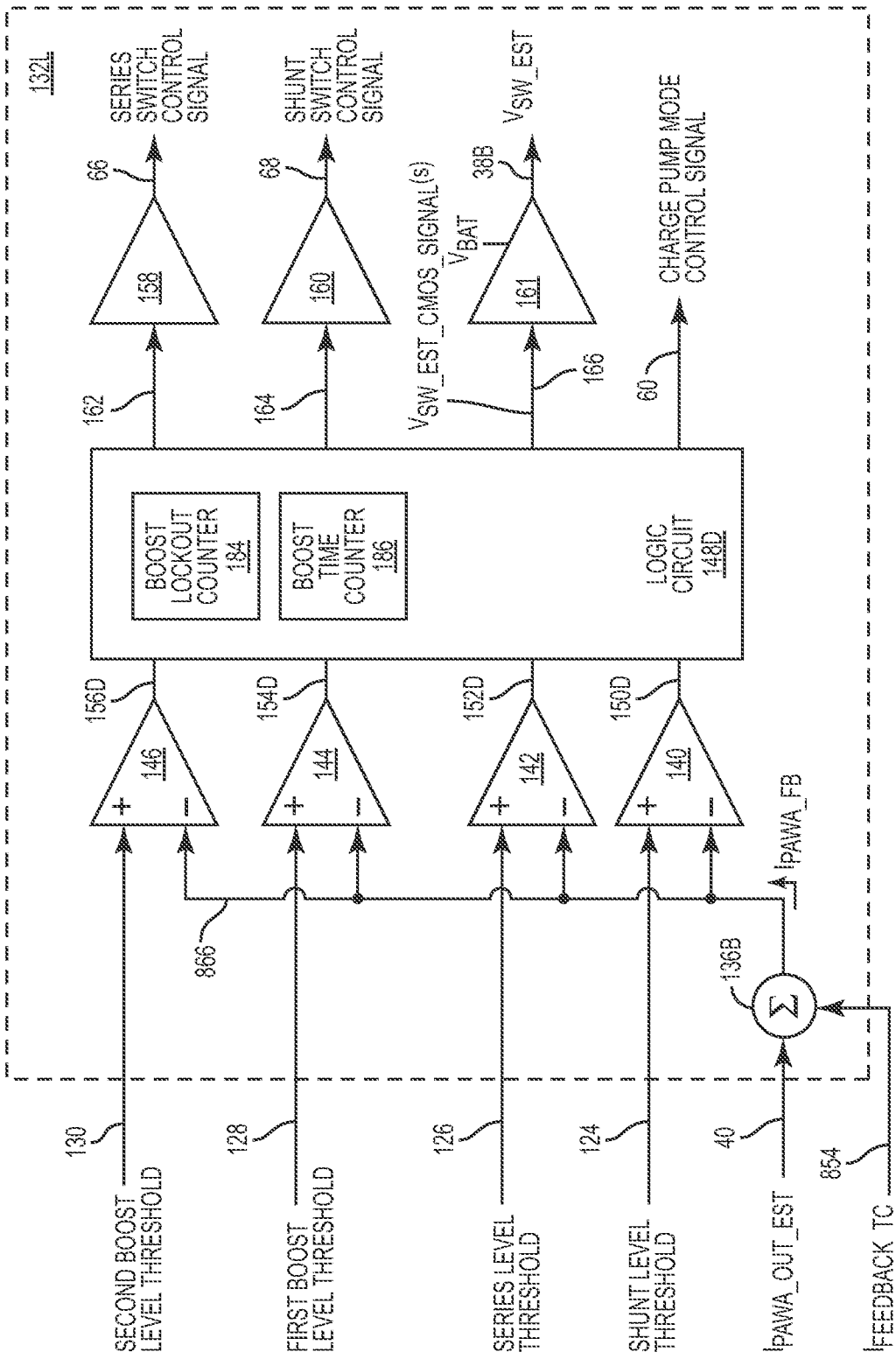

132L
SERIES SWITCH CONTROL SIGNAL
66
158
SHUNT SWITCH CONTROL SIGNAL
68
160
V_{SW_EST}
38B
161
CHARGE PUMP MODE CONTROL SIGNAL
60
162
164
$V_{SW_EST_CMOS_SIGNAL(s)}$
V_{BAT}
166
BOOST LOCKOUT COUNTER 194
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148D
156D
154D
152D
150D
146
144
142
140
866
136B
I_{PAWA_FB}
130
128
126
124
40
854
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$
$I_{FEEDBACK_TC}$

FIG. 4L

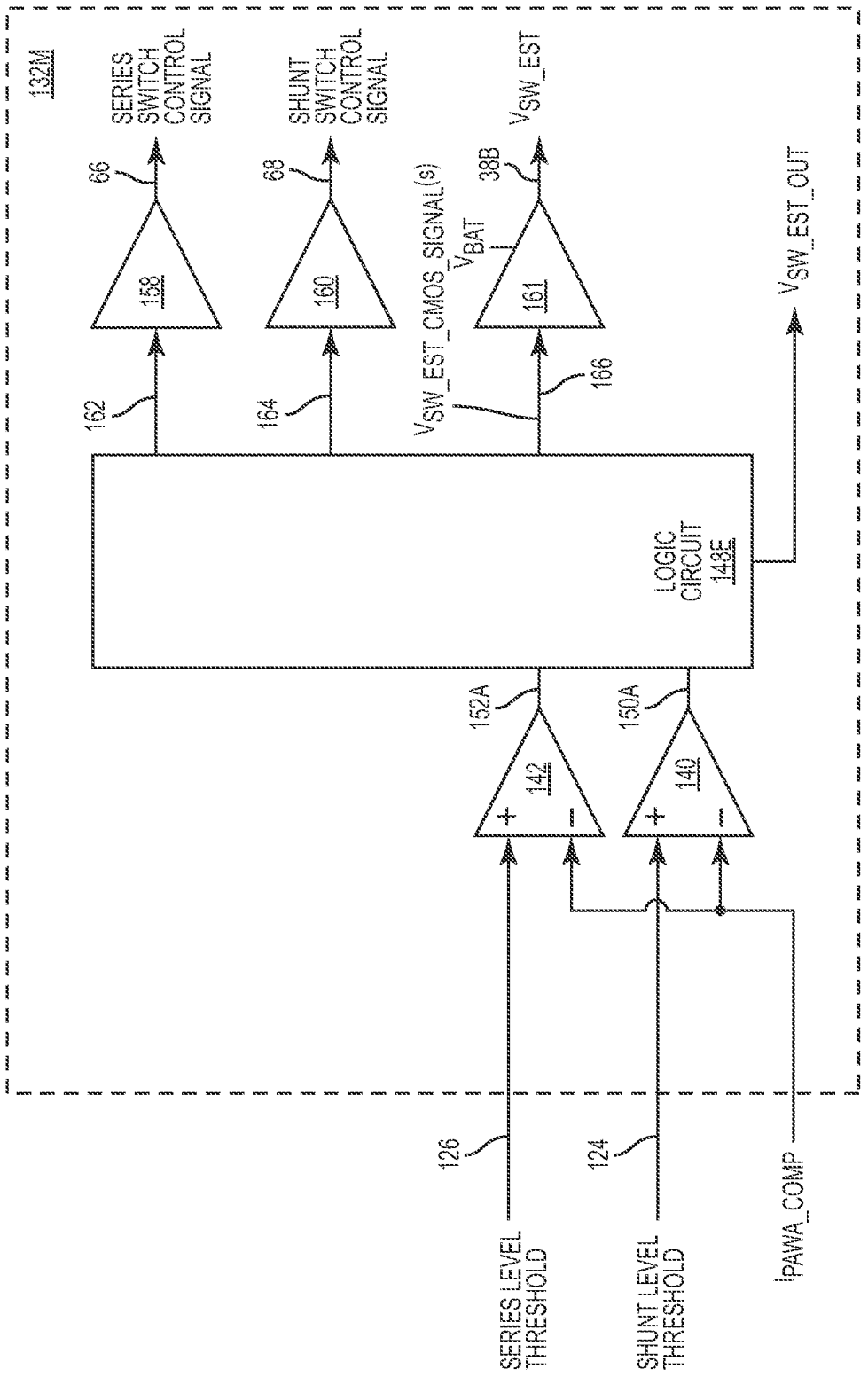

132M
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
V_{SW_EST}
66
68
38B
158
160
161
V_{BAT}
$V_{SW_EST_CMOS_SIGNAL(s)}$
162
164
166
$V_{SW_EST_OUT}$
LOGIC CIRCUIT 148E
152A
150A
142
140
126
124
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
I_{PAWA_COMP}

FIG. 4M

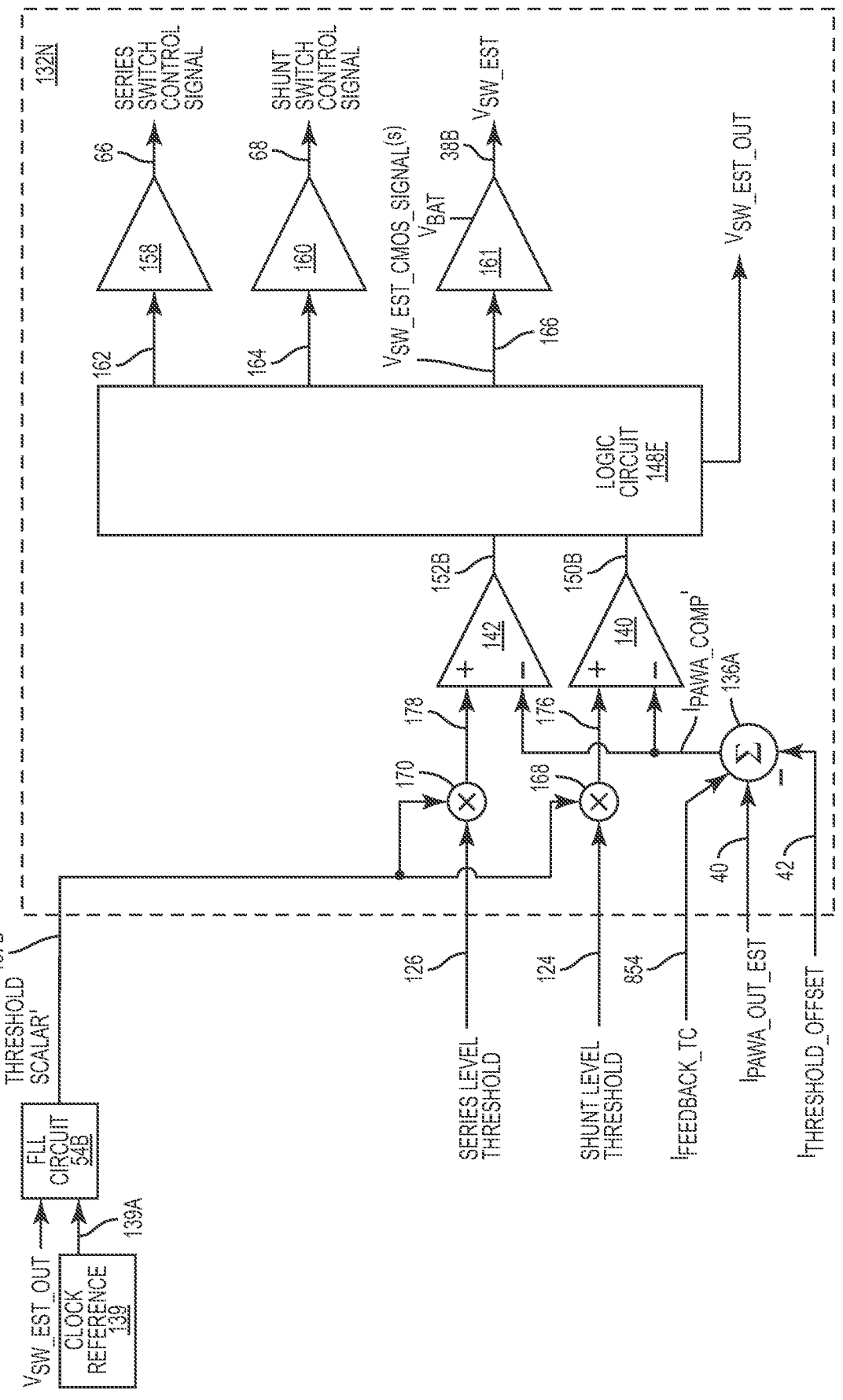

132N
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
VSW_EST
VSW_EST_OUT
66
68
38B
158
160
161
VBAT
VSW_EST_CMOS_SIGNAL(s)
162
164
166
LOGIC CIRCUIT 148E
152B
150B
142
140
178
176
170
168
IPAWA_COMP'
136A
126
124
854
40
42
137B
THRESHOLD SCALAR'
FLL CIRCUIT 54B
139A
CLOCK REFERENCE 139
VSW_EST_OUT
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
IFEEDBACK_TC
IPAWA_OUT_EST
ITHRESHOLD_OFFSET

FIG. 4N

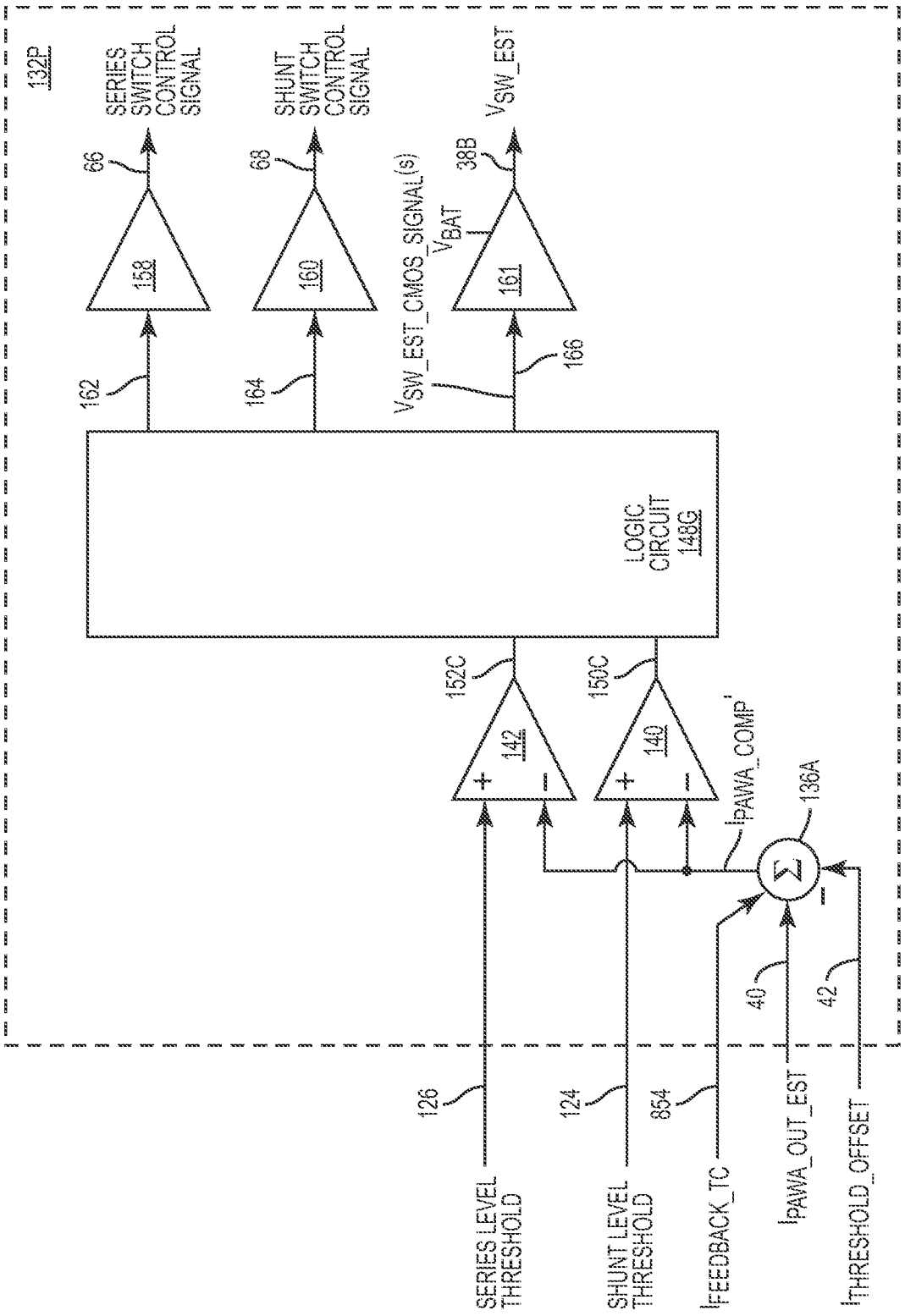

132P
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
V_{SW_EST}
66
68
38B
158
160
161
V_{BAT}
$V_{SW_EST_CMOS_SIGNAL(S)}$
162
164
166
LOGIC CIRCUIT 148G
152C
150C
142
140
I_{PAWA_COMP}'
136A
126
124
854
40
42
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{FEEDBACK_TC}$
$I_{PAWA_OUT_EST}$
$I_{THRESHOLD_OFFSET}$

FIG. 4P

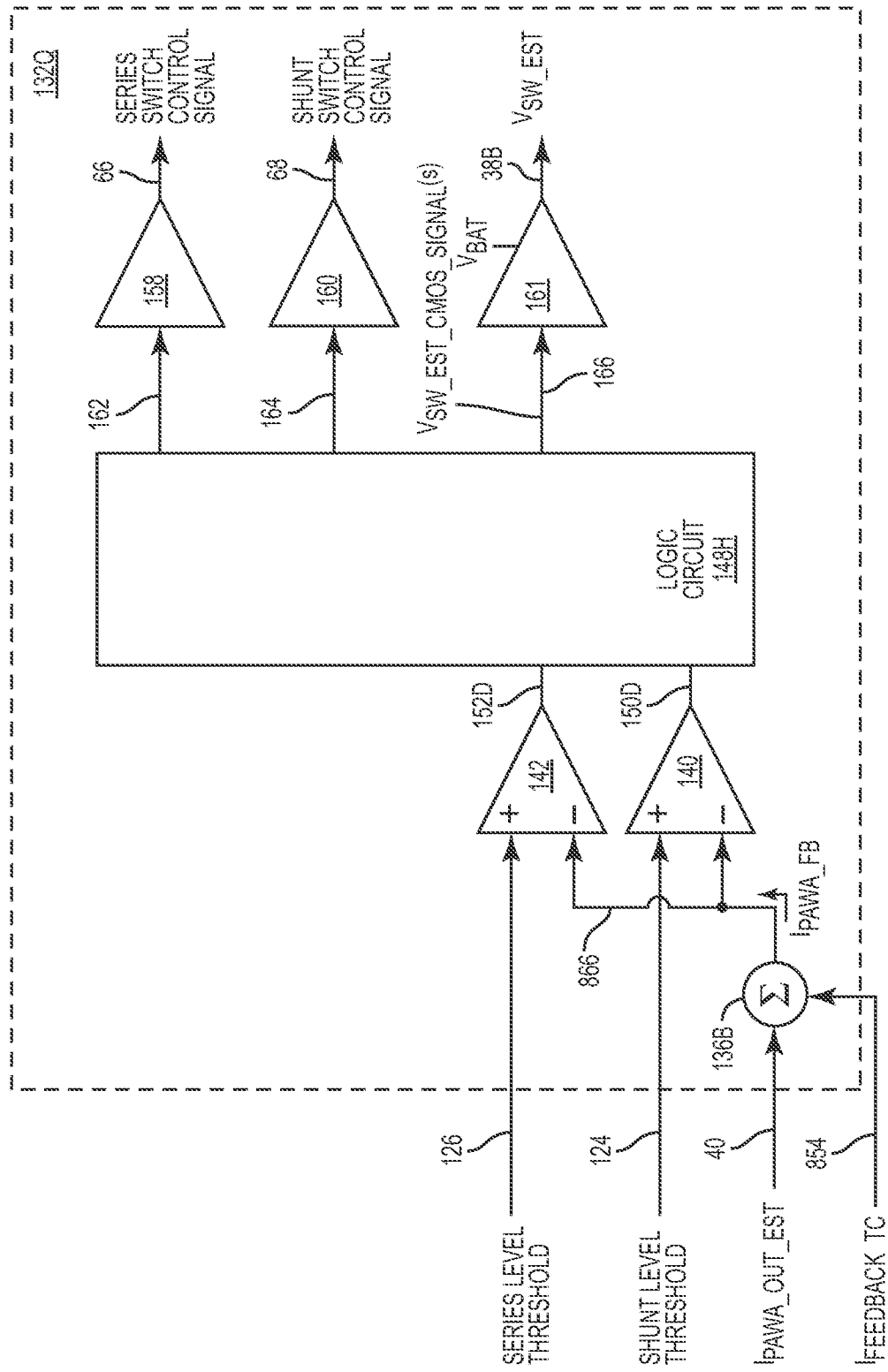

132Q
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
V_{SW_EST}
66
68
38B
158
160
161
V_{BAT}
$V_{SW_EST_CMOS_SIGNAL(S)}$
162
164
166
LOGIC CIRCUIT 148H
152D
150D
142
140
866
I_{PAWA_FB}
136B
126
124
40
854
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$
$I_{FEEDBACK_TC}$

FIG. 4Q

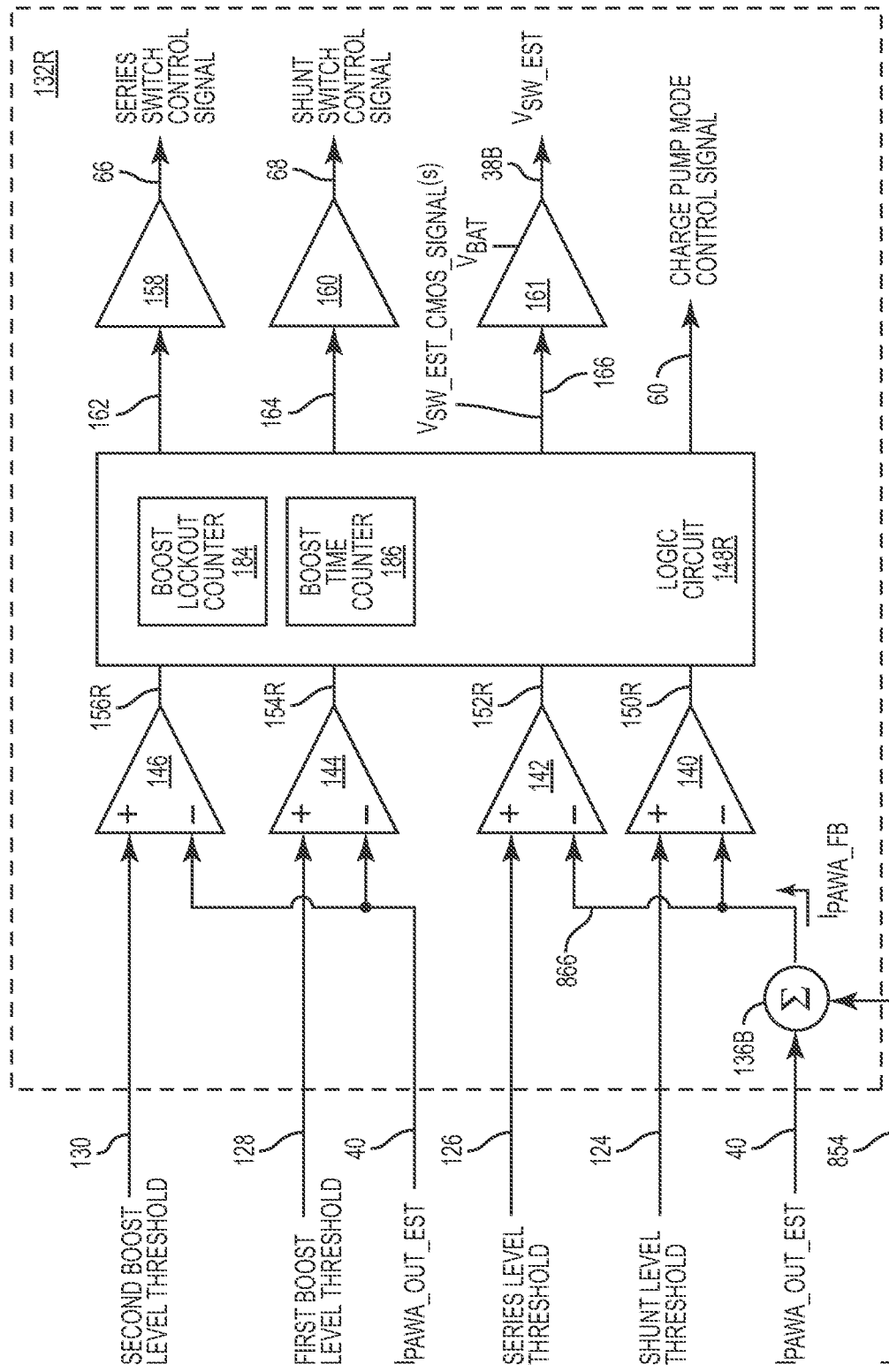

132R
SERIES SWITCH CONTROL SIGNAL
66
158
SHUNT SWITCH CONTROL SIGNAL
68
160
V_{SW_EST}
38B
V_{BAT}
161
$V_{SW_EST_CMOS_SIGNAL(s)}$
CHARGE PUMP MODE CONTROL SIGNAL
60
162
164
166
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148R
156R
154R
152R
150R
146
144
142
140
130
128
40
126
124
40
854
136B
866
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$
SERIES LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
$I_{PAWA_OUT_EST}$
I_{PAWA_FB}
$I_{FEEDBACK_TC}$

FIG. 4R

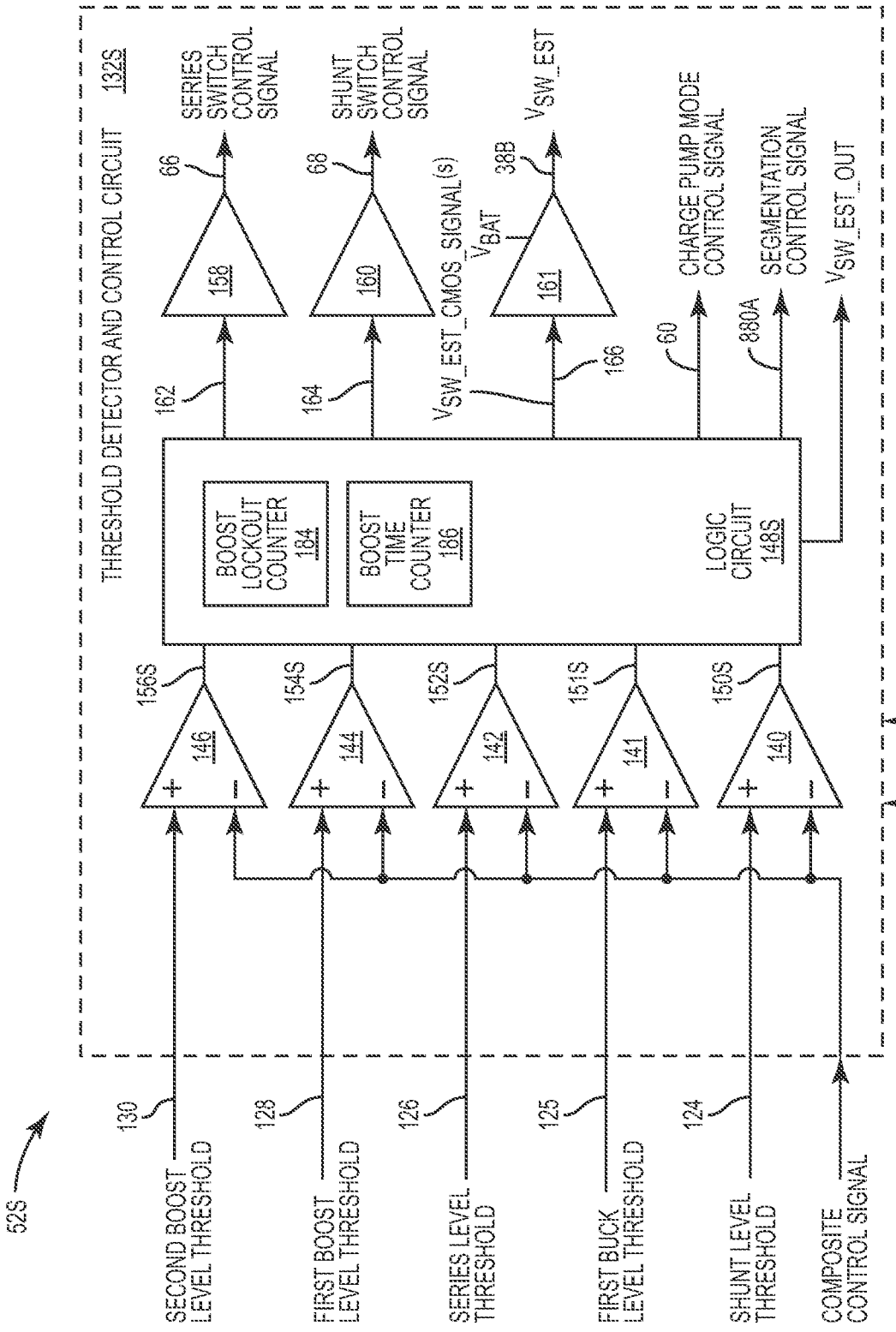

52S
THRESHOLD DETECTOR AND CONTROL CIRCUIT 132S
SECOND BOOST LEVEL THRESHOLD
FIRST BOOST LEVEL THRESHOLD
SERIES LEVEL THRESHOLD
FIRST BUCK LEVEL THRESHOLD
SHUNT LEVEL THRESHOLD
COMPOSITE CONTROL SIGNAL
130
128
126
125
124
156S
154S
152S
151S
150S
146
144
142
141
140
BOOST LOCKOUT COUNTER 184
BOOST TIME COUNTER 186
LOGIC CIRCUIT 148S
162
164
166
158
160
161
66
68
38B
SERIES SWITCH CONTROL SIGNAL
SHUNT SWITCH CONTROL SIGNAL
VSW_EST_CMOS_SIGNAL(S)
VBAT
VSW_EST
60
880A
CHARGE PUMP MODE CONTROL SIGNAL
SEGMENTATION CONTROL SIGNAL
VSW_EST_OUT
CONTROL BUS
44
131
MODE SWITCH CONTROL SIGNAL
CONTROLLER 50

FIG. 4S

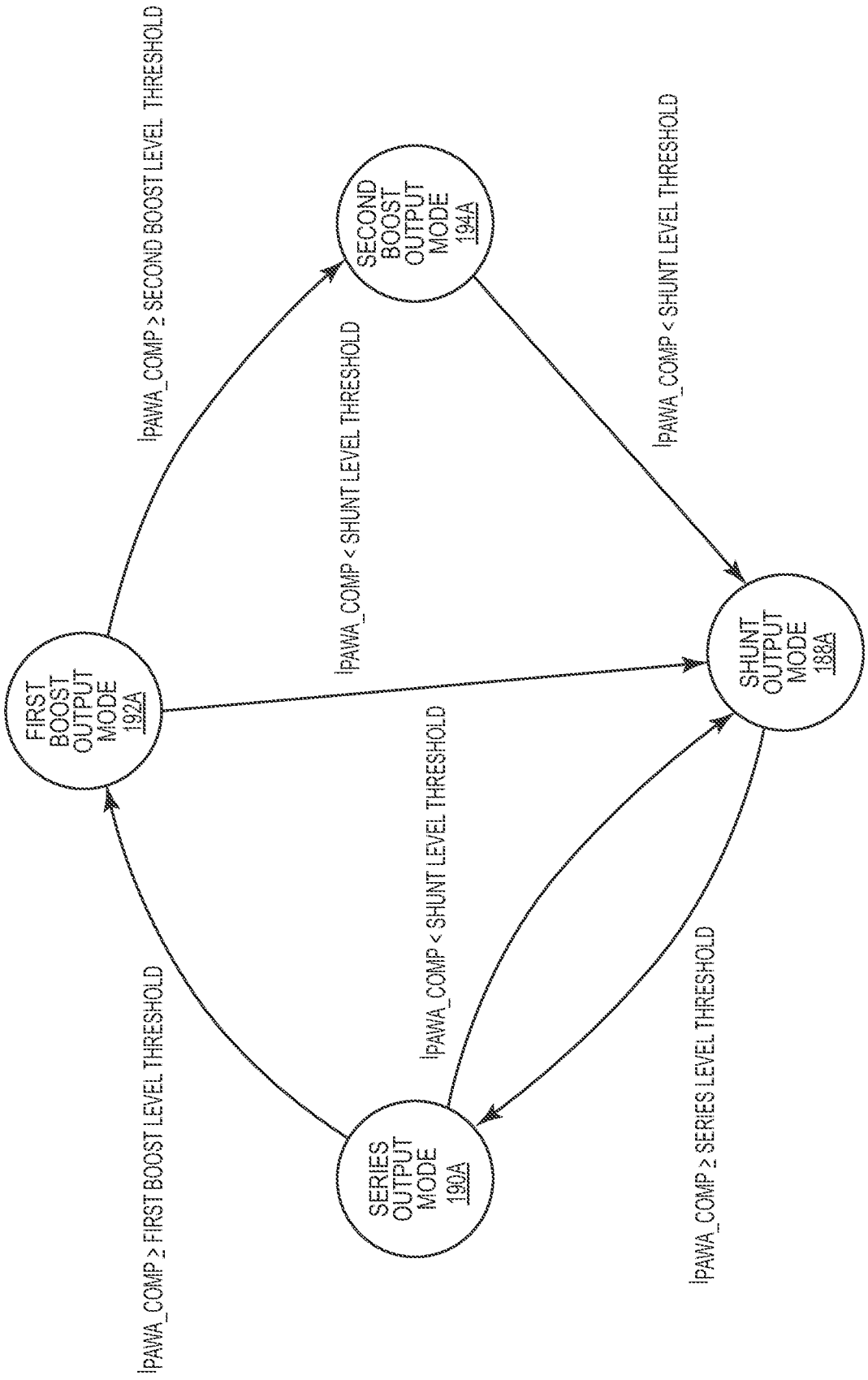

FIRST BOOST OUTPUT MODE 192A
SECOND BOOST OUTPUT MODE 194A
SHUNT OUTPUT MODE 188A
SERIES OUTPUT MODE 190A
|PAWA_COMP ≥ SECOND BOOST LEVEL THRESHOLD
|PAWA_COMP < SHUNT LEVEL THRESHOLD
|PAWA_COMP < SHUNT LEVEL THRESHOLD
|PAWA_COMP ≥ FIRST BOOST LEVEL THRESHOLD
|PAWA_COMP < SHUNT LEVEL THRESHOLD
|PAWA_COMP ≥ SERIES LEVEL THRESHOLD

FIG. 5A

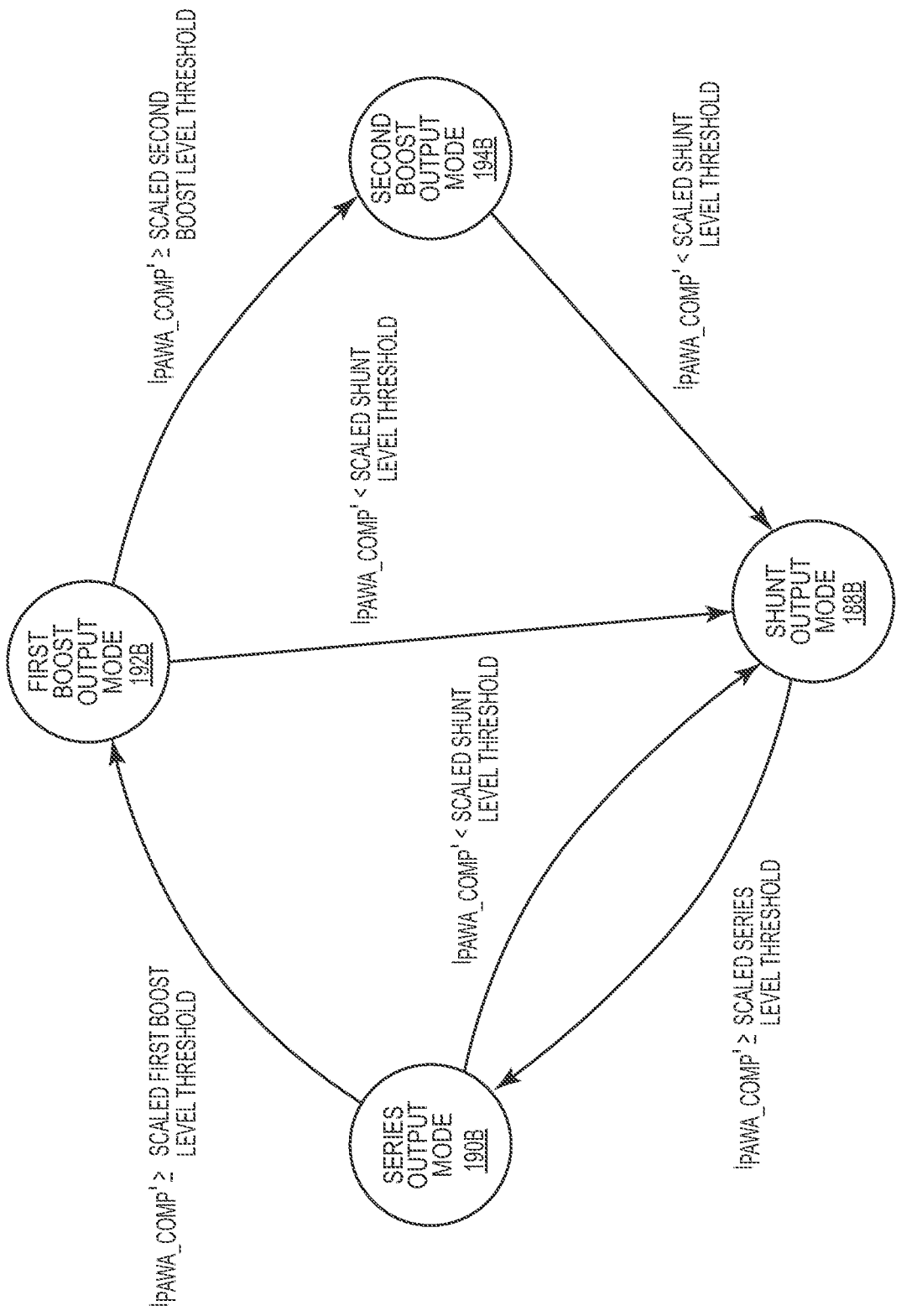

FIRST BOOST OUTPUT MODE 192B
SECOND BOOST OUTPUT MODE 194B
SERIES OUTPUT MODE 190B
SHUNT OUTPUT MODE 188B
IPAWA_COMP' ≥ SCALED SECOND BOOST LEVEL THRESHOLD
IPAWA_COMP' < SCALED SHUNT LEVEL THRESHOLD
IPAWA_COMP' < SCALED SHUNT LEVEL THRESHOLD
IPAWA_COMP' ≥ SCALED FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' < SCALED SHUNT LEVEL THRESHOLD
IPAWA_COMP' ≥ SCALED SERIES LEVEL THRESHOLD

FIG. 5B

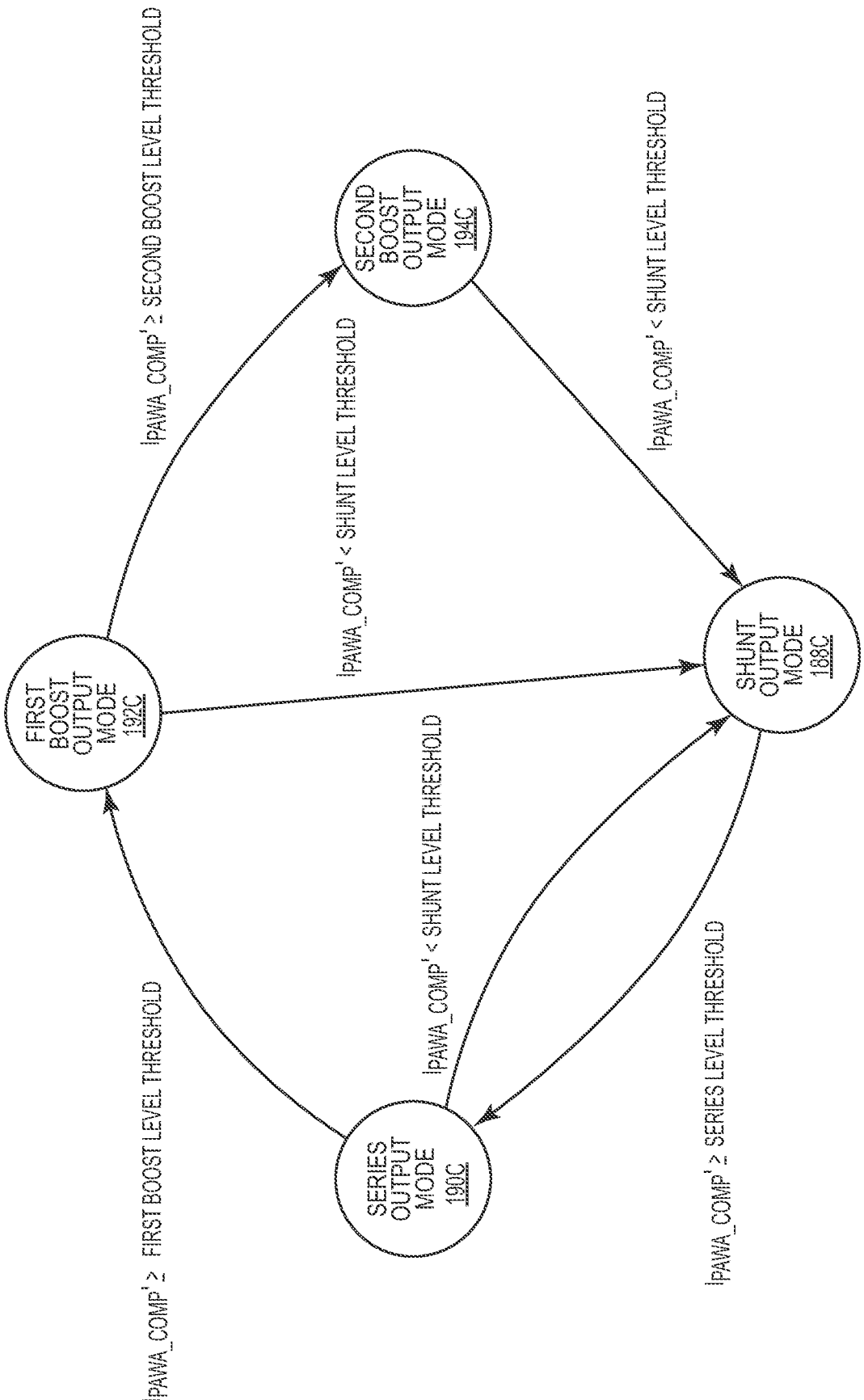

FIRST BOOST OUTPUT MODE 192C
SECOND BOOST OUTPUT MODE 194C
SERIES OUTPUT MODE 190C
SHUNT OUTPUT MODE 188C
IPAWA_COMP' ≥ SECOND BOOST LEVEL THRESHOLD
IPAWA_COMP' < SHUNT LEVEL THRESHOLD
IPAWA_COMP' < SHUNT LEVEL THRESHOLD
IPAWA_COMP' ≥ FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' < SHUNT LEVEL THRESHOLD
IPAWA_COMP' ≥ SERIES LEVEL THRESHOLD

FIG. 5C

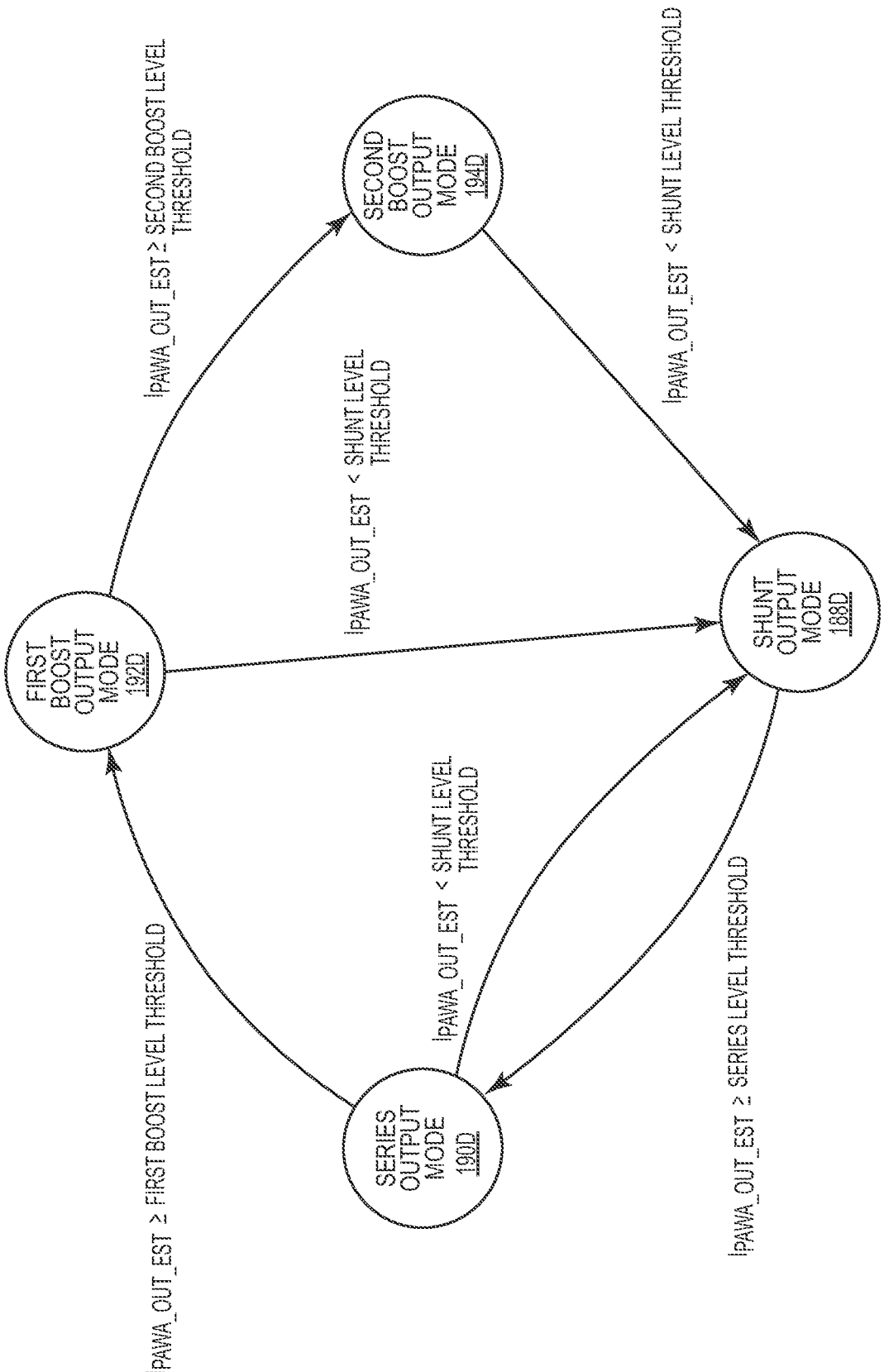

FIRST BOOST OUTPUT MODE 192D
SECOND BOOST OUTPUT MODE 194D
SHUNT OUTPUT MODE 188D
SERIES OUTPUT MODE 190D
IPAWA_OUT_EST ≥ SECOND BOOST LEVEL THRESHOLD
IPAWA_OUT_EST < SHUNT LEVEL THRESHOLD
IPAWA_OUT_EST < SHUNT LEVEL THRESHOLD
IPAWA_OUT_EST ≥ FIRST BOOST LEVEL THRESHOLD
IPAWA_OUT_EST < SHUNT LEVEL THRESHOLD
IPAWA_OUT_EST ≥ SERIES LEVEL THRESHOLD

FIG. 5D

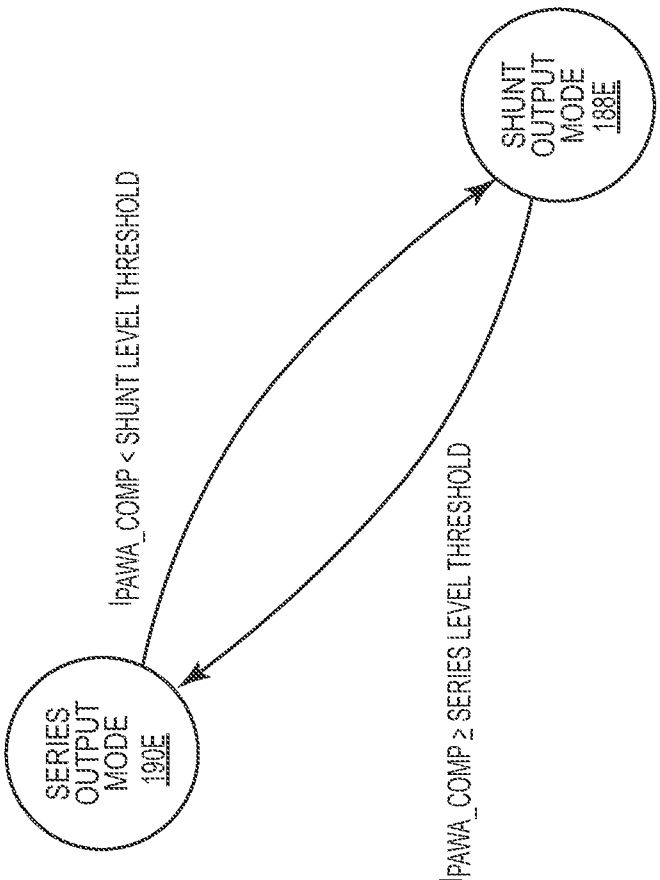

SERIES OUTPUT MODE 190E
SHUNT OUTPUT MODE 188E
IPAWA_COMP < SHUNT LEVEL THRESHOLD
IPAWA_COMP ≥ SERIES LEVEL THRESHOLD

FIG. 5E

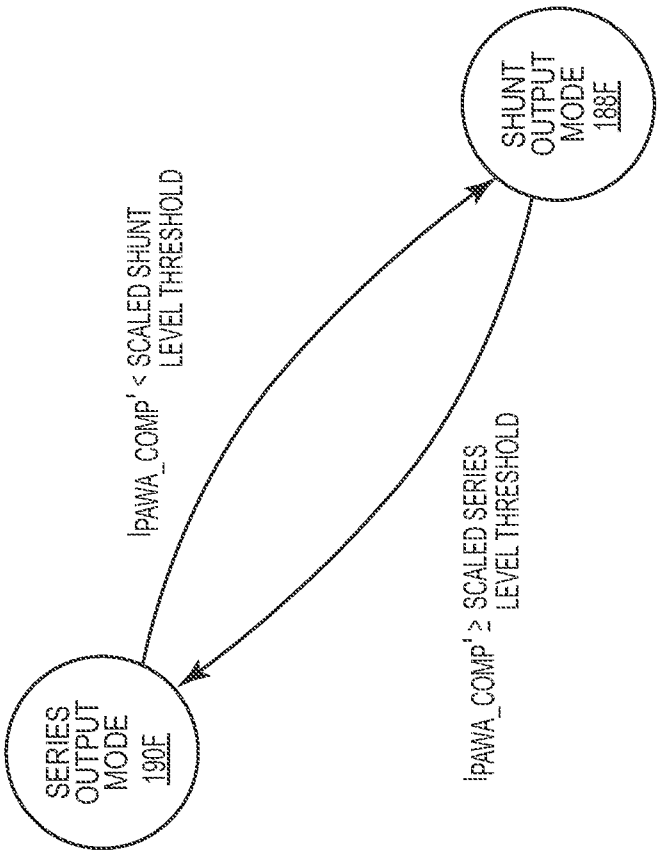

SERIES OUTPUT MODE 190E
SHUNT OUTPUT MODE 188E
|PAWA_COMP'| < SCALED SHUNT LEVEL THRESHOLD
|PAWA_COMP'| ≥ SCALED SERIES LEVEL THRESHOLD

FIG. 5F

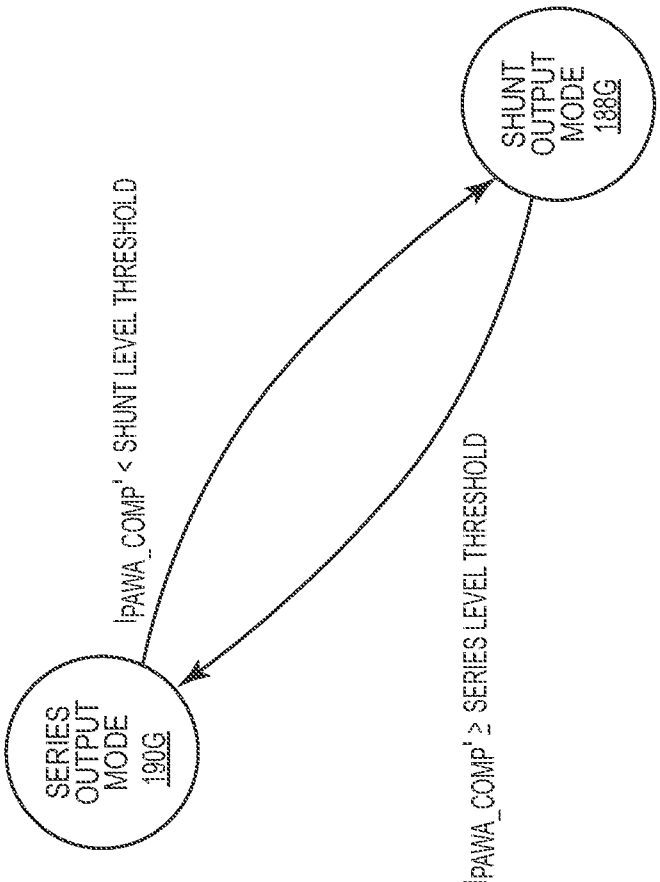

SERIES OUTPUT MODE 190G
SHUNT OUTPUT MODE 188G
IPAWA_COMP' < SHUNT LEVEL THRESHOLD
IPAWA_COMP' ≥ SERIES LEVEL THRESHOLD

FIG. 5G

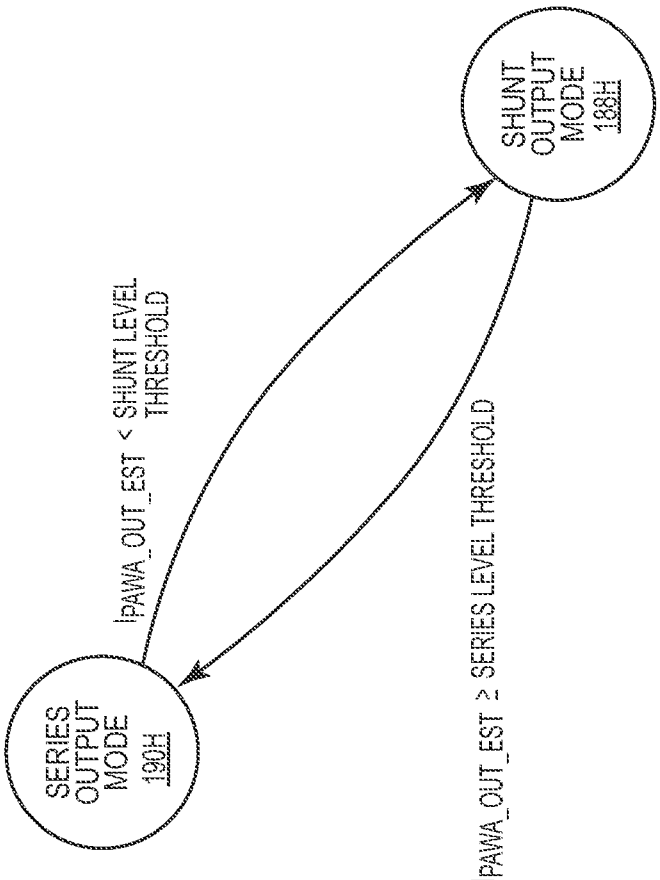

SERIES OUTPUT MODE 190H
SHUNT OUTPUT MODE 188H
IPAWA_OUT_EST < SHUNT LEVEL THRESHOLD
IPAWA_OUT_EST ≥ SERIES LEVEL THRESHOLD

FIG. 5H

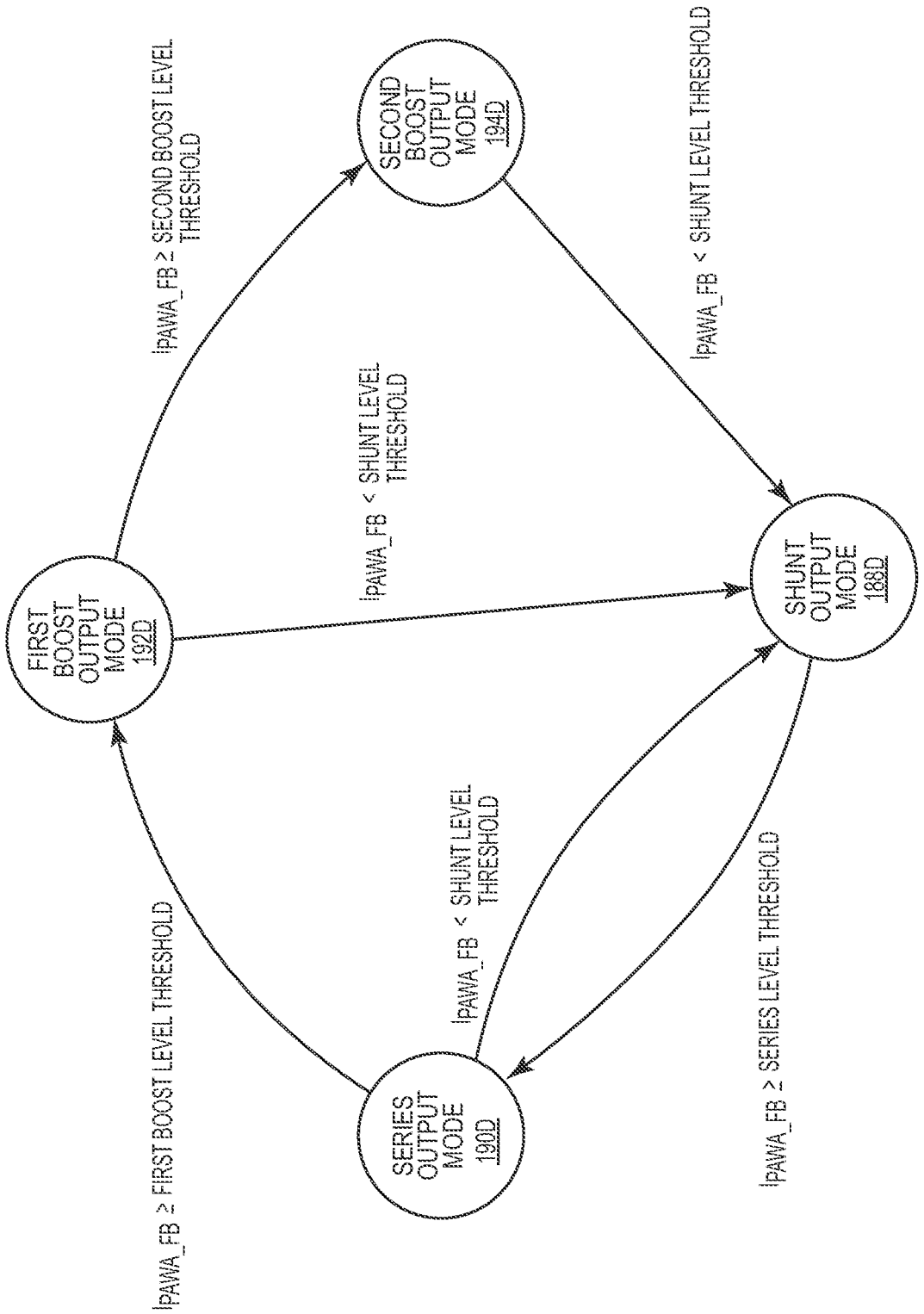

FIRST BOOST OUTPUT MODE 192D
SECOND BOOST OUTPUT MODE 194D
SERIES OUTPUT MODE 190D
SHUNT OUTPUT MODE 188D
IPAWA_FB ≥ SECOND BOOST LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
IPAWA_FB ≥ FIRST BOOST LEVEL THRESHOLD
IPAWA_FB ≥ SERIES LEVEL THRESHOLD

FIG. 5L

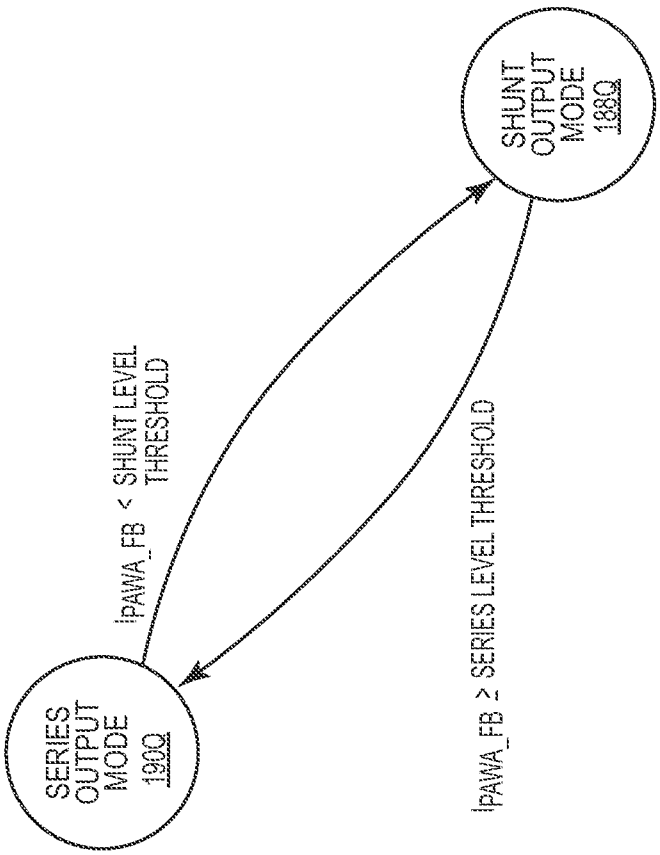

SERIES OUTPUT MODE 190Q
SHUNT OUTPUT MODE 188Q
IPAWA_FB < SHUNT LEVEL THRESHOLD
IPAWA_FB ≥ SERIES LEVEL THRESHOLD

FIG. 5Q

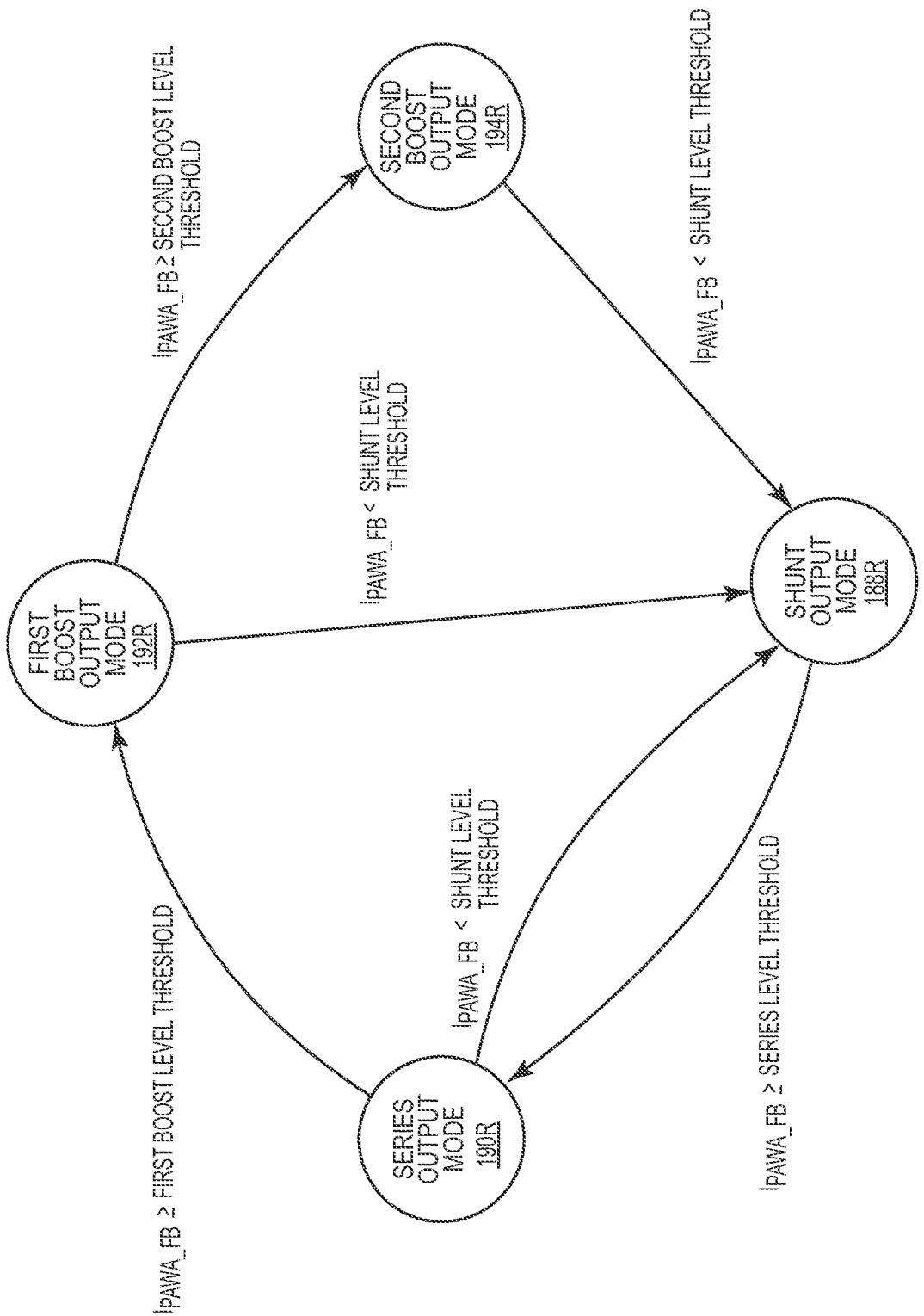

FIRST BOOST OUTPUT MODE 192R
SECOND BOOST OUTPUT MODE 194R
SHUNT OUTPUT MODE 188R
SERIES OUTPUT MODE 190R
IPAWA_FB ≥ SECOND BOOST LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
IPAWA_FB ≥ FIRST BOOST LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
IPAWA_FB ≥ SERIES LEVEL THRESHOLD

FIG. 5R

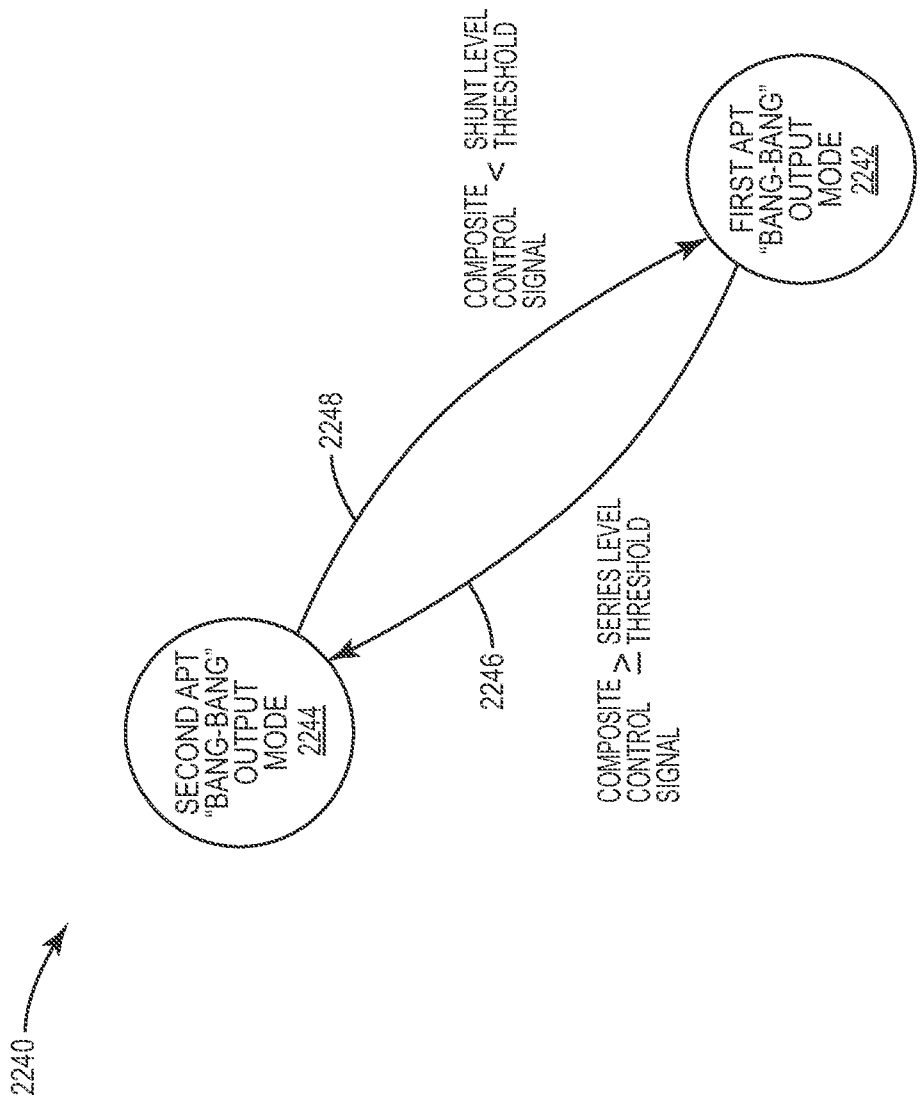

AVERAGE POWER TRACKING (APT) MODES
2240
SECOND APT "BANG-BANG" OUTPUT MODE 2244
FIRST APT "BANG-BANG" OUTPUT MODE 2242
2248
2246
COMPOSITE CONTROL SIGNAL < SHUNT LEVEL THRESHOLD
COMPOSITE CONTROL SIGNAL ≥ SERIES LEVEL THRESHOLD

FIG. 5S

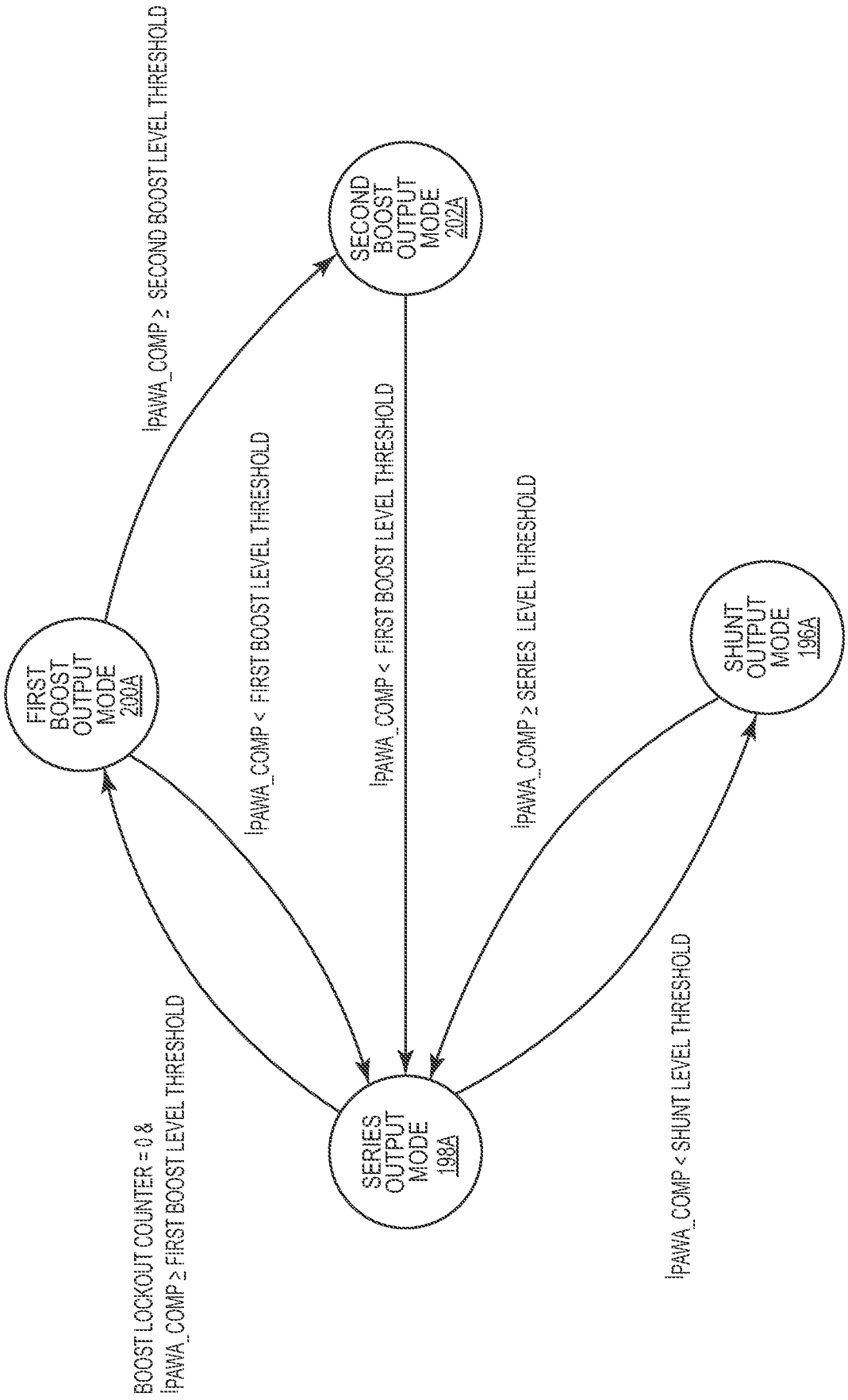

FIRST BOOST OUTPUT MODE 200A
SECOND BOOST OUTPUT MODE 202A
SERIES OUTPUT MODE 198A
SHUNT OUTPUT MODE 196A
IPAWA_COMP ≥ SECOND BOOST LEVEL THRESHOLD
IPAWA_COMP < FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP < FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP ≥ SERIES LEVEL THRESHOLD
BOOST LOCKOUT COUNTER = 0 &
IPAWA_COMP ≥ FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP < SHUNT LEVEL THRESHOLD

FIG. 6A

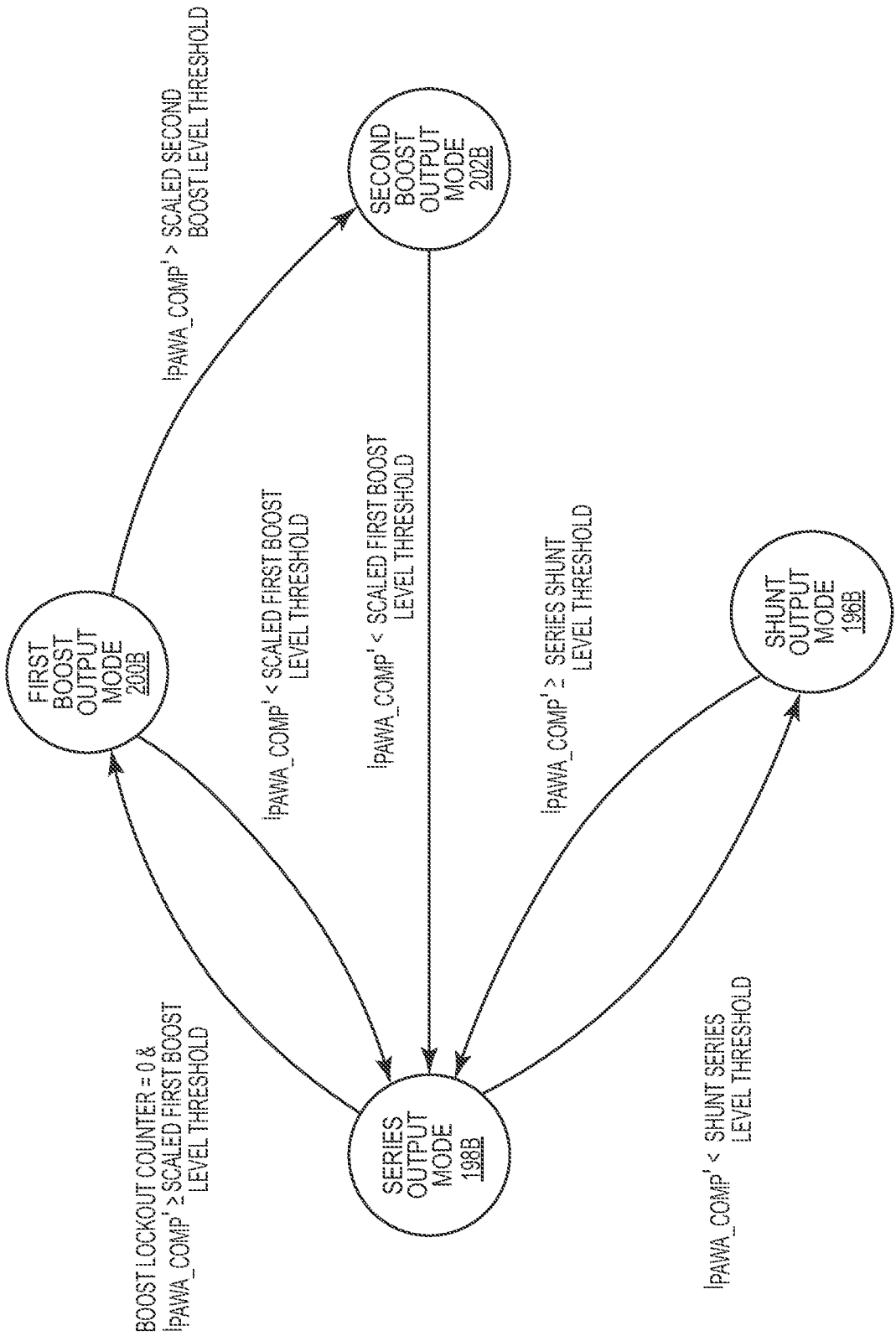

FIRST BOOST OUTPUT MODE 200B
SECOND BOOST OUTPUT MODE 202B
SERIES OUTPUT MODE 198B
SHUNT OUTPUT MODE 196B
IPAWA_COMP' > SCALED SECOND BOOST LEVEL THRESHOLD
IPAWA_COMP' < SCALED FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' < SCALED FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' ≥ SERIES SHUNT LEVEL THRESHOLD
BOOST LOCKOUT COUNTER = 0 & IPAWA_COMP' ≥ SCALED FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' < SHUNT SERIES LEVEL THRESHOLD

FIG. 6B

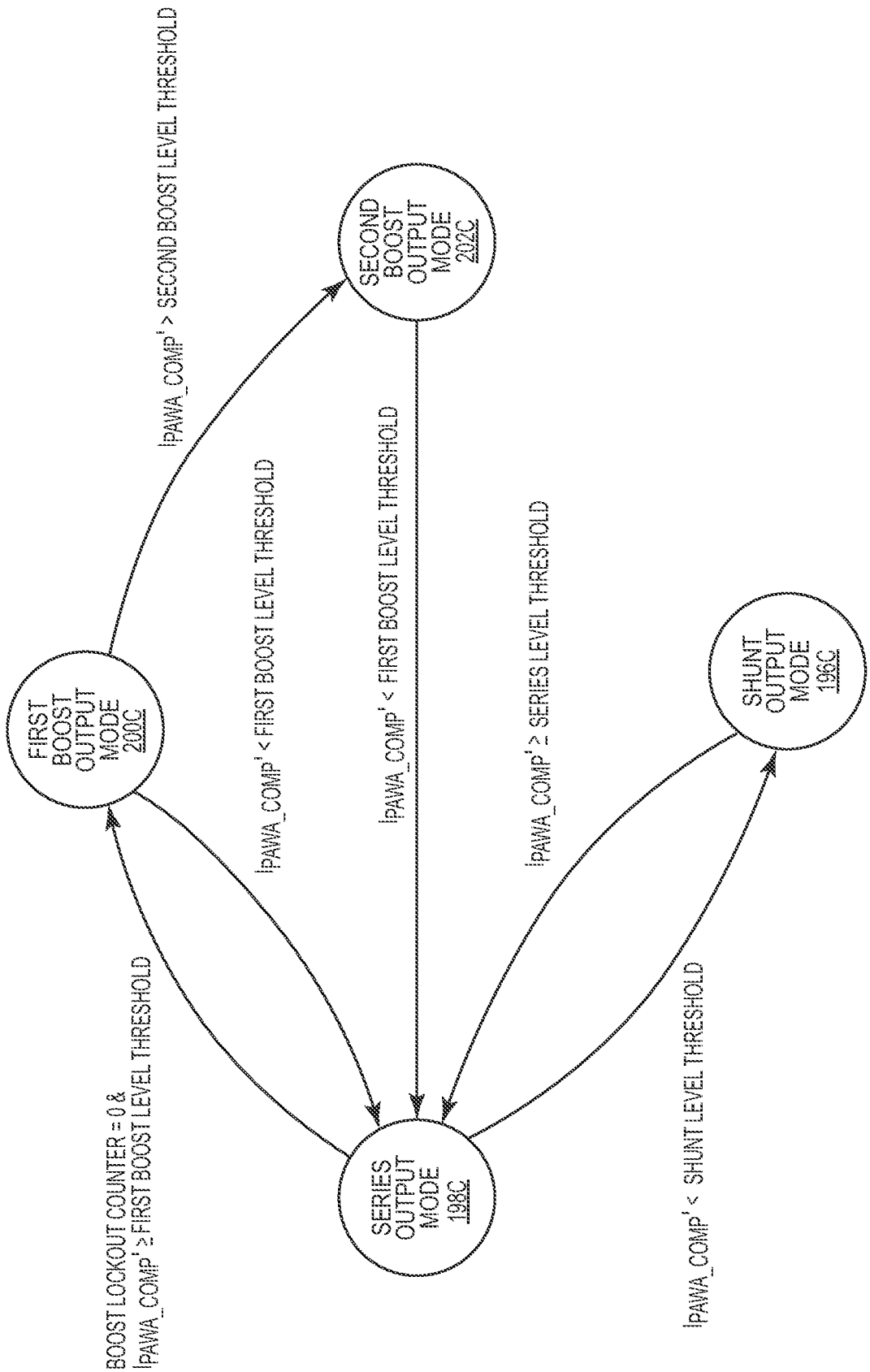

FIRST BOOST OUTPUT MODE 200C
SECOND BOOST OUTPUT MODE 202C
SERIES OUTPUT MODE 198C
SHUNT OUTPUT MODE 196C
IPAWA_COMP' > SECOND BOOST LEVEL THRESHOLD
IPAWA_COMP' < FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' < FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' ≥ SERIES LEVEL THRESHOLD
BOOST LOCKOUT COUNTER = 0 &
IPAWA_COMP' ≥ FIRST BOOST LEVEL THRESHOLD
IPAWA_COMP' < SHUNT LEVEL THRESHOLD

FIG. 6C

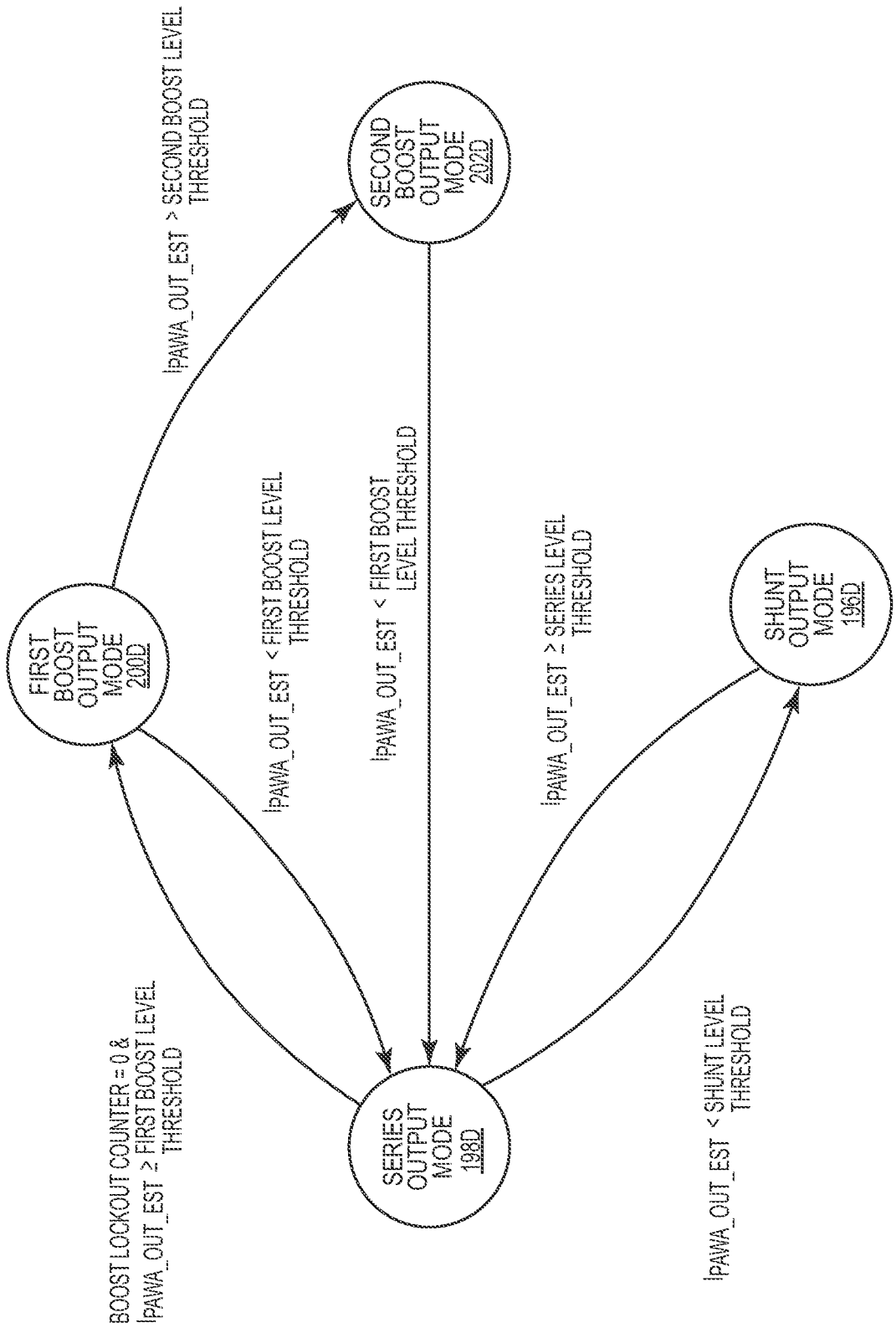

FIRST BOOST OUTPUT MODE 200D
SECOND BOOST OUTPUT MODE 202D
SERIES OUTPUT MODE 198D
SHUNT OUTPUT MODE 196D
IPAWA_OUT_EST > SECOND BOOST LEVEL THRESHOLD
IPAWA_OUT_EST < FIRST BOOST LEVEL THRESHOLD
IPAWA_OUT_EST < FIRST BOOST LEVEL THRESHOLD
IPAWA_OUT_EST ≥ SERIES LEVEL THRESHOLD
BOOST LOCKOUT COUNTER = 0 & IPAWA_OUT_EST ≥ FIRST BOOST LEVEL THRESHOLD
IPAWA_OUT_EST < SHUNT LEVEL THRESHOLD

FIG. 6D

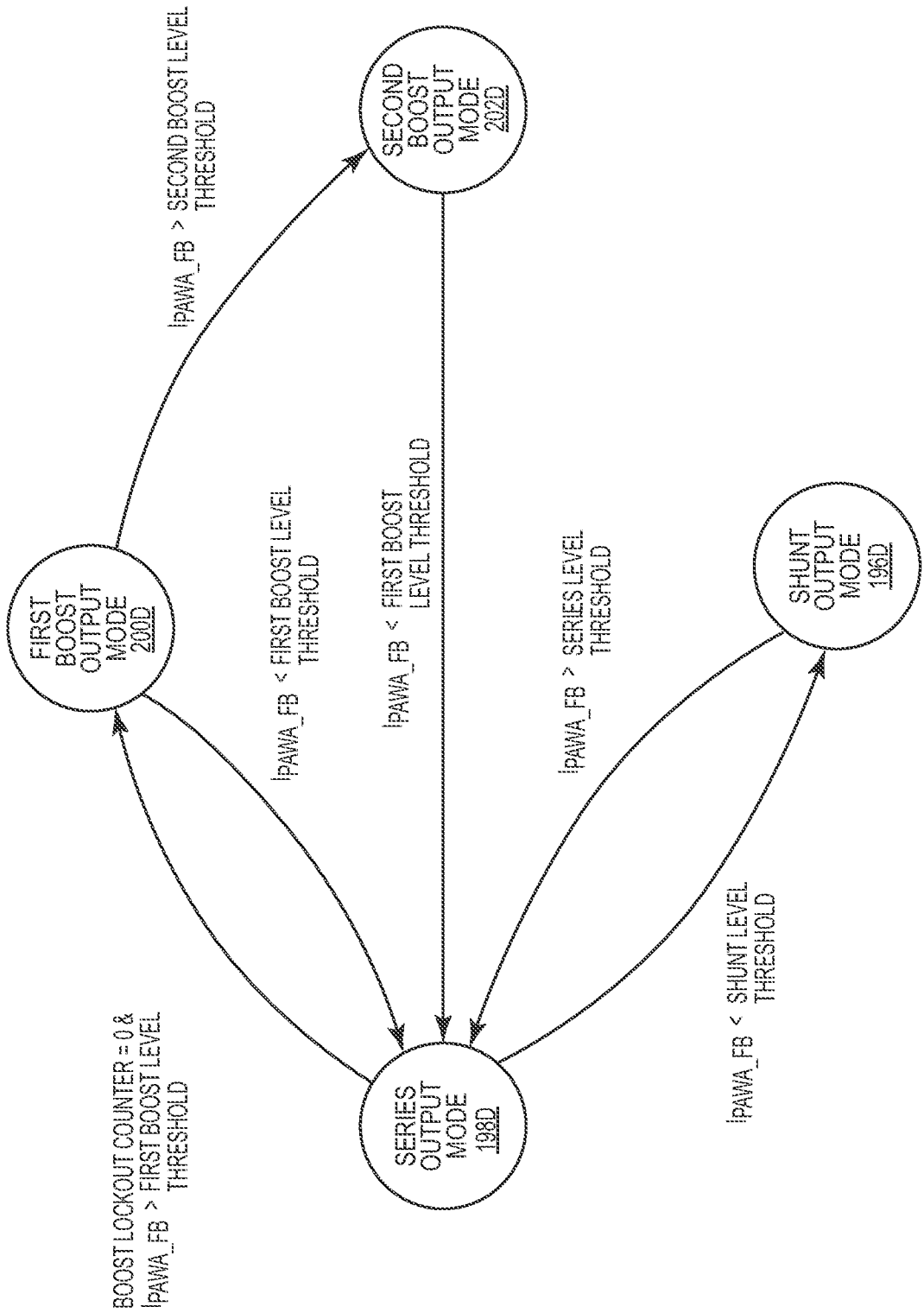

FIRST BOOST OUTPUT MODE 200D
SECOND BOOST OUTPUT MODE 202D
SERIES OUTPUT MODE 198D
SHUNT OUTPUT MODE 196D
IPAWA_FB > SECOND BOOST LEVEL THRESHOLD
IPAWA_FB < FIRST BOOST LEVEL THRESHOLD
IPAWA_FB < FIRST BOOST LEVEL THRESHOLD
IPAWA_FB > SERIES LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
BOOST LOCKOUT COUNTER = 0 & IPAWA_FB > FIRST BOOST LEVEL THRESHOLD

FIG. 6L

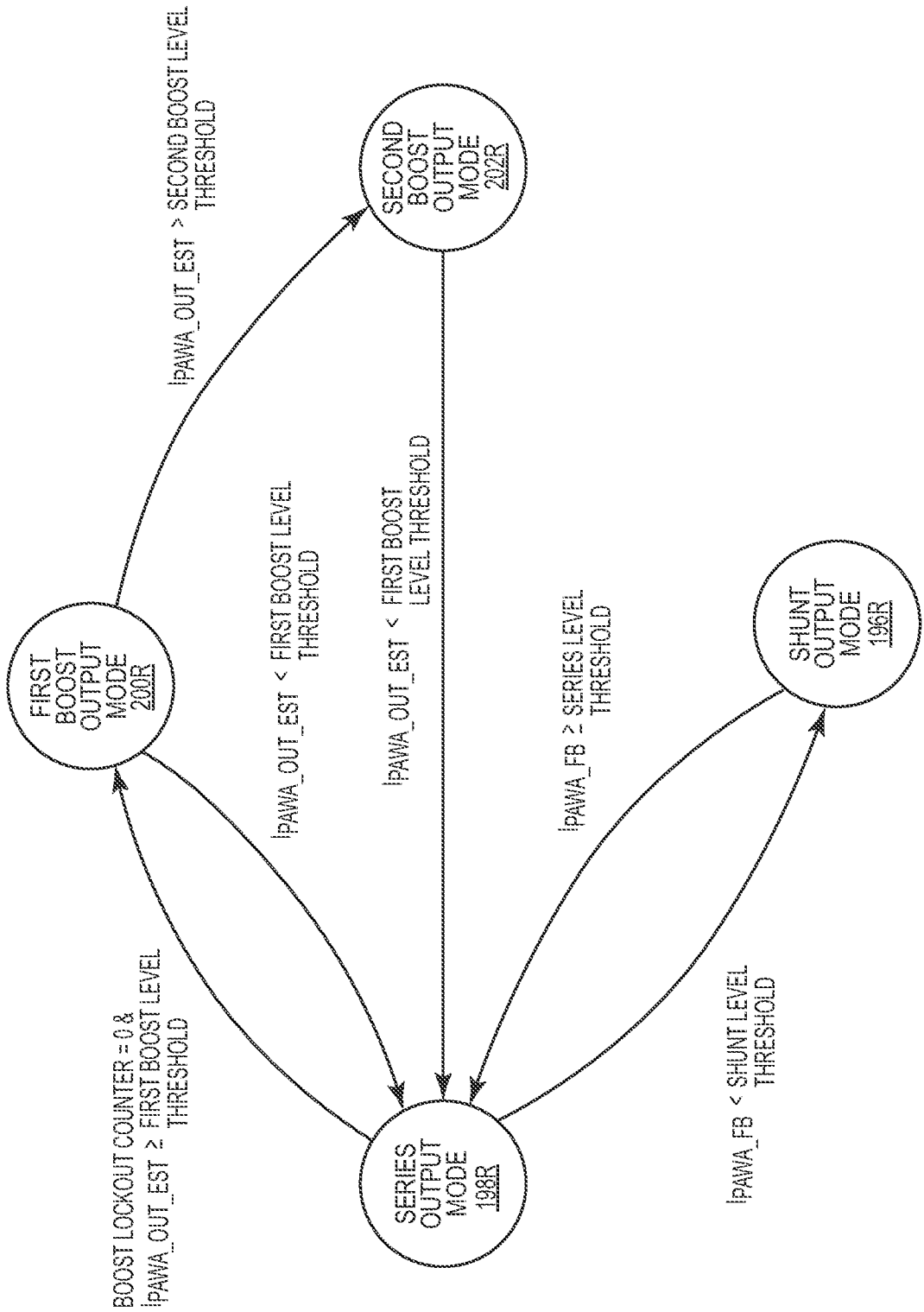

FIRST BOOST OUTPUT MODE 200R
SECOND BOOST OUTPUT MODE 202R
SERIES OUTPUT MODE 198R
SHUNT OUTPUT MODE 196R
IPAWA_OUT_EST > SECOND BOOST LEVEL THRESHOLD
IPAWA_OUT_EST < FIRST BOOST LEVEL THRESHOLD
IPAWA_OUT_EST < FIRST BOOST LEVEL THRESHOLD
IPAWA_FB ≥ SERIES LEVEL THRESHOLD
IPAWA_FB < SHUNT LEVEL THRESHOLD
BOOST LOCKOUT COUNTER = 0 & IPAWA_OUT_EST ≥ FIRST BOOST LEVEL THRESHOLD

FIG. 6R

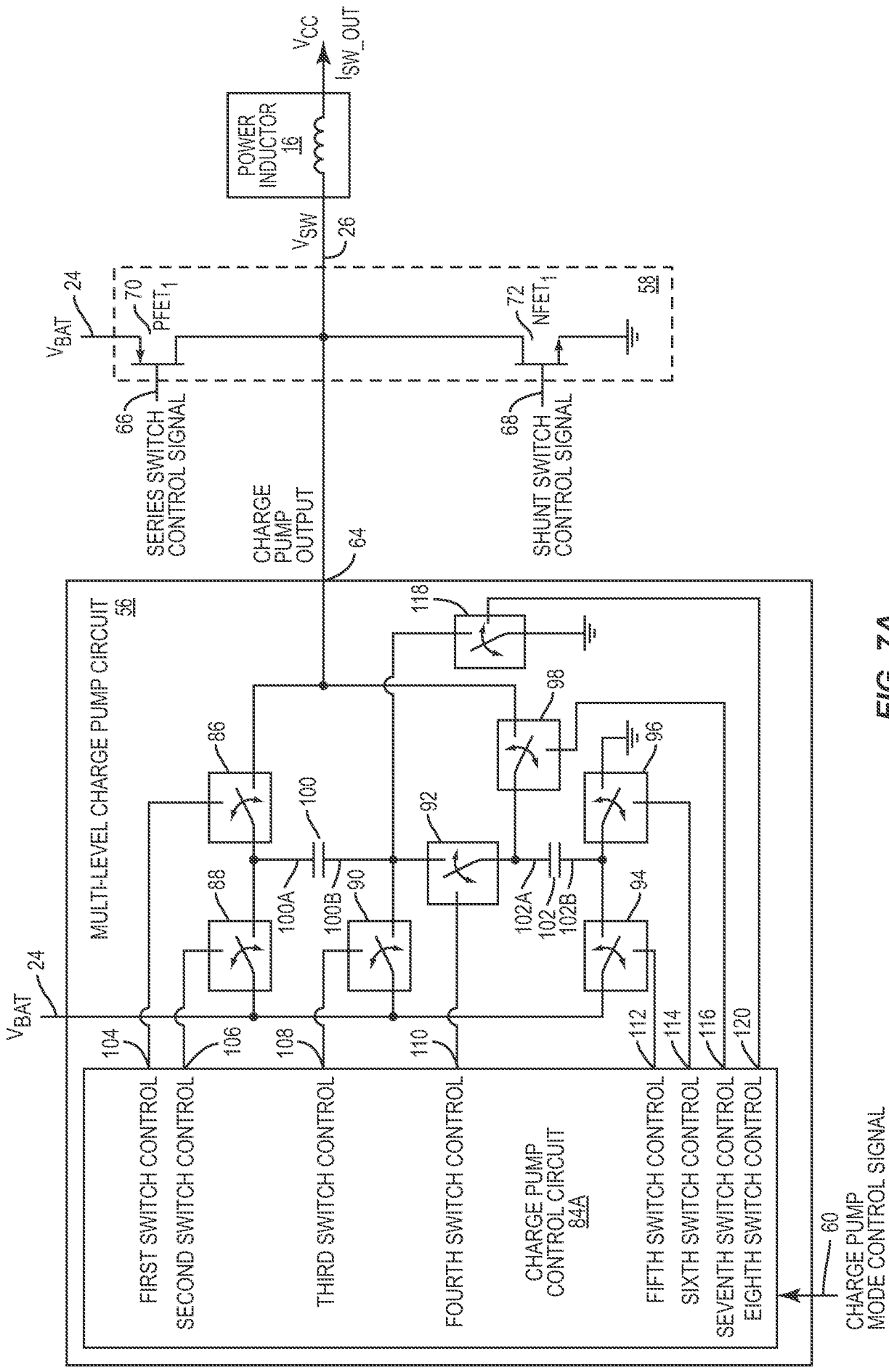

V_{CC}
I_{SW_OUT}
POWER INDUCTOR 16
V_{SW}
26
V_{BAT} 24
70 $PFET_1$
72 $NFET_1$
58
66 SERIES SWITCH CONTROL SIGNAL
68 SHUNT SWITCH CONTROL SIGNAL
CHARGE PUMP OUTPUT
64
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
V_{BAT} 24
86
88
100
100A
100B
90
92
98
96
94
102A
102
102B
118
104
106
108
110
112
114
116
120
FIRST SWITCH CONTROL
SECOND SWITCH CONTROL
THIRD SWITCH CONTROL
FOURTH SWITCH CONTROL
CHARGE PUMP CONTROL CIRCUIT 84A
FIFTH SWITCH CONTROL
SIXTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
60
CHARGE PUMP MODE CONTROL SIGNAL

FIG. 7A

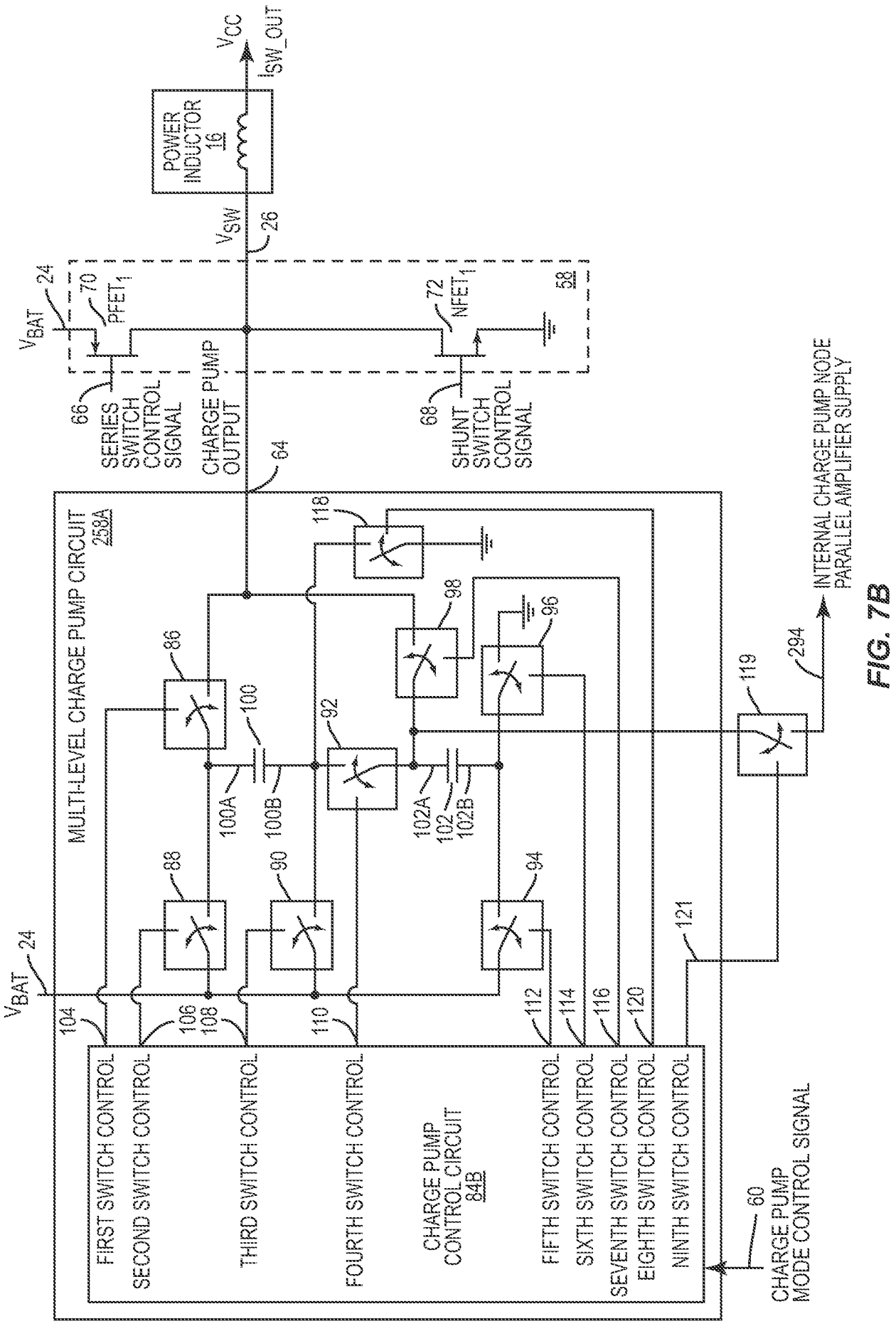

MULTI-LEVEL CHARGE PUMP CIRCUIT 258A
FIRST SWITCH CONTROL
SECOND SWITCH CONTROL
THIRD SWITCH CONTROL
FOURTH SWITCH CONTROL
CHARGE PUMP CONTROL CIRCUIT 84B
FIFTH SWITCH CONTROL
SIXTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
NINTH SWITCH CONTROL
CHARGE PUMP MODE CONTROL SIGNAL
60
V_{BAT}
24
104
106
108
110
112
114
116
120
121
88
86
90
92
94
96
98
100
100A
100B
102
102A
102B
118
119
294
INTERNAL CHARGE PUMP NODE PARALLEL AMPLIFIER SUPPLY
CHARGE PUMP OUTPUT
64
SERIES SWITCH CONTROL SIGNAL
66
SHUNT SWITCH CONTROL SIGNAL
68
$PFET_1$
70
$NFET_1$
72
58
V_{SW}
26
POWER INDUCTOR 16
V_{CC}
I_{SW_OUT}

FIG. 7B

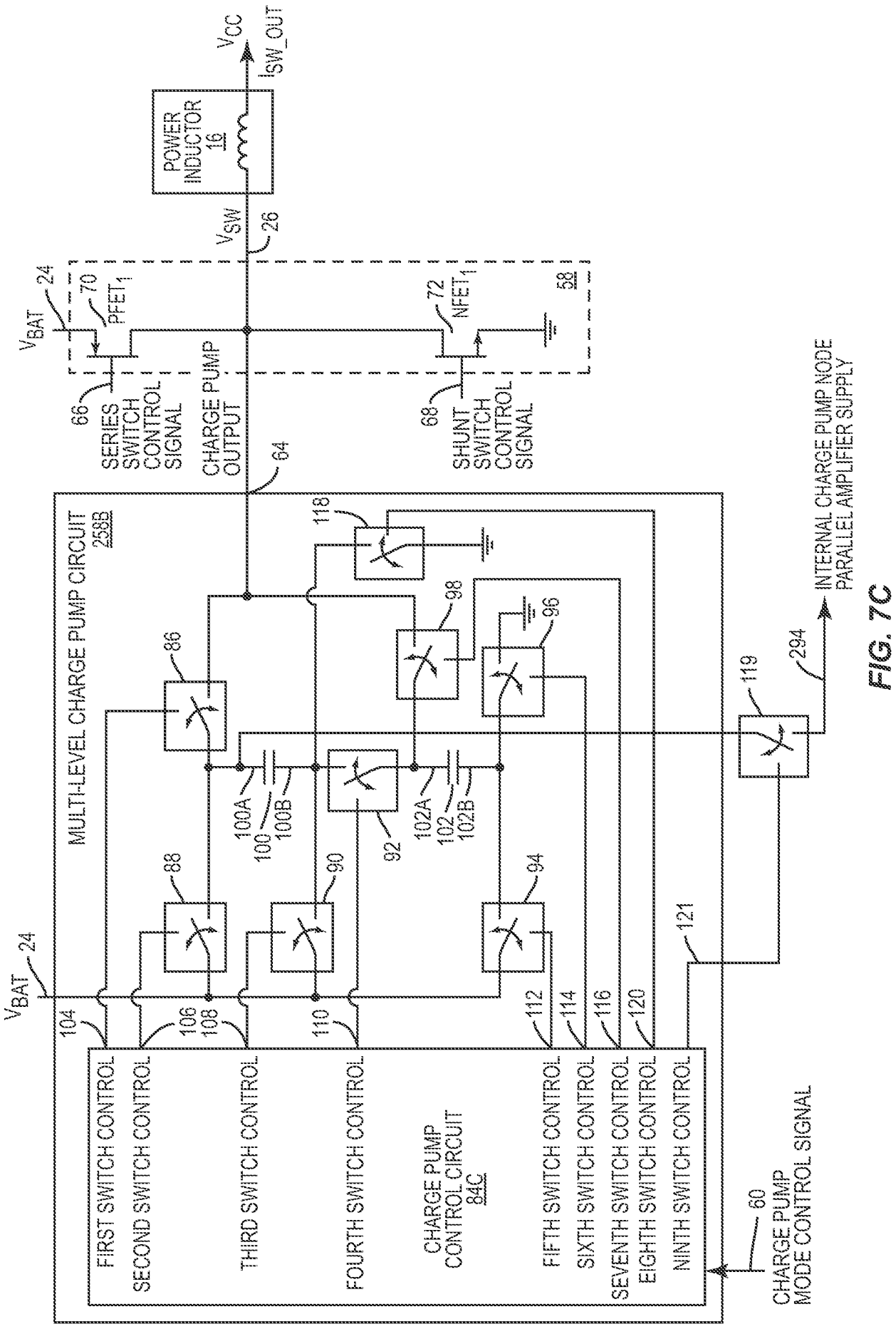

V_{CC}
I_{SW_OUT}
POWER INDUCTOR 16
V_{SW}
26
V_{BAT} 24
70 $PFET_1$
72 $NFET_1$
58
66 SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP OUTPUT
64
68 SHUNT SWITCH CONTROL SIGNAL
INTERNAL CHARGE PUMP NODE PARALLEL AMPLIFIER SUPPLY
294
MULTI-LEVEL CHARGE PUMP CIRCUIT 258B
86
88
90
92
94
96
98
100A
100
100B
102A
102
102B
118
119
121
104
106
108
110
112
114
116
120
FIRST SWITCH CONTROL
SECOND SWITCH CONTROL
THIRD SWITCH CONTROL
FOURTH SWITCH CONTROL
CHARGE PUMP CONTROL CIRCUIT 84C
FIFTH SWITCH CONTROL
SIXTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
NINTH SWITCH CONTROL
60
CHARGE PUMP MODE CONTROL SIGNAL

FIG. 7C

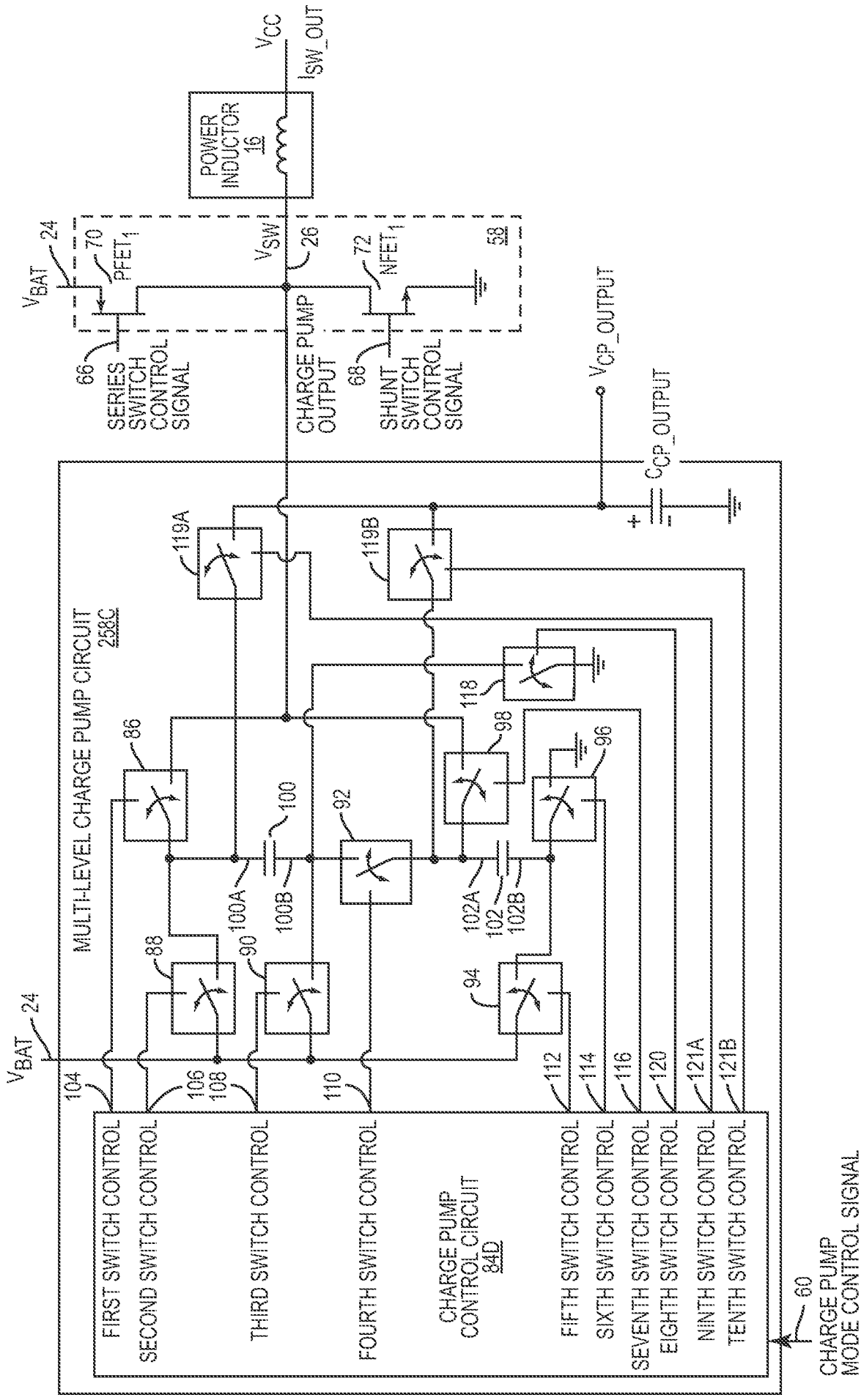

V_{CC}
I_{SW_OUT}
POWER INDUCTOR 16
V_{BAT} 24
70 $PFET_1$
V_{SW} 26
72 $NFET_1$
58
66 SERIES SWITCH CONTROL SIGNAL
CHARGE PUMP OUTPUT
68 SHUNT SWITCH CONTROL SIGNAL
V_{CP_OUTPUT}
C_{CP_OUTPUT}
MULTI-LEVEL CHARGE PUMP CIRCUIT 258C
119A
119B
118
86
98
96
100
92
88
90
94
100A
100B
102A
102
102B
V_{BAT} 24
104
106
108
110
112
114
116
120
121A
121B
FIRST SWITCH CONTROL
SECOND SWITCH CONTROL
THIRD SWITCH CONTROL
FOURTH SWITCH CONTROL
CHARGE PUMP CONTROL CIRCUIT 84D
FIFTH SWITCH CONTROL
SIXTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
NINTH SWITCH CONTROL
TENTH SWITCH CONTROL
60
CHARGE PUMP MODE CONTROL SIGNAL

FIG. 7D

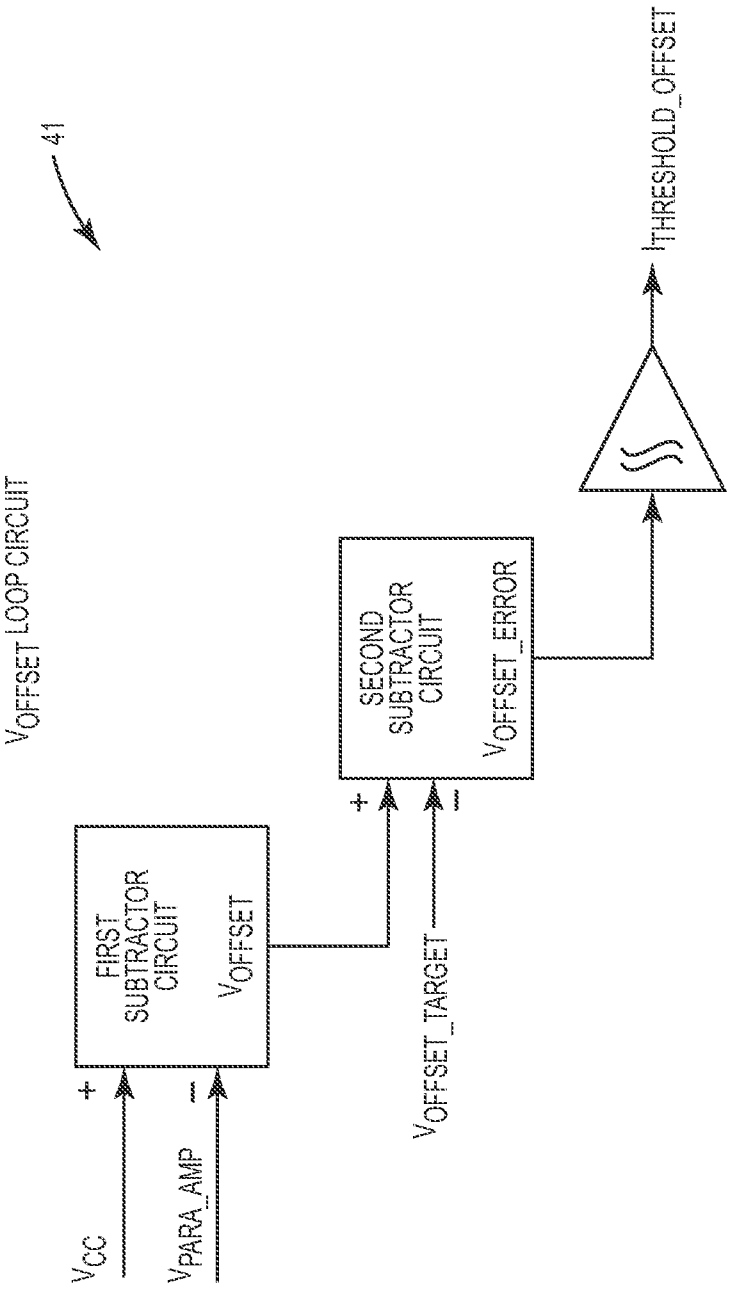

41
VOFFSET LOOP CIRCUIT
FIRST SUBTRACTOR CIRCUIT
VOFFSET
SECOND SUBTRACTOR CIRCUIT
VOFFSET_ERROR
ITHRESHOLD_OFFSET
VCC
VPARA_AMP
VOFFSET_TARGET
+
−
+
−

FIG. 8

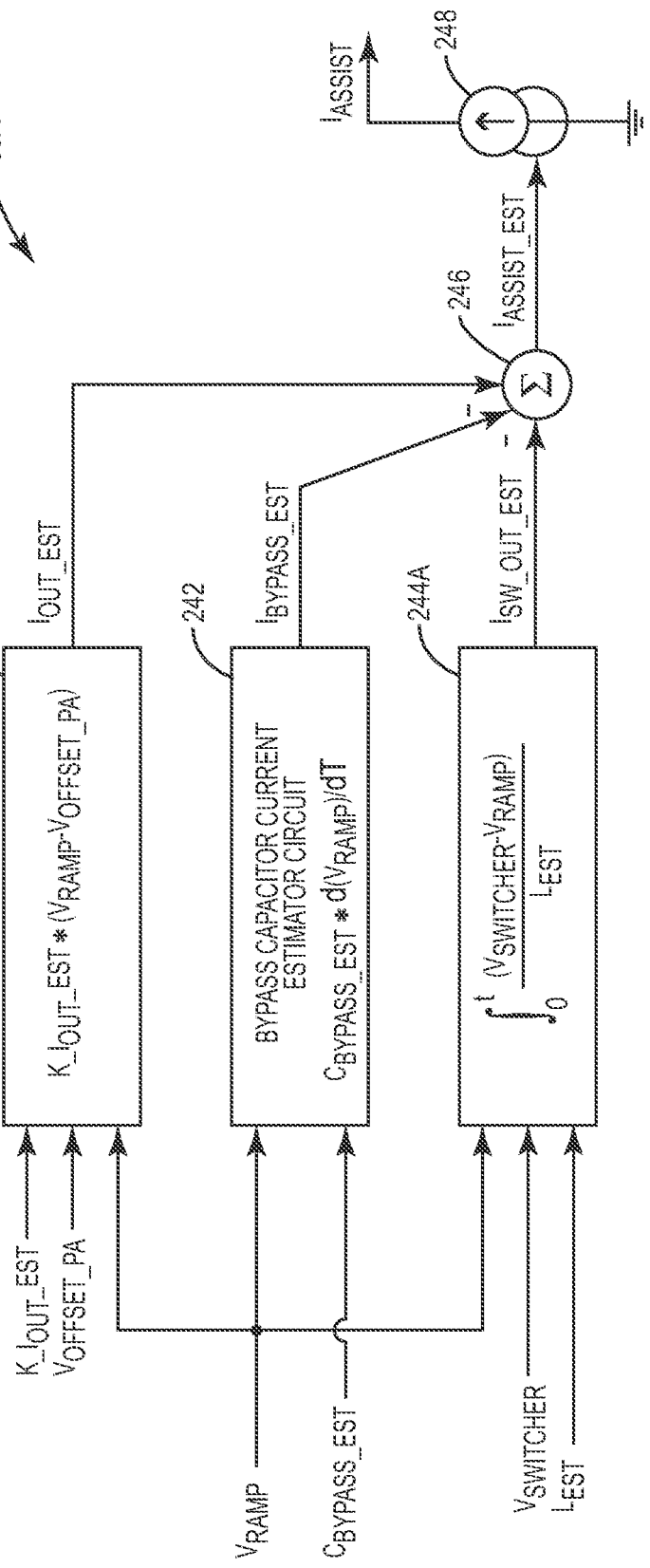

39A
240
242
244A
246
248
I_{OUT_EST}
I_{BYPASS_EST}
$I_{SW_OUT_EST}$
I_{ASSIST_EST}
I_{ASSIST}
$K_I_{OUT_EST} * (V_{RAMP}-V_{OFFSET_PA})$
BYPASS CAPACITOR CURRENT ESTIMATOR CIRCUIT
$C_{BYPASS_EST} * d(V_{RAMP})/dT$
$\int_0^t \frac{(V_{SWITCHER}-V_{RAMP})}{L_{EST}}$
OPEN LOOP ASSIST CIRCUIT
$K_I_{OUT_EST}$
V_{OFFSET_PA}
V_{RAMP}
C_{BYPASS_EST}
$V_{SWITCHER}$
L_{EST}

FIG. 9A

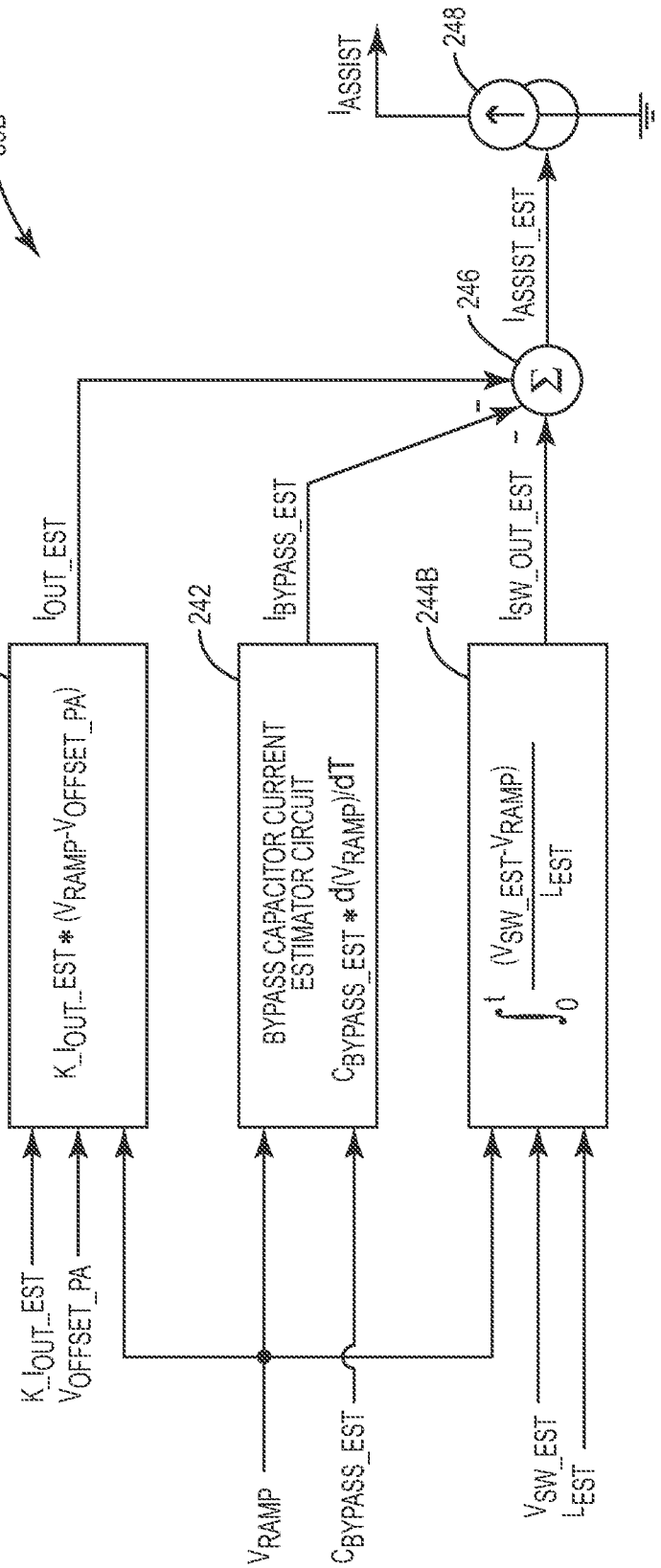

39B
240
242
244B
246
248
I_{OUT_EST}
I_{BYPASS_EST}
$I_{SW_OUT_EST}$
I_{ASSIST_EST}
I_{ASSIST}
$K_I_{OUT_EST} * (V_{RAMP}-V_{OFFSET_PA})$
BYPASS CAPACITOR CURRENT ESTIMATOR CIRCUIT
$C_{BYPASS_EST} * d(V_{RAMP})/dT$
$\int_0^t \frac{(V_{SW_EST}-V_{RAMP})}{L_{EST}}$
OPEN LOOP ASSIST CIRCUIT
$K_I_{OUT_EST}$
V_{OFFSET_PA}
V_{RAMP}
C_{BYPASS_EST}
V_{SW_EST}
L_{EST}

FIG. 9B

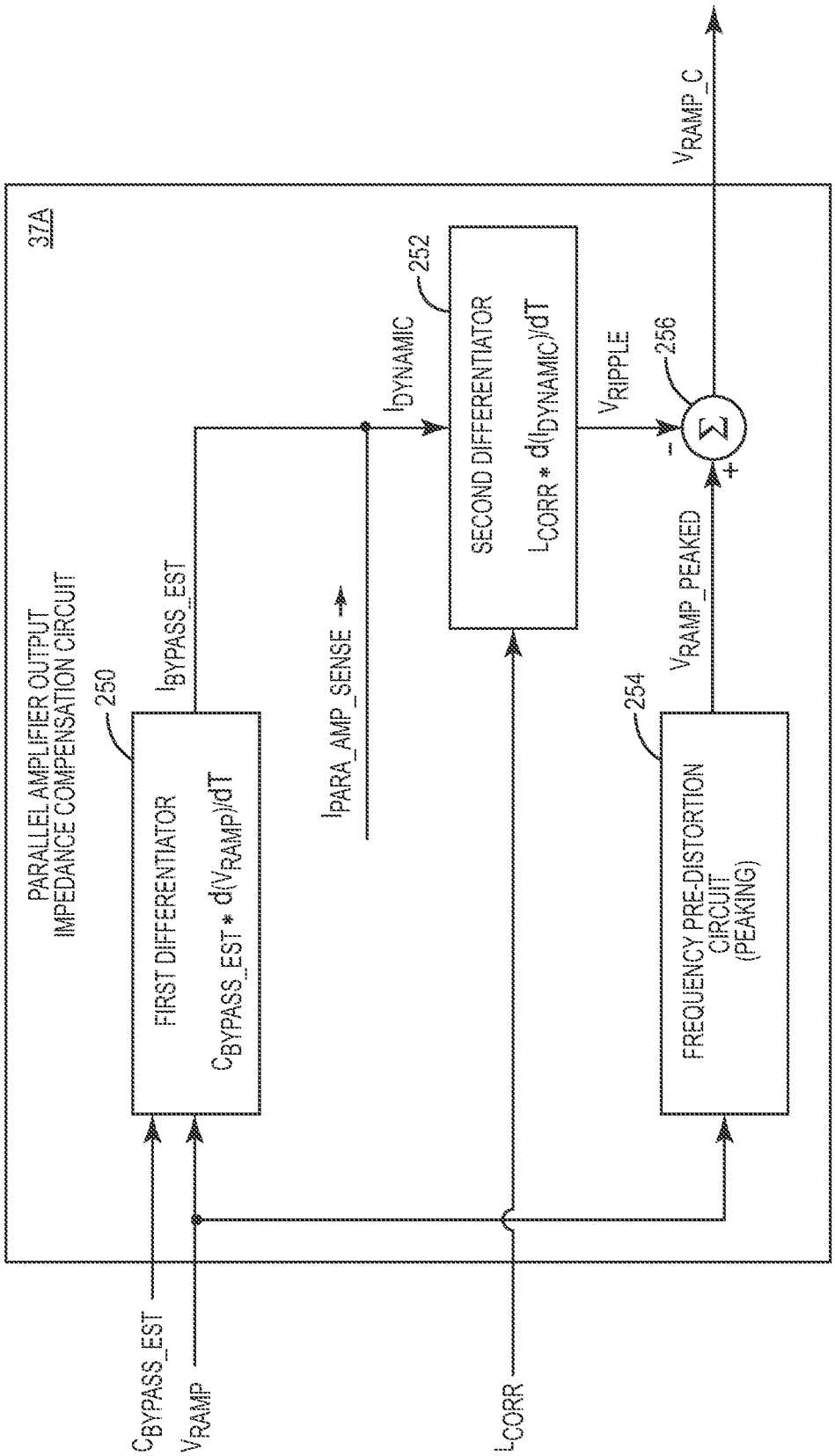

37A
PARALLEL AMPLIFIER OUTPUT IMPEDANCE COMPENSATION CIRCUIT
250
FIRST DIFFERENTIATOR
$C_{BYPASS_EST} * d(V_{RAMP})/dT$
I_{BYPASS_EST}
$I_{PARA_AMP_SENSE}$
$I_{DYNAMIC}$
252
SECOND DIFFERENTIATOR
$L_{CORR} * d(I_{DYNAMIC})/dT$
V_{RIPPLE}
256
V_{RAMP_PEAKED}
254
FREQUENCY PRE-DISTORTION CIRCUIT (PEAKING)
V_{RAMP_C}
C_{BYPASS_EST}
V_{RAMP}
L_{CORR}

FIG. 10

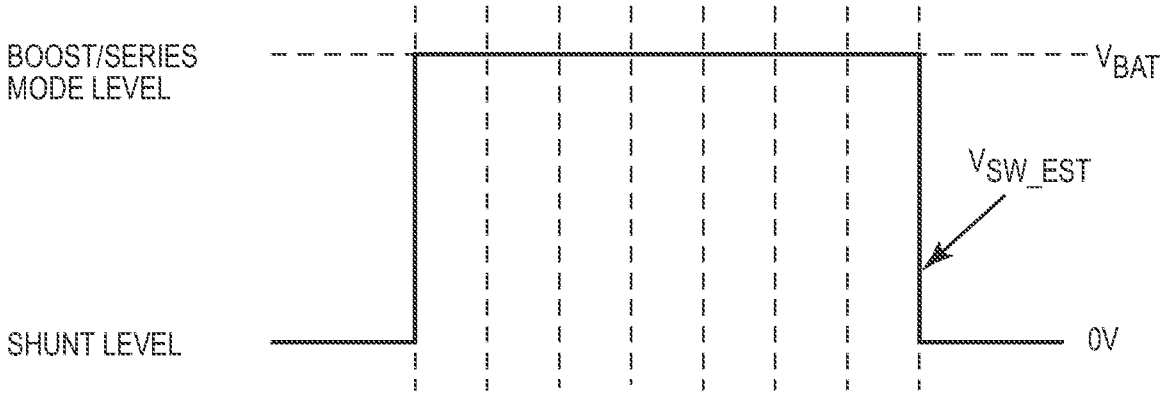


FIG. 11A

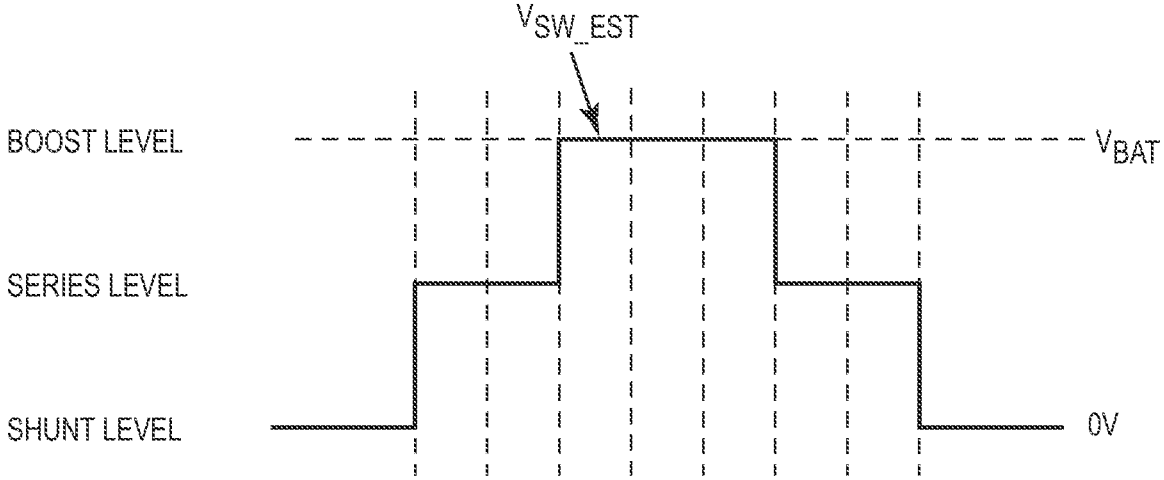


FIG. 11B

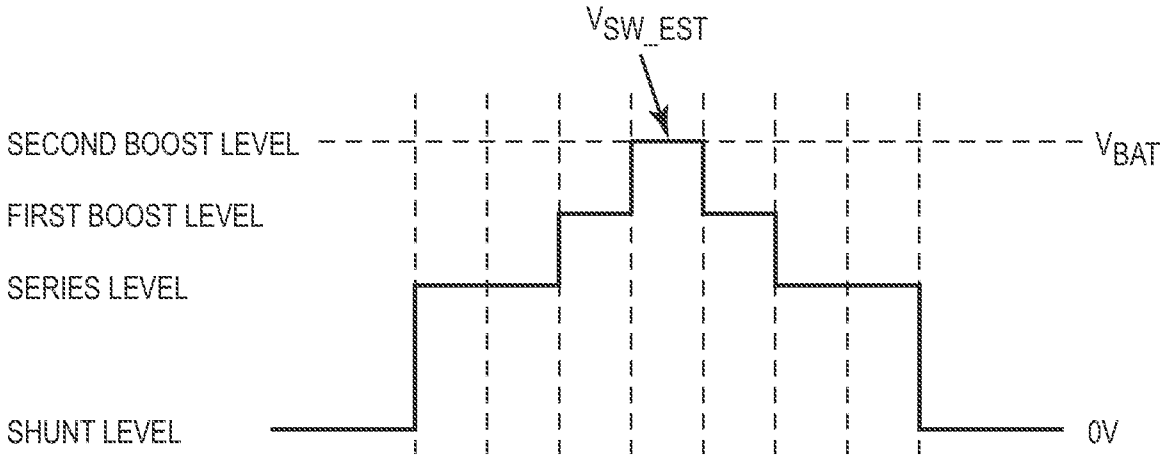


FIG. 11C

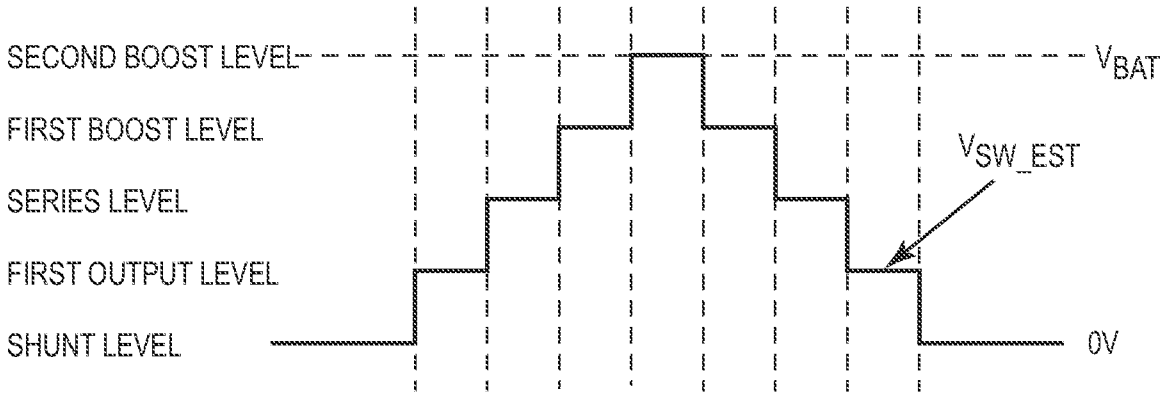


FIG. 11D

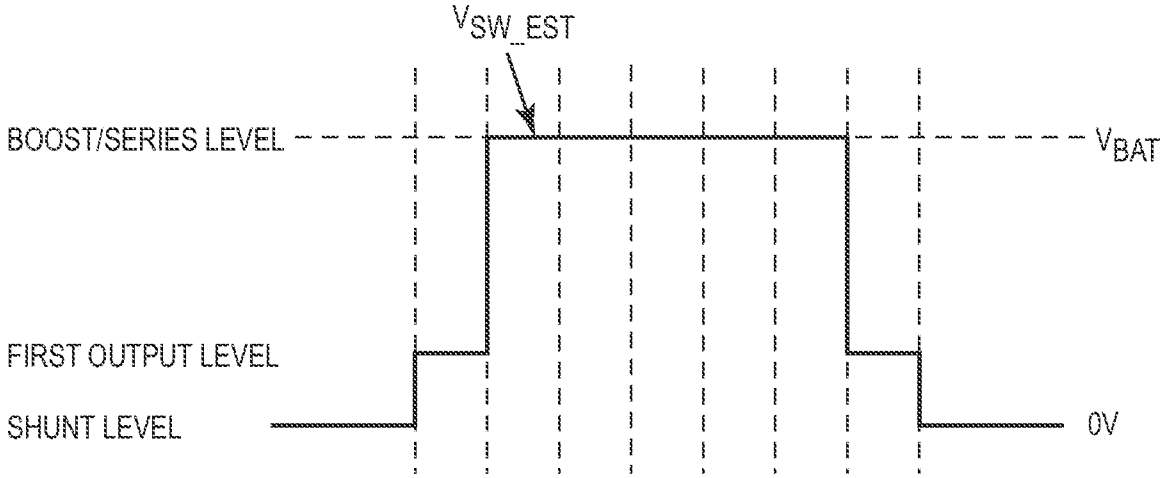


FIG. 11E

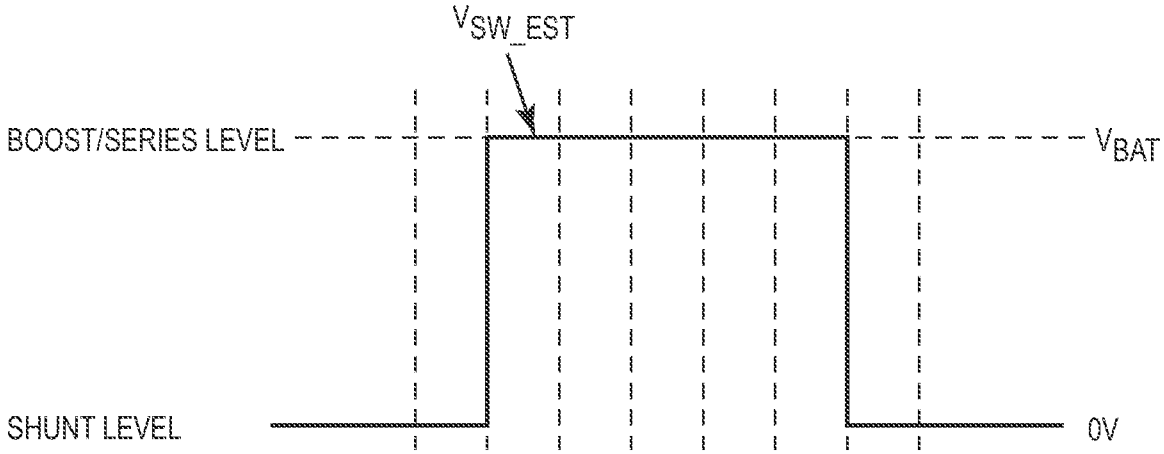


FIG. 11F

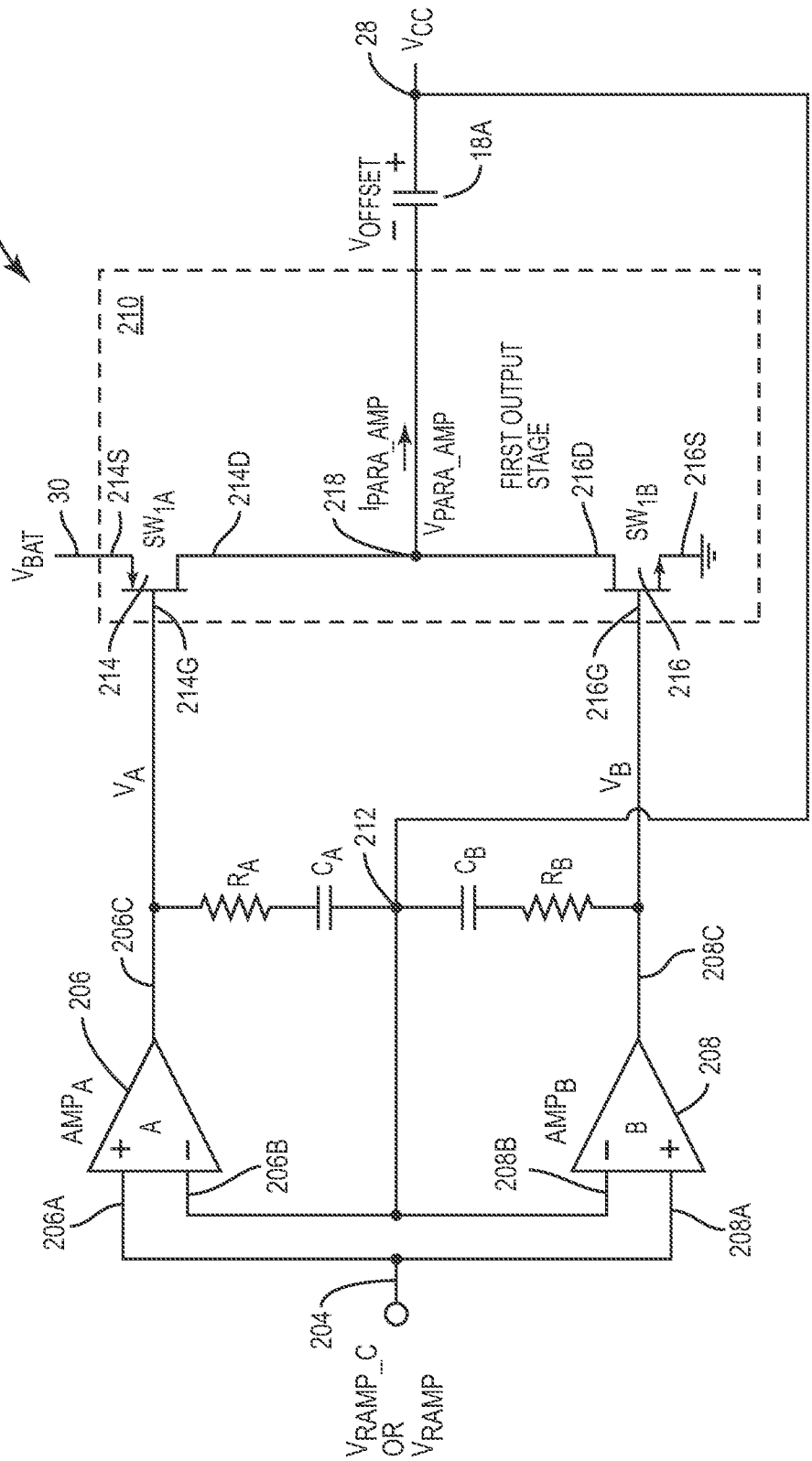

35A
28
V_{CC}
18A
V_{OFFSET}
210
FIRST OUTPUT STAGE
30
V_{BAT}
214S
SW_{1A}
214D
218
I_{PARA_AMP}
V_{PARA_AMP}
216D
SW_{1B}
216S
214
214G
216G
216
V_A
V_B
R_A
C_A
212
C_B
R_B
206C
208C
206
208
AMP_A
AMP_B
206B
208B
206A
208A
204
V_{RAMP_C}
OR
V_{RAMP}

FIG. 12A

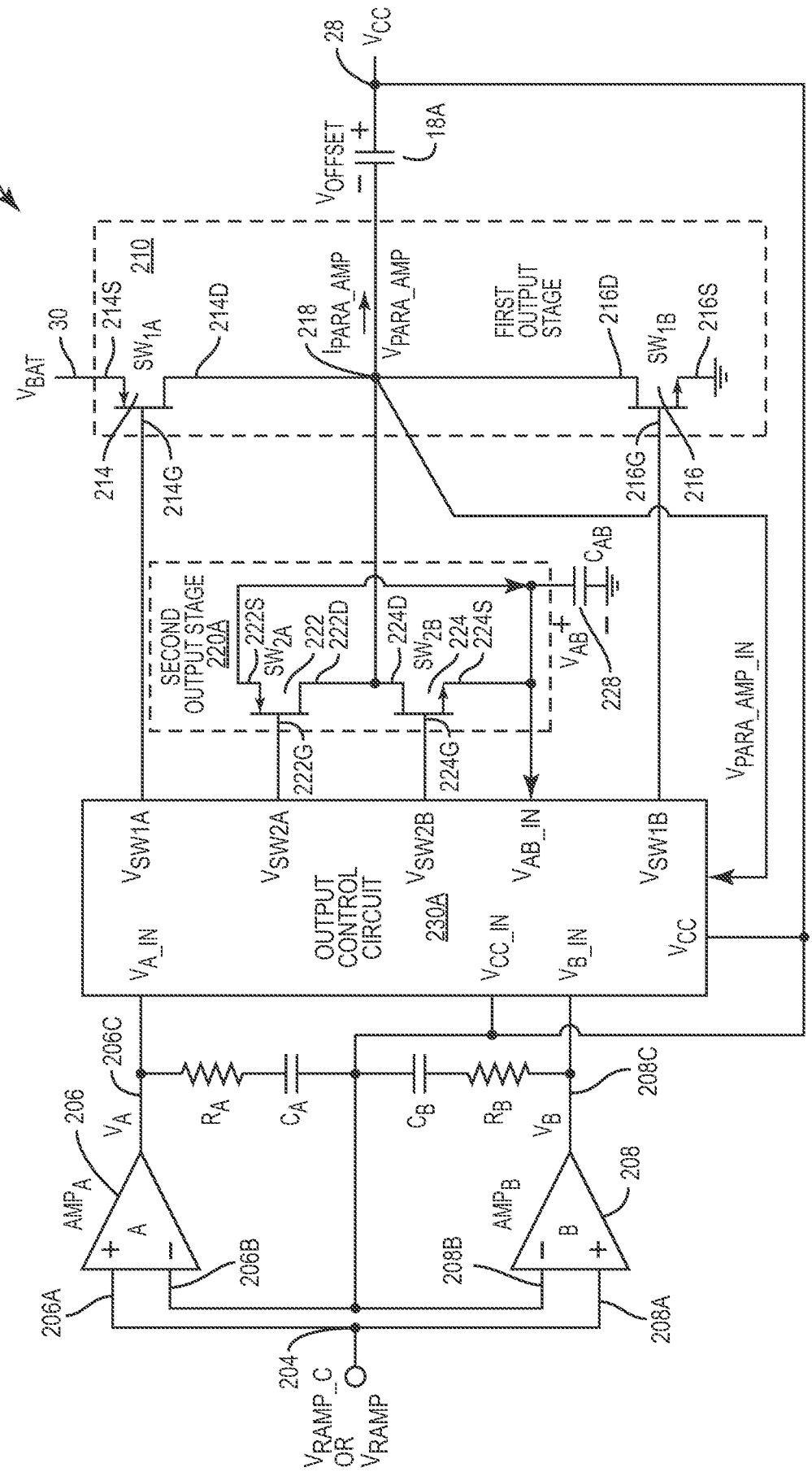

35B
28
V_{CC}
18A
V_{OFFSET}
210
214S
214D
214
214G
30
V_{BAT}
SW_{1A}
218
I_{PARA_AMP}
V_{PARA_AMP}
FIRST OUTPUT STAGE
216D
216S
216
216G
SW_{1B}
SECOND OUTPUT STAGE 220A
222S
222
222D
SW_{2A}
222G
224D
224
224S
SW_{2B}
224G
C_{AB}
V_{AB}
228
$V_{PARA_AMP_IN}$
OUTPUT CONTROL CIRCUIT 230A
V_{SW1A}
V_{SW2A}
V_{SW2B}
V_{AB_IN}
V_{SW1B}
V_{A_IN}
V_{CC_IN}
V_{B_IN}
V_{CC}
206C
206
V_A
R_A
C_A
C_B
R_B
V_B
208C
AMP_A
A
AMP_B
B
208
206B
208B
206A
208A
204
V_{RAMP_C}
OR
V_{RAMP}

FIG. 12B

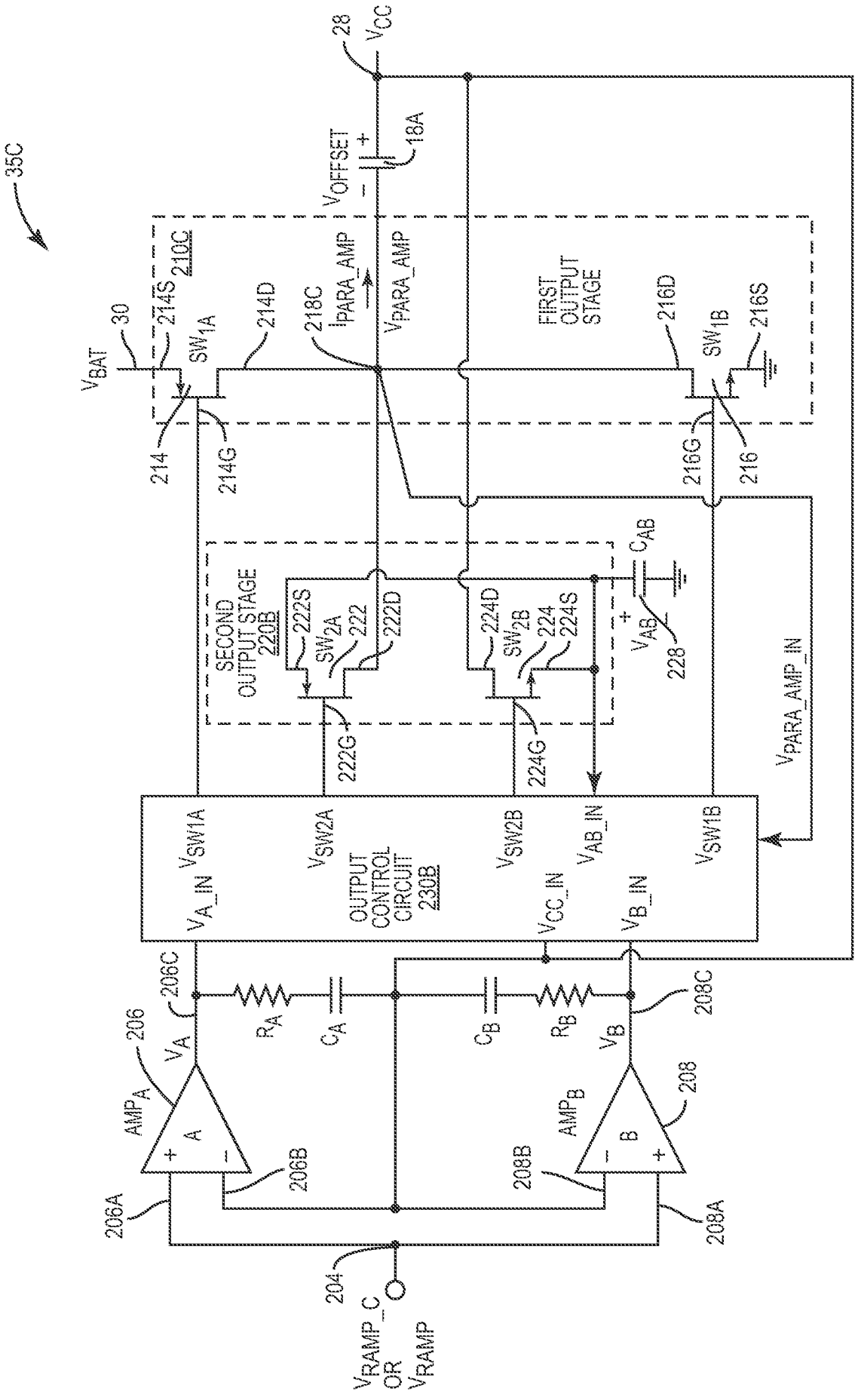

35C
28
V_{CC}
18A
V_{OFFSET}
210C
214S
30
V_{BAT}
SW_{1A}
214D
218C
I_{PARA_AMP}
V_{PARA_AMP}
FIRST OUTPUT STAGE
216D
SW_{1B}
216S
214
214G
216G
216
SECOND OUTPUT STAGE 220B
222S
SW_{2A}
222
222D
224D
SW_{2B}
224
224S
C_{AB}
V_{AB}
228
222G
224G
$V_{PARA_AMP_IN}$
V_{A_IN}
V_{SW1A}
V_{SW2A}
OUTPUT CONTROL CIRCUIT 230B
V_{SW2B}
V_{AB_IN}
V_{SW1B}
V_{CC_IN}
V_{B_IN}
206C
206
V_A
R_A
C_A
C_B
R_B
V_B
208C
AMP_A
A
208
AMP_B
B
206B
208B
206A
208A
204
V_{RAMP_C}
OR
V_{RAMP}

FIG. 12C

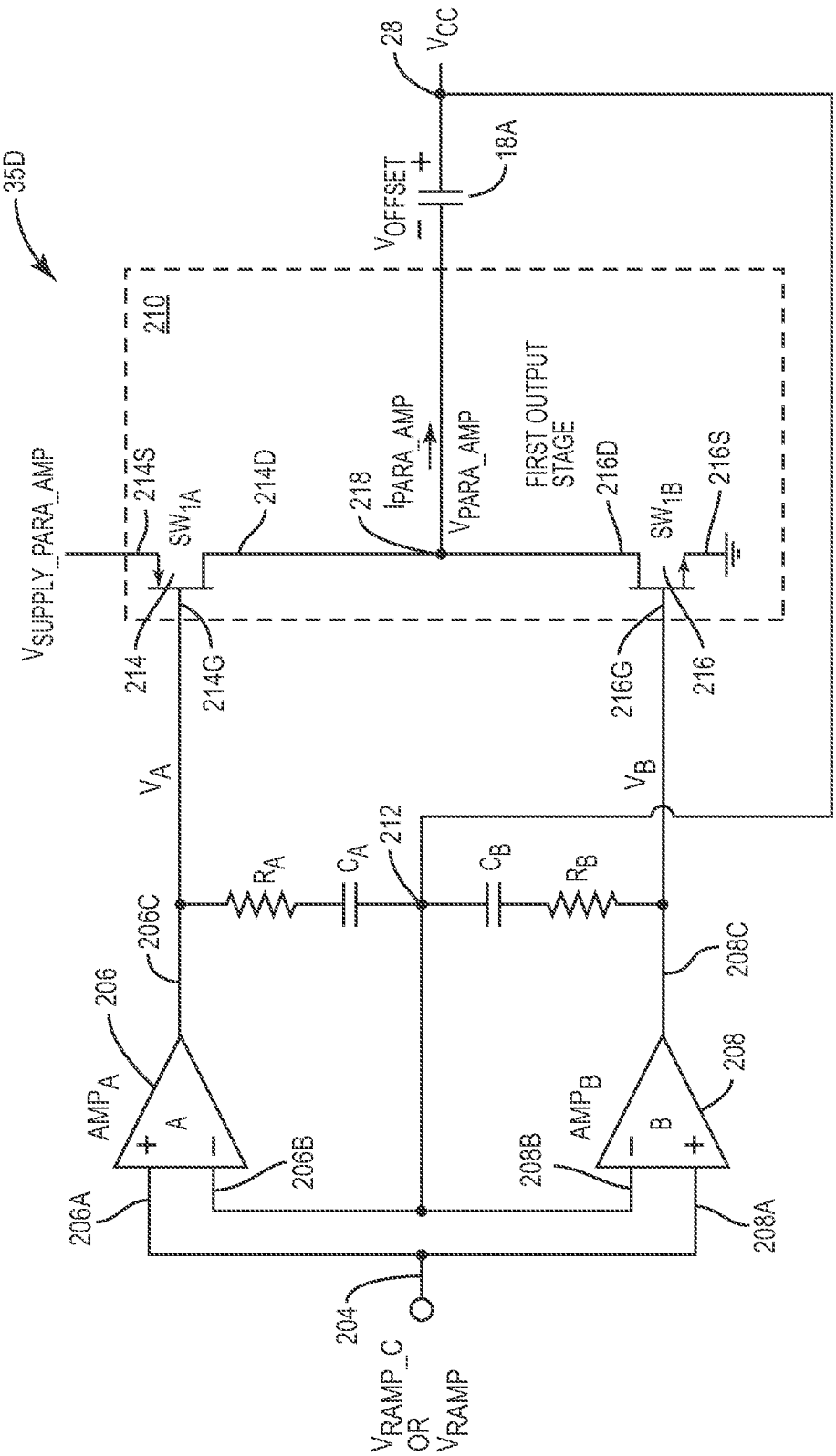

35D
28
V_{CC}
18A
V_{OFFSET}
210
$V_{SUPPLY_PARA_AMP}$
214S
SW_{1A}
214D
218
I_{PARA_AMP}
V_{PARA_AMP}
FIRST OUTPUT STAGE
216D
SW_{1B}
216S
214
214G
216G
216
V_A
V_B
212
R_A
C_A
C_B
R_B
206C
208C
206
208
AMP_A
AMP_B
206B
208B
206A
208A
204
V_{RAMP_C}
OR
V_{RAMP}

FIG. 12D

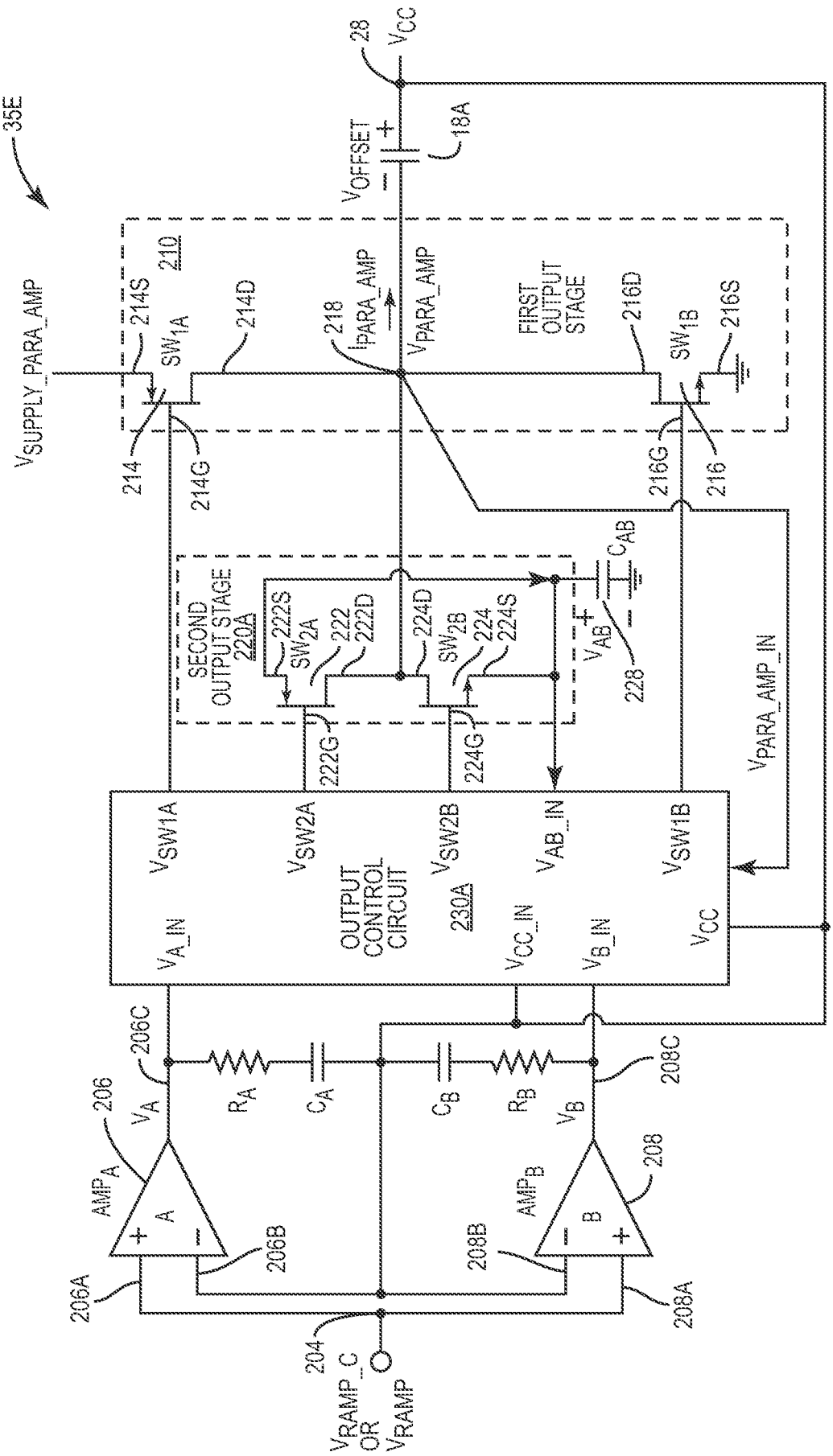

35E
28
V_{CC}
18A
V_{OFFSET}
$V_{SUPPLY_PARA_AMP}$
210
214S
SW_{1A}
214D
218
I_{PARA_AMP}
V_{PARA_AMP}
FIRST OUTPUT STAGE
216D
SW_{1B}
216S
214
214G
216G
216
SECOND OUTPUT STAGE 220A
222S
SW_{2A}
222
222D
224D
SW_{2B}
224
224S
C_{AB}
V_{AB}
228
222G
224G
$V_{PARA_AMP_IN}$
V_{SW1A}
V_{SW2A}
V_{SW2B}
V_{AB_IN}
V_{SW1B}
V_{A_IN}
OUTPUT CONTROL CIRCUIT
230A
V_{CC_IN}
V_{B_IN}
V_{CC}
206C
206
V_A
R_A
C_A
C_B
R_B
V_B
208C
AMP_A
A
AMP_B
B
208
206B
208B
206A
208A
204
V_{RAMP_C}
OR
V_{RAMP}

FIG. 12E

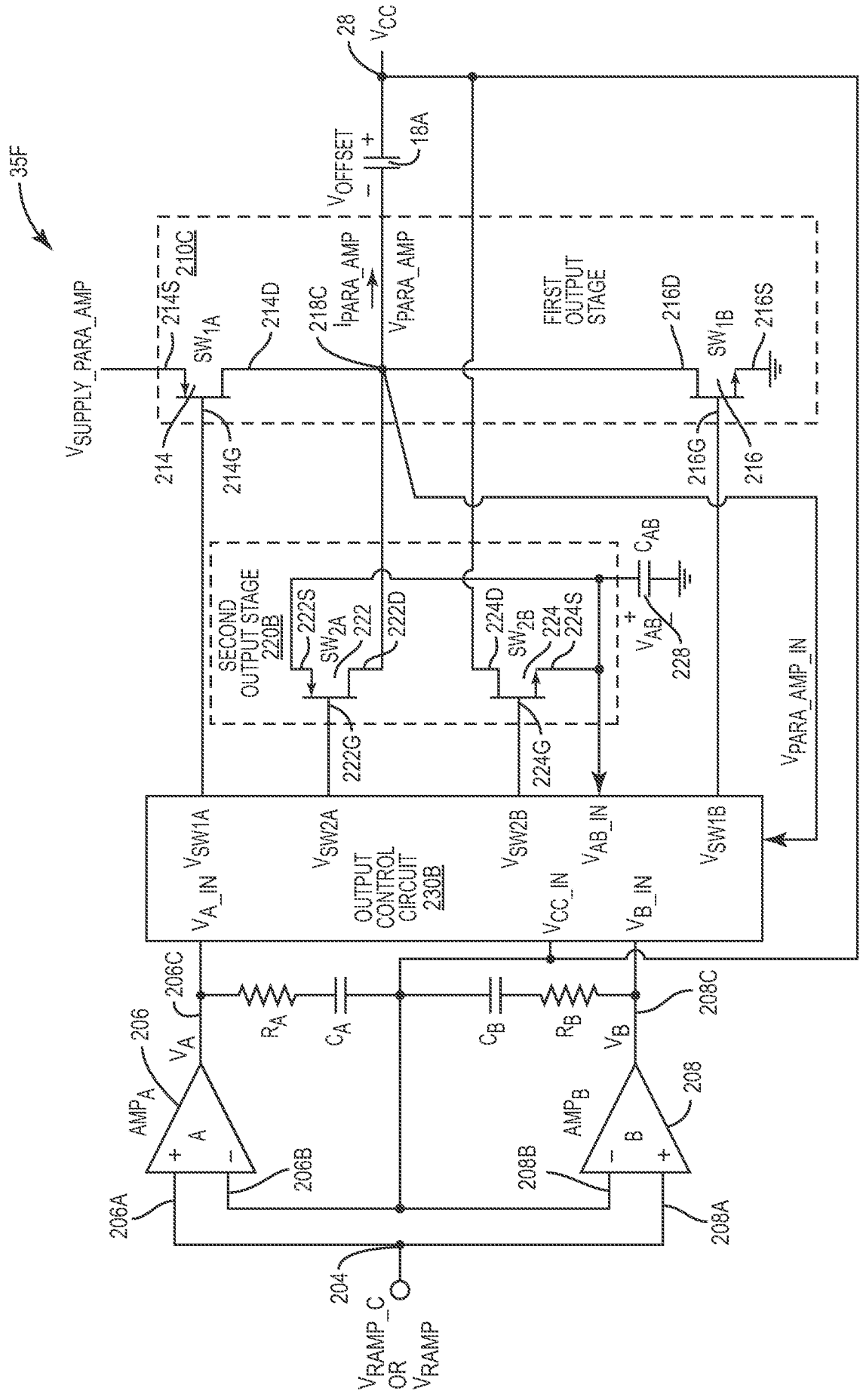

35F
VSUPPLY_PARA_AMP
214
214S
210C
SW1A
214G
214D
218C
IPARA_AMP
VPARA_AMP
VOFFSET
18A
28
VCC
FIRST OUTPUT STAGE
216D
SW1B
216S
216G
216
SECOND OUTPUT STAGE 220B
222S
SW2A
222
222D
222G
224D
SW2B
224
224S
224G
CAB
VAB
228
VPARA_AMP_IN
VA_IN
VSW1A
VSW2A
OUTPUT CONTROL CIRCUIT 230B
VSW2B
VCC_IN
VAB_IN
VB_IN
VSW1B
206C
206
VA
AMPA
A
206B
206A
RA
CA
CB
RB
VB
208C
208
AMPB
B
208B
208A
204
VRAMP_C OR VRAMP

FIG. 12F

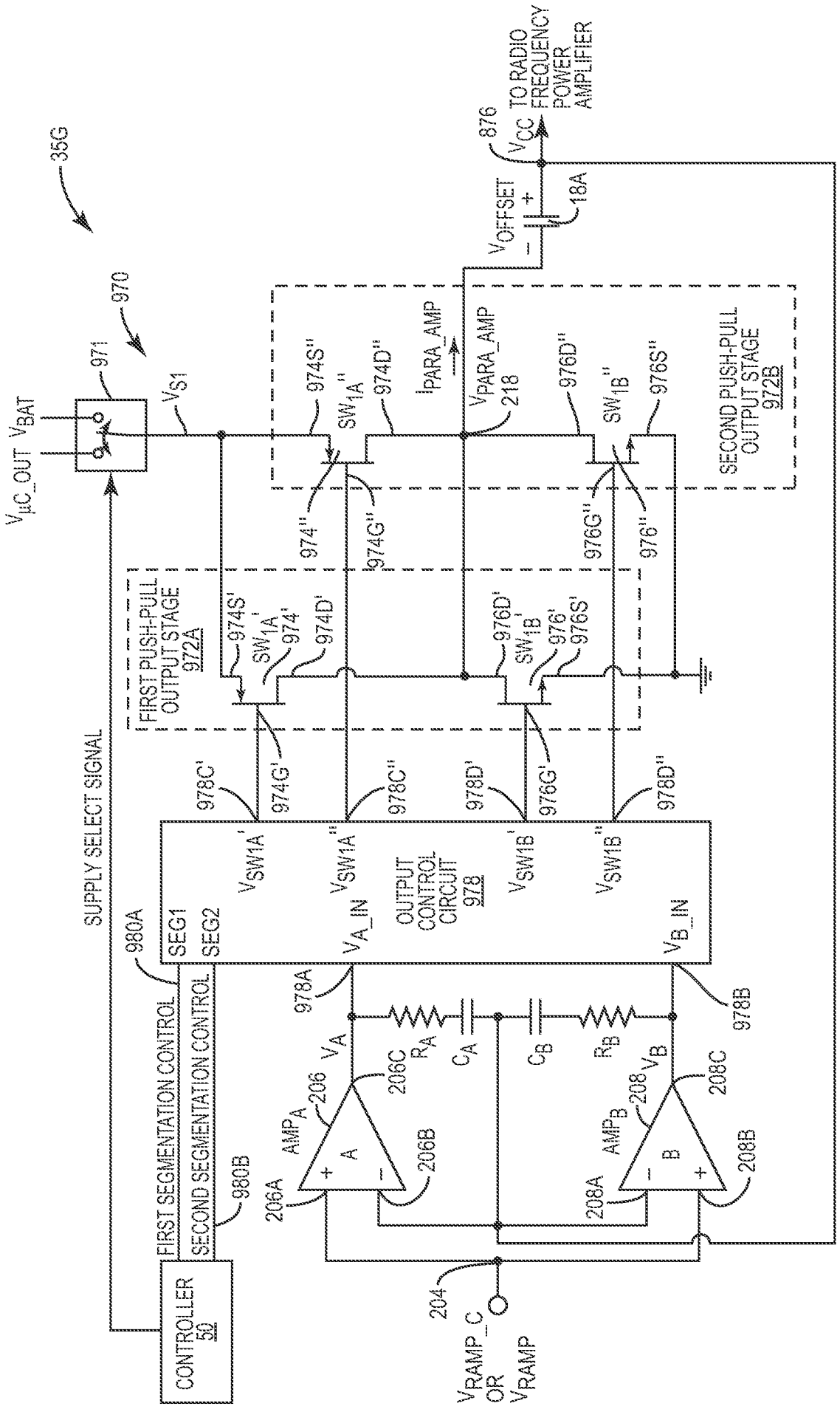

35G
970
971
$V_{\mu C_OUT}$
V_{BAT}
V_{S1}
876
V_{CC} TO RADIO FREQUENCY POWER AMPLIFIER
18A
V_{OFFSET}
I_{PARA_AMP}
V_{PARA_AMP}
218
974S''
SW_{1A}''
974D''
974''
974G''
976D''
SW_{1B}''
976S''
976G''
976''
SECOND PUSH-PULL OUTPUT STAGE 972B
FIRST PUSH-PULL OUTPUT STAGE 972A
974S'
SW_{1A}'
974'
974D'
976D'
SW_{1B}'
976'
976S'
SUPPLY SELECT SIGNAL
978C'
974G'
978C''
978D'
976G'
978D''
980A
SEG1
SEG2
V_{SW1A}'
V_{SW1A}''
V_{A_IN}
OUTPUT CONTROL CIRCUIT 978
V_{SW1B}'
V_{SW1B}''
V_{B_IN}
978A
978B
FIRST SEGMENTATION CONTROL
SECOND SEGMENTATION CONTROL
980B
V_A
R_A
C_A
C_B
R_B
V_B
206
206C
AMP_A
A
206B
206A
208
208C
AMP_B
B
208B
208A
CONTROLLER 50
204
V_{RAMP_C} OR V_{RAMP}

FIG. 12G

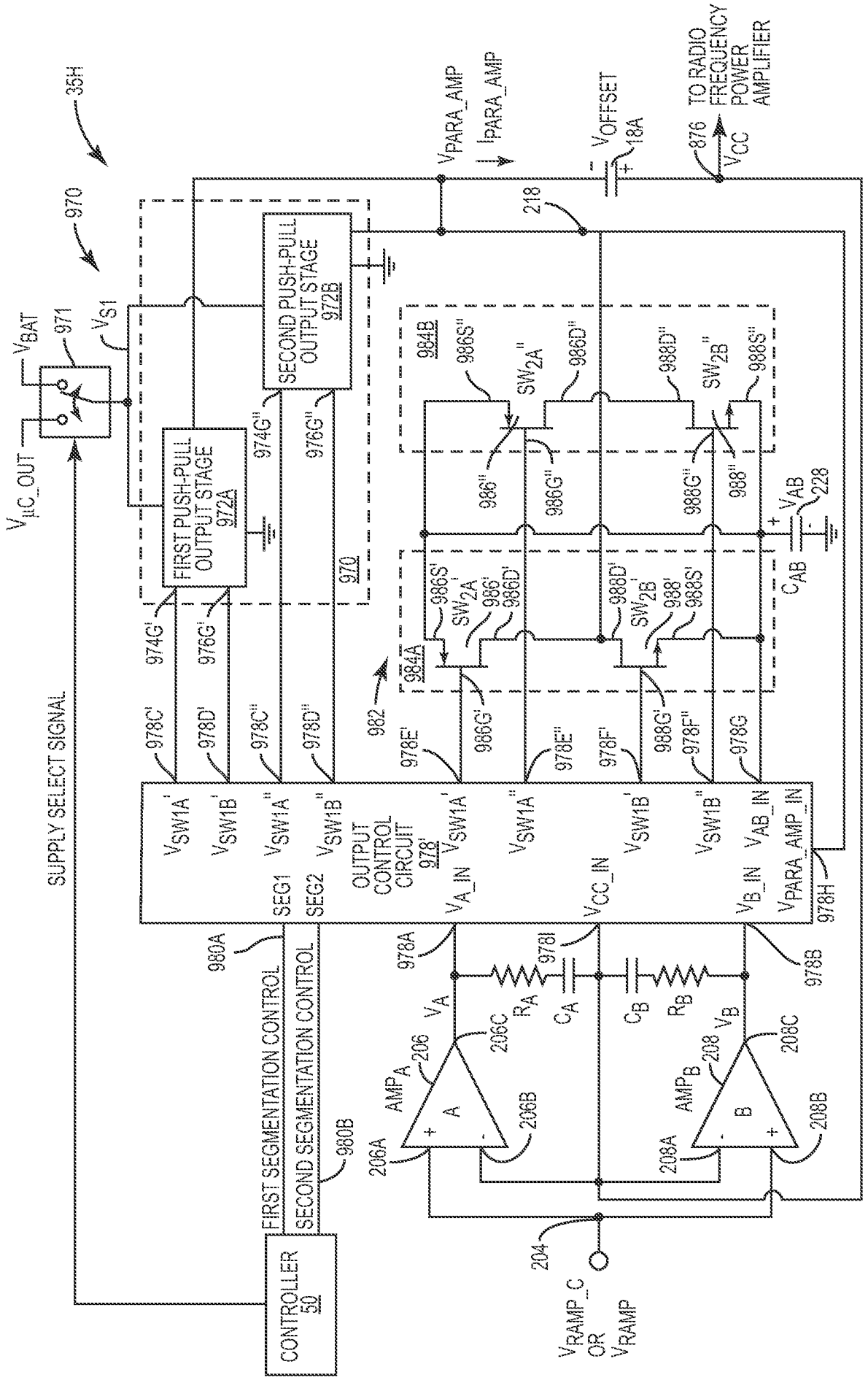

35H
970
971
V_{BAT}
V_{S1}
$V_{\mu C_OUT}$
SUPPLY SELECT SIGNAL
FIRST PUSH-PULL OUTPUT STAGE 972A
SECOND PUSH-PULL OUTPUT STAGE 972B
V_{PARA_AMP}
I_{PARA_AMP}
V_{OFFSET}
18A
876
TO RADIO FREQUENCY POWER AMPLIFIER
V_{CC}
218
984B
984A
982
970
974G'
976G'
974G''
976G''
978C'
978D'
978C''
978D''
978E'
978E''
978F'
978F''
978G
978G'
986S'
SW_{2A}'
986'
986D'
986G'
986S''
SW_{2A}''
986''
986D''
986G''
988S'
SW_{2B}'
988'
988D'
988G'
988S''
SW_{2B}''
988''
988D''
988G''
228
V_{AB}
C_{AB}
OUTPUT CONTROL CIRCUIT 978'
V_{SW1A}'
V_{SW1B}'
V_{SW1A}''
V_{SW1B}''
SEG1
SEG2
V_{A_IN}
V_{CC_IN}
V_{B_IN}
V_{AB_IN}
$V_{PARA_AMP_IN}$
978H
980A
980B
FIRST SEGMENTATION CONTROL
SECOND SEGMENTATION CONTROL
CONTROLLER 50
978A
978I
978B
V_A
R_A
C_A
C_B
R_B
V_B
AMP_A
AMP_B
206
206A
206B
206C
208
208A
208B
208C
204
V_{RAMP_C} OR V_{RAMP}

FIG. 12H

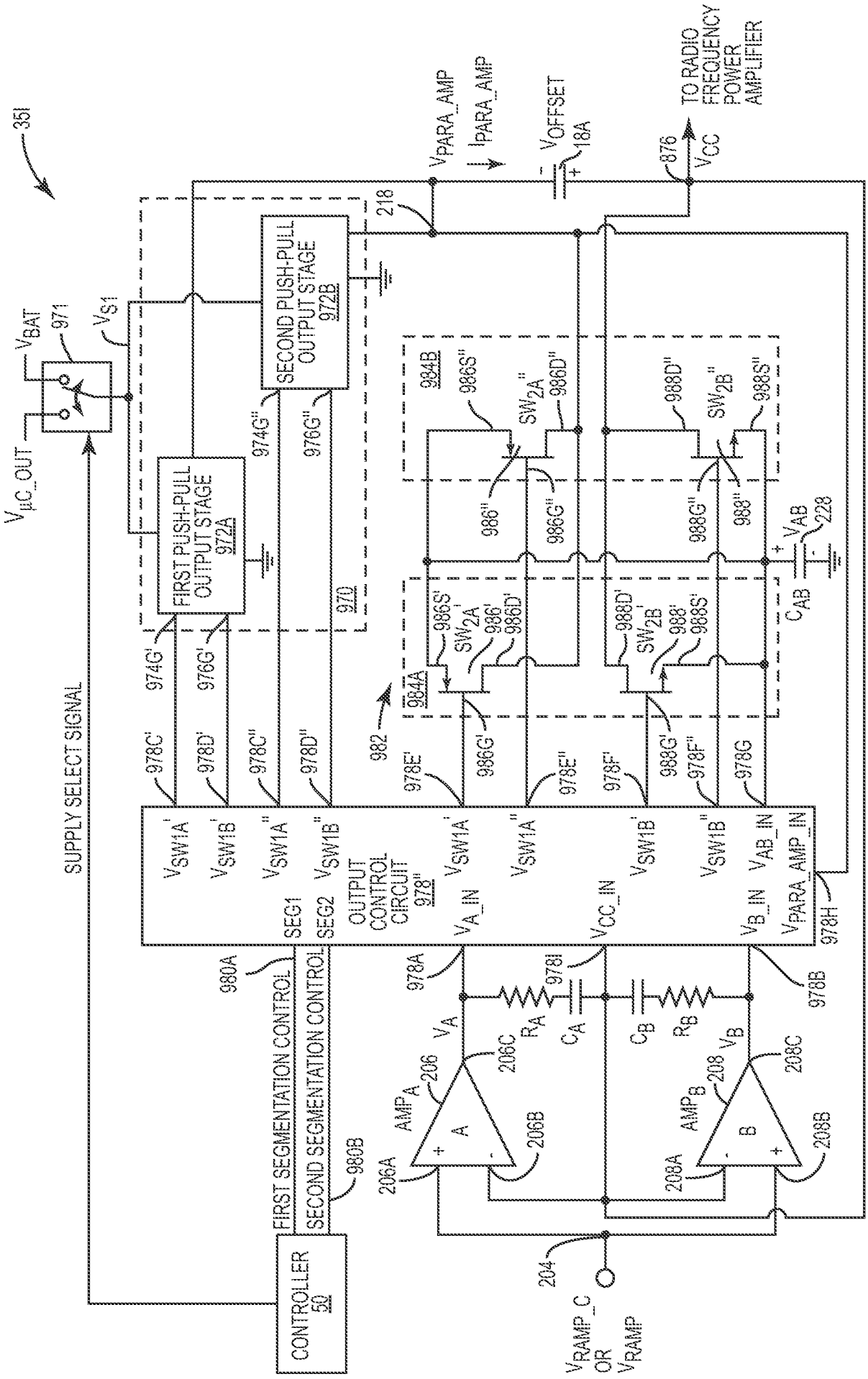

351
$V_{\mu C_OUT}$
V_{BAT}
971
V_{S1}
SUPPLY SELECT SIGNAL
FIRST PUSH-PULL OUTPUT STAGE 972A
SECOND PUSH-PULL OUTPUT STAGE 972B
970
974G'
976G'
974G"
976G"
218
V_{PARA_AMP}
I_{PARA_AMP}
V_{OFFSET}
18A
876
V_{CC}
TO RADIO FREQUENCY POWER AMPLIFIER
984B
986S"
SW_{2A}"
986D"
986"
986G"
988D"
SW_{2B}"
988S"
988"
988G"
V_{AB}
228
C_{AB}
986S'
SW_{2A}'
986'
986D'
988D'
SW_{2B}'
988'
988S'
982
984A
978C'
978D'
978C"
978D"
978E'
986G'
978E"
978F'
988G'
978F"
978G
OUTPUT CONTROL CIRCUIT 978"
V_{SW1A}'
V_{SW1B}'
V_{SW1A}"
V_{SW1B}"
SEG1
SEG2
V_{A_IN}
V_{CC_IN}
V_{B_IN}
V_{AB_IN}
$V_{PARA_AMP_IN}$
978H
980A
980B
FIRST SEGMENTATION CONTROL
SECOND SEGMENTATION CONTROL
CONTROLLER 50
978A
978I
978B
V_A
R_A
C_A
C_B
R_B
V_B
206
206C
206B
AMP_A
A
206A
208
208C
208B
AMP_B
B
208A
204
V_{RAMP_C} OR V_{RAMP}

FIG. 12I

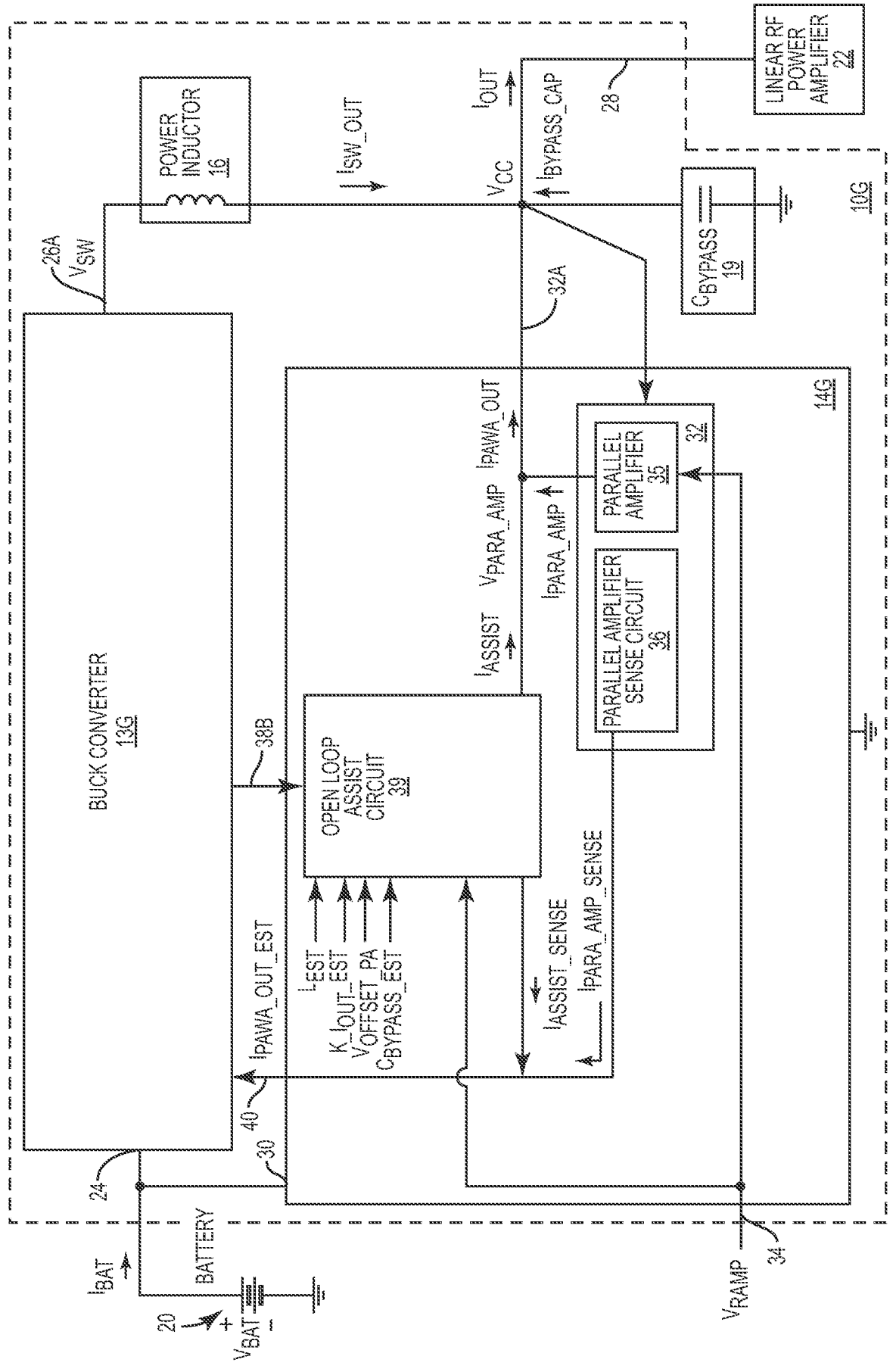

BUCK CONVERTER
13G
26A
VSW
POWER INDUCTOR
16
ISW_OUT
IOUT
VCC
IBYPASS_CAP
28
LINEAR RF POWER AMPLIFIER
22
CBYPASS
19
10G
32A
14G
IPAWA_OUT
VPARA_AMP
IPARA_AMP
PARALLEL AMPLIFIER
35
32
PARALLEL AMPLIFIER SENSE CIRCUIT
36
IASSIST
38B
OPEN LOOP ASSIST CIRCUIT
39
IEST
K_IOUT_EST
VOFFSET_PA
CBYPASS_EST
IPAWA_OUT_EST
IASSIST_SENSE
IPARA_AMP_SENSE
40
30
24
IBAT
BATTERY
20
VBAT
VRAMP
34

FIG. 13

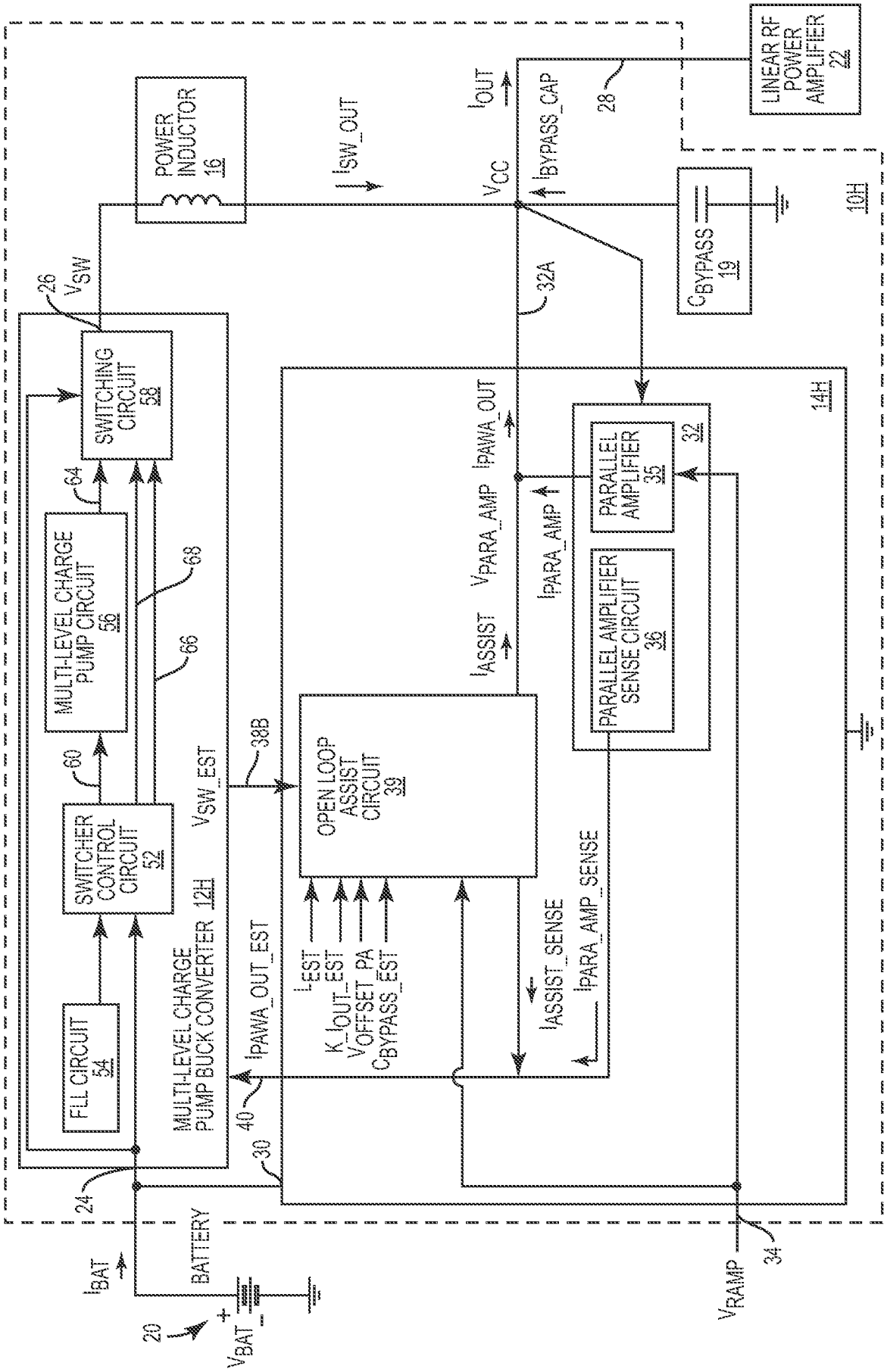

LINEAR RF POWER AMPLIFIER 22
POWER INDUCTOR 16
ISW_OUT
IOUT
VCC
IBYPASS_CAP
28
CBYPASS 19
10H
32A
26 VSW
SWITCHING CIRCUIT 58
64
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
68
66
60
SWITCHER CONTROL CIRCUIT 52
FLL CIRCUIT 54
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12H
VSW_EST
38B
OPEN LOOP ASSIST CIRCUIT 39
IPAWA_OUT_EST
40
30
24
IBAT
BATTERY
20
VBAT
IEST
K_IOUT_EST
VOFFSET_PA
CBYPASS_EST
IASSIST_SENSE
IPARA_AMP_SENSE
IASSIST
VPARA_AMP
IPAWA_OUT
IPARA_AMP
PARALLEL AMPLIFIER 35
32
PARALLEL AMPLIFIER SENSE CIRCUIT 36
14H
VRAMP
34

FIG. 14

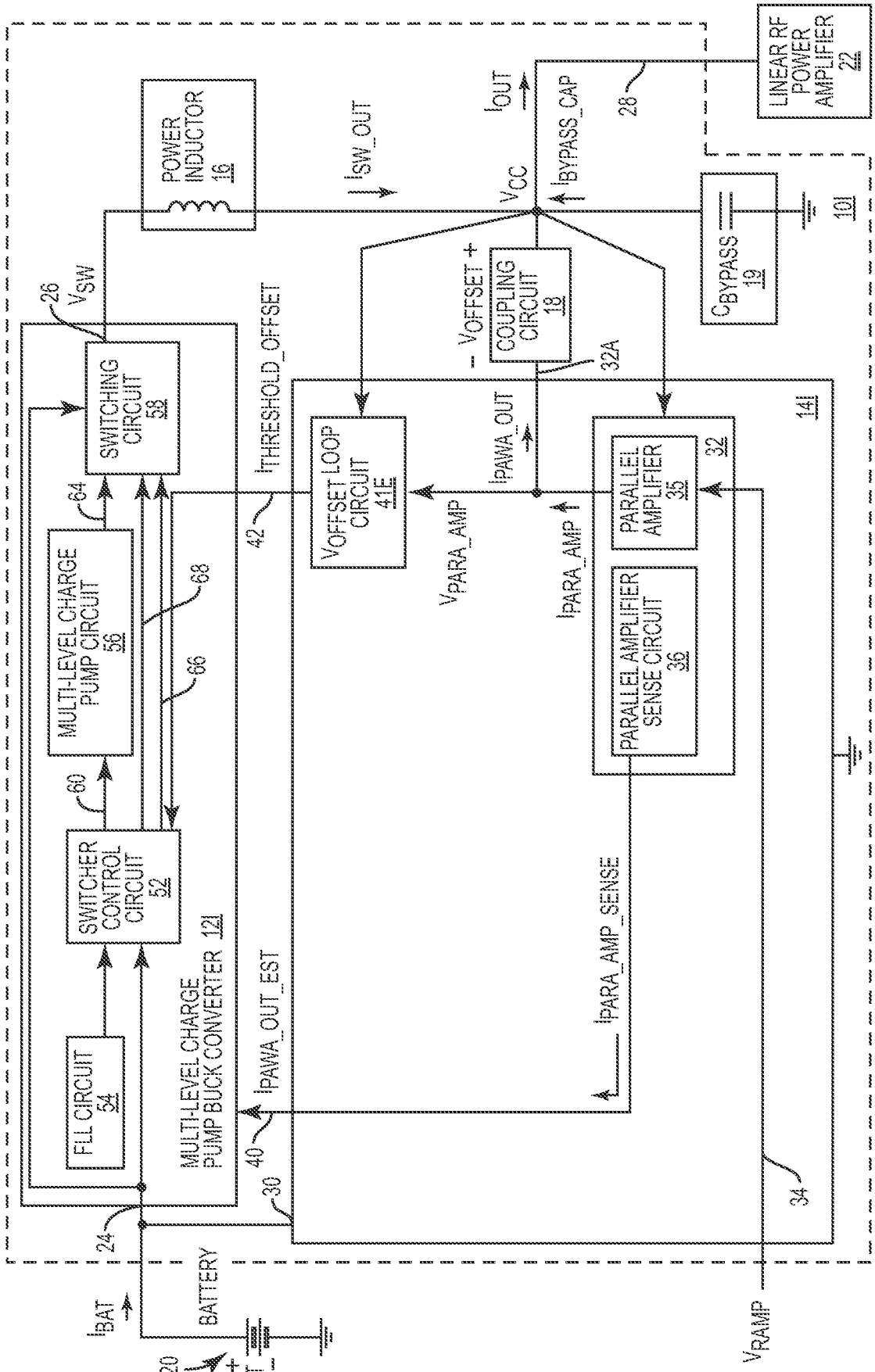

LINEAR RF POWER AMPLIFIER 22
POWER INDUCTOR 16
ISW_OUT
IOUT
VCC
IBYPASS_CAP
28
CBYPASS 19
101
26
VSW
SWITCHING CIRCUIT 58
64
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
68
66
60
SWITCHER CONTROL CIRCUIT 52
FLL CIRCUIT 54
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 121
24
BATTERY
IBAT
20
VBAT
IPAWA_OUT_EST
40
30
ITHRESHOLD_OFFSET
42
VOFFSET LOOP CIRCUIT 41E
VPARA_AMP
IPAWA_OUT
- VOFFSET +
COUPLING CIRCUIT 18
32A
IPARA_AMP
PARALLEL AMPLIFIER 35
32
PARALLEL AMPLIFIER SENSE CIRCUIT 36
IPARA_AMP_SENSE
141
34
VRAMP

FIG. 15

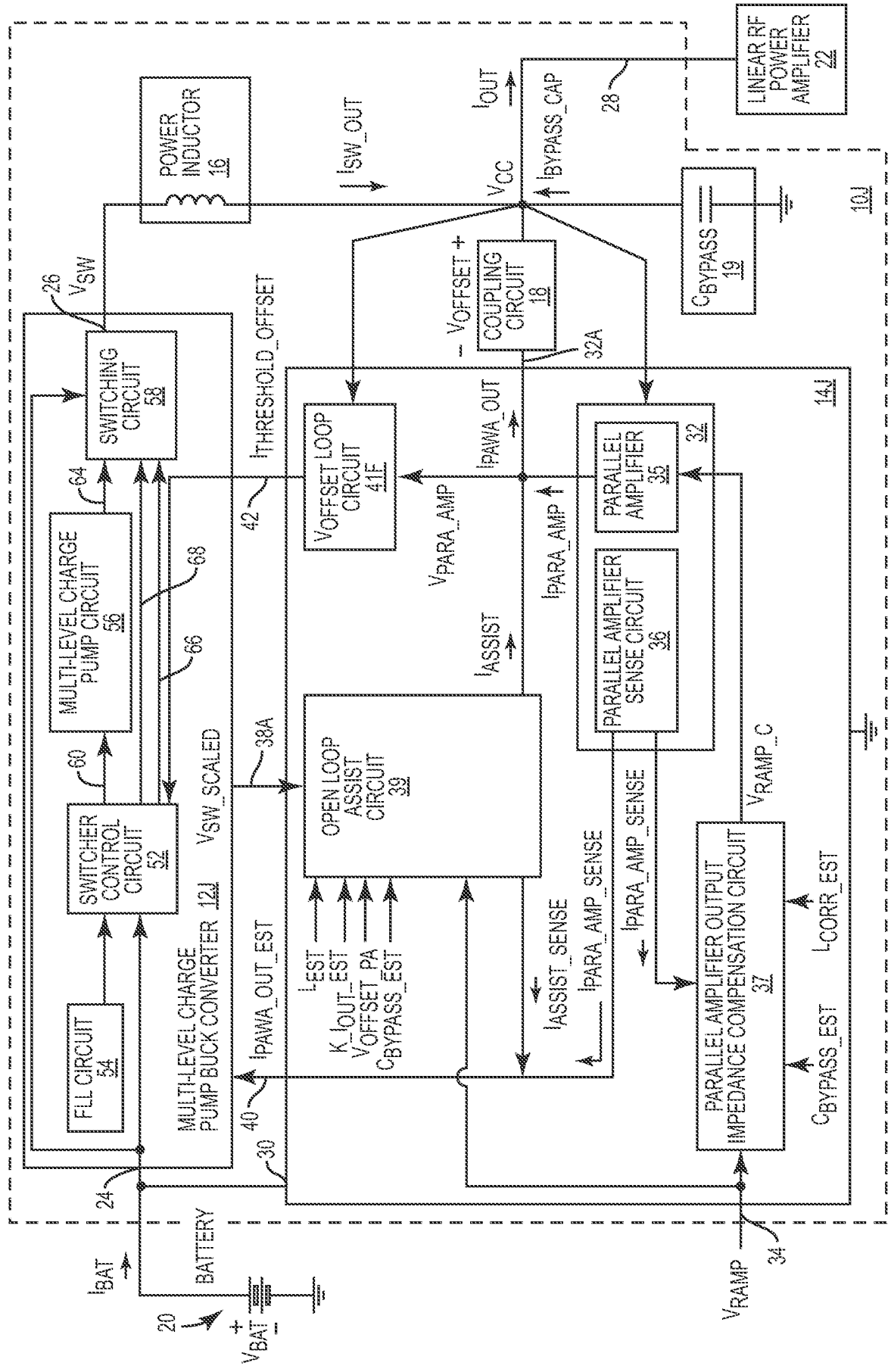

BATTERY
20
I_{BAT}
V_{BAT}
24
30
40
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12J
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 52
60
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
SWITCHING CIRCUIT 58
26
V_{SW}
POWER INDUCTOR 16
I_{SW_OUT}
I_{OUT}
V_{CC}
I_{BYPASS_CAP}
28
LINEAR RF POWER AMPLIFIER 22
C_{BYPASS} 19
10J
$-V_{OFFSET}+$
COUPLING CIRCUIT 18
32A
$I_{THRESHOLD_OFFSET}$
42
V_{OFFSET} LOOP CIRCUIT 41E
I_{PAWA_OUT}
14J
PARALLEL AMPLIFIER 35
32
V_{PARA_AMP}
I_{PARA_AMP}
PARALLEL AMPLIFIER SENSE CIRCUIT 36
I_{ASSIST}
66
68
V_{SW_SCALED}
38A
OPEN LOOP ASSIST CIRCUIT 39
I_{EST}
$K_I_{OUT_EST}$
V_{OFFSET_PA}
C_{BYPASS_EST}
$I_{PAWA_OUT_EST}$
I_{ASSIST_SENSE}
$I_{PARA_AMP_SENSE}$
$I_{PARA_AMP_SENSE}$
V_{RAMP_C}
PARALLEL AMPLIFIER OUTPUT IMPEDANCE COMPENSATION CIRCUIT 37
L_{CORR_EST}
C_{BYPASS_EST}
V_{RAMP}
34

FIG. 16

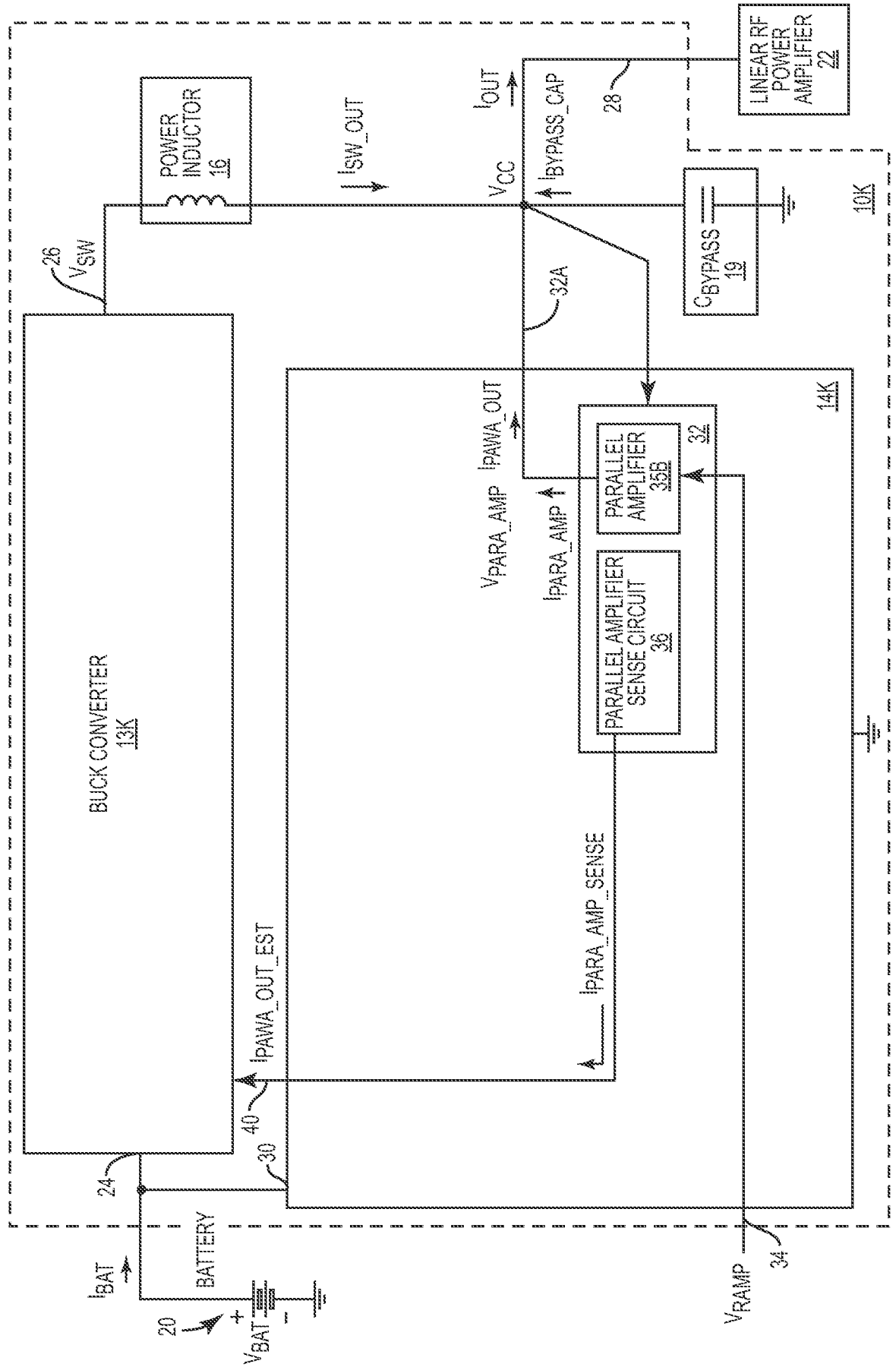

BUCK CONVERTER
13K
POWER INDUCTOR
16
LINEAR RF POWER AMPLIFIER
22
BATTERY
20
I_{BAT}
V_{BAT}
I_{SW_OUT}
I_{OUT}
V_{CC}
I_{BYPASS_CAP}
C_{BYPASS}
19
$I_{PAWA_OUT_EST}$
I_{PAWA_OUT}
V_{PARA_AMP}
I_{PARA_AMP}
$I_{PARA_AMP_SENSE}$
PARALLEL AMPLIFIER
35B
PARALLEL AMPLIFIER SENSE CIRCUIT
36
V_{RAMP}
14K
10K
24
26
28
30
32
32A
34
40

FIG. 17A

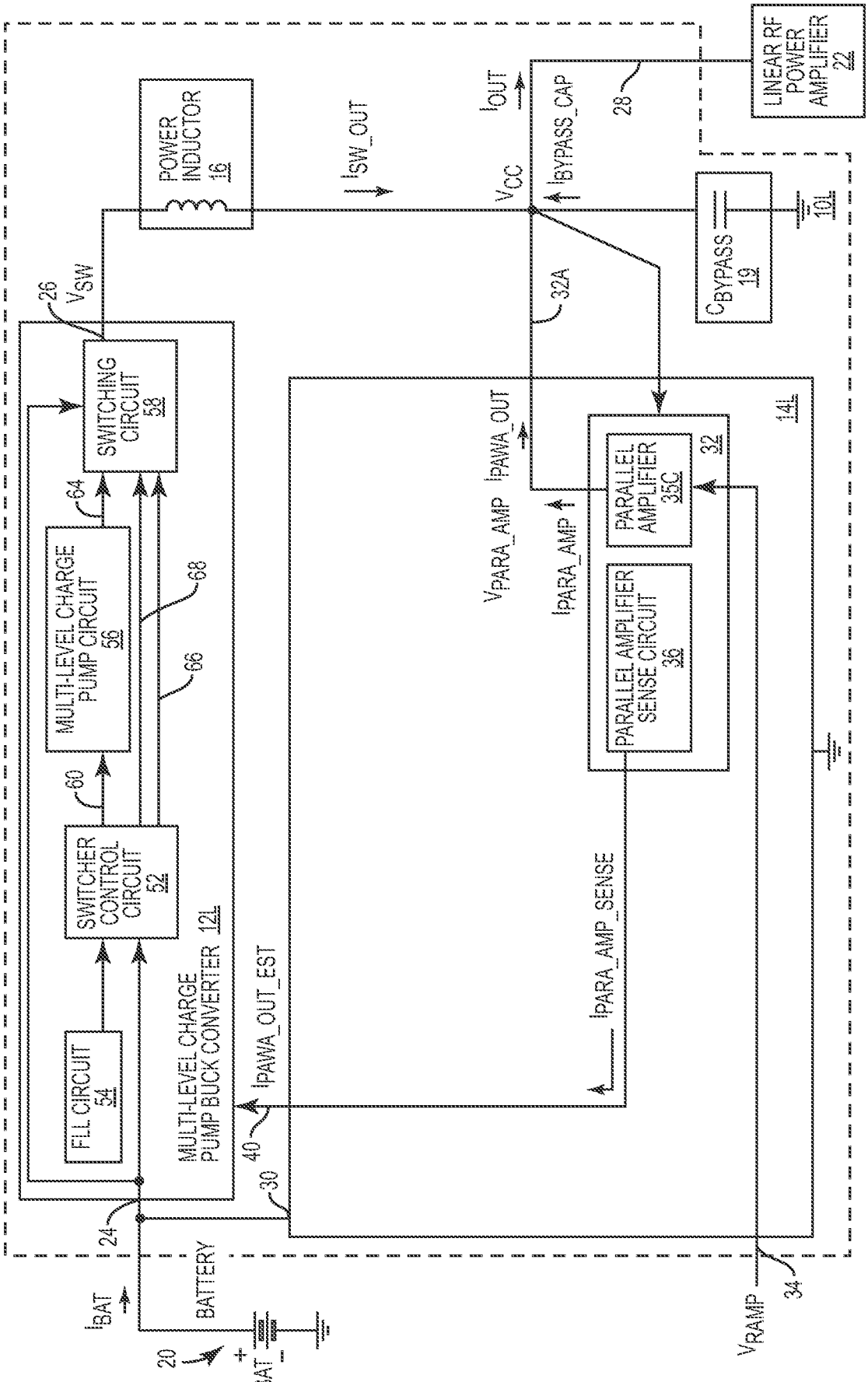

LINEAR RF POWER AMPLIFIER 22
28
I_{OUT}
I_{BYPASS_CAP}
V_{CC}
I_{SW_OUT}
POWER INDUCTOR 16
C_{BYPASS} 19
10L
32A
26
V_{SW}
SWITCHING CIRCUIT 58
64
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
68
66
60
SWITCHER CONTROL CIRCUIT 52
FLL CIRCUIT 54
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12L
$I_{PAWA_OUT_EST}$
40
30
24
I_{BAT}
BATTERY
20
V_{BAT}
V_{PARA_AMP}
I_{PAWA_OUT}
I_{PARA_AMP}
PARALLEL AMPLIFIER 35C
32
PARALLEL AMPLIFIER SENSE CIRCUIT 36
$I_{PARA_AMP_SENSE}$
14L
V_{RAMP}
34

FIG. 17B

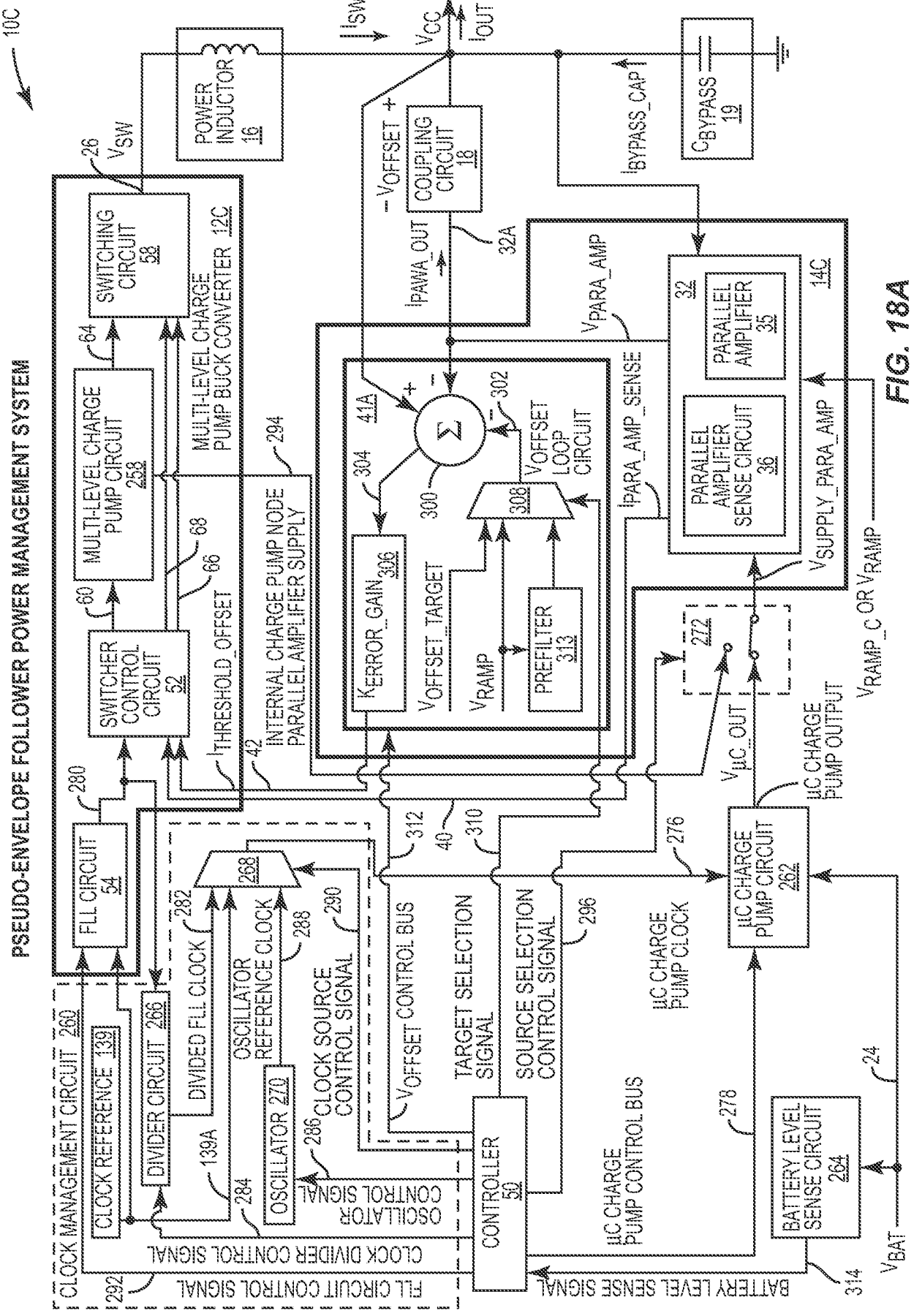

10C
PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM
POWER INDUCTOR 16
I_{SW_OUT}
V_{CC}
I_{OUT}
I_{BYPASS_CAP}
C_{BYPASS} 19
26 V_{SW}
SWITCHING CIRCUIT 58
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12C
MULTI-LEVEL CHARGE PUMP CIRCUIT 25B
64
60
SWITCHER CONTROL CIRCUIT 52
68
66
$I_{THRESHOLD_OFFSET}$
42
294
INTERNAL CHARGE PUMP NODE PARALLEL AMPLIFIER SUPPLY
$-V_{OFFSET}$ +
COUPLING CIRCUIT 18
32A
I_{PAWA_OUT}
V_{PARA_AMP}
32
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
14C
$I_{PARA_AMP_SENSE}$
$V_{SUPPLY_PARA_AMP}$
41A
304
300
302
K_{ERROR_GAIN} 306
V_{OFFSET_TARGET}
V_{RAMP}
308
V_{OFFSET} LOOP CIRCUIT
PREFILTER 313
272
$V_{\mu C_OUT}$
V_{RAMP_C} OR V_{RAMP}
μC CHARGE PUMP OUTPUT
280
FLL CIRCUIT 54
312
40
310
276
μC CHARGE PUMP CIRCUIT 262
CLOCK MANAGEMENT CIRCUIT 260
CLOCK REFERENCE 139
DIVIDER CIRCUIT 266
DIVIDED FLL CLOCK
282
268
OSCILLATOR REFERENCE CLOCK
288
290
139A
284
OSCILLATOR 270
286
CLOCK SOURCE CONTROL SIGNAL
V_{OFFSET} CONTROL BUS
TARGET SELECTION SIGNAL
SOURCE SELECTION CONTROL SIGNAL
296
μC CHARGE PUMP CLOCK
μC CHARGE PUMP CONTROL BUS
278
CONTROLLER 50
OSCILLATOR CONTROL SIGNAL
CLOCK DIVIDER CONTROL SIGNAL
FLL CIRCUIT CONTROL SIGNAL
292
BATTERY LEVEL SENSE SIGNAL
BATTERY LEVEL SENSE CIRCUIT 264
24
314
V_{BAT}

FIG. 18A

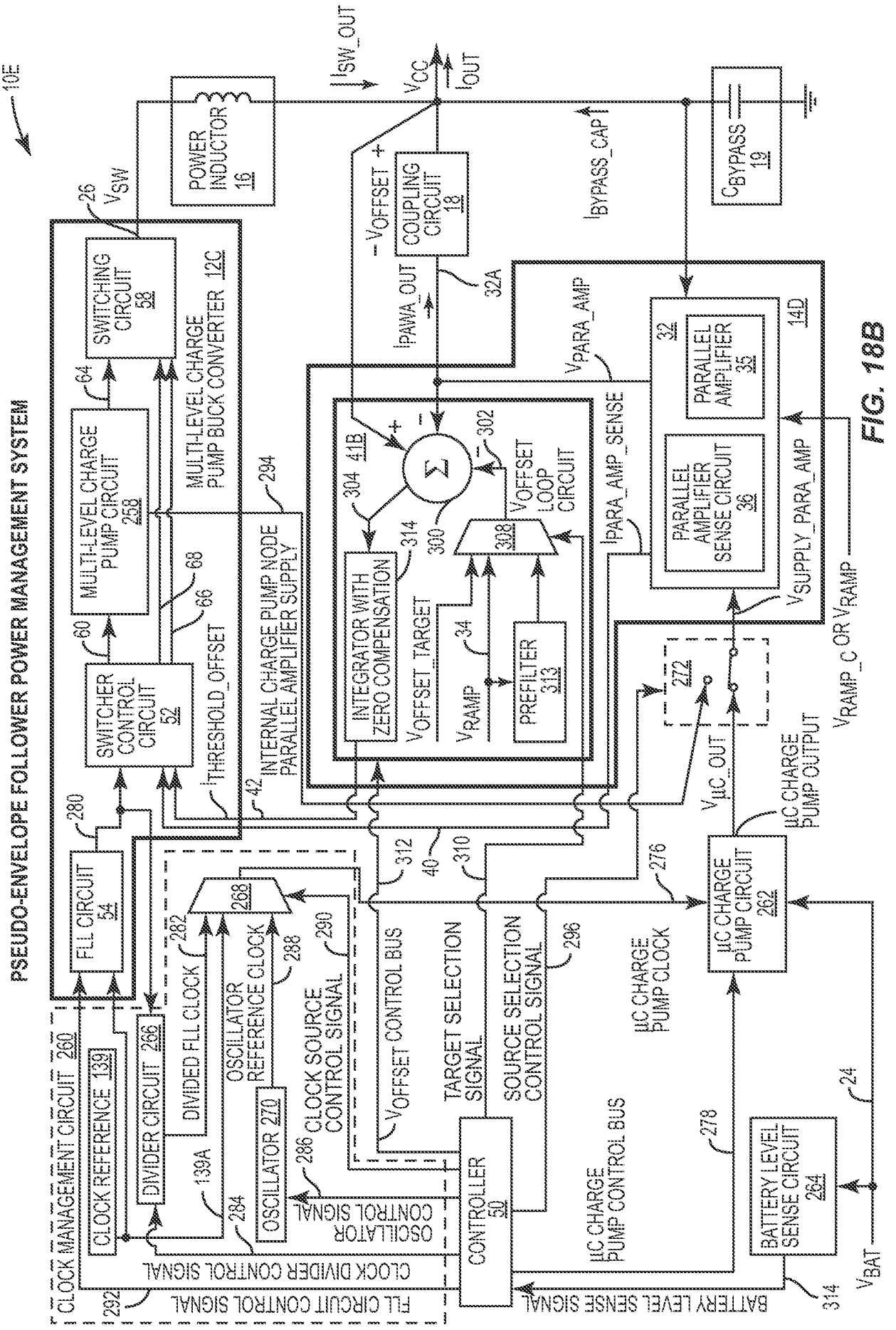

10E
PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM
POWER INDUCTOR 16
I_{SW_OUT}
V_{CC}
I_{OUT}
C_{BYPASS} 19
I_{BYPASS_CAP}
26 V_{SW}
SWITCHING CIRCUIT 58
64
MULTI-LEVEL CHARGE PUMP CIRCUIT 258
60
MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12C
$-V_{OFFSET}$ +
COUPLING CIRCUIT 18
I_{PAWA_OUT}
32A
V_{PARA_AMP}
32
PARALLEL AMPLIFIER 35
14D
PARALLEL AMPLIFIER SENSE CIRCUIT 39
$I_{PARA_AMP_SENSE}$
$V_{SUPPLY_PARA_AMP}$
294
INTERNAL CHARGE PUMP NODE PARALLEL AMPLIFIER SUPPLY
42
304 41B
302
300
314
INTEGRATOR WITH ZERO COMPENSATION
V_{OFFSET_TARGET}
308
V_{OFFSET} LOOP CIRCUIT
V_{RAMP} 34
PREFILTER 313
$I_{THRESHOLD_OFFSET}$
68
66
SWITCHER CONTROL CIRCUIT 52
280
FLL CIRCUIT 54
268
282
DIVIDED FLL CLOCK
OSCILLATOR REFERENCE CLOCK
288
290
CLOCK SOURCE CONTROL SIGNAL
286
OSCILLATOR CONTROL SIGNAL
284
OSCILLATOR 270
139A
DIVIDER CIRCUIT 266
CLOCK REFERENCE 139
CLOCK MANAGEMENT CIRCUIT 260
292
FLL CIRCUIT CONTROL SIGNAL
CLOCK DIVIDER CONTROL SIGNAL
312
40
310
V_{OFFSET} CONTROL BUS
TARGET SELECTION SIGNAL
SOURCE SELECTION CONTROL SIGNAL
296
276
272
$V_{\mu C_OUT}$
V_{RAMP_C} OR V_{RAMP}
μC CHARGE PUMP OUTPUT
μC CHARGE PUMP CIRCUIT 262
μC CHARGE PUMP CLOCK
μC CHARGE PUMP CONTROL BUS
278
CONTROLLER 50
BATTERY LEVEL SENSE SIGNAL
BATTERY LEVEL SENSE CIRCUIT 264
24
314
V_{BAT}

FIG. 18B

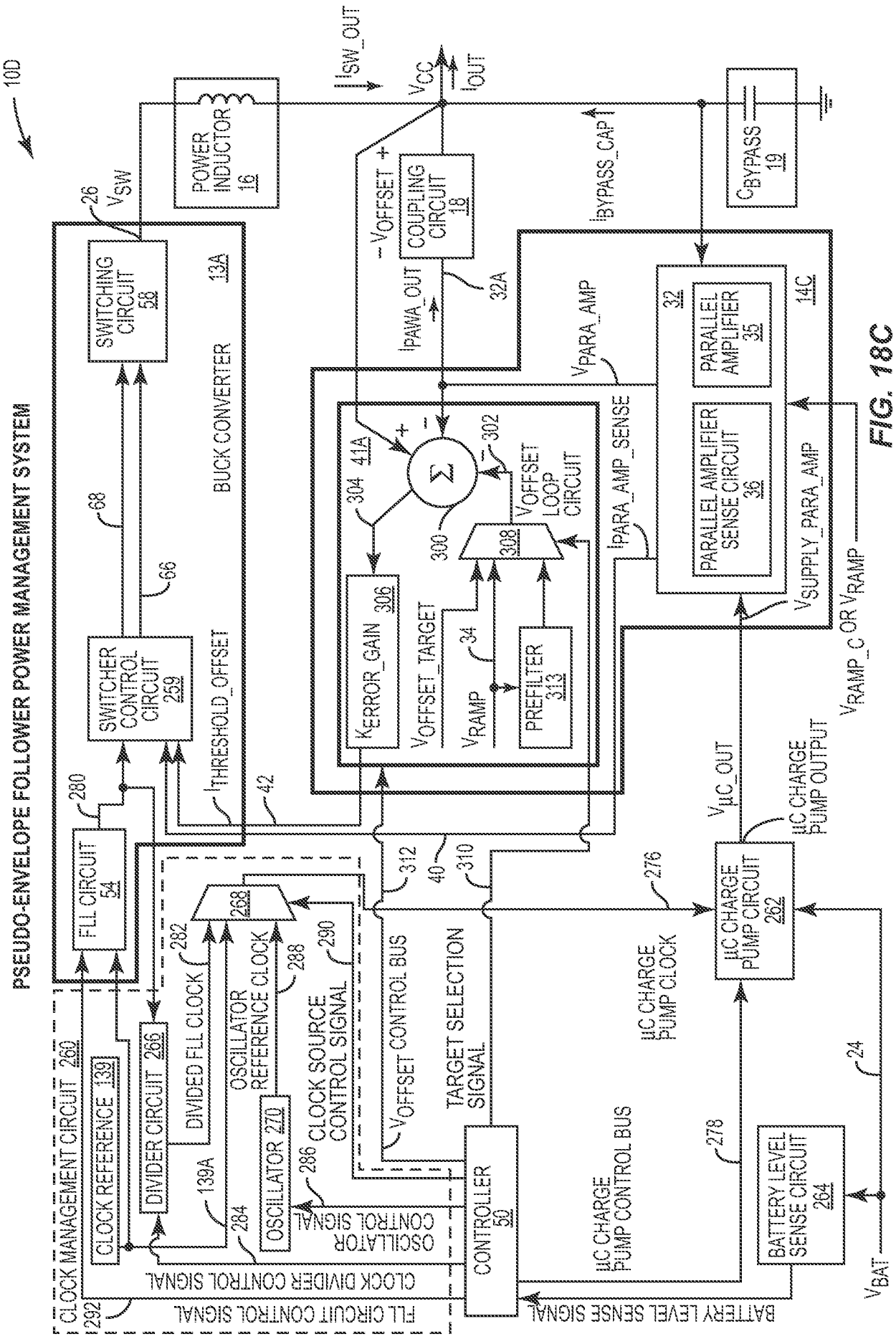

10D
PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM
POWER INDUCTOR 16
I_{SW_OUT}
V_{CC}
I_{OUT}
C_{BYPASS} 19
I_{BYPASS_CAP}
SWITCHING CIRCUIT 58
26
V_{SW}
BUCK CONVERTER 13A
$-V_{OFFSET}$ +
COUPLING CIRCUIT 18
I_{PAWA_OUT}
32A
V_{PARA_AMP}
32
PARALLEL AMPLIFIER 35
14C
PARALLEL AMPLIFIER SENSE CIRCUIT 36
$I_{PARA_AMP_SENSE}$
$V_{SUPPLY_PARA_AMP}$
V_{RAMP_C} OR V_{RAMP}
68
66
SWITCHER CONTROL CIRCUIT 259
$I_{THRESHOLD_OFFSET}$
42
280
FLL CIRCUIT 54
304
41A
302
300
308
V_{OFFSET} LOOP CIRCUIT
K_{ERROR_GAIN} 306
V_{OFFSET_TARGET}
V_{RAMP}
34
PREFILTER 313
312
40
310
276
$V_{\mu C_OUT}$
μC CHARGE PUMP OUTPUT
CLOCK MANAGEMENT CIRCUIT 260
CLOCK REFERENCE 139
DIVIDER CIRCUIT 266
139A
284
DIVIDED FLL CLOCK
282
OSCILLATOR REFERENCE CLOCK
268
288
290
OSCILLATOR 270
286
CLOCK SOURCE CONTROL SIGNAL
V_{OFFSET} CONTROL BUS
TARGET SELECTION SIGNAL
μC CHARGE PUMP CLOCK
μC CHARGE PUMP CIRCUIT 262
CONTROLLER 50
μC CHARGE PUMP CONTROL BUS
278
24
BATTERY LEVEL SENSE CIRCUIT 264
V_{BAT}
292
CLOCK DIVIDER CONTROL SIGNAL
FLL CIRCUIT CONTROL SIGNAL
OSCILLATOR CONTROL SIGNAL
BATTERY LEVEL SENSE SIGNAL

FIG. 18C

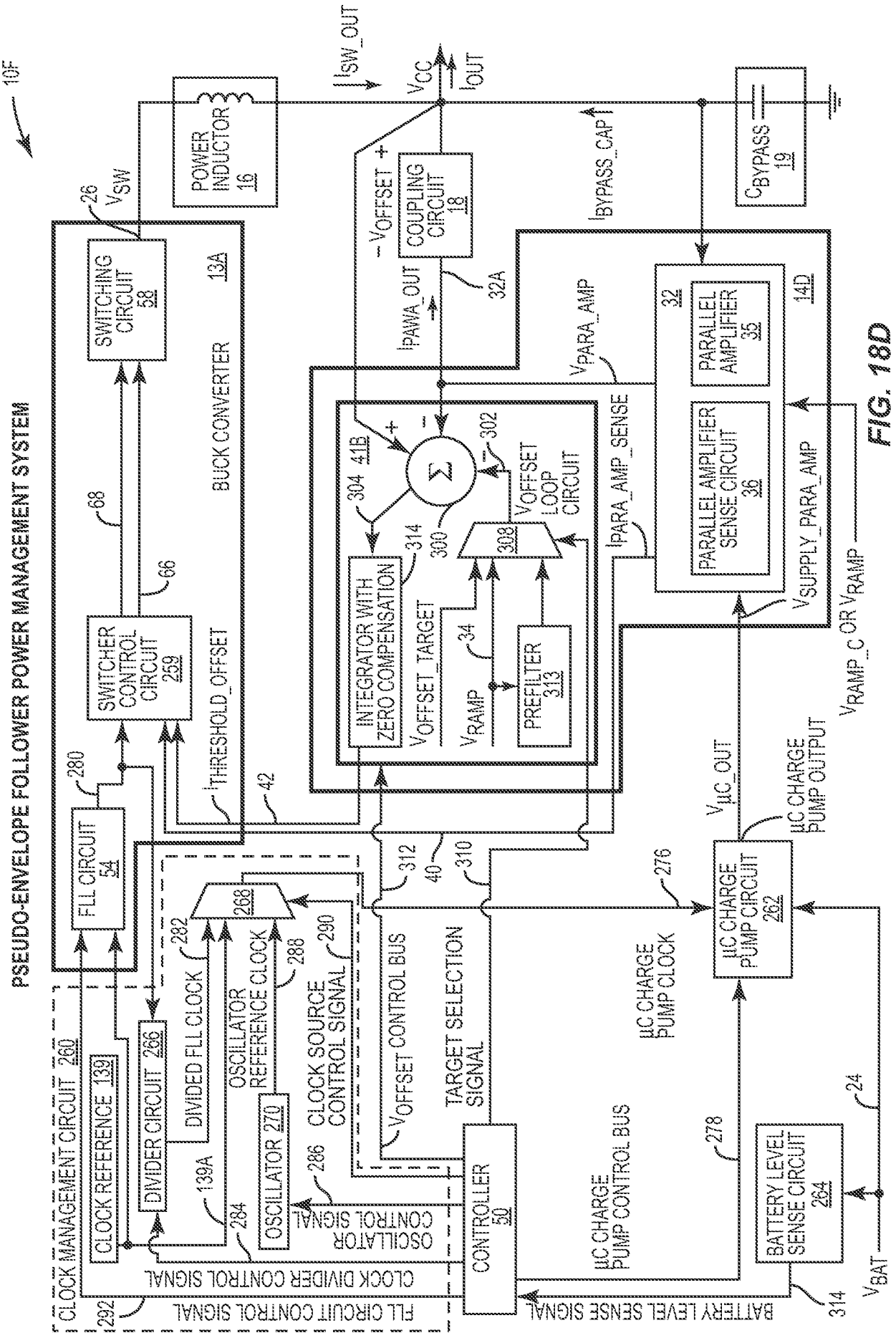

10F
PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM
POWER INDUCTOR 16
I_{SW_OUT}
V_{CC}
I_{OUT}
26
V_{SW}
SWITCHING CIRCUIT 58
BUCK CONVERTER 13A
68
66
SWITCHER CONTROL CIRCUIT 259
$I_{THRESHOLD_OFFSET}$
42
280
FLL CIRCUIT 54
CLOCK MANAGEMENT CIRCUIT 260
CLOCK REFERENCE 139
DIVIDER CIRCUIT 266
DIVIDED FLL CLOCK
282
139A
284
OSCILLATOR REFERENCE CLOCK
OSCILLATOR 270
288
286
CLOCK SOURCE CONTROL SIGNAL
290
268
OSCILLATOR CONTROL SIGNAL
292
FLL CIRCUIT CONTROL SIGNAL
CLOCK DIVIDER CONTROL SIGNAL
CONTROLLER 50
312
40
310
$V_{OFFSET_CONTROL\ BUS}$
TARGET SELECTION SIGNAL
276
μC CHARGE PUMP CLOCK
μC CHARGE PUMP CONTROL BUS
278
μC CHARGE PUMP CIRCUIT 262
$V_{\mu C_OUT}$
μC CHARGE PUMP OUTPUT
BATTERY LEVEL SENSE CIRCUIT 264
BATTERY LEVEL SENSE SIGNAL
24
314
V_{BAT}
$-V_{OFFSET}$ +
COUPLING CIRCUIT 18
I_{PAWA_OUT}
32A
I_{BYPASS_CAP}
C_{BYPASS} 19
V_{PARA_AMP}
32
PARALLEL AMPLIFIER 35
14D
PARALLEL AMPLIFIER SENSE CIRCUIT 36
$I_{PARA_AMP_SENSE}$
$V_{SUPPLY_PARA_AMP}$
V_{RAMP_C} OR V_{RAMP}
INTEGRATOR WITH ZERO COMPENSATION
314
304
41B
300
302
308
V_{OFFSET} LOOP CIRCUIT
V_{OFFSET_TARGET}
V_{RAMP}
34
PREFILTER 313

FIG. 18D

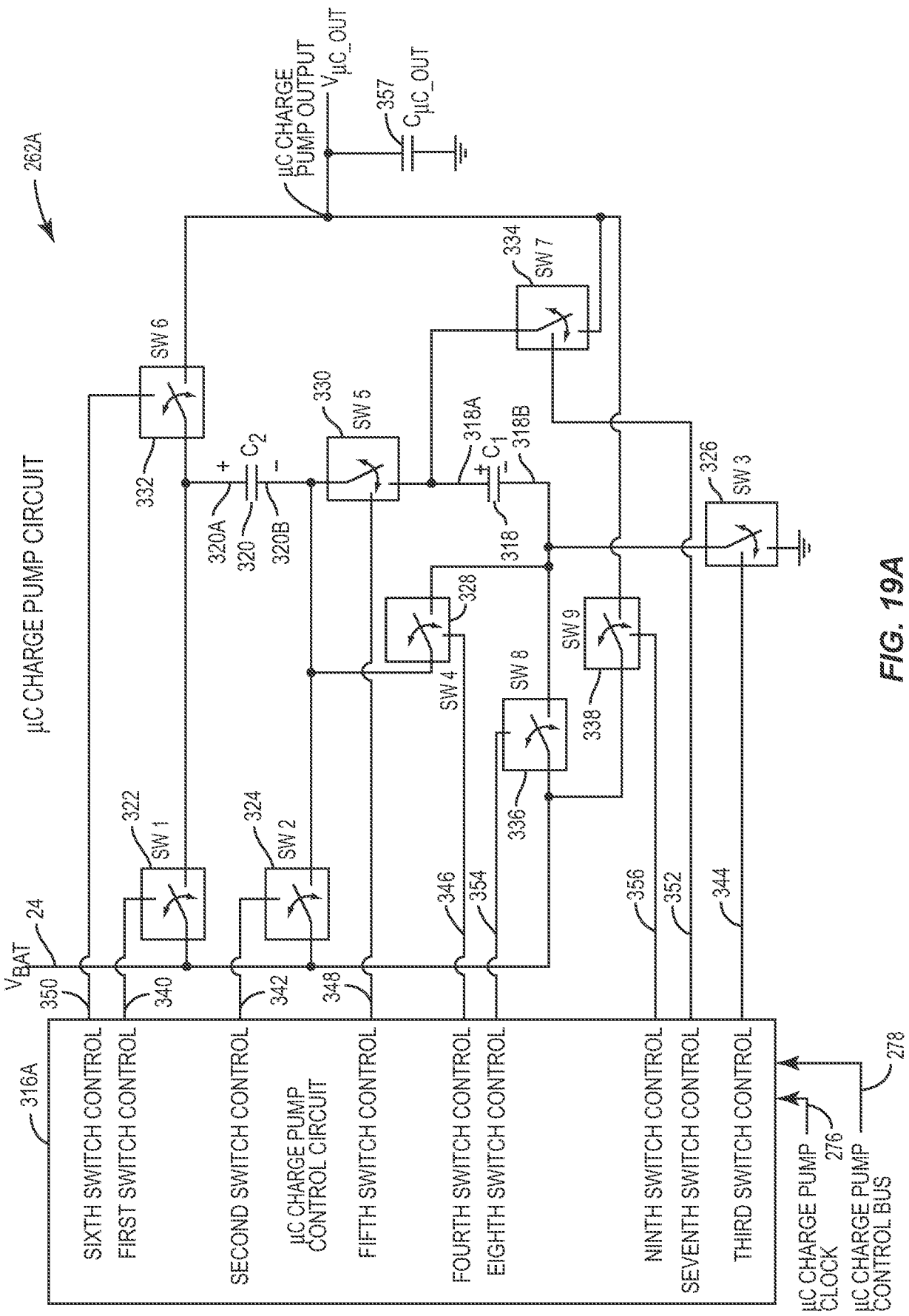

262A
μC CHARGE PUMP CIRCUIT
μC CHARGE PUMP OUTPUT
$V_{\mu C_OUT}$
357
$C_{\mu C_OUT}$
334
SW 7
330
SW 5
332
SW 6
C_2
320A
320
320B
318A
C_1
318B
318
326
SW 3
322
SW 1
324
SW 2
328
SW 4
SW 8
SW 9
336
338
V_{BAT}
24
350
340
342
348
346
354
356
352
344
316A
SIXTH SWITCH CONTROL
FIRST SWITCH CONTROL
SECOND SWITCH CONTROL
μC CHARGE PUMP CONTROL CIRCUIT
FIFTH SWITCH CONTROL
FOURTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
NINTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
THIRD SWITCH CONTROL
μC CHARGE PUMP CLOCK
276
μC CHARGE PUMP CONTROL BUS
278

FIG. 19A

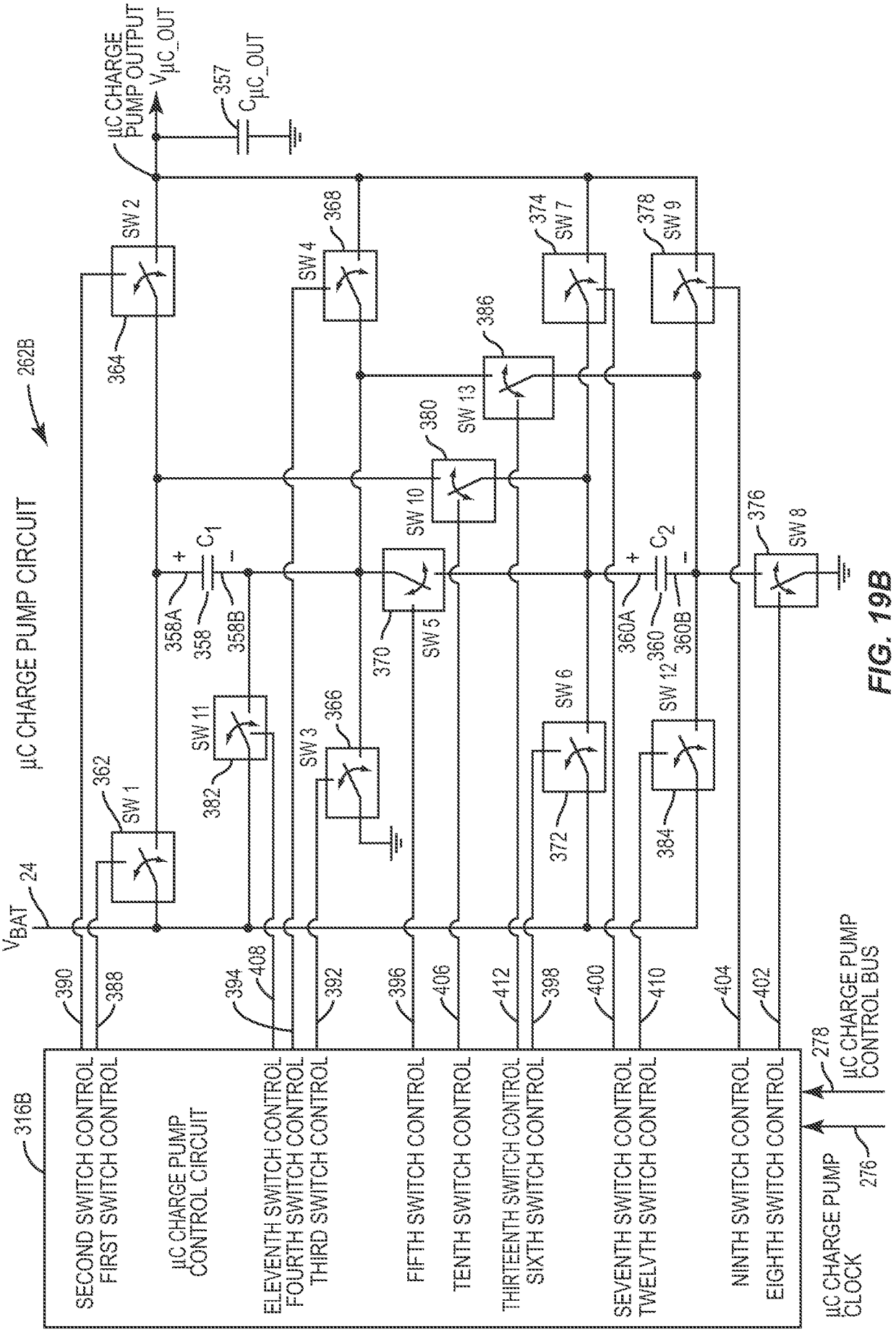

262B
µC CHARGE PUMP CIRCUIT
µC CHARGE PUMP OUTPUT
$V_{\mu C_OUT}$
357
$C_{\mu C_OUT}$
V_{BAT}
24
316B
SECOND SWITCH CONTROL
FIRST SWITCH CONTROL
µC CHARGE PUMP CONTROL CIRCUIT
ELEVENTH SWITCH CONTROL
FOURTH SWITCH CONTROL
THIRD SWITCH CONTROL
FIFTH SWITCH CONTROL
TENTH SWITCH CONTROL
THIRTEENTH SWITCH CONTROL
SIXTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
TWELVTH SWITCH CONTROL
NINTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
µC CHARGE PUMP CLOCK
276
278
µC CHARGE PUMP CONTROL BUS
SW 1
SW 2
SW 3
SW 4
SW 5
SW 6
SW 7
SW 8
SW 9
SW 10
SW 11
SW 12
SW 13
362
364
366
368
370
372
374
376
378
380
382
384
386
C_1
C_2
358A
358
358B
360A
360
360B
388
390
392
394
396
398
400
402
404
406
408
410
412

FIG. 19B

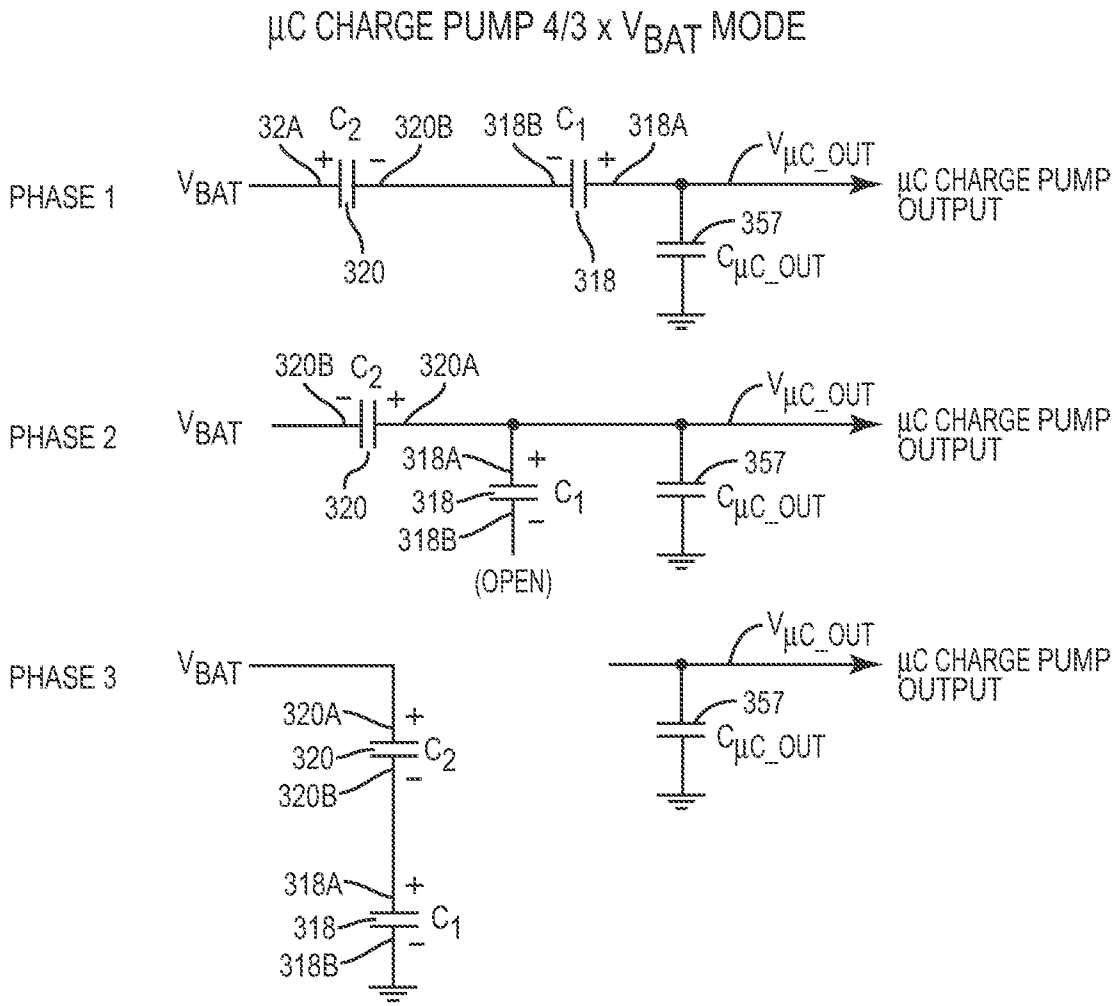

µC CHARGE PUMP 4/3 x V_{BAT} MODE
PHASE 1
PHASE 2
PHASE 3
V_{BAT}
32A
C_2
320B
318B
C_1
318A
$V_{µC_OUT}$
µC CHARGE PUMP OUTPUT
357
$C_{µC_OUT}$
320
318
320B
320A
318A
318B
(OPEN)

FIG. 20A

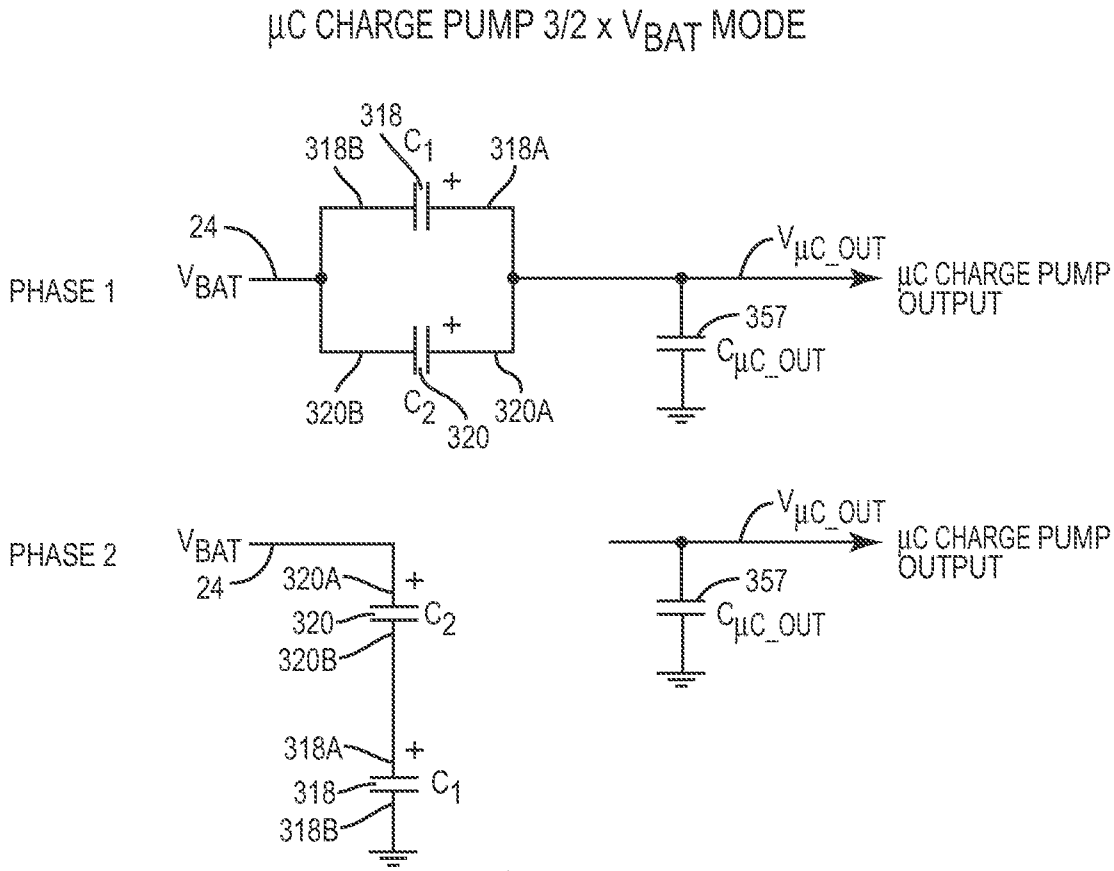


FIG. 20B

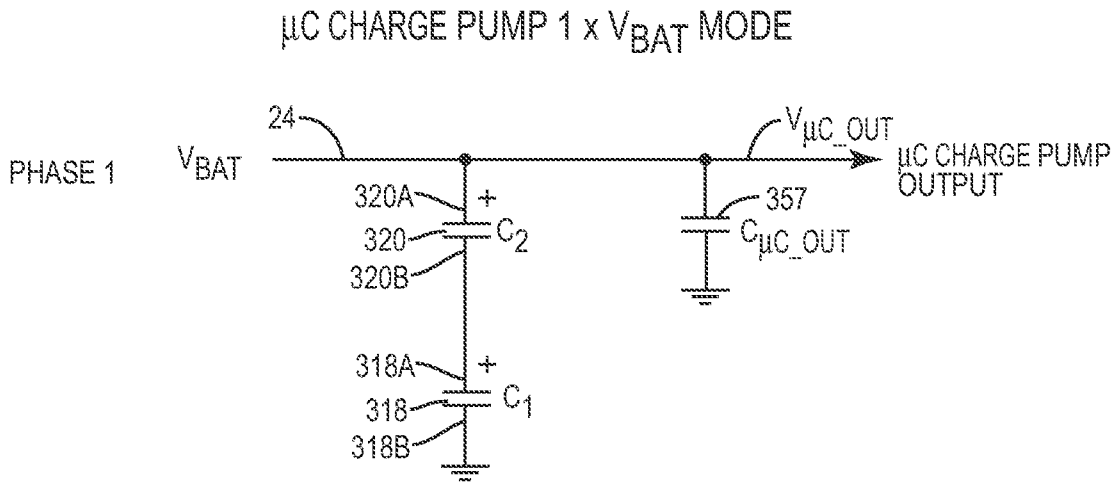


FIG. 20C

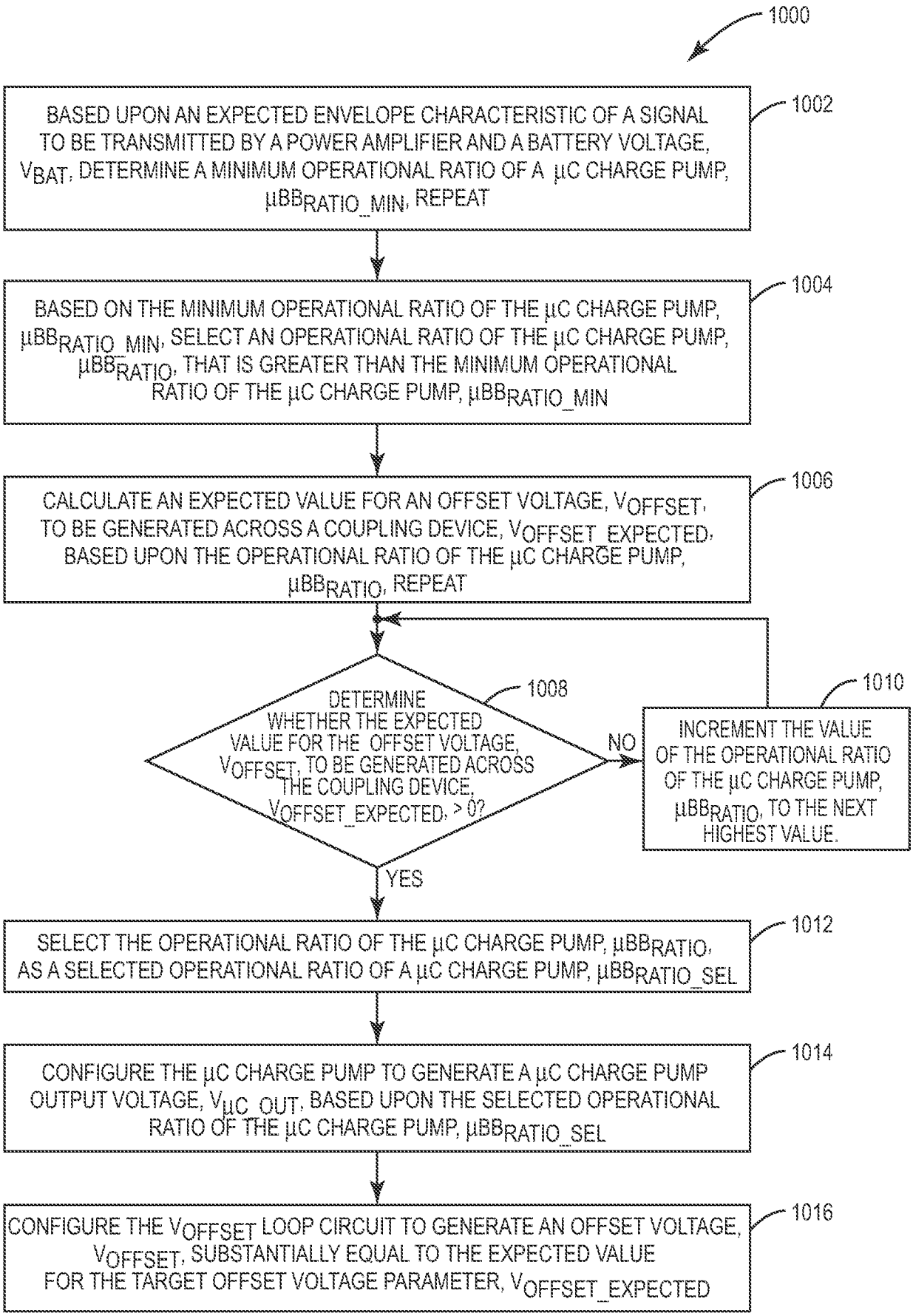

1000
BASED UPON AN EXPECTED ENVELOPE CHARACTERISTIC OF A SIGNAL TO BE TRANSMITTED BY A POWER AMPLIFIER AND A BATTERY VOLTAGE, V_{BAT}, DETERMINE A MINIMUM OPERATIONAL RATIO OF A µC CHARGE PUMP, μBB_{RATIO_MIN}, REPEAT
1002
BASED ON THE MINIMUM OPERATIONAL RATIO OF THE µC CHARGE PUMP, μBB_{RATIO_MIN}, SELECT AN OPERATIONAL RATIO OF THE µC CHARGE PUMP, μBB_{RATIO}, THAT IS GREATER THAN THE MINIMUM OPERATIONAL RATIO OF THE µC CHARGE PUMP, μBB_{RATIO_MIN}
1004
CALCULATE AN EXPECTED VALUE FOR AN OFFSET VOLTAGE, V_{OFFSET}, TO BE GENERATED ACROSS A COUPLING DEVICE, $V_{OFFSET_EXPECTED}$, BASED UPON THE OPERATIONAL RATIO OF THE µC CHARGE PUMP, μBB_{RATIO}, REPEAT
1006
DETERMINE WHETHER THE EXPECTED VALUE FOR THE OFFSET VOLTAGE, V_{OFFSET}, TO BE GENERATED ACROSS THE COUPLING DEVICE, $V_{OFFSET_EXPECTED}$, > 0?
1008
NO
INCREMENT THE VALUE OF THE OPERATIONAL RATIO OF THE µC CHARGE PUMP, μBB_{RATIO}, TO THE NEXT HIGHEST VALUE.
1010
YES
SELECT THE OPERATIONAL RATIO OF THE µC CHARGE PUMP, μBB_{RATIO}, AS A SELECTED OPERATIONAL RATIO OF A µC CHARGE PUMP, μBB_{RATIO_SEL}
1012
CONFIGURE THE µC CHARGE PUMP TO GENERATE A µC CHARGE PUMP OUTPUT VOLTAGE, $V_{\mu C_OUT}$, BASED UPON THE SELECTED OPERATIONAL RATIO OF THE µC CHARGE PUMP, μBB_{RATIO_SEL}
1014
CONFIGURE THE V_{OFFSET} LOOP CIRCUIT TO GENERATE AN OFFSET VOLTAGE, V_{OFFSET}, SUBSTANTIALLY EQUAL TO THE EXPECTED VALUE FOR THE TARGET OFFSET VOLTAGE PARAMETER, $V_{OFFSET_EXPECTED}$
1016

FIG. 21

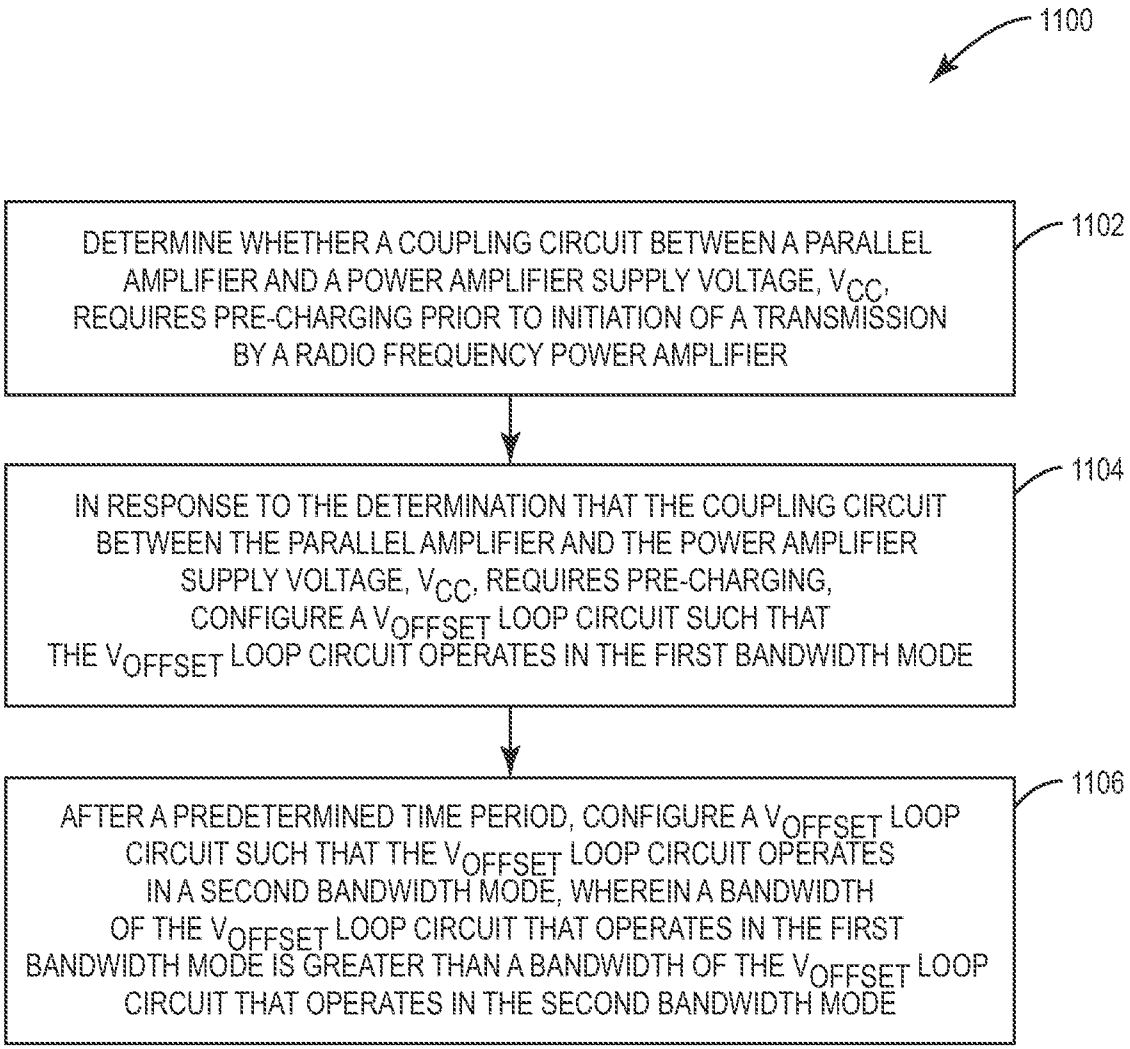

1100
DETERMINE WHETHER A COUPLING CIRCUIT BETWEEN A PARALLEL AMPLIFIER AND A POWER AMPLIFIER SUPPLY VOLTAGE, V_{CC}, REQUIRES PRE-CHARGING PRIOR TO INITIATION OF A TRANSMISSION BY A RADIO FREQUENCY POWER AMPLIFIER
1102
IN RESPONSE TO THE DETERMINATION THAT THE COUPLING CIRCUIT BETWEEN THE PARALLEL AMPLIFIER AND THE POWER AMPLIFIER SUPPLY VOLTAGE, V_{CC}, REQUIRES PRE-CHARGING, CONFIGURE A V_{OFFSET} LOOP CIRCUIT SUCH THAT THE V_{OFFSET} LOOP CIRCUIT OPERATES IN THE FIRST BANDWIDTH MODE
1104
AFTER A PREDETERMINED TIME PERIOD, CONFIGURE A V_{OFFSET} LOOP CIRCUIT SUCH THAT THE V_{OFFSET} LOOP CIRCUIT OPERATES IN A SECOND BANDWIDTH MODE, WHEREIN A BANDWIDTH OF THE V_{OFFSET} LOOP CIRCUIT THAT OPERATES IN THE FIRST BANDWIDTH MODE IS GREATER THAN A BANDWIDTH OF THE V_{OFFSET} LOOP CIRCUIT THAT OPERATES IN THE SECOND BANDWIDTH MODE
1106

FIG. 22

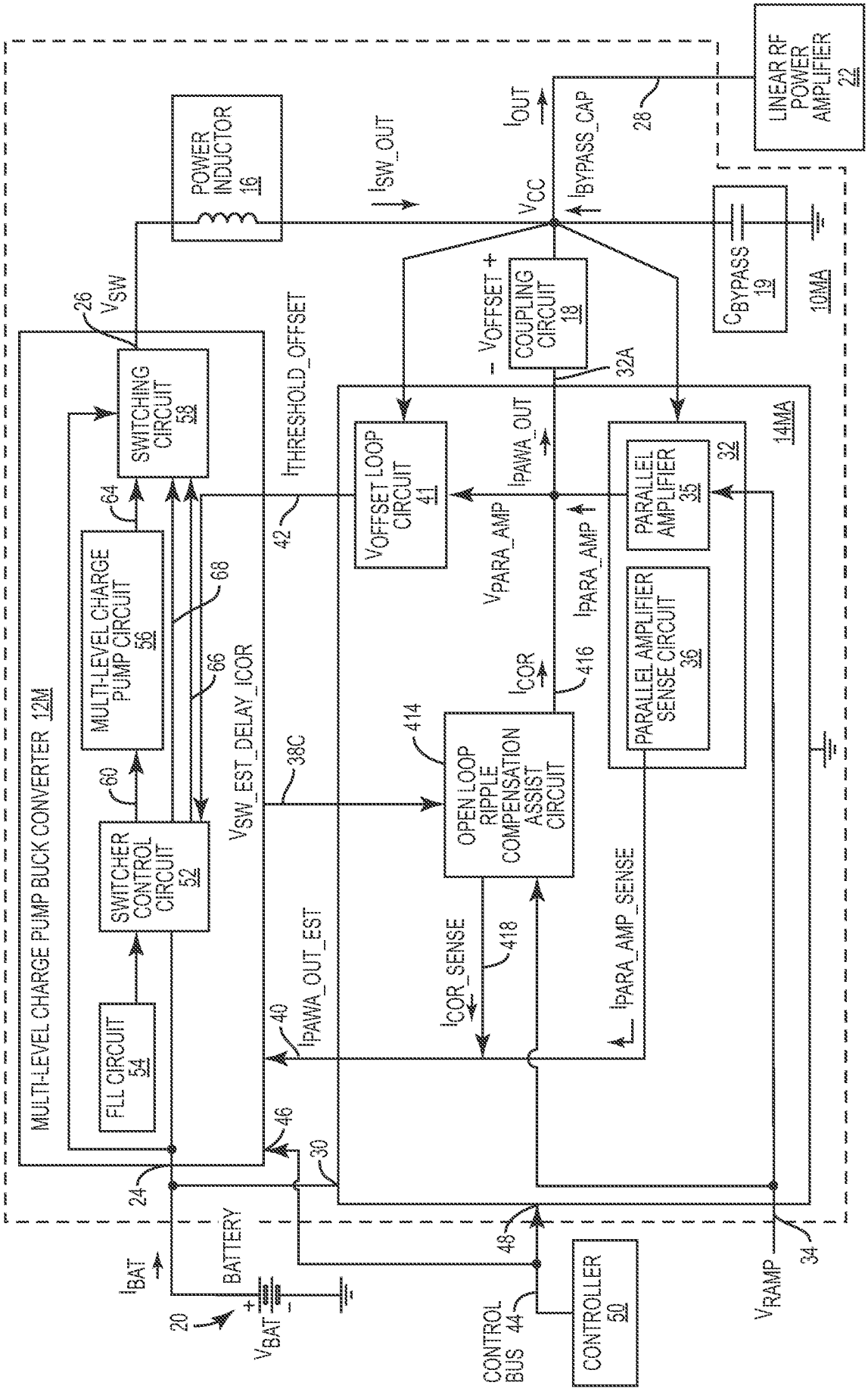

MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12M
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 52
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
SWITCHING CIRCUIT 58
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
COUPLING CIRCUIT 18
CBYPASS 19
10MA
14MA
VOFFSET LOOP CIRCUIT 41
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
BATTERY
CONTROLLER 50
CONTROL BUS 44
VSW
VSW_EST_DELAY_ICOR
ITHRESHOLD_OFFSET
ISW_OUT
IOUT
VCC
IBYPASS_CAP
IPAWA_OUT
IPAWA_OUT_EST
VPARA_AMP
IPARA_AMP
IPARA_AMP_SENSE
ICOR
ICOR_SENSE
IBAT
VBAT
VRAMP
26
64
60
66
68
42
38C
414
416
418
40
46
30
24
48
34
20
28
32
32A

FIG. 23A

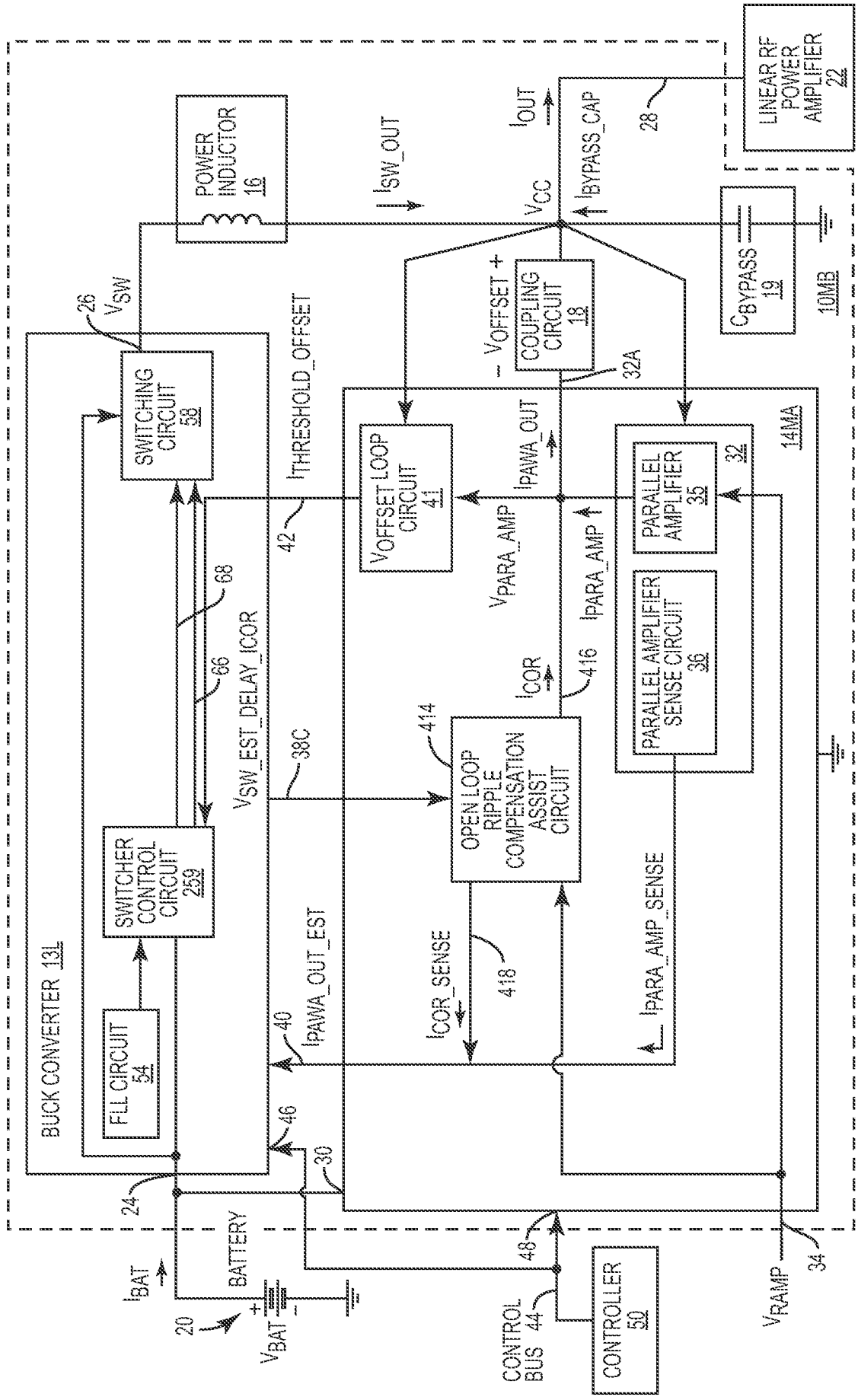

BUCK CONVERTER 13L
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 259
SWITCHING CIRCUIT 58
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
COUPLING CIRCUIT 18
CBYPASS 19
VOFFSET LOOP CIRCUIT 41
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
BATTERY
CONTROLLER 50
CONTROL BUS 44
VSW
ISW_OUT
IOUT
VCC
IBYPASS_CAP
VOFFSET
ITHRESHOLD_OFFSET
VSW_EST_DELAY_ICOR
IPAWA_OUT
VPARA_AMP
IPARA_AMP
ICOR
ICOR_SENSE
IPAWA_OUT_EST
IPARA_AMP_SENSE
IBAT
VBAT
VRAMP
10MB
14MA
20
24
26
28
30
32
32A
34
38C
40
42
46
48
66
68
414
416
418

FIG. 23B

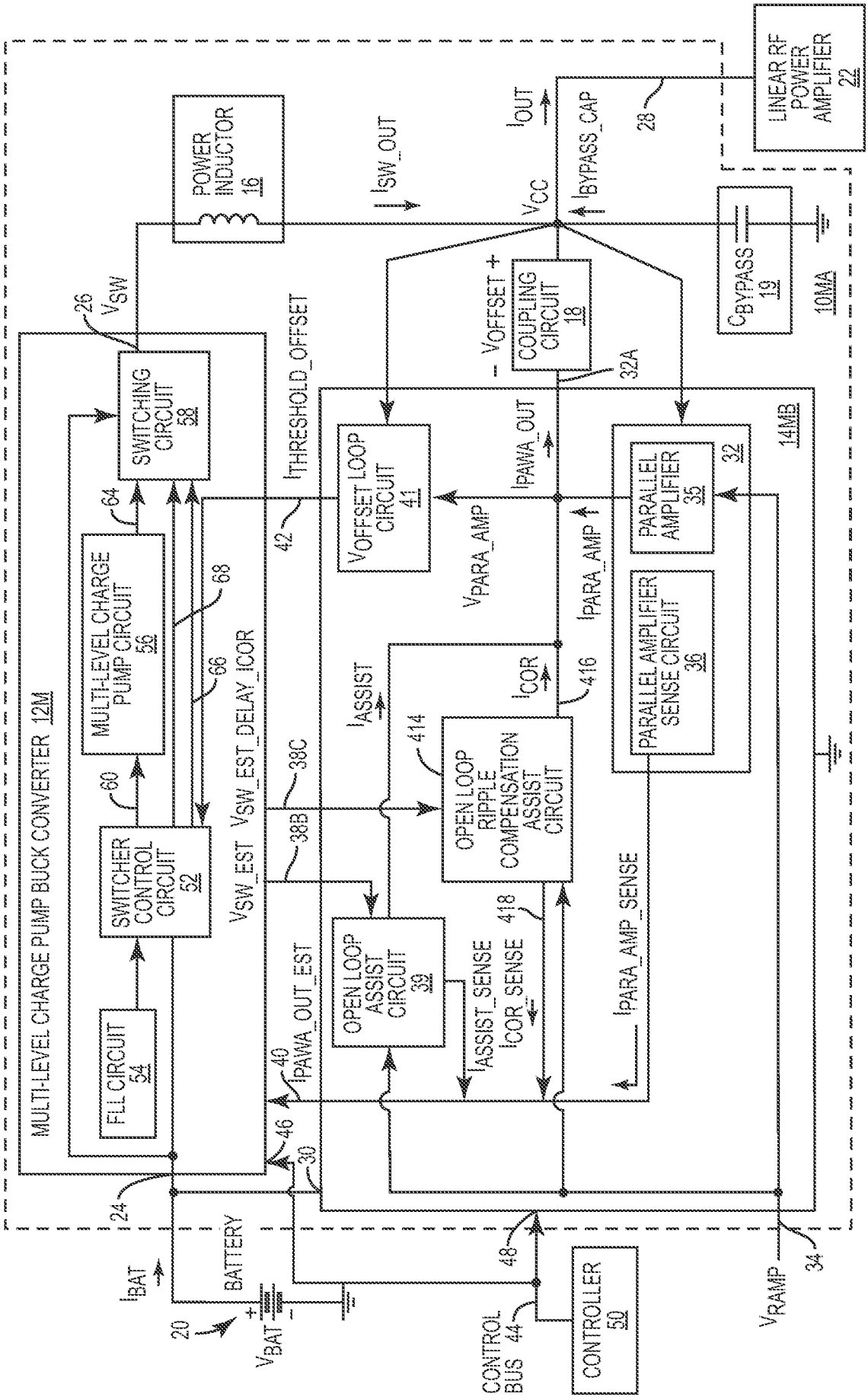

MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12M
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
SWITCHING CIRCUIT 58
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
SWITCHER CONTROL CIRCUIT 52
FLL CIRCUIT 54
OPEN LOOP ASSIST CIRCUIT 39
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT
VOFFSET LOOP CIRCUIT 41
COUPLING CIRCUIT 18
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
CBYPASS 19
10MA
14MB
CONTROLLER 50
BATTERY
ISW_OUT
IOUT
VCC
IBYPASS_CAP
VSW
ITHRESHOLD_OFFSET
VOFFSET +
VPARA_AMP
IPAWA_OUT
IPARA_AMP
IASSIST
ICOR
VSW_EST_DELAY_ICOR
VSW_EST
IPAWA_OUT_EST
IASSIST_SENSE
ICOR_SENSE
IPARA_AMP_SENSE
IBAT
VBAT
CONTROL BUS 44
VRAMP

FIG. 23C

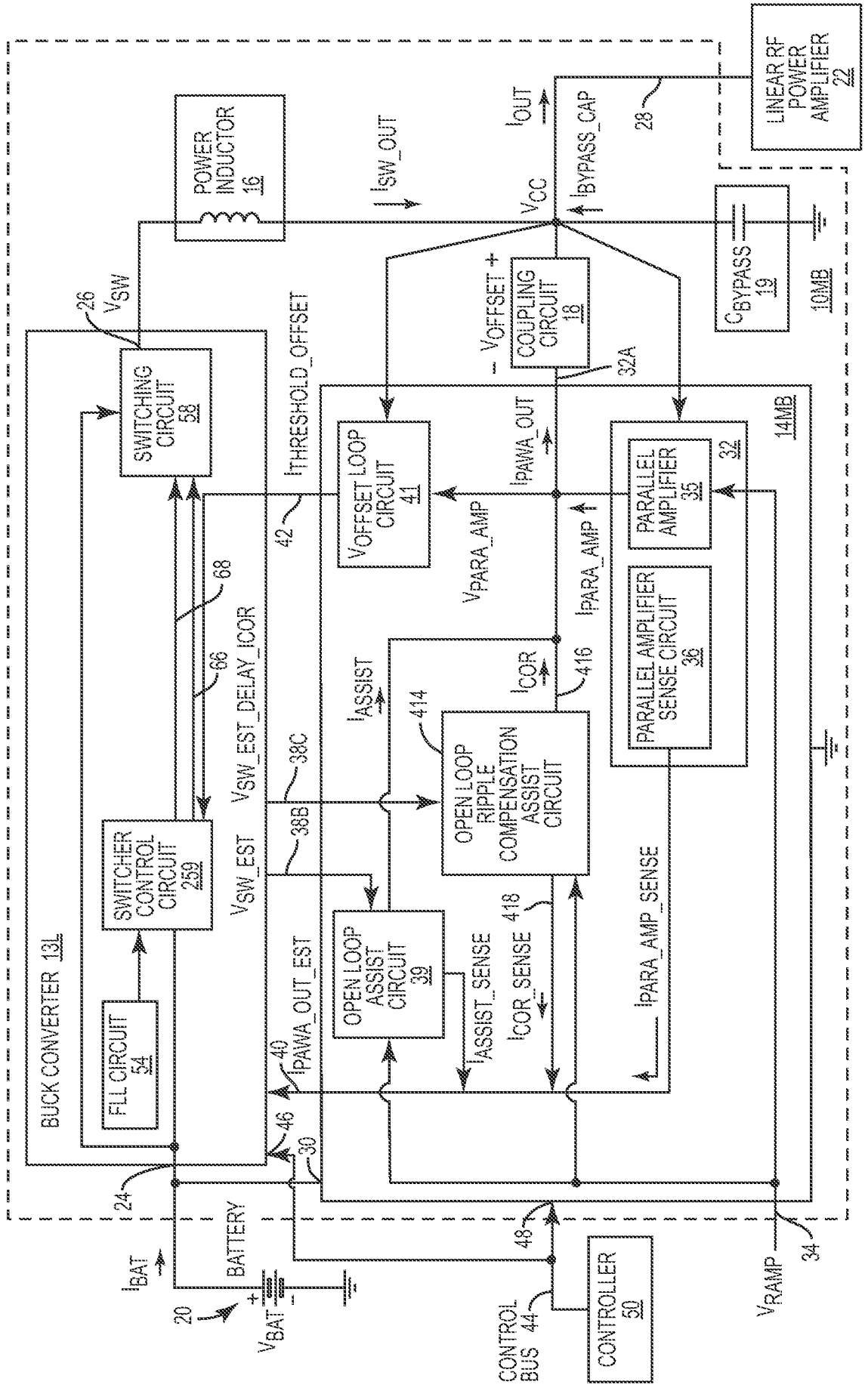

BUCK CONVERTER 13L
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 259
SWITCHING CIRCUIT 58
POWER INDUCTOR 16
26
VSW
VSW_EST
VSW_EST_DELAY_ICOR
68
66
38B
38C
42
ITHRESHOLD_OFFSET
VOFFSET LOOP CIRCUIT 41
VPARA_AMP
IPAWA_OUT
IPARA_AMP
ICOR
416
414
IASSIST
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT
OPEN LOOP ASSIST CIRCUIT 39
IASSIST_SENSE
ICOR_SENSE
418
IPARA_AMP_SENSE
PARALLEL AMPLIFIER SENSE CIRCUIT 36
PARALLEL AMPLIFIER 35
32
14MB
40
IPAWA_OUT_EST
46
30
24
BATTERY
IBAT
20
VBAT
48
CONTROL BUS 44
CONTROLLER 50
34
VRAMP
ISW_OUT
IOUT
VCC
IBYPASS_CAP
28
LINEAR RF POWER AMPLIFIER 22
CBYPASS 19
10MB
VOFFSET
COUPLING CIRCUIT 18
32A

FIG. 23D

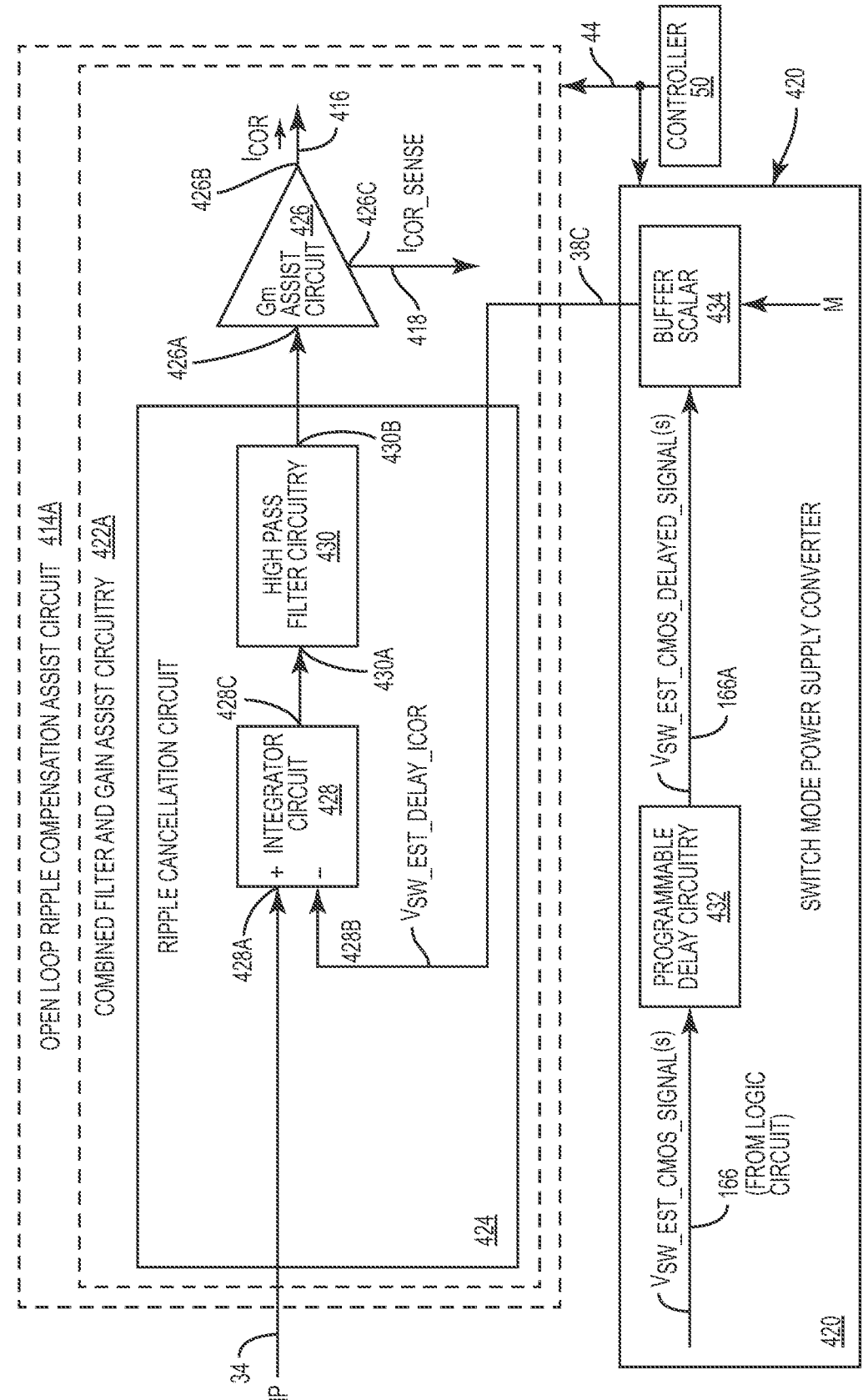

OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT 414A
COMBINED FILTER AND GAIN ASSIST CIRCUITRY 422A
RIPPLE CANCELLATION CIRCUIT
INTEGRATOR CIRCUIT 428
HIGH PASS FILTER CIRCUITRY 430
Gm ASSIST CIRCUIT 426
CONTROLLER 50
BUFFER SCALAR 434
PROGRAMMABLE DELAY CIRCUITRY 432
SWITCH MODE POWER SUPPLY CONVERTER
VRAMP
34
428A
428B
428C
430A
430B
426A
426B
426C
416
418
424
44
38C
420
M
166A
166
(FROM LOGIC CIRCUIT)
VSW_EST_DELAY_ICOR
VSW_EST_CMOS_DELAYED_SIGNAL(s)
VSW_EST_CMOS_SIGNAL(s)
ICOR
ICOR_SENSE

FIG. 24

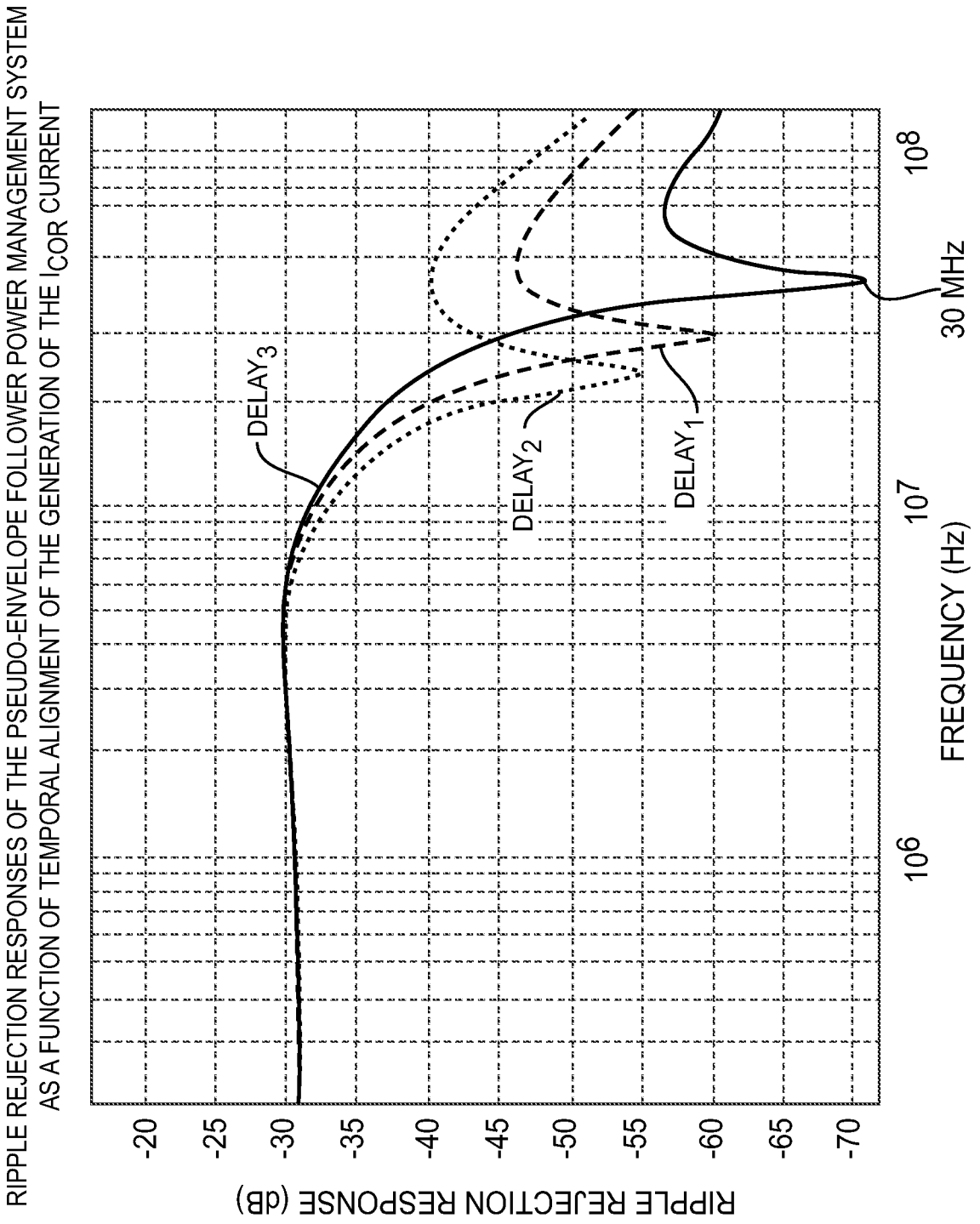

RIPPLE REJECTION RESPONSES OF THE PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM AS A FUNCTION OF TEMPORAL ALIGNMENT OF THE GENERATION OF THE I_{COR} CURRENT
RIPPLE REJECTION RESPONSE (dB)
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
-70
10^6
10^7
10^8
FREQUENCY (Hz)
30 MHz
$DELAY_3$
$DELAY_2$
$DELAY_1$

FIG. 25

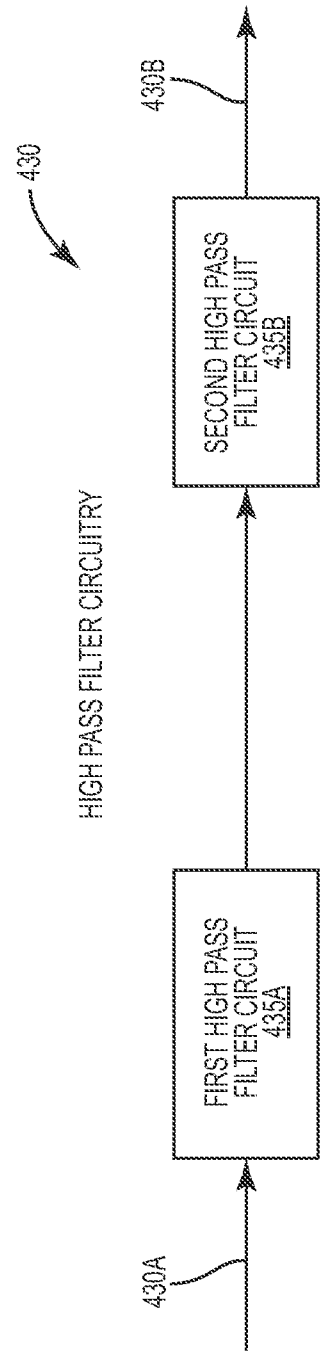

430
HIGH PASS FILTER CIRCUITRY
FIRST HIGH PASS FILTER CIRCUIT 435A
SECOND HIGH PASS FILTER CIRCUIT 435B
430A
430B

FIG. 26

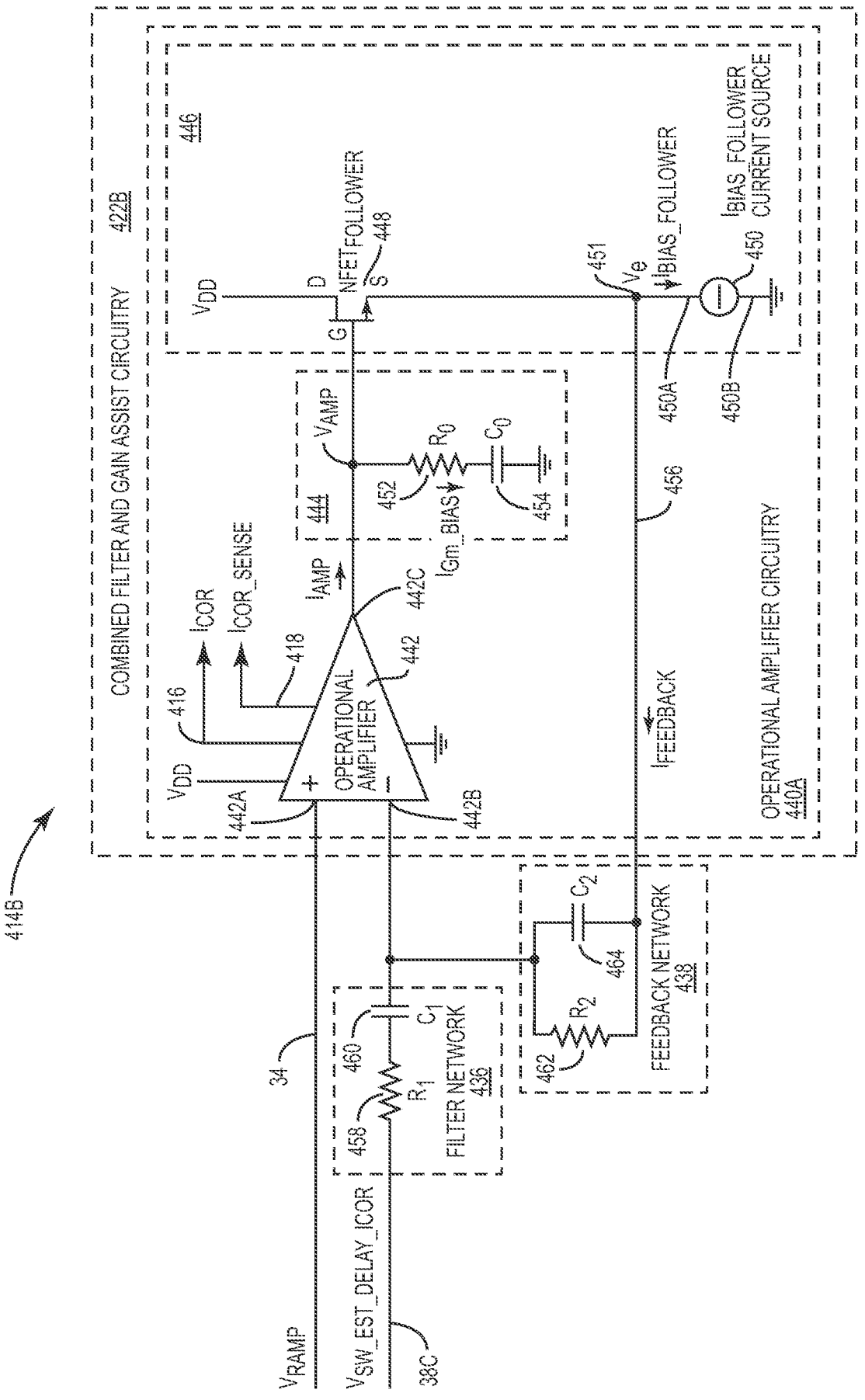

414B
COMBINED FILTER AND GAIN ASSIST CIRCUITRY 422B
446
VDD
D
NFET FOLLOWER
S
448
G
451
Ve
IBIAS_FOLLOWER
450
IBIAS_FOLLOWER CURRENT SOURCE
450A
450B
VAMP
444
R0
C0
452
454
IGm_BIAS
456
ICOR
ICOR_SENSE
416
418
IAMP
442C
442
OPERATIONAL AMPLIFIER
442A
442B
IFEEDBACK
OPERATIONAL AMPLIFIER CIRCUITRY 440A
34
460
C1
458
R1
FILTER NETWORK 436
462
R2
C2
464
FEEDBACK NETWORK 438
VRAMP
VSW_EST_DELAY_ICOR
38C

FIG. 27A

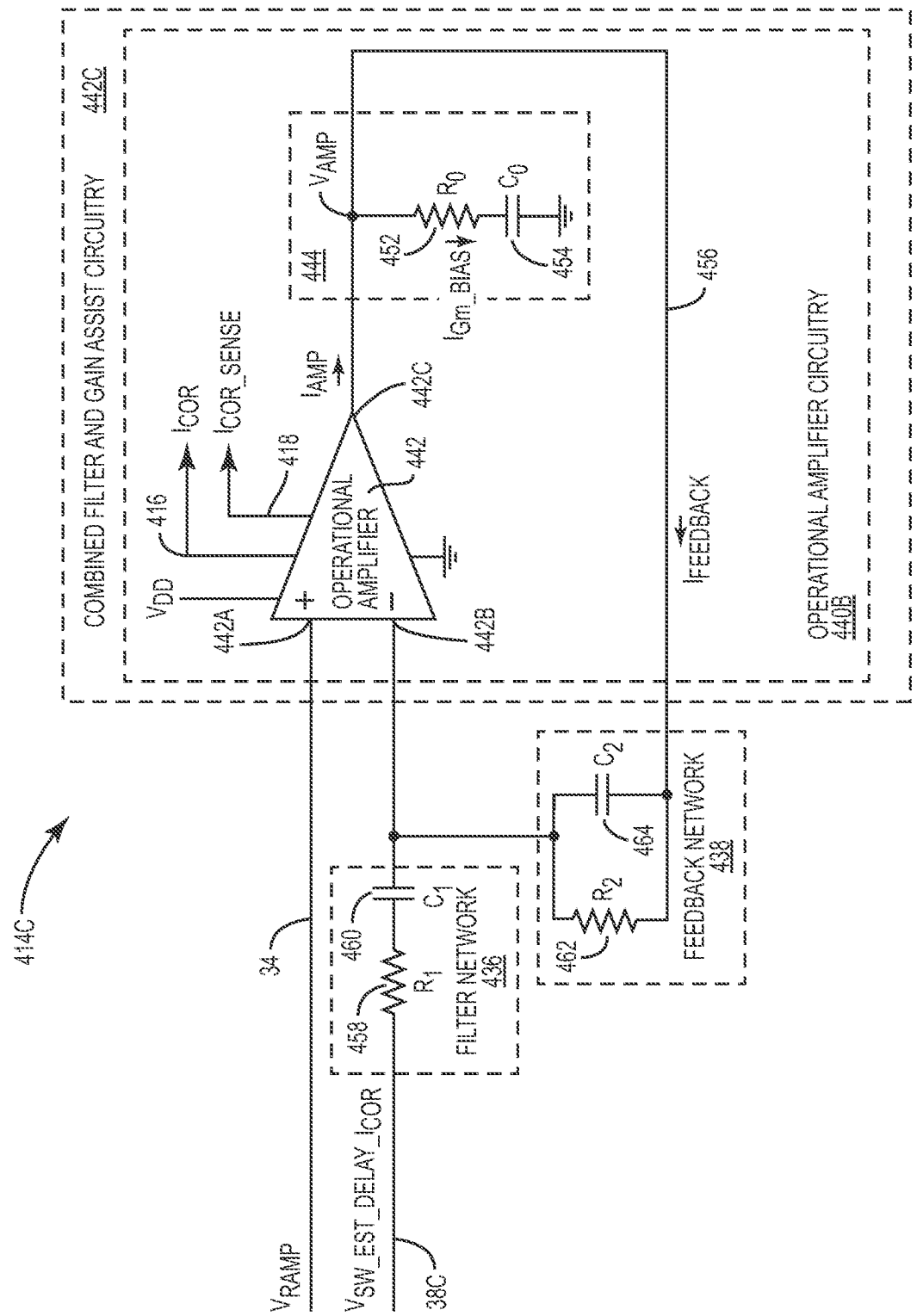

414C
COMBINED FILTER AND GAIN ASSIST CIRCUITRY 442C
OPERATIONAL AMPLIFIER 442
442A
442B
442C
VDD
416
ICOR
ICOR_SENSE
418
IAMP
VAMP
444
452
R0
C0
454
IGm_BIAS
456
IFEEDBACK
OPERATIONAL AMPLIFIER CIRCUITRY 440B
34
460
458
R1
C1
FILTER NETWORK 436
462
R2
C2
464
FEEDBACK NETWORK 438
VRAMP
VSW_EST_DELAY_ICOR
38C

FIG. 27B

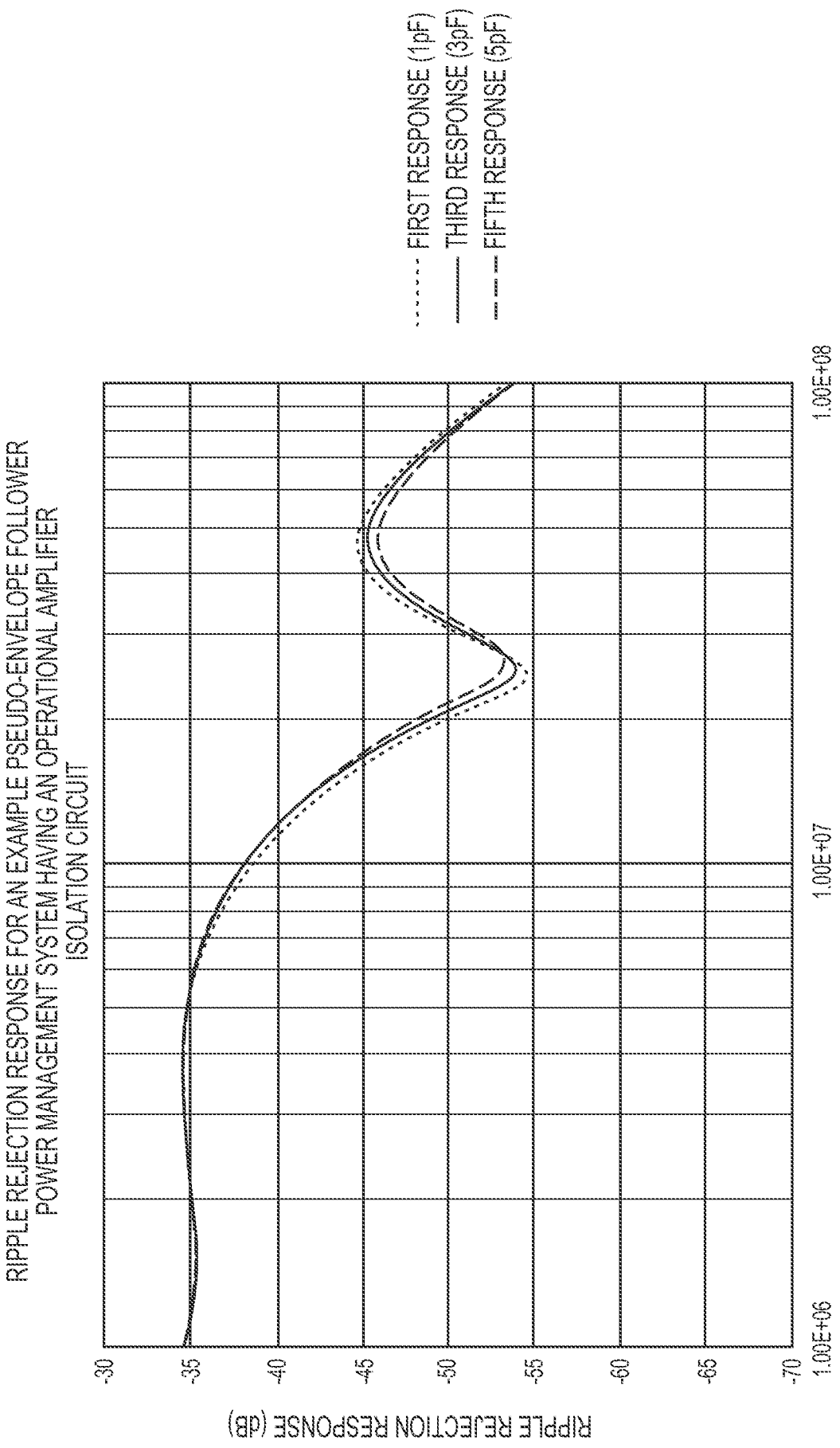

RIPPLE REJECTION RESPONSE FOR AN EXAMPLE PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM HAVING AN OPERATIONAL AMPLIFIER ISOLATION CIRCUIT
FIRST RESPONSE (1pF)
THIRD RESPONSE (3pF)
FIFTH RESPONSE (5pF)
RIPPLE REJECTION RESPONSE (dB)
-30
-35
-40
-45
-50
-55
-60
-65
-70
1.00E+06
1.00E+07
1.00E+08
FREQUENCY

FIG. 28A

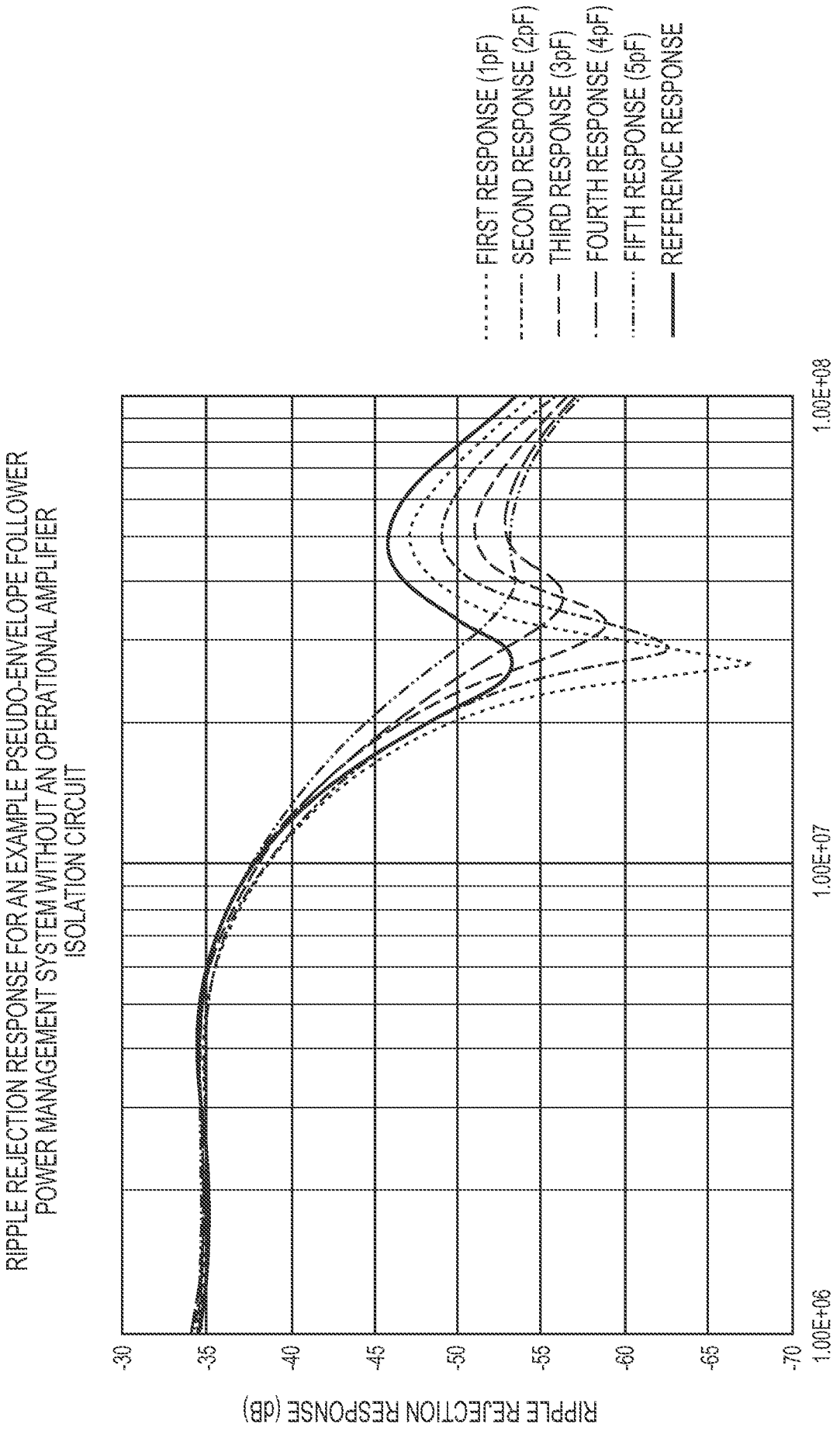

RIPPLE REJECTION RESPONSE FOR AN EXAMPLE PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM WITHOUT AN OPERATIONAL AMPLIFIER ISOLATION CIRCUIT
FIRST RESPONSE (1pF)
SECOND RESPONSE (2pF)
THIRD RESPONSE (3pF)
FOURTH RESPONSE (4pF)
FIFTH RESPONSE (5pF)
REFERENCE RESPONSE
RIPPLE REJECTION RESPONSE (dB)
-30
-35
-40
-45
-50
-55
-60
-65
-70
1.00E+06
1.00E+07
1.00E+08
FREQUENCY

FIG. 28B

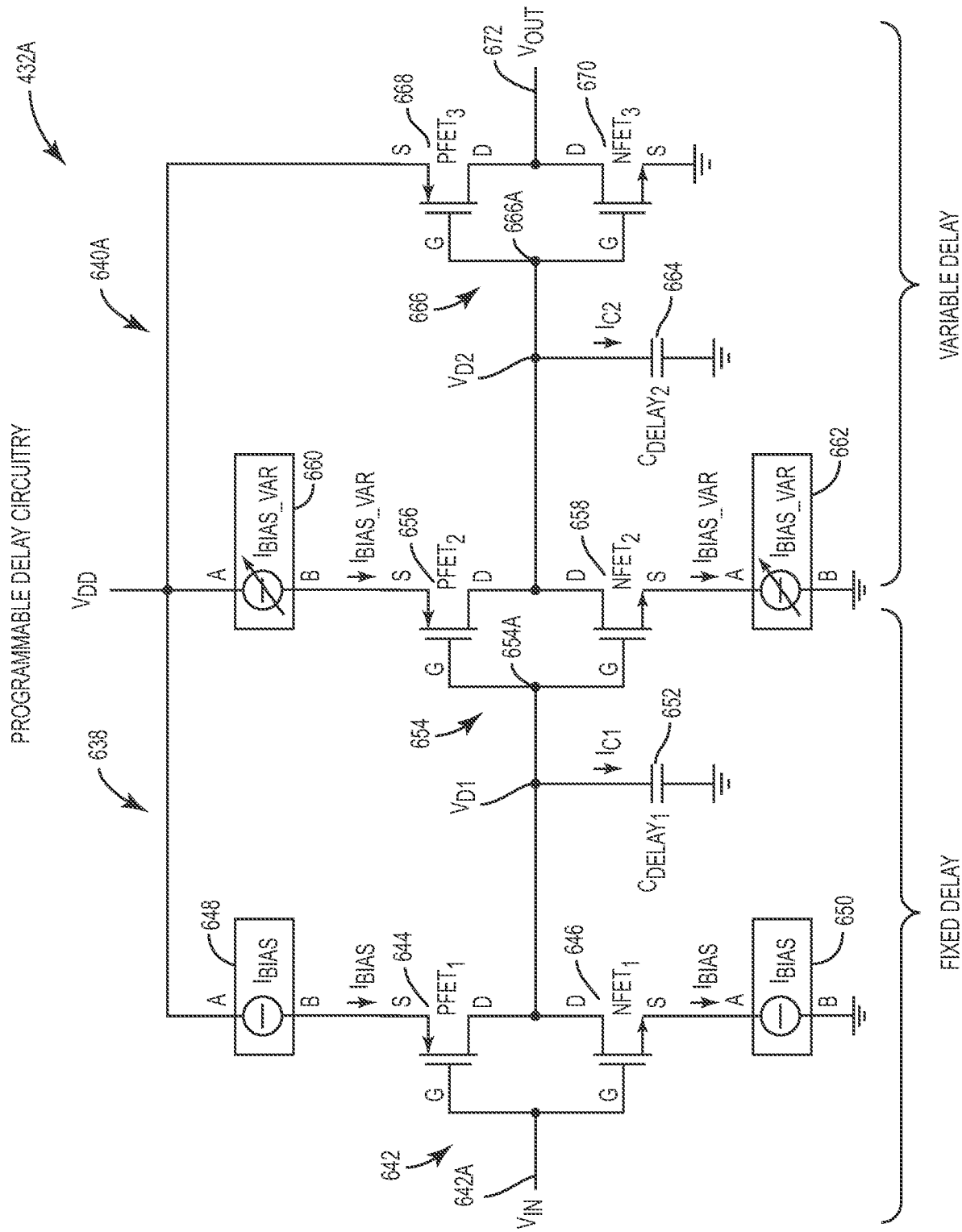

PROGRAMMABLE DELAY CIRCUITRY
432A
640A
638
642
642A
V_{IN}
V_{DD}
V_{OUT}
672
V_{D1}
V_{D2}
654
654A
666
666A
I_{BIAS}
I_{BIAS_VAR}
I_{C1}
I_{C2}
C_{DELAY1}
C_{DELAY2}
$PFET_1$
$PFET_2$
$PFET_3$
$NFET_1$
$NFET_2$
$NFET_3$
644
646
648
650
652
656
658
660
662
664
668
670
A
B
S
D
G
VARIABLE DELAY
FIXED DELAY

FIG. 29A

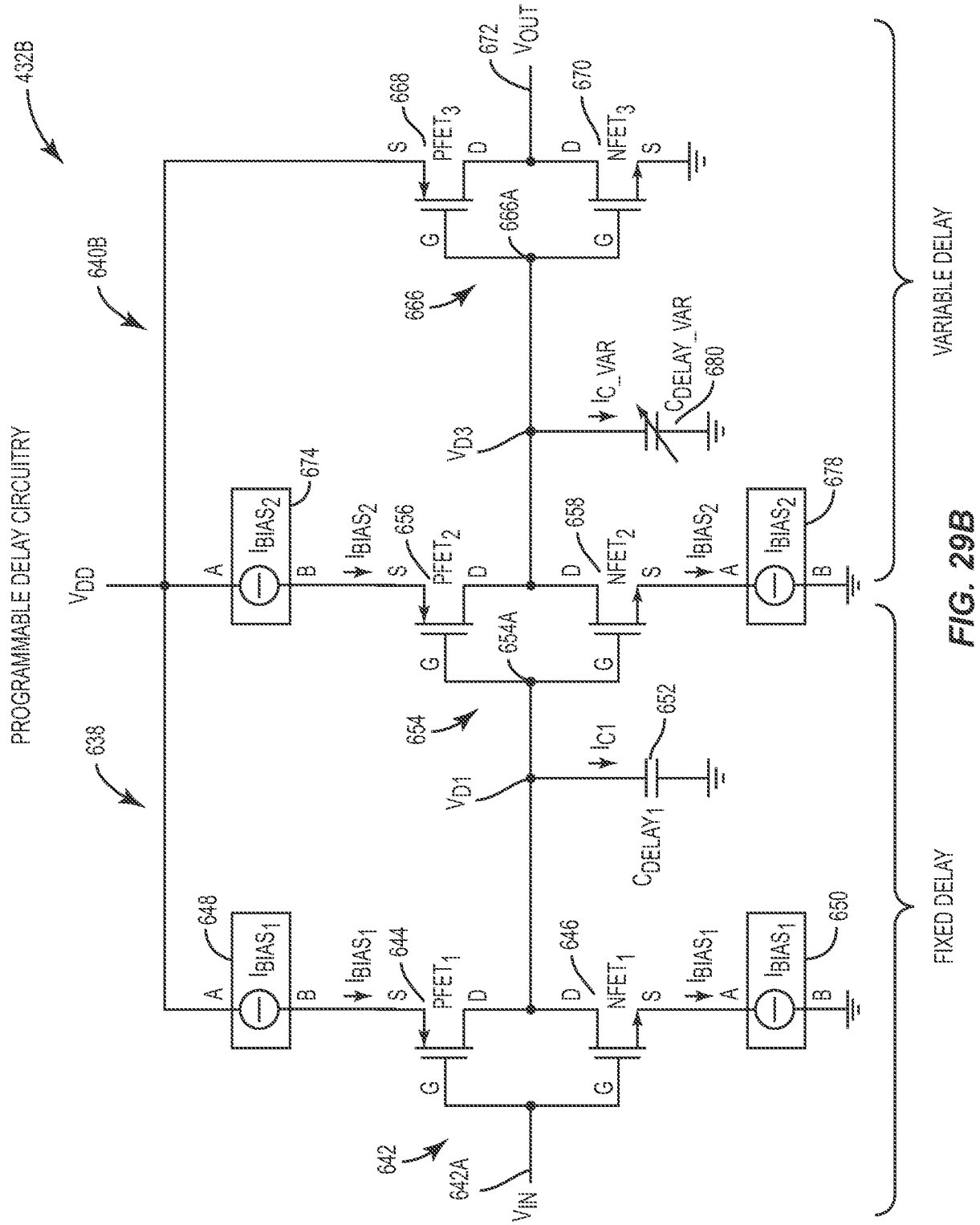

PROGRAMMABLE DELAY CIRCUITRY
432B
640B
638
VDD
VIN
642
642A
PFET1
NFET1
PFET2
NFET2
PFET3
NFET3
IBIAS1
IBIAS2
644
646
648
650
652
654
654A
656
658
666
666A
668
670
672
674
678
680
VD1
VD3
IC1
IC_VAR
CDELAY1
CDELAY_VAR
FIXED DELAY
VARIABLE DELAY

FIG. 29B

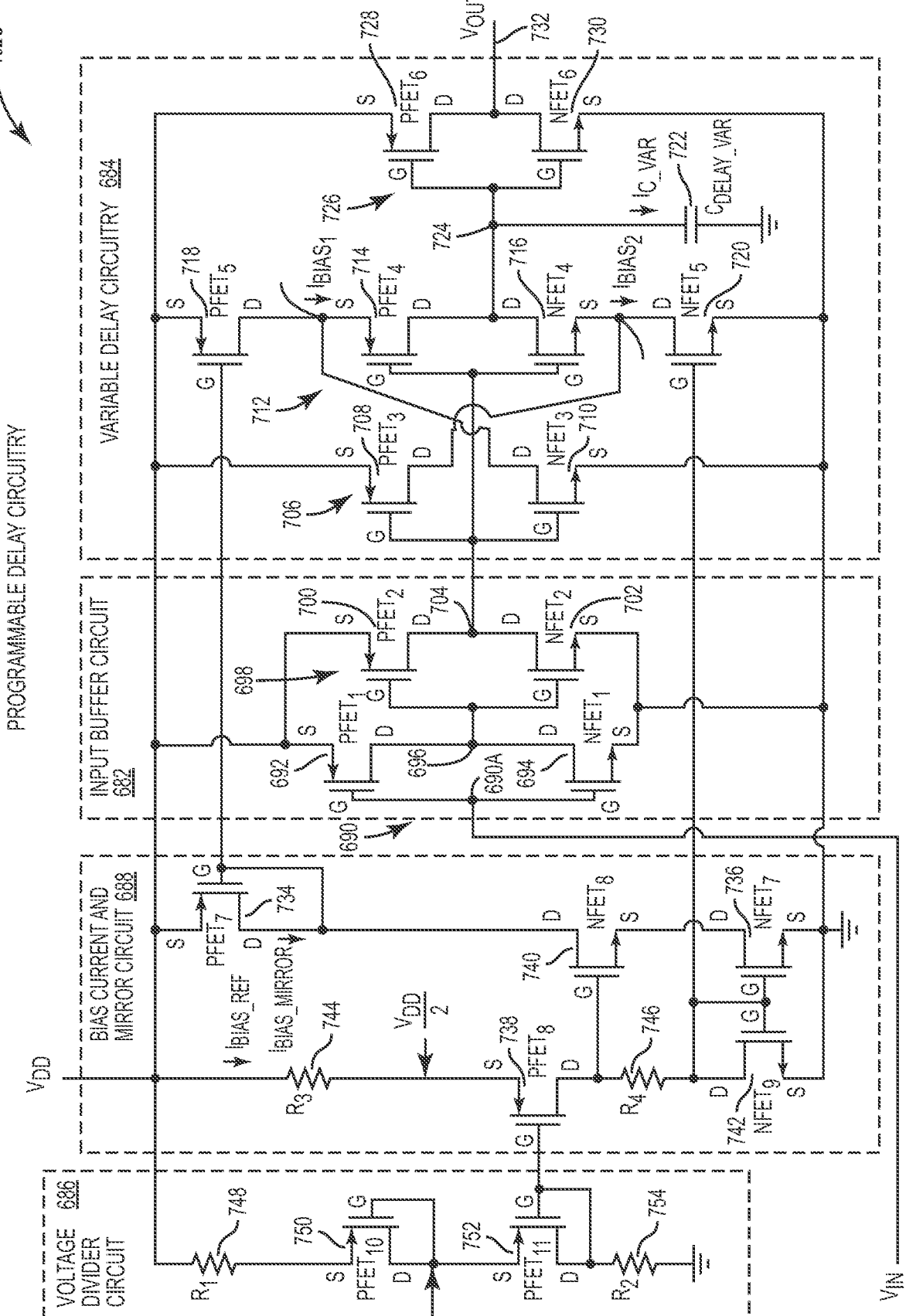

432C
PROGRAMMABLE DELAY CIRCUITRY
VOLTAGE DIVIDER CIRCUIT 686
BIAS CURRENT AND MIRROR CIRCUIT 688
INPUT BUFFER CIRCUIT 682
VARIABLE DELAY CIRCUITRY 684
VDD
VDD/2
VIN
VOUT
IBIAS_REF
IBIAS_MIRROR
IBIAS1
IBIAS2
IC_VAR
CDELAY_VAR
R1
R2
R3
R4
PFET1
PFET2
PFET3
PFET4
PFET5
PFET6
PFET7
PFET8
PFET10
PFET11
NFET1
NFET2
NFET3
NFET4
NFET5
NFET6
NFET7
NFET8
NFET9

FIG. 30A

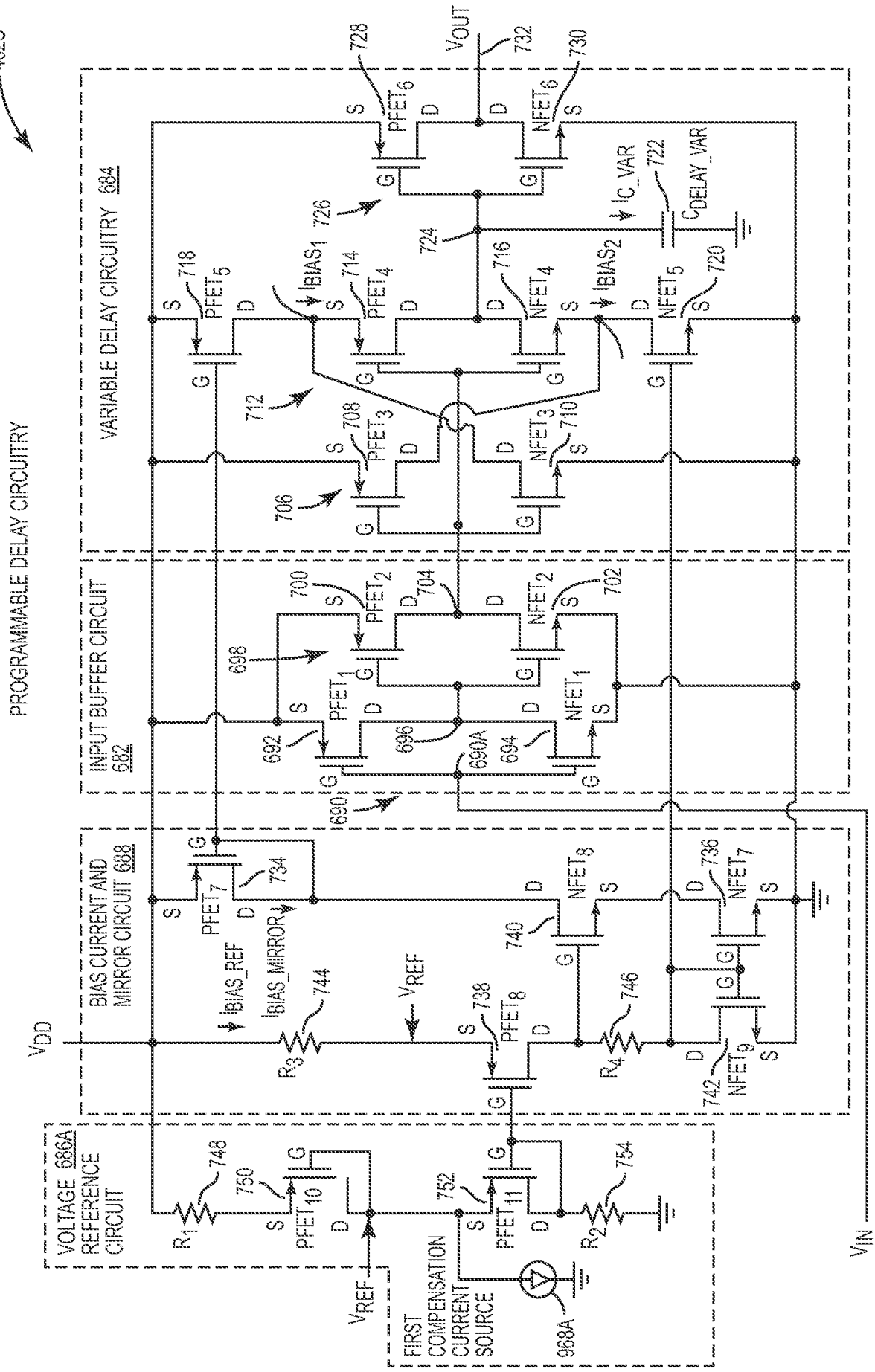

432C'
PROGRAMMABLE DELAY CIRCUITRY
VARIABLE DELAY CIRCUITRY 684
INPUT BUFFER CIRCUIT 682
BIAS CURRENT AND MIRROR CIRCUIT 688
VOLTAGE REFERENCE CIRCUIT 686A
FIRST COMPENSATION CURRENT SOURCE
VDD
VOUT
VIN
VREF
IBIAS_REF
IBIAS_MIRROR
IBIAS1
IBIAS2
IC_VAR
CDELAY_VAR
PFET1
PFET2
PFET3
PFET4
PFET5
PFET6
PFET7
PFET8
PFET10
PFET11
NFET1
NFET2
NFET3
NFET4
NFET5
NFET6
NFET7
NFET8
NFET9
R1
R2
R3
R4
692
694
696
698
700
702
704
706
708
710
712
714
716
718
720
722
724
726
728
730
732
734
736
738
740
742
744
746
748
750
752
754
968A

FIG. 30B

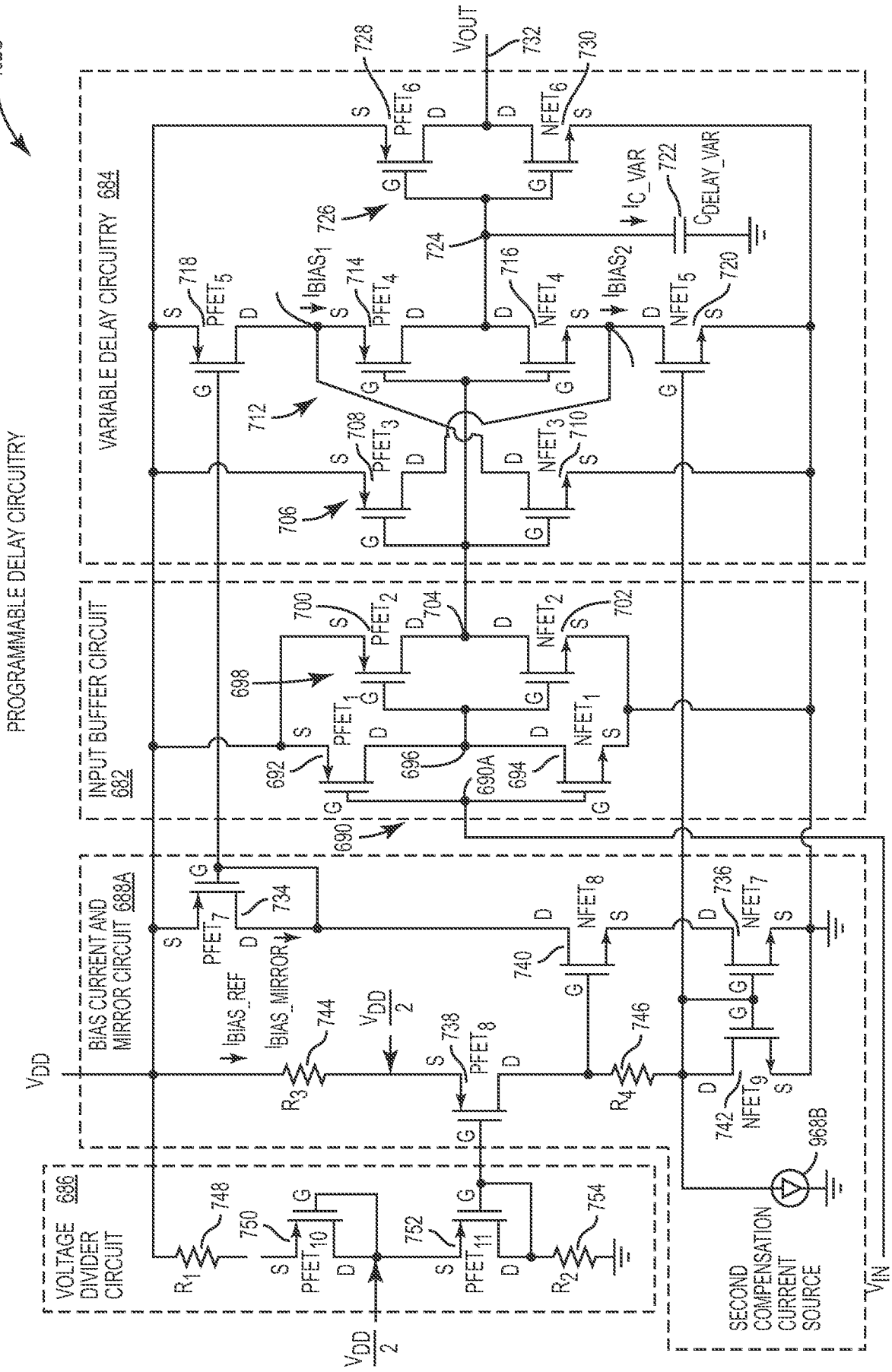

432C''
PROGRAMMABLE DELAY CIRCUITRY
VARIABLE DELAY CIRCUITRY 684
INPUT BUFFER CIRCUIT 682
BIAS CURRENT AND MIRROR CIRCUIT 688A
VOLTAGE DIVIDER CIRCUIT 686
SECOND COMPENSATION CURRENT SOURCE
VDD
VOUT
VIN
IBIAS_REF
IBIAS_MIRROR
IBIAS1
IBIAS2
IC_VAR
CDELAY_VAR
PFET1
PFET2
PFET3
PFET4
PFET5
PFET6
PFET7
PFET8
PFET10
PFET11
NFET1
NFET2
NFET3
NFET4
NFET5
NFET6
NFET7
NFET8
NFET9
R1
R2
R3
R4
692
694
696
698
700
702
704
706
708
710
712
714
716
718
720
722
724
726
728
730
732
734
736
738
740
742
744
746
748
750
752
754
690
690A
968B

FIG. 30C

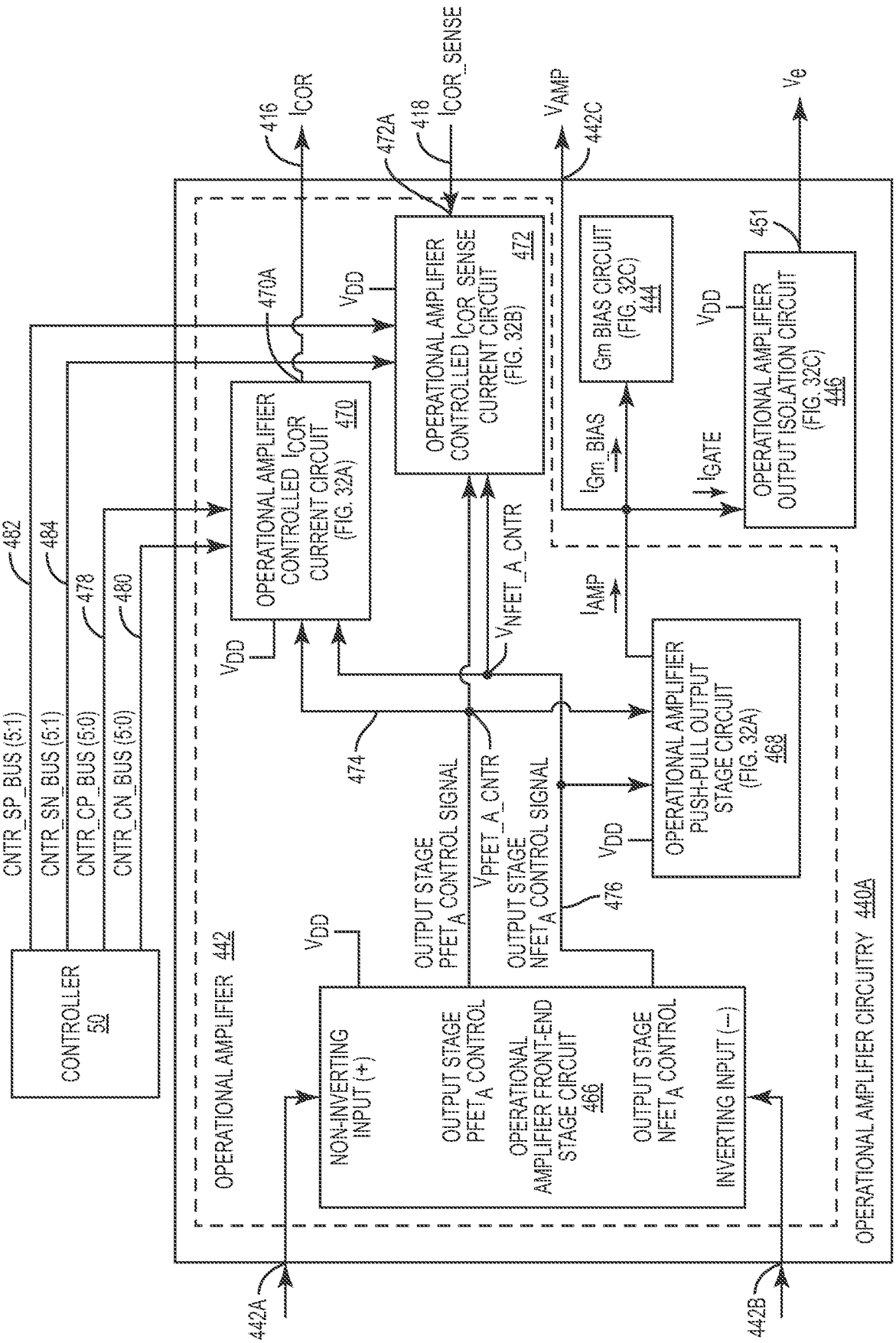

CONTROLLER 50
CNTR_SP_BUS (5:1)
CNTR_SN_BUS (5:1)
CNTR_CP_BUS (5:0)
CNTR_CN_BUS (5:0)
482
484
478
480
OPERATIONAL AMPLIFIER 442
OPERATIONAL AMPLIFIER CIRCUITRY 440A
442A
442B
NON-INVERTING INPUT (+)
INVERTING INPUT (–)
OPERATIONAL AMPLIFIER FRONT-END STAGE CIRCUIT 466
OUTPUT STAGE PFET_A CONTROL
OUTPUT STAGE NFET_A CONTROL
OUTPUT STAGE PFET_A CONTROL SIGNAL
OUTPUT STAGE NFET_A CONTROL SIGNAL
VPFET_A_CNTR
VNFET_A_CNTR
VDD
474
476
OPERATIONAL AMPLIFIER CONTROLLED ICOR CURRENT CIRCUIT (FIG. 32A) 470
470A
OPERATIONAL AMPLIFIER CONTROLLED ICOR_SENSE CURRENT CIRCUIT (FIG. 32B) 472
472A
OPERATIONAL AMPLIFIER PUSH-PULL OUTPUT STAGE CIRCUIT (FIG. 32A) 468
IAMP
Gm BIAS CIRCUIT (FIG. 32C) 444
IGm_BIAS
IGATE
OPERATIONAL AMPLIFIER OUTPUT ISOLATION CIRCUIT (FIG. 32C) 446
451
416 ICOR
418 ICOR_SENSE
VAMP 442C
Ve

FIG. 31A

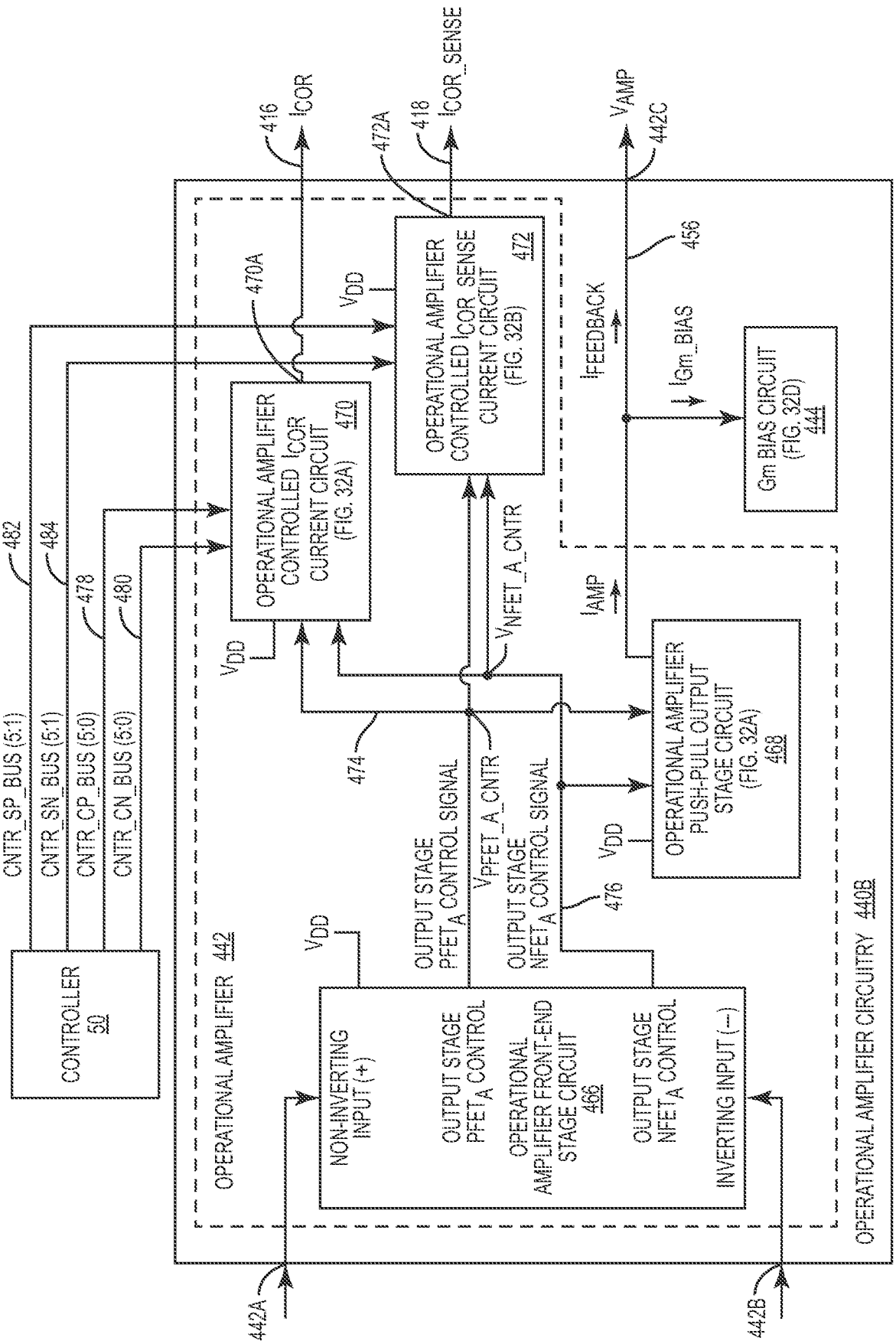

CONTROLLER 50
CNTR_SP_BUS (5:1)
CNTR_SN_BUS (5:1)
CNTR_CP_BUS (5:0)
CNTR_CN_BUS (5:0)
482
484
478
480
OPERATIONAL AMPLIFIER 442
OPERATIONAL AMPLIFIER CIRCUITRY 440B
NON-INVERTING INPUT (+)
INVERTING INPUT (–)
OUTPUT STAGE PFET_A CONTROL
OUTPUT STAGE NFET_A CONTROL
OPERATIONAL AMPLIFIER FRONT-END STAGE CIRCUIT 466
OUTPUT STAGE PFET_A CONTROL SIGNAL
OUTPUT STAGE NFET_A CONTROL SIGNAL
474
476
VDD
VPFET_A_CNTR
VNFET_A_CNTR
IAMP
OPERATIONAL AMPLIFIER PUSH-PULL OUTPUT STAGE CIRCUIT (FIG. 32A) 468
OPERATIONAL AMPLIFIER CONTROLLED ICOR CURRENT CIRCUIT (FIG. 32A) 470
470A
OPERATIONAL AMPLIFIER CONTROLLED ICOR_SENSE CURRENT CIRCUIT (FIG. 32B) 472
472A
416
ICOR
418
ICOR_SENSE
VAMP
442C
456
IFEEDBACK
IGm_BIAS
Gm BIAS CIRCUIT (FIG. 32D) 444
442A
442B

FIG. 31B

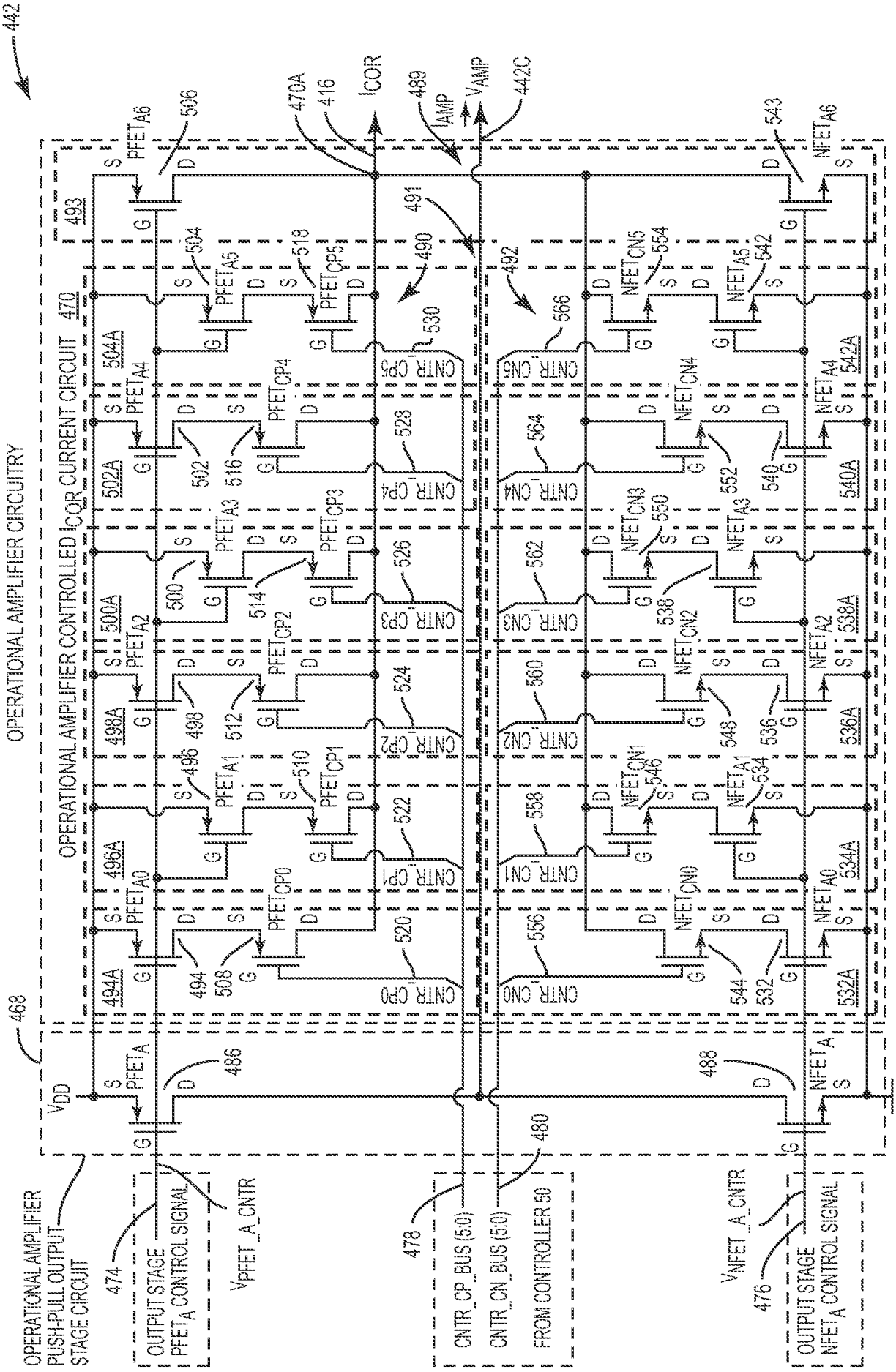

442
OPERATIONAL AMPLIFIER CIRCUITRY
OPERATIONAL AMPLIFIER CONTROLLED ICOR CURRENT CIRCUIT 470
468
VDD
PFETA
PFETA6
PFETA5
PFETA4
PFETA3
PFETA2
PFETA1
PFETA0
PFETCP0
PFETCP1
PFETCP2
PFETCP3
PFETCP4
PFETCP5
NFETA
NFETA6
NFETA5
NFETA4
NFETA3
NFETA2
NFETA1
NFETA0
NFETCN0
NFETCN1
NFETCN2
NFETCN3
NFETCN4
NFETCN5
CNTR_CP0
CNTR_CP1
CNTR_CP2
CNTR_CP3
CNTR_CP4
CNTR_CP5
CNTR_CN0
CNTR_CN1
CNTR_CN2
CNTR_CN3
CNTR_CN4
CNTR_CN5
ICOR
IAMP
VAMP
OPERATIONAL AMPLIFIER PUSH-PULL OUTPUT STAGE CIRCUIT
OUTPUT STAGE PFETA CONTROL SIGNAL
VPFET_A_CNTR
CNTR_CP_BUS (5:0)
CNTR_CN_BUS (5:0)
FROM CONTROLLER 50
VNFET_A_CNTR
OUTPUT STAGE NFETA CONTROL SIGNAL

FIG. 32A

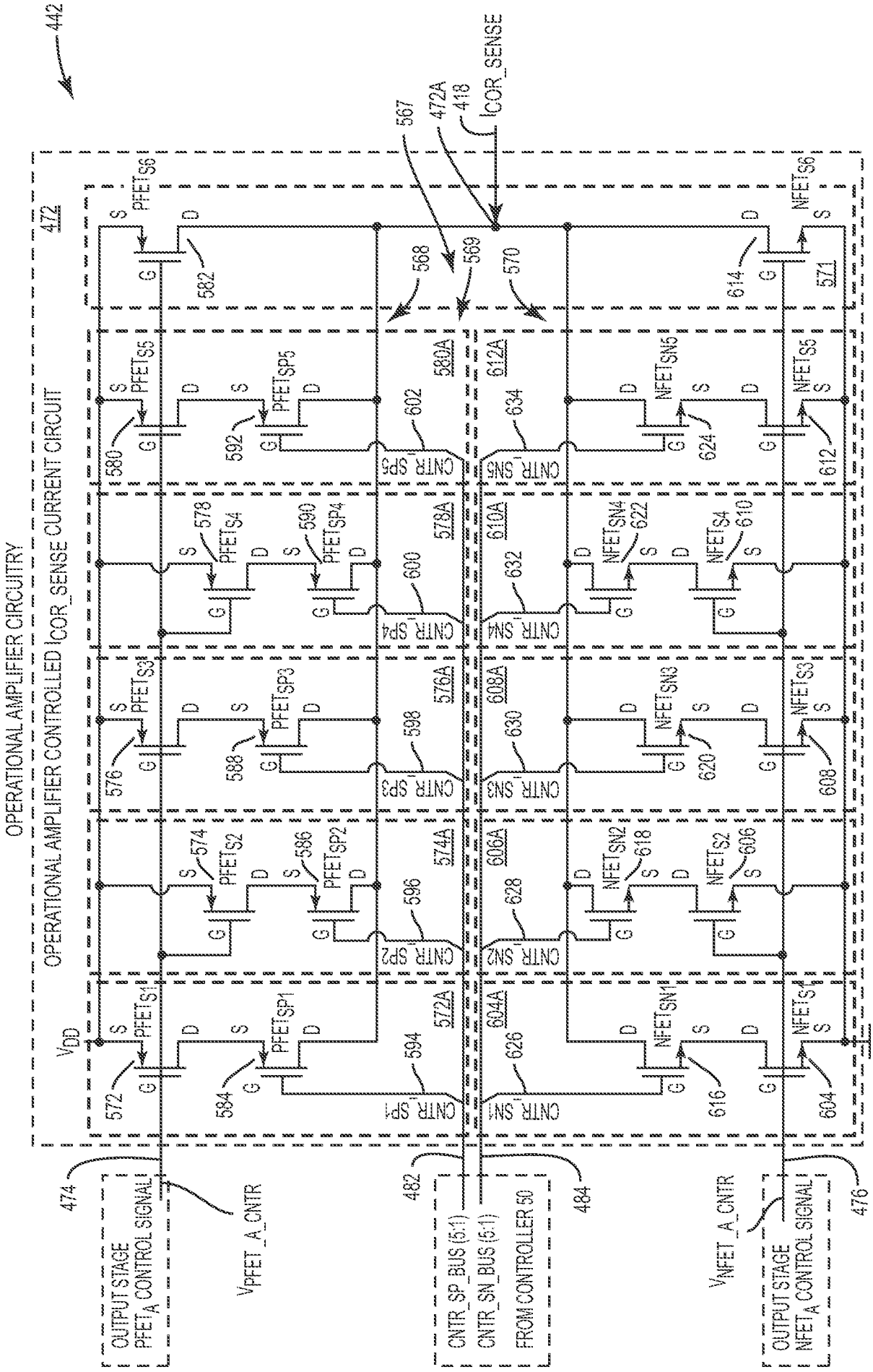

442
OPERATIONAL AMPLIFIER CIRCUITRY
OPERATIONAL AMPLIFIER CONTROLLED ICOR_SENSE CURRENT CIRCUIT
472
ICOR_SENSE
472A
418
567
568
569
570
VDD
PFETS1
PFETSP1
PFETS2
PFETSP2
PFETS3
PFETSP3
PFETS4
PFETSP4
PFETS5
PFETSP5
PFETS6
NFETSN1
NFETS2
NFETSN2
NFETS3
NFETSN3
NFETS4
NFETSN4
NFETS5
NFETSN5
NFETS6
572
574
576
578
580
582
584
586
588
590
592
594
596
598
600
602
604
606
608
610
612
614
616
618
620
622
624
626
628
630
632
634
572A
574A
576A
578A
580A
604A
606A
608A
610A
612A
CNTR_SP1
CNTR_SP2
CNTR_SP3
CNTR_SP4
CNTR_SP5
CNTR_SN1
CNTR_SN2
CNTR_SN3
CNTR_SN4
CNTR_SN5
571
474
OUTPUT STAGE
PFETA CONTROL SIGNAL
VPFET_A_CNTR
482
CNTR_SP_BUS (5:1)
CNTR_SN_BUS (5:1)
FROM CONTROLLER 50
484
VNFET_A_CNTR
476
OUTPUT STAGE
NFETA CONTROL SIGNAL

FIG. 32B

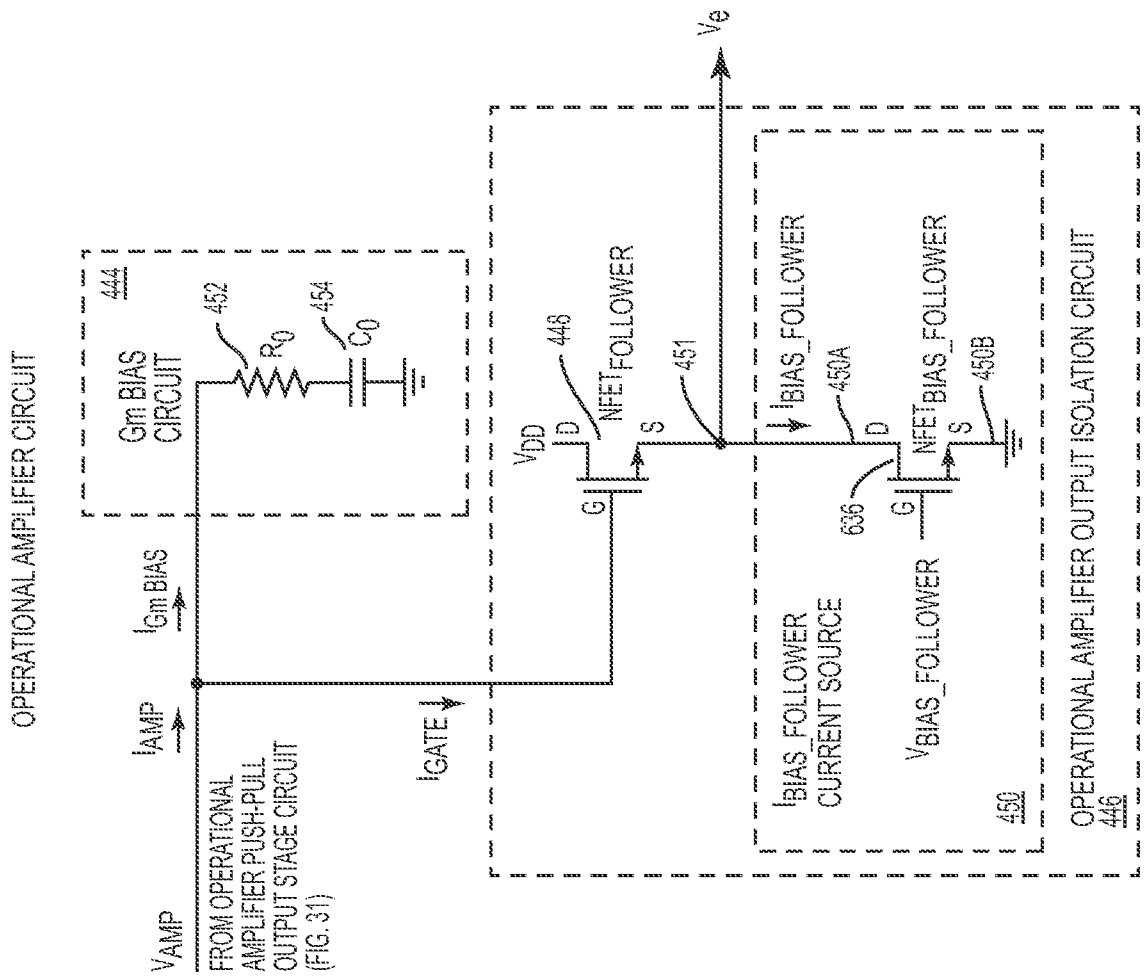

OPERATIONAL AMPLIFIER CIRCUIT
VAMP
IAMP
IGm BIAS
FROM OPERATIONAL AMPLIFIER PUSH-PULL OUTPUT STAGE CIRCUIT (FIG. 31)
444
Gm BIAS CIRCUIT
452
R0
454
C0
IGATE
VDD
D
G
S
448
NFET FOLLOWER
451
Ve
IBIAS_FOLLOWER
450A
D
636
G
NFET BIAS_FOLLOWER
S
450B
IBIAS_FOLLOWER CURRENT SOURCE
VBIAS_FOLLOWER
460
OPERATIONAL AMPLIFIER OUTPUT ISOLATION CIRCUIT
446

FIG. 32C

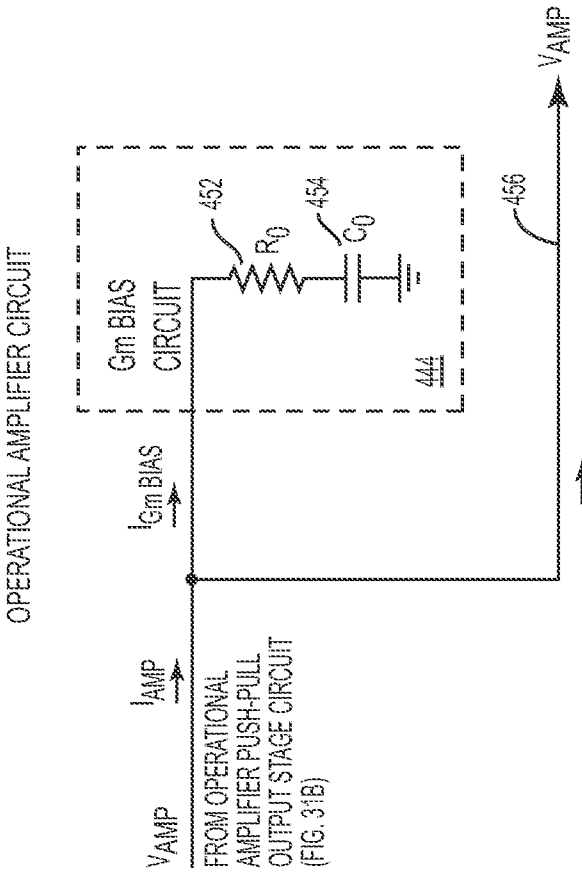

OPERATIONAL AMPLIFIER CIRCUIT
Gm BIAS CIRCUIT
$I_{Gm\ BIAS}$
I_{AMP}
V_{AMP}
FROM OPERATIONAL AMPLIFIER PUSH-PULL OUTPUT STAGE CIRCUIT (FIG. 31B)
452
R_0
454
C_0
444
456
V_{AMP}
$I_{FEEDBACK}$

FIG. 32D

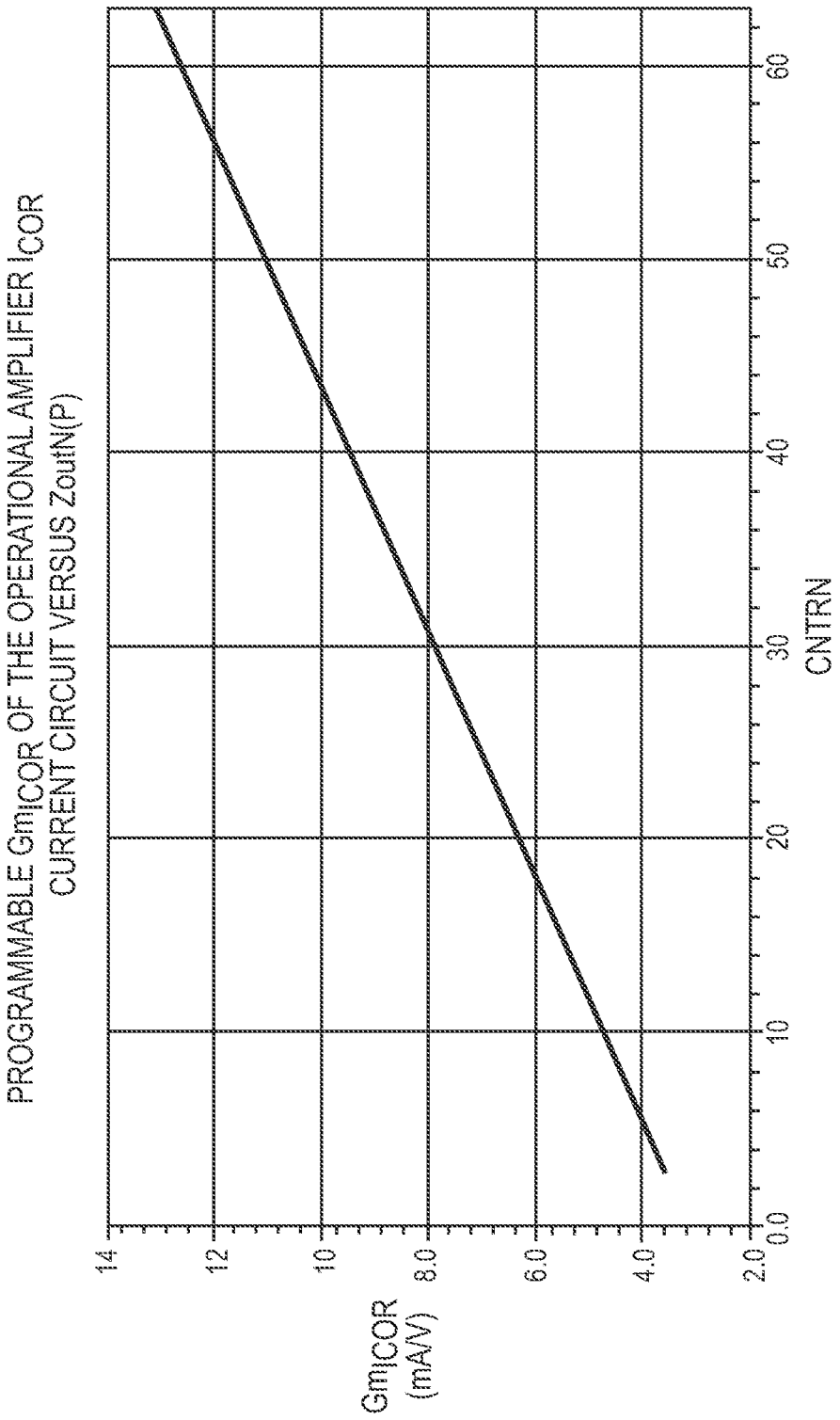

PROGRAMMABLE GmICOR OF THE OPERATIONAL AMPLIFIER ICOR
CURRENT CIRCUIT VERSUS ZoutN(P)
GmICOR (mA/V)
14
12
10
8.0
6.0
4.0
2.0
0.0
10
20
30
40
50
60
CNTRN

FIG. 33

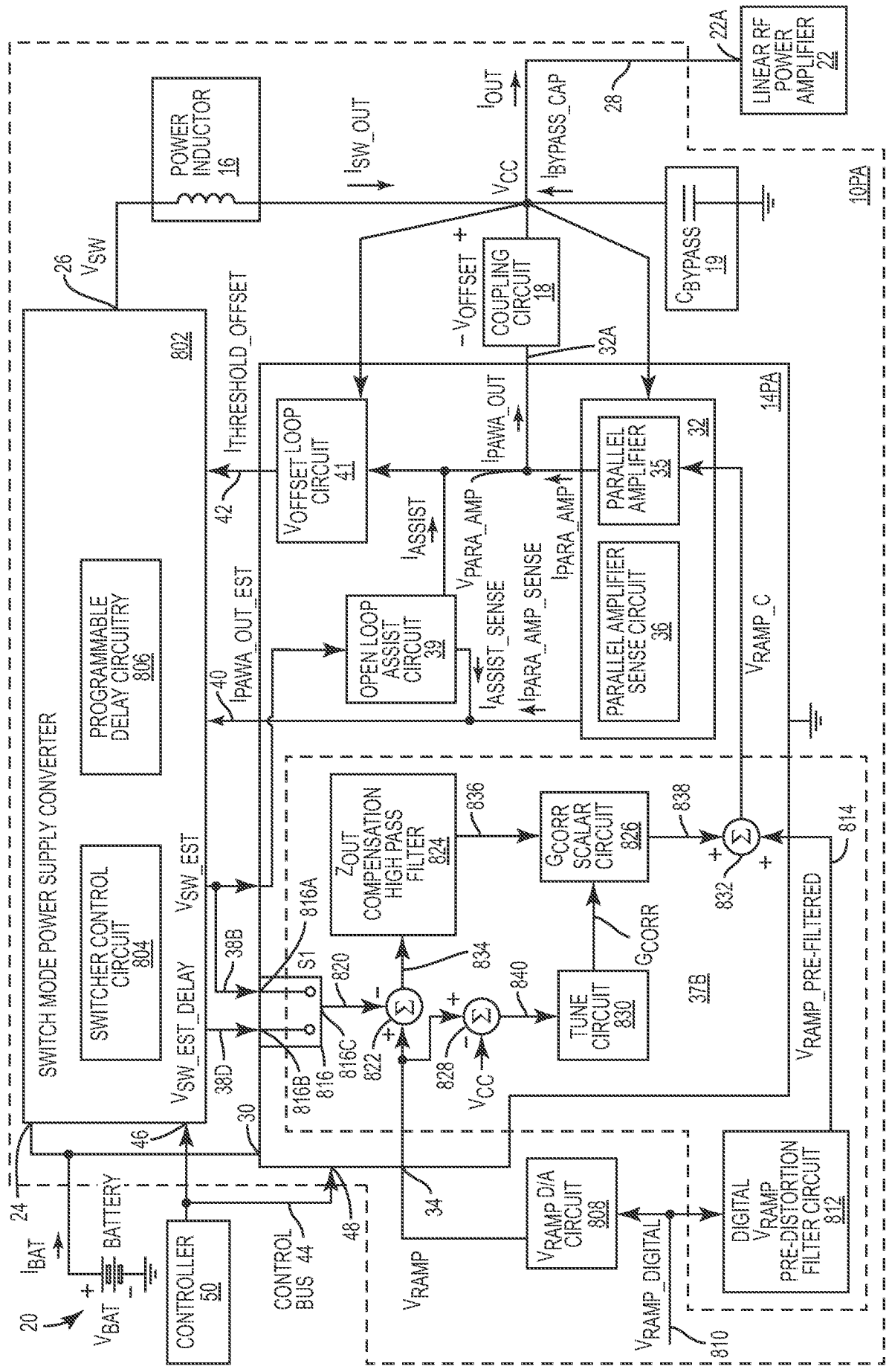

SWITCH MODE POWER SUPPLY CONVERTER
802
SWITCHER CONTROL CIRCUIT 804
PROGRAMMABLE DELAY CIRCUITRY 806
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
COUPLING CIRCUIT 18
CBYPASS 19
VOFFSET LOOP CIRCUIT 41
OPEN LOOP ASSIST CIRCUIT 39
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
14PA
10PA
ZOUT COMPENSATION HIGH PASS FILTER 824
GCORR SCALAR CIRCUIT 826
TUNE CIRCUIT 830
37B
VRAMP D/A CIRCUIT 808
DIGITAL VRAMP PRE-DISTORTION FILTER CIRCUIT 812
CONTROLLER 50
BATTERY
CONTROL BUS 44
VBAT
IBAT
VSW
VSW_EST
VSW_EST_DELAY
ISW_OUT
IOUT
VCC
IBYPASS_CAP
VOFFSET
ITHRESHOLD_OFFSET
IPAWA_OUT
IPAWA_OUT_EST
IASSIST
VPARA_AMP
IASSIST_SENSE
IPARA_AMP_SENSE
VRAMP_C
VRAMP_PRE-FILTERED
VRAMP_DIGITAL
VRAMP
GCORR
S1
816A
816B
816C
816
820
822
828
834
836
838
840
832
814
810
20
22A
24
26
28
30
32
32A
34
38B
38D
40
42
46
48

FIG. 34A

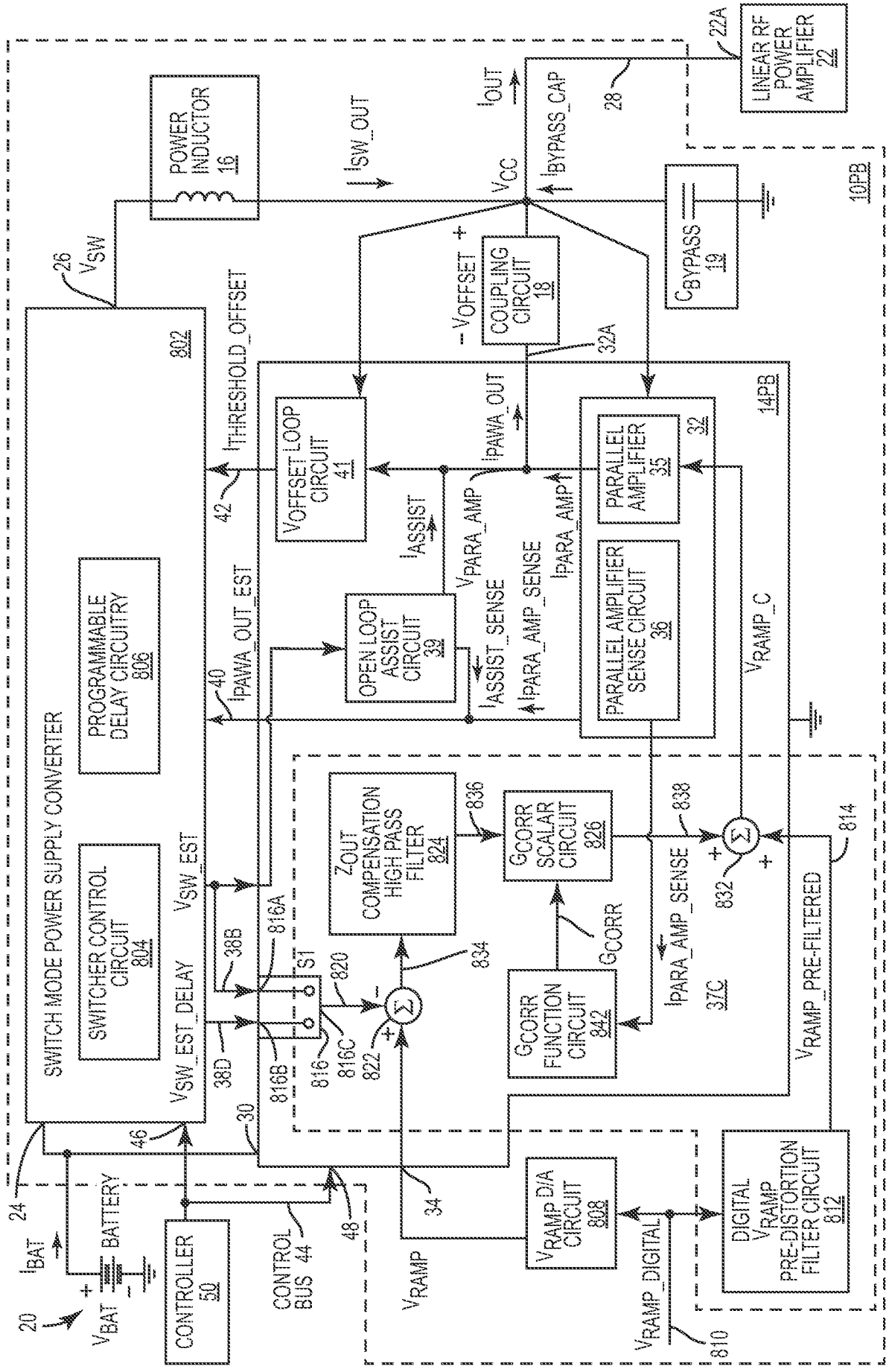

SWITCH MODE POWER SUPPLY CONVERTER
802
SWITCHER CONTROL CIRCUIT 804
PROGRAMMABLE DELAY CIRCUITRY 806
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
22A
28
10PB
14PB
BATTERY
CONTROLLER 50
CONTROL BUS 44
VRAMP D/A CIRCUIT 808
DIGITAL VRAMP PRE-DISTORTION FILTER CIRCUIT 812
VOFFSET LOOP CIRCUIT 41
OPEN LOOP ASSIST CIRCUIT 39
COUPLING CIRCUIT 18
CBYPASS 19
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
ZOUT COMPENSATION HIGH PASS FILTER 824
GCORR SCALAR CIRCUIT 826
GCORR FUNCTION CIRCUIT 842
VBAT
IBAT
VSW
VSW_EST
VSW_EST_DELAY
ITHRESHOLD_OFFSET
IPAWA_OUT_EST
IPAWA_OUT
IASSIST
VPARA_AMP
IASSIST_SENSE
IPARA_AMP_SENSE
IPARA_AMP
VRAMP_C
VRAMP_PRE-FILTERED
VRAMP_DIGITAL
VRAMP
ISW_OUT
IOUT
IBYPASS_CAP
VCC
VOFFSET
GCORR
IPARA_AMP_SENSE
S1
816
816A
816B
816C
820
822
834
836
838
832
814
810
20
24
26
30
32A
34
37C
38B
38D
40
42
46
48

FIG. 34B

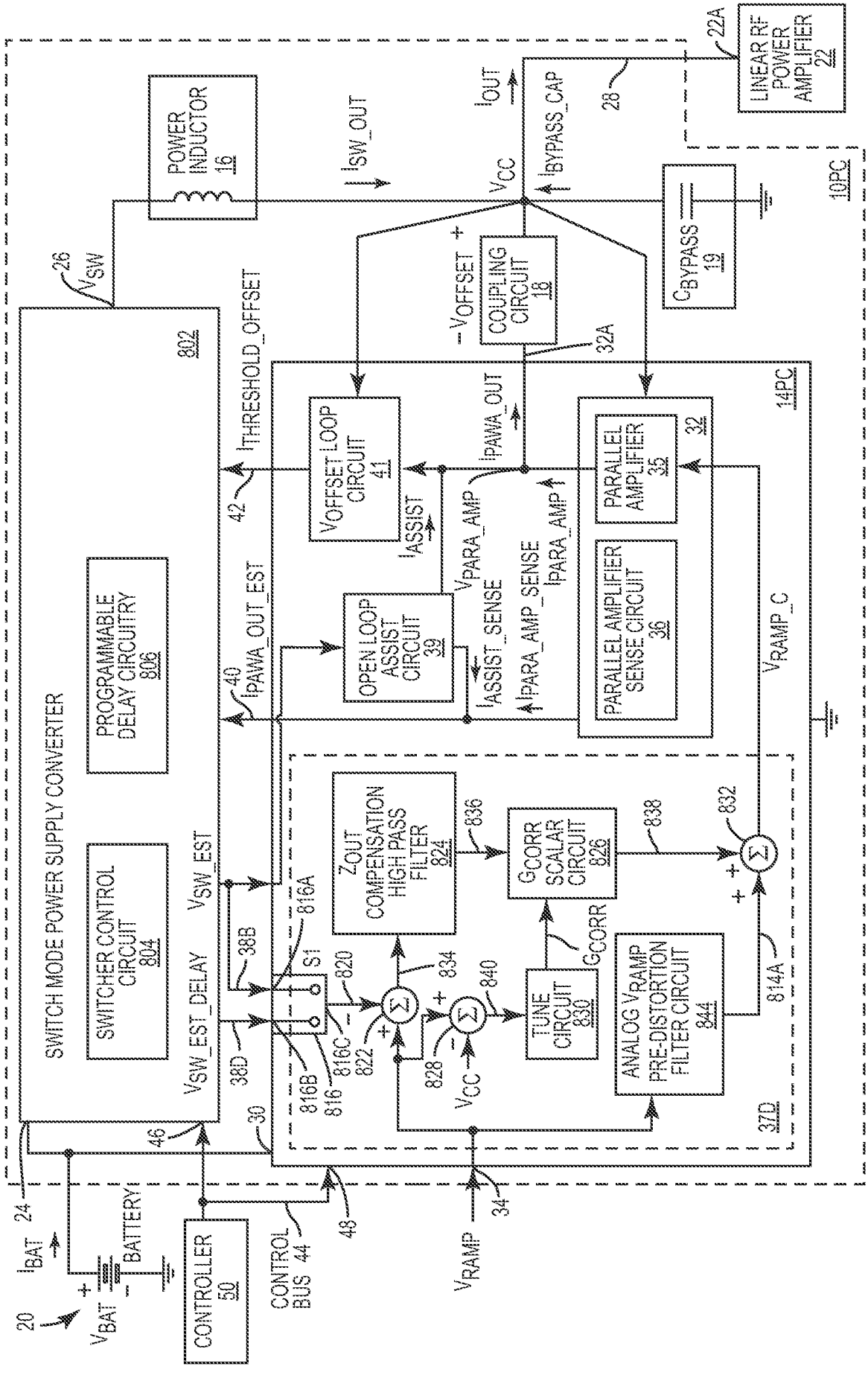

SWITCH MODE POWER SUPPLY CONVERTER
802
SWITCHER CONTROL CIRCUIT 804
PROGRAMMABLE DELAY CIRCUITRY 806
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
COUPLING CIRCUIT 18
CBYPASS 19
VOFFSET LOOP CIRCUIT 41
OPEN LOOP ASSIST CIRCUIT 39
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
ZOUT COMPENSATION HIGH PASS FILTER 824
GCORR SCALAR CIRCUIT 826
TUNE CIRCUIT 830
ANALOG VRAMP PRE-DISTORTION FILTER CIRCUIT 844
CONTROLLER 50
BATTERY
CONTROL BUS 44
VSW
VSW_EST
VSW_EST_DELAY
VRAMP
VRAMP_C
ISW_OUT
IOUT
VCC
IBYPASS_CAP
VOFFSET
ITHRESHOLD_OFFSET
IPAWA_OUT_EST
IPAWA_OUT
IASSIST
IASSIST_SENSE
VPARA_AMP
IPARA_AMP_SENSE
IPARA_AMP
IBAT
VBAT
S1
10PC
14PC
32A
37D

FIG. 34C

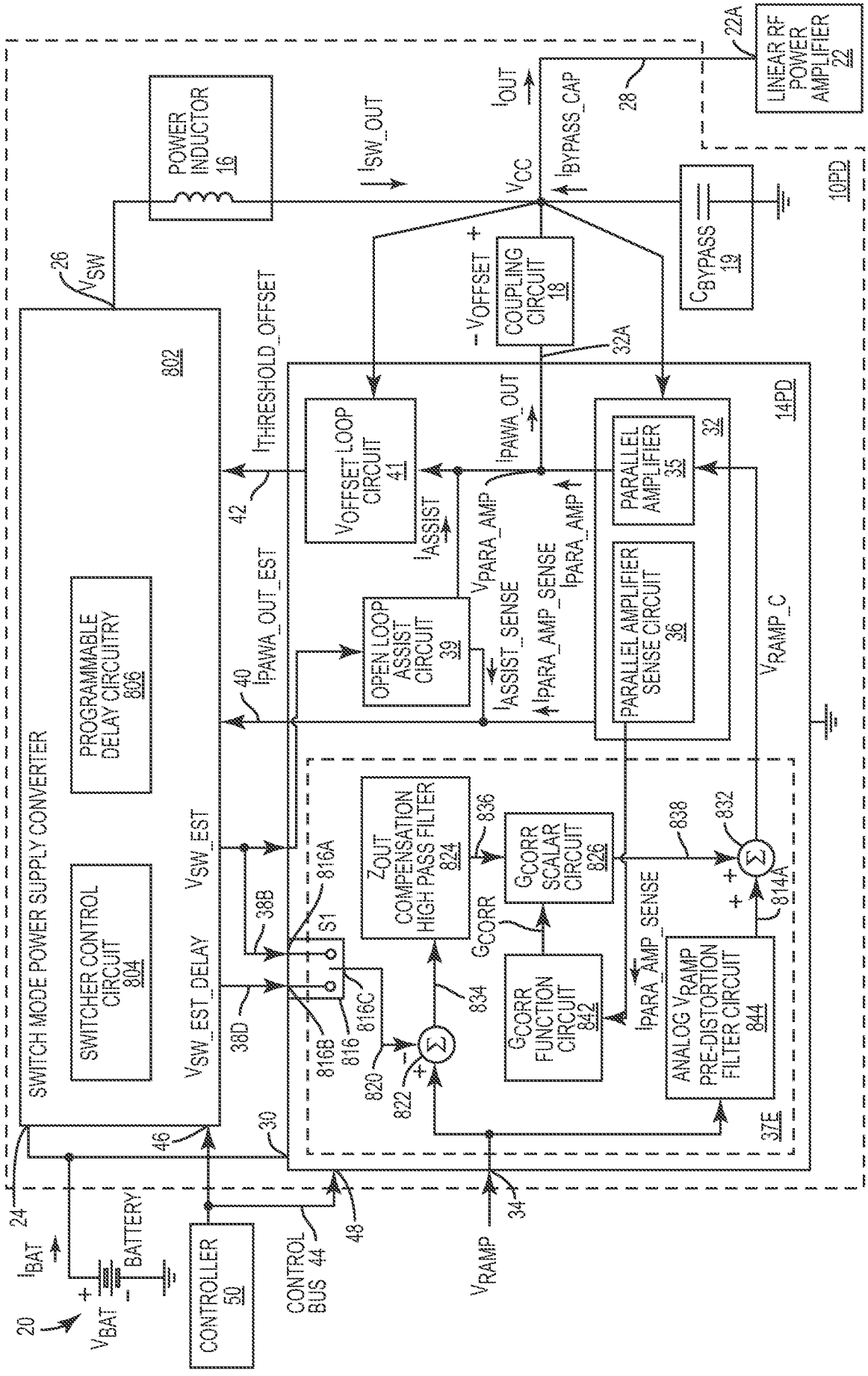

SWITCH MODE POWER SUPPLY CONVERTER
802
PROGRAMMABLE DELAY CIRCUITRY 806
SWITCHER CONTROL CIRCUIT 804
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
COUPLING CIRCUIT 18
CBYPASS 19
VOFFSET LOOP CIRCUIT 41
OPEN LOOP ASSIST CIRCUIT 39
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
ZOUT COMPENSATION HIGH PASS FILTER 824
GCORR SCALAR CIRCUIT 826
GCORR FUNCTION CIRCUIT 842
ANALOG VRAMP PRE-DISTORTION FILTER CIRCUIT 844
CONTROLLER 50
BATTERY
CONTROL BUS 44
VBAT
IBAT
VSW
ISW_OUT
IOUT
VCC
IBYPASS_CAP
VOFFSET
ITHRESHOLD_OFFSET
IPAWA_OUT_EST
IPAWA_OUT
IASSIST
VPARA_AMP
IASSIST_SENSE
IPARA_AMP_SENSE
IPARA_AMP
VRAMP_C
VSW_EST
VSW_EST_DELAY
VRAMP
GCORR
IPARA_AMP_SENSE
S1
816A
816B
816C
816
820
822
834
836
838
832
814A
38B
38D
40
42
46
48
30
34
24
20
22A
28
32A
32
37E
14PD
10PD

FIG. 34D

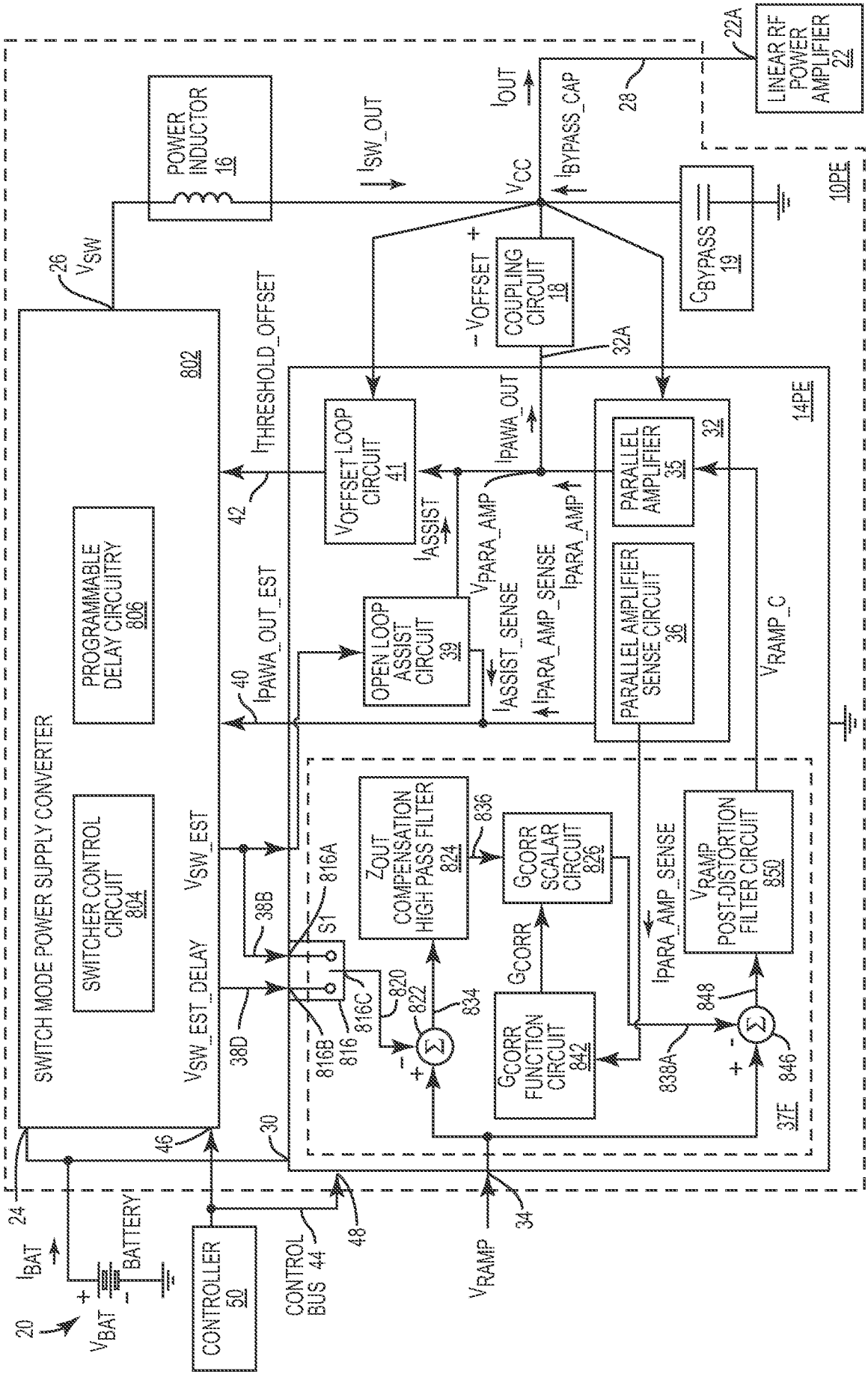

SWITCH MODE POWER SUPPLY CONVERTER
802
PROGRAMMABLE DELAY CIRCUITRY 806
SWITCHER CONTROL CIRCUIT 804
POWER INDUCTOR 16
LINEAR RF POWER AMPLIFIER 22
COUPLING CIRCUIT 18
CBYPASS 19
OFFSET LOOP CIRCUIT 41
OPEN LOOP ASSIST CIRCUIT 39
PARALLEL AMPLIFIER 35
PARALLEL AMPLIFIER SENSE CIRCUIT 36
ZOUT COMPENSATION HIGH PASS FILTER 824
GCORR SCALAR CIRCUIT 826
GCORR FUNCTION CIRCUIT 842
VRAMP POST-DISTORTION FILTER CIRCUIT 850
CONTROLLER 50
BATTERY
CONTROL BUS 44
VBAT
IBAT
VSW
VSW_EST
VSW_EST_DELAY
ISW_OUT
IOUT
VCC
IBYPASS_CAP
VOFFSET
ITHRESHOLD_OFFSET
IPAWA_OUT
IPAWA_OUT_EST
IASSIST
IASSIST_SENSE
VPARA_AMP
IPARA_AMP_SENSE
VRAMP_C
VRAMP
GCORR
IPARA_AMP_SENSE
S1
816A
816B
816C
816
820
822
834
836
838A
848
846
37E
14PE
10PE
20
24
26
28
30
32
32A
34
38B
38D
40
42
46
48
22A

FIG. 34E

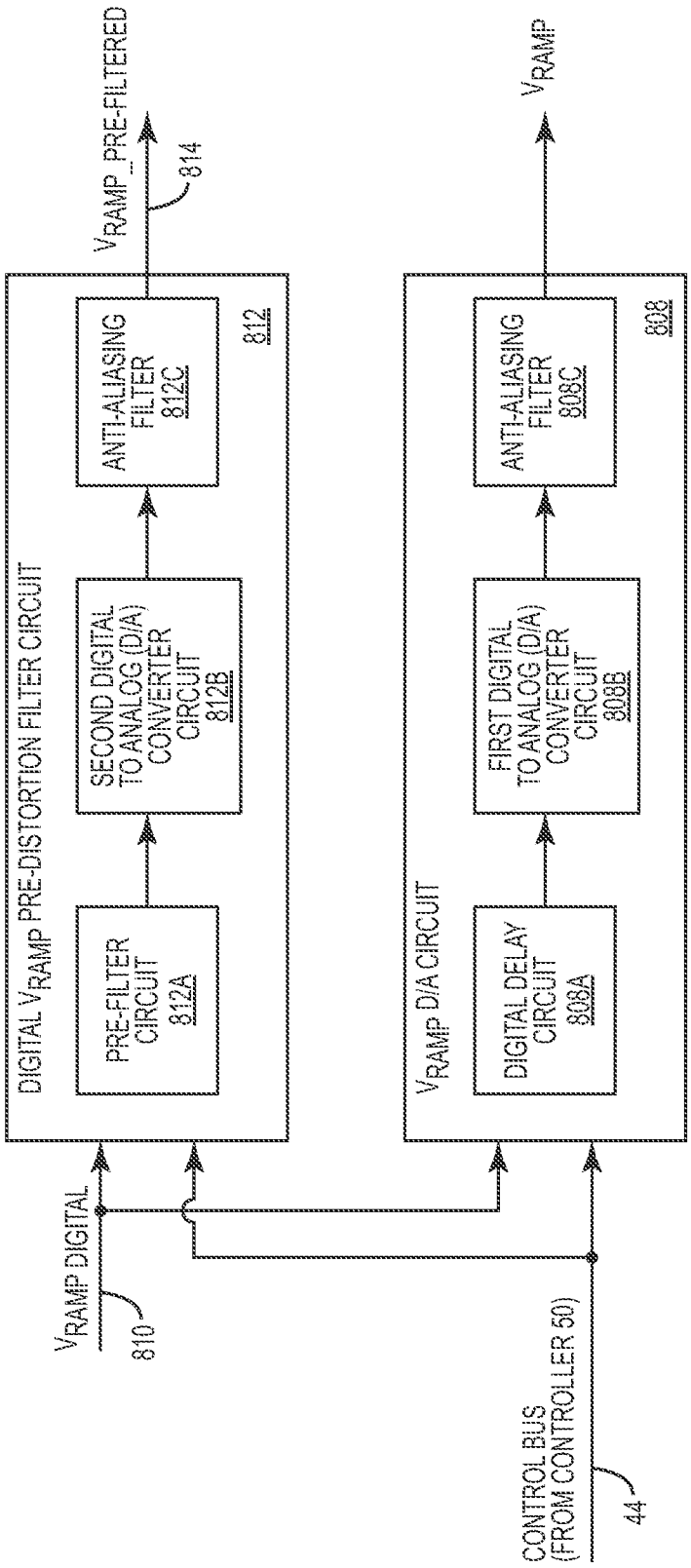

DIGITAL VRAMP PRE-DISTORTION FILTER CIRCUIT
PRE-FILTER CIRCUIT 812A
SECOND DIGITAL TO ANALOG (D/A) CONVERTER CIRCUIT 812B
ANTI-ALIASING FILTER 812C
812
VRAMP_PRE-FILTERED
814
VRAMP D/A CIRCUIT
DIGITAL DELAY CIRCUIT 808A
FIRST DIGITAL TO ANALOG (D/A) CONVERTER CIRCUIT 808B
ANTI-ALIASING FILTER 808C
808
VRAMP
VRAMP DIGITAL
810
CONTROL BUS (FROM CONTROLLER 50)
44

FIG. 35

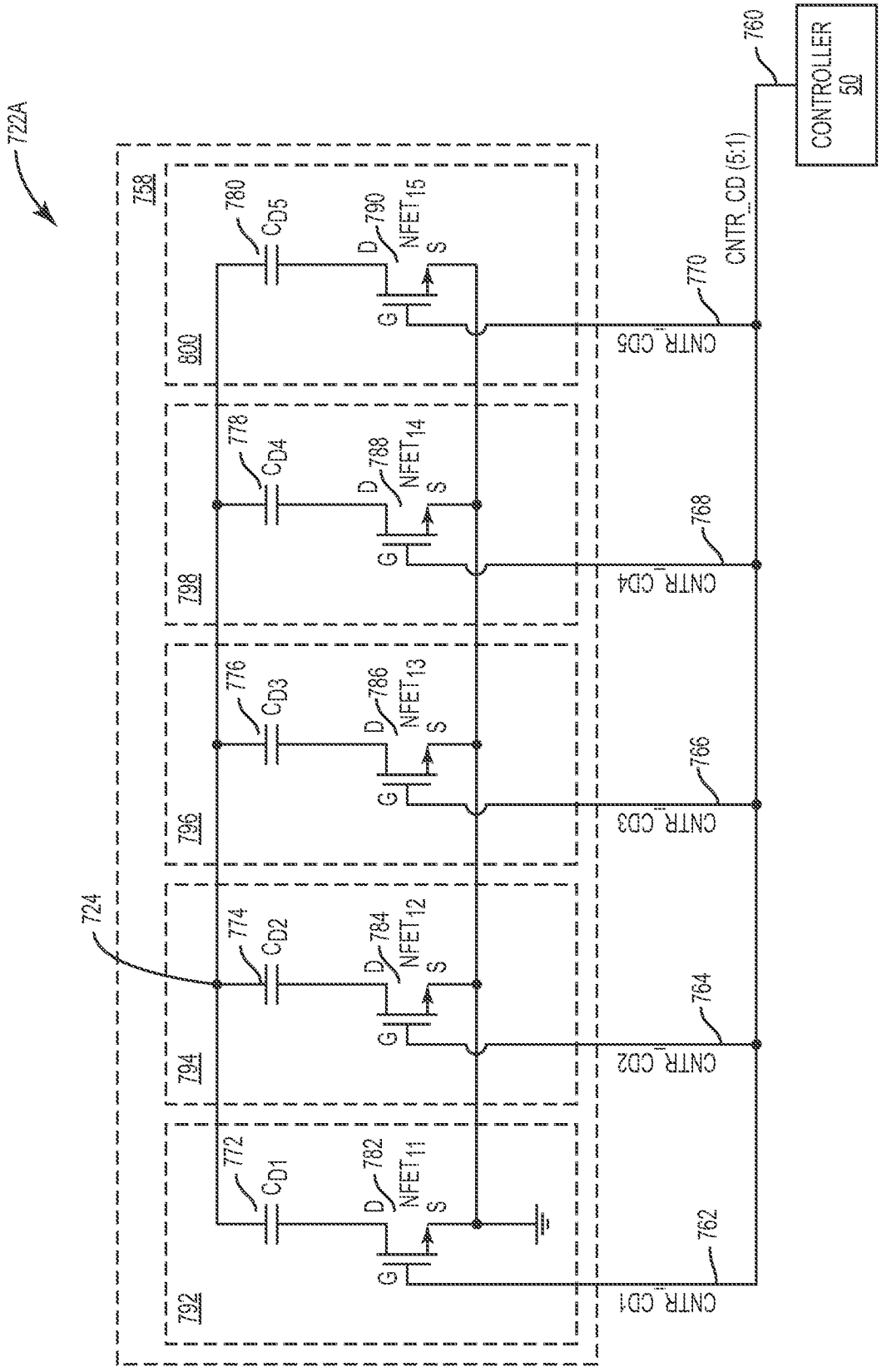

722A
724
758
792
794
796
798
800
772
774
776
778
780
782
784
786
788
790
NFET 11
NFET 12
NFET 13
NFET 14
NFET 15
C_D1
C_D2
C_D3
C_D4
C_D5
S
D
G
762
764
766
768
770
CNTR_CD1
CNTR_CD2
CNTR_CD3
CNTR_CD4
CNTR_CD5
CNTR_CD (6:1)
760
CONTROLLER 50

FIG. 36

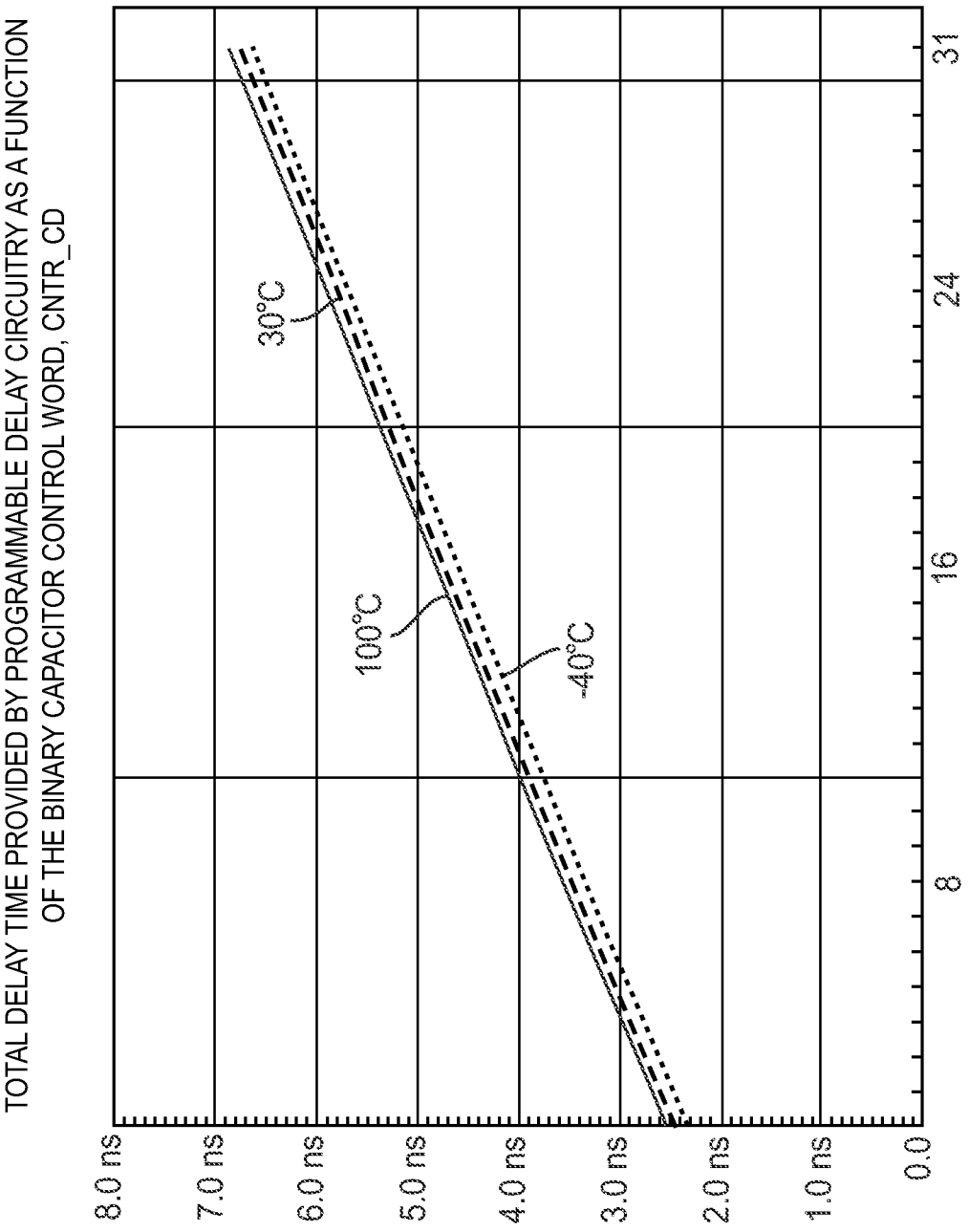

TOTAL DELAY TIME PROVIDED BY PROGRAMMABLE DELAY CIRCUITRY AS A FUNCTION OF THE BINARY CAPACITOR CONTROL WORD, CNTR_CD
8.0 ns
7.0 ns
6.0 ns
5.0 ns
4.0 ns
3.0 ns
2.0 ns
1.0 ns
0.0
30°C
100°C
-40°C
8
16
24
31
0 ≥ CNTR_CD ≥ 31

FIG. 37

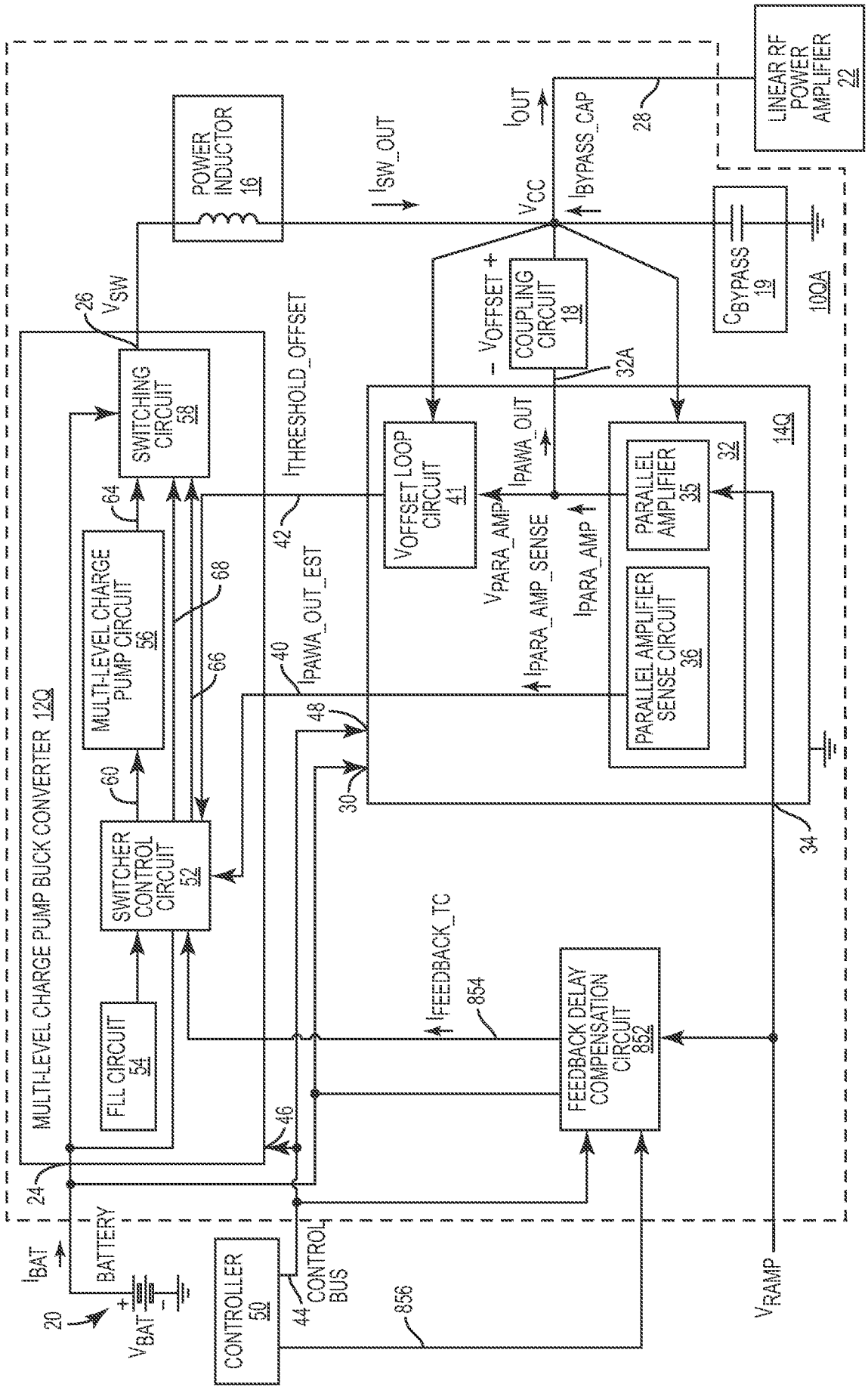

MULTI-LEVEL CHARGE PUMP BUCK CONVERTER 12Q
BATTERY
20
I_{BAT}
V_{BAT}
24
CONTROLLER 50
CONTROL BUS
44
856
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 52
60
MULTI-LEVEL CHARGE PUMP CIRCUIT 56
64
SWITCHING CIRCUIT 58
26
V_{SW}
POWER INDUCTOR 16
I_{SW_OUT}
I_{OUT}
V_{CC}
I_{BYPASS_CAP}
28
LINEAR RF POWER AMPLIFIER 22
C_{BYPASS} 19
100A
$-V_{OFFSET}+$
COUPLING CIRCUIT 18
32A
$I_{THRESHOLD_OFFSET}$
42
$I_{PAWA_OUT_EST}$
40
V_{OFFSET} LOOP CIRCUIT 41
I_{PAWA_OUT}
V_{PARA_AMP}
$I_{PARA_AMP_SENSE}$
I_{PARA_AMP}
PARALLEL AMPLIFIER SENSE CIRCUIT 36
PARALLEL AMPLIFIER 35
32
14Q
48
30
34
46
$I_{FEEDBACK_TC}$
854
FEEDBACK DELAY COMPENSATION CIRCUIT 852
V_{RAMP}
66
68

FIG. 38A

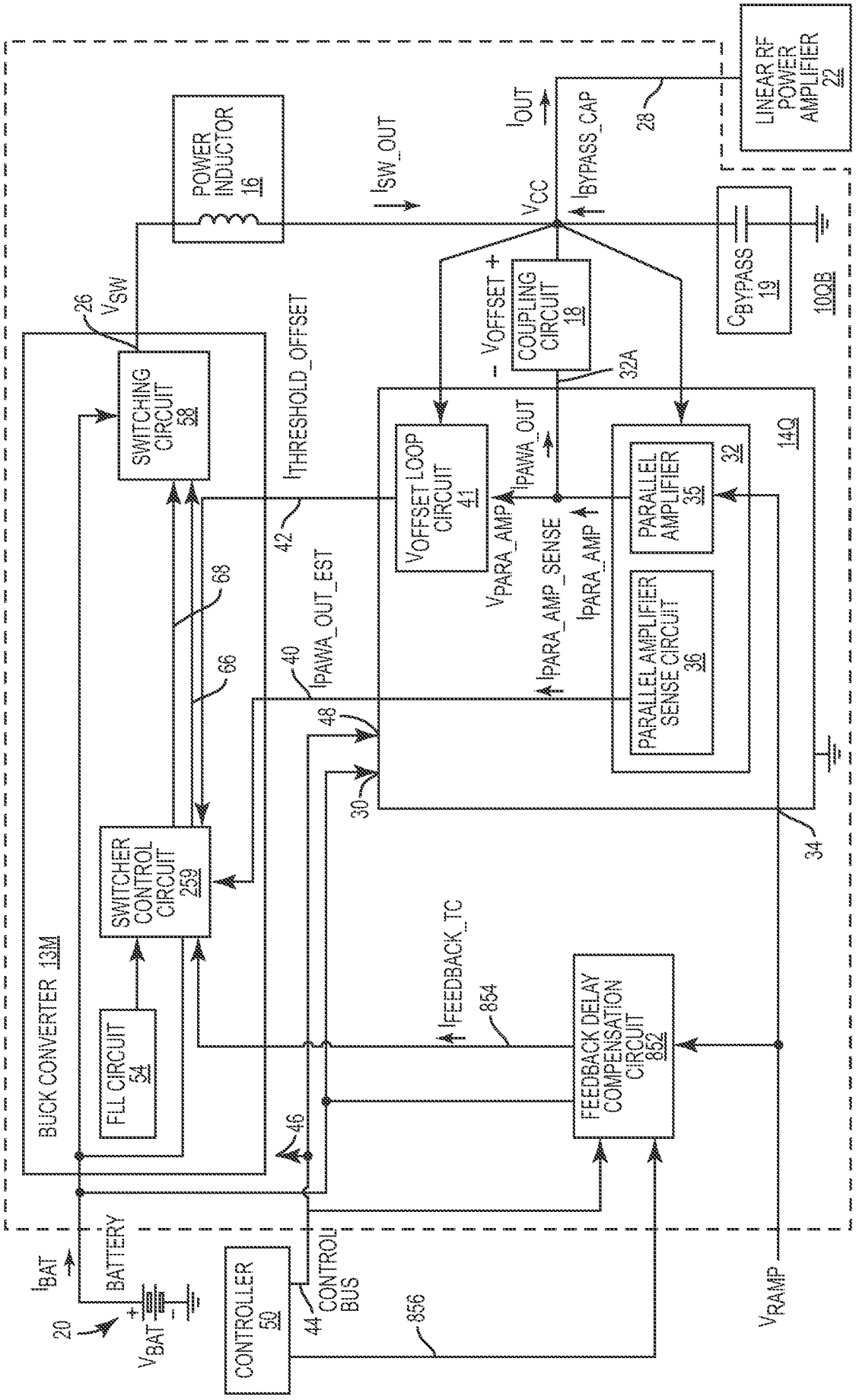

BUCK CONVERTER 13M
BATTERY
I_{BAT}
V_{BAT}
20
CONTROLLER 50
CONTROL BUS
44
856
FLL CIRCUIT 54
SWITCHER CONTROL CIRCUIT 259
SWITCHING CIRCUIT 58
26
V_{SW}
POWER INDUCTOR 16
I_{SW_OUT}
I_{OUT}
V_{CC}
I_{BYPASS_CAP}
28
LINEAR RF POWER AMPLIFIER 22
C_{BYPASS} 19
10QB
$-V_{OFFSET}+$
COUPLING CIRCUIT 18
32A
$I_{THRESHOLD_OFFSET}$
42
VOFFSET LOOP CIRCUIT 41
I_{PAWA_OUT}
V_{PARA_AMP}
$I_{PARA_AMP_SENSE}$
I_{PARA_AMP}
PARALLEL AMPLIFIER 35
32
PARALLEL AMPLIFIER SENSE CIRCUIT 36
14Q
68
66
40
$I_{PAWA_OUT_EST}$
48
30
34
46
$I_{FEEDBACK_TC}$
854
FEEDBACK DELAY COMPENSATION CIRCUIT 852
V_{RAMP}

FIG. 38B

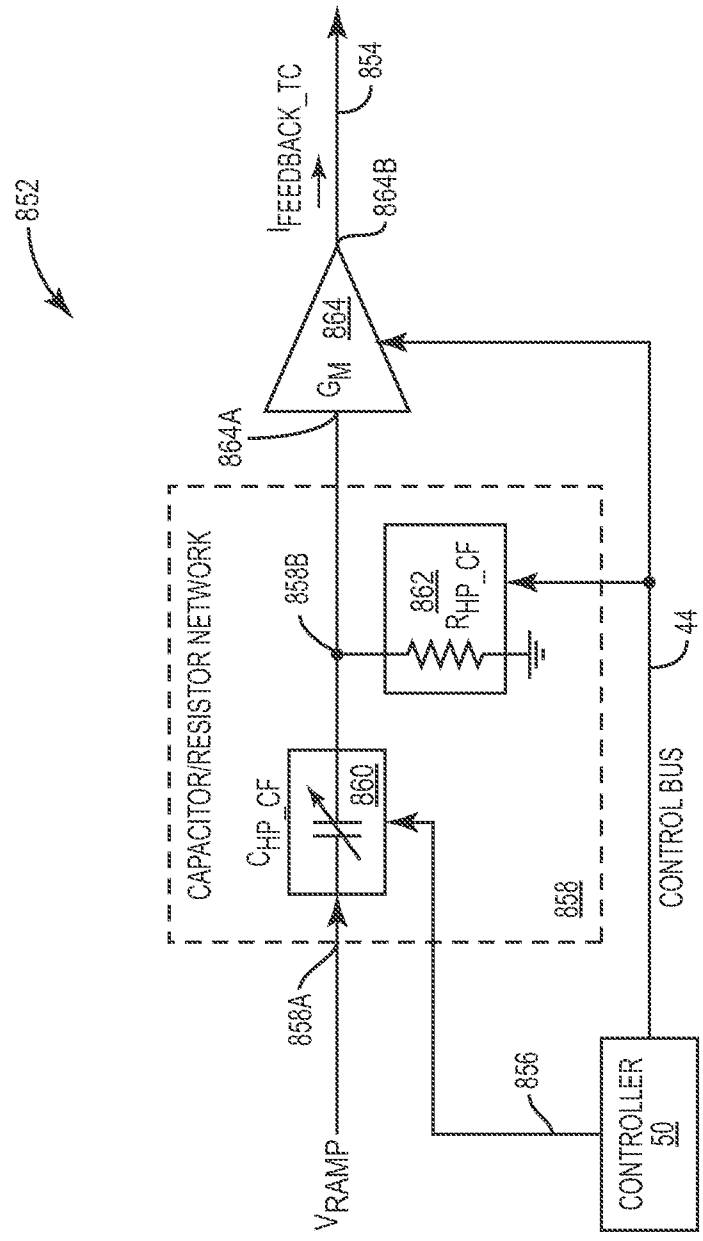

852
IFEEDBACK_TC
854
864B
GM 864
864A
CAPACITOR/RESISTOR NETWORK
853B
862
RHP_CF
CHP_CF
860
858
858A
856
CONTROL BUS
44
CONTROLLER 50
VRAMP

FIG. 39A

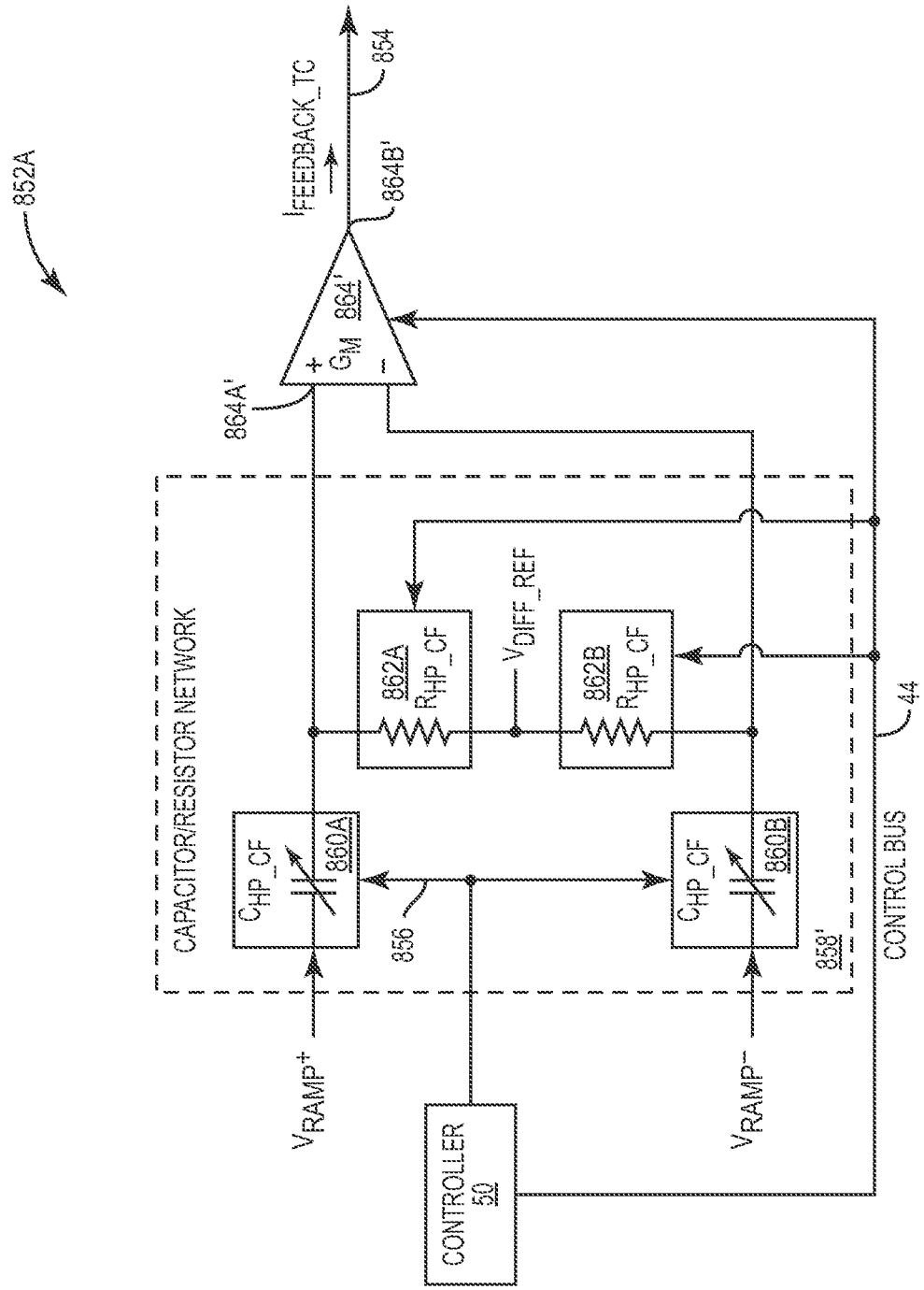

852A
IFEEDBACK_TC
864
864B'
864A'
GM 864'
CAPACITOR/RESISTOR NETWORK
862A RHP_CF
VDIFF_REF
862B RHP_CF
44
CHP_CF 860A
856
CHP_CF 860B
858'
CONTROL BUS
VRAMP+
VRAMP−
CONTROLLER 50

FIG. 39B

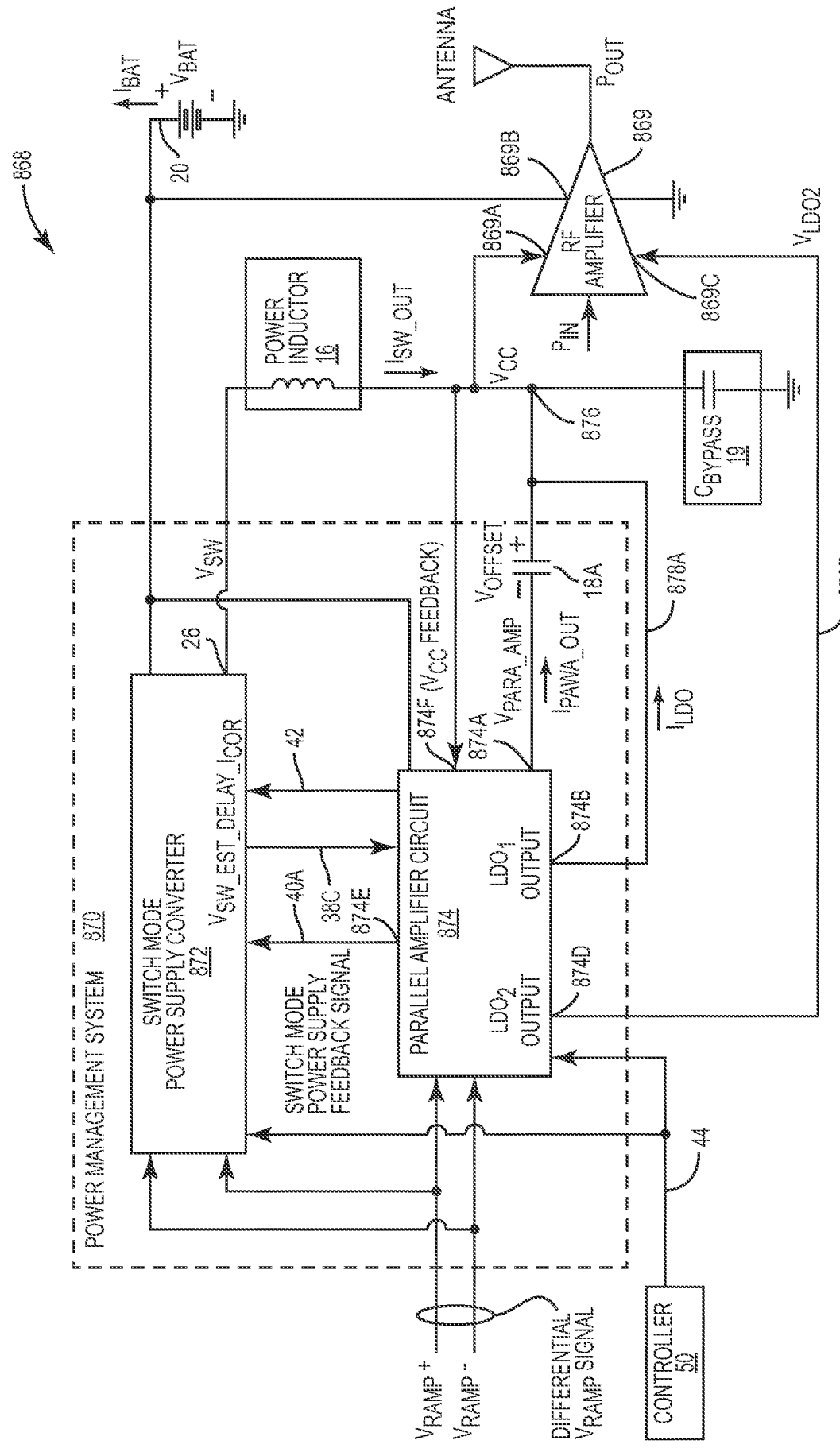

868
POWER MANAGEMENT SYSTEM 870
SWITCH MODE POWER SUPPLY CONVERTER 872
$V_{SW_EST_DELAY_ICOR}$
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL
PARALLEL AMPLIFIER CIRCUIT 874
LDO_1 OUTPUT
LDO_2 OUTPUT
V_{PARA_AMP}
I_{PAWA_OUT}
I_{LDO}
V_{OFFSET}
874F (V_{CC} FEEDBACK)
V_{SW}
I_{SW_OUT}
POWER INDUCTOR 16
I_{BAT}
V_{BAT}
20
ANTENNA
P_{OUT}
869
869B
869A
869C
RF AMPLIFIER
P_{IN}
V_{CC}
876
C_{BYPASS} 19
V_{LDO2}
878A
878D
18A
26
42
40A
38C
874E
874A
874B
874D
44
CONTROLLER 50
V_{RAMP} +
V_{RAMP} -
DIFFERENTIAL V_{RAMP} SIGNAL

FIG. 40A

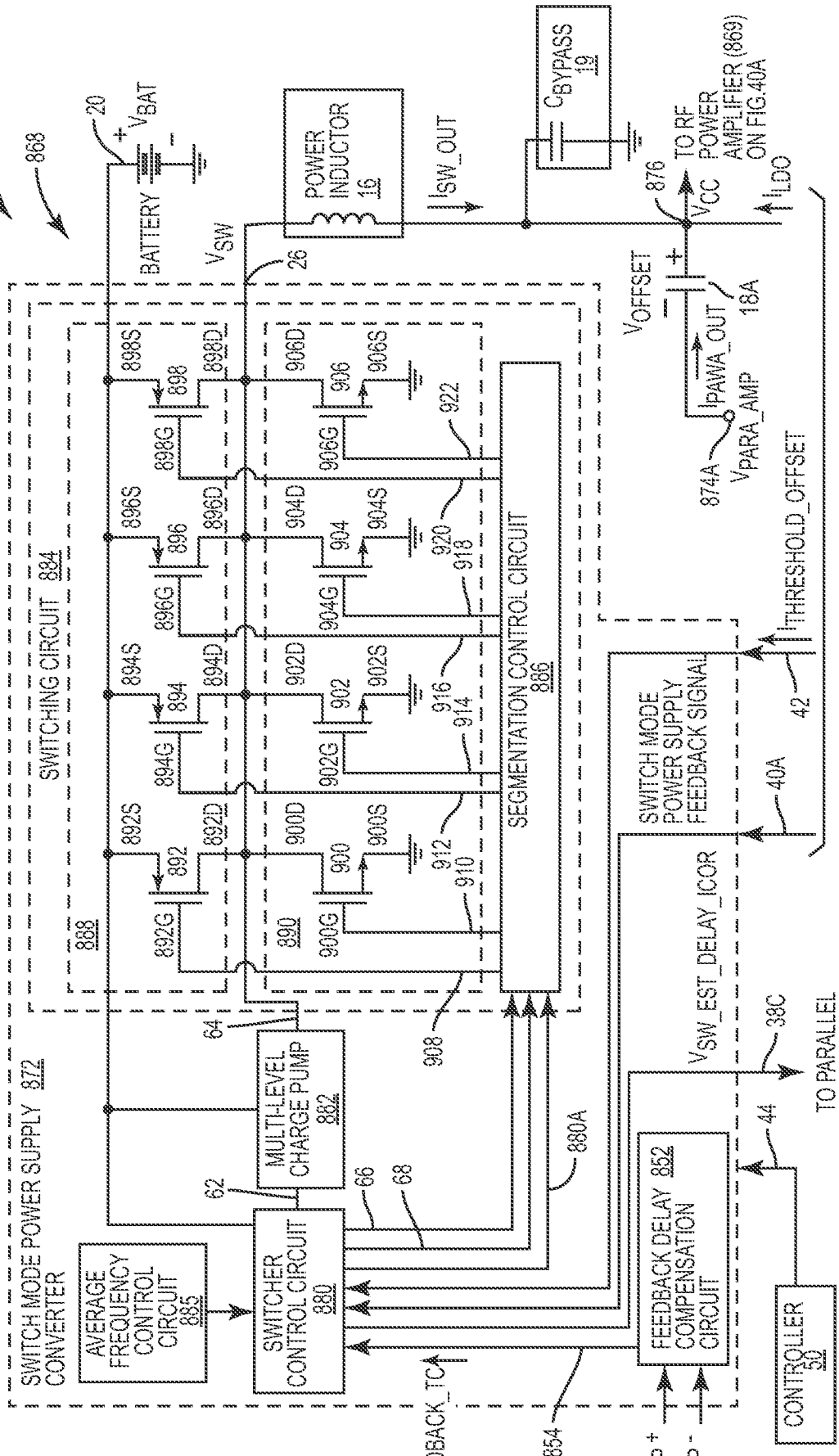

870
868
20
BATTERY
V_{BAT}
SWITCH MODE POWER SUPPLY 872
CONVERTER
SWITCHING CIRCUIT 894
888
V_{SW}
26
POWER INDUCTOR 16
I_{SW_OUT}
C_{BYPASS} 19
876
TO RF POWER AMPLIFIER (869) ON FIG.40A
I_{LDO}
V_{CC}
V_{OFFSET}
18A
I_{PAWA_OUT}
V_{PARA_AMP}
874A
$I_{THRESHOLD_OFFSET}$
FROM PARALLEL AMPLIFIER CIRCUIT
42
40A
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL
SEGMENTATION CONTROL CIRCUIT 886
892S
892
892G
892D
894S
894
894G
894D
896S
896
896G
896D
898S
898
898G
898D
900D
900
900G
900S
902D
902
902G
902S
904D
904
904G
904S
906D
906
906G
906S
908
910
912
914
916
918
920
922
MULTI-LEVEL CHARGE PUMP 882
64
62
66
68
880A
SWITCHER CONTROL CIRCUIT 880
AVERAGE FREQUENCY CONTROL CIRCUIT 885
FEEDBACK DELAY COMPENSATION CIRCUIT 852
$V_{SW_EST_DELAY_ICOR}$
38C
44
TO PARALLEL AMPLIFIER CIRCUIT
CONTROLLER 50
$I_{FEEDBACK_TCA}$
854
V_{RAMP} +
V_{RAMP} -

FIG. 40B

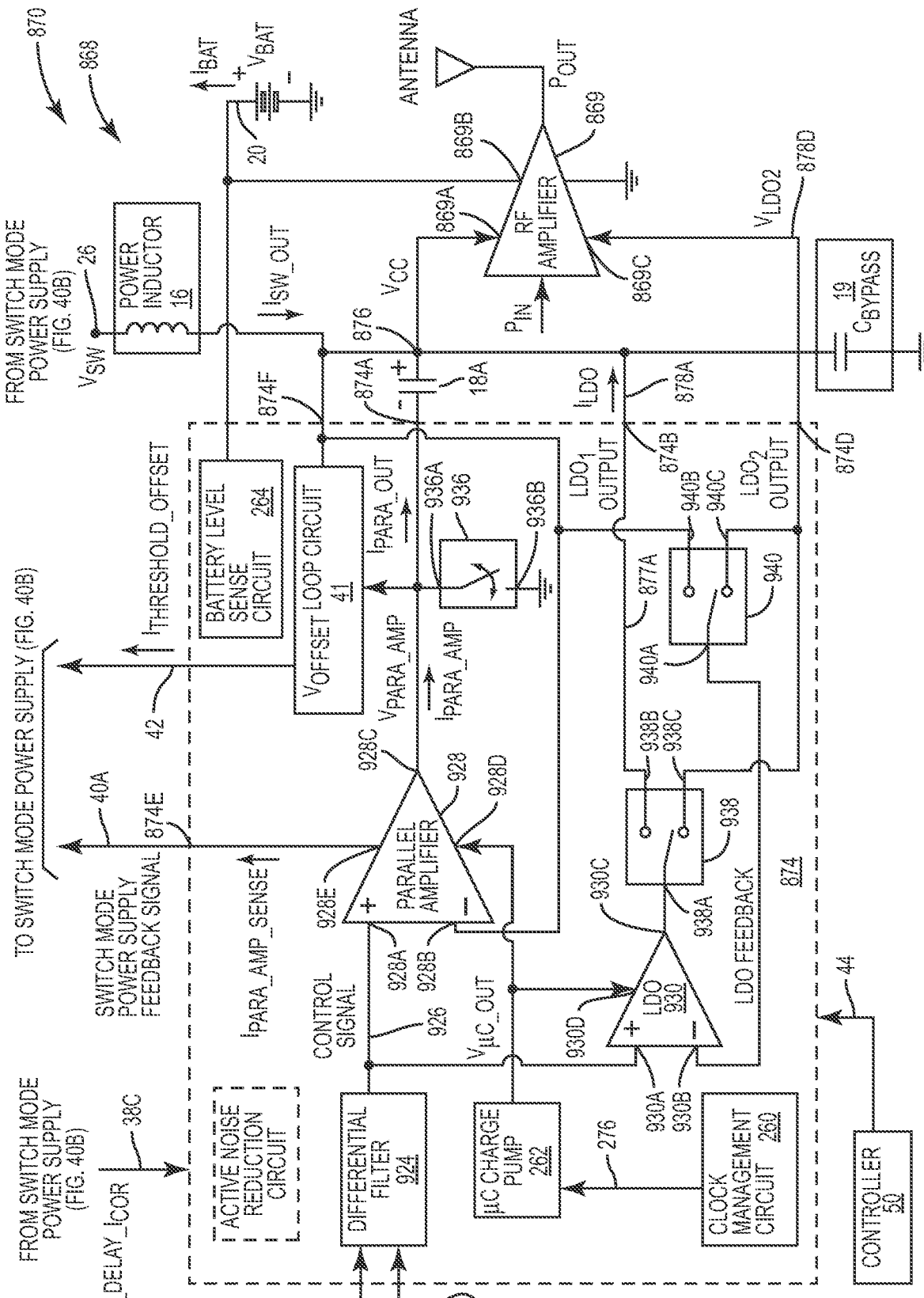

870
868
FROM SWITCH MODE POWER SUPPLY (FIG. 40B)
26
V_{SW}
POWER INDUCTOR 16
I_{SW_OUT}
I_{BAT}
V_{BAT}
20
ANTENNA
P_{OUT}
869
869B
869A
RF AMPLIFIER
869C
P_{IN}
V_{CC}
876
874A
18A
874F
V_{LDO2}
878D
19
C_{BYPASS}
I_{LDO}
878A
874B
874D
LDO_1 OUTPUT
LDO_2 OUTPUT
940B
940C
940
877A
940A
938B
938C
938
938A
930C
930D
930A
930B
LDO 930
LDO FEEDBACK
874
44
CONTROLLER 50
CLOCK MANAGEMENT CIRCUIT 260
276
μC CHARGE PUMP 262
DIFFERENTIAL FILTER 924
ACTIVE NOISE REDUCTION CIRCUIT
FROM SWITCH MODE POWER SUPPLY (FIG. 40B)
38C
$V_{SW_EST_DELAY_ICOR}$
V_{RAMP} +
V_{RAMP} -
DIFFERENTIAL V_{RAMP} SIGNAL
CONTROL SIGNAL
926
928A
928B
928E
PARALLEL AMPLIFIER
928
928C
928D
$V_{\mu C_OUT}$
$I_{PARA_AMP_SENSE}$
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL
874E
40A
TO SWITCH MODE POWER SUPPLY (FIG. 40B)
42
$I_{THRESHOLD_OFFSET}$
BATTERY LEVEL SENSE CIRCUIT 264
V_{OFFSET} LOOP CIRCUIT 41
I_{PARA_AMP}
V_{PARA_AMP}
I_{PARA_OUT}
936A
936
936B

FIG. 40C

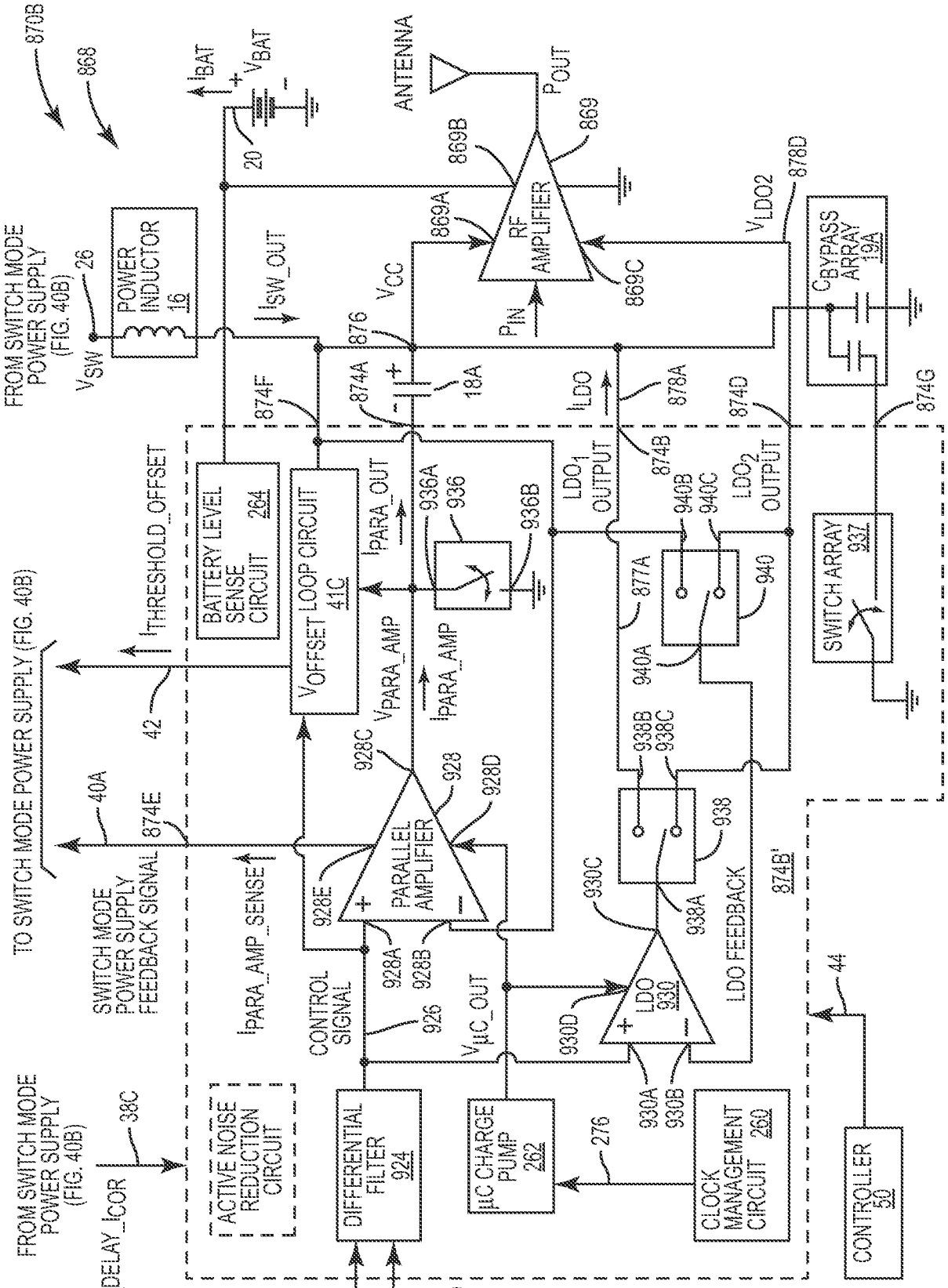

870B
868
FROM SWITCH MODE POWER SUPPLY (FIG. 40B)
26
V_{SW}
POWER INDUCTOR 16
I_{SW_OUT}
I_{BAT}
V_{BAT}
20
ANTENNA
P_{OUT}
869
869B
869A
RF AMPLIFIER
869C
P_{IN}
V_{CC}
876
874A
18A
874F
V_{LDO2}
878D
C_{BYPASS} ARRAY 19A
874G
I_{LDO}
878A
874D
LDO_2 OUTPUT
LDO_1 OUTPUT
874B
940B
940C
940
940A
877A
SWITCH ARRAY 937
936A
936
936B
I_{PARA_OUT}
$V_{OFFSET\ LOOP\ CIRCUIT}$ 41C
BATTERY LEVEL SENSE CIRCUIT 264
$I_{THRESHOLD_OFFSET}$
42
TO SWITCH MODE POWER SUPPLY (FIG. 40B)
40A
874E
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL
$I_{PARA_AMP_SENSE}$
928C
928
928D
V_{PARA_AMP}
I_{PARA_AMP}
PARALLEL AMPLIFIER
928E
928A
928B
CONTROL SIGNAL
926
$V_{\mu C_OUT}$
938B
938C
938
938A
930C
930D
LDO 930
LDO FEEDBACK
874B'
44
FROM SWITCH MODE POWER SUPPLY (FIG. 40B)
38C
$V_{SW_EST_DELAY}$ I_{COR}
ACTIVE NOISE REDUCTION CIRCUIT
DIFFERENTIAL FILTER 924
μC CHARGE PUMP 262
276
930A
930B
CLOCK MANAGEMENT CIRCUIT 260
CONTROLLER 50
V_{RAMP}+
V_{RAMP}-
DIFFERENTIAL V_{RAMP} SIGNAL

FIG. 40D

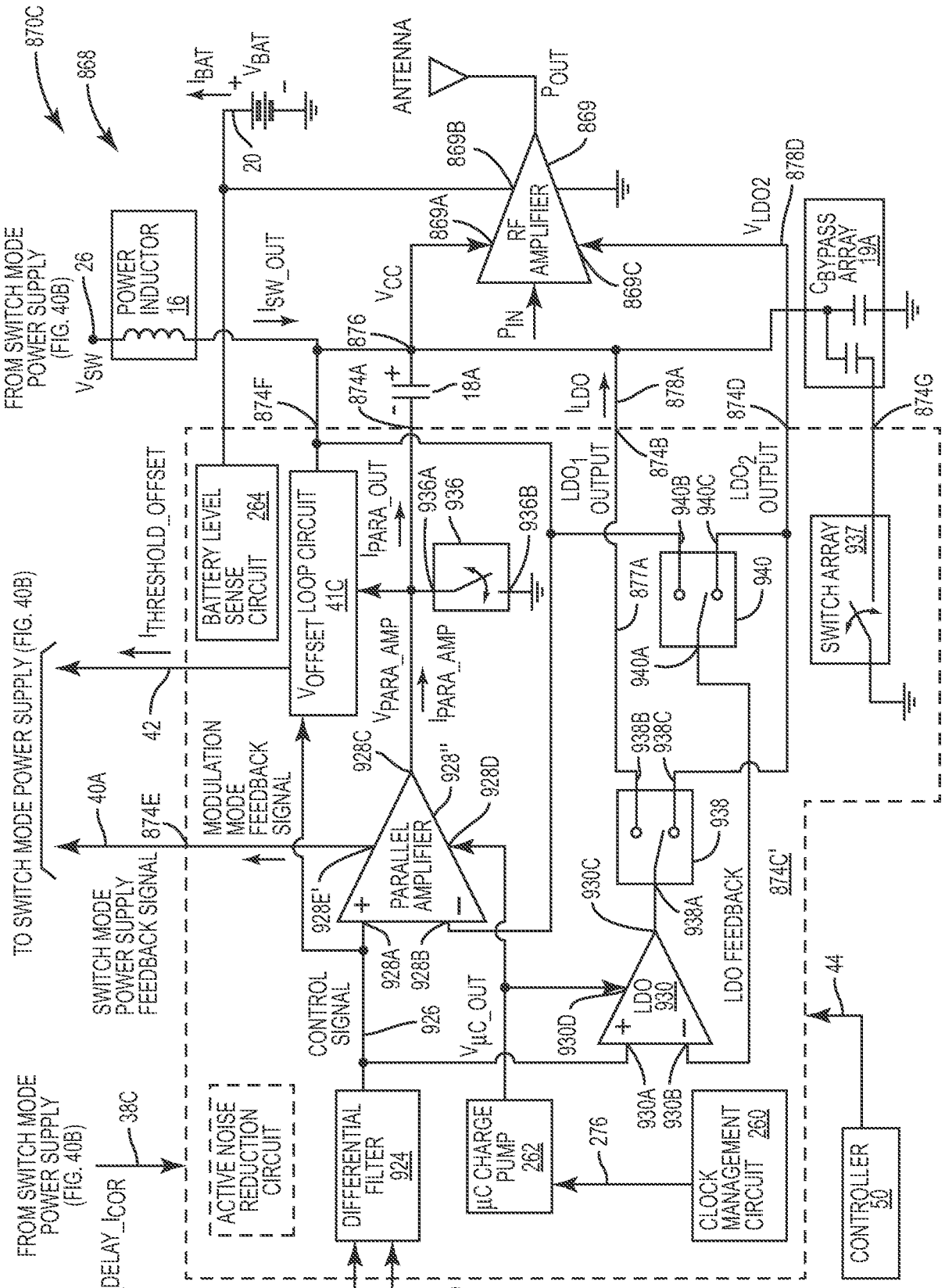

870C
868
FROM SWITCH MODE POWER SUPPLY (FIG. 40B)
26
V_{SW}
POWER INDUCTOR 16
I_{SW_OUT}
I_{BAT}
V_{BAT}
20
ANTENNA
P_{OUT}
869
869B
869A
RF AMPLIFIER
869C
P_{IN}
876
V_{CC}
V_{LDO2}
878D
C_{BYPASS} ARRAY 19A
874F
874A
18A
874D
874G
I_{LDO}
878A
874B
LDO_1 OUTPUT
LDO_2 OUTPUT
940B
940C
940
877A
940A
SWITCH ARRAY 937
TO SWITCH MODE POWER SUPPLY (FIG. 40B)
40A
874E
42
$I_{THRESHOLD_OFFSET}$
BATTERY LEVEL SENSE CIRCUIT 264
V_{OFFSET} LOOP CIRCUIT 41C
I_{PARA_OUT}
936A
936
936B
MODULATION MODE FEEDBACK SIGNAL
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL
928C
V_{PARA_AMP}
I_{PARA_AMP}
928''
928D
928E'
PARALLEL AMPLIFIER
928A
928B
CONTROL SIGNAL
926
$V_{\mu C_OUT}$
930C
938B
938C
938
938A
LDO FEEDBACK
874C'
930D
LDO 930
930A
930B
44
FROM SWITCH MODE POWER SUPPLY (FIG. 40B)
38C
$V_{SW_EST_DELAY_ICOR}$
ACTIVE NOISE REDUCTION CIRCUIT
DIFFERENTIAL FILTER 924
μC CHARGE PUMP 262
276
CLOCK MANAGEMENT CIRCUIT 260
CONTROLLER 50
V_{RAMP}+
V_{RAMP}-
DIFFERENTIAL V_{RAMP} SIGNAL

FIG. 40E

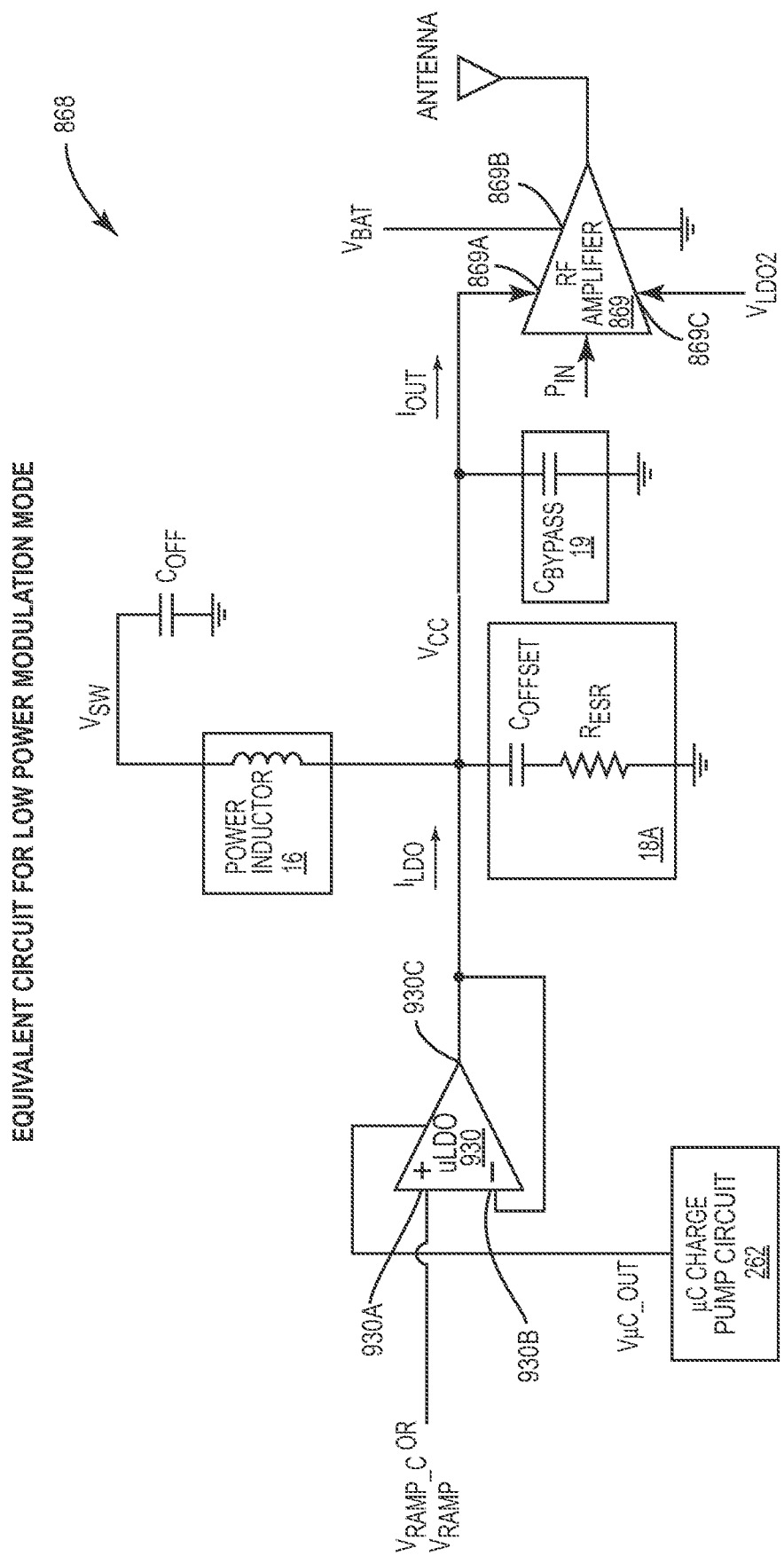

EQUIVALENT CIRCUIT FOR LOW POWER MODULATION MODE
868
ANTENNA
V_{BAT}
869B
869A
RF AMPLIFIER 869
869C
V_{LDO2}
P_{IN}
I_{OUT}
C_{BYPASS} 19
C_{OFF}
V_{SW}
V_{CC}
C_{OFFSET}
R_{ESR}
18A
POWER INDUCTOR 16
I_{LDO}
930C
uLDO 930
930A
930B
$V_{\mu C_OUT}$
µC CHARGE PUMP CIRCUIT 262
V_{RAMP_C} OR V_{RAMP}

FIG. 41

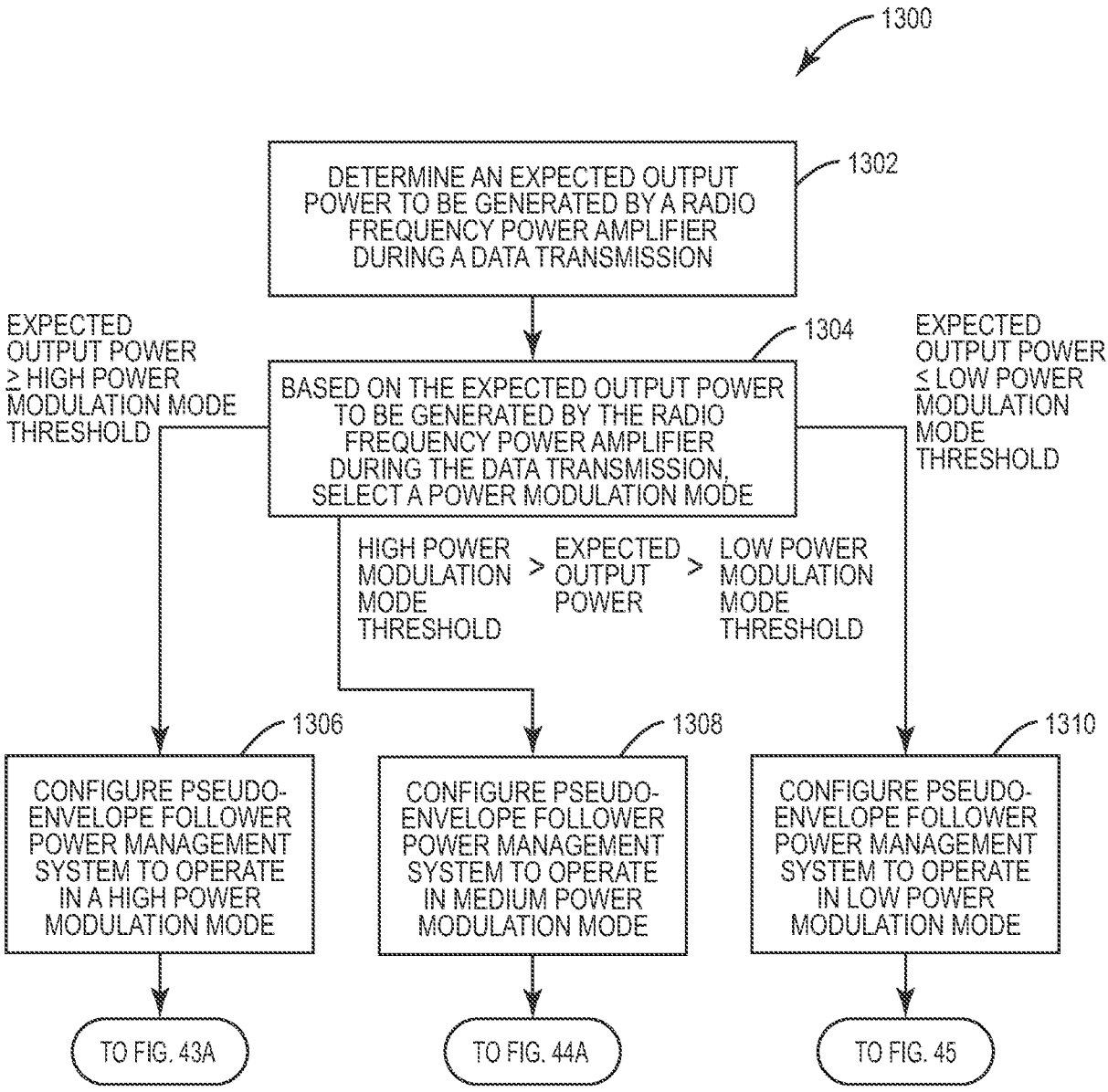

1300
DETERMINE AN EXPECTED OUTPUT POWER TO BE GENERATED BY A RADIO FREQUENCY POWER AMPLIFIER DURING A DATA TRANSMISSION
1302
EXPECTED OUTPUT POWER ≥ HIGH POWER MODULATION MODE THRESHOLD
1304
BASED ON THE EXPECTED OUTPUT POWER TO BE GENERATED BY THE RADIO FREQUENCY POWER AMPLIFIER DURING THE DATA TRANSMISSION, SELECT A POWER MODULATION MODE
EXPECTED OUTPUT POWER ≤ LOW POWER MODULATION MODE THRESHOLD
HIGH POWER MODULATION MODE THRESHOLD > EXPECTED OUTPUT POWER > LOW POWER MODULATION MODE THRESHOLD
1306
CONFIGURE PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM TO OPERATE IN A HIGH POWER MODULATION MODE
1308
CONFIGURE PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM TO OPERATE IN MEDIUM POWER MODULATION MODE
1310
CONFIGURE PSEUDO-ENVELOPE FOLLOWER POWER MANAGEMENT SYSTEM TO OPERATE IN LOW POWER MODULATION MODE
TO FIG. 43A
TO FIG. 44A
TO FIG. 45

FIG. 42

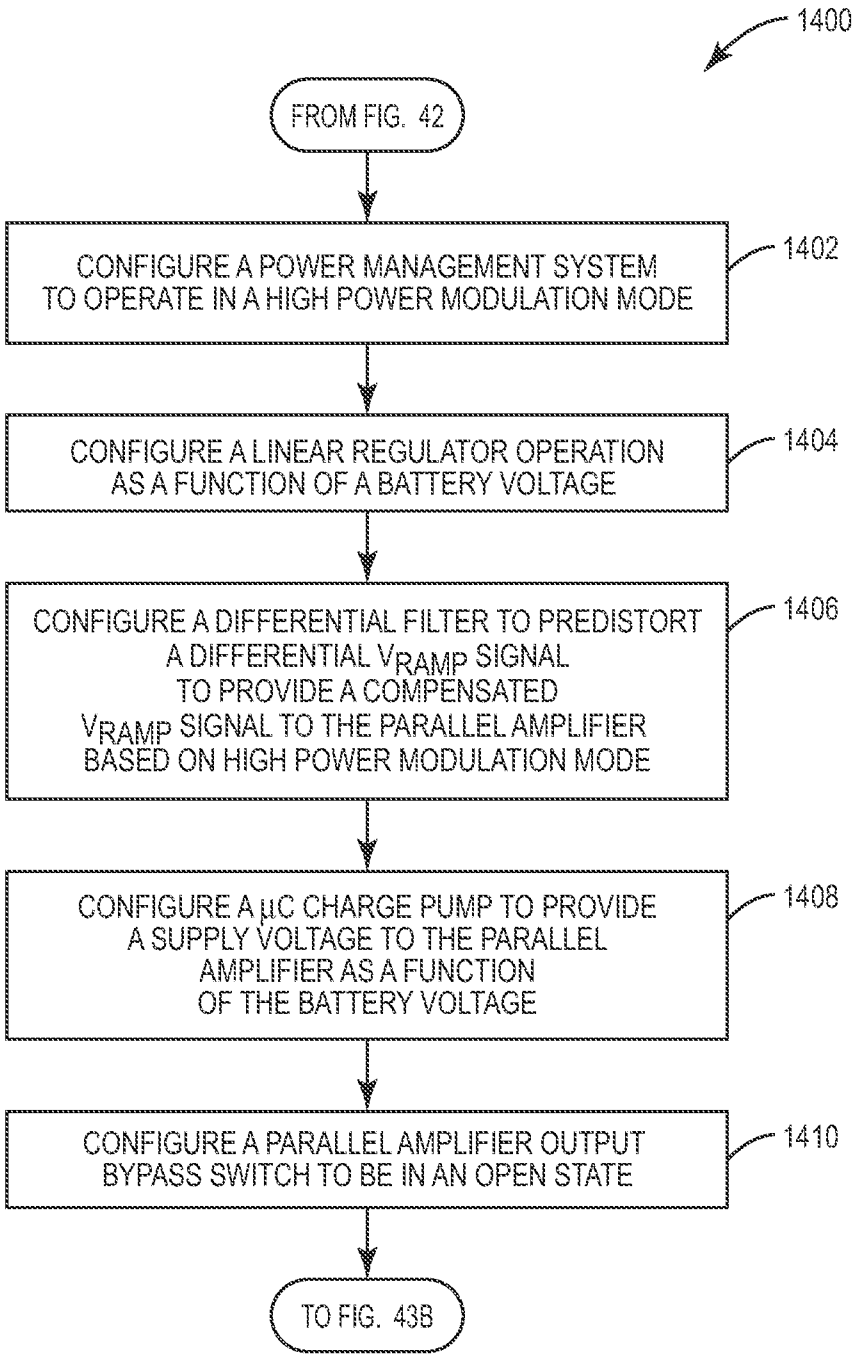

1400
FROM FIG. 42
CONFIGURE A POWER MANAGEMENT SYSTEM TO OPERATE IN A HIGH POWER MODULATION MODE
1402
CONFIGURE A LINEAR REGULATOR OPERATION AS A FUNCTION OF A BATTERY VOLTAGE
1404
CONFIGURE A DIFFERENTIAL FILTER TO PREDISTORT A DIFFERENTIAL V_{RAMP} SIGNAL TO PROVIDE A COMPENSATED V_{RAMP} SIGNAL TO THE PARALLEL AMPLIFIER BASED ON HIGH POWER MODULATION MODE
1406
CONFIGURE A μC CHARGE PUMP TO PROVIDE A SUPPLY VOLTAGE TO THE PARALLEL AMPLIFIER AS A FUNCTION OF THE BATTERY VOLTAGE
1408
CONFIGURE A PARALLEL AMPLIFIER OUTPUT BYPASS SWITCH TO BE IN AN OPEN STATE
1410
TO FIG. 43B

FIG. 43A

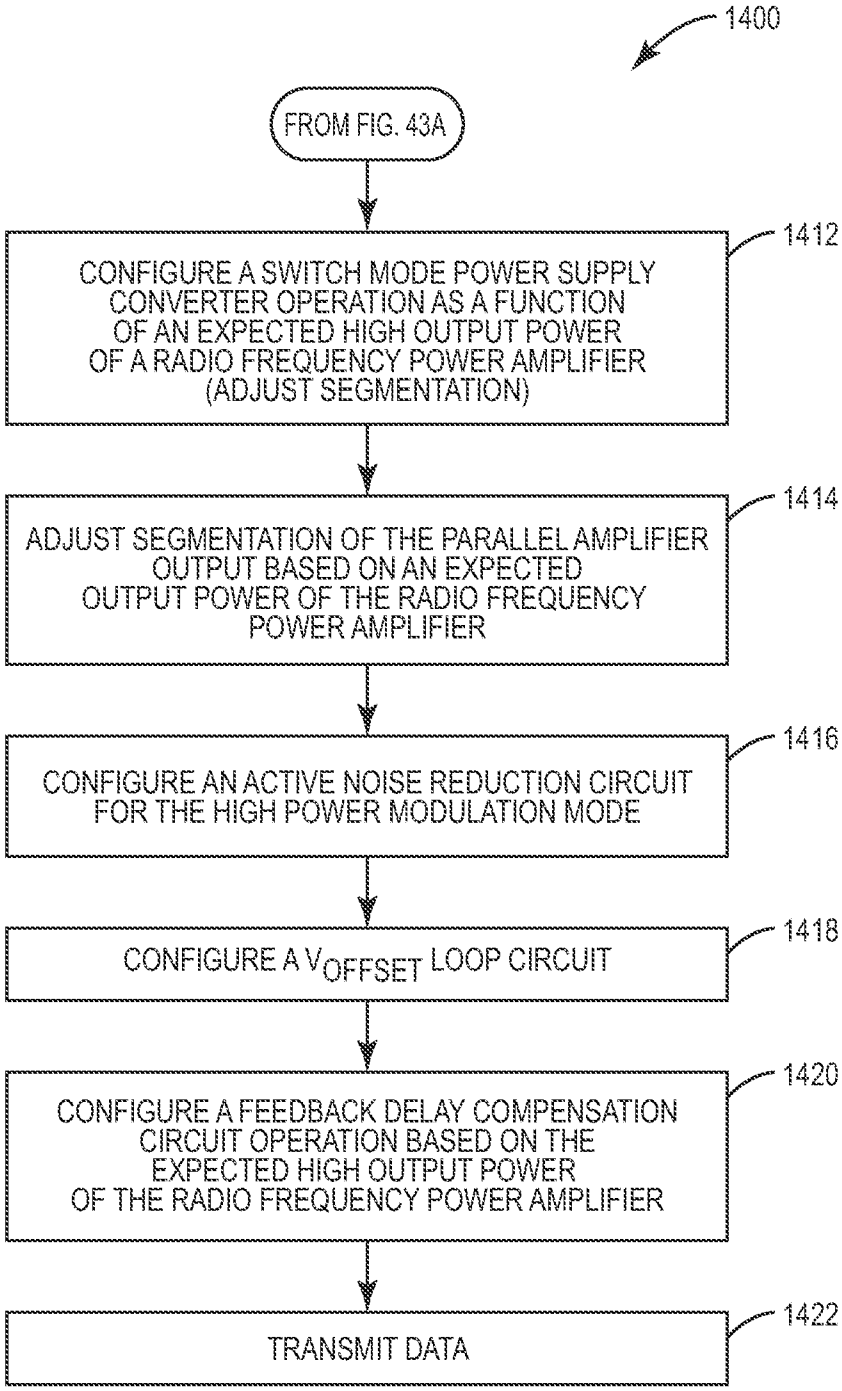

1400
FROM FIG. 43A
CONFIGURE A SWITCH MODE POWER SUPPLY CONVERTER OPERATION AS A FUNCTION OF AN EXPECTED HIGH OUTPUT POWER OF A RADIO FREQUENCY POWER AMPLIFIER (ADJUST SEGMENTATION)
1412
ADJUST SEGMENTATION OF THE PARALLEL AMPLIFIER OUTPUT BASED ON AN EXPECTED OUTPUT POWER OF THE RADIO FREQUENCY POWER AMPLIFIER
1414
CONFIGURE AN ACTIVE NOISE REDUCTION CIRCUIT FOR THE HIGH POWER MODULATION MODE
1416
CONFIGURE A V_{OFFSET} LOOP CIRCUIT
1418
CONFIGURE A FEEDBACK DELAY COMPENSATION CIRCUIT OPERATION BASED ON THE EXPECTED HIGH OUTPUT POWER OF THE RADIO FREQUENCY POWER AMPLIFIER
1420
TRANSMIT DATA
1422

FIG. 43B

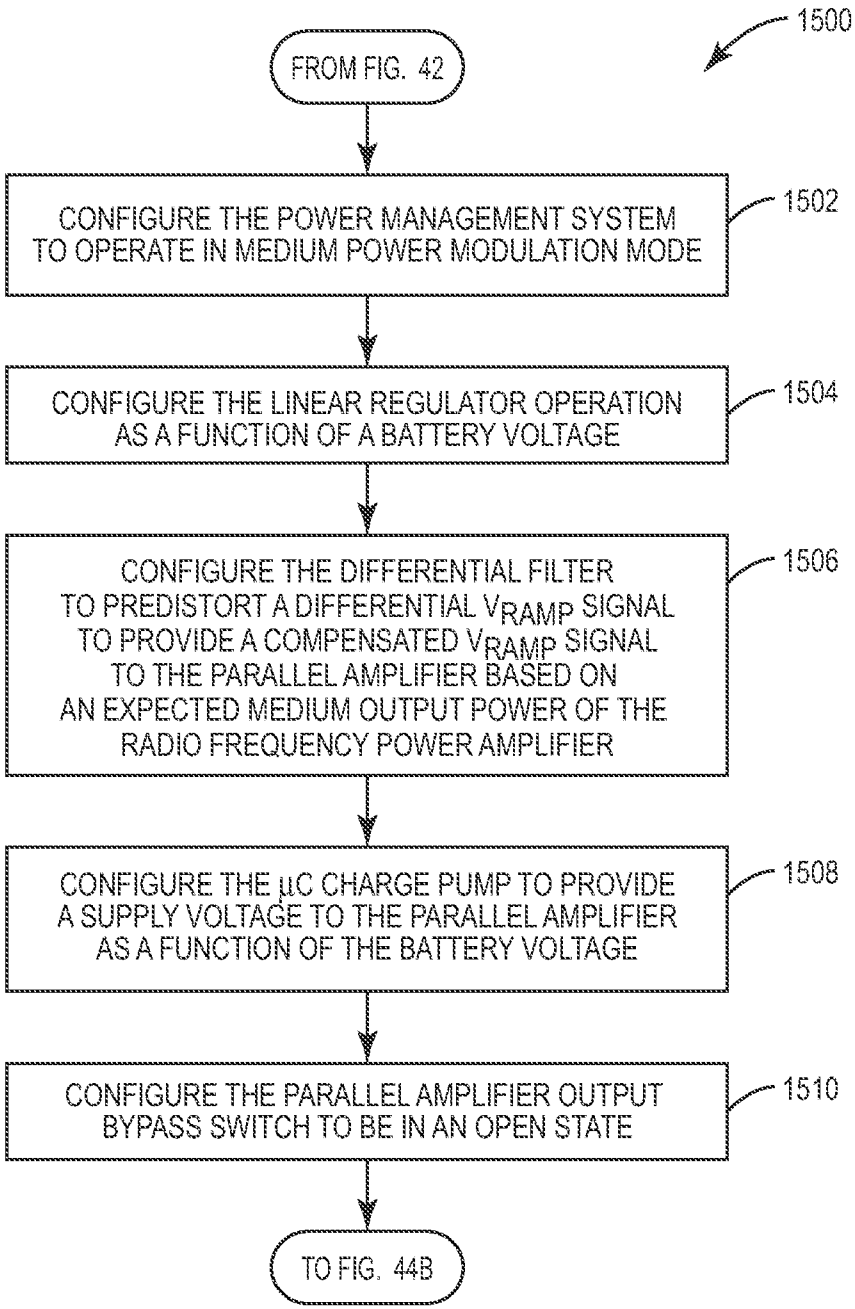

1500
FROM FIG. 42
CONFIGURE THE POWER MANAGEMENT SYSTEM TO OPERATE IN MEDIUM POWER MODULATION MODE
1502
CONFIGURE THE LINEAR REGULATOR OPERATION AS A FUNCTION OF A BATTERY VOLTAGE
1504
CONFIGURE THE DIFFERENTIAL FILTER TO PREDISTORT A DIFFERENTIAL V_{RAMP} SIGNAL TO PROVIDE A COMPENSATED V_{RAMP} SIGNAL TO THE PARALLEL AMPLIFIER BASED ON AN EXPECTED MEDIUM OUTPUT POWER OF THE RADIO FREQUENCY POWER AMPLIFIER
1506
CONFIGURE THE µC CHARGE PUMP TO PROVIDE A SUPPLY VOLTAGE TO THE PARALLEL AMPLIFIER AS A FUNCTION OF THE BATTERY VOLTAGE
1508
CONFIGURE THE PARALLEL AMPLIFIER OUTPUT BYPASS SWITCH TO BE IN AN OPEN STATE
1510
TO FIG. 44B

FIG. 44A

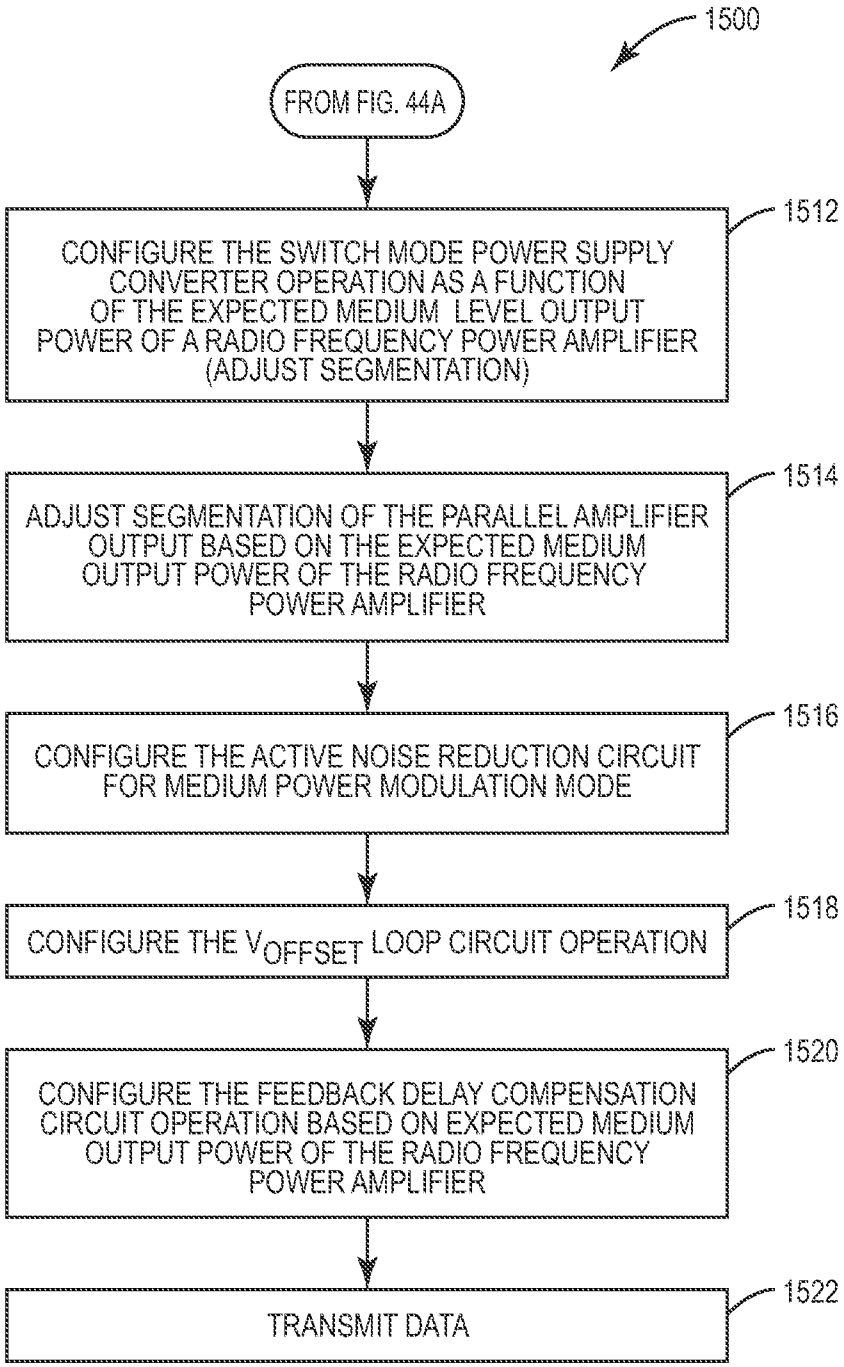

1500
FROM FIG. 44A
CONFIGURE THE SWITCH MODE POWER SUPPLY CONVERTER OPERATION AS A FUNCTION OF THE EXPECTED MEDIUM LEVEL OUTPUT POWER OF A RADIO FREQUENCY POWER AMPLIFIER (ADJUST SEGMENTATION)
1512
ADJUST SEGMENTATION OF THE PARALLEL AMPLIFIER OUTPUT BASED ON THE EXPECTED MEDIUM OUTPUT POWER OF THE RADIO FREQUENCY POWER AMPLIFIER
1514
CONFIGURE THE ACTIVE NOISE REDUCTION CIRCUIT FOR MEDIUM POWER MODULATION MODE
1516
CONFIGURE THE V_{OFFSET} LOOP CIRCUIT OPERATION
1518
CONFIGURE THE FEEDBACK DELAY COMPENSATION CIRCUIT OPERATION BASED ON EXPECTED MEDIUM OUTPUT POWER OF THE RADIO FREQUENCY POWER AMPLIFIER
1520
TRANSMIT DATA
1522

FIG. 44B

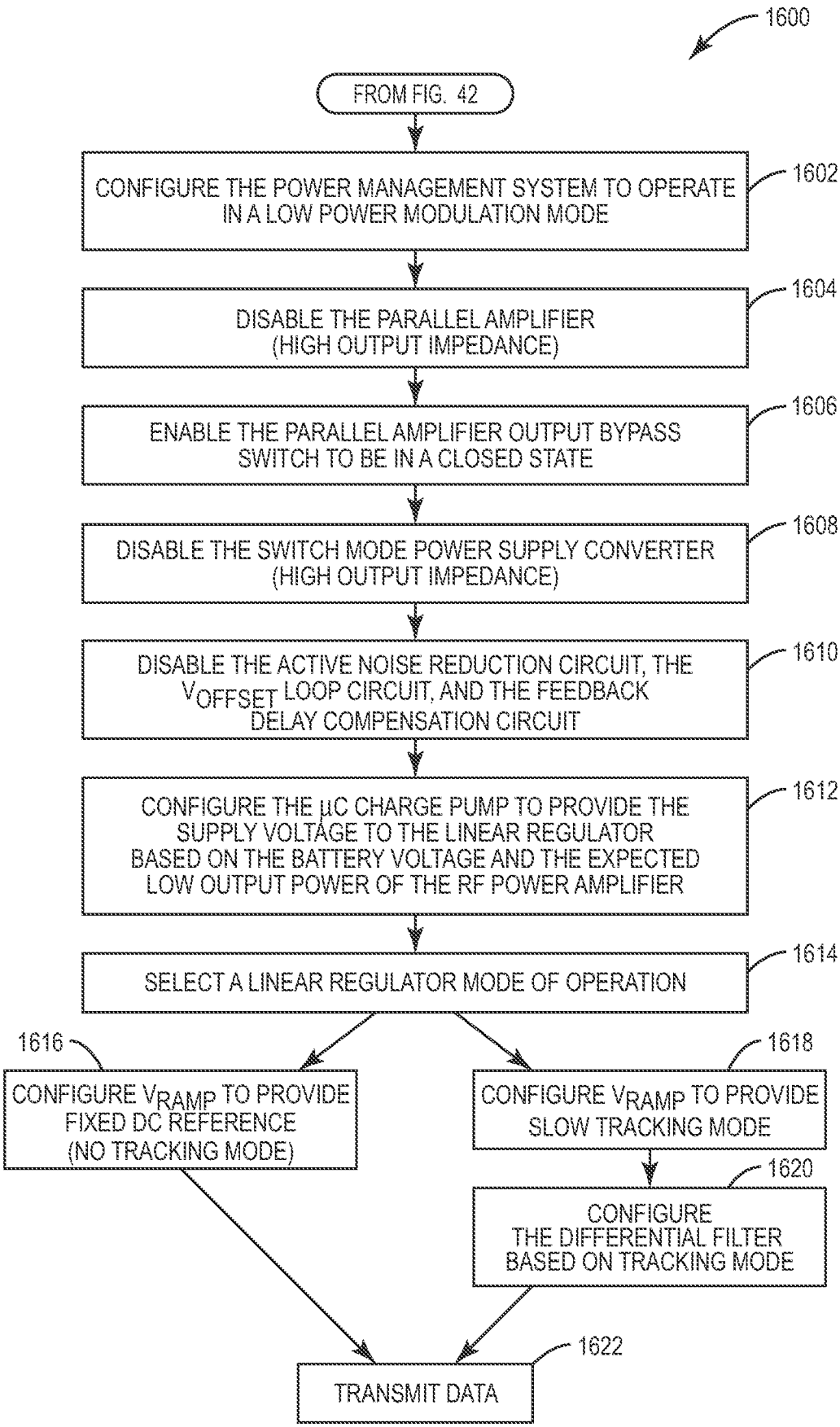

1600
FROM FIG. 42
CONFIGURE THE POWER MANAGEMENT SYSTEM TO OPERATE IN A LOW POWER MODULATION MODE
1602
DISABLE THE PARALLEL AMPLIFIER (HIGH OUTPUT IMPEDANCE)
1604
ENABLE THE PARALLEL AMPLIFIER OUTPUT BYPASS SWITCH TO BE IN A CLOSED STATE
1606
DISABLE THE SWITCH MODE POWER SUPPLY CONVERTER (HIGH OUTPUT IMPEDANCE)
1608
DISABLE THE ACTIVE NOISE REDUCTION CIRCUIT, THE V_{OFFSET} LOOP CIRCUIT, AND THE FEEDBACK DELAY COMPENSATION CIRCUIT
1610
CONFIGURE THE µC CHARGE PUMP TO PROVIDE THE SUPPLY VOLTAGE TO THE LINEAR REGULATOR BASED ON THE BATTERY VOLTAGE AND THE EXPECTED LOW OUTPUT POWER OF THE RF POWER AMPLIFIER
1612
SELECT A LINEAR REGULATOR MODE OF OPERATION
1614
1616
CONFIGURE V_{RAMP} TO PROVIDE FIXED DC REFERENCE (NO TRACKING MODE)
1618
CONFIGURE V_{RAMP} TO PROVIDE SLOW TRACKING MODE
1620
CONFIGURE THE DIFFERENTIAL FILTER BASED ON TRACKING MODE
1622
TRANSMIT DATA

FIG. 45

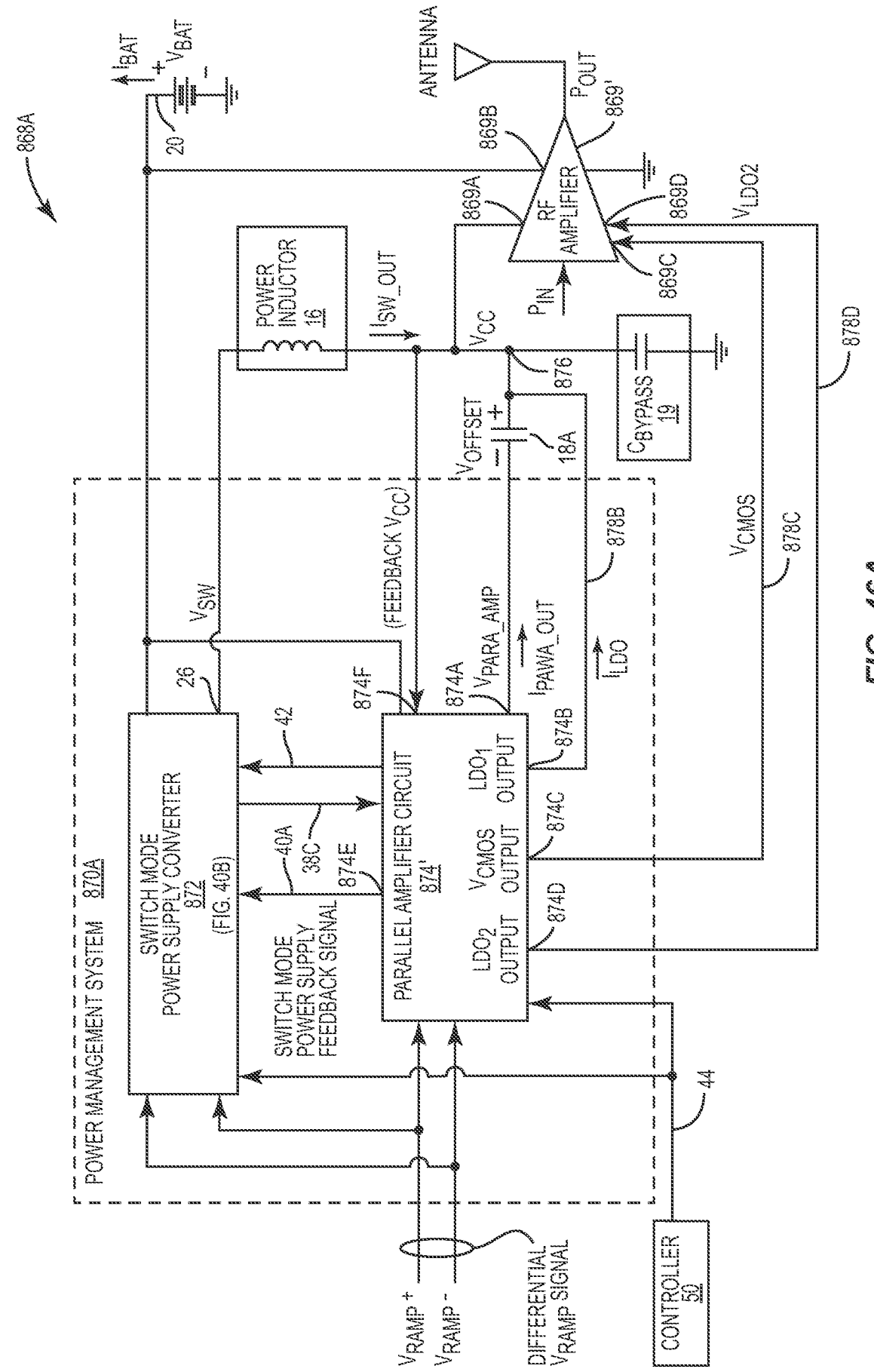

868A
I_{BAT}
V_{BAT}
20
ANTENNA
P_{OUT}
869'
869B
869A
RF AMPLIFIER
869C
868D
V_{LDO2}
P_{IN}
POWER INDUCTOR 16
I_{SW_OUT}
V_{CC}
876
878D
C_{BYPASS} 19
V_{OFFSET}
18A
POWER MANAGEMENT SYSTEM 870A
SWITCH MODE POWER SUPPLY CONVERTER 872 (FIG. 40B)
26
V_{SW}
(FEEDBACK V_{CC})
874F
874A
V_{PARA_AMP}
I_{PAWA_OUT}
878B
I_{LDO}
V_{CMOS}
878C
42
PARALLEL AMPLIFIER CIRCUIT 874'
LDO_1 OUTPUT
874B
40A
38C
874E
V_{CMOS} OUTPUT
874C
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL
LDO_2 OUTPUT
874D
44
V_{RAMP} +
V_{RAMP} -
DIFFERENTIAL V_{RAMP} SIGNAL
CONTROLLER 50

FIG. 46A

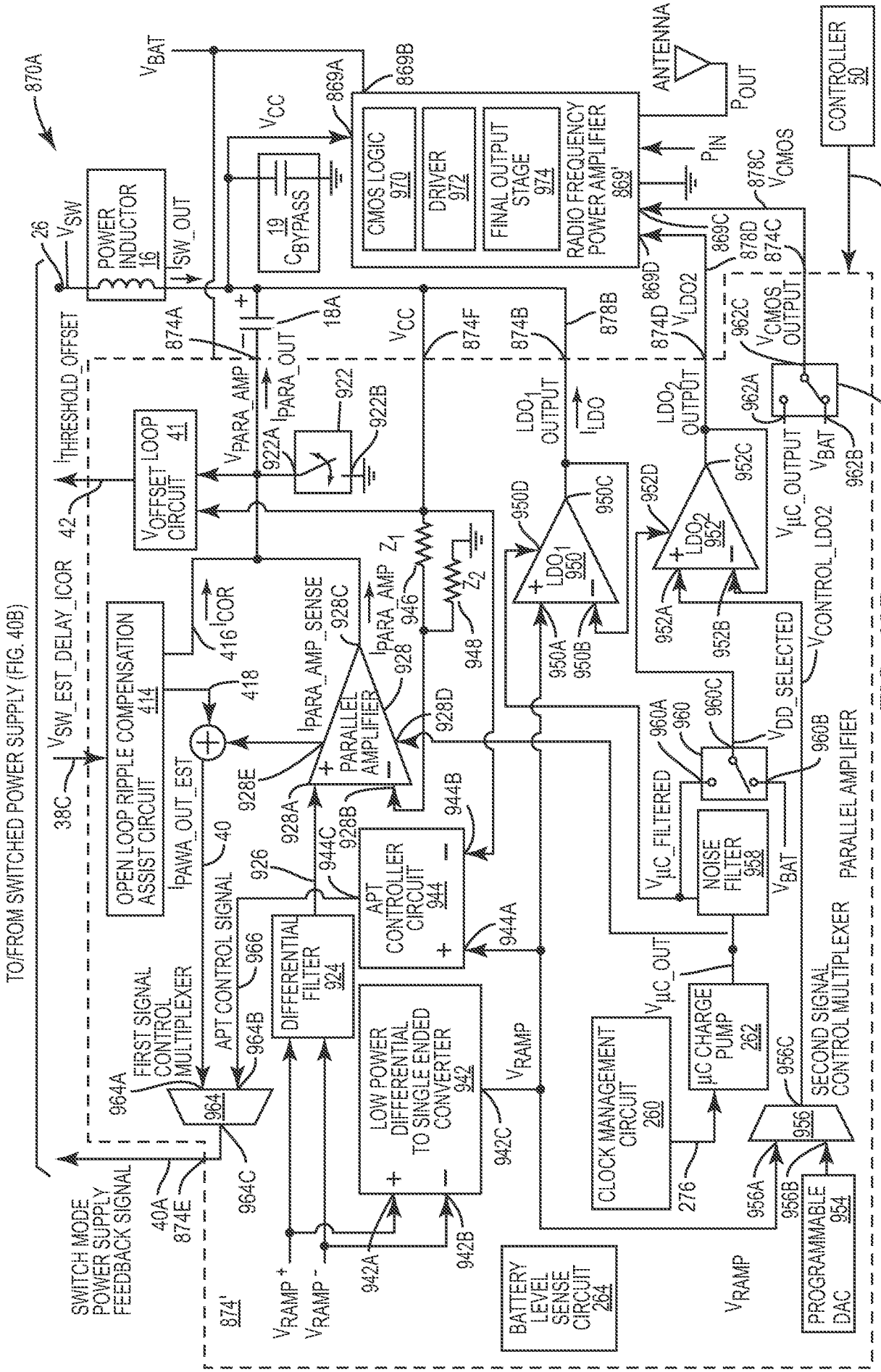

870A
TO/FROM SWITCH MODE POWER SUPPLY (FIG. 40B)
874'
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL
40A
874E
964C
964
964A
FIRST SIGNAL CONTROL MULTIPLEXER
964B
APT CONTROL SIGNAL
966
DIFFERENTIAL FILTER 924
926
928A
928B
944C
APT CONTROLLER CIRCUIT 944
944A
944B
928E
928
928D
PARALLEL AMPLIFIER
928C
IPARA_AMP_SENSE
IPARA_AMP
Z1
946
Z2
948
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT 414
IPAWA_OUT_EST
40
418
416
ICOR
VSW_EST_DELAY_ICOR
42
38C
VOFFSET LOOP CIRCUIT 41
ITHRESHOLD_OFFSET
VPARA_AMP
IPARA_OUT
922A
922
922B
18A
874A
VBAT
VCC
19
CBYPASS
869A
869B
CMOS LOGIC 970
DRIVER 972
FINAL OUTPUT STAGE 974
RADIO FREQUENCY POWER AMPLIFIER 869'
ANTENNA
PIN
POUT
26
VSW
POWER INDUCTOR 16
ISW_OUT
874F
874B
878B
LDO1 OUTPUT
ILDO
LDO1 950
950A
950B
950C
950D
LDO2 952
952A
952B
952C
952D
874D
869D
VLDO2
LDO2 OUTPUT
878D
874C
878C
VCMOS
962C
VCMOS OUTPUT
962A
962B
962
VBAT
VμC_OUTPUT
VCONTROL_LDO2
CONTROLLER 50
44
VRAMP+
VRAMP-
LOW POWER DIFFERENTIAL TO SINGLE ENDED CONVERTER 942
942A
942B
942C
VRAMP
CLOCK MANAGEMENT CIRCUIT 260
VμC_OUT
276
μC CHARGE PUMP 262
VμC_FILTERED
960A
960
960C
NOISE FILTER 958
VBAT
VDD_SELECTED
960B
PARALLEL AMPLIFIER
956A
956B
956C
956
SECOND SIGNAL CONTROL MULTIPLEXER
VRAMP
PROGRAMMABLE DAC 954
BATTERY LEVEL SENSE CIRCUIT 264

FIG. 46B

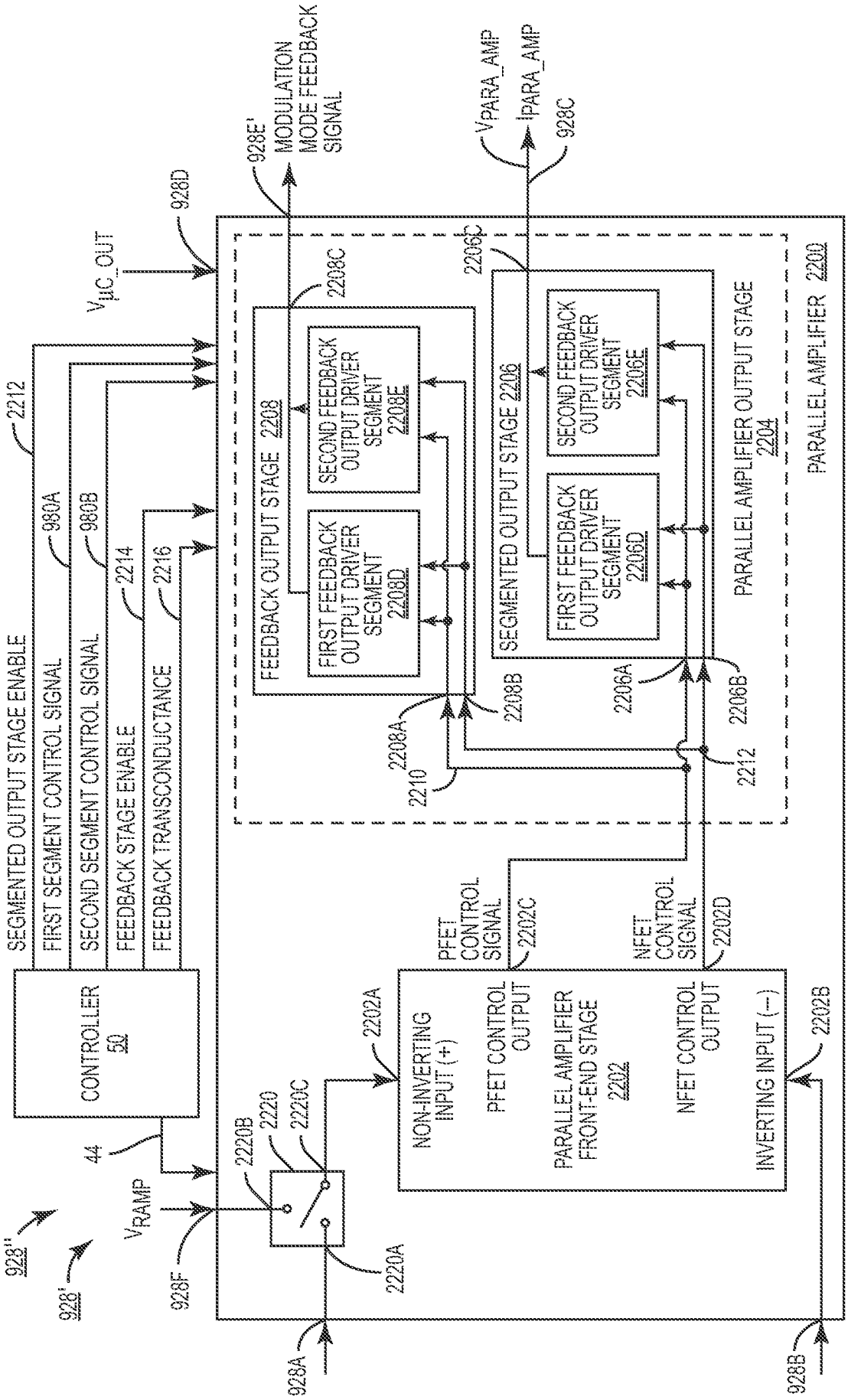

928''
928'
928A
928B
928C
928D
928E'
928F
MODULATION MODE FEEDBACK SIGNAL
$V_{\mu C_OUT}$
V_{PARA_AMP}
I_{PARA_AMP}
V_{RAMP}
44
CONTROLLER 50
SEGMENTED OUTPUT STAGE ENABLE
FIRST SEGMENT CONTROL SIGNAL
SECOND SEGMENT CONTROL SIGNAL
FEEDBACK STAGE ENABLE
FEEDBACK TRANSCONDUCTANCE
2212
980A
980B
2214
2216
2220
2220A
2220B
2220C
2202A
NON-INVERTING INPUT (+)
INVERTING INPUT (−)
PARALLEL AMPLIFIER FRONT-END STAGE 2202
PFET CONTROL OUTPUT
NFET CONTROL OUTPUT
PFET CONTROL SIGNAL 2202C
NFET CONTROL SIGNAL 2202D
2202B
PARALLEL AMPLIFIER OUTPUT STAGE 2204
FEEDBACK OUTPUT STAGE 2208
FIRST FEEDBACK OUTPUT DRIVER SEGMENT 2208D
SECOND FEEDBACK OUTPUT DRIVER SEGMENT 2208E
2208C
2208A
2208B
2210
SEGMENTED OUTPUT STAGE 2206
FIRST FEEDBACK OUTPUT DRIVER SEGMENT 2206D
SECOND FEEDBACK OUTPUT DRIVER SEGMENT 2206E
2206C
2206A
2206B
PARALLEL AMPLIFIER 2200

FIG. 46C

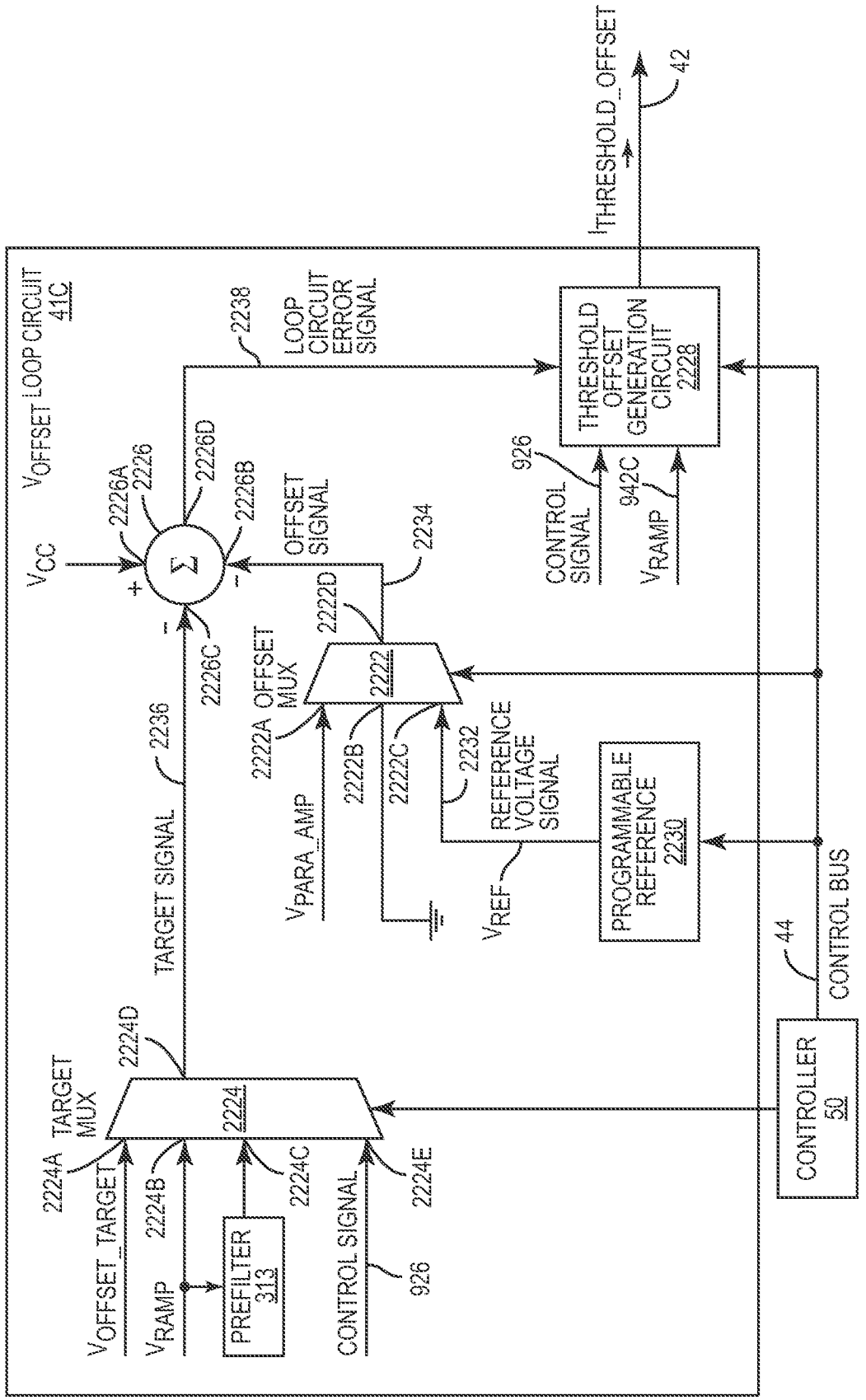

VOFFSET LOOP CIRCUIT 41C
ITHRESHOLD_OFFSET
42
2238
LOOP CIRCUIT ERROR SIGNAL
THRESHOLD OFFSET GENERATION CIRCUIT 2228
926
CONTROL SIGNAL
942C
VRAMP
VCC
2226A
2226
2226D
2226B
OFFSET SIGNAL
2234
2226C
2222D
2222A OFFSET MUX
2222
2222B
2222C
2232
REFERENCE VOLTAGE SIGNAL
VPARA_AMP
VREF
PROGRAMMABLE REFERENCE 2230
TARGET SIGNAL
2236
2224D
2224A TARGET MUX
2224
2224B
2224C
2224E
VOFFSET_TARGET
VRAMP
PREFILTER 313
CONTROL SIGNAL
926
CONTROLLER 50
44
CONTROL BUS

FIG. 46D

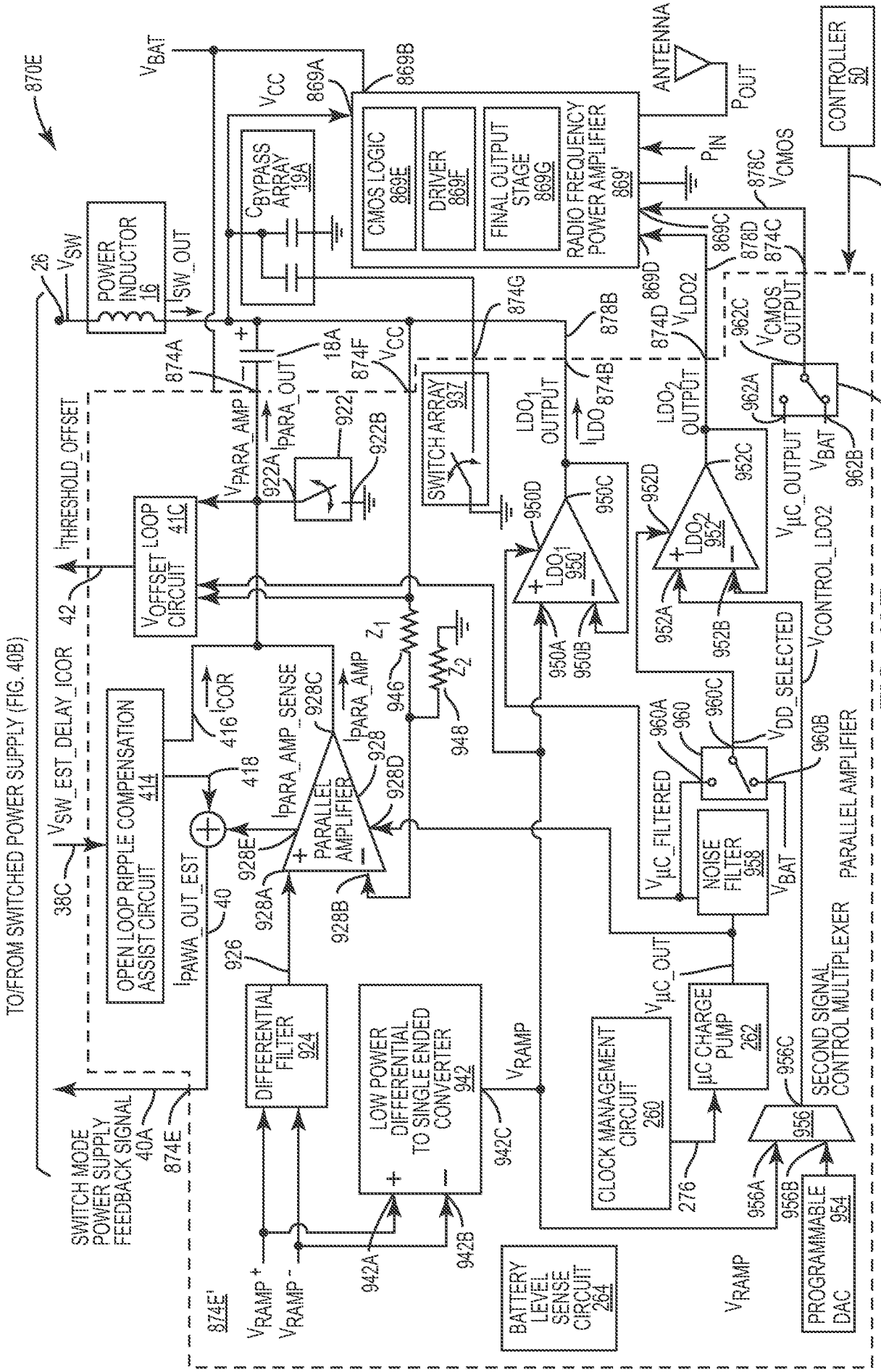

870E
TO/FROM SWITCHED POWER SUPPLY (FIG. 40B)
874E'
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL 40A
874E
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT 414
DIFFERENTIAL FILTER 924
LOW POWER DIFFERENTIAL TO SINGLE ENDED CONVERTER 942
CLOCK MANAGEMENT CIRCUIT 260
μC CHARGE PUMP 262
BATTERY LEVEL SENSE CIRCUIT 264
PROGRAMMABLE DAC 954
SECOND SIGNAL CONTROL MULTIPLEXER 956
PARALLEL AMPLIFIER
NOISE FILTER 958
V_OFFSET LOOP CIRCUIT 41C
PARALLEL AMPLIFIER
SWITCH ARRAY 937
LDO1 950
LDO2 952
POWER INDUCTOR 16
C_BYPASS ARRAY 19A
CMOS LOGIC 869E
DRIVER 869F
FINAL OUTPUT STAGE 869G
RADIO FREQUENCY POWER AMPLIFIER 869'
ANTENNA
CONTROLLER 50
V_BAT
V_SW
I_SW_OUT
V_CC
I_THRESHOLD_OFFSET
I_PARA_AMP
I_PARA_OUT
I_COR
I_PAWA_OUT_EST
I_PARA_AMP_SENSE
V_SW_EST_DELAY_ICOR
V_RAMP+
V_RAMP-
V_RAMP
V_μC_OUT
V_μC_FILTERED
V_DD_SELECTED
V_CONTROL_LDO2
V_μC_OUTPUT
V_CMOS
V_CMOS OUTPUT
LDO1 OUTPUT
LDO2 OUTPUT
I_LDO
P_IN
P_OUT
Z1
Z2

FIG. 46E

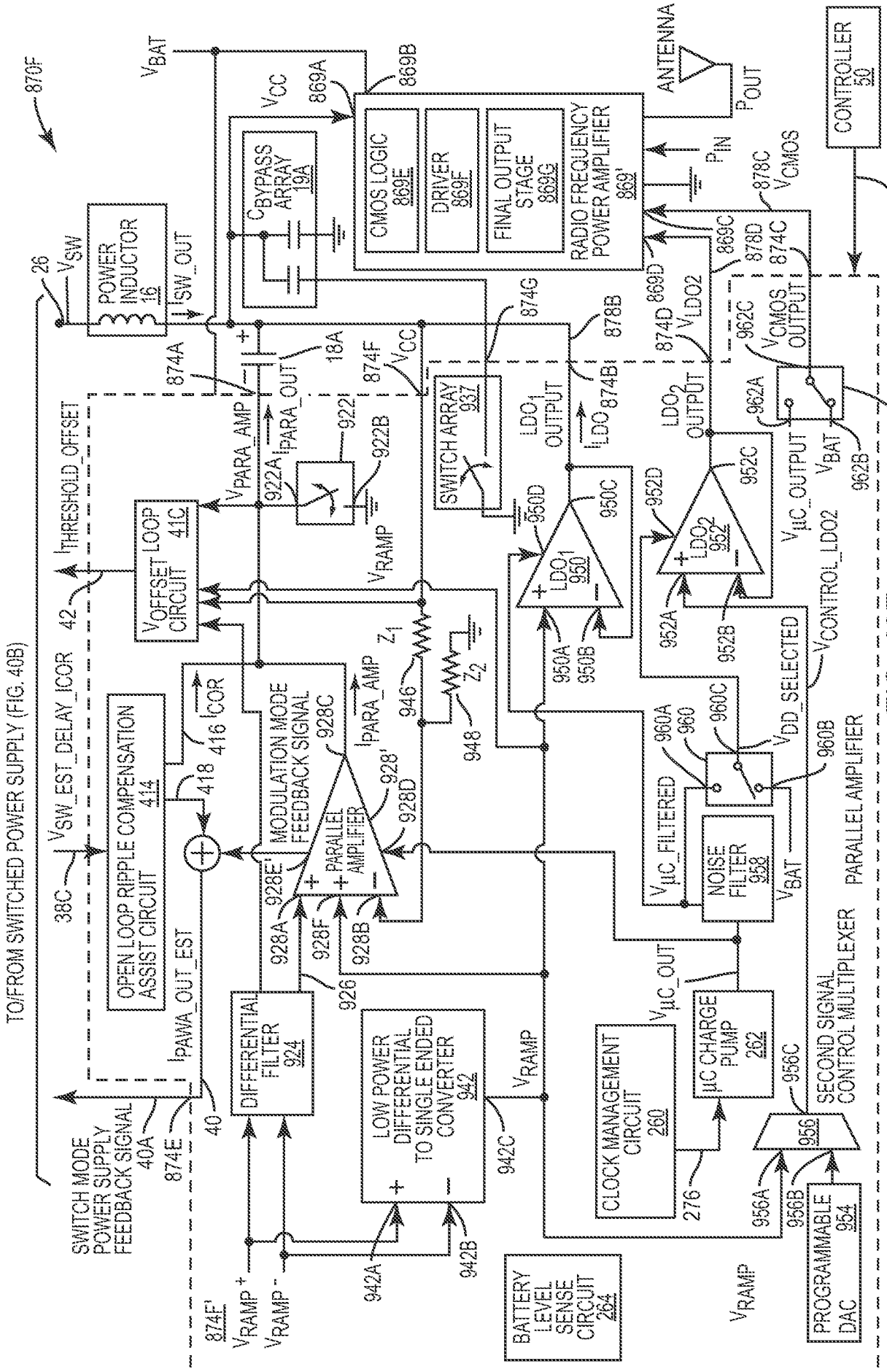

870F
TO/FROM SWITCHED POWER SUPPLY (FIG. 40B)
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL 40A
874E
40
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT 414
IPAWA_OUT_EST
38C
VSW_EST_DELAY_ICOR
42
416 ICOR
418
VOFFSET LOOP CIRCUIT 410
ITHRESHOLD_OFFSET
26
VSW
POWER INDUCTOR 16
ISW_OUT
VBAT
874A
VCC
CBYPASS ARRAY 19A
869A
869B
CMOS LOGIC 869E
DRIVER 869F
FINAL OUTPUT STAGE 869G
RADIO FREQUENCY POWER AMPLIFIER 869'
ANTENNA
PIN
POUT
878C VCMOS
869C
869D
878D
874C
VLDO2
874D
962C
VCMOS OUTPUT
962A
962B
962
VBAT
VμC_OUTPUT
VCONTROL_LDO2
952C
952D
LDO2 952
LDO2 OUTPUT
952A
952B
VDD_SELECTED
960B
960C
960
960A
VμC_FILTERED
NOISE FILTER 958
VBAT
PARALLEL AMPLIFIER
950A
950B
950C
950D
LDO1 960
LDO1 OUTPUT
LDO 874B
878B
874G
SWITCH ARRAY 937
874F
VCC
18A
IPARA_OUT
922
922A
922B
VRAMP
VPARA_AMP
IPARA_AMP
928'
928C
928D
928E'
MODULATION MODE FEEDBACK SIGNAL
PARALLEL AMPLIFIER
928A
928B
928F
926
Z1
Z2
946
948
DIFFERENTIAL FILTER 924
LOW POWER DIFFERENTIAL TO SINGLE ENDED CONVERTER 942
942A
942B
942C
VRAMP
VRAMP +
VRAMP -
874F'
BATTERY LEVEL SENSE CIRCUIT 264
CLOCK MANAGEMENT CIRCUIT 260
VμC_OUT
276
μC CHARGE PUMP 262
956C
956
956A
956B
SECOND SIGNAL CONTROL MULTIPLEXER
PROGRAMMABLE DAC 954
VRAMP
CONTROLLER 50
44

FIG. 46F

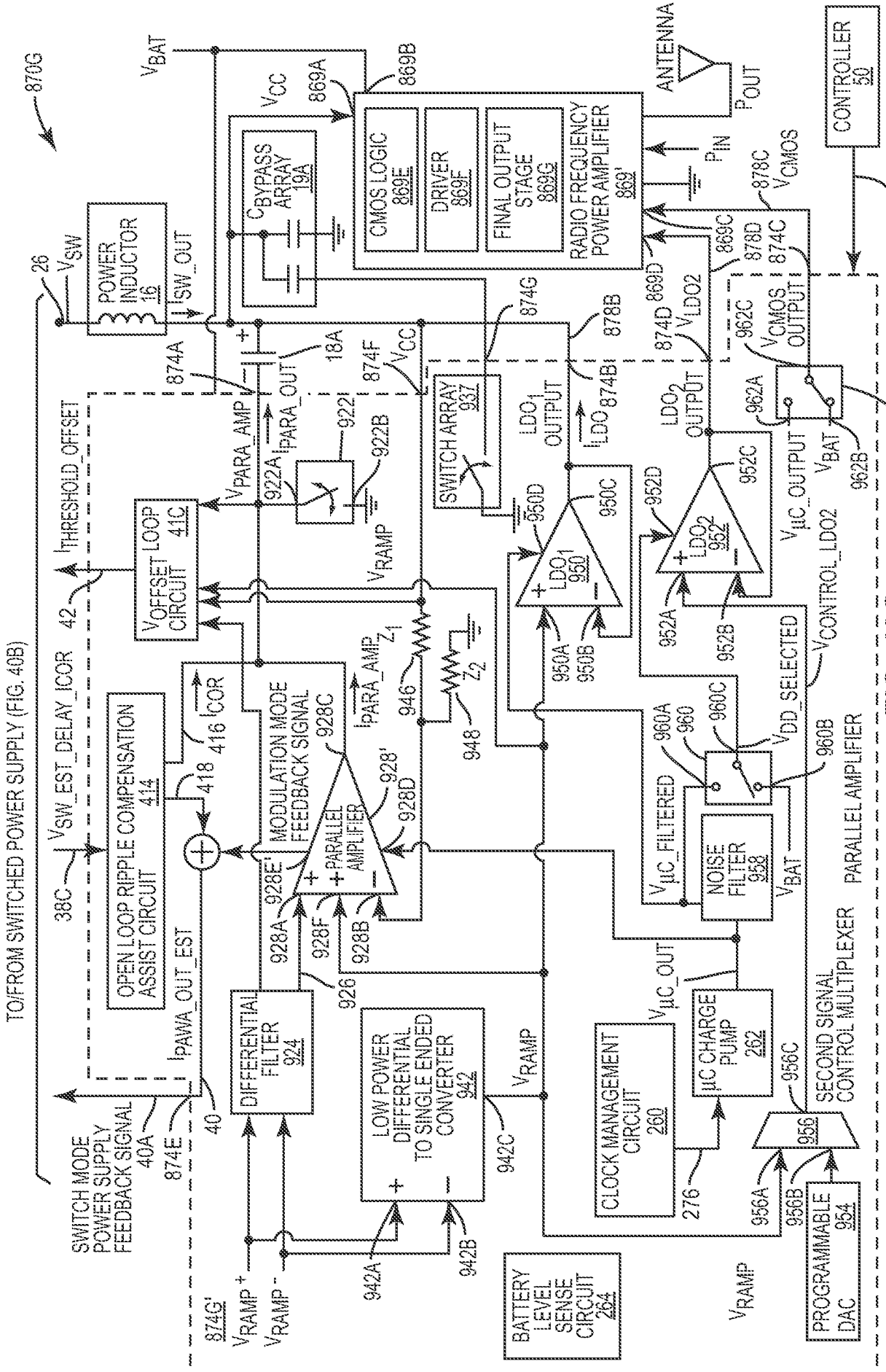

870G
TO/FROM SWITCHED POWER SUPPLY (FIG. 40B)
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL 40A
874E
40
$I_{PAWA_OUT_EST}$
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT 414
418
416 I_{COR}
$V_{SW_EST_DELAY_ICOR}$ 42
38C
V_{SW}
26
POWER INDUCTOR 16
I_{SW_OUT}
V_{BAT}
V_{CC}
869A
869B
C_{BYPASS} ARRAY 19A
CMOS LOGIC 869E
DRIVER 869F
FINAL OUTPUT STAGE 869G
RADIO FREQUENCY POWER AMPLIFIER 869'
ANTENNA
P_{IN}
P_{OUT}
CONTROLLER 50
44
$I_{THRESHOLD_OFFSET}$
V_{OFFSET} LOOP CIRCUIT 41C
874A
18A
I_{PARA_OUT}
V_{PARA_AMP}
922A
922
922B
V_{RAMP}
874F
V_{CC}
874G
SWITCH ARRAY 937
LDO_1 OUTPUT
I_{LDO} 874B
878B
874D
869D
V_{LDO2}
878D
874C
878C
V_{CMOS}
869C
LDO_2 OUTPUT
962C
V_{CMOS} OUTPUT
962A
962B
962
V_{BAT}
$V_{\mu C_OUTPUT}$
$V_{CONTROL_LDO2}$
LDO_1 950
950D
950C
950A
950B
LDO_2 952
952D
952C
952A
952B
$V_{DD_SELECTED}$
960B
960C
960A
960
$V_{\mu C_FILTERED}$
NOISE FILTER 958
V_{BAT}
PARALLEL AMPLIFIER
I_{PARA_AMP}
Z_1
946
Z_2
948
MODULATION MODE FEEDBACK SIGNAL 928C
928E'
928A
928F
928B
926
PARALLEL AMPLIFIER
928'
928D
DIFFERENTIAL FILTER 924
LOW POWER DIFFERENTIAL TO SINGLE ENDED CONVERTER 942
942A
942B
942C
V_{RAMP}
874G'
V_{RAMP} +
V_{RAMP} -
BATTERY LEVEL SENSE CIRCUIT 264
CLOCK MANAGEMENT CIRCUIT 260
$V_{\mu C_OUT}$
276
μC CHARGE PUMP 262
956C
956
956A
956B
SECOND SIGNAL CONTROL MULTIPLEXER
PROGRAMMABLE DAC 954

FIG. 46G

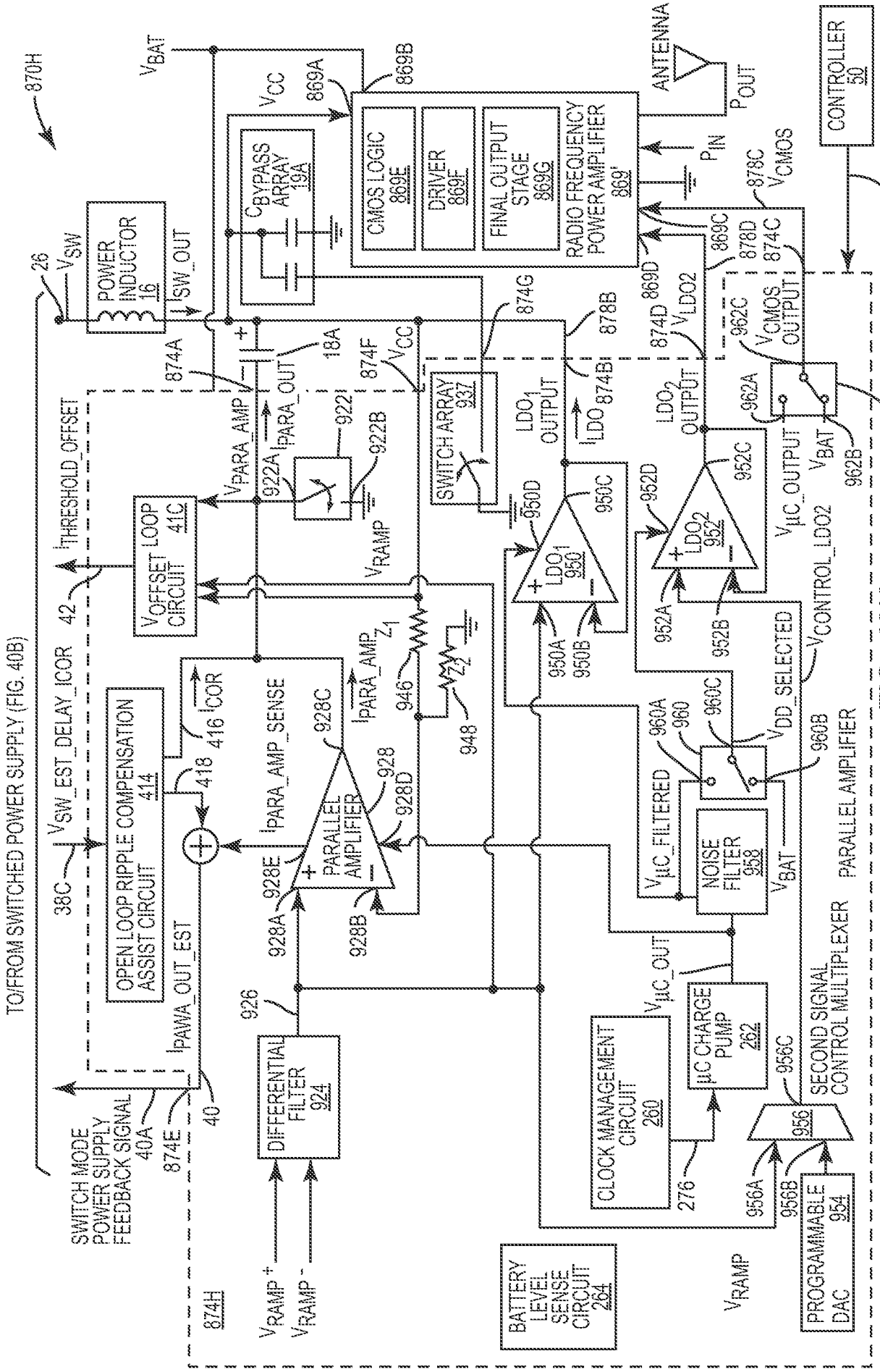

870H
TO/FROM SWITCHED POWER SUPPLY (FIG. 40B)
V_{BAT}
26
V_{SW}
POWER INDUCTOR 16
I_{SW_OUT}
C_{BYPASS} ARRAY 19A
V_{CC}
869A
869B
CMOS LOGIC 869E
DRIVER 869F
FINAL OUTPUT STAGE 869G
RADIO FREQUENCY POWER AMPLIFIER 869'
ANTENNA
P_{IN}
P_{OUT}
878C
V_{CMOS}
CONTROLLER 50
44
874A
I_{PARA_AMP}
18A
874F
V_{CC}
874G
878B
874D
869D
V_{LDO2}
869C
878D
874C
962C
V_{CMOS} OUTPUT
962A
962
962B
V_{BAT}
$V_{\mu C_OUTPUT}$
$V_{CONTROL_LDO2}$
LDO_2 OUTPUT
LDO_1 OUTPUT
I_{LDO} 874B
SWITCH ARRAY 937
922
922A
922B
I_{PARA_OUT}
V_{RAMP}
V_{OFFSET} LOOP CIRCUIT 41C
42
$I_{THRESHOLD_OFFSET}$
950D
950C
952D
952C
LDO_1 950
LDO_2 952
950A
950B
952A
952B
$V_{DD_SELECTED}$
960B
960C
960A
960
$V_{\mu C_FILTERED}$
NOISE FILTER 958
V_{BAT}
$V_{\mu C_OUT}$
I_{COR}
416
418
$I_{PARA_AMP_SENSE}$
928C
928
928D
928A
928B
926
I_{PARA_AMP}
Z_1
946
Z_2
948
OPEN LOOP RIPPLE COMPENSATION ASSIST CIRCUIT 414
$I_{PAWA_OUT_EST}$
40
874E
SWITCH MODE POWER SUPPLY FEEDBACK SIGNAL 40A
38C
$V_{SW_EST_DELAY_ICOR}$
DIFFERENTIAL FILTER 924
PARALLEL AMPLIFIER
CLOCK MANAGEMENT CIRCUIT 260
276
μC CHARGE PUMP 262
956C
956
SECOND SIGNAL CONTROL MULTIPLEXER
PARALLEL AMPLIFIER
956A
956B
PROGRAMMABLE DAC 954
874H
V_{RAMP} +
V_{RAMP} -
BATTERY LEVEL SENSE CIRCUIT 264

FIG. 46H

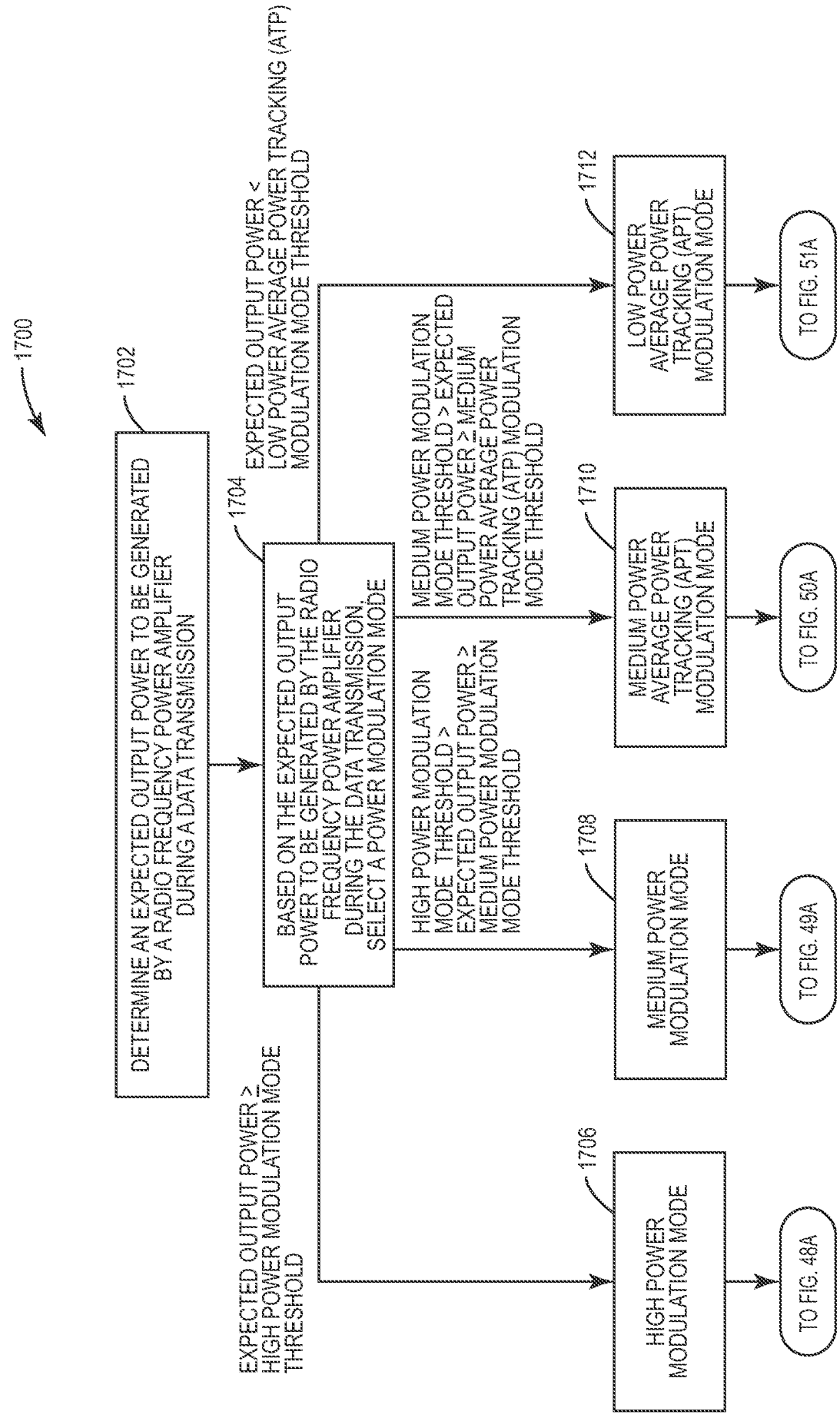

1700
1702
DETERMINE AN EXPECTED OUTPUT POWER TO BE GENERATED BY A RADIO FREQUENCY POWER AMPLIFIER DURING A DATA TRANSMISSION
1704
BASED ON THE EXPECTED OUTPUT POWER TO BE GENERATED BY THE RADIO FREQUENCY POWER AMPLIFIER DURING THE DATA TRANSMISSION, SELECT A POWER MODULATION MODE
EXPECTED OUTPUT POWER < LOW POWER AVERAGE POWER TRACKING (ATP) MODULATION MODE THRESHOLD
MEDIUM POWER MODULATION MODE THRESHOLD > EXPECTED OUTPUT POWER ≥ MEDIUM POWER AVERAGE POWER TRACKING (ATP) MODULATION MODE THRESHOLD
HIGH POWER MODULATION MODE THRESHOLD > EXPECTED OUTPUT POWER ≥ MEDIUM POWER MODULATION MODE THRESHOLD
EXPECTED OUTPUT POWER ≥ HIGH POWER MODULATION MODE THRESHOLD
1706
HIGH POWER MODULATION MODE
1708
MEDIUM POWER MODULATION MODE
1710
MEDIUM POWER AVERAGE POWER TRACKING (APT) MODULATION MODE
1712
LOW POWER AVERAGE POWER TRACKING (APT) MODULATION MODE
TO FIG. 48A
TO FIG. 49A
TO FIG. 50A
TO FIG. 51A

FIG. 47

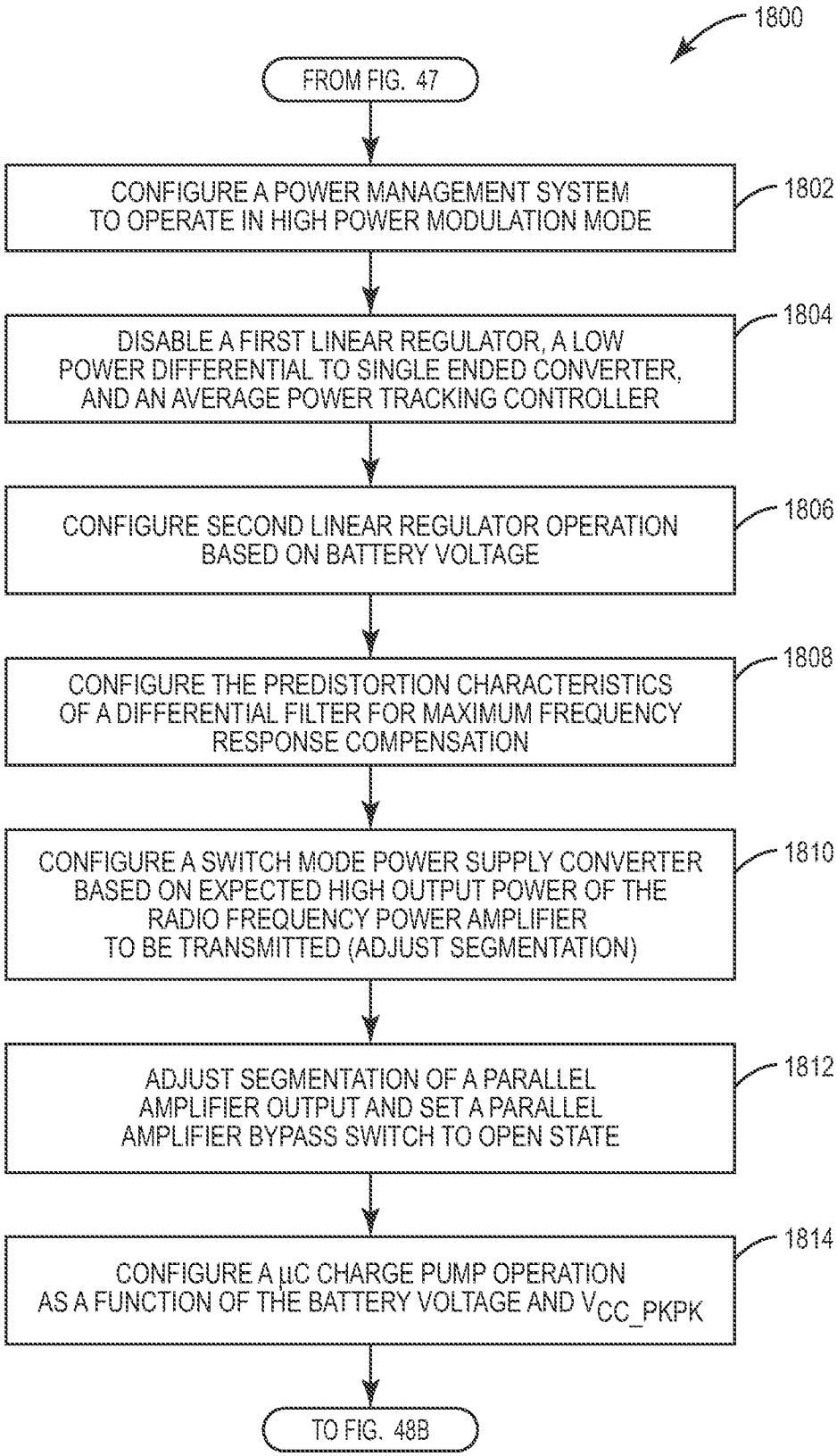

1800
FROM FIG. 47
CONFIGURE A POWER MANAGEMENT SYSTEM TO OPERATE IN HIGH POWER MODULATION MODE
1802
DISABLE A FIRST LINEAR REGULATOR, A LOW POWER DIFFERENTIAL TO SINGLE ENDED CONVERTER, AND AN AVERAGE POWER TRACKING CONTROLLER
1804
CONFIGURE SECOND LINEAR REGULATOR OPERATION BASED ON BATTERY VOLTAGE
1806
CONFIGURE THE PREDISTORTION CHARACTERISTICS OF A DIFFERENTIAL FILTER FOR MAXIMUM FREQUENCY RESPONSE COMPENSATION
1808
CONFIGURE A SWITCH MODE POWER SUPPLY CONVERTER BASED ON EXPECTED HIGH OUTPUT POWER OF THE RADIO FREQUENCY POWER AMPLIFIER TO BE TRANSMITTED (ADJUST SEGMENTATION)
1810
ADJUST SEGMENTATION OF A PARALLEL AMPLIFIER OUTPUT AND SET A PARALLEL AMPLIFIER BYPASS SWITCH TO OPEN STATE
1812
CONFIGURE A µC CHARGE PUMP OPERATION AS A FUNCTION OF THE BATTERY VOLTAGE AND V_{CC_PKPK}
1814
TO FIG. 48B

FIG. 48A

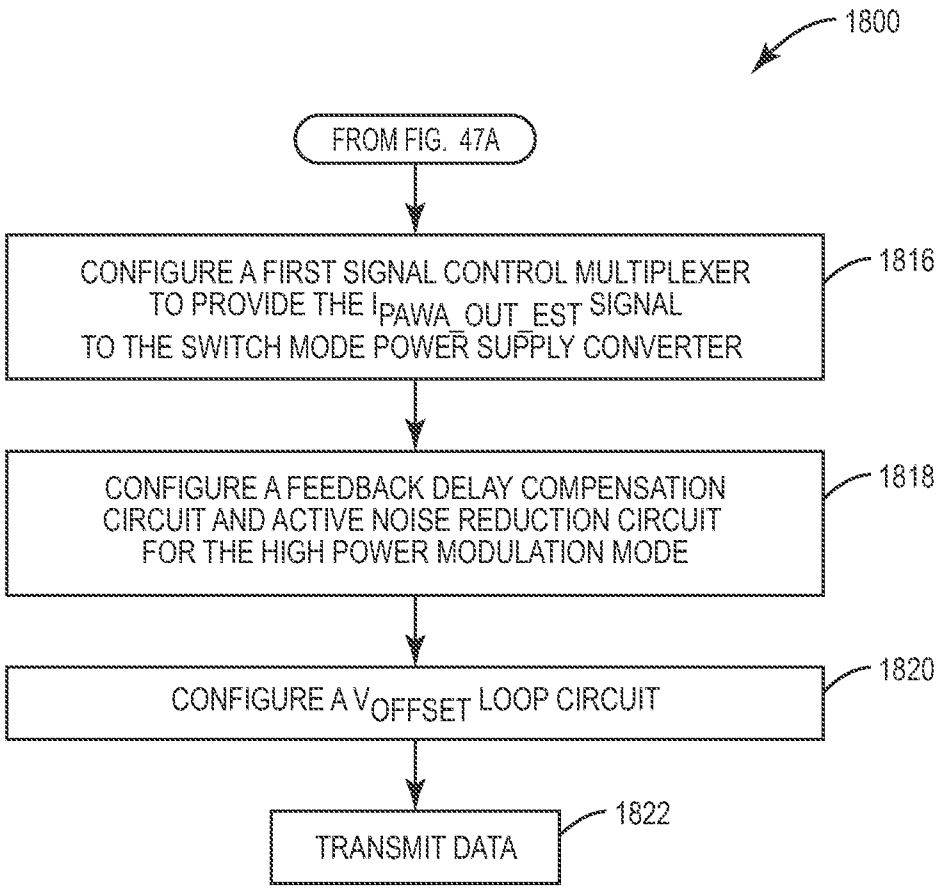

1800
FROM FIG. 47A
CONFIGURE A FIRST SIGNAL CONTROL MULTIPLEXER TO PROVIDE THE $I_{PAWA_OUT_EST}$ SIGNAL TO THE SWITCH MODE POWER SUPPLY CONVERTER
1816
CONFIGURE A FEEDBACK DELAY COMPENSATION CIRCUIT AND ACTIVE NOISE REDUCTION CIRCUIT FOR THE HIGH POWER MODULATION MODE
1818
CONFIGURE A V_{OFFSET} LOOP CIRCUIT
1820
TRANSMIT DATA
1822

FIG. 48B

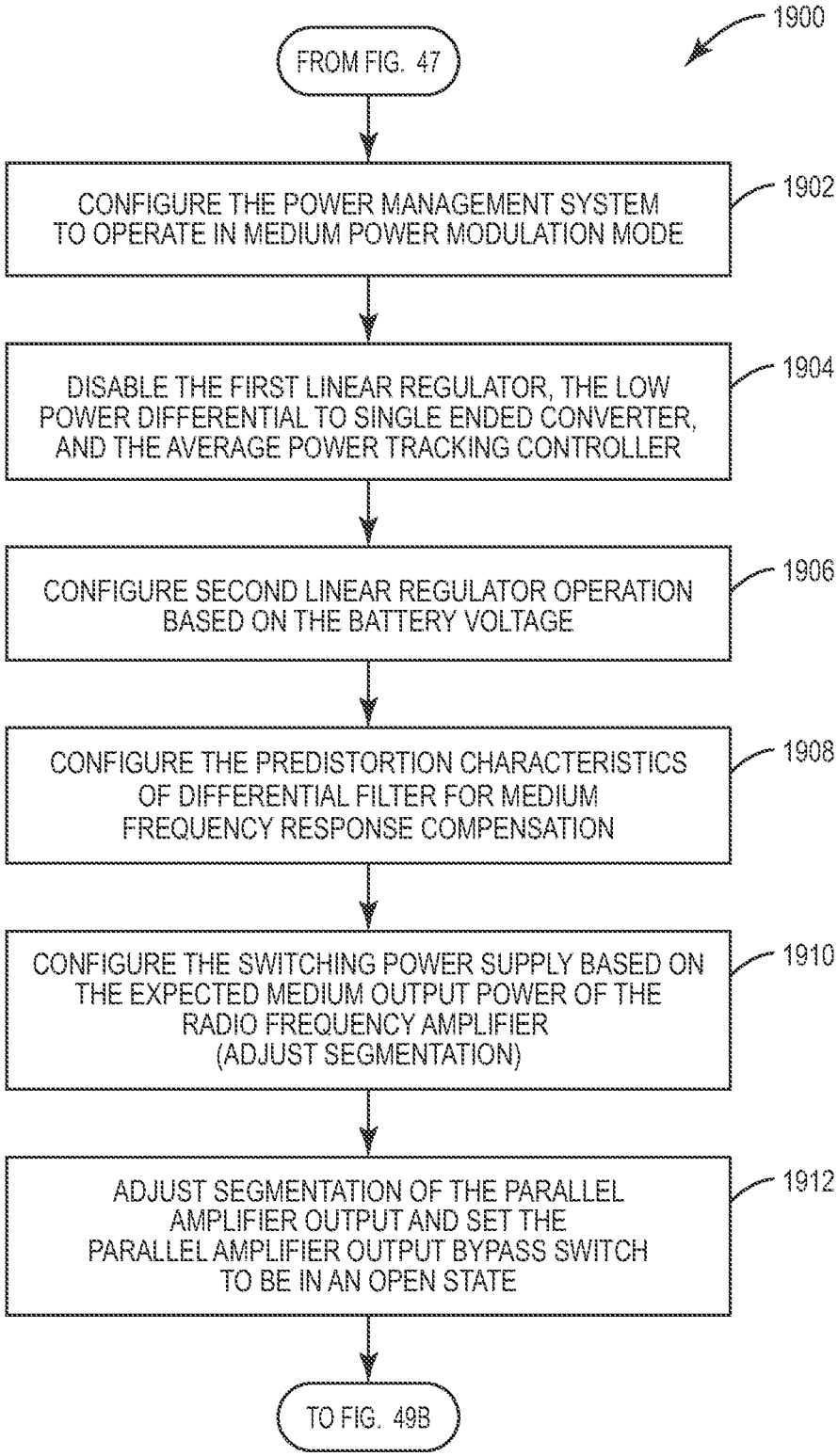

1900
FROM FIG. 47
CONFIGURE THE POWER MANAGEMENT SYSTEM TO OPERATE IN MEDIUM POWER MODULATION MODE
1902
DISABLE THE FIRST LINEAR REGULATOR, THE LOW POWER DIFFERENTIAL TO SINGLE ENDED CONVERTER, AND THE AVERAGE POWER TRACKING CONTROLLER
1904
CONFIGURE SECOND LINEAR REGULATOR OPERATION BASED ON THE BATTERY VOLTAGE
1906
CONFIGURE THE PREDISTORTION CHARACTERISTICS OF DIFFERENTIAL FILTER FOR MEDIUM FREQUENCY RESPONSE COMPENSATION
1908
CONFIGURE THE SWITCHING POWER SUPPLY BASED ON THE EXPECTED MEDIUM OUTPUT POWER OF THE RADIO FREQUENCY AMPLIFIER (ADJUST SEGMENTATION)
1910
ADJUST SEGMENTATION OF THE PARALLEL AMPLIFIER OUTPUT AND SET THE PARALLEL AMPLIFIER OUTPUT BYPASS SWITCH TO BE IN AN OPEN STATE
1912
TO FIG. 49B

FIG. 49A

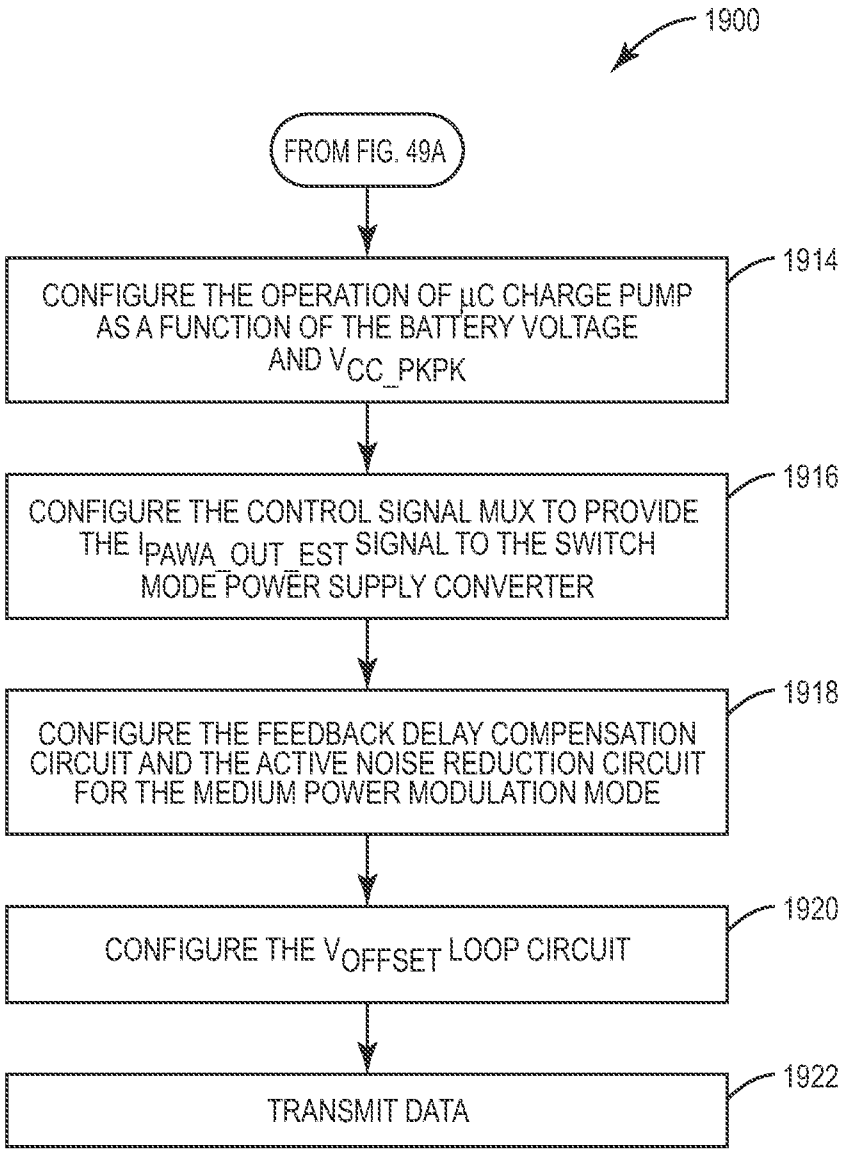

1900
FROM FIG. 49A
CONFIGURE THE OPERATION OF µC CHARGE PUMP AS A FUNCTION OF THE BATTERY VOLTAGE AND V_{CC_PKPK}
1914
CONFIGURE THE CONTROL SIGNAL MUX TO PROVIDE THE $I_{PAWA_OUT_EST}$ SIGNAL TO THE SWITCH MODE POWER SUPPLY CONVERTER
1916
CONFIGURE THE FEEDBACK DELAY COMPENSATION CIRCUIT AND THE ACTIVE NOISE REDUCTION CIRCUIT FOR THE MEDIUM POWER MODULATION MODE
1918
CONFIGURE THE V_{OFFSET} LOOP CIRCUIT
1920
TRANSMIT DATA
1922

FIG. 49B

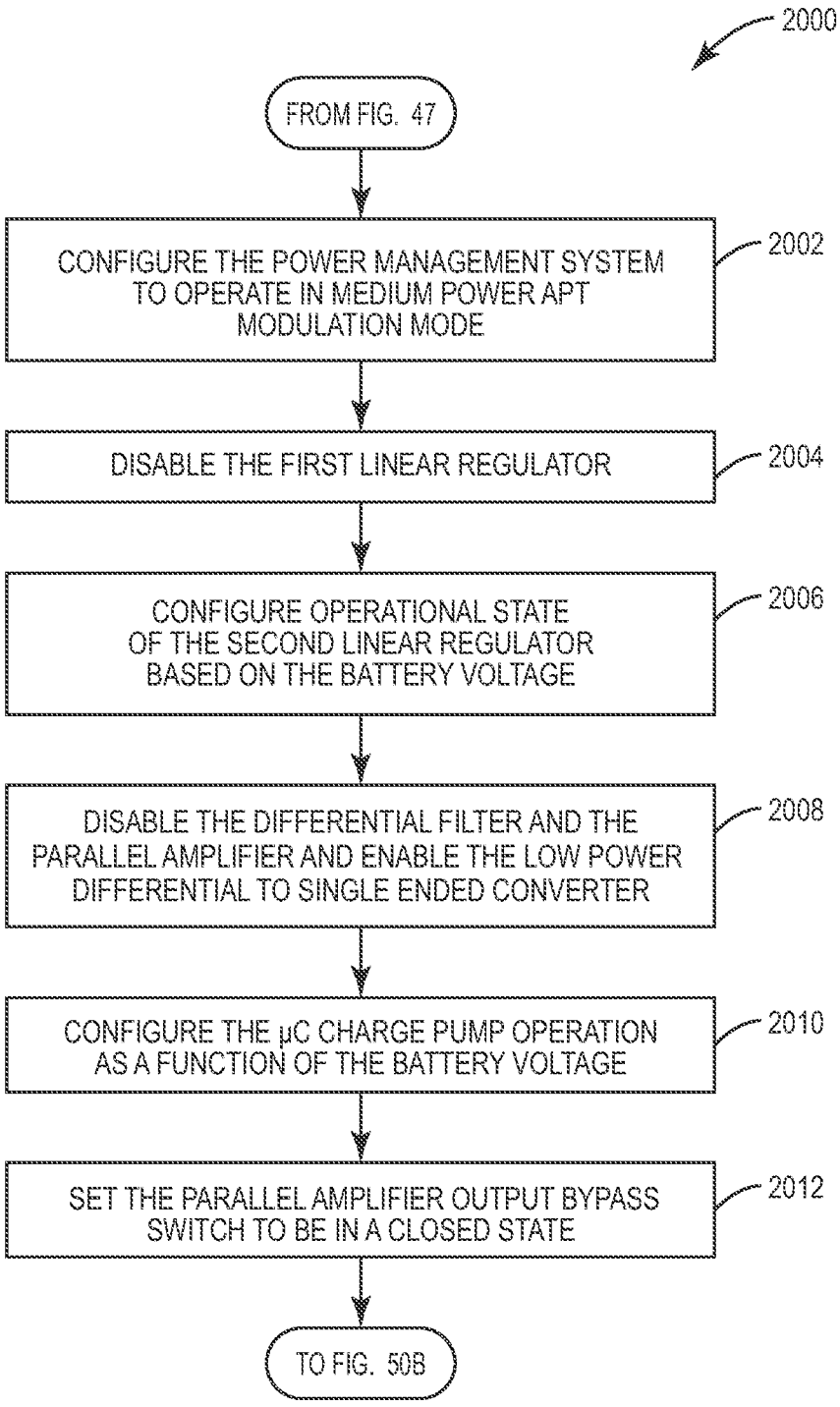

2000
FROM FIG. 47
CONFIGURE THE POWER MANAGEMENT SYSTEM TO OPERATE IN MEDIUM POWER APT MODULATION MODE
2002
DISABLE THE FIRST LINEAR REGULATOR
2004
CONFIGURE OPERATIONAL STATE OF THE SECOND LINEAR REGULATOR BASED ON THE BATTERY VOLTAGE
2006
DISABLE THE DIFFERENTIAL FILTER AND THE PARALLEL AMPLIFIER AND ENABLE THE LOW POWER DIFFERENTIAL TO SINGLE ENDED CONVERTER
2008
CONFIGURE THE μC CHARGE PUMP OPERATION AS A FUNCTION OF THE BATTERY VOLTAGE
2010
SET THE PARALLEL AMPLIFIER OUTPUT BYPASS SWITCH TO BE IN A CLOSED STATE
2012
TO FIG. 50B

FIG. 50A

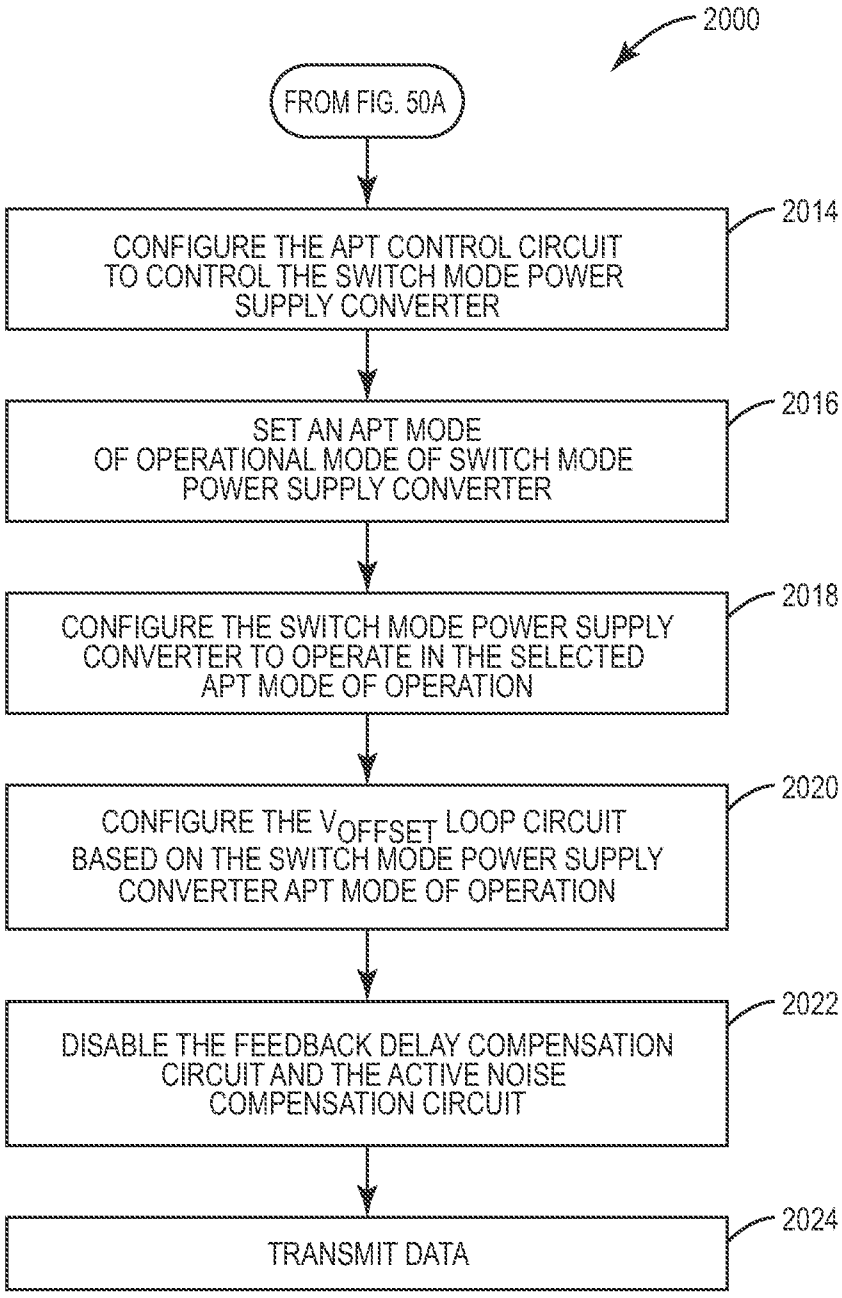

2000
FROM FIG. 50A
CONFIGURE THE APT CONTROL CIRCUIT TO CONTROL THE SWITCH MODE POWER SUPPLY CONVERTER
2014
SET AN APT MODE OF OPERATIONAL MODE OF SWITCH MODE POWER SUPPLY CONVERTER
2016
CONFIGURE THE SWITCH MODE POWER SUPPLY CONVERTER TO OPERATE IN THE SELECTED APT MODE OF OPERATION
2018
CONFIGURE THE V_{OFFSET} LOOP CIRCUIT BASED ON THE SWITCH MODE POWER SUPPLY CONVERTER APT MODE OF OPERATION
2020
DISABLE THE FEEDBACK DELAY COMPENSATION CIRCUIT AND THE ACTIVE NOISE COMPENSATION CIRCUIT
2022
TRANSMIT DATA
2024

FIG. 50B

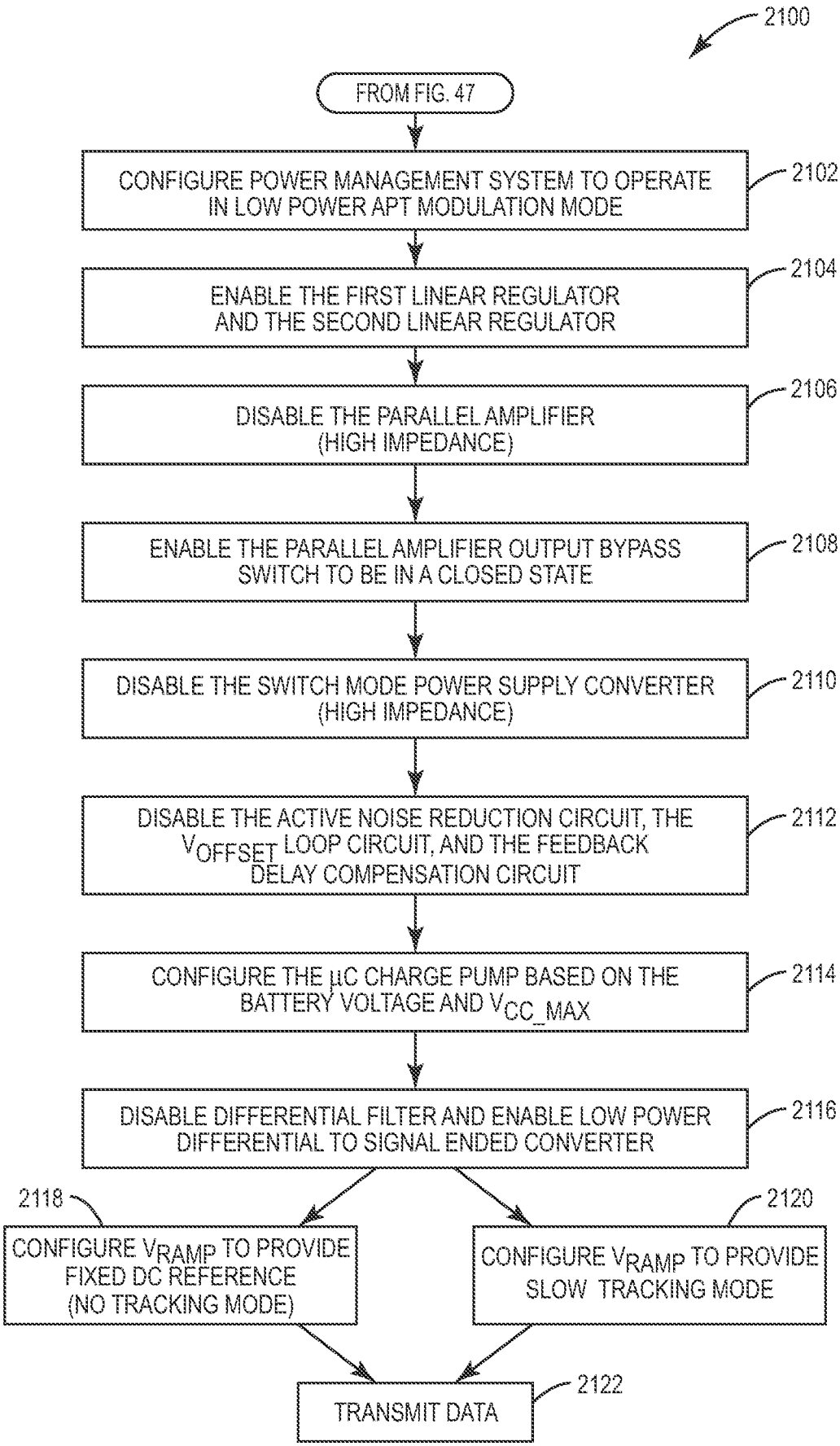

2100
FROM FIG. 47
CONFIGURE POWER MANAGEMENT SYSTEM TO OPERATE IN LOW POWER APT MODULATION MODE
2102
ENABLE THE FIRST LINEAR REGULATOR AND THE SECOND LINEAR REGULATOR
2104
DISABLE THE PARALLEL AMPLIFIER (HIGH IMPEDANCE)
2106
ENABLE THE PARALLEL AMPLIFIER OUTPUT BYPASS SWITCH TO BE IN A CLOSED STATE
2108
DISABLE THE SWITCH MODE POWER SUPPLY CONVERTER (HIGH IMPEDANCE)
2110
DISABLE THE ACTIVE NOISE REDUCTION CIRCUIT, THE V_{OFFSET} LOOP CIRCUIT, AND THE FEEDBACK DELAY COMPENSATION CIRCUIT
2112
CONFIGURE THE µC CHARGE PUMP BASED ON THE BATTERY VOLTAGE AND V_{CC_MAX}
2114
DISABLE DIFFERENTIAL FILTER AND ENABLE LOW POWER DIFFERENTIAL TO SIGNAL ENDED CONVERTER
2116
2118
CONFIGURE V_{RAMP} TO PROVIDE FIXED DC REFERENCE (NO TRACKING MODE)
2120
CONFIGURE V_{RAMP} TO PROVIDE SLOW TRACKING MODE
TRANSMIT DATA
2122

FIG. 51

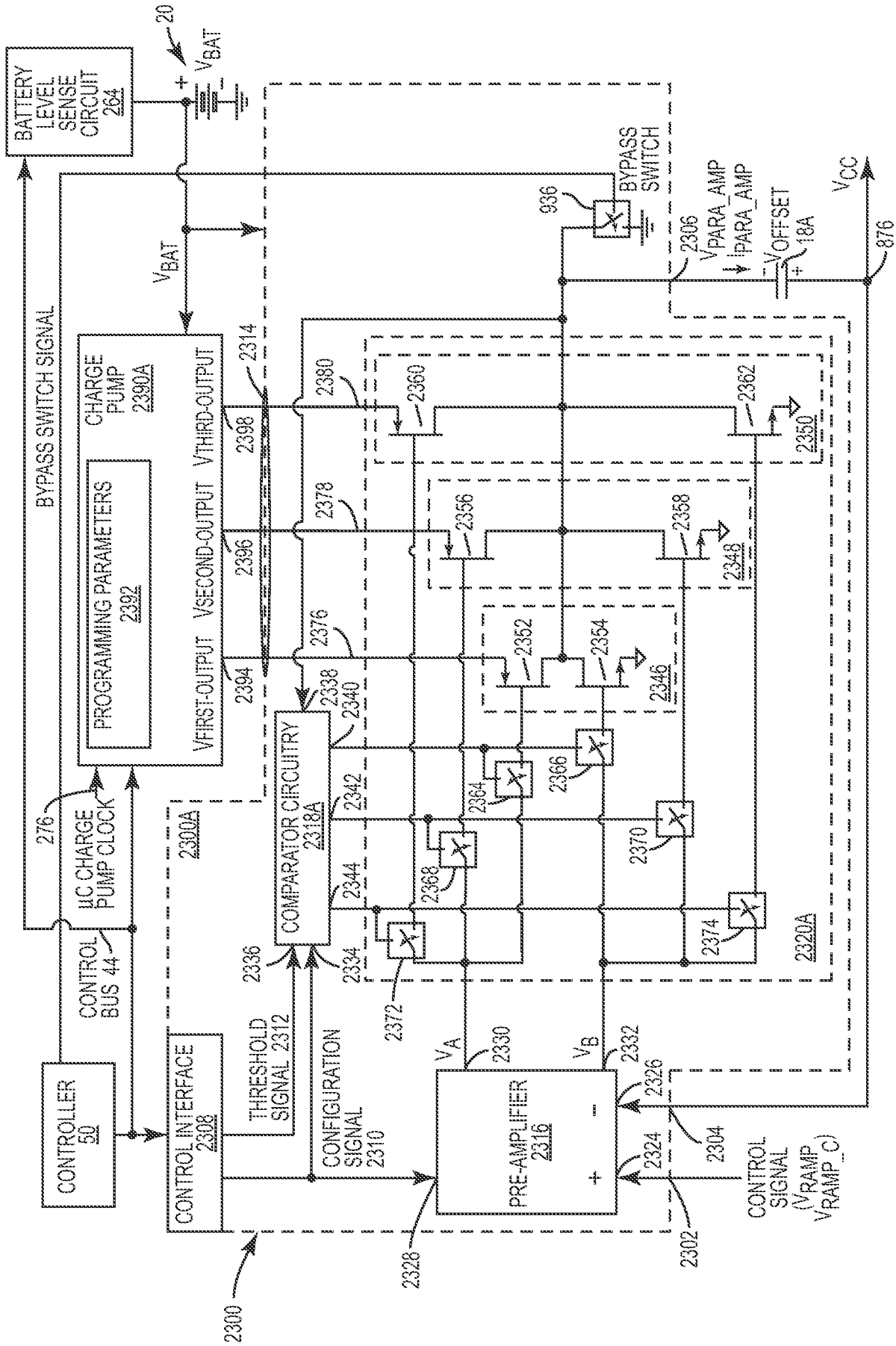

BATTERY LEVEL SENSE CIRCUIT 264
20
V_{BAT}
BYPASS SWITCH SIGNAL
CHARGE PUMP 2390A
PROGRAMMING PARAMETERS 2392
$V_{FIRST-OUTPUT}$ $V_{SECOND-OUTPUT}$ $V_{THIRD-OUTPUT}$
2314
2398
2396
2394
2380
2378
2376
2360
2362
2350
2356
2358
2348
2352
2354
2346
2366
2364
2370
2368
2374
2320A
936
BYPASS SWITCH
2306
V_{PARA_AMP}
I_{PARA_AMP}
V_{OFFSET}
18A
V_{CC}
876
276
μC CHARGE PUMP CLOCK
2390A
CONTROL BUS 44
CONTROLLER 50
CONTROL INTERFACE 2308
THRESHOLD SIGNAL 2312
CONFIGURATION SIGNAL 2310
COMPARATOR CIRCUITRY 2318A
2336
2338
2340
2342
2344
2334
2372
V_A
2330
V_B
2332
PRE-AMPLIFIER 2316
2326
2324
2304
2302
2328
2300
CONTROL SIGNAL (V_{RAMP}, V_{RAMP_C})

FIG. 52A

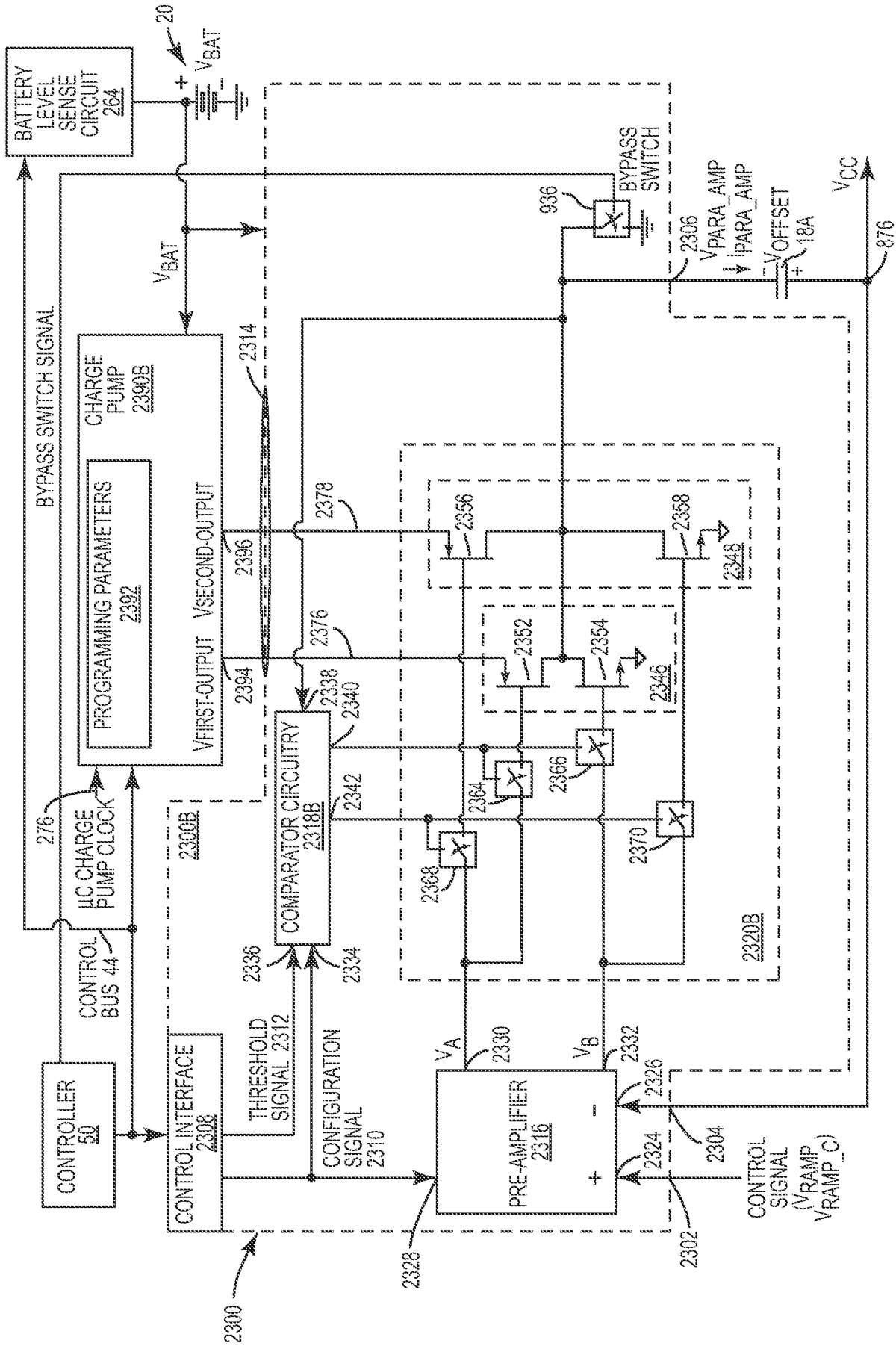

BATTERY LEVEL SENSE CIRCUIT 264
20
V_{BAT}
BYPASS SWITCH SIGNAL
CHARGE PUMP 2390B
PROGRAMMING PARAMETERS 2392
$V_{FIRST-OUTPUT}$ $V_{SECOND-OUTPUT}$
2314
2396
2378
2356
2358
2348
2376
2352
2354
2346
2394
2338
2340
2342
2366
2364
2368
2370
276
µC CHARGE PUMP CLOCK
2390B
CONTROL BUS 44
COMPARATOR CIRCUITRY 2318B
2336
2334
2320B
CONTROLLER 50
CONTROL INTERFACE 2308
THRESHOLD SIGNAL 2312
CONFIGURATION SIGNAL 2310
V_A
2330
V_B
2332
PRE-AMPLIFIER 2316
2326
2324
2304
2328
2302
2300
CONTROL SIGNAL (V_{RAMP}, V_{RAMP_C})
936
BYPASS SWITCH
2306
V_{PARA_AMP}
I_{PARA_AMP}
V_{OFFSET}
18A
V_{CC}
876

FIG. 52B

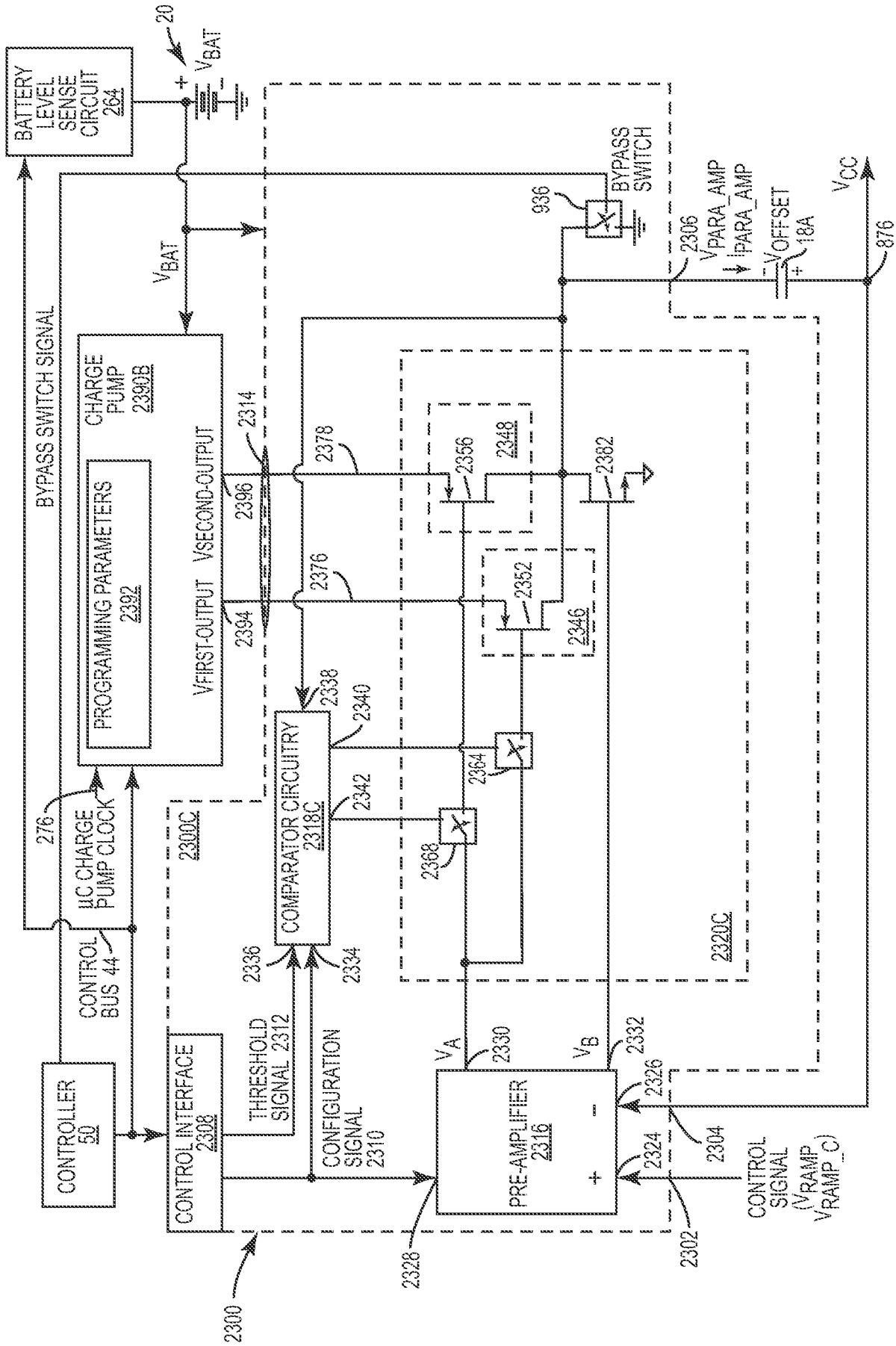

BATTERY LEVEL SENSE CIRCUIT 264
20
V_{BAT}
BYPASS SWITCH SIGNAL
CHARGE PUMP 2390B
PROGRAMMING PARAMETERS 2392
$V_{FIRST-OUTPUT}$ $V_{SECOND-OUTPUT}$
2314
2396
2378
2356
2348
2382
2376
2352
2394
2346
2338
2340
2364
2342
2368
2336
2334
COMPARATOR CIRCUITRY 2318C
2300C
276
µC CHARGE PUMP CLOCK
CONTROL BUS 44
CONTROLLER 50
CONTROL INTERFACE 2308
THRESHOLD SIGNAL 2312
CONFIGURATION SIGNAL 2310
V_A
2330
V_B
2332
PRE-AMPLIFIER 2316
2326
2324
2304
2328
2300
2302
2320C
936
BYPASS SWITCH
2306
V_{PARA_AMP}
I_{PARA_AMP}
V_{OFFSET}
18A
V_{CC}
876
CONTROL SIGNAL (V_{RAMP}, V_{RAMP_C})

FIG. 52C

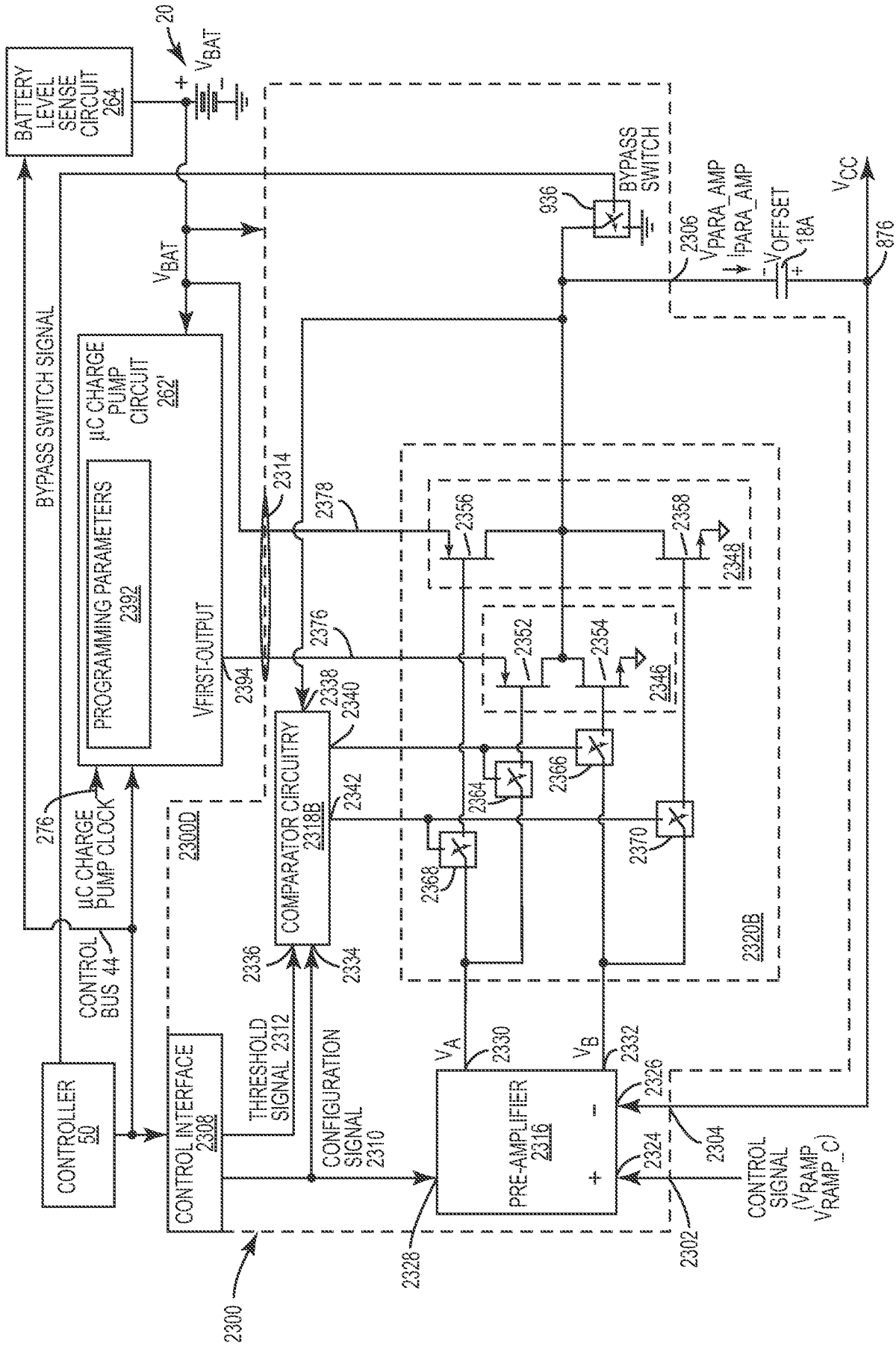

BATTERY LEVEL SENSE CIRCUIT 264
20
VBAT
BYPASS SWITCH SIGNAL
μC CHARGE PUMP CIRCUIT 262'
PROGRAMMING PARAMETERS 2392
VFIRST-OUTPUT
2314
2378
2356
2358
2348
2376
2352
2354
2346
2338
2340
2342
2366
2364
2368
2370
2320B
276
μC CHARGE PUMP CLOCK
2300D
COMPARATOR CIRCUITRY 2318B
2336
2334
CONTROL BUS 44
CONTROLLER 50
CONTROL INTERFACE 2308
THRESHOLD SIGNAL 2312
CONFIGURATION SIGNAL 2310
VA
2330
VB
2332
PRE-AMPLIFIER 2316
2326
2324
2304
2328
2302
2300
CONTROL SIGNAL (VRAMP, VRAMP_C)
936
BYPASS SWITCH
2306
VPARA_AMP
IPARA_AMP
VOFFSET
18A
VCC
876

FIG. 52D

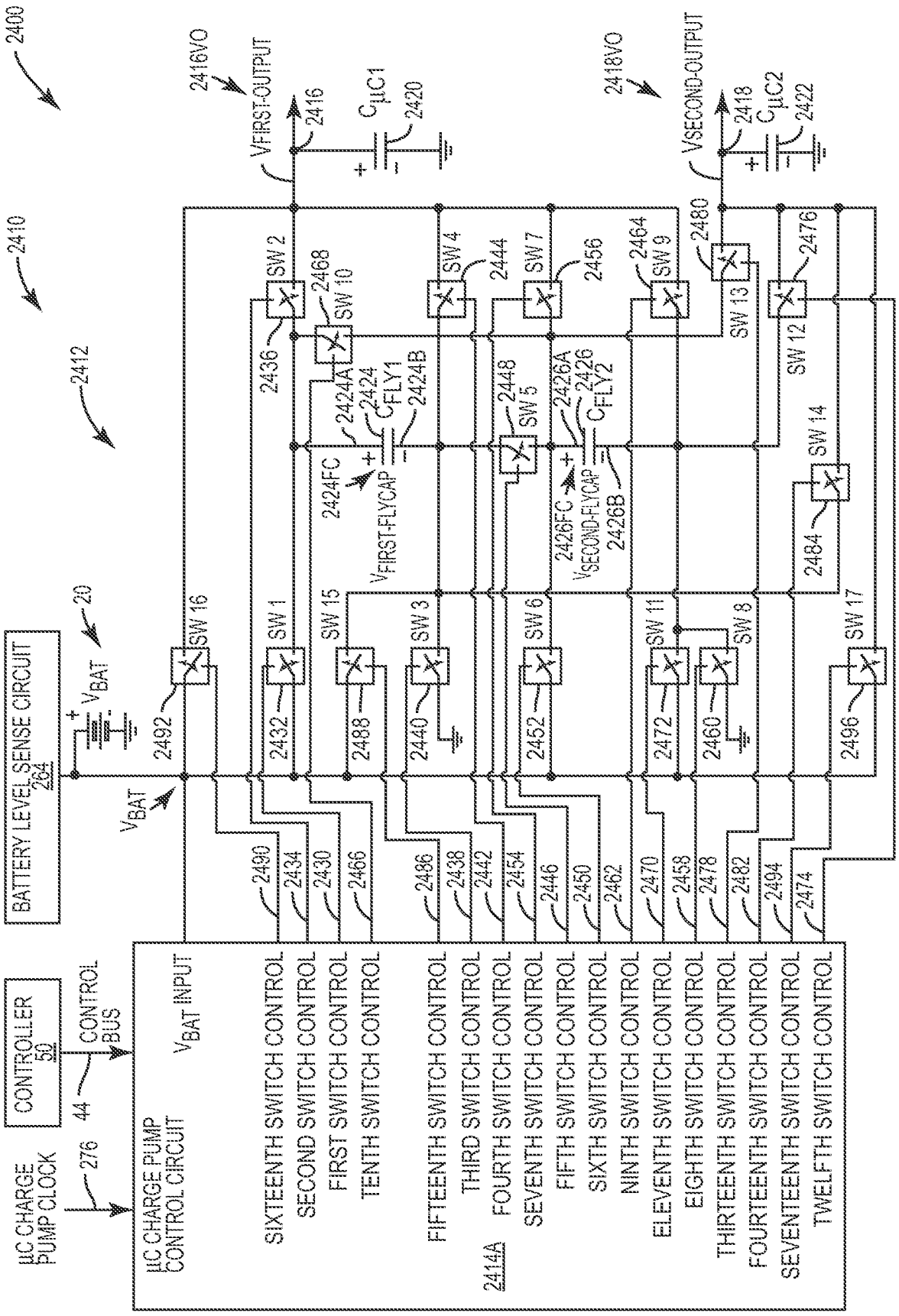

2400
2410
2412
2414A
2416VO
VFIRST-OUTPUT
2416
CμC1
2420
2418VO
VSECOND-OUTPUT
2418
CμC2
2422
BATTERY LEVEL SENSE CIRCUIT 264
20
VBAT
2492
SW 16
SW 1
SW 15
SW 3
SW 6
SW 11
SW 8
SW 17
SW 2
SW 10
SW 4
SW 7
SW 9
SW 13
SW 12
SW 14
2424FC
VFIRST-FLYCAP
2424A
2424
CFLY1
2424B
2426FC
VSECOND-FLYCAP
2426A
2426
CFLY2
2426B
2436
2448
2444
2456
2464
2480
2476
2484
2496
2432
2488
2440
2452
2472
2460
2468
μC CHARGE PUMP CLOCK
276
CONTROLLER 50
44
CONTROL BUS
μC CHARGE PUMP CONTROL CIRCUIT
VBAT INPUT
SIXTEENTH SWITCH CONTROL
SECOND SWITCH CONTROL
FIRST SWITCH CONTROL
TENTH SWITCH CONTROL
FIFTEENTH SWITCH CONTROL
THIRD SWITCH CONTROL
FOURTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
FIFTH SWITCH CONTROL
SIXTH SWITCH CONTROL
NINTH SWITCH CONTROL
ELEVENTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
THIRTEENTH SWITCH CONTROL
FOURTEENTH SWITCH CONTROL
SEVENTEENTH SWITCH CONTROL
TWELFTH SWITCH CONTROL
2490
2434
2430
2466
2486
2438
2442
2454
2446
2450
2462
2470
2458
2478
2482
2494
2474

FIG. 53A

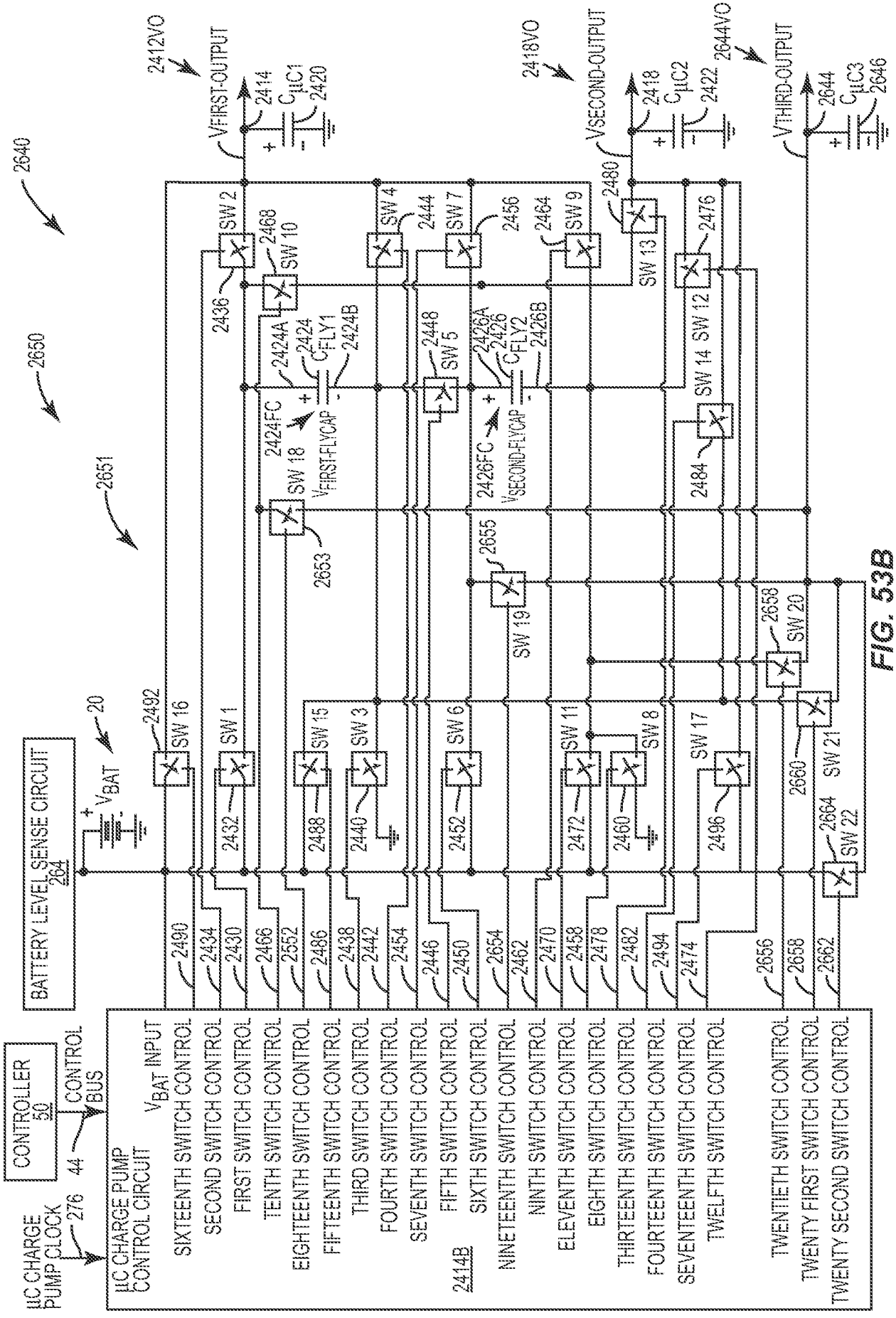

μC CHARGE PUMP CLOCK
276
CONTROLLER 50
44
CONTROL BUS
μC CHARGE PUMP CONTROL CIRCUIT
2414B
BATTERY LEVEL SENSE CIRCUIT 264
20
V_{BAT}
V_{BAT} INPUT
SIXTEENTH SWITCH CONTROL
SECOND SWITCH CONTROL
FIRST SWITCH CONTROL
TENTH SWITCH CONTROL
EIGHTEENTH SWITCH CONTROL
FIFTEENTH SWITCH CONTROL
THIRD SWITCH CONTROL
FOURTH SWITCH CONTROL
SEVENTH SWITCH CONTROL
FIFTH SWITCH CONTROL
SIXTH SWITCH CONTROL
NINETEENTH SWITCH CONTROL
NINTH SWITCH CONTROL
ELEVENTH SWITCH CONTROL
EIGHTH SWITCH CONTROL
THIRTEENTH SWITCH CONTROL
FOURTEENTH SWITCH CONTROL
SEVENTEENTH SWITCH CONTROL
TWELFTH SWITCH CONTROL
TWENTIETH SWITCH CONTROL
TWENTY FIRST SWITCH CONTROL
TWENTY SECOND SWITCH CONTROL
2490
2434
2430
2466
2552
2486
2438
2442
2454
2446
2450
2654
2462
2470
2458
2478
2482
2494
2474
2656
2658
2662
2492
SW 16
SW 1
SW 15
SW 3
SW 6
SW 19
SW 11
SW 8
SW 17
SW 20
SW 21
SW 22
2432
2488
2440
2452
2655
2472
2460
2496
2660
2664
2651
2650
2640
2653
SW 18
2424FC
$V_{FIRST-FLYCAP}$
2424A
2424
C_{FLY1}
2424B
2426FC
$V_{SECOND-FLYCAP}$
2426A
2426
C_{FLY2}
2426B
2436
SW 2
SW 10
2468
SW 4
2444
SW 5
2448
SW 7
2456
SW 9
2464
SW 13
2480
SW 12
2476
SW 14
2484
2412VO
$V_{FIRST-OUTPUT}$
2414
$C_{\mu C1}$
2420
2418VO
$V_{SECOND-OUTPUT}$
2418
$C_{\mu C2}$
2422
2644VO
$V_{THIRD-OUTPUT}$
2644
$C_{\mu C3}$
2646

FIG. 53B

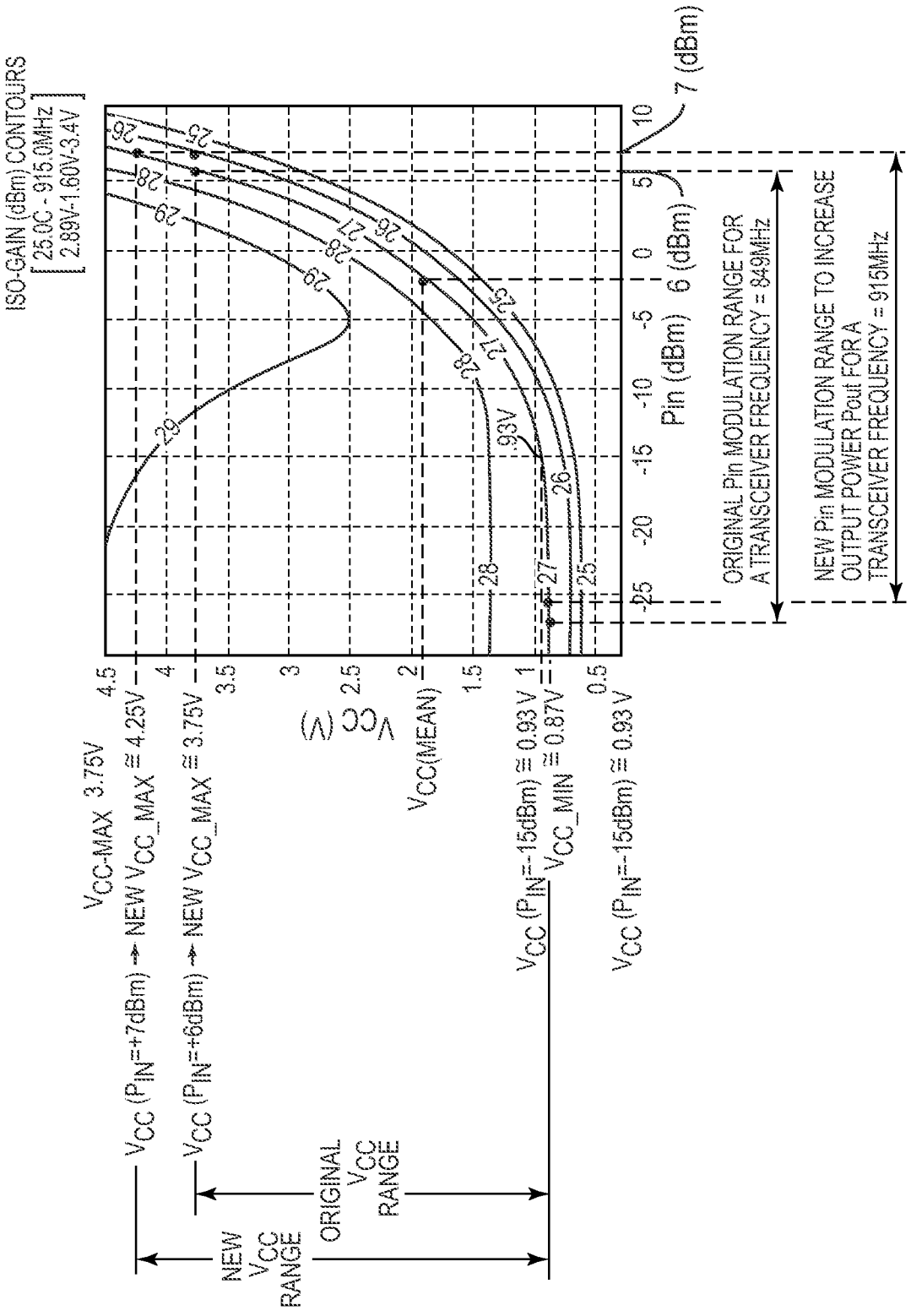

ISO-GAIN (dBm) CONTOURS
[25.0C - 915.0MHz
2.89V-1.60V-3.4V]
Pin (dBm)
7 (dBm)
6 (dBm)
ORIGINAL Pin MODULATION RANGE FOR A TRANSCEIVER FREQUENCY = 849MHz
NEW Pin MODULATION RANGE TO INCREASE OUTPUT POWER Pout FOR A TRANSCEIVER FREQUENCY = 915MHz
VCC (V)
VCC(MEAN)
VCC-MAX 3.75V
VCC (PIN=+7dBm) → NEW VCC_MAX ≅ 4.25V
VCC (PIN=+6dBm) → NEW VCC_MAX ≅ 3.75V
VCC (PIN=-15dBm) ≅ 0.93 V
VCC_MIN ≅ 0.87V
VCC (PIN=-15dBm) ≅ 0.93 V
NEW VCC RANGE
ORIGINAL VCC RANGE

FIG. 54

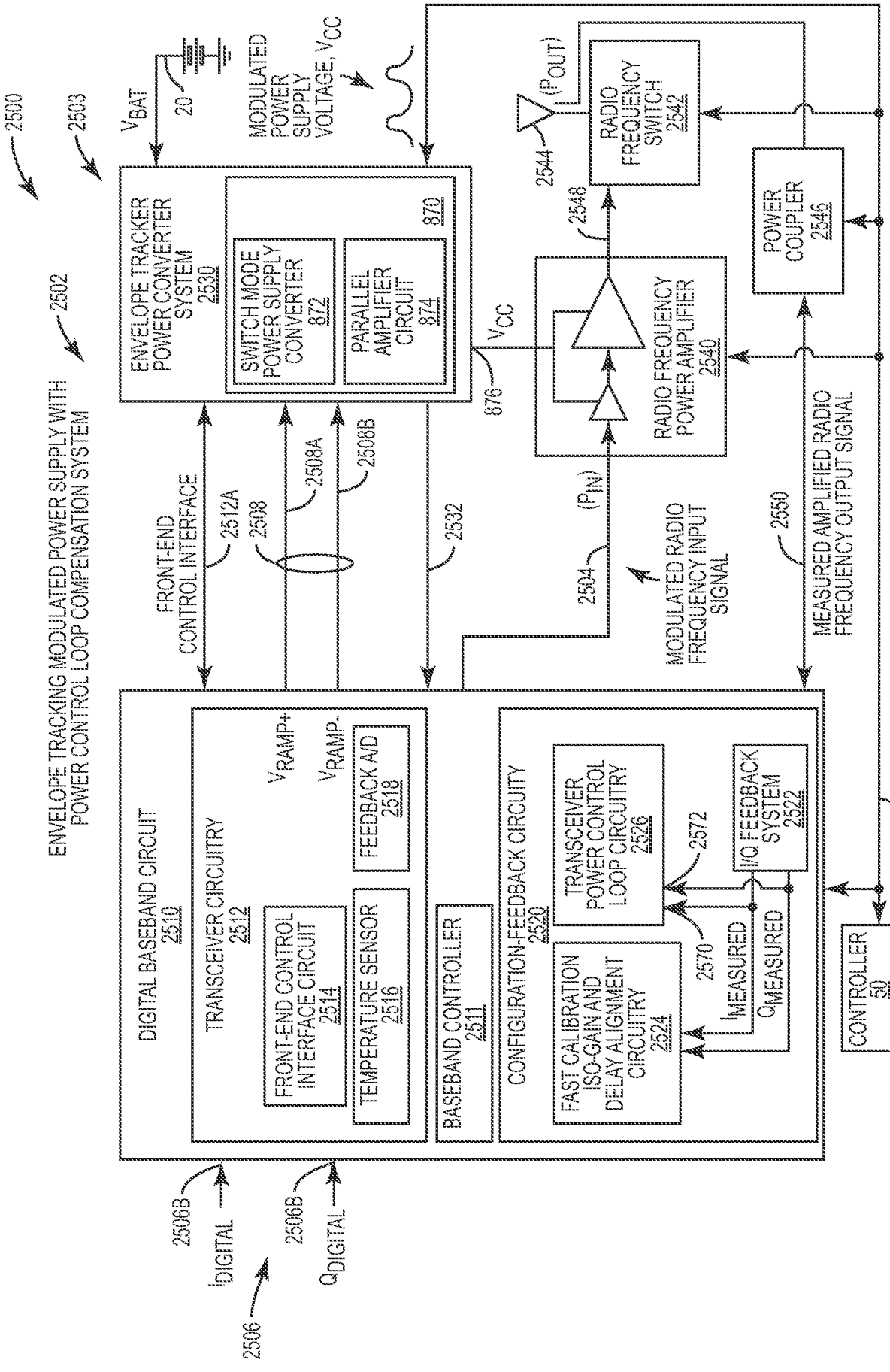

2500
2503
2502
ENVELOPE TRACKING MODULATED POWER SUPPLY WITH POWER CONTROL LOOP COMPENSATION SYSTEM
V_{BAT}
20
MODULATED POWER SUPPLY VOLTAGE, V_{CC}
ENVELOPE TRACKER POWER CONVERTER SYSTEM 2530
SWITCH MODE POWER SUPPLY CONVERTER 872
PARALLEL AMPLIFIER CIRCUIT 874
870
V_{CC}
876
FRONT-END CONTROL INTERFACE
2512A
2508
2508A
2508B
2532
2504
(P_{IN})
MODULATED RADIO FREQUENCY INPUT SIGNAL
RADIO FREQUENCY POWER AMPLIFIER 2540
2548
2544
(P_{OUT})
RADIO FREQUENCY SWITCH 2542
POWER COUPLER 2546
2550
MEASURED AMPLIFIED RADIO FREQUENCY OUTPUT SIGNAL
DIGITAL BASEBAND CIRCUIT 2510
TRANSCEIVER CIRCUITRY 2512
FRONT-END CONTROL INTERFACE CIRCUIT 2514
TEMPERATURE SENSOR 2516
V_{RAMP+}
V_{RAMP-}
FEEDBACK A/D 2518
BASEBAND CONTROLLER 2511
CONFIGURATION-FEEDBACK CIRCUITY 2520
FAST CALIBRATION ISO-GAIN AND DELAY ALIGNMENT CIRCUITRY 2524
TRANSCEIVER POWER CONTROL LOOP CIRCUITRY 2526
2572
2570
$I_{MEASURED}$
$Q_{MEASURED}$
I/Q FEEDBACK SYSTEM 2522
CONTROLLER 50
44
2506
2506B
$I_{DIGITAL}$
2506B
$Q_{DIGITAL}$

FIG. 55

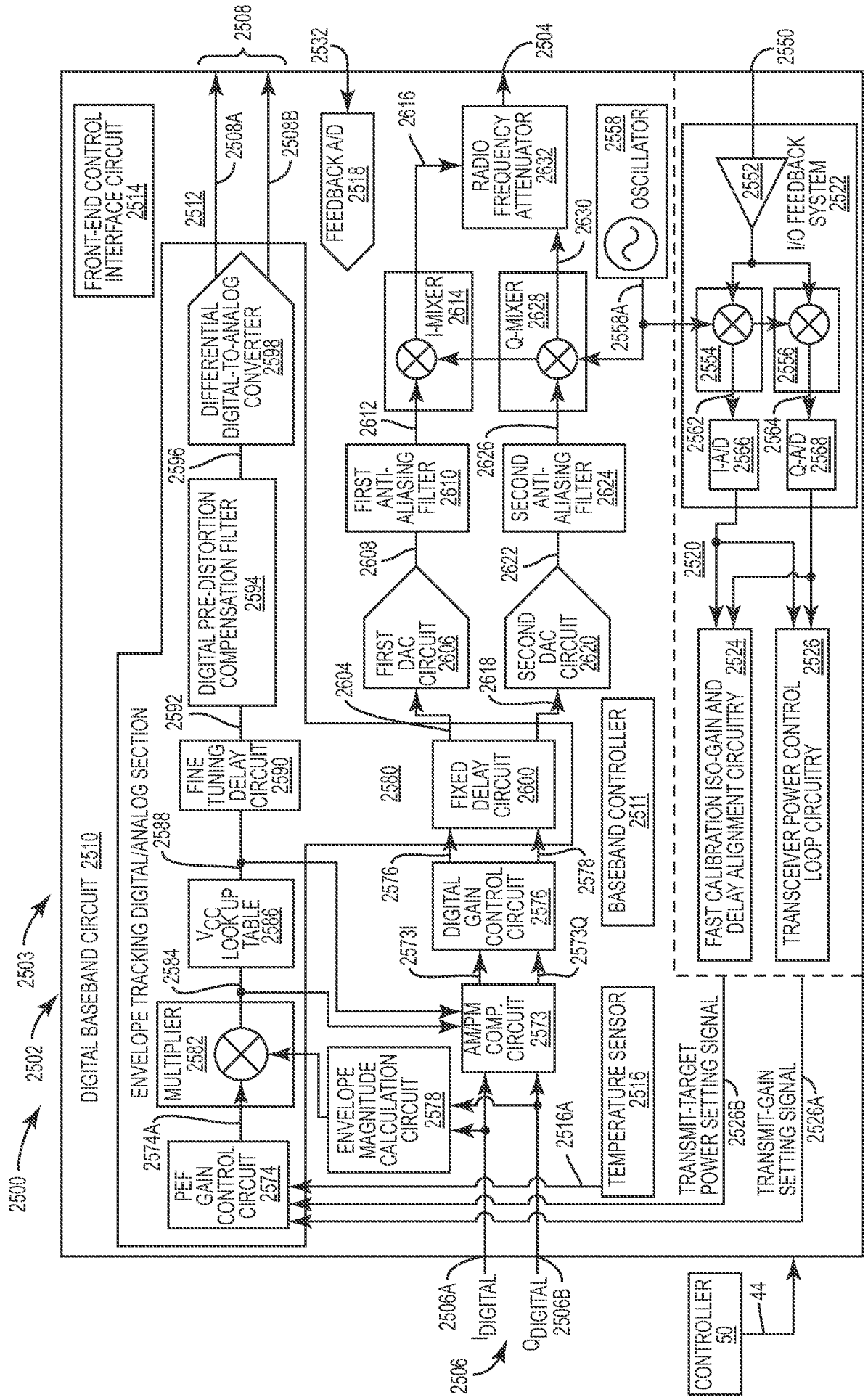

2500
2502
2503
DIGITAL BASEBAND CIRCUIT 2510
ENVELOPE TRACKING DIGITAL/ANALOG SECTION
FRONT-END CONTROL INTERFACE CIRCUIT 2514
2508
2532
2504
2550
2512
2508A
2508B
FEEDBACK A/D 2518
2616
RADIO FREQUENCY ATTENUATOR 2632
2558 OSCILLATOR
2552
I/O FEEDBACK SYSTEM 2522
DIFFERENTIAL DIGITAL-TO-ANALOG CONVERTER 2598
I-MIXER 2614
Q-MIXER 2628
2630
2558A
2554
2556
2596
2612
2626
FIRST ANTI-ALIASING FILTER 2610
SECOND ANTI-ALIASING FILTER 2624
2562
I-A/D 2566
2564
Q-A/D 2568
DIGITAL PRE-DISTORTION COMPENSATION FILTER 2594
2608
2622
2520
2592
FIRST DAC CIRCUIT 2606
SECOND DAC CIRCUIT 2620
2604
2618
FINE TUNING DELAY CIRCUIT 2590
2580
FIXED DELAY CIRCUIT 2600
BASEBAND CONTROLLER 2511
FAST CALIBRATION ISO-GAIN AND DELAY ALIGNMENT CIRCUITRY 2524
TRANSCEIVER POWER CONTROL LOOP CIRCUITRY 2526
2588
2576
2578
2573I
2573Q
DIGITAL GAIN CONTROL CIRCUIT 2576
V_{CC} LOOK UP TABLE 2586
2584
2574A
MULTIPLIER 2582
AM/PM COMP. CIRCUIT 2573
TEMPERATURE SENSOR 2516
TRANSMIT-TARGET POWER SETTING SIGNAL 2526B
TRANSMIT-GAIN SETTING SIGNAL 2526A
PEF GAIN CONTROL CIRCUIT 2574
ENVELOPE MAGNITUDE CALCULATION CIRCUIT 2578
2516A
2506A
$I_{DIGITAL}$
$Q_{DIGITAL}$ 2506B
2506
CONTROLLER 50
44

FIG. 56

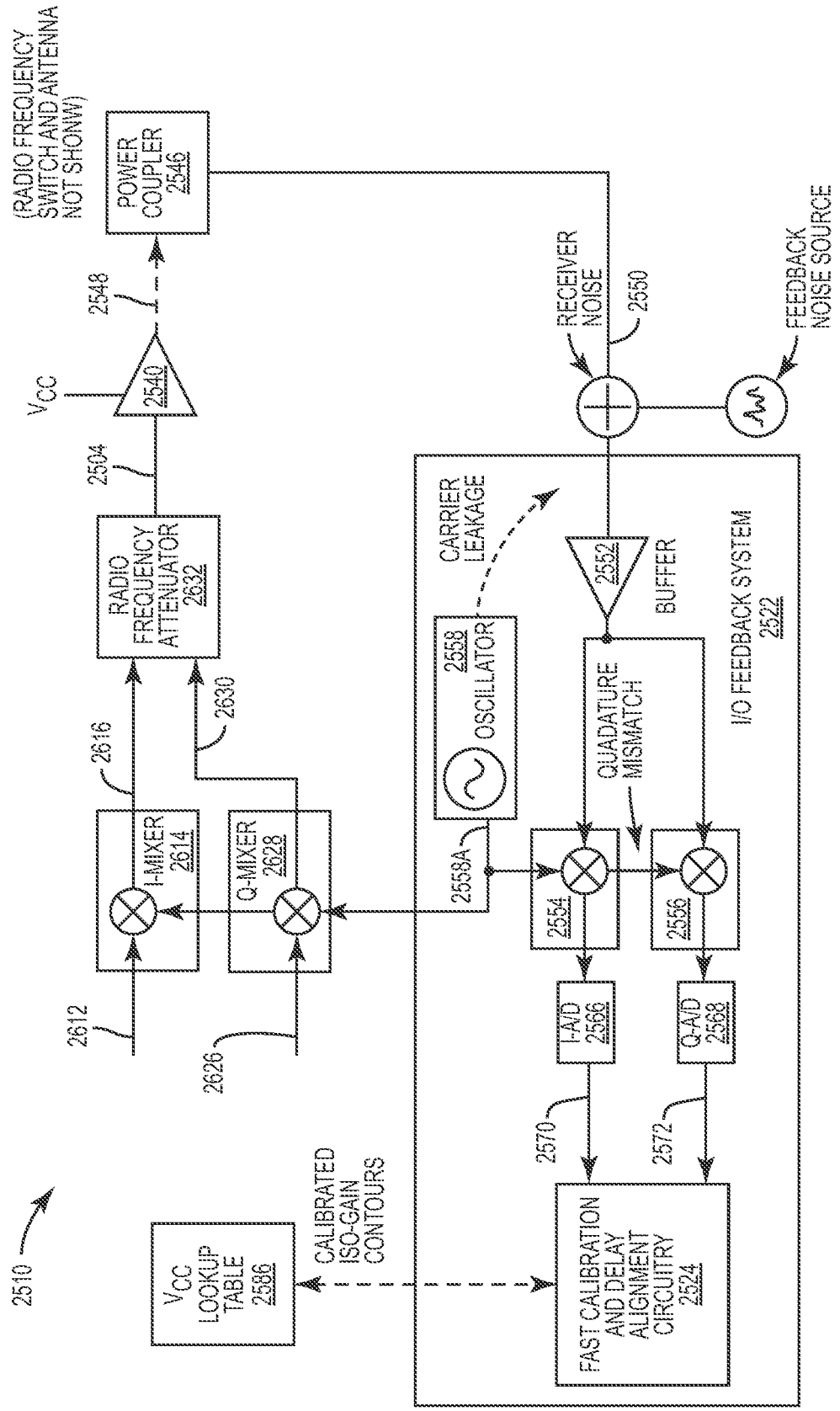

2510
VCC LOOKUP TABLE 2586
CALIBRATED ISO-GAIN CONTOURS
FAST CALIBRATION AND DELAY ALIGNMENT CIRCUITRY 2524
I/O FEEDBACK SYSTEM 2522
I-A/D 2566
Q-A/D 2568
2570
2572
2554
2556
QUADATURE MISMATCH
BUFFER 2552
2558 OSCILLATOR
CARRIER LEAKAGE
2558A
I-MIXER 2614
Q-MIXER 2628
2612
2626
2616
2630
RADIO FREQUENCY ATTENUATOR 2632
2504
VCC
2540
2548
POWER COUPLER 2546
(RADIO FREQUENCY SWITCH AND ANTENNA NOT SHONW)
RECEIVER NOISE
2550
FEEDBACK NOISE SOURCE

FIG. 57A

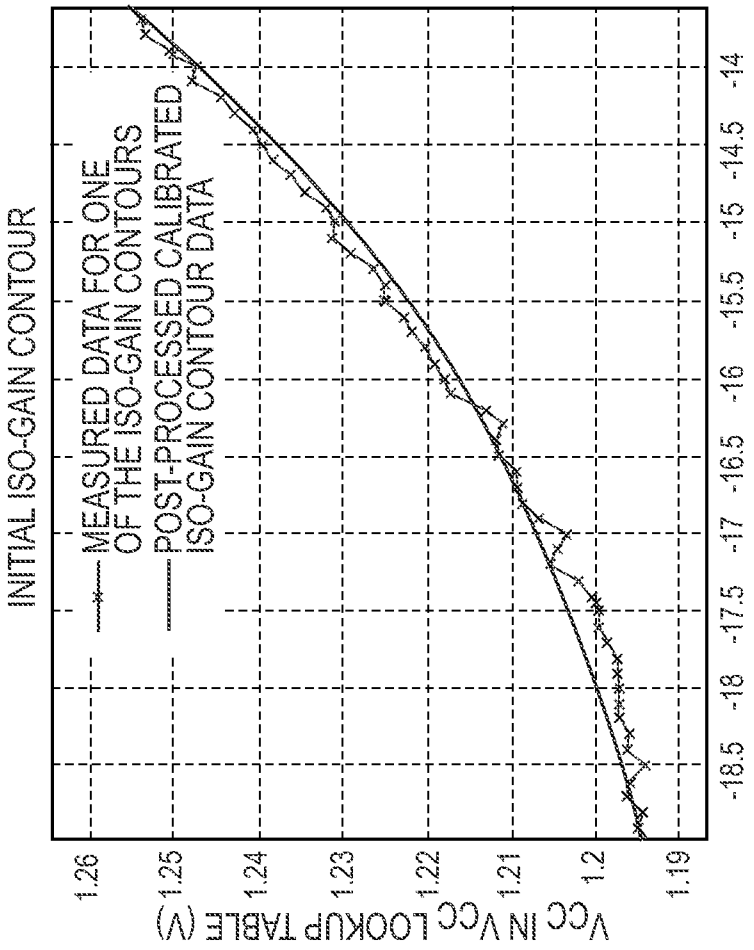

INITIAL ISO-GAIN CONTOUR
MEASURED DATA FOR ONE OF THE ISO-GAIN CONTOURS
POST-PROCESSED CALIBRATED ISO-GAIN CONTOUR DATA
VCC IN VCC LOOKUP TABLE (V)
1.26
1.25
1.24
1.23
1.22
1.21
1.2
1.19
-18.5
-18
-17.5
-17
-16.5
-16
-15.5
-15
-14.5
-14
INPUT POWER Pin (dB)

FIG. 57B

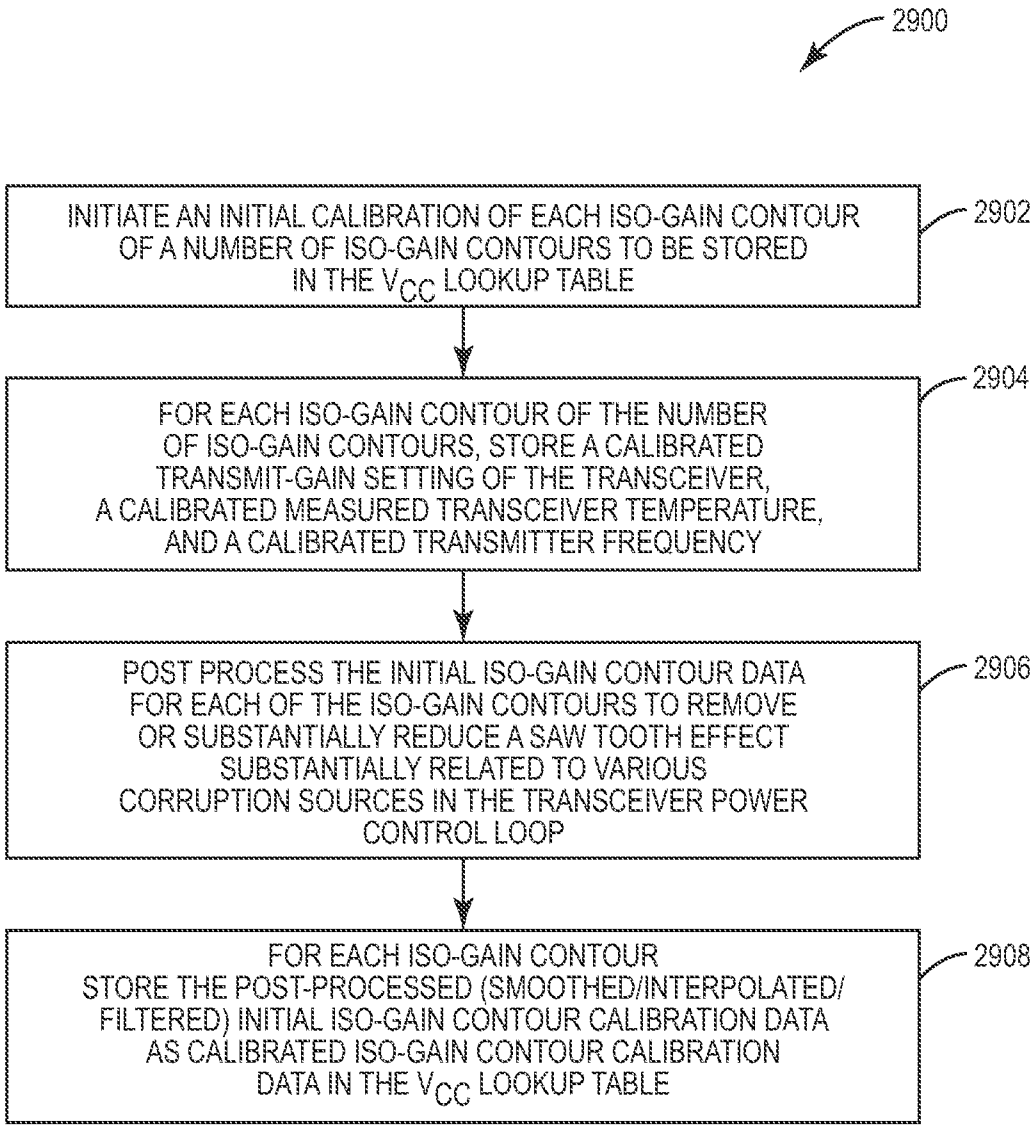

2900
INITIATE AN INITIAL CALIBRATION OF EACH ISO-GAIN CONTOUR OF A NUMBER OF ISO-GAIN CONTOURS TO BE STORED IN THE V_{CC} LOOKUP TABLE
2902
FOR EACH ISO-GAIN CONTOUR OF THE NUMBER OF ISO-GAIN CONTOURS, STORE A CALIBRATED TRANSMIT-GAIN SETTING OF THE TRANSCEIVER, A CALIBRATED MEASURED TRANSCEIVER TEMPERATURE, AND A CALIBRATED TRANSMITTER FREQUENCY
2904
POST PROCESS THE INITIAL ISO-GAIN CONTOUR DATA FOR EACH OF THE ISO-GAIN CONTOURS TO REMOVE OR SUBSTANTIALLY REDUCE A SAW TOOTH EFFECT SUBSTANTIALLY RELATED TO VARIOUS CORRUPTION SOURCES IN THE TRANSCEIVER POWER CONTROL LOOP
2906
FOR EACH ISO-GAIN CONTOUR STORE THE POST-PROCESSED (SMOOTHED/INTERPOLATED/ FILTERED) INITIAL ISO-GAIN CONTOUR CALIBRATION DATA AS CALIBRATED ISO-GAIN CONTOUR CALIBRATION DATA IN THE V_{CC} LOOKUP TABLE
2908

FIG.57C

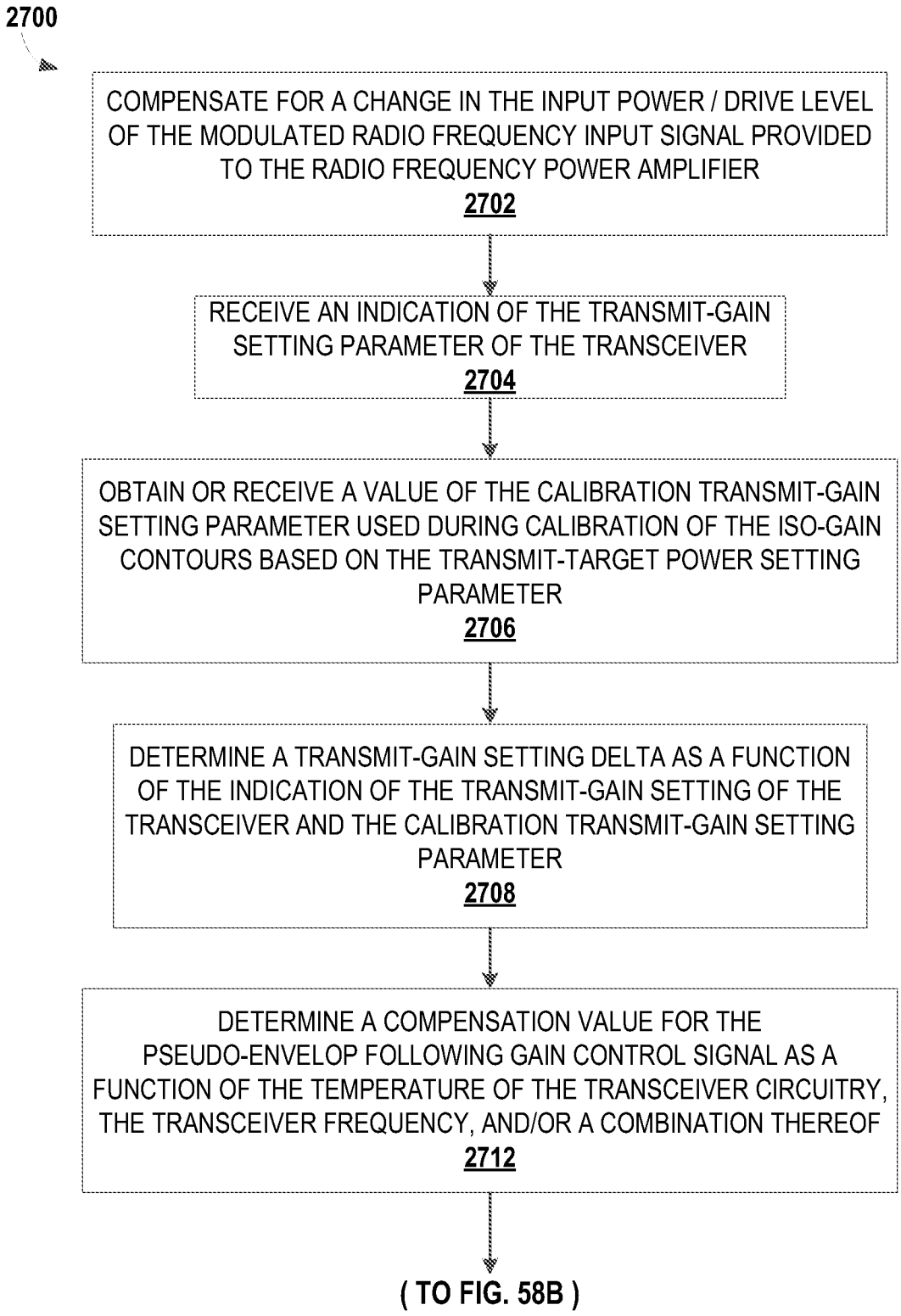

2700
COMPENSATE FOR A CHANGE IN THE INPUT POWER / DRIVE LEVEL OF THE MODULATED RADIO FREQUENCY INPUT SIGNAL PROVIDED TO THE RADIO FREQUENCY POWER AMPLIFIER
2702
RECEIVE AN INDICATION OF THE TRANSMIT-GAIN SETTING PARAMETER OF THE TRANSCEIVER
2704
OBTAIN OR RECEIVE A VALUE OF THE CALIBRATION TRANSMIT-GAIN SETTING PARAMETER USED DURING CALIBRATION OF THE ISO-GAIN CONTOURS BASED ON THE TRANSMIT-TARGET POWER SETTING PARAMETER
2706
DETERMINE A TRANSMIT-GAIN SETTING DELTA AS A FUNCTION OF THE INDICATION OF THE TRANSMIT-GAIN SETTING OF THE TRANSCEIVER AND THE CALIBRATION TRANSMIT-GAIN SETTING PARAMETER
2708
DETERMINE A COMPENSATION VALUE FOR THE PSEUDO-ENVELOP FOLLOWING GAIN CONTROL SIGNAL AS A FUNCTION OF THE TEMPERATURE OF THE TRANSCEIVER CIRCUITRY, THE TRANSCEIVER FREQUENCY, AND/OR A COMBINATION THEREOF
2712
(TO FIG. 58B)

FIG. 58A

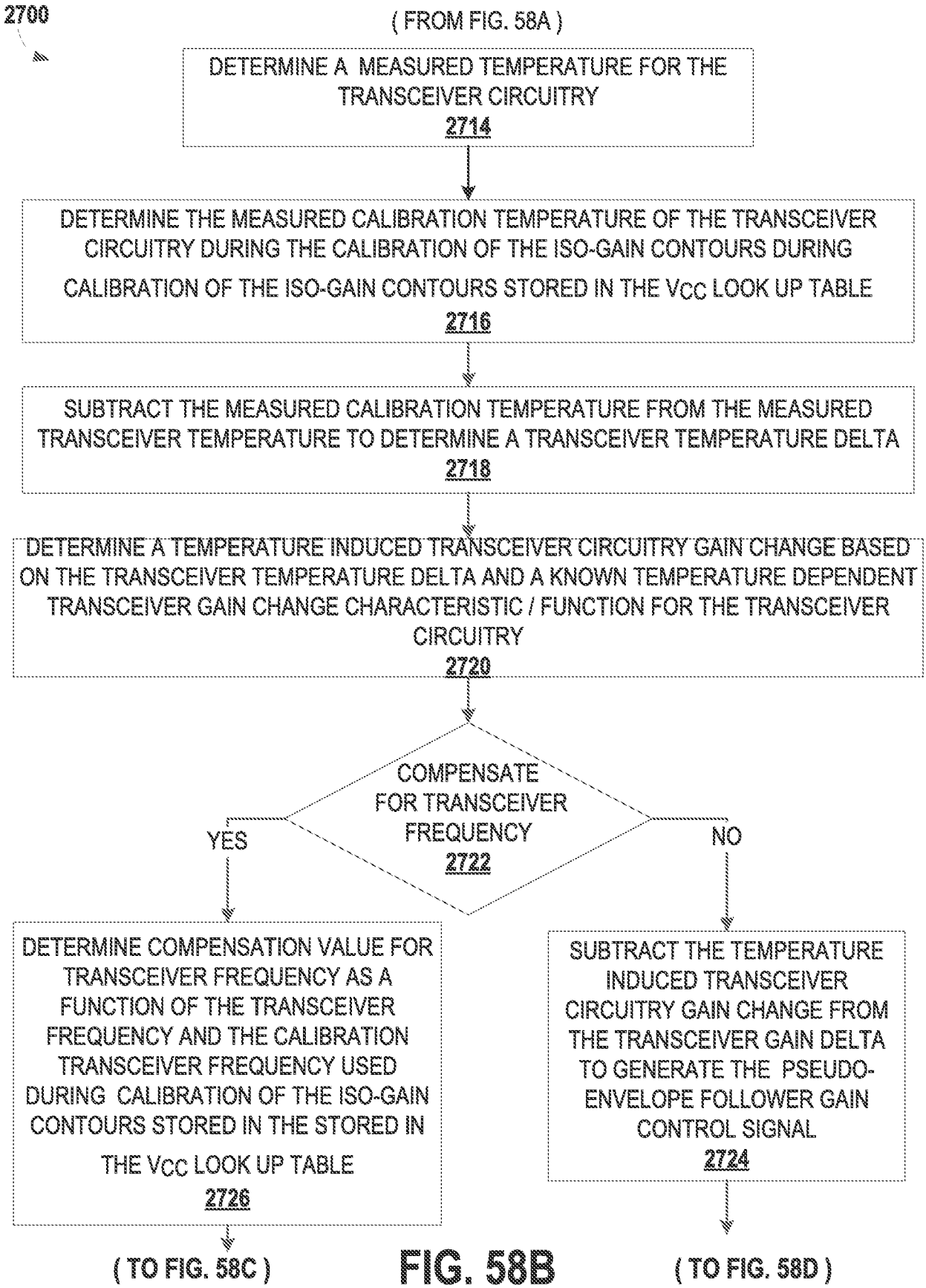

2700
(FROM FIG. 58A)
DETERMINE A MEASURED TEMPERATURE FOR THE TRANSCEIVER CIRCUITRY
2714
DETERMINE THE MEASURED CALIBRATION TEMPERATURE OF THE TRANSCEIVER CIRCUITRY DURING THE CALIBRATION OF THE ISO-GAIN CONTOURS DURING CALIBRATION OF THE ISO-GAIN CONTOURS STORED IN THE VCC LOOK UP TABLE
2716
SUBTRACT THE MEASURED CALIBRATION TEMPERATURE FROM THE MEASURED TRANSCEIVER TEMPERATURE TO DETERMINE A TRANSCEIVER TEMPERATURE DELTA
2718
DETERMINE A TEMPERATURE INDUCED TRANSCEIVER CIRCUITRY GAIN CHANGE BASED ON THE TRANSCEIVER TEMPERATURE DELTA AND A KNOWN TEMPERATURE DEPENDENT TRANSCEIVER GAIN CHANGE CHARACTERISTIC / FUNCTION FOR THE TRANSCEIVER CIRCUITRY
2720
COMPENSATE FOR TRANSCEIVER FREQUENCY
2722
YES
NO
DETERMINE COMPENSATION VALUE FOR TRANSCEIVER FREQUENCY AS A FUNCTION OF THE TRANSCEIVER FREQUENCY AND THE CALIBRATION TRANSCEIVER FREQUENCY USED DURING CALIBRATION OF THE ISO-GAIN CONTOURS STORED IN THE STORED IN THE VCC LOOK UP TABLE
2726
SUBTRACT THE TEMPERATURE INDUCED TRANSCEIVER CIRCUITRY GAIN CHANGE FROM THE TRANSCEIVER GAIN DELTA TO GENERATE THE PSEUDO-ENVELOPE FOLLOWER GAIN CONTROL SIGNAL
2724
(TO FIG. 58C)
(TO FIG. 58D)

FIG. 58B

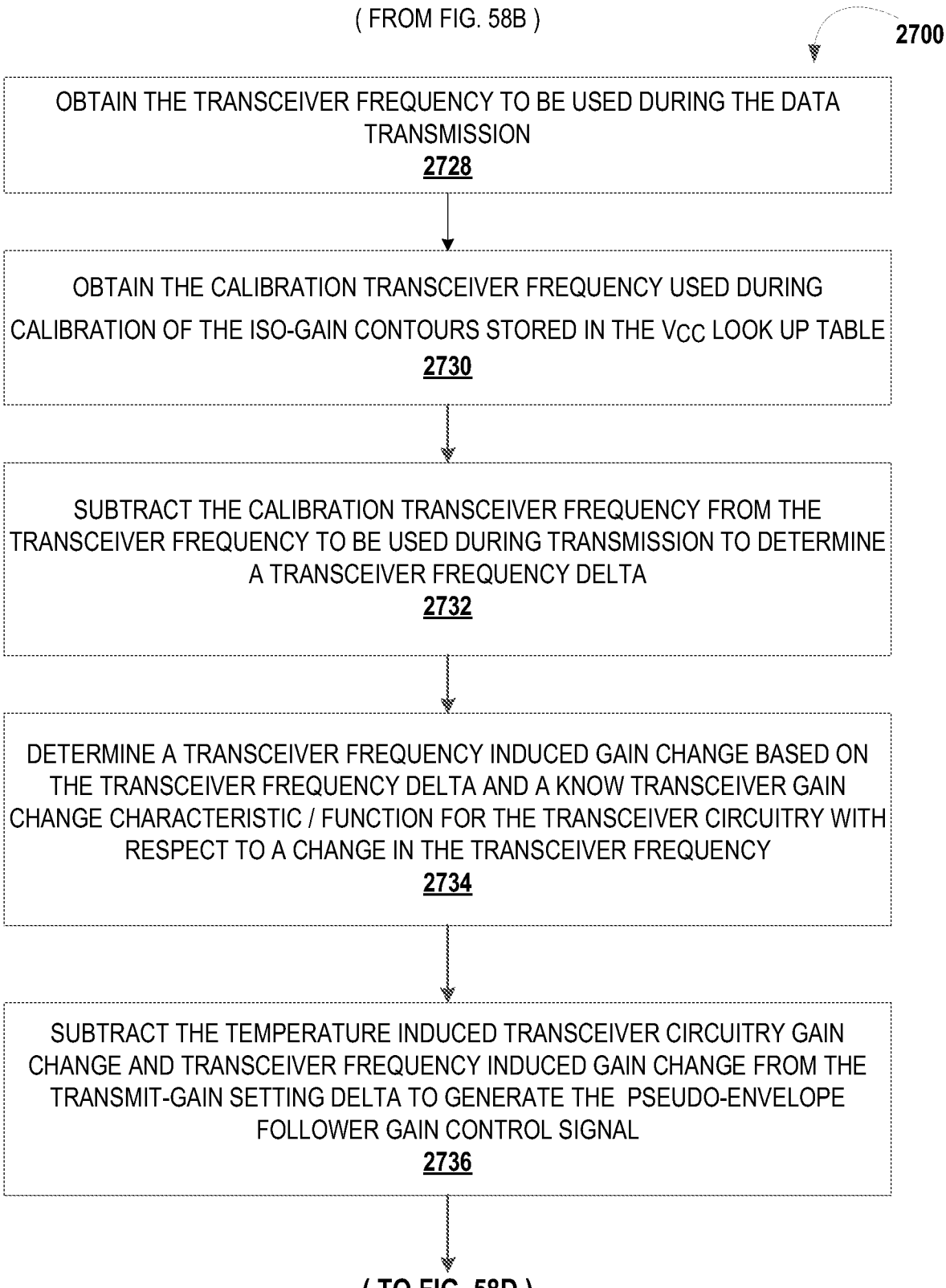

(FROM FIG. 58B)
2700
OBTAIN THE TRANSCEIVER FREQUENCY TO BE USED DURING THE DATA TRANSMISSION
2728
OBTAIN THE CALIBRATION TRANSCEIVER FREQUENCY USED DURING CALIBRATION OF THE ISO-GAIN CONTOURS STORED IN THE V_{CC} LOOK UP TABLE
2730
SUBTRACT THE CALIBRATION TRANSCEIVER FREQUENCY FROM THE TRANSCEIVER FREQUENCY TO BE USED DURING TRANSMISSION TO DETERMINE A TRANSCEIVER FREQUENCY DELTA
2732
DETERMINE A TRANSCEIVER FREQUENCY INDUCED GAIN CHANGE BASED ON THE TRANSCEIVER FREQUENCY DELTA AND A KNOW TRANSCEIVER GAIN CHANGE CHARACTERISTIC / FUNCTION FOR THE TRANSCEIVER CIRCUITRY WITH RESPECT TO A CHANGE IN THE TRANSCEIVER FREQUENCY
2734
SUBTRACT THE TEMPERATURE INDUCED TRANSCEIVER CIRCUITRY GAIN CHANGE AND TRANSCEIVER FREQUENCY INDUCED GAIN CHANGE FROM THE TRANSMIT-GAIN SETTING DELTA TO GENERATE THE PSEUDO-ENVELOPE FOLLOWER GAIN CONTROL SIGNAL
2736
(TO FIG. 58D)

FIG. 58C

(FROM FIGS. 58B AND 58C)

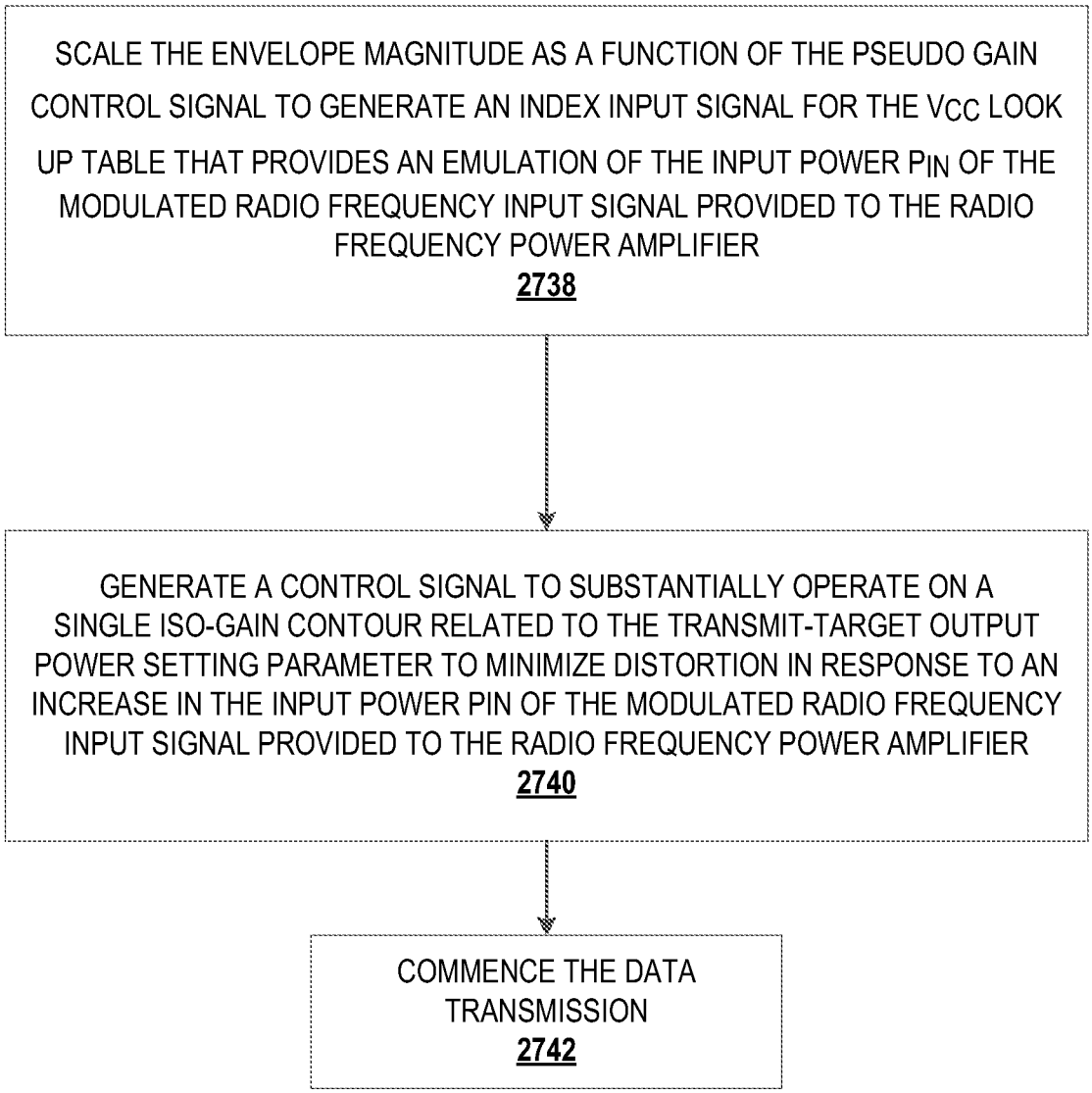


FIG. 58D

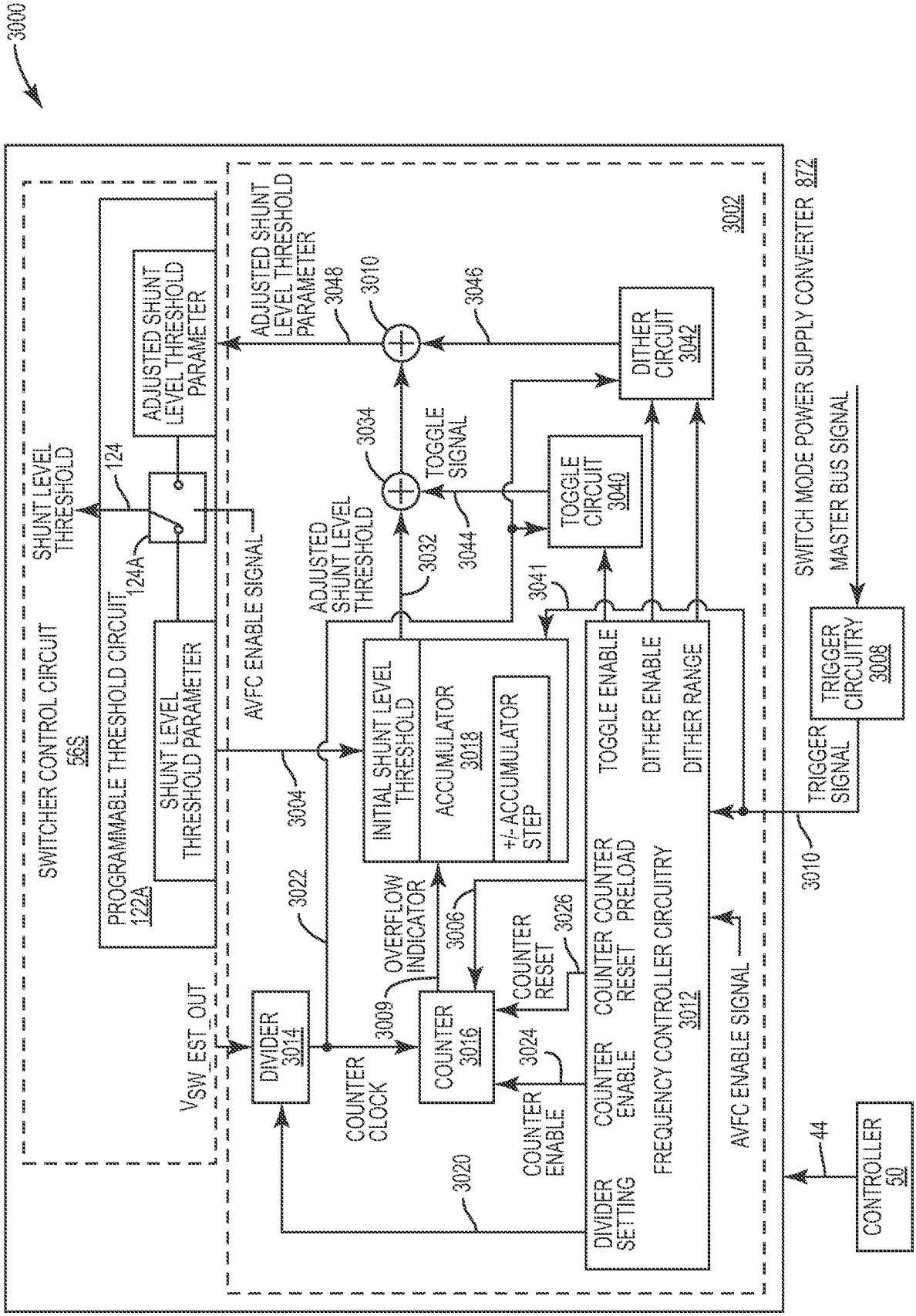

3000
SWITCHER CONTROL CIRCUIT
56S
SHUNT LEVEL THRESHOLD
124
PROGRAMMABLE THRESHOLD CIRCUIT
122A
124A
SHUNT LEVEL THRESHOLD PARAMETER
ADJUSTED SHUNT LEVEL THRESHOLD PARAMETER
ADJUSTED SHUNT LEVEL THRESHOLD PARAMETER
3048
3010
3046
3034
TOGGLE SIGNAL
AVFC ENABLE SIGNAL
ADJUSTED SHUNT LEVEL THRESHOLD
3032
3044
3041
TOGGLE CIRCUIT
3040
DITHER CIRCUIT
3042
3004
INITIAL SHUNT LEVEL THRESHOLD
ACCUMULATOR
3018
+/- ACCUMULATOR STEP
3022
TOGGLE ENABLE
DITHER ENABLE
DITHER RANGE
3002
OVERFLOW INDICATOR
3009
3006
COUNTER RESET
3026
COUNTER COUNTER PRELOAD
COUNTER CLOCK
COUNTER
3016
3024
COUNTER ENABLE
COUNTER ENABLE
3020
DIVIDER SETTING
FREQUENCY CONTROLLER CIRCUITRY
3012
AVFC ENABLE SIGNAL
DIVIDER
3014
$V_{SW_EST_OUT}$
SWITCH MODE POWER SUPPLY CONVERTER 872
TRIGGER SIGNAL
3010
TRIGGER CIRCUITRY
3008
MASTER BUS SIGNAL
44
CONTROLLER
50

FIG. 59

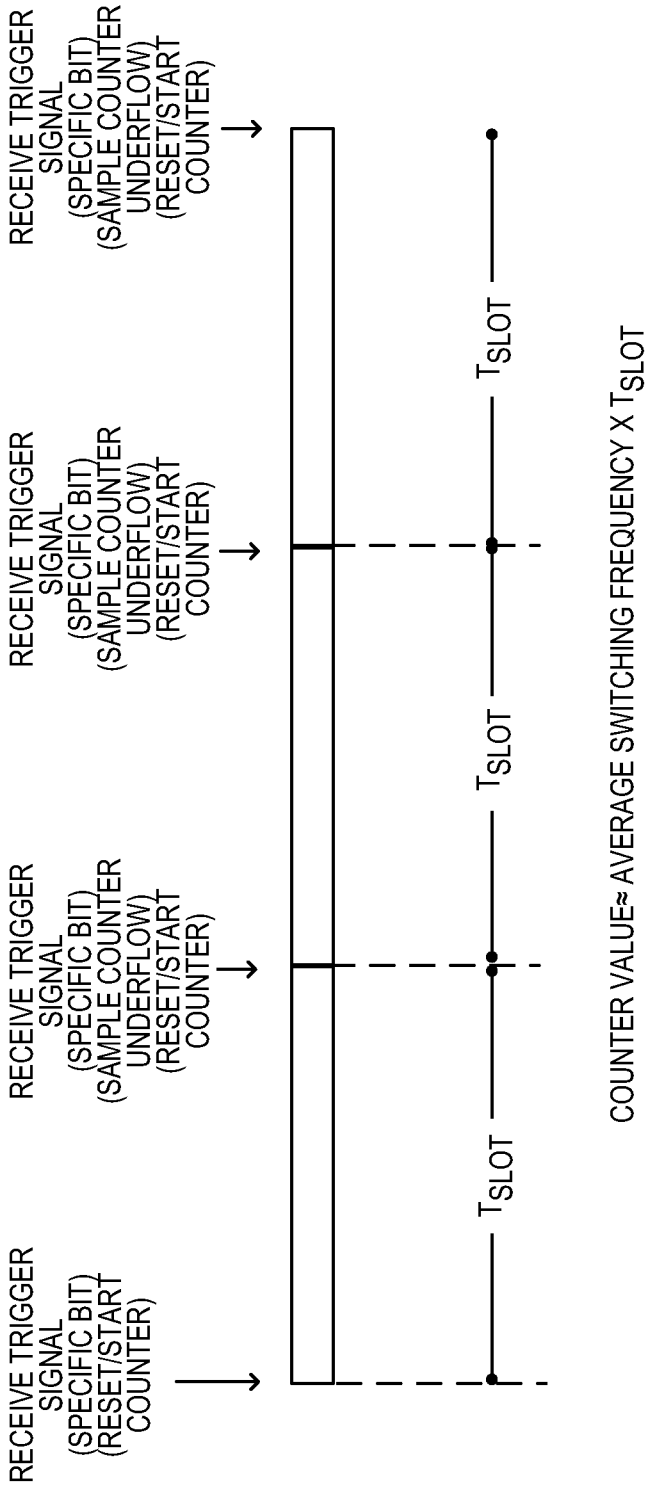

RECEIVE TRIGGER SIGNAL (SPECIFIC BIT) (RESET/START COUNTER)
RECEIVE TRIGGER SIGNAL (SPECIFIC BIT) (SAMPLE COUNTER UNDERFLOW) (RESET/START COUNTER)
RECEIVE TRIGGER SIGNAL (SPECIFIC BIT) (SAMPLE COUNTER UNDERFLOW) (RESET/START COUNTER)
T_{SLOT}
T_{SLOT}
T_{SLOT}
COUNTER VALUE≈ AVERAGE SWITCHING FREQUENCY X T_{SLOT}

FIG. 61

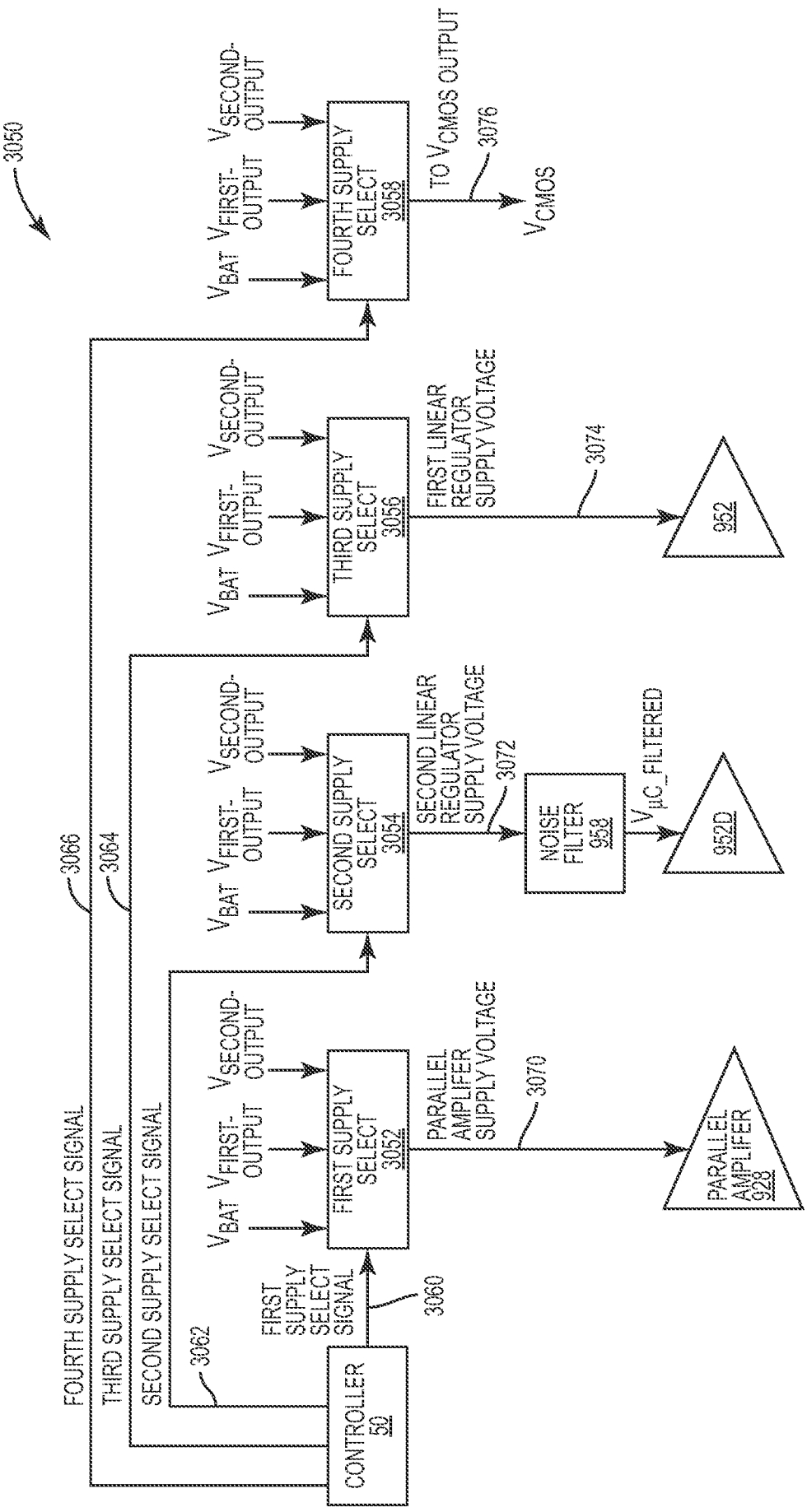

3050
CONTROLLER 50
FIRST SUPPLY SELECT SIGNAL
3060
3062
SECOND SUPPLY SELECT SIGNAL
THIRD SUPPLY SELECT SIGNAL
3064
FOURTH SUPPLY SELECT SIGNAL
3066
FIRST SUPPLY SELECT 3052
SECOND SUPPLY SELECT 3054
THIRD SUPPLY SELECT 3056
FOURTH SUPPLY SELECT 3058
VBAT
VFIRST-OUTPUT
VSECOND-OUTPUT
PARALLEL AMPLIFER SUPPLY VOLTAGE
3070
SECOND LINEAR REGULATOR SUPPLY VOLTAGE
3072
FIRST LINEAR REGULATOR SUPPLY VOLTAGE
3074
TO VCMOS OUTPUT
3076
VCMOS
NOISE FILTER 958
VμC_FILTERED
PARALLEL AMPLIFER 928
952
952D

FIG. 62

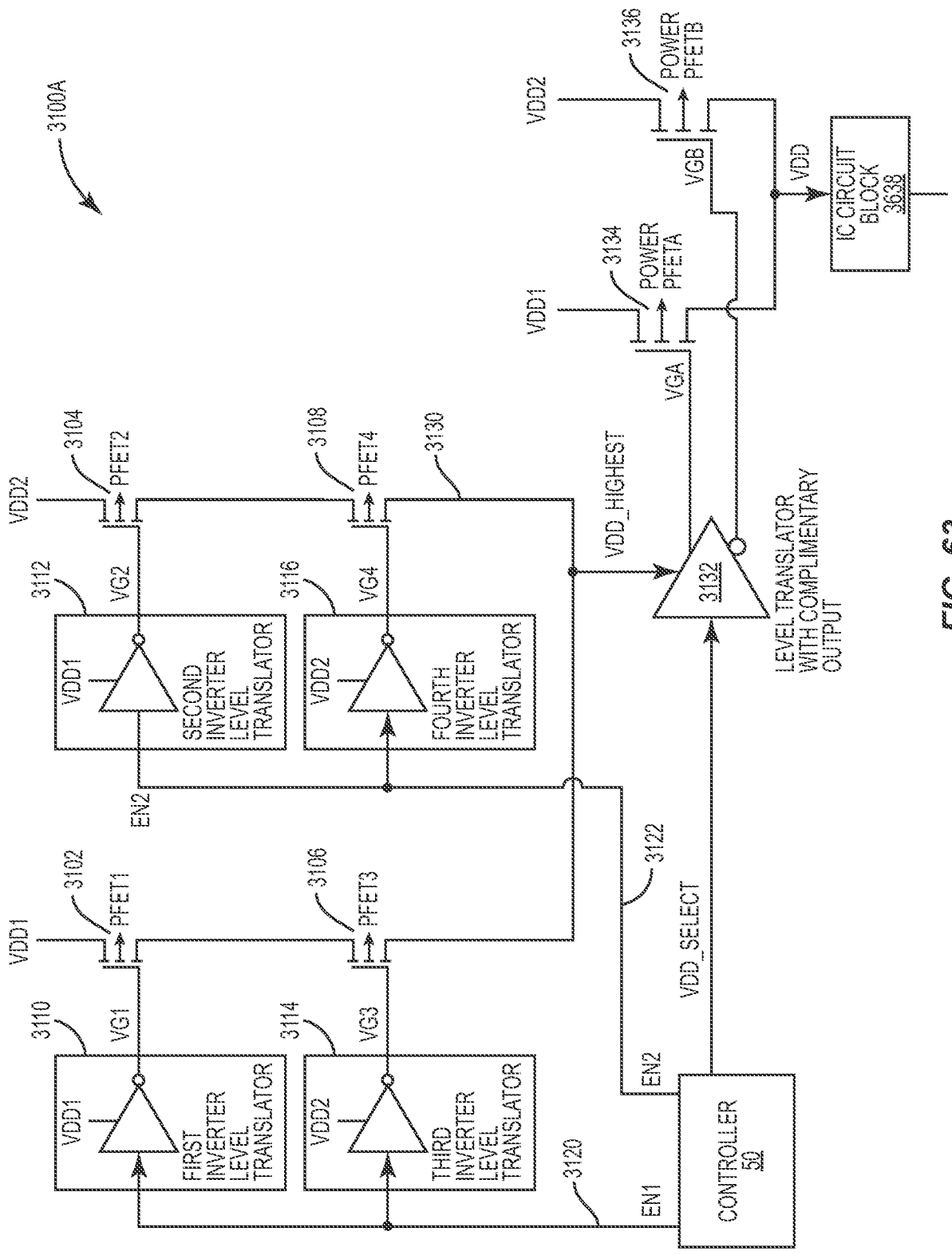

3100A
VDD2
3136
POWER PFETB
VGB
VDD
IC CIRCUIT BLOCK 3638
VDD1
3134
POWER PFETA
VGA
VDD2
3104
PFET2
3108
PFET4
3130
VDD_HIGHEST
3112
VG2
3116
VG4
VDD1
SECOND INVERTER LEVEL TRANSLATOR
VDD2
FOURTH INVERTER LEVEL TRANSLATOR
3132
LEVEL TRANSLATOR WITH COMPLIMENTARY OUTPUT
EN2
3122
VDD_SELECT
VDD1
3102
PFET1
3106
PFET3
3110
VG1
3114
VG3
VDD1
FIRST INVERTER LEVEL TRANSLATOR
VDD2
THIRD INVERTER LEVEL TRANSLATOR
EN2
3120
EN1
CONTROLLER 50

FIG. 63

PATENT COOPERATION TREATY

PCT

DECLARATION OF NON-ESTABLISHMENT OF INTERNATIONAL SEARCH REPORT

(PCT Article 17(2)(a), Rules 13*ter*.1(c) and Rule 39)

Applicant's or agent's file reference	IMPORTANT DECLARATION	Date of mailing *(day/month/year)*
2867-964-WO		10 August 2012 (10-08-2012)
International application No.	International filing date *(day/month/year)*	(Earliest) Priority date *(day/month/year)*
PCT/US2012/036858	7 May 2012 (07-05-2012)	5 May 2011 (05-05-2011)

International Patent Classification (IPC) or both national classification and IPC

H03F1/32, H03F1/02, H03F3/195, H03F3/24, H04B17/00, H03G3/00, H03G3/30, H03F3/217

Applicant

RF MICRO DEVICES, INC.

This International Searching Authority hereby declares, according to Article 17(2)(a), that **no international search report will be established** on the international application for the reasons indicated below

1. ☐ The subject matter of the international application relates to:
   - a. ☐ scientific theories
   - b. ☐ mathematical theories
   - c. ☐ plant varieties
   - d. ☐ animal varieties
   - e. ☐ essentially biological processes for the production of plants and animals, other than microbiological processes and the products of such processes
   - f. ☐ schemes, rules or methods of doing business
   - g. ☐ schemes, rules or methods of performing purely mental acts
   - h. ☐ schemes, rules or methods of playing games
   - i. ☐ methods for treatment of the human body by surgery or therapy
   - j. ☐ methods for treatment of the animal body by surgery or therapy
   - k. ☐ diagnostic methods practised on the human or animal body
   - l. ☐ mere presentations of information
   - m. ☐ computer programs for which this International Searching Authority is not equipped to search prior art
2. ☒ The failure of the following parts of the international application to comply with prescribed requirements prevents a meaningful search from being carried out:
   ☐ the description ☒ the claims ☐ the drawings
3. ☐ A meaningful search could not be carried out without the sequence listing; the applicant did not, within the prescribed time limit:
   - ☐ furnish a sequence listing on paper complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - ☐ furnish a sequence listing in electronic form complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - ☐ pay the required late furnishing fee for the furnishing of a sequence listing in response to an invitation under Rule 13*ter*.1(a) or (b).
4. *Further comments:*

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040 Fax: (+31-70) 340-3016	GAUR, Claudia Tel: +49 (0)89 2399-5717

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 203

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.2), should the problems which led to the Article 17(2) declaration be overcome.