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54 **Display control method and apparatus for ferroelectric liquid crystal panel.**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a display control method and apparatus for a ferroelectric liquid crystal panel (hereinafter abbreviated also as FLC_D).

2. Description of the Prior Art

Fig. 1 is a block diagram schematically showing a typical conventional configuration of a display system using an FLC_D 1. In the display system, a signal necessary for the image display is digitized, and the digital signal outputted to a CRT (cathode ray tube) 3 displaying images from a personal computer 2 is used. The digital signal outputted from the personal computer 2 is transformed in a separate control circuit 4, and by the transformation signal the image is displayed on the FLC_D 1.

Fig. 2 is a cross-sectional view showing a schematic configuration of the FLC_D 1. Two sheets of glass substrates 5a, 5b are disposed in opposition to each other, a signal electrode S consisting of indium tin oxide (hereinafter abbreviated as ITO) being arranged plurally in parallel on the surface of one glass substrate 5a, and covered by a transparent insulating film 6a consisting of SiO₂ thereon. On the surface of the other glass substrate 5b opposing the signal electrode S, a scanning electrode L consisting of ITO is arranged plurally in parallel in a direction orthogonal to the signal electrode S, and covered by an insulating film 6b consisting of SiO₂ thereon. On the insulating films 6a, 6b, orientation films 7a, 7b consisting of polyvinyl alcohol and treated by rubbing processing are formed respectively. The two glass substrates 5a, 5b are bonded together with a sealing agent 8 partially leaving an injection port, which is sealed by the sealing agent 8 after a ferroelectric liquid crystal 9 is introduced into a space between the orientation films 7a, 7b by vacuum injection therethrough. The two glass substrates 5a, 5b thus bonded together are clamped between two polarizing plates 10a, 10b arranged such that their respective polarizing axes intersect orthogonally.

Fig. 3 is a plan view showing the configuration, in which a scanning side driving circuit 11 is connected to the scanning electrode L of the FLC_D 1 having a simple matrix configuration above mentioned, and a signal side driving circuit 12 is connected to the signal electrode S. The scanning side driving circuit 11 is a circuit for applying voltages to the scanning electrodes L, and the signal side driving circuit 12 is a circuit for applying voltages to the signal electrodes S. Here, for the purpose of simplification, the case wherein the scanning electrodes L are 32 and the signal electro-

des S are 16, i.e. the case of FLC_D 1 which is constructed by picture elements of 32 x 16 is shown, and respective electrodes of the scanning electrodes L are distinguished by adding an index i (i = 1 to 32) to the symbol L, and respective electrodes of the signal electrodes S are distinguished by adding an index j (j = 1 to 16) to the symbol S. In the description made hereinafter, a picture element at the intersection of any scanning electrode L_i and any signal electrode S_j is represented by a symbol A_{ij}.

Fig. 4 is a waveform diagram showing respective signals outputted from the personal computer 2. Fig. 4 (1) is a horizontal synchronizing signal HD which gives the timing of one scanning interval of a screen of the CRT 3, Fig. 4 (2) is a vertical synchronizing signal VD showing a period for one picture screen and Fig. 4 (3) shows display data Data of an image. Fig. 4 (4) is a waveform diagram showing an expanded scanning interval of the horizontal synchronizing signal HD, Fig. 4 (5) is a waveform diagram showing an expanded scanning interval of the display data Data, and Fig. 4 (6) is a waveform diagram showing a data transfer clock CLK of the display data Data for one picture element.

Fig. 5 is a waveform diagram showing respective signals outputted from the control circuit 4. Fig. 5 (1) is a waveform diagram showing a clock YCLK for sequentially transferring the selective signal YI which selects the scanning electrode L, in a shift register, not shown, included in the scanning side driving circuit 11, Fig. 5 (2) is a waveform diagram showing the selective signal YI and Fig. 5 (3) shows the display data DATA corresponding to respective picture elements of the FLC_D 1. Fig. 5 (4) is a waveform diagram showing an expanded one period of the clock YCLK, Fig. 5 (5) is a waveform diagram showing an expanded one period of the clock YCLK of the selective signal YI, Fig. 5 (6) is a waveform diagram showing an expanded one period of the clock YCLK of the display data DATA, Fig. 5 (7) is a waveform diagram showing a display data transfer clock XCLK for sequentially transferring the display data DATA, in a shift register, not shown, included in the signal side driving circuit 12, Fig. 5 (8) is an expanded waveform diagram of a latch pulse LP which gives timing for taking in and holding the display data DATA in the shift register of the signal side driving circuit 12, into a separate register, not shown, included in the same signal side driving circuit 12, Fig. 5 (9) is a waveform diagram showing a signal VC which designates kinds of voltage applied to the scanning electrodes L, and Fig. 5 (10) is a waveform diagram showing a signal VS which designates kinds of voltage applied to the signal electrodes S.

As such, to the control circuit 4, a function is given to transform four kinds of signals show in Fig. 4, i.e. the horizontal synchronizing signal HD, vertical synchronizing signal VD, display data Data and data

transfer clock YCLK, into seven kinds of signals shown in Fig. 5, i.e. the clock YCLK, selective signal YI, display data DATA, display data transfer clock XCLK, latch pulse LP and signals VC, VS.

Fig. 6 is a waveform diagram showing respective impressed voltage wave forms to the scanning electrodes L and the signal electrodes S used in a driving method of the FLC1D 1 proposed in Japanese Patent Application Laid Open No. Sho 64-59389 (1989). A waveform shown in Fig. 6 (1) is applied to the scanning electrode L and is the waveform of a selective voltage A which is able to rewrite a memory state of picture elements on the scanning electrodes L, or a luminance state displayed, and though a waveform shown in Fig. 6 (2) is applied to the scanning electrodes L, it is the waveform of a non-selective voltage B which can not rewrite the display state of picture elements on the scanning electrodes L. A waveform shown in Fig. 6 (3) is the waveform of a rewriting bright voltage C applied to the signal electrodes S when rewriting the picture elements into the "bright" luminance state, a waveform shown in Fig. 6 (4) is the waveform of a rewriting dark voltage D applied to the signal electrodes S when rewriting the picture elements into the "dark" luminance state, and a waveform shown in Fig. 6 (5) is the waveform of a non-rewriting voltage G applied to the signal electrodes S when the display state of the picture element S is not rewritten. Fig. 6 (6) through Fig. 6 (11) show the waveforms of the effective voltage applied to the picture element Aij, among which, a waveform A-C in Fig. 6 (6) shows the waveform when the selective voltage A is applied to the scanning electrode Li and the rewriting bright voltage C is applied to the signal electrode Sj, a waveform A-D in Fig. 6 (7) shows the waveform when the selective voltage A is applied to the scanning electrode Li and the rewriting dark voltage D is applied to the signal electrode Sj, a waveform A-G in Fig. 6 (8) shows the waveform when the selective voltage A is applied to the scanning electrode Li and the non-rewriting voltage G is applied to the signal electrode Sj, a waveform B-C in Fig. 6 (9) shows the waveform when the non-selective voltage B is applied to the scanning electrode Li and the rewriting bright voltage C is applied to the signal electrode Sj, a waveform B-D in Fig. 6 (10) shows the waveform when the non-selective voltage B is applied to the scanning electrode Li and the rewriting dark voltage D is applied to the signal electrode Sj, and a waveform B-G in Fig. 6 (11) shows the waveform when the non-selective voltage B is applied to the scanning electrode Li and the non-rewriting voltage G is applied to the signal electrode Sj. In case the display state of the picture element Aij of the FLC1D 1 in Fig. 3 is rewritten by the driving method above mentioned, the selective voltage A in Fig. 6 (1) is applied to the scanning electrode Li, and to the rest of the scanning electrodes Lk ($k \neq i$, $k = 1$ to 32) the non-selective voltage B shown

in Fig. 6 (2) is applied, and when the picture element Aij is rewritten into the "bright" display state, the rewriting bright voltage C shown in Fig. 6 (3) is applied to the signal electrode Sj, when the picture element Aij is rewritten into the "dark" display state, the rewriting dark voltage D shown in Fig. 6 (4) is applied to the signal electrode Sj, and when the "bright" display state or the "dark" display state in a frame before the picture element Aij may be kept as it is, the non-rewriting voltage G shown in Fig. 6 (5) is applied to the signal electrode Sj.

For example, in the FLC1D 1 of Fig. 3, when a state wherein Japanese characters meaning "FERRO-ELECTRIC" are displayed on a picture screen by respective picture elements Aij on the "dark" display state indicated by oblique lines is rewritten into a state wherein Japanese characters meaning "ORDINARY DIELECTRIC" are displayed as shown in Fig. 7, the picture element Aij rewritten into the "bright" display state from the "dark" display state is represented by a symbol C corresponding to the rewriting bright voltage C, the picture element Aij rewritten into the "dark" display state from the "bright" display state is represented by a symbol D corresponding to the rewriting dark voltage D, the picture element Aij which remains as the "dark" display state is indicated by a symbol F and the picture element Aij which remains as the bright display state is indicated by an unscripted symbol, the entire picture screen is displayed as shown in Fig. 8. In this case, the picture element Aij of symbol F and that of unscripted symbol correspond to the non-rewriting voltage G.

Fig. 9 shows respective voltage waveforms applied to the scanning electrodes L1, L2, L3, signal electrodes S5, S6, and picture elements A15, A16, A25, A26 at this time. For reference, Fig. 9 (1) shows a waveform of the transferring clock YCLK of the selective signal YI at the shift register in the scanning side driving circuit 11, Fig. 9 (2) shows a waveform of the selective signal YI, Fig. 9 (3) shows an impressed voltage waveform to the scanning electrode L1, Fig. 9 (4) shows an impressed voltage waveform to the scanning electrode L2, Fig. 9 (5) shows an impressed voltage waveform to the scanning electrode L3, Fig. 9 (6) shows an impressed voltage waveform to the signal electrode S5, Fig. 9 (7) shows an impressed voltage waveform to the signal electrode S6, Fig. 9 (8) shows an effective voltage waveform applied to the picture element A15, Fig. 9 (9) shows an effective voltage waveform applied to the picture element A16, Fig. 9 (10) shows an effective voltage waveform applied to the picture element A25 and Fig. 9 (11) shows an effective voltage waveform applied to the picture element A26. In Fig. 9 (6) and Fig. 9 (7), a symbol E, F in parentheses corresponds to the non-symbolic picture element in Fig. 8, that is, it indicates that the non-rewriting voltage G is applied to the non-symbolic picture element in Fig. 8.

In the abovementioned driving method, as it will be understood from the effective voltage of the picture element A16 shown in Fig. 9 (9) and the effective voltage of the picture element A26 shown in Fig. 9 (11), the voltages applied to the picture element Aij are substantially equal whether or not the scanning electrode Li is selected, as far as its display state is not rewritten. Thereby, even in the case of low-speed driving wherein the time required for applying the selective voltage A to a certain scanning electrode Li and to the same scanning longer than 33.3 millisecond (corresponds to 30 Hz), it can be displayed without sensing any flicker.

Now, in case of the ferroelectric liquid crystal generally used in the FLC1 at present, when the scanning side driving circuit 11 and the signal side driving circuit 12 of for example, 24V voltage-proof are used, approximately 50 microsecond must be set as a unit pulse width t_0 of respective impressed voltages shown in Fig. 6, thus approximately 300 microsecond must be allocated as one selective time ($6 \cdot t_0$), when the aforesaid driving method is adopted. Therefore, when the FLC1 having one thousand scanning electrodes L is driven under this condition, one frame period in this case will become 0.3 millisecond.

This means, however, that it takes more than 0.3 millisecond for the display on the picture screen to be rewritten after the user has made some input from a keyboard, thus such a problem is encountered that, even though the display is realized without flicker as aforementioned, the number of scanning electrodes has to be restricted after all because of a limit on the response speed.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a display control method and a display controller for a ferroelectric liquid crystal display panel capable of shortening a frame period independently of the number of scanning electrodes.

In one aspect, the present invention, as defined by claim 1, provides a controller for a ferroelectric liquid crystal display panel, the panel comprising an array of picture elements each defined by the intersection of one of a plurality of scanning electrodes and one of a plurality of signal electrodes, and ferroelectric liquid crystal disposed therebetween, the controller comprising:

control means for supplying selection signals for selecting scanning electrodes of the display panel and, during the selection of each scanning electrode, data signals for applying data to the signal electrodes of the display panel;

characterised by:

a first memory which receives and stores the data for the next display frame;

a second memory which receives and stores

that part of the data for the current display frame which differs from said data for the next display frame;

a line memory for storing the result of a comparison, on a line-by-line basis, of said data for the next display frame with said data for the current display frame, for each line; and

said control means being arranged to supply, according to the content of said line memory, a succession of said selection signals which excludes selection signals for all or certain of all the scanning electrodes which correspond to lines for which said comparison indicates identity of data content between the current and next display frames, thereby reducing the length of time required to update a frame of data displayed on the display panel.

In another aspect, the present invention, as defined by claim 3, provides a method of controlling a ferroelectric liquid crystal display panel, the panel comprising an array of picture elements each defined by the intersection of one of a plurality of scanning electrodes and one of a plurality of signal electrodes, and ferroelectric liquid crystal disposed therebetween, the method comprising:

supplying to the display panel, selection signals for selecting scanning electrodes thereof and, during the selection of each scanning electrode, data signals for applying data to the signal electrodes thereof;

characterised by:

storing in a first memory the data for the next display frame;

storing in a second memory that part of the data for the current display frame which differs from said data for the next display frame;

comparing, on a line-by-line basis, said data for the next display frame with said data for the current display frame;

storing in memory the result of the comparison for each line; and

the supplying step comprising outputting, according to the content of said memory, a succession of said selection signals which excludes selection signals for all or certain of all the scanning electrodes which correspond to lines for which said comparison indicates identity of data content between the current and next display frames, thereby reducing the length of time required to update a frame of data displayed on the display panel.

The combination of features of the preamble of claim 1 and claim 3 is known from EP-A-0 167 398.

The dependent claims 2 and 4 relate to features of a preferred embodiment of the invention.

According to the present invention, in the case of a ferroelectric liquid crystal display panel having m scanning electrodes, when the number of scanning electrodes wherein display data displayed at present by the picture elements on the scanning electrodes

differs from display data to be displayed in the following frame is q, to the rest of (m-q) scanning electrodes wherein there is no difference in the display data the selective voltage is not applied at all or only applied to some of the (m-q) scanning electrodes, so that even when p scanning electrodes out of the rest (m-q) are selected, the selective voltage is not applied to (m-q-p) scanning electrodes during one frame. Thus, a frame period is considerably shortened.

According to the present invention, since the scanning electrodes wherein the displayed data of the picture elements on the scanning electrode displayed at present is the same as the display data in the following frame, are not selected at all in the following frame or are selected at the rate of one out of several scanning electrodes, even in the case of a ferroelectric liquid crystal panel having a large number of scanning electrodes, the frame period can be shortened by the decreased number of scanning electrodes being selected in one frame, and a response time till the display data inputted is displayed on the picture screen can be shortened accordingly.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a schematic configuration of a display system using a conventional display control apparatus,

Fig. 2 is a cross-sectional view showing a configuration of a ferroelectric liquid crystal panel used in the display system,

Fig. 3 is a view showing a state wherein Japanese characters meaning "FERROELECTRIC" are displayed on the ferroelectric liquid crystal panel,

Fig. 4 is a waveform diagram showing the output signal from a personal computer in the display system,

Fig. 5 is a waveform diagram showing the output signal from a control circuit in the display system,

Fig. 6 is a waveform diagram showing respective impressed voltages used in driving the ferroelectric liquid crystal panel in the display system,

Fig. 7 is a view showing a state wherein Japanese characters meaning "ORDINARY DIELECTRIC" are displayed on the ferroelectric liquid crystal panel,

Fig. 8 is a view showing the kinds of impressed voltage corresponding to a display state of the ferroelectric liquid crystal panel,

Fig. 9 is a waveform diagram showing respective voltages applied to some scanning electrodes, signal electrodes and picture elements of the ferroelectric liquid crystal panel,

Fig. 10 is a block diagram showing a schematic configuration of a display system applied in a display control apparatus for a ferroelectric liquid crystal panel as one embodiment of the invention,

Fig. 11 is a block diagram showing a schematic configuration of a control circuit serving as the display control apparatus,

Fig. 12 is a view showing the ferroelectric liquid crystal panel on which Japanese characters meaning "ORDINARY DIELECTRIC" are displayed by using the control circuit,

Fig. 13 is a view schematically showing an example of transformation data held in a frame memory for reference,

Fig. 14 and Fig. 15 are waveform diagrams respectively showing the output signal of the control circuit,

Fig. 16 is a waveform diagram showing the output signal of an input control circuit in the control circuit,

Fig. 17 is a waveform diagram showing the output signal of an output control circuit in the control circuit,

Fig. 18 is a waveform diagram showing respective voltages applied to some scanning electrodes, signal electrodes and picture elements of the ferroelectric liquid crystal panel,

Fig. 19 is a circuit diagram showing an example of specific configuration of the output control circuit,

Fig. 20 is a circuit diagram showing an example of specific configuration of a frame memory for display data in the control circuit,

Fig. 21 is a circuit diagram showing an example of specific configuration of a line memory in the control circuit, and

Fig. 22 is a circuit diagram showing an example of specific configuration of a frame memory for reference.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 10 is a block diagram showing a configuration of a display system in which a display control apparatus for a ferroelectric liquid crystal panel as one embodiment of the invention is applied. The configuration of the display system is schematically as same as the case of a conventional display system stated above, and wherein a signal necessary for the image display is digitized, and the digital signal outputted to a CRT (cathode ray tube) 23 for image display from a personal computer 22 is used. The digital signal outputted from the personal computer 22 is transformed in a control circuit 24 serving as the display control apparatus of the embodiment, the transformation signal displaying images on an FLCD 21.

As to the specific configuration of the FLCD 21, since it is as same as the conventional FLCD 1 shown in Fig. 2, explanation thereof will be omitted. As a ferroelectric liquid crystal of the FLCD 21, ZLI-4237/000 by Merck Corp. is used and as an orientation film

polyimide is used.

Fig. 11 is a block diagram schematically showing, a configuration of the control circuit 24. A frame memory for display data 25 is a memory for holding display data Data for one picture screen outputted from the personal computer 22. From the frame memory for display data 25, transformation data Rx indicating the difference between the display data displayed at present on the picture screen of the FLCDC 21 and display data to be displayed in the following frame is output.

A line memory 26 is a memory for, in response to the transformation data Rx outputted from the frame memory for display data 25, holding line difference identification data indicating whether there is even one picture element which is different in the display data displayed at present and display data to be displayed in the following frame, in the picture elements on each scanning electrode of the FLCDC 21, separately for each scanning electrode. In the line memory 26 a 1-bit memory area is allocated respectively for holding the line difference identification data of each of the scanning electrodes.

A frame memory for reference 27 is a memory for holding the transformation data Rx for one picture screen outputted from the frame memory for display data 25.

An input control circuit 28 is a circuit for controlling data writing into the frame memory for display data 25, line memory 26 and frame memory for reference 27, in response to the horizontal synchronizing signal HD, vertical synchronizing signal VD and clock CLK outputted from the personal computer 22, and signals OW, OAc and OAs outputted from an output control circuit 29.

The output control circuit 29 is a circuit for controlling the read out of hold data from the frame memory for display data 25, line memory 26 and frame memory for reference 27 and the output of a drive control circuit 30.

The drive control circuit 30 is a circuit for outputting the signal which controls the display drive of the FLCDC 21, in response to data DO given from the frame memory for display data 25 and data DRE given from the frame memory for reference 27.

Fig. 12 is a plan view showing a configuration, wherein to the scanning electrodes L of the FLCDC 21 of a simple matrix construction above mentioned a scanning side driving circuit 31 is connected, and to the signal electrodes S a signal side driving circuit 32 is connected. The scanning side driving circuit 31 is a circuit for applying the voltage to the scanning electrodes L, and the signal side driving circuit 32 is a circuit for applying the voltage to the signal electrodes S. Here, the same as the case of the conventional example, for the purpose of simplification, the FLCDC 21 having 32 scanning electrodes L and 16 signal electrodes S, i.e. 32 x 16 picture elements is shown, re-

spective scanning electrodes L being discriminated by adding an index i ($i = 1$ to 32) to a symbol L, and respective signal electrodes S being discriminated by adding an index j ($j = 1$ to 16) to a symbol S. In the following description, the same as the conventional example, a picture element at the intersection of any scanning electrode L_i and any signal electrode S_j is represented by a symbol A_{ij} .

Fig. 13 is a view schematically showing the transformation data Rx of one picture screen held in the frame memory for reference 27 in the form of display on the picture screen of the FLCDC 21, when the picture screen of the FLCDC 21 is switched to a state wherein Japanese characters meaning "ORDINARY DIELECTRIC" are displayed by the "dark" display picture elements indicated by oblique lines as shown in Fig. 12, from a state wherein Japanese characters meaning "FERROELECTRIC" shown in Fig. 3 in the explanation of the prior art are displayed. The portions of the display where the picture elements are provided with the oblique lines represent that, the transformation data Rx of the picture elements is the data which indicates that display data displayed at present and display data to be displayed in the following frame are different.

Fig. 14 and Fig. 15 are waveform diagrams showing respective output signals outputted from the control circuit 24 to the FLCDC 21 at switching operation of the picture screen. Fig. 14 (1) and Fig. 15 (1) are waveform diagrams showing a clock YCLK for sequentially transferring the selective signal YI which selects the scanning electrodes L in a shift register, not shown, included in the scanning side driving circuit 11, Fig. 14 (2) and Fig. 15 (2) are waveform diagrams showing the selective signal YI, and Fig. 14 (3) and Fig. 15 (3) show display data DATA corresponding to each picture element of the FLCDC 21. Fig. 14 (4) and Fig. 15 (4) are waveform diagrams showing the clock LCLK given to the scanning side driving circuit 31 at every one selective time of the scanning electrodes L. Fig. 14 (5) is an expanded waveform diagram showing one period of the clock YCLK, Fig. 14 (6) is an expanded waveform diagram showing one one period of the clock YCLK of the selective signal YI, Fig. 14 (7) is an expanded waveform diagram showing one period of the clock YCLK of the display data DATA, Fig. 14 (8) is a waveform diagram showing data transfer clock XCLK for sequentially transferring the display data DATA in a shift register, not shown, included in the signal side driving circuit 32, Fig. 14 (9) is an expanded waveform diagram of a latch pulse LP which gives timing for taking in and holding the display data DATA in the shift register of the signal side driving circuit 32, in a separate register, not shown, included in the same signal side driving circuit 32, Fig. 14 (10) is a waveform diagram showing the signal VC which designates the kinds of voltage applied to the scanning electrodes L, and Fig. 14 (11) is a waveform

diagram showing the signal VS which designates the kinds of voltage applied to the signal electrode S. Fig. 15 (1) through Fig. 15. (4) show the waveforms following respective waveforms of Fig. 14 (1) through Fig. 14 (4).

Fig. 16 is a waveform diagram showing respective signals outputted from the input control circuit 28 at the operation. Fig. 16 (1) shows a waveform of an input side clock ISCP in which the data transfer clock CLK outputted from the personal computer 22 is delayed by the constant time, Fig. 16 (2) shows a waveform of a timing pulse RE for parallel transformation of the display data Data, Fig. 16 (3) shows data of a line address Ac of the frame memory for display data 25, line memory 26 and frame memory for reference 27 corresponding to the scanning electrodes L, Fig. 16 (4) shows data of a row address As of the frame memory for display data 25 and the frame memory for reference 27 corresponding to the signal electrodes S, Fig. 16 (5) shows a waveform of a timing pulse IOE for reading data from the frame memory for display data 25, line memory 26 and frame memory for reference 27 on the input side in synchronism with the clock ISCP, Fig. 16 (6) shows a waveform of a timing pulse IWE for writing data into the frame memory for display data 25, line memory 26 and frame memory for reference 27 on the input side in synchronism with the clock ISCP, Fig. 16 (7) shows a waveform of a timing pulse OOE for reading data from the output side of the frame memory for display data 25 and the frame memory for reference 27, Fig. 16 (8) shows a waveform of a timing pulse ROE which is outputted to the line memory 26 in synchronism with the clock ISCP, and Fig. 16 (9) also shows a waveform of a timing pulse RWE which is sent out to the line memory 26 in synchronism with the clock ISCP.

Fig. 17 is a waveform diagram showing respective signals outputted from the output control circuit 29 at the operation. Fig. 17 (1) shows a waveform diagram of an output side clock CP, Fig. 17 (2) shows a waveform of a timing pulse LO for serial transformation of data which are outputted to the frame memory for display data 25, line memory 26 and frame memory for reference 27 in synchronism with the clock CP, Fig. 17 (3) shows line difference identification data SAME given to the output control circuit 29 from the line memory 26 shown for reference, Fig. 17 (4) shows a timing pulse OW synchronizing with the clock CP, Fig. 17 (5) shows an output side line address OAc of the memories given to the frame memory for display data 25, line memory 26 and frame memory for reference 27, Fig. 17 (6) shows an output side row address OAs of the memories given to the frame memory for display data 25 and the frame memory for reference 27, Fig. 17 (7) is a waveform diagram showing a timing pulse HCE for producing the clock YCLK given to the scanning side driving circuit 31 in the drive control circuit 30, Fig. 17 (8) is a wa-

veform diagram showing a timing pulse HP for producing the clock LCLK given to the scanning side driving circuit 31, the latch pulse LP given to the signal side driving circuit 32 and respective impressed voltages in the drive control circuit 30, and Fig. 17 (9) is a waveform diagram showing a timing pulse VP for producing the selective signal YI given to the scanning side driving circuit 31 in the drive control circuit 30.

Fig. 18 is a waveform diagram showing respective voltage waveforms applied to the scanning electrodes L1, L2, L3, signal electrodes S5, S6 and picture elements A15, A16, A25, A26. Fig. 18 (1) shows a waveform of the transfer clock YCLK of the selective signal YI in the shift register in the scanning side driving circuit 31 for reference, Fig. 18 (2) shows a waveform of the selective signal YI and Fig. 18 (3) shows a waveform of the clock LCLK which gives the timing of one selective time. Fig. 18 (4) shows an impressed voltage waveform to the scanning electrode L1, Fig. 18 (5) shows an impressed voltage waveform to the scanning electrode L2, Fig. 18 (6) shows an impressed voltage waveform to the scanning electrode L3, Fig. 18 (7) shows an impressed voltage waveform to the signal electrode S5, Fig. 18 (8) shows an impressed voltage waveform to the signal electrode S6, Fig. 18 (9) shows an effective voltage waveform applied to the picture element A15, Fig. 18 (10) shows an effective voltage waveform applied to the picture element A16, Fig. 18 (11) shows an effective voltage waveform applied to the picture element A25 and Fig. 18 (12) shows an effective voltage waveform applied to the picture element A26. In Fig. 18 (6) and Fig. 18 (7), a symbol E, F in parentheses corresponds to the non-symbolic picture element in Fig. 8, that is, it indicates that the non-rewriting voltage G is applied to the non-symbolic picture element in Fig. 8.

Next, the operation whereby the picture screen of the FLCD 21 is switched to a state displaying the Japanese characters meaning "ORDINARY DIELECTRIC" from a state displaying the Japanese characters meaning "FERROELECTRIC", in case the FLCD 21 in the display system is driven by a driving method using the impressed voltage of Fig. 6 shown in the description of the conventional example, is described with reference to Fig. 12 through Fig. 18. In this case, however, one selective time (6.t0) is about 600 microsecond.

In a frame wherein the Japanese characters meaning "FERROELECTRIC" are displayed on the picture screen of the FLCD 21, display data Data held in the frame memory for display data 25 in the state of Fig. 3 shown in the description of the conventional example.

Under this state, display data Data displaying the Japanese characters meaning "ORDINARY DIELECTRIC" are transmitted to the frame memory for display data 25 from the personal computer 22. Then,

from the frame memory for display data 25, transformation data Rx of one picture screen, which is the difference between "ORDINARY DIELECTRIC" and "FERROELECTRIC" and shown schematically in Fig. 13 is outputted to the line memory 26 and the frame memory for reference 27. Although the transformation data Rx is held as it is in the frame memory for reference 27, in the line memory 26, the transformation data Rx for one scanning electrode are held en masse. That is, referring to Fig. 13, when there is even one picture element indicated by the "dark" display in the picture elements on one scanning electrode L, or when there is the picture element whose display data differ in the new and old frames, "1" is held as line difference identification data SAME, and when there is no picture element which is indicated by the "dark" display, "0" is held.

The operation abovementioned is controlled by the input control circuit 28. That is, in the input control circuit 28, the horizontal synchronizing signal HD and the vertical synchronizing signal VD outputted from the personal computer 22 are used for initialization, and the clock ISCP obtained by delaying the data transfer clock CLK outputted from the personal computer 22 by a constant time is used as a clock, and outputted to the frame memory for display data 25 with the clock ISCP and the timing pulse RE for parallel transformation of the display data Data. Also, in synchronism with the clock ISCP, a timing pulse IOE for reading out data from the memories 25, 26 and 27, a timing pulse IWE for writing data into the memories 25, 26 and 27 and address data switching an output-side line address OAc and an input-side line address OAc of these memories as a line address Ac accessing the memories 25, 26 and 27 are outputted from the input control circuit 28. Furthermore, from the input control circuit 28, in synchronism with the clock CP outputted from the output control circuit 29, a timing pulse OOE for reading out data from the memories 25, 27, and address data switching an output-side row address OAs and an input-side row address OAs of respective memories as a row address As accessing these memories are outputted.

Next, data DO held in the frame memory for display data 25 and data DRE held in the frame memory for reference 27 are outputted to the drive control circuit 30. At this time, a data transfer time T1 necessary for actually outputting the data DO and DRE, is set sufficiently shorter than one selective time (6.t0), and the line difference data SAME of the line memory 26 corresponding to the scanning electrode L is confirmed by the output control circuit 29 before entering the data transfer time T1. At this time, when a state wherein the line difference identification data SAME is "0" continues, the operation to confirm the line difference identification data SAME corresponding to the following scanning electrode L is repeated up to a maximum of four times, and when the line differ-

ence identification data SAME is still not "1", the data DO and DRE of the fourth scanning electrode L are outputted to the drive control circuit 30. When the line difference identification data SAME of "1" appears before completion of the four operations, the data DO, DRE corresponding to the scanning electrode L are outputted to the drive control circuit 30. In the line memory 26, after the line difference identification data SAME has been outputted, the content of line difference identification data SAME corresponding to the scanning electrode L is reset to "0".

A series of operations above mentioned are effected by timing pulses ROE, RWE controlled by a timing pulse OW outputted from the output control circuit 29 and outputted to the line memory 26 from the input control circuit 28, and a timing pulse LO which is outputted to the frame memory for display data 25, line memory 26 and frame memory for reference 27 from the output control circuit 29.

Hereinafter, when display data Data "ORDINARY DIELECTRIC" is continued to be outputted to the frame memory for display data 25 from the personal computer 22, though the frame memory for display data 25 is to hold the character display data "ORDINARY DIELECTRIC" continuously, all of the transformation data Rx outputted from the frame memory for display data 25 become "0" corresponding to the picture elements with no oblique lines in Fig. 13. Although the transformation data Rx are outputted to the line memory 26 and the frame memory for reference 27, so as to hold data of the frame memory for reference 27, as long as the line difference identification data SAME of the line memory 26 do not become "0", data on the corresponding scanning electrode L are not rewritten to "0".

From the output control circuit 29 to the drive control circuit 30, a timing pulse VP for producing the selective signal YI inputted to the scanning side driving circuit 31, a timing pulse HCE for producing the clock YCLK inputted to the scanning side driving circuit 31, a timing pulse HP for producing the clock LCLK inputted to the scanning side drawing circuit 31, a latch pulse LP given to the signal side driving circuit 32 and respective impressed voltages, are outputted respectively.

As a result of the above operations, from the control circuit 24 to the FLCD 21, respective signals shown in Fig. 14 and Fig. 15 are outputted. That is, display data held in the frame memory for display data 25 changes from that of the character display of Japanese character meaning "FERROELECTRIC" to that of the character display of Japanese character meaning "ORDINARY DIELECTRIC", data of the frame memory for reference 27 become as shown schematically in Fig. 13, and the line difference identification data SAME of becomes "1" from the scanning electrodes L1 to L16, and "0" from the scanning electrodes L17 to L32.

Now, assuming that a display is started from the scanning electrode L1, first a line address OAc = 1 is inputted to each of the memories 25, 26 and 27 from the output control circuit 29 via the input control circuit 28, at this time, the line difference identification data SAME of the line memory 26 becomes "1", and data DO of the frame memory for display data 25 and data DRE of the frame memory for reference 27 corresponding to the scanning electrode L1 are transferred to the drive control circuit 30.

The aforesaid operations are repeated from the scanning electrodes L2 to L16. Next, when a line address OAc = 17 is outputted to the memories 25, 26 and 27 from the output control circuit 29, the line difference identification data SAME of the line memory 26 becomes "0", and the line address OAc outputted from the output control circuit 29 is incremented by 1 and switched to 18. Thereafter, though the line difference identification data SAME is continued as "0", since this operation is limited to a maximum of four times, when the line address OAc becomes 20, the data DO of the frame memory for display data 25 and the data DRE of the frame memory for reference 27 corresponding to the scanning electrode L20 are transferred to the drive control circuit 30. The same operations are repeated for the rest.

Impressed voltages to the scanning electrodes L1, L2, L3, signal electrodes S5, S6 and picture elements A15, A16, A25, A26 at this time are as shown in Fig. 18.

In this case, the kinds of signal voltage applied to the signal electrodes S are decided by the data DO of the frame memory for display data 25 and the data DRE of the frame memory for reference 27. That is, for example, when the data DO is "bright" display data and the data DRE is data indicating the difference between display data in the present frame and the following frame, a rewriting bright voltage C is selected as the signal voltage, and when the data DO is "dark" display data and the data DRE is data indicating the difference between display data in the present and after frames, a rewriting dark voltage D is selected as the signal electrode. Furthermore, in case the data DO is "bright" display data and the data DRE is data indicating that there is no difference between display data in the present and after frames, and in case the data DO is "dark" display data and the data DRE is data indicating that there is no difference between display data in the present frame and the following frame, in both cases, a non-rewriting voltage G is selected as the signal electrode.

In this embodiment, for the scanning electrodes wherein there is no picture element which differs between display data displayed at present and display data to be displayed in the following frame, even when these scanning electrodes continue, only one out of four is selected in the following frame, so that an apparent period of the frame is shortened by the

number of scanning electrodes being not selected. It may be so arranged that all of the scanning electrodes for which there is no picture element which differs between display data in the present and following frames are not selected.

Now, for example, a display screen of a personal computer is rarely rewritten all at once, thus the number of scanning electrodes for which display data are changed can be substantially reduced depending upon a program design. Particularly, in the case of a word processor, there is little chance that characters for several lines are rewritten at a time since the display data for each character is inputted, therefore, when one screen corresponds to one page, the number of scanning electrodes, for which the display data used to be rewritten, per one screen is about one line of characters and very few. Accordingly, in case the display control apparatus is used for display control of such personal computer and word processor, a frame period is shortened considerably and a response speed at which the screen is rewritten for the input is quickened.

In the embodiment aforementioned, for the purpose of simplification, the case wherein display on the FLCFD 21 having the picture elements of 16 x 32 has been described, as a result of applying actually the above embodiment in the FLCFD having the picture elements of 1024 x 1024, it has been confirmed that the display of quick response speed without flicker is obtained.

Now, in a display method applied in the embodiment, or a display method using the impressed voltages of respective waveforms in Fig. 6 shown in the description of the prior art, as will be apparent from a waveform diagram shown in Fig. 18, since three kinds of impressed voltages, that is, the rewriting bright voltage C, the rewriting dark voltage D and the non-rewriting voltage G are outputted from the signal side driving circuit 32, as compared with the signal side driving circuit requiring only two kinds of impressed voltages, the manufacturing cost is high.

However, by observing the waveforms of Fig. 6 carefully, it becomes clear that a first-half waveform of the non-rewriting voltage G is equal to a first half waveform of the rewriting dark voltage D, and a later-half waveform of the non-rewriting voltage G is equal to a later-half waveform of the rewriting bright voltage C.

Therefore, viewing this point, when the signal value for selecting the impressed voltage given to the signal side driving circuit 32 is decided in such a way that, the rewriting dark voltage D and the non-rewriting voltage G show the same value in the first half of the signal value, and the rewriting bright voltage C and the non-rewriting voltage G show the same value in the later half thereof, the cost of the signal side driving circuit 32 can be cut.

In this embodiment, polarizing plates are dis-

posed so that the polarizing axis is parallel or orthogonal to the local alignment of the liquid crystal molecules. However, when polarizing plates are disposed so that an angle of the polarizing axis and the liquid crystal molecules is an angle of 10° through 80°, the rewriting bright voltage C is used as a rewriting dark voltage and the rewriting dark voltage D is used as a rewriting bright voltage.

Therefore, it may be that a waveform of a non-rewriting voltage is composed of a first-half waveform, which can not rewrite a picture element by combining with a selective voltage, of either the rewriting bright voltage or the rewriting dark voltage and a later-half waveform, which can not rewrite a picture element by combining with a selective voltage, of either the rewriting bright voltage or the rewriting dark voltage.

Specific examples of constitutional circuits of respective portions of the control circuit 24 are respectively shown in Fig. 19 through Fig. 22. In the figures, Fig. 19 shows the output control circuit 29 which is constituted by, four counters 33a to 33d, three D flip-flops 34a to 34c, six NAND gates 35a to 35f, one AND gate 36a, four NOR gates 37a to 37d, two OR gates 38a, 38b and four DIP switches 39a to 39d.

Fig. 20 shows the frame memory for display data 25 which is constituted by, eight NOT gates 40a to 40h, eight EX-OR gates 41a to 41h, two shift registers with latch 42a, 42b, one 3-state output buffer 43, one shift register 44, one static RAM (Random Access Memory) 45, two D flip-flops 46a, 46b, five NAND gates 47a to 47e, four AND gates 48a to 48d and a switch 49.

Fig. 21 shows the line memory 26 which is constituted by, one static RAM 50, four NOT gates 51a to 51d, two 3-state output buffers 52a, 52b, four D flip-flops 53a to 53d, two NAND gates 54a, 54b and ten AND gates 55a to 55j.

Moreover, Fig. 22 shows the frame memory for reference 27 which is constituted by, seven NOT gates 56a to 56g, one static RAM 57, two D flip-flops 58a, 58b, one three-state output buffer 59, one shift register 60, eleven NAND gates 61a to 61k, four AND gates 62a to 62d and eight OR gates 63a to 63h.

In the embodiment, though the case of driving method using three kinds of voltages, a rewriting bright voltage C, a rewriting dark voltage D and a non-rewriting voltage G, as the signal voltage has been described, when a flicker is ignored, a frame period can be shortened in the same manner even in the case of driving method in which the non-rewriting voltage G is not used as the signal voltage.

The invention may be embodied in other specific forms without departing from its scope as defined by the claims.

Claims

1. A controller for a ferroelectric liquid crystal display panel (21), the panel comprising an array (Aij) of picture elements each defined by the intersection of one of a plurality of scanning electrodes (Li) and one of a plurality of signal electrodes (Sj), and ferroelectric liquid crystal disposed therebetween, the controller comprising:
 - control means (28,29,30) for supplying selection signals for selecting scanning electrodes of the display panel and, during the selection of each scanning electrode, data signals for applying data to the signal electrodes of the display panel;
 - characterised by:
 - a first memory (25) which receives and stores the data for the next display frame;
 - a second memory (27) which receives and stores that part of the data for the current display frame which differs from said data for the next display frame;
 - a line memory (26) for storing the result of a comparison, on a line-by-line basis, of said data for the next display frame with said data for the current display frame, for each line; and
 - said control means (28,29,30) being arranged to supply, according to the content of said line memory (26), a succession of said selection signals which excludes selection signals for all or certain of all the scanning electrodes which correspond to lines for which said comparison indicates identity of data content between the current and next display frames, thereby reducing the length of time required to update a frame of data displayed on the display panel.
2. A display panel controller according to claim 1, further comprising signal electrode driving means (32) for generating driving signals for the signal electrodes of the display panel in dependence on said data signals, said driving signals comprising a first driving signal (C) for rewriting a picture element from a dark state to a bright state, a second driving signal (D) for rewriting a picture element from a bright state to a dark state, and a third driving signal (G) for driving a picture element which does not change state, wherein the waveform of the third driving signal (G) is composed solely of components of the waveforms of the first and second driving signals (C,D).
3. A method of controlling a ferroelectric liquid crystal display panel (21), the panel comprising an array (Aij) of picture elements each defined by the intersection of one of a plurality of scanning electrodes (Li) and one of a plurality of signal electro-

des (S_j), and ferroelectric liquid crystal disposed therebetween, the method comprising:

supplying to the display panel, selection signals for selecting scanning electrodes thereof and, during the selection of each scanning electrode, data signals for applying data to the signal electrodes thereof;

characterised by:

storing in a first memory (25) the data for the next display frame;

storing in a second memory (27) that part of the data for the current display frame which differs from said data for the next display frame;

comparing, on a line-by-line basis, said data for the next display frame with said data for the current display frame;

storing in memory (26) the result of the comparison for each line; and

the supplying step comprising outputting, according to the content of said memory (26), a succession of said selection signals which excludes selection signals for all or certain of all the scanning electrodes which correspond to lines for which said comparison indicates identity of data content between the current and next display frames, thereby reducing the length of time required to update a frame of data displayed on the display panel.

4. A display control method according to claim 3, further comprising generating driving signals for the signal electrodes of the display panel in dependence on said data signals, said driving signals comprising a first driving signal (C) for rewriting a picture element from a dark state to a bright state, a second driving signal (D) for rewriting a picture element from a bright state to a dark state, and a third driving signal (G) for driving a picture element which does not change state, wherein the waveform of the third driving signal (G) is composed solely of components of the waveforms of the first and second driving signals (C,D).

Patentansprüche

1. Steuerung für eine ferroelektrische Flüssigkristall-Anzeigetafel (21), die ein Array (A_{ij}) von Bildelementen, von denen jedes durch die Schnittstelle einer von mehreren Abrasterelektroden (L_i) mit einer von mehreren Signalelektroden (S_j) festgelegt ist, und einen dazwischen angeordneten ferroelektrischen Flüssigkristall aufweist, mit:
- einer Steuereinrichtung (28, 29, 30) zum Liefern von Auswahlsignalen zum Auswählen von Abrasterelektroden der Anzeigetafel,

und während der Auswahl jeder Abrasterelektrode, von Datensignalen zum Anlegen von Daten an die Signalelektroden der Anzeigetafel;

gekennzeichnet durch

- einen ersten Speicher (25), der die Daten für das nächste Anzeigevollbild empfängt und einspeichert;
- einen zweiten Speicher (27), der denjenigen Teil der Daten für das aktuelle Anzeigevollbild empfängt und einspeichert, die sich von den Daten für das nächste Anzeigevollbild unterscheiden;
- einen Zeilenspeicher (26) zum Einspeichern des Ergebnisses eines Vergleichs auf zeilenweiser Basis zwischen den Daten für das nächste Anzeigevollbild und den Daten für das aktuelle Anzeigevollbild, für jede Zeile;
- wobei die Steuereinrichtung (28, 29, 30) so ausgebildet ist, daß sie abhängig vom Inhalt des Zeilenspeichers (26) eine Folge von Auswahlsignalen liefert, wobei Auswahlsignale für alle oder bestimmte unter allen Auswahlelektroden ausgeschlossen sind, die Zeilen entsprechen, für die der Vergleich Identität des Dateninhalts für das aktuelle und das nächste Anzeigevollbild anzeigt, um dadurch die Dauer der Zeit zu verkürzen, die erforderlich ist, um ein Vollbild von auf der Anzeigetafel angezeigten Daten zu aktualisieren.

2. Anzeigetafel-Steuerung nach Anspruch 1, ferner mit einer Signalelektroden-Treibereinrichtung (32) zum Erzeugen von Treibersignalen für die Signalelektroden der Anzeigetafel abhängig von den Datensignalen, wobei die Treibersignale ein erstes Treibersignal (C) zum Überschreiben eines Bildelements von einem dunklen Zustand in einen hellen Zustand, ein zweites Treibersignal (D) zum Überschreiben eines Bildelements von einem hellen Zustand in einen dunklen Zustand und ein drittes Treibersignal (G) zum Ansteuern eines Bildelements, dessen Zustand sich nicht ändert, umfassen, wobei der Signalverlauf des dritten Treibersignals (G) nur aus Komponenten der Signalverläufe des ersten und zweiten Treibersignals (C, D) besteht.

3. Verfahren zum Steuern einer ferroelektrischen Flüssigkristall-Anzeigetafel (21), die ein Array (A_{ij}) von Bildelementen, die jeweils durch die Schnittstelle einer von mehreren Abrasterelektroden (L_i) mit einer von mehreren Signalelektroden (S_j) festgelegt sind, und einen dazwischen angeordneten ferroelektrischen Flüssigkristall aufweist, das folgendes umfaßt:

- Zuführen von Auswahlsignalen an die Anzeigetafel, zum Auswählen von Abrasterelektroden derselben, und, während der Auswahl jeder Abrasterelektrode, von Datensignalen zum Anlegen von Daten an die Signalelektroden derselben;
gekennzeichnet durch
- Einspeichern von Daten für das nächste Anzeigevollbild in einen ersten Speicher (25);
- Einspeichern desjenigen Teils der Daten für das aktuelle Anzeigevollbild, die sich von den Daten für das nächste Anzeigevollbild unterscheiden, in einen zweiten Speicher (27);
- Vergleichen, Zeile für Zeile, der Daten für das nächste Anzeigevollbild mit den Daten für das aktuelle Anzeigevollbild;
- Einspeichern des Vergleichsergebnisses für jede Zeile in einen Speicher (26);
- wobei der Zuführschritt das Ausgeben, abhängig vom Inhalt des Speichers (26), einer Folge der Auswahlsignale beinhaltet, ohne Auswahlsignale für alle oder bestimmte unter allen Abrasterelektroden, die Zeilen entsprechen, für die der Vergleich Identität des Dateninhalts zwischen dem aktuellen und dem nächsten Anzeigevollbild anzeigt, um dadurch die Zeitdauer zu verkürzen, wie sie erforderlich ist, um ein auf der Anzeigetafel angezeigtes Datenvollbild zu aktualisieren.

4. Anzeigesteuerverfahren nach Anspruch 3, bei dem ferner Treibersignale für die Signalelektroden der Anzeigetafel abhängig von den Datensignalen erzeugt werden, wobei die Treibersignale ein erstes Treibersignal (C) zum Überschreiben eines Bildelements aus einem dunklen Zustand in einen hellen Zustand, ein zweites Treibersignal (D) zum Überschreiben eines Bildelements von einem hellen Zustand in einen dunklen Zustand und ein drittes Treibersignal (G) zum Ansteuern eines Bildelements ohne Zustandsänderung umfassen, wobei der Signalverlauf des dritten Treibersignals (G) nur aus Komponenten der Signalverläufe des ersten und zweiten Treibersignals (C, D) besteht.

Revendications

1. Régisseur pour un panneau d'affichage à cristaux liquides ferroélectriques (21), le panneau comprenant une matrice (A_{ij}) d'éléments d'image dont chacun est défini par l'intersection de l'une de plusieurs électrodes de balayage (Li) et de l'une de plusieurs électrodes de signaux (Sj), et des cristaux liquides ferroélectriques placés en-

tre celles-ci, le régisseur comprenant :

des moyens de commande (28, 29, 30) pour délivrer des signaux de sélection afin de sélectionner des électrodes de balayage du panneau d'affichage et, pendant la sélection de chaque électrode de balayage, des signaux de données afin d'appliquer des données aux électrodes de signaux du panneau d'affichage ;

caractérisé par :

une première mémoire (25) qui reçoit et mémorise les données pour l'image d'affichage suivante ;

une seconde mémoire (27) qui reçoit et mémorise la partie des données pour l'image d'affichage en cours, qui diffère desdites données pour l'image d'affichage en cours,

une mémoire de lignes (26) pour mémoriser le résultat d'une comparaison effectuée ligne par ligne desdites données pour l'image d'affichage suivante avec lesdites données pour l'image d'affichage en cours, pour chaque ligne ; et

en ce que lesdits moyens de commande (28, 29, 30) sont conçus pour fournir, en fonction du contenu de ladite mémoire de lignes (26), une succession desdits signaux de sélection, excluant les signaux de sélection pour toutes ou pour certaines des électrodes de balayage, qui correspondent à des lignes pour lesquelles ladite comparaison indique l'identité du contenu de données entre les images d'affichage en cours et suivante, en réduisant par ce moyen le temps nécessaire pour mettre à jour une image de données affichée sur le panneau d'affichage.

2. Régisseur de panneau d'affichage selon la revendication 1, comprenant en outre des moyens d'excitation d'électrode de signaux (32) pour produire des signaux d'excitation pour les électrodes de signaux du panneau d'affichage en fonction desdits signaux de données, lesdits signaux d'excitation comprenant un premier signal d'excitation (C) pour réécrire un élément d'image passant d'un état sombre à un état clair, un second signal d'excitation (D) pour réécrire un élément d'image passant d'un état clair à un état sombre, et un troisième signal d'excitation (G) pour exciter un élément d'image qui ne change pas d'état, la forme d'onde du troisième signal d'excitation (G) étant uniquement constituée de composantes des formes d'onde des premier et second signaux d'excitation (C, D).

3. Procédé de commande d'un panneau d'affichage à cristaux liquides ferroélectriques (21), le panneau comprenant une matrice (A_{ij}) d'éléments d'image dont chacun est défini par l'intersection de l'une de plusieurs électrodes de balayage (Li) et de l'une de plusieurs électrodes de

signaux (S_j), et des cristaux liquides ferroélectriques placés entre celles-ci, le procédé comprenant :

la fourniture au panneau d'affichage de signaux de sélection pour sélectionner les électrodes de balayage de celui-ci et, pendant la sélection de chaque électrode de balayage, de signaux de données pour appliquer des données aux électrodes de signaux dudit panneau d'affichage; 5 10

caractérisé par :

la mémorisation dans une première mémoire (25) des données pour l'image d'affichage suivante ;

la mémorisation dans une seconde mémoire (27) de la partie des données pour l'image d'affichage en cours, qui diffère desdites données pour l'image d'affichage suivante ; 15

la comparaison effectuée ligne par ligne desdites données pour l'image d'affichage suivante avec lesdites données pour l'image d'affichage en cours ; 20

la mémorisation dans une mémoire (26) du résultat de la comparaison pour chaque ligne ; et

en ce que l'étape de fourniture comprend la fourniture en sortie, en fonction du contenu de ladite mémoire (26), d'une succession desdits signaux de sélection, excluant les signaux de sélection pour toutes ou pour certaines des électrodes de balayage, qui correspondent à des lignes pour lesquelles ladite comparaison indique l'identité du contenu de données entre les images d'affichage en cours et suivante, en réduisant par ce moyen le temps nécessaire pour mettre à jour une image de données affichée sur le panneau d'affichage. 25 30 35

4. Procédé de commande d'affichage selon la revendication 3, comprenant en outre la production de signaux d'excitation pour les électrodes de signaux du panneau d'affichage en fonction desdits signaux de données, lesdits signaux d'excitation comprenant un premier signal d'excitation (C) pour réécrire un élément d'image passant d'un état sombre à un état clair, un second signal d'excitation (D) pour réécrire un élément d'image passant d'un état clair à un état sombre, et un troisième signal d'excitation (G) pour exciter un élément d'image qui ne change pas d'état, la forme d'onde du troisième signal d'excitation (G) étant uniquement constituée de composantes des formes d'onde des premier et second signaux d'excitation (C, D). 40 45 50

55

Fig. 1
Prior Art

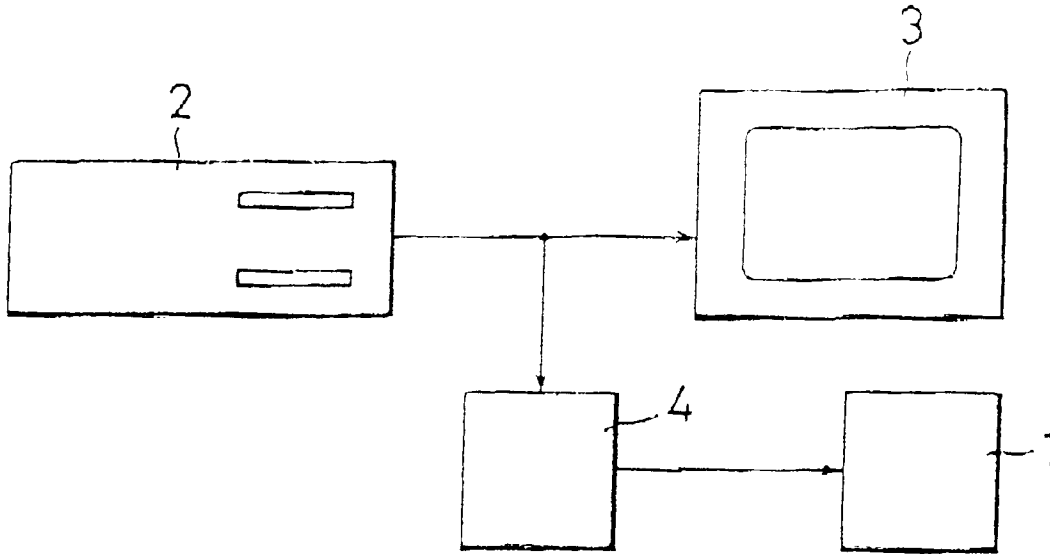
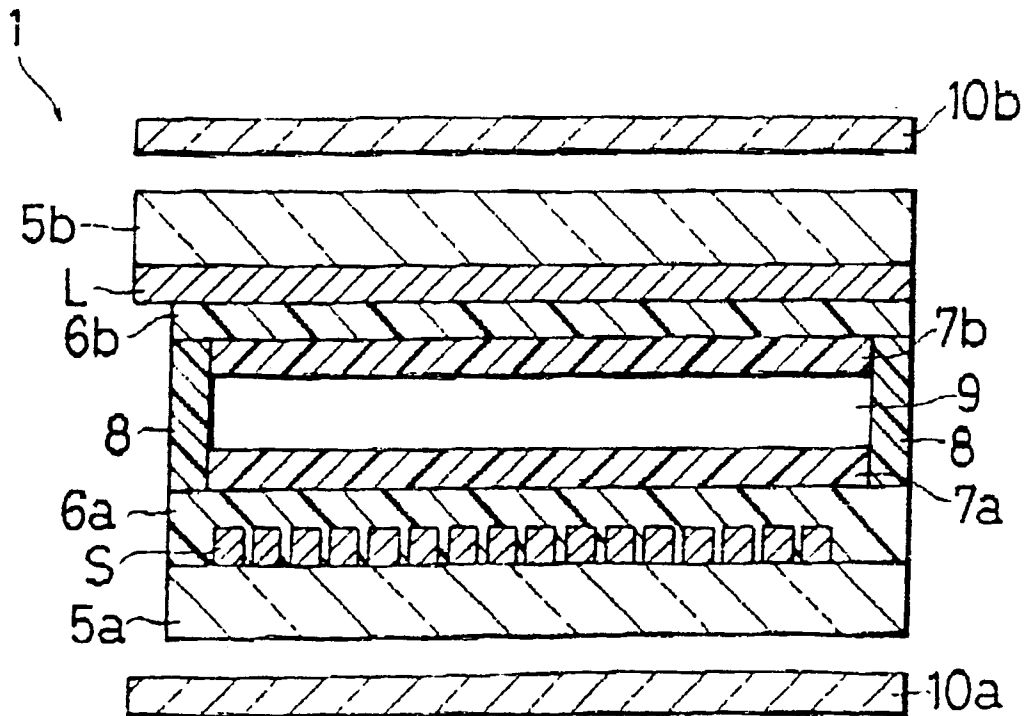


Fig. 2
Prior Art



Prior Art Fig. 3

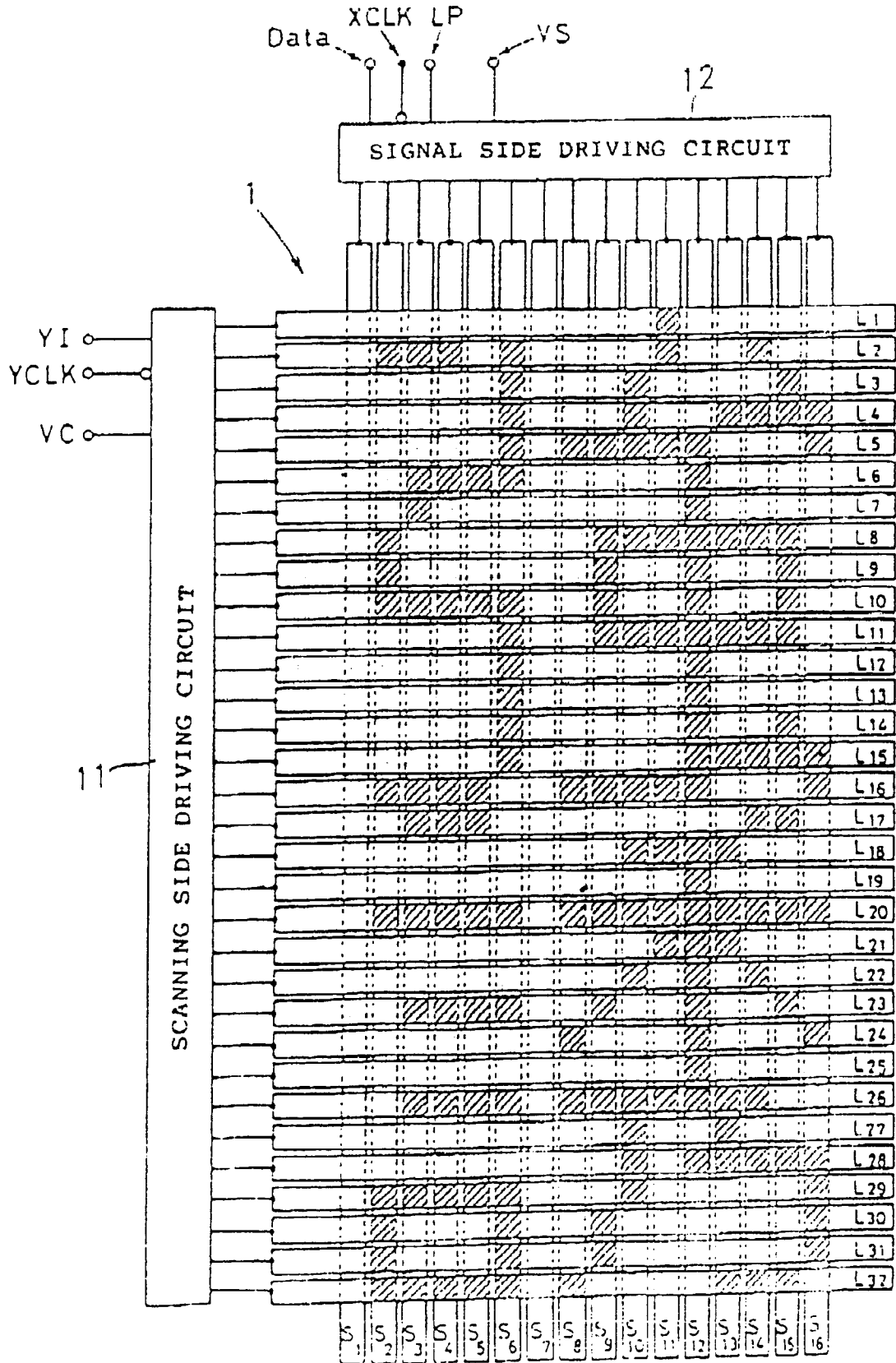


Fig. 4 Prior Art

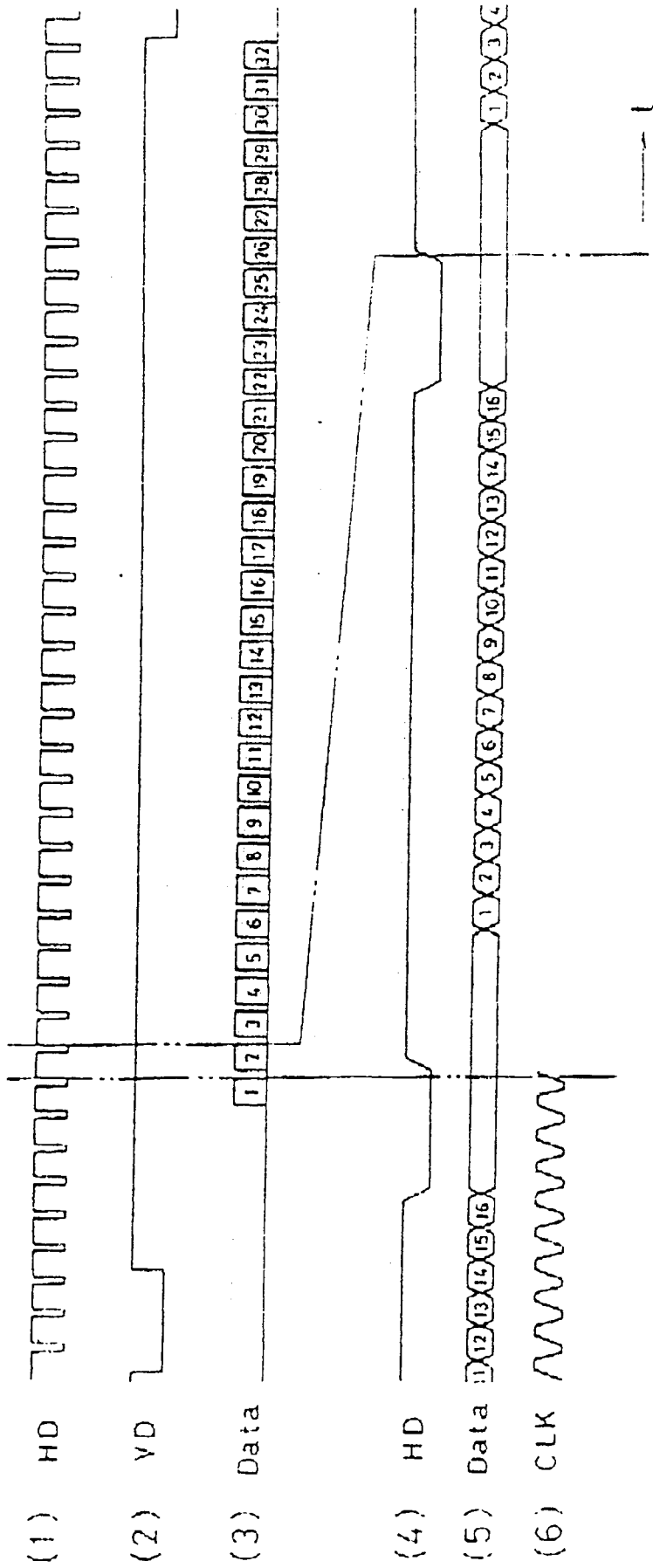


Fig. 5 Prior Art

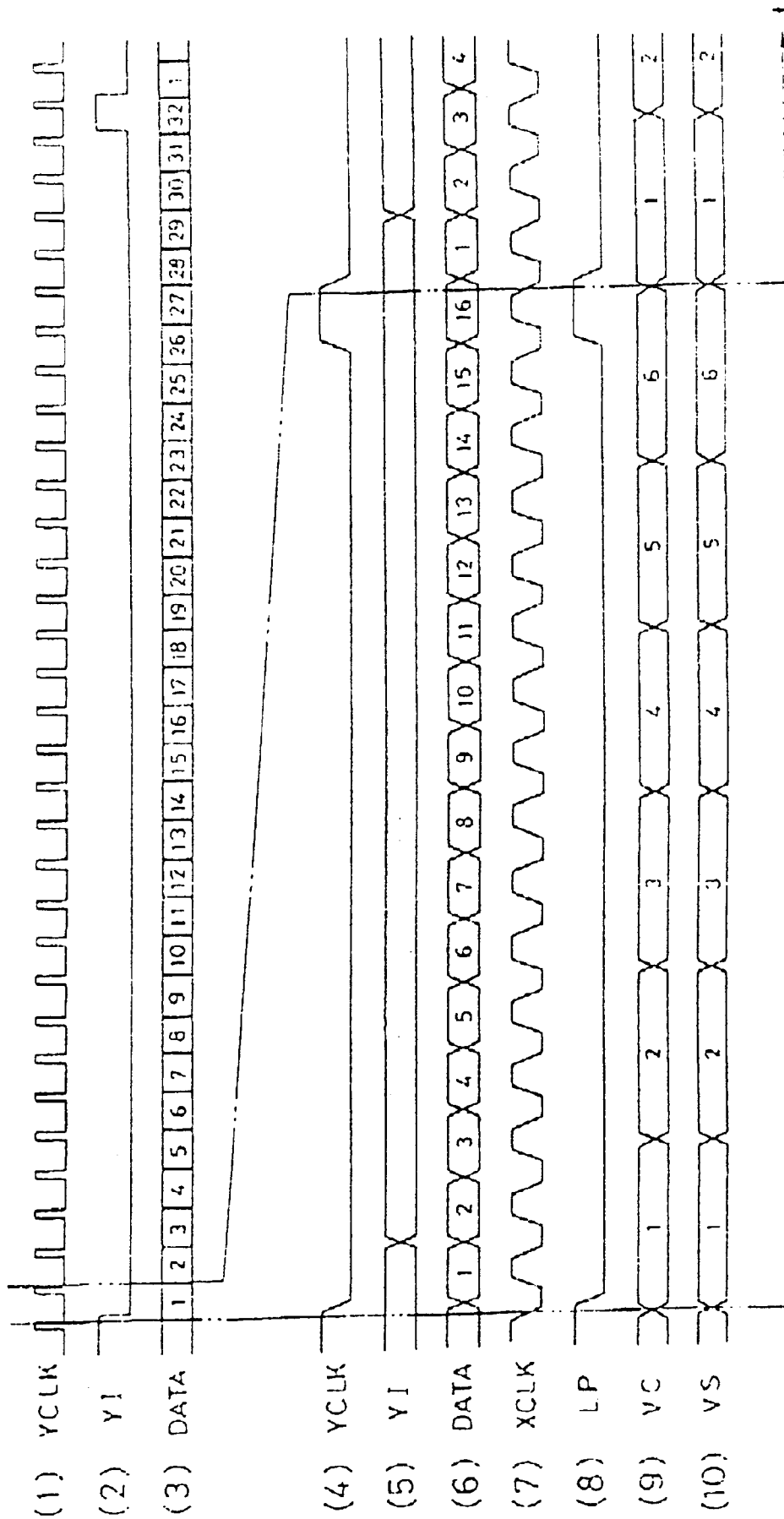
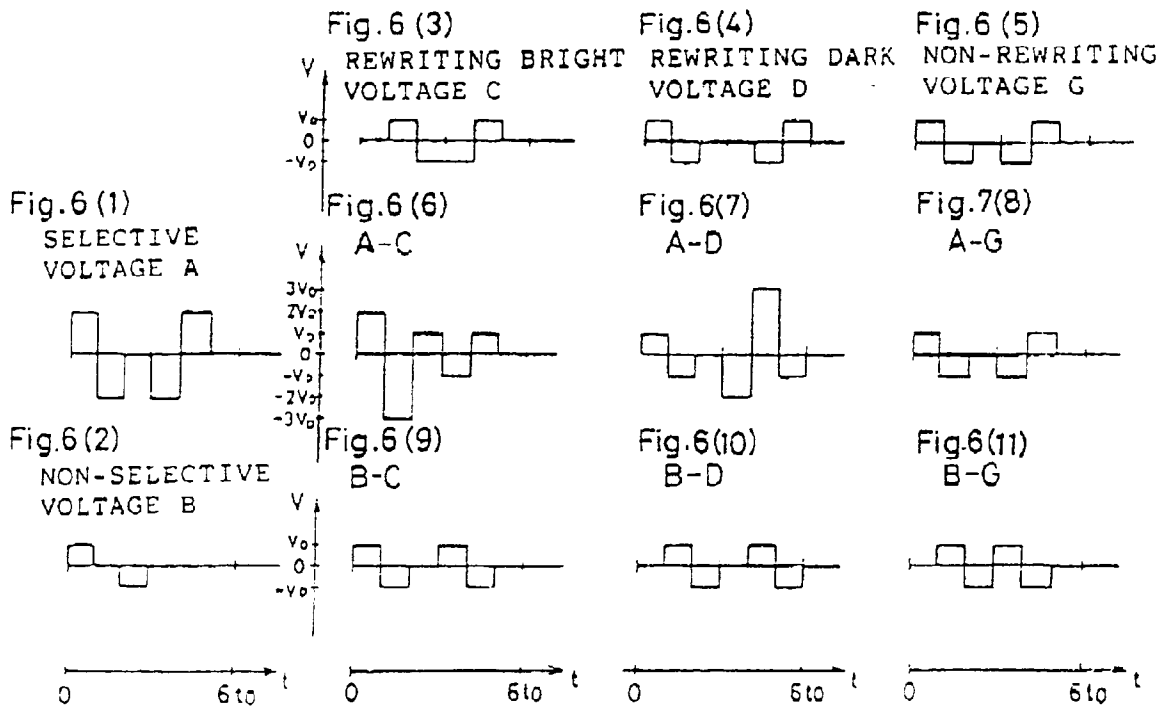
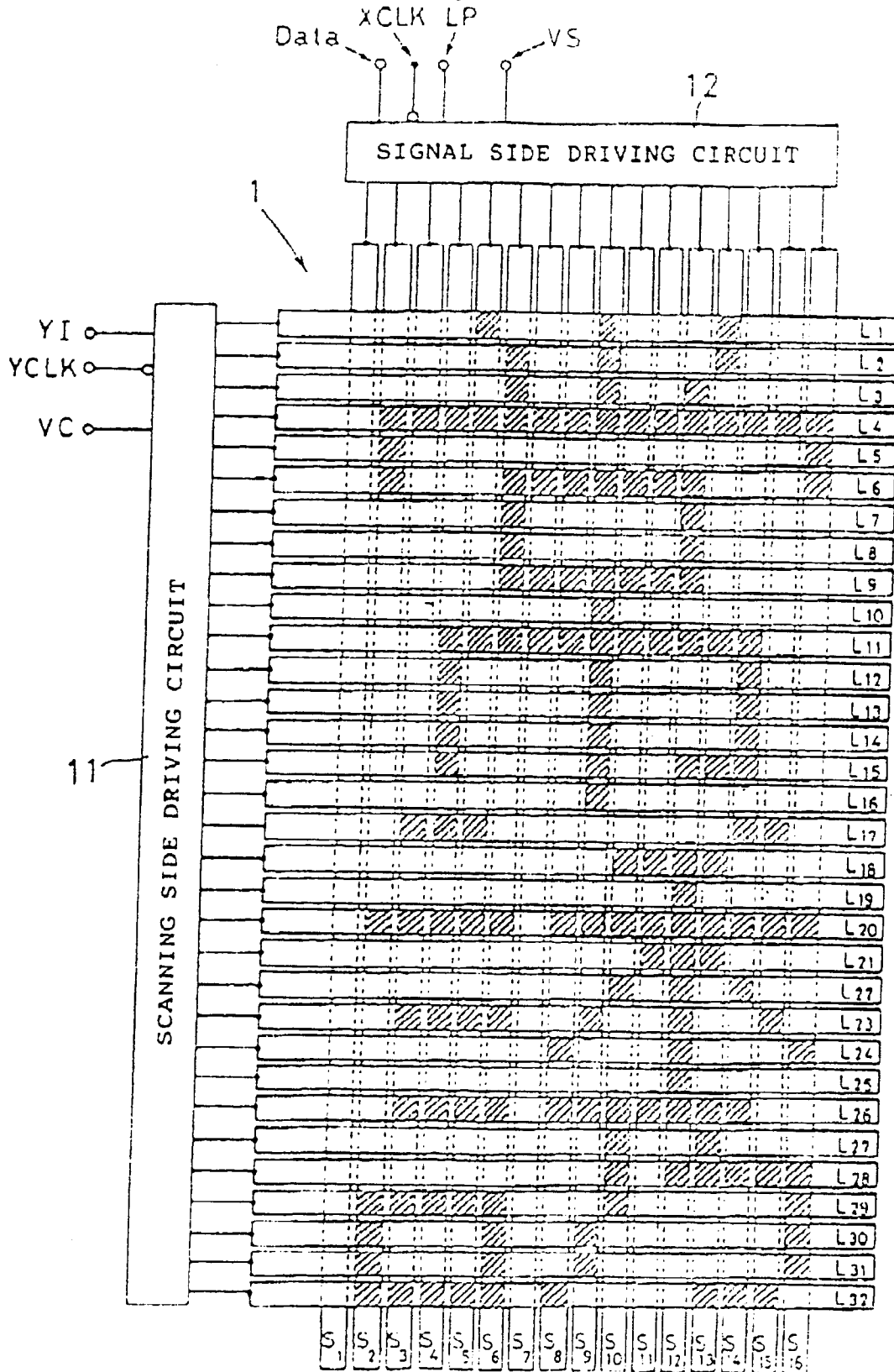


Fig. 6 Prior Art



Prior Art Fig. 7



Prior Art
Fig. 8

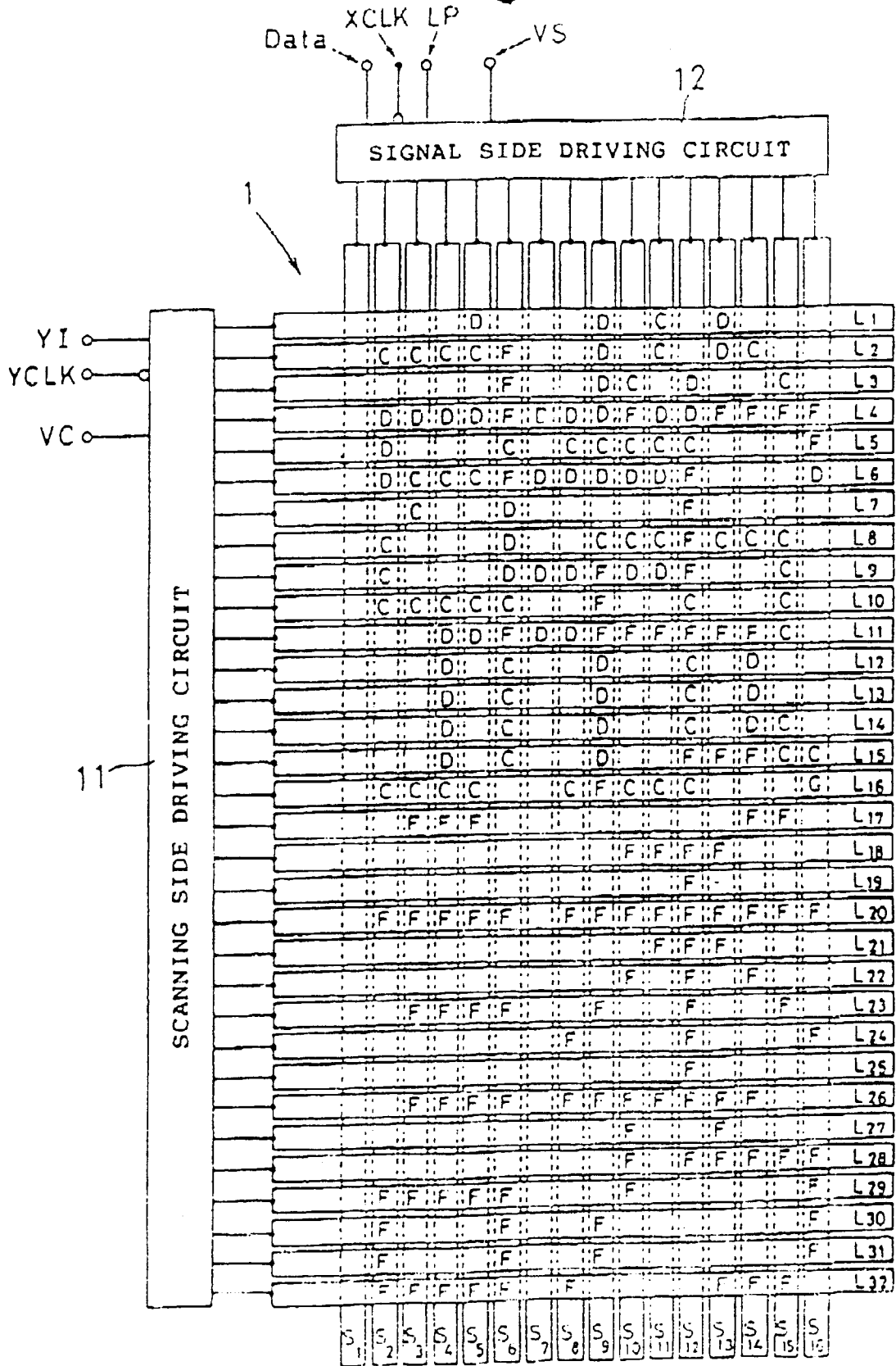


Fig. 9 Prior Art

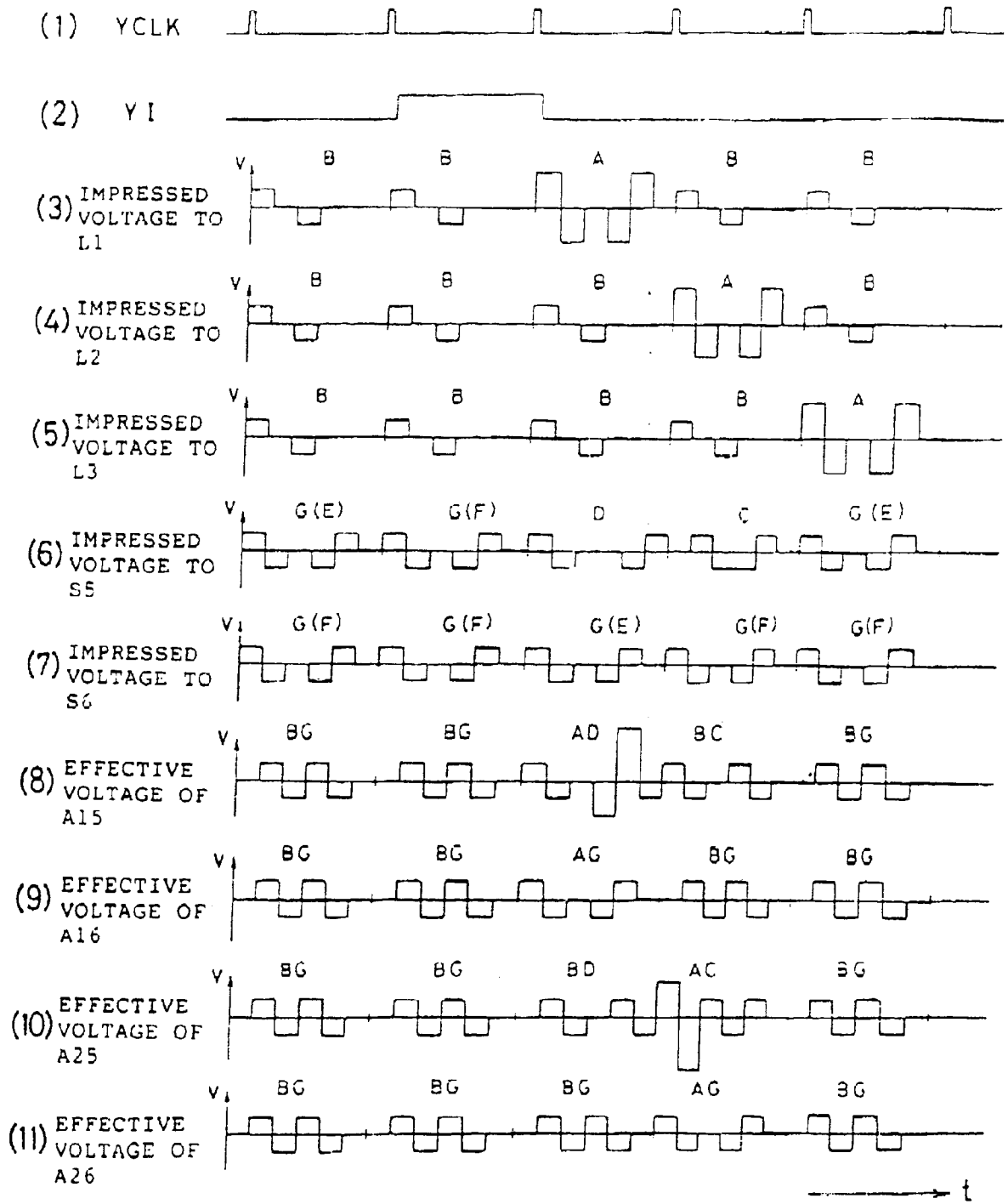


Fig. 10

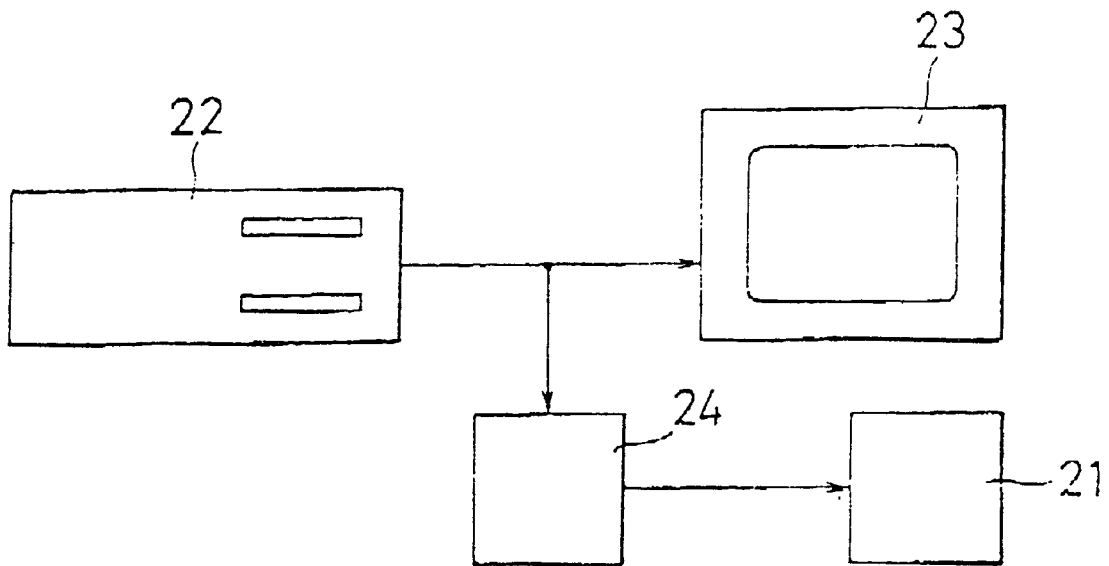


Fig. 11

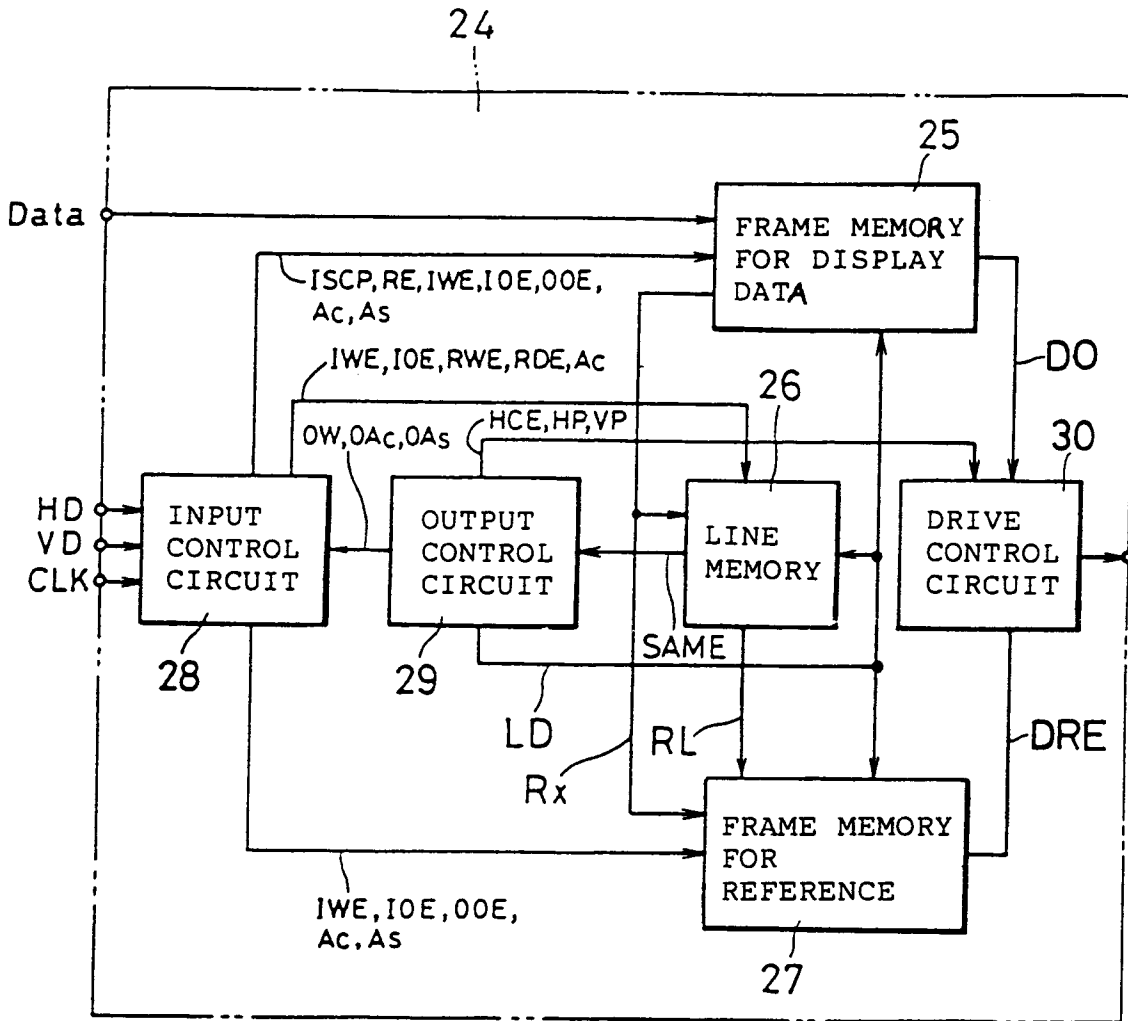


Fig. 12

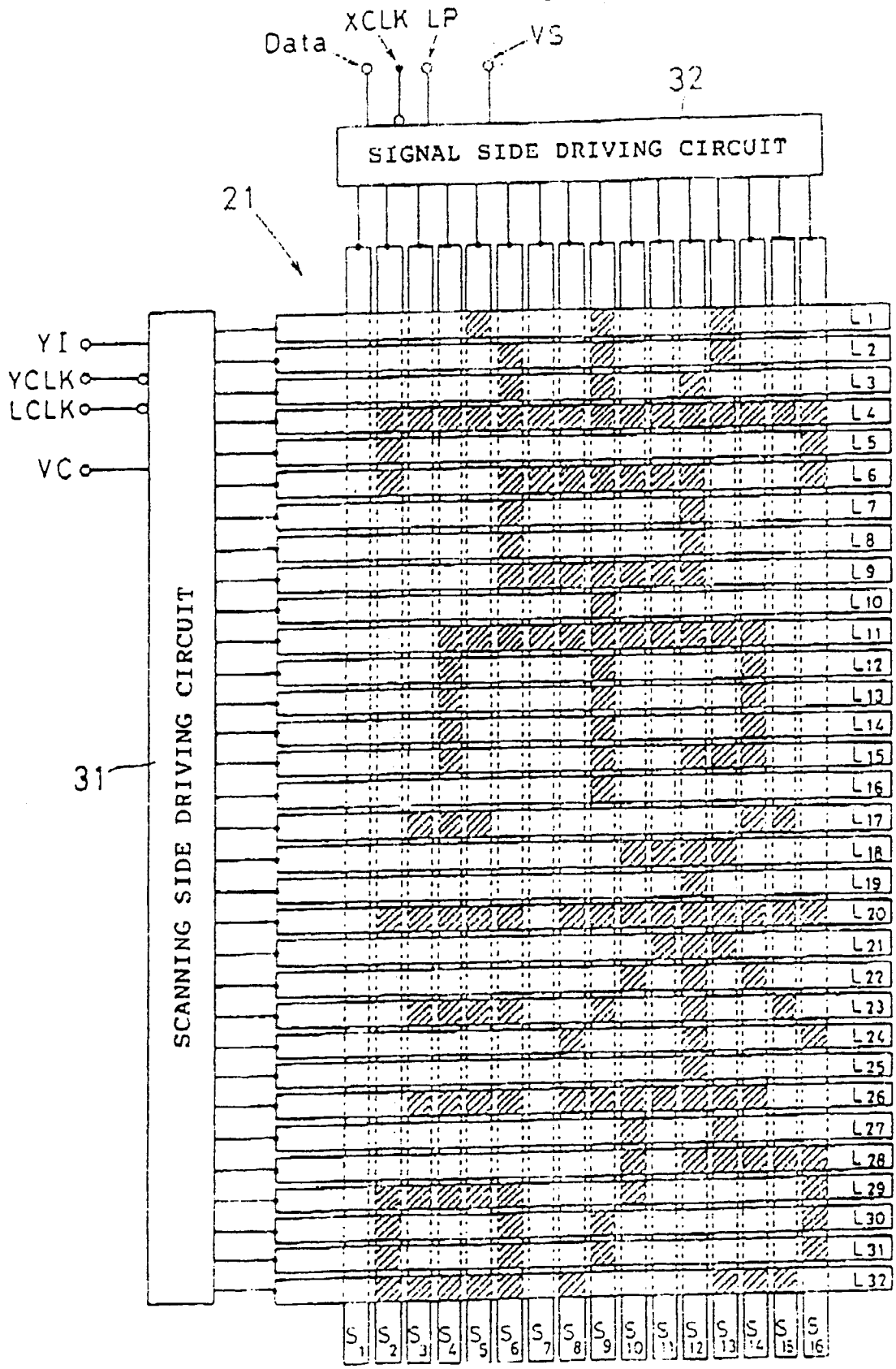


Fig. 13

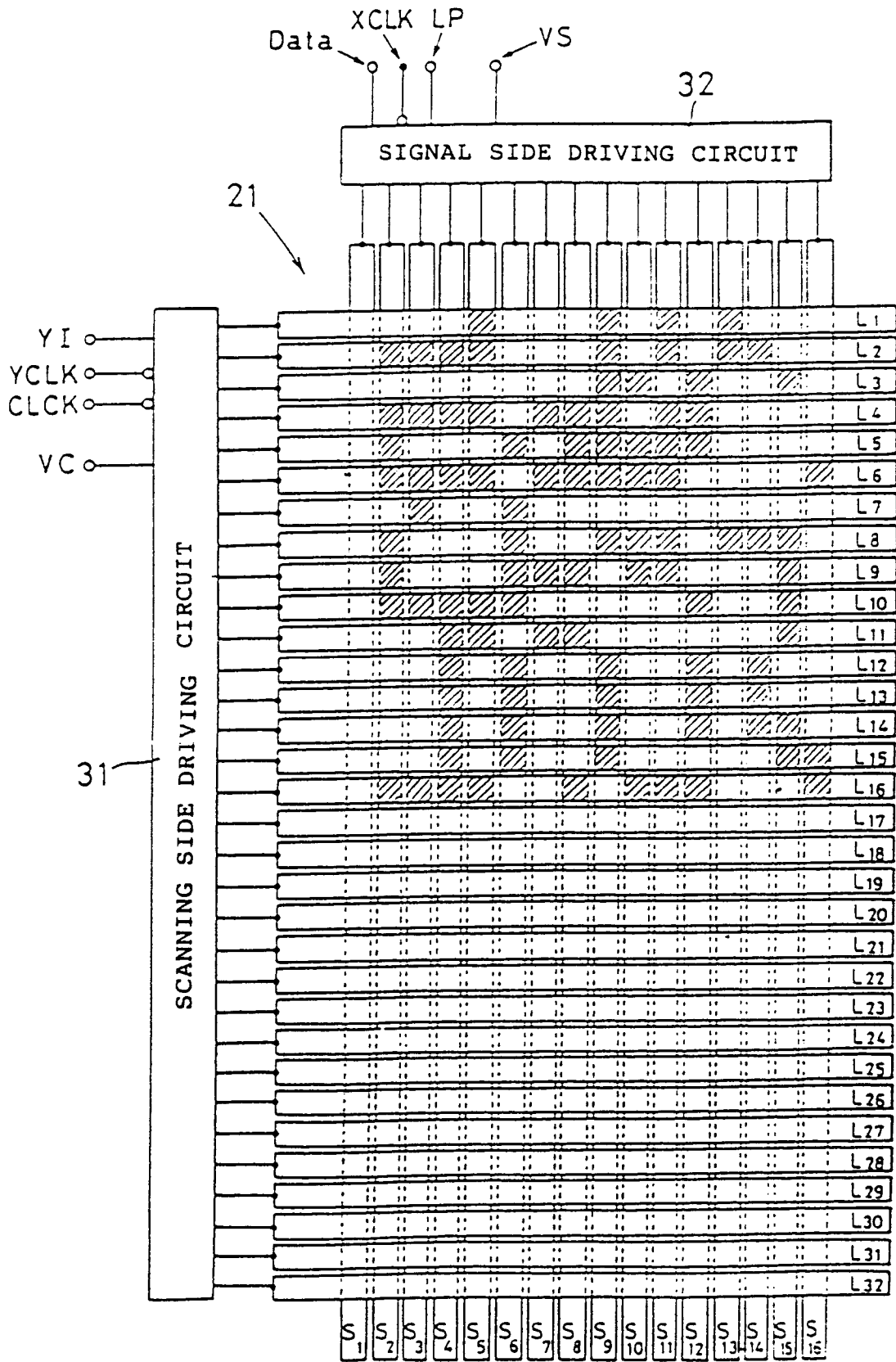


Fig. 14

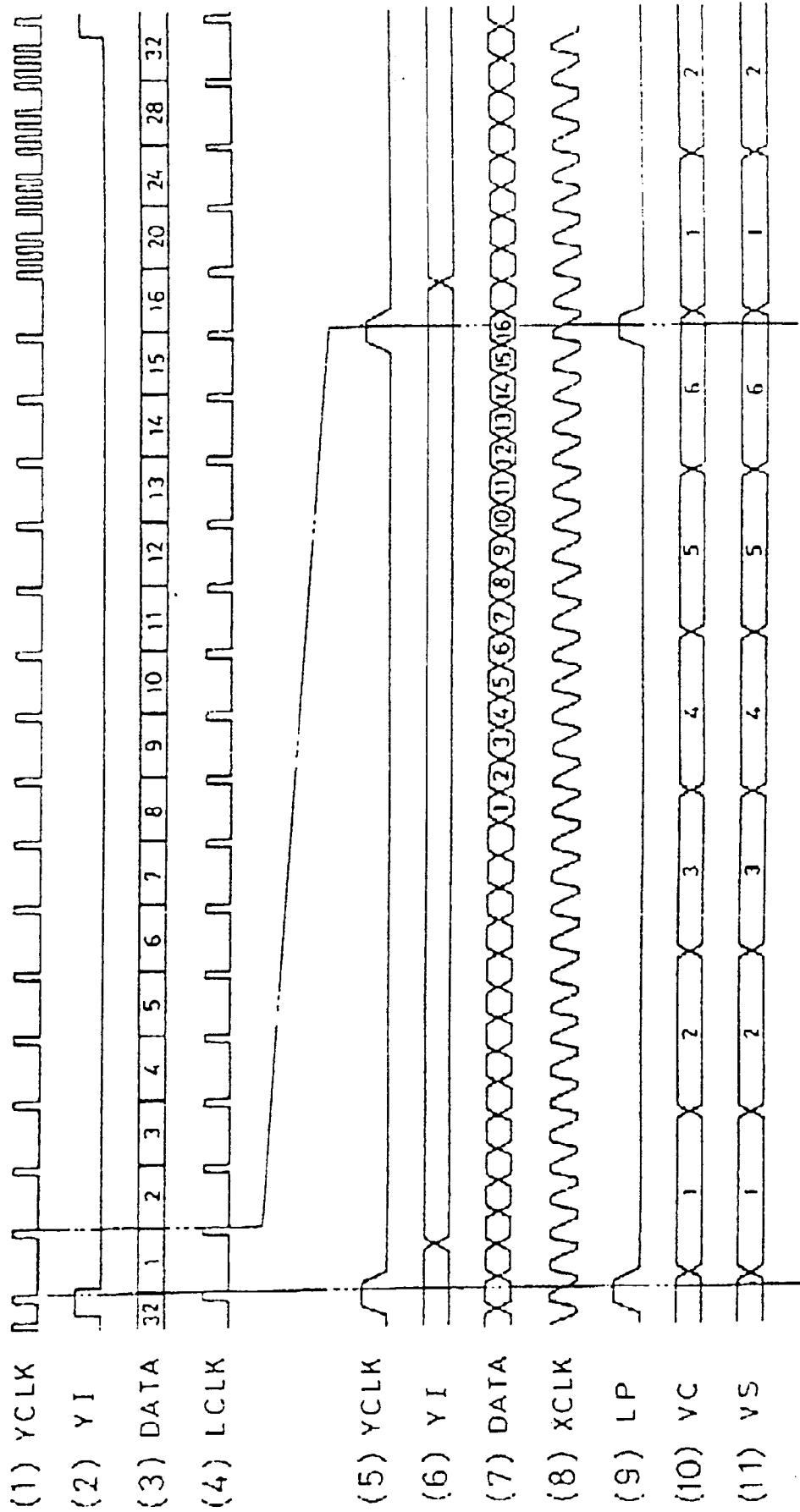


Fig. 15

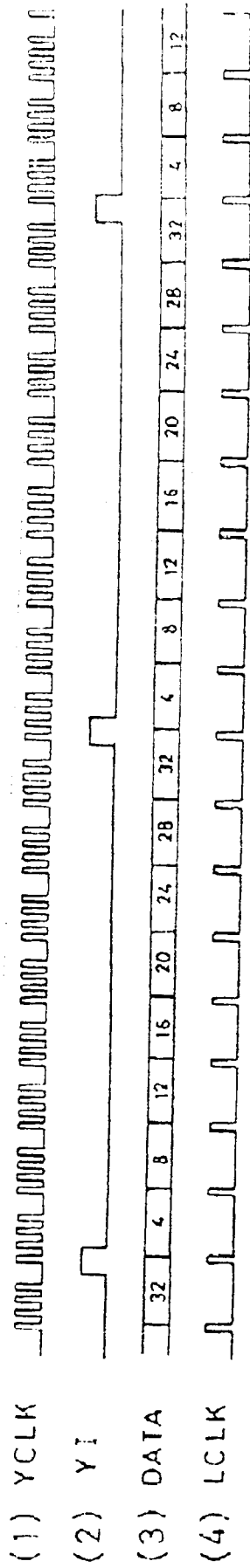


Fig. 16

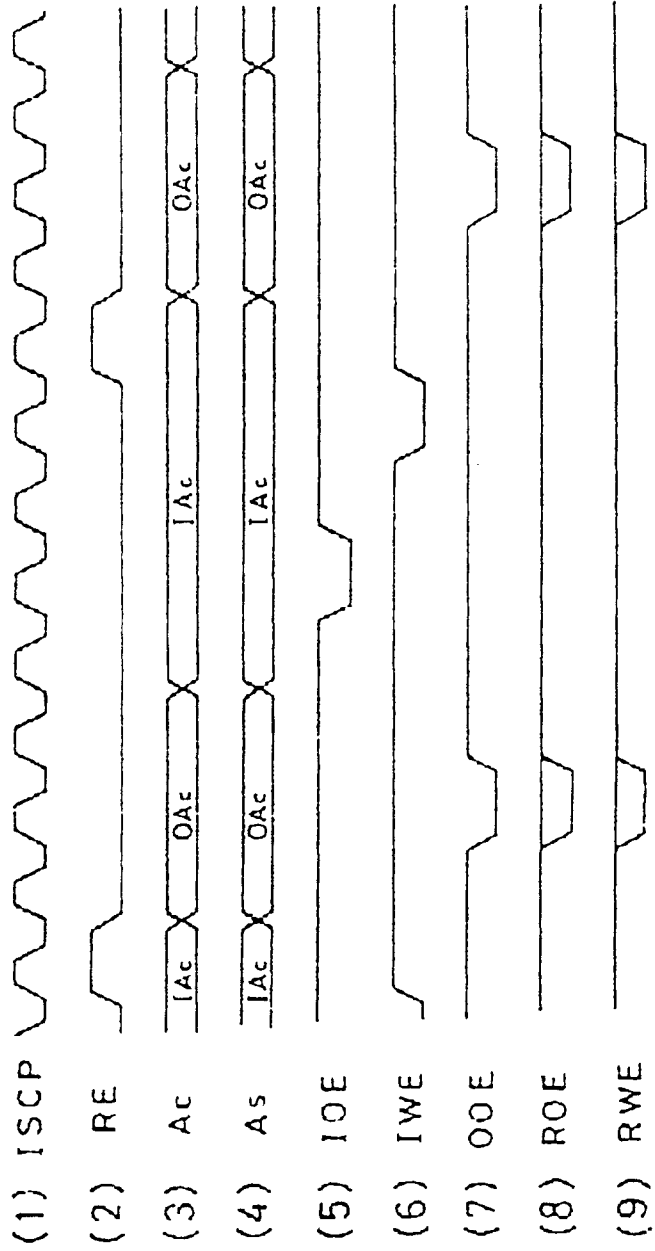


Fig. 17

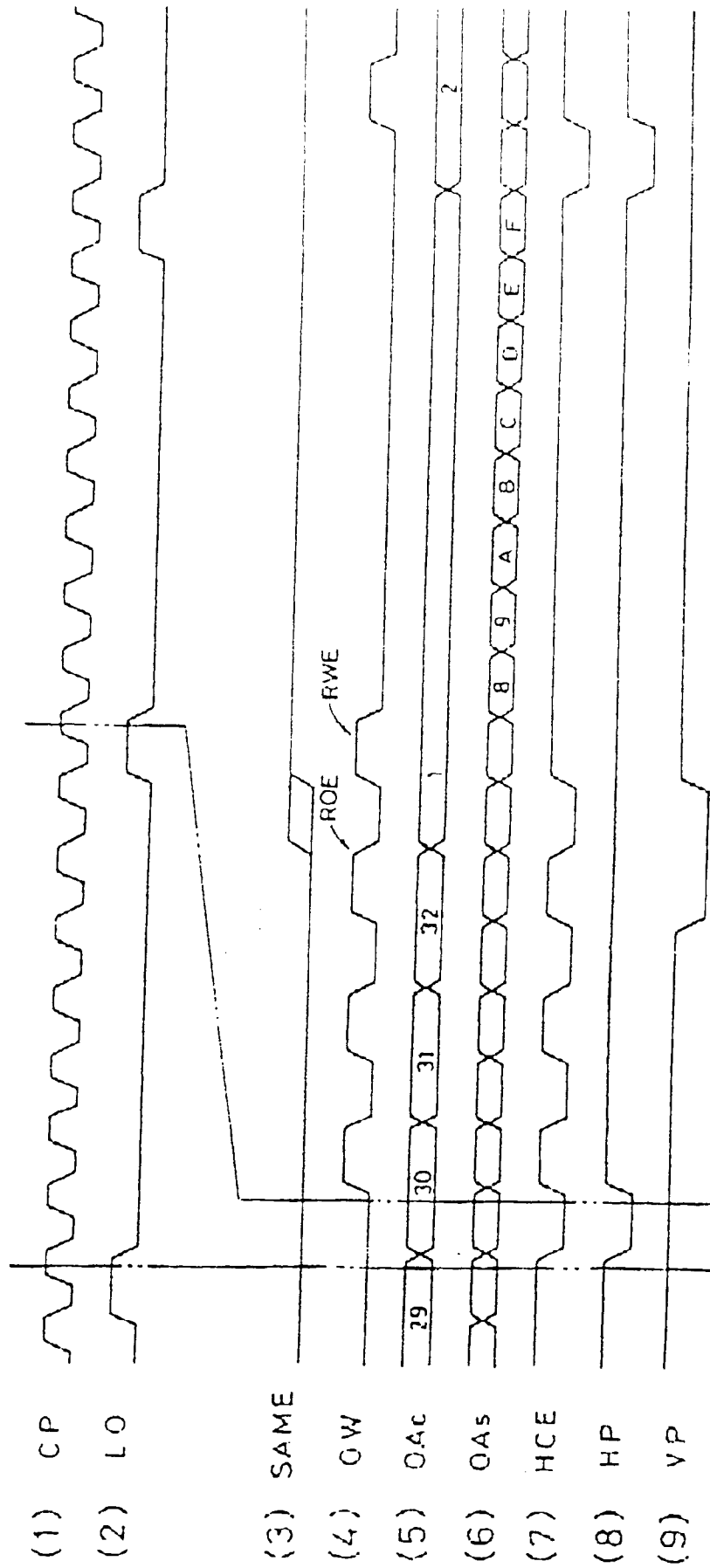


Fig. 18

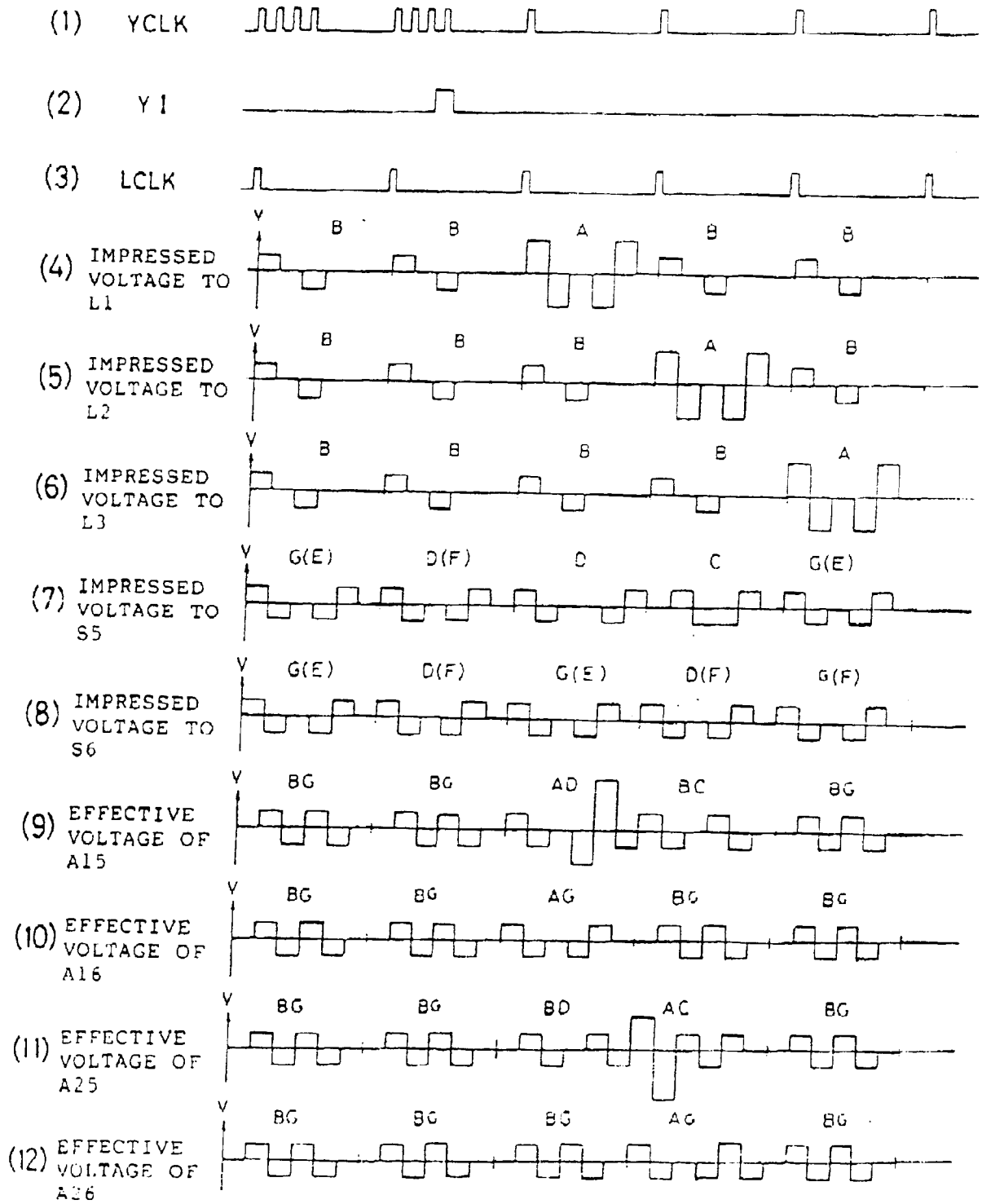


Fig. 19

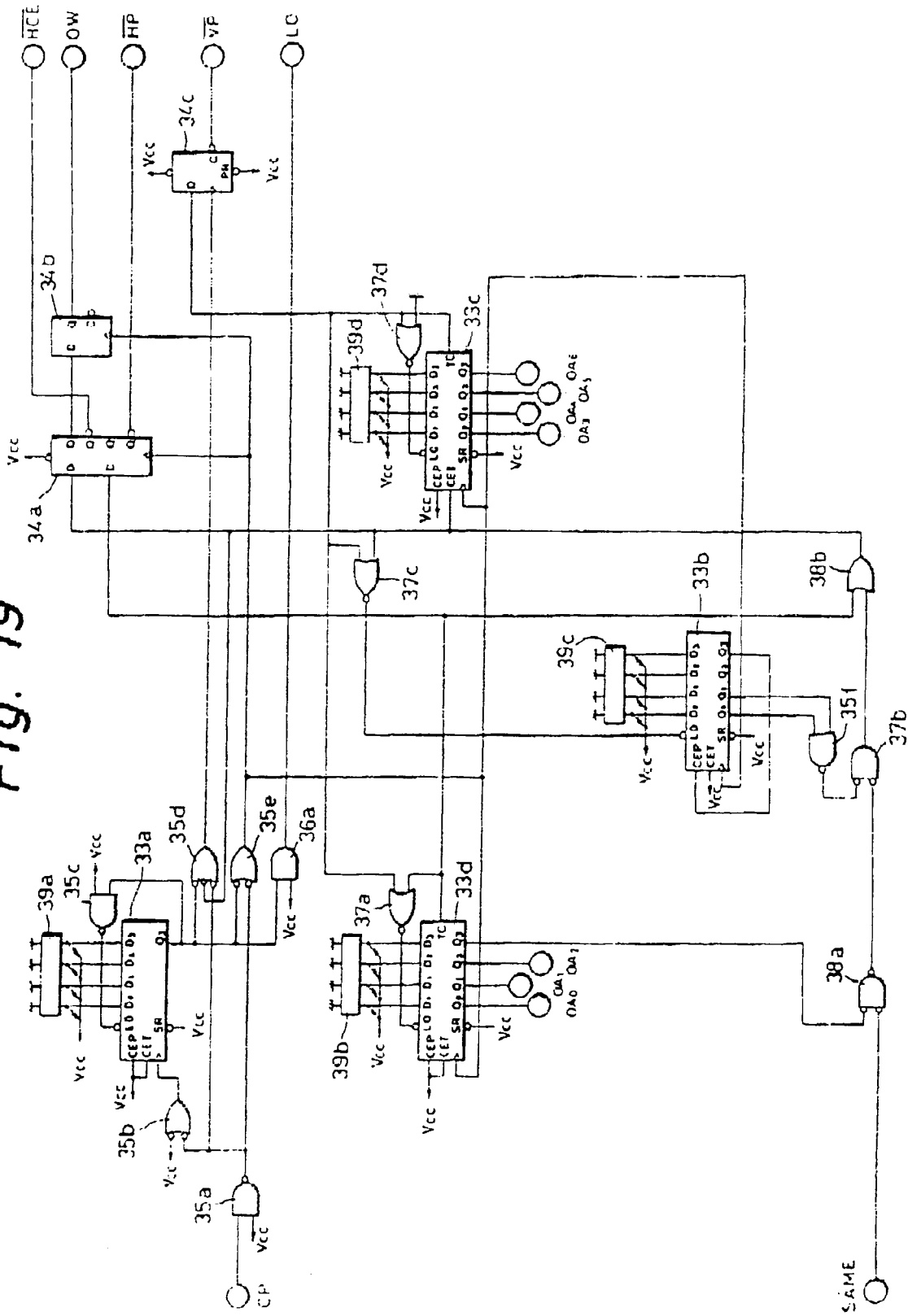


Fig. 20

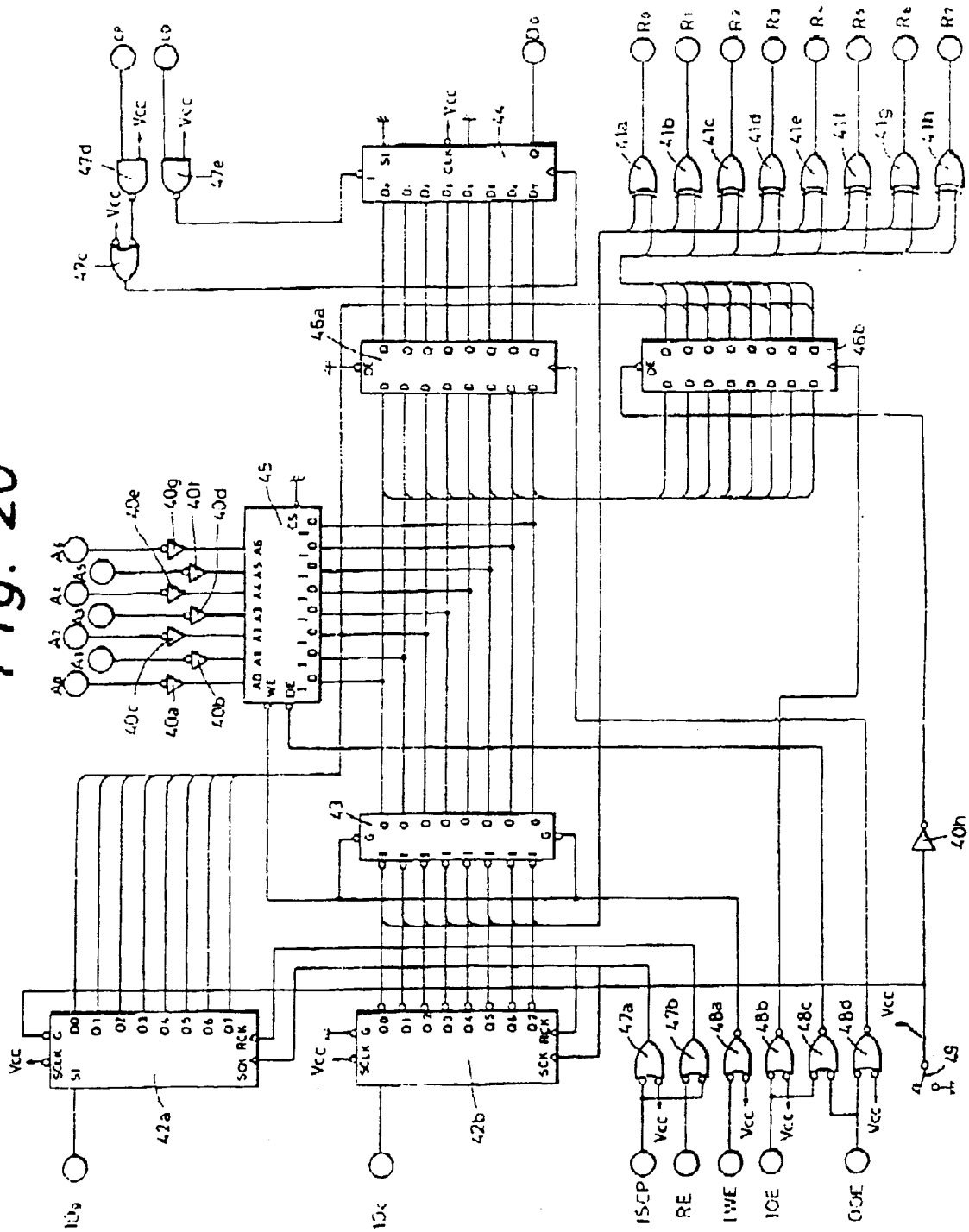


Fig. 21

