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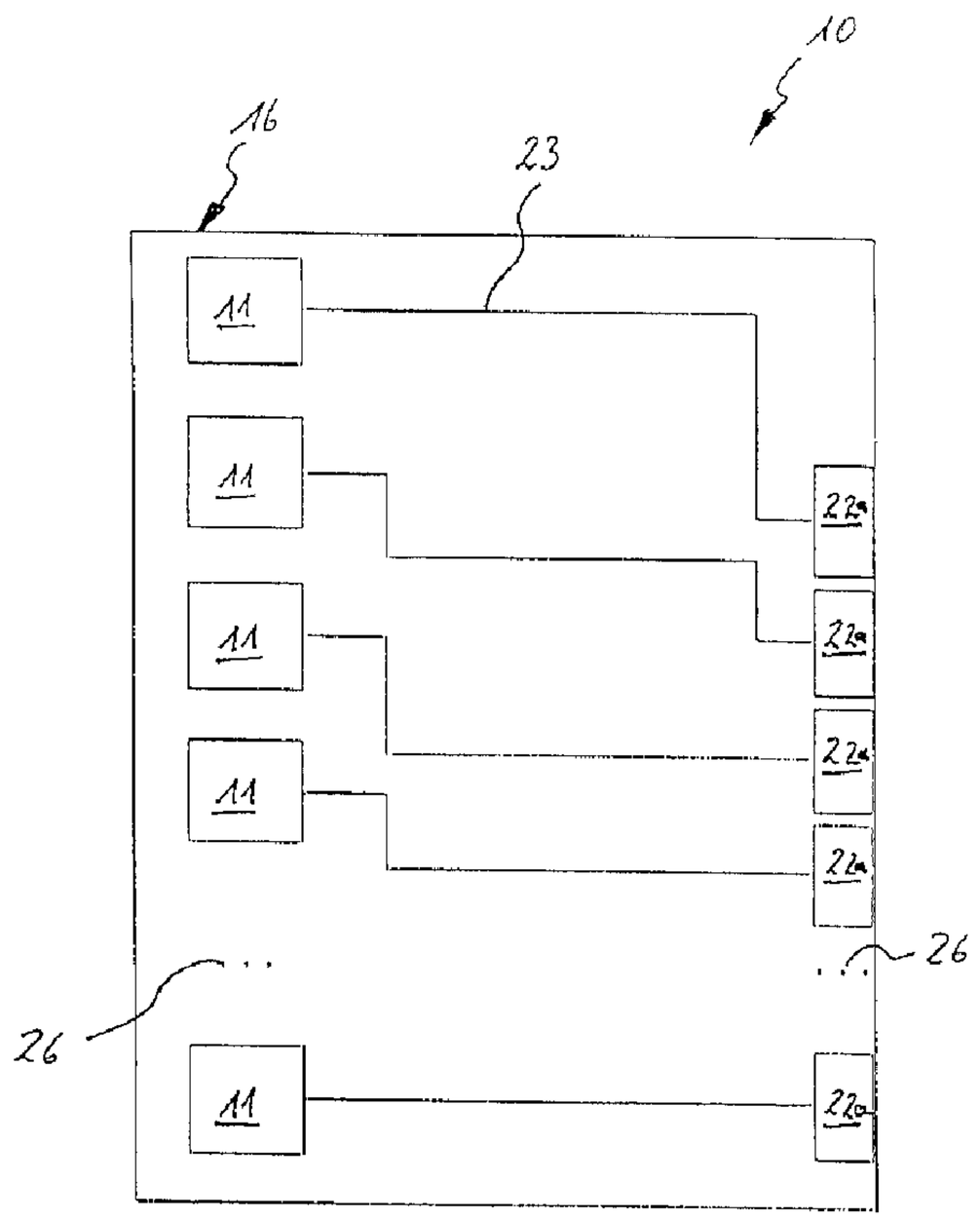
(54) Titre : SYSTEME INFORMATIQUE POUR RESEAU INFORMATIQUE INTERNE
(54) Title: A COMPUTER SYSTEM FOR AN INTERNAL COMPUTER NETWORK



(57) Abrégé/Abstract:
An internal computer network comprising a plurality of electronic computer subsystems for forming a multiprocessor system or mainframe computer, wherein a plurality of plug-in places for central processing units (CPUs 11) are disposed on a circuit board. The CPUs (11) are connected through internal busses (23) to backplanes (22a, 22b, 22c, 22d, 22e). The backplanes (22a, 22b, 22c, 22d, 22e) in turn connect slave cards (17, 18, 19) to a master card.

Abstract of the Disclosure

A computer system for an internal computer network

An internal computer network comprising a plurality of electronic computer subsystems for forming a multiprocessor system or mainframe computer, wherein a plurality of plug-in places for central processing units (CPUs 11) are disposed on a circuit board. The CPUs (11) are connected through internal busses (23) to backplanes (22a, 22b, 22c, 22d, 22e). The backplanes (22a, 22b, 22c, 22d, 22e) in turn connect slave cards (17, 18, 19) to a master card.

A computer system for an internal computer network

The invention relates to an internal computer network comprising a plurality of electronic computer subsystems for forming a multiprocessor or mainframe computer.

Usually a plurality of central processing units (CPUs) in a multiprocessor system communicate through network adapters and that places a burden on the network due to the data load to be dealt with so that the speed is slowed down. Merely raising the clock frequency of the processors from 400 to 500 MHz, for instance, means that the computer speed will be increased by only 25 %, and of that value a maximum of 5 % is all that is left for the overall system.

It is the object of the instant invention to provide a computer system capable of adapting its operating performance to users' growing demands, increasing the computing power while, at the same time, maintaining the data processing speed at a constant high level.

This object is met by the measures recited in claim 1, especially by an internal computer network consisting of a plurality of electronic computer subsystems for forming a multiprocessor system or mainframe computer, wherein a plurality of plug-in places for central processing units (CPUs) are disposed on a circuit board, the CPUs are connected through internal busses to backplanes which in turn are connected to slave cards on each of which a plurality of plug-in places are provided for DSP units and/or PLD units and/or network adapter units.

The computer system may be terminated by a processor bridge slave card (PB slave card) comprising a plurality of plug-in places at processor bridge units (PB units). This permits the computer subsystems to be connected directly without loading the local area network (LAN).

The measures described make it possible to interconnect any desired number of CPUs, thereby avoiding that data get jammed in a LAN and, at the same time, accelerating the operating performance of the network.

Any desired number of CPUs communicate with each other across processor bridges rather than in the conventional way through network adapters. Each CPU has its own plug-in processor bridge by way of which it can communicate with another CPU of another computer subsystem. Inside a computer, any desired number of computer subsystems may be interconnected by such processor bridges.

An internal network is established in the form of a multi-processor system. The processor bridge adapters which interconnect the various CPUs may be connected in a ring bus, for example. Any desired number of the various processors and coprocessors of the computer subsystems are located on their own respective circuit boards, and these are interconnected through backplanes. Thus it becomes possible to execute different application programs in parallel and manage them by any desired number of CPUs on a circuit board (master card) without having the computing performance slowed down or the network overloaded by the data traffic to be handled.

Different coprocessors may be associated with one central processing unit and addressed flexibly. This arrangement likewise permits interprocessor communication. One master card may allow a number of processing units of from CPU 1 to CPU n to be provided. The operating systems used in such a multiprocessor system, for instance, may be Linux or comparable Unix derivatives.

Further advantageous measures are defined in the subclaims. The invention is illustrated in the accompanying drawing and will be described in greater detail below.

Fig. 1 is a schematic block diagram of a circuit board (master card) including any desired number of central processing units (CPUs) connected to backplanes;

Fig. 2 is a schematic block diagram of a circuit board (slave card) including any desired number of DSP units connected to backplanes;

Fig. 3 is a schematic block diagram of a circuit board (slave card) including any desired number of PLD units connected to backplanes;

Fig. 4 is a schematic block diagram of a circuit board (slave card) including any desired number of network adapter (NA) units connected to backplanes;

Fig. 5 is a schematic block diagram of a circuit board (slave card) including any desired number of processor bridge (PB) units connected to backplanes;

Fig. 6 is an isometric illustration of the individual computer subsystems which are interconnected by PB units and inserted in a conventional 19-inch casing;

Fig. 7 is a schematic block diagram of the connections existing between the individual components when inserted in the casing.

Fig. 1 illustrates a central processing unit master card 16 (CPU master card) implemented by 19-inch technology. On it, there are a plurality of plug-in places 26 for CPUs 11 which are arranged on the CPU master card 16.

The CPUs 11 are connected by internal busses 23 to backplanes 22a. The backplanes 22a serve for transmission of data and exchange of information between the individual components of the computer subsystems 10.

The digital signal processor slave card 17 (DSP slave card) shown in fig. 2 comprises a plurality of plug-in places 26 for DSP units 12. The processors again are connected by internal busses 23 to the backplanes 22c.

Fig. 3 shows the circuit board of a programmable logic device slave card 18 (PLD slave card). A plurality of PLD units 13 are plugged into plug-in places 26 provided on the PLD slave card 18. The number of plug-in places 26 is limited only by the

configuration of the circuit board. Again the PLD units 13 are connected by internal busses 23 to backplanes 22c.

Fig. 4 shows a circuit board of a network adapter slave card 19 (NA slave card). This NA slave card 19 is formed with a plurality of plug-in places 26 to receive network adapter units 14 (NA units). Internal busses 23 connect the NA units 14 to their backplanes 22d, thus establishing a connection with the entire computer subsystem 10.

Fig. 5 shows a processor bridge slave card 20 (PB slave card) provided with a plurality of plug-in places 26 for processor bridge units 15 (PB units). The PB units 15 are connected by internal busses 23 to their backplanes 22e. Processor bridge connections 25 establish connections among the PB units 15.

PCI or SCI busses are especially well suited for use as processor bridge connections 25. Bus mastering is supported in particular by the SCI bus. Adapters may function either as master module or as slave module. Master-type adapters can relieve processors quite considerably, especially when multitasking operating systems are employed. The processor bridge connections 25 may be embodied by a ring bus.

Fig. 6 shows an overall system housed in a commercially available 19-inch casing 21. The back 24 of the 19-inch casing 21 is provided with plug-in places (not shown) where CPU master cards 16, DSP slave cards 17, PLD slave cards 18, NA slave cards 19, and PB slave cards 20 may be plugged in.

In this manner a multiprocessor system or mainframe computer is provided which may be composed of a plurality of computer subsystems 10. The computer subsystems 10, in horizontal division, are connected through their respective internal busses 23 to their backplanes 22a, 22b, 22c, 22d, and 22e, respectively.

The PB slave cards 20 permit communication with the vertically arranged CPUs 11 via a plurality of plug-in places 26. In this manner each horizontal computer subsystem 10 is incorporated in an internal high-speed network.

Fig. 7 is a diagrammatic presentation of the connections formed between the individual components when the CPU master card 16, the DSP slave card 17, the PLD slave card 18, the NA slave card 19, and the PB slave card 20 are plugged into the casing 21. The internal busses 23 and the respective backplanes 22a, 22b, 22c, 22d, 22e define corresponding horizontal computer systems I, II, ...

The horizontal computer systems I, II, ... exchange data via the PB units 15 on the PB slave card 20. Furthermore, the computer systems I, II, ... may exchange data with the LAN through the respective NA adapter units 14, as is known per se.

With the arrangement described above, the plurality of CPUs 11 each disposing of their own memory and using their own operating system, whereby they differ from symmetric multiprocessor machines (SMP machines), are connected by means of NA adapter units 14 to the local area network of a multiprocessor or mainframe computer system. The plurality of CPUs 11 form part of this network. At the same time, an internal network is formed with the arrangement described, specifically with the internal busses 23, the plug-in places 26 on the respective backplanes 22a, 22b, 22c, 22d, 22e and the PB units 15 on the PB slave card 20, and data can be exchanged through this internal network between the various horizontal computer systems I, II, ..., specifically the CPUs 11.

This offers the opportunity of supplementing or upgrading multiprocessor systems or mainframe computers by means of a plurality of additional computer subsystems 10. These additional computer subsystems handle a substantial portion of the data traffic through the internal network which is established particularly with the help of the internal busses 23 and the PB units 15.

Adding computer subsystems 10 to the multiprocessor system or mainframe computer, therefore, does not cause overloading of the

multiprocessor or mainframe computer LAN which usually exists in parallel and to which the plurality of CPUs 11 are coupled through the NA units 14. Thus one or more internal networks may be formed within the multiprocessor or mainframe computer, and the computer subsystems 10 will use the connections of the parallel LAN of the multiprocessor or mainframe computer only as may be required, for example, for data traffic between two internal networks each designed as specified above, for configuration purposes, or for a booting operation.

Just like the plurality of CPUs 11, also the DSP units 12 and the PLD units 13 may be coupled to the internal network by means of DSP slave cards 17 and PLD slave cards 18, respectively (cf. fig. 7). The arrangement illustrated in fig. 7 may be used for electronic data exchange between the plurality of CPUs 11 disposed on an individual CPU master card 16 and the DSP units 12 and the PLD units 13, the data passing through the internal busses 23, the backplane 22, and the PB units 15. The PLD units 13 and/or the DSP units 12 may be accociated with the plurality of CPUs 11 in dependence on the task to be performed.

The features of the invention disclosed in the instant specification, in the drawing and claims may be essential to the implementation of the invention in its various embodiments, both individually and in any combination.

WHAT IS CLAIMED IS:

1. An internal computer network comprising a plurality of electronic computer subsystems for forming a multiprocessor or mainframe computer, wherein a plurality of plug-in places for central processing units (CPUs 11) are disposed on a circuit board, the CPUs (11) are connected through internal busses (23) to backplanes (22a, 22b, 22c, 22d, 22e) which in turn are connected to slave cards (17, 18, 19) on each of which a plurality of plug-in places (26) are provided for DSP units (12) and/or PLD units (13) and/or network adapter units (14).

2. The computer network as claimed in claim 1, characterized by PB units (15) terminated by a PB slave card (20) each.

3. The computer network as claimed in claim 1 or 2, characterized in that a plurality of plug-in places (26) are provided for PB units (15) permitting computer subsystems (10) to be connected.

4. The computer network as claimed in any one of claims 1 to 3, characterized in that a CPU (11), a DSP unit (12), a PLD unit (13), and a network adapter unit (14) together form a computer subsystem (10) which is connected through a PB unit (15) to other computer subsystems.

5. The computer network as claimed in any one or more of claims 1 to 4, characterized in that coprocessors are connected to the CPUs (11) through internal busses (23).

6. The computer network as claimed in any one or more of claims 1 to 5, characterized in that the PLD units (13) are connected to the CPUs (11) through internal busses (23).

7. The computer network as claimed in any one or more of claims 1 to 6, characterized in that each CPU (11) has its own operating system.

8. The computer network as claimed in any one or more of claims 1 to 7, characterized in that computer subsystems (10) are provided which operate in parallel.

9. The computer network as claimed in any one or more of claims 1 to 8, characterized in that CPUs (11) are provided which communicate through the PB units (15), each CPU (11) having its own associated PB unit (15).

10. The computer network as claimed in any one or more of claims 1 to 9, characterized in that a plurality of user applications are executed on a single CPU master card (16).

11. The computer network as claimed in any one or more of claims 1 to 10, characterized in that different application programs are distributed among several of the CPUs (11) and are executed by a plurality of computer subsystems (10).

12. The computer network as claimed in any one or more of claims 1 to 11, characterized in that CPU master cards (16) and/or slave cards (17, 18, 19, 20) are provided which are made in 19 inch technology.

13. The computer network as claimed in any one or more of claims 1 to 12, characterized in that the computer

subsystems (10) are arranged in a PC casing (21) separated from one another in space.

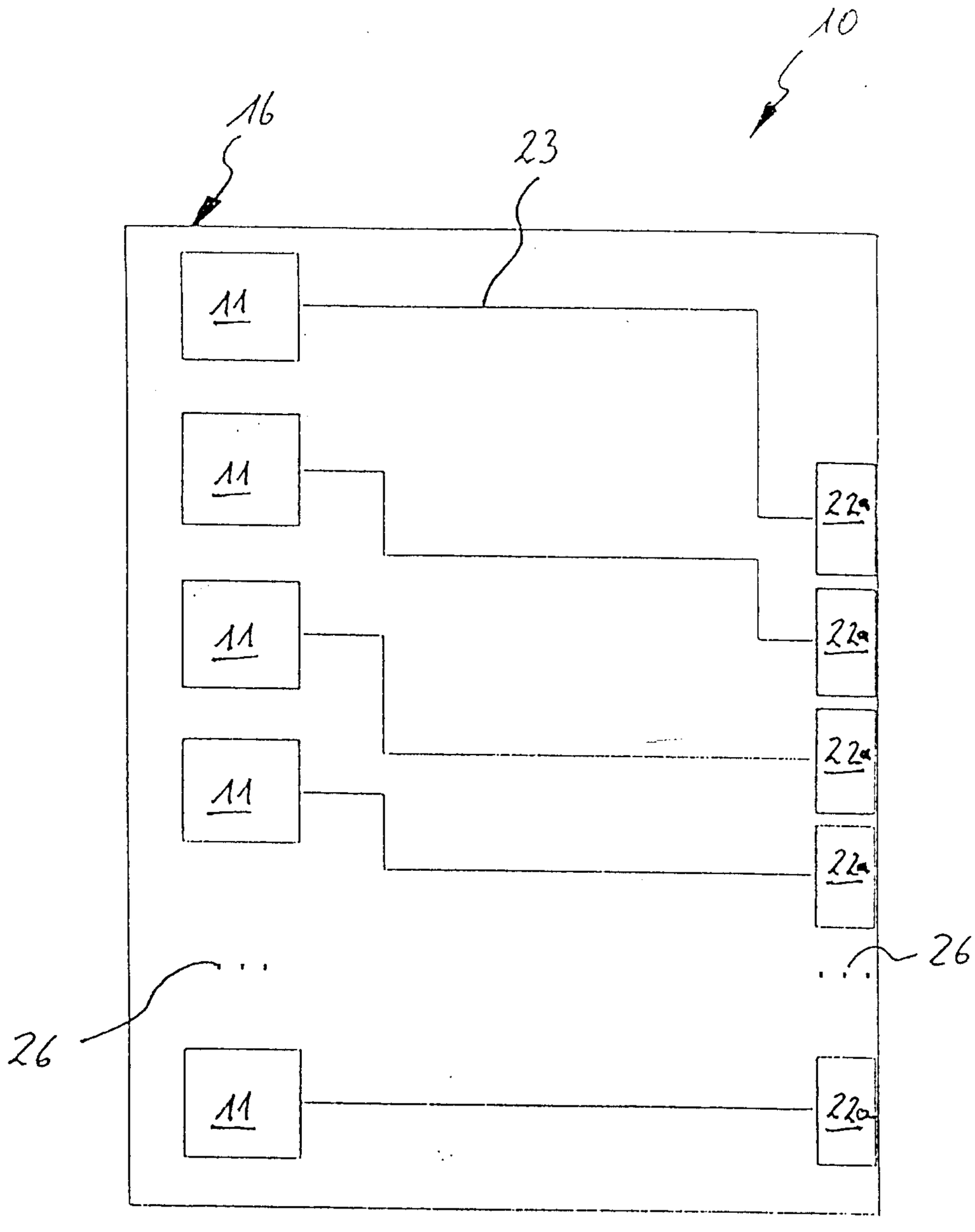


Fig. 1

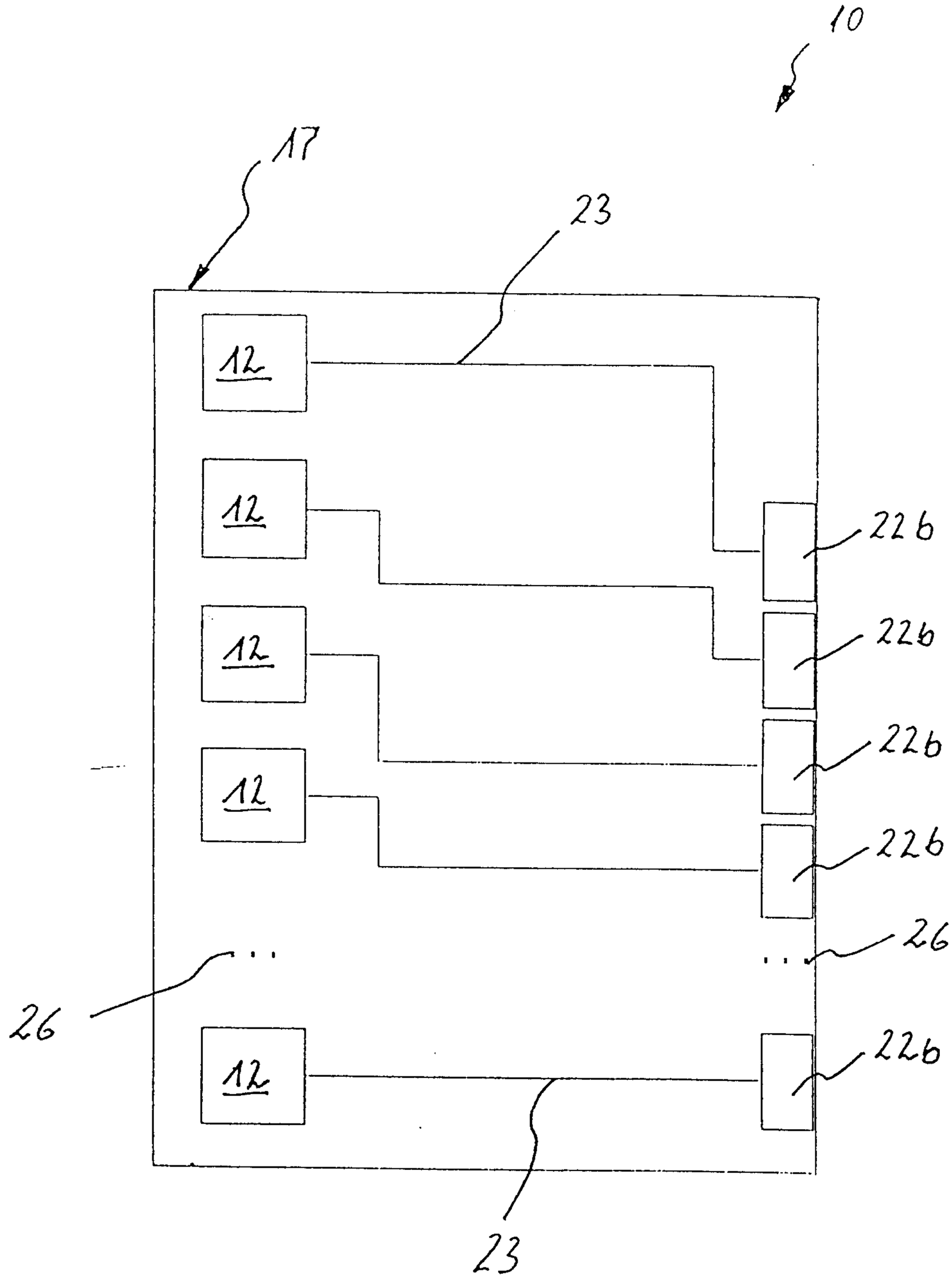


Fig. 2

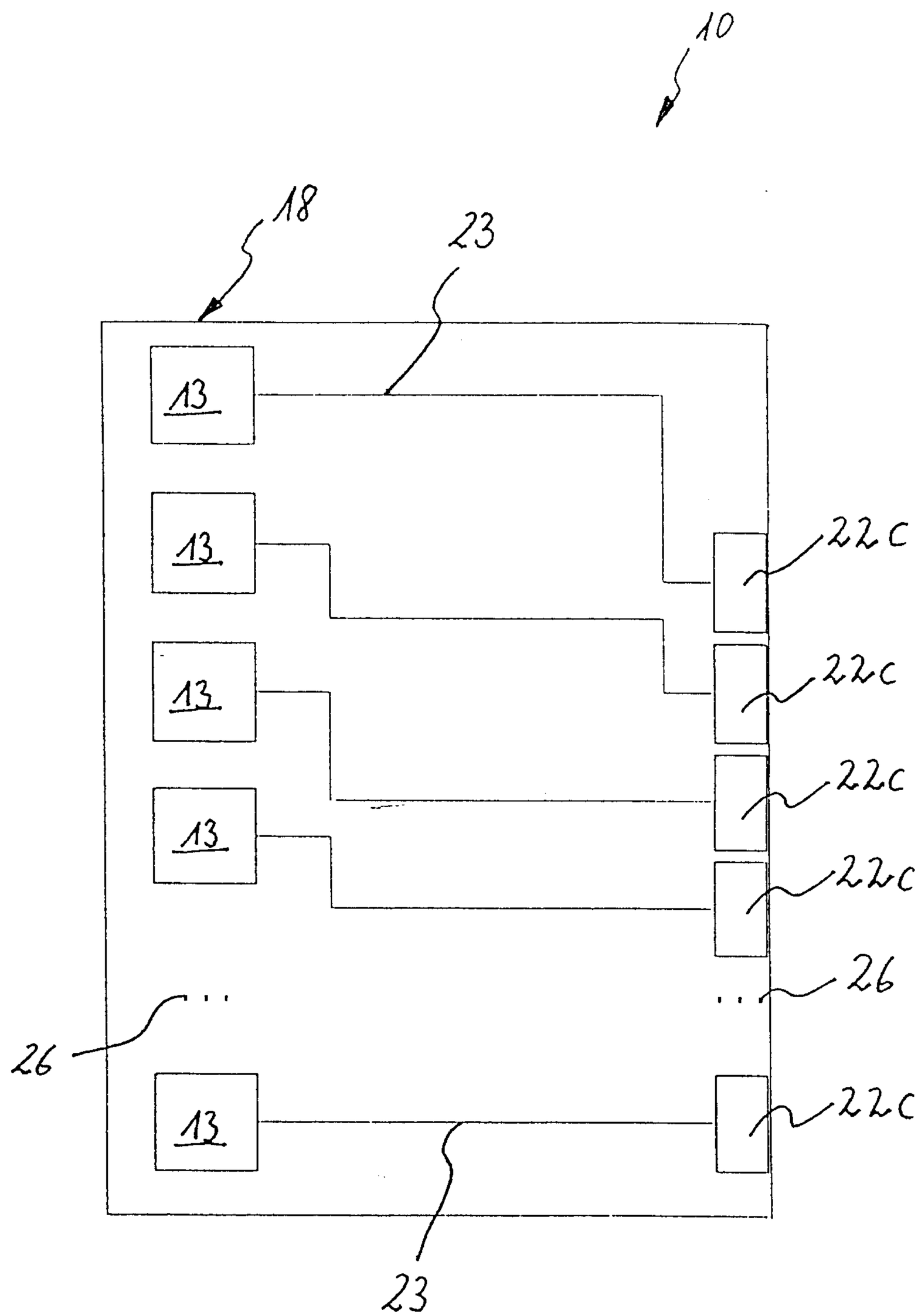


Fig. 3

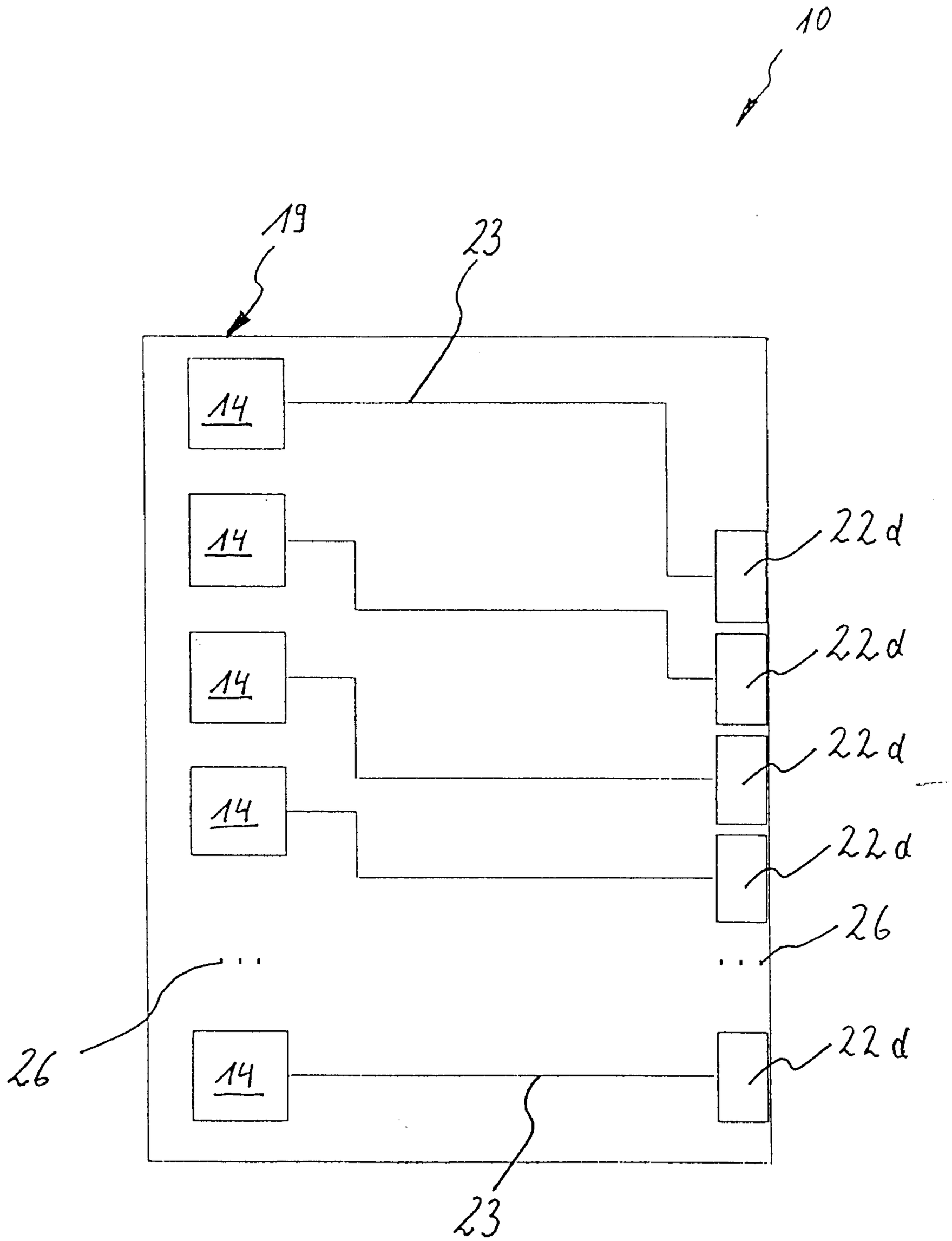


Fig. 4

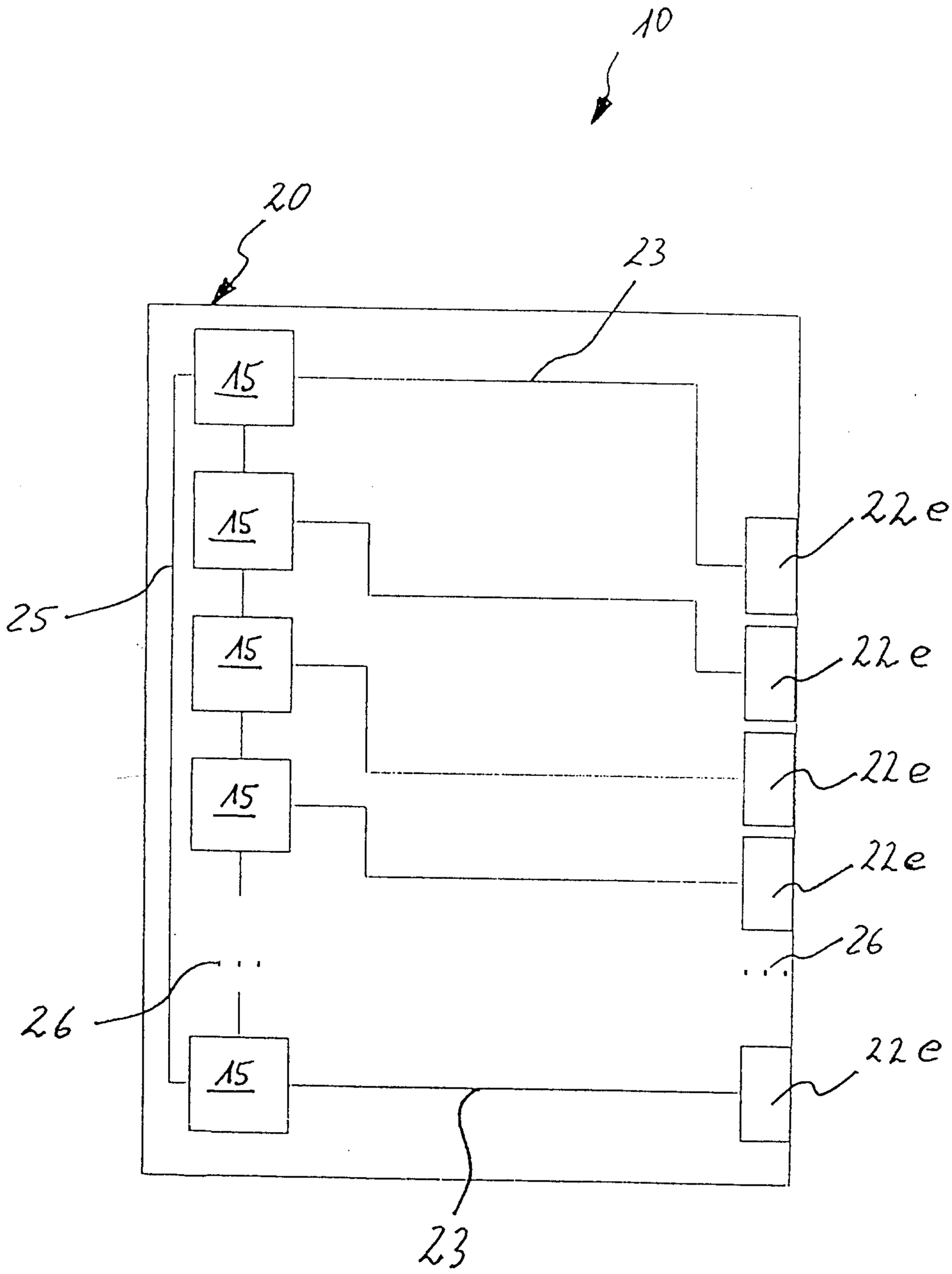


Fig. 5

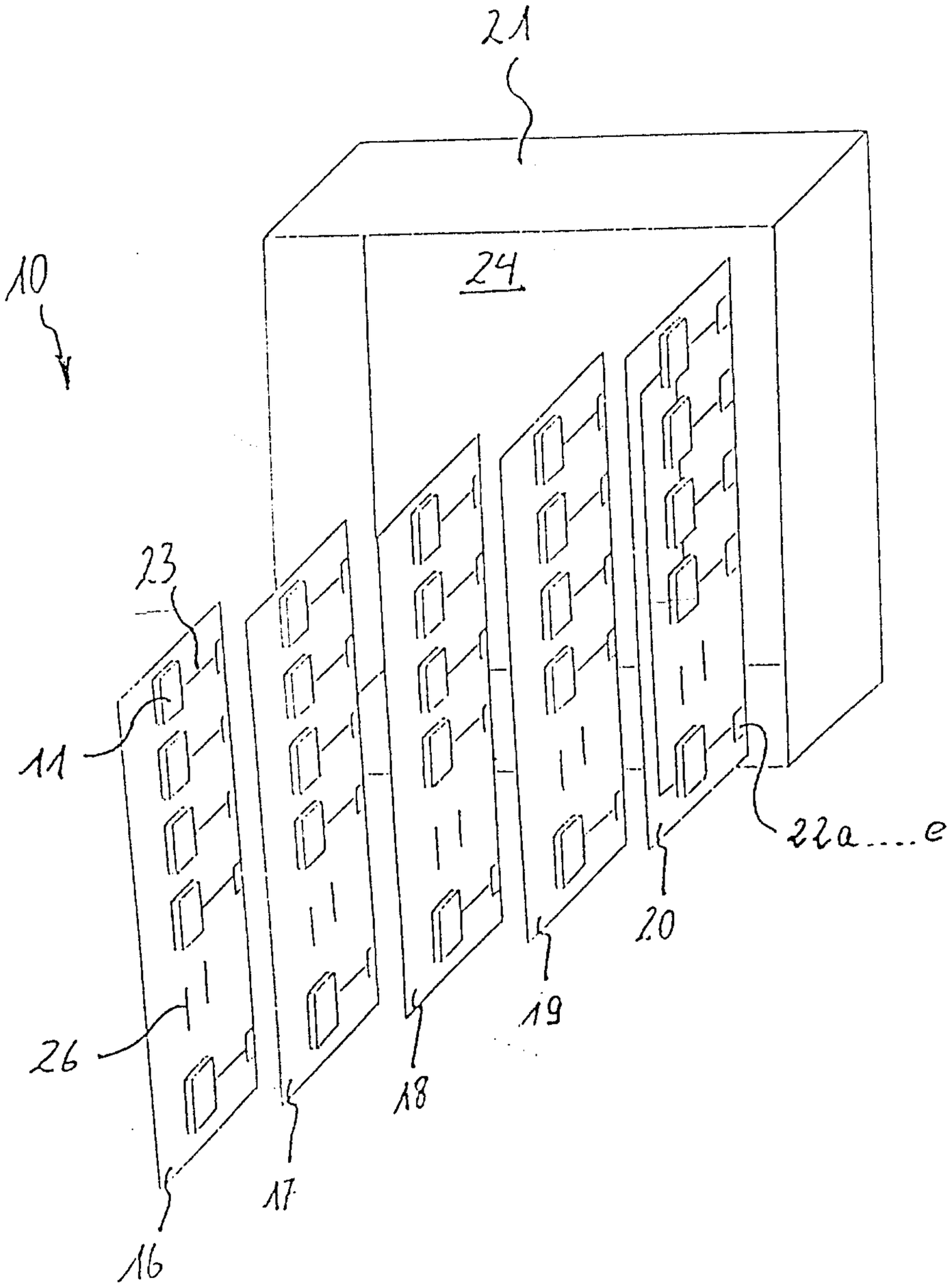


Fig. 6

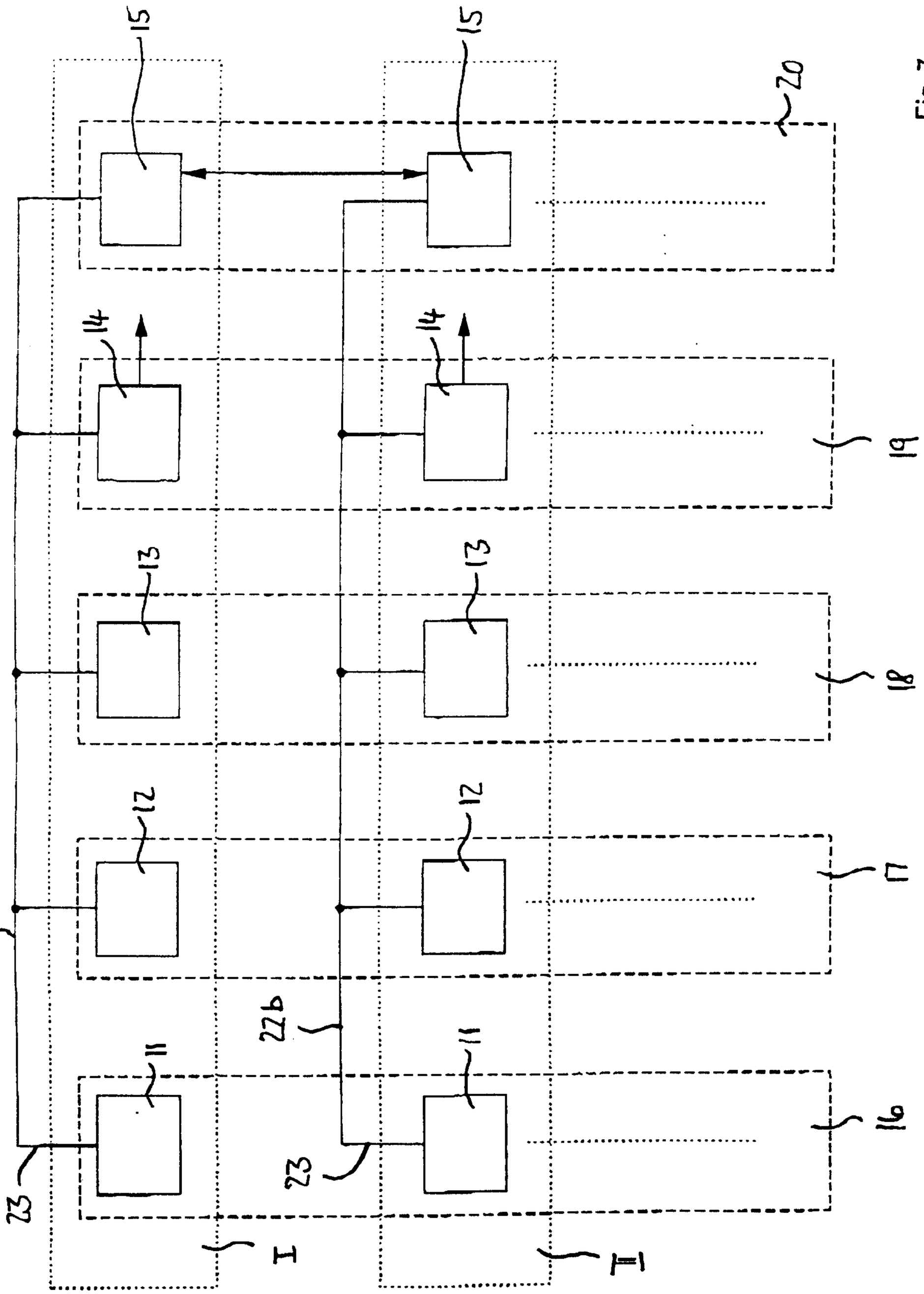
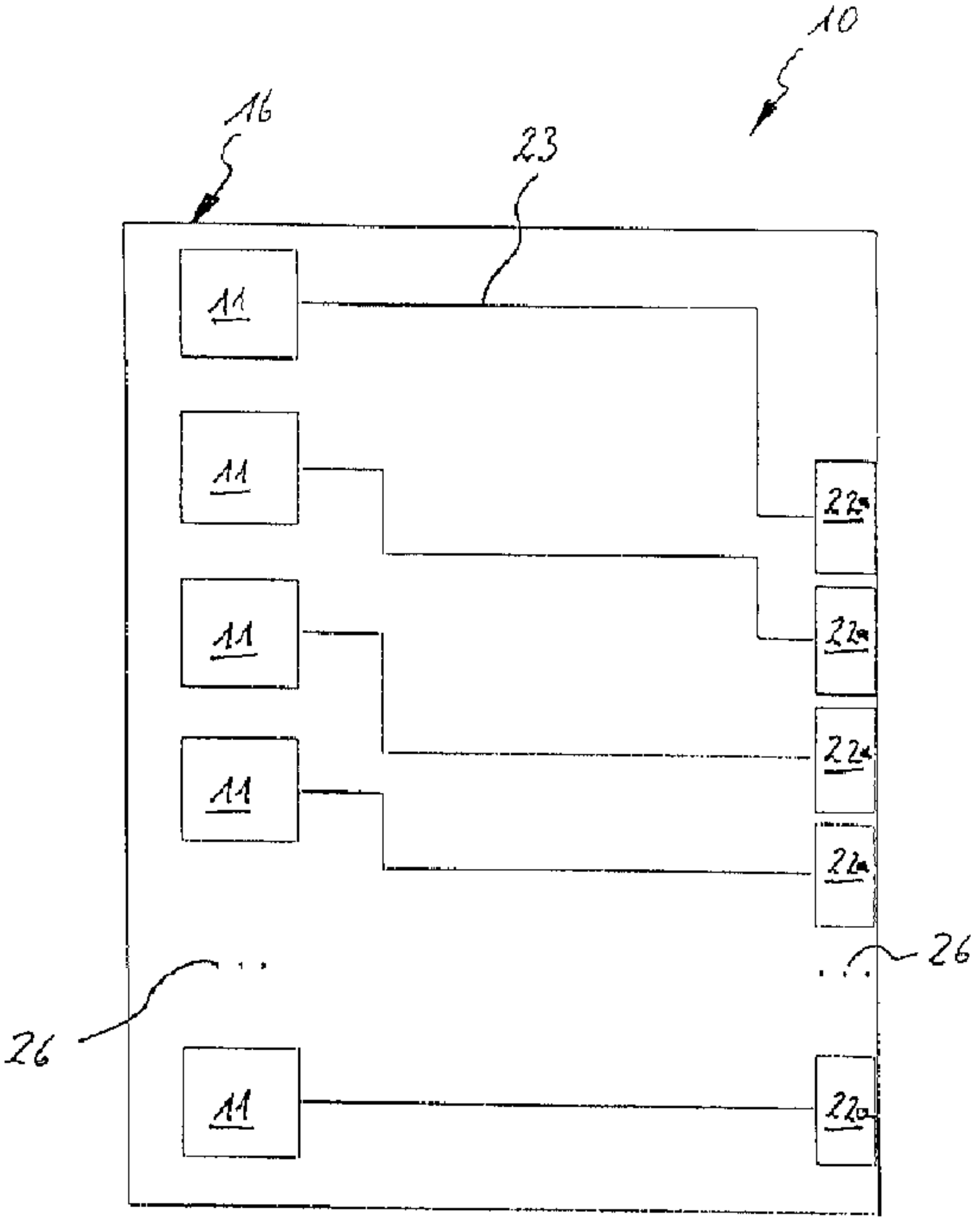


Fig. 7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