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(54) Title: SPREAD SPECTRUM COMMUNICATION NETWORK SIGNAL PROCESSOR

(57) Abstract

A base station communicates with a plurality of mobile stations over a cellular network. In one embodiment, the base station includes a receiver configured to receive inbound information from the mobile station and a transmitter configured to transmit outbound information to the mobile station. The base station further has a central processor that includes a signal processor array. The signal processor architecture is designed to increase the throughput and task-based allocation of processing resources. The signal processing array has both series and parallel signal processing elements. A plurality of signal processor elements are disposed in series to form a signal processing string. A plurality of signal processing strings are disposed in parallel. Each of the signal processor strings includes at least two signal processor elements that are each dedicated to performing a specific task. As a result, the parallel processor strings simultaneously process information corresponding to predetermined criteria, such as TDMA time slots, while the series processors sequentially process that information by an efficient task-based pipeline processing. A preferred protocol is Global Systems for Mobile Communication (GSM).

SPREAD SPECTRUM COMMUNICATION NETWORK SIGNAL PROCESSOR

RELATED APPLICATIONS

The present application incorporates the following patent applications by reference:

CELLULAR PRIVATE BRANCH EXCHANGES, U.S. Ser. No. 08/435,709, filed on May 4, 1995, Attorney docket No. WAVEP001;

METHODS AND APPARATUSSES FOR AN INTELLIGENT SWITCH, U.S. Ser. No. 08/435,838, filed on May 4, 1995, Attorney docket No. WAVEP004;

SPREAD SPECTRUM COMMUNICATION NETWORK WITH ADAPTIVE FREQUENCY AGILITY, U.S. Ser. No. 08/434,597, filed on May 4, 1995, Attorney docket No. A-60820; and

CELLULAR BASE STATION WITH INTELLIGENT CALL ROUTING, U.S. Ser. No. 08/434,598, filed on May 4, 1995, Attorney docket No. A-61115.

FIELD

The present invention relates to a spread spectrum communication network signal processor. In particular, the present invention is used in a cellular communication network to improve the information channel capacity with a distributed signal processing architecture.

BACKGROUND

Spread spectrum communication typically includes two type of techniques: direct sequence spread spectrum (DSSS), where the information signal in-phase and quadrature-phase are varied; and frequency hopping spread spectrum (FHSS), where the information carrier frequency is varied. Moreover, these techniques can include formats for what is known as time division multiple access (TDMA) and frequency division multiple access (FDMA). These formats dedicate a specific periodic time slot or frequency to each mobile station. Advantages of DSSS, FHSS, TDMA and FDMA include reduced co-channel interference and improved information channel capacity over a given bandwidth. While these techniques can be employed independently, they can also be combined.

One limitation of existing communication networks is that the base station must have a multiplicity of dedicated transmitters and receivers to adequately process all the mobile station signals. Since each base station transmitter and receiver can communicate only one frequency, a large number of transmitters and receivers are required to serve the communication network employing multiple frequencies. For example, eight transmitters and eight receivers are required to serve eight receive frequencies and eight transmit frequencies.

Moreover, since existing communication networks use a multiplicity of dedicated transmitters and receivers, a fault can cause data to be lost, or even cause the network to malfunction. When a transmitter or receiver is broken, the network must operate in a reduced capacity, if it can operate at all.

Another limitation of existing communication networks is that the FHSS protocol sequence is predetermined. That is, the frequency hops are periodic within the same frequency set. This results in continual interference from other operating electro-magnetic fields. The existing communication protocols do not adapt to avoid interference.

Another limitation of existing communication networks is that the processing is performed within a central signal processor. A central signal processor employs software to perform the procedures necessary to process the data. While this configuration provides high flexibility, it is also slow and requires high computational and memory overhead.

Another limitation of existing communication networks is that in the communication protocol, the specific periodic TDMA time slot is fixed. Each mobile station is entitled to a single slot and may not receive an additional slot even if other mobile stations are not fully utilizing their respective information channel capacity.

SUMMARY

The present invention relates to a spread spectrum communication network signal processor. In particular, the present invention is used in a cellular communication network to improve the information channel capacity with a distributed signal processing architecture. Exemplary embodiments are provided for use with the Global Systems for Mobile Communication (GSM) protocol.

A base station communicates with a plurality of mobile stations over a cellular network. In one embodiment, the base station includes a receiver configured to receive inbound information from the mobile station and a transmitter configured to transmit outbound information to the mobile station.

The base station further has a central processor that includes a signal processor array. The signal processor architecture is designed to increase the throughput and task-based allocation of processing resources. The signal processing array has both series and parallel signal processing elements. A plurality of signal processor elements are disposed in series to form a signal processing string. A plurality of signal processing strings are disposed in parallel. Each of the signal processor strings includes at least two signal processor elements that are each dedicated to performing a specific task. As a result, the parallel processor strings simultaneously process information corresponding to predetermined criteria, such as TDMA time slots, while the series processors sequentially process that information by an efficient task-based pipeline processing.

Once the inbound information is processed by the signal processor array, the inbound information is sent to the central processor. The central processor is responsible for communicating information with a public switched telephone network.

The base station further receives outbound information from the public switched telephone network and sends the outbound information to the signal processor array to encode the information and send it to a transmitter to be delivered to the mobile station. The outbound signal processing is similar to the inbound signal processing, only in reverse.

In another embodiment, the base station further includes a plurality of receivers and transmitters (transceivers) where each transceiver has a dedicated signal processor array. This architecture promotes front end distributed processing and relieves the processing load on the central processor.

The advantages of the present invention include reduced interference, improved communication bandwidth, fault tolerance, modularity, scalability, and more efficient and cost-effective base stations and mobile stations.

BRIEF DESCRIPTION OF THE DRAWINGS

Additional advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings, in which:

Figure 1 depicts a cellular network showing several base stations and several mobile stations;

Figures 2A-C illustrate the frequency bands allocated to GSM communication, a typical frequency hopping table, and the GSM frequency hopping algorithm;

Figure 3 illustrates a speech waveform sampled and assembled into a digital GSM format;

Figure 4 illustrates a GSM frame and associated data;

Figure 5 depicts one embodiment of a base station architecture according to the invention;

Figure 6 is a flow chart showing steps performed by the base station of Figure 5;

Figures 7A-B depict an embodiment of a signal processor architecture according to the invention;

Figure 8 is a data processing chart showing information demultiplexed to the plurality of parallel signal processor elements of Figure 7;

Figure 9 is a flow chart showing steps performed by the signal processor of Figure 7;

Figures 10A-B depict another embodiment of a signal processor architecture according to the invention;

Figure 11 is a flow chart showing steps performed by the signal processor of Figure 10;

Figures 12A-B depict another embodiment of a signal processor architecture according to the invention; and

Figure 13 depicts another embodiment of a signal processor architecture according to the invention.

DETAILED DESCRIPTION

The present invention relates to a spread spectrum communication network signal processor. In particular, the present invention is used in a cellular communication network to improve the information channel capacity with a distributed signal processing architecture. Exemplary embodiments are provided for use with the Global Systems for Mobile Communication (GSM) communication protocol.

The exemplary embodiments are described herein with reference to specific configurations and protocols. Those skilled in the art will appreciate that various changes and modifications can be made to the exemplary embodiments while remaining within the scope of the present invention.

A first embodiment is described with reference to Figures 1 through 6. Figure 1 is a relatively general illustration of a cellular communication network. A number of base stations (BS) 10 are positioned to serve a number of geographically distinct cells, for example cell A and cell B. Each base station 10 is responsible for serving all the mobile stations (MS) 12 within its respective cell boundary. To perform this task, each base station 10 downloads a frequency hopping table (also known as a mobile allocation table) to each mobile station 12 so that the communication between base station 10 and mobile station 12 is on predefined frequencies, as explained more fully below.

A base station controller (BSC) 14 is coupled to every base station 10, typically via land line 92, and controls the communication between users, such as between mobile station users or existing infrastructure telephone users. Moveover, base station controller 14 controls the hand-off from one base station 10 to another base station 10 as a mobile station 12 moves among cells.

A protocol selected for the embodiments is the Global Systems for Mobile Communication (GSM) protocol. The GSM protocol is lengthy and complicated. Therefore, the salient features are discussed with respect to the embodiments. For additional information on the subject, the reader is referred to the GSM specification. One important GSM protocol requirement is frequency hopping spread spectrum (FHSS). That is, sequentially communicating over more than one frequency.

Figure 2A shows the allocated frequency spectrum for GSM communication (from the mobile station standpoint). As can be seen, the mobile station transmit frequency band (T_f) is disjoint from the mobile station receive frequency band (R_f). Each of these frequency bands occupies approximately 25MHz. Within that 25MHz, there are 124 200KHz frequency steps on which the communication frequencies are permitted to hop. An extended GSM specification is currently under development, and will include a broader range of operational frequencies. The specific hopping sequence is a function of the GSM hopping algorithm defined by the GSM specification and a given frequency hopping table that is downloaded from base station 10 to mobile station 12. An example frequency hopping table is presented in Figure 2B. Based on the GSM hopping algorithm (Figure 2C), the mobile station receiver and transmitter operate on specified 200KHz frequencies in their respective frequency bands T_f, R_f. Of course, the base station T_f and R_f correspond to the mobile station R_f and T_f respectively.

Since GSM is a digital data communication network, Figure 3 shows how a speech waveform is sampled and digitally encoded. Figure 4 shows how the encoded data is formatted into the GSM frame structure. Note that the information from one mobile station 12 is processed and placed into a specific time slot reserved for that particular mobile station 12 within a TDMA frame. Further, note that after the TDMA frame is collected, a multiframe is constructed from 26 TDMA frames, including 24 TDMA speech frames and 2 control frames. Beyond the multiframe are superframes and hyperframes. There are 51 multiframes in a superframe, and there are 2048 superframes in a hyperframe. The hyperframe number is one variable used by the GSM frequency hopping algorithm to define the frequency hopping sequence.

Based on the GSM frequency hopping algorithm (Figure 2C), the TDMA frames are then frequency hopped over the frequencies of the frequency hopping table. The mobile station receivers are also periodically hopped onto a fixed monitor frequency that is unique to each base station. The frequency hopping serves to spread the communication signal over the frequency bands T_f, R_f. One advantage of spread spectrum is reduced interference effects from other electro-magnetic sources and other base station/mobile station communications. Another advantage is that it the avoidance of frequency-selective nulls due to multipath effects. For the mobile station, three frequencies are tuned onto in one 4.615ms TDMA time frame (transmit, receive, monitor). Each mobile station transmitter and receiver synthesizer has 1 or 2 time slots (4.615ms times 1/8 or 2/8, i.e., .58ms or 1.15ms) to change frequencies. Frequency hopping once per frame is easily accomplished because the synthesizers have plenty of time (1 or 2 time slots) to settle before a new reception or transmission is required. However, the base station receiver and transmitter have only 30μs to change frequencies (the time duration of the guard bits). This short time period is difficult to accommodate, so the invention incorporates a plurality of receiver synthesizers and transmitter synthesizers as now explained.

Figure 5 depicts a base station 10 having a receiver 20, a transmitter 40 and a processor 80. As shown, receiver 20 and transmitter 40 share common antenna 21 via diplexer 23. This configuration is possible since the receive frequency and transmit frequency are different (see Figure 2A).

Diplexer 23 is used to permit the receive frequency to pass from antenna 21 to receiver 20, and to permit the transmit frequency to pass from transmitter 40 to antenna 21. Receiver 20 and transmitter 40 each employ two independent synthesizers in order to facilitate fast frequency agility. The detail of the embodiment and the operation is explained with reference to the Figure 6 flow chart.

The reset step 102 is performed only at start-up, such as when base station 10 initially comes on-line or when recovering from a power failure. Step 104 is turns off transmitter 40 to prevent invalid transmission before initialization of the base station 10. Thereafter, step 106 waits for the processor 80 to perform its self-test and other required procedures before base station 10 can become operational in the cellular network. Step 108 calculates the required first frequency and the subsequent second frequency from the GSM hyperframe number and the frequency hopping table. Once these first and second frequencies are calculated, the first and second receiver synthesizers 32, 34, and transmitter synthesizers 52, 54 are programmed to generate the required frequencies. At this point, the switches 36, 56 are set to provide the mixers 24, 44 with the frequencies from the first synthesizers 32, 52 respectively.

A loop sequence begins with step 110, where processor 80 waits for the transmitter interrupt from the CPU 82 to indicate that the TDMA frame should be processed. If the step 112 is being queried for the first time (i.e., transmitter 40 was turned off in step 104), step 114 is performed to turn transmitter 40 on. Once transmitter 40 is on, step 116 proceeds to transmit a TDMA frame and then to toggle the transmitter synthesizer selector switch 56 to the other transmitter synthesizer 54. Step 116 also calculates the next transmitter frequency and programs the previously active synthesizer 52 to generate that frequency.

When the receiver interrupt occurs in step 118, step 120 proceeds to receive a TDMA frame and then to toggle the receiver synthesizer selector switch 36 to the other receiver synthesizer 34. Step 120 also calculates the next receiver frequency and programs the previously active synthesizer 32 to generate that frequency.

Steps 110 through 120 are then repeatedly performed to transmit and receive the TDMA frames to and from the mobile stations 12 on the proper frequencies. This configuration of the dual synthesizer receiver 20 and dual synthesizer transmitter 40 permits base station 10 to faithfully accomplish all the frequency hops required for proper communication.

It is important to note that base station 10 of Figure 5 employs processor 80 to orchestrate the synthesizers 32, 34, 52, 54 and the synthesizer switches 36, 56. Processor 80 includes a central processing unit (CPU) 82 for performing many of the general procedures required to communicate over the network with mobile station 12. Processor 80 also performs procedures necessary to communicate with base station controller 14. A digital signal processor (DSP) 84 is included in processor 80 to perform many of the application specific and computationally intensive procedures such as encoding and decoding the TDMA frame data. As shown, the processor 80 also includes memory (RAM) 86, and may optionally include bulk disk memory 88. Moreover, user interface 90 is provided to receive instructions from a user and to display requested information. Ground line 92 is also provided to connect to base station controller 14 and other base stations 10 as required by the GSM specification.

In another embodiment depicted in Figures 7 through 9, the signal processing architecture is provided to increase the throughput and task-based allocation of processing resources. A first aspect of this embodiment is shown in Figure 7A, where an array of 2 wide and 2 deep DSPs are configured. A second aspect of this embodiment is shown in Figure 7B, where an N by M array of DSPs are configured. In essence, Figure 7A is Figure 7B where N=2 and M=2.

This embodiment shows how an array of signal processors 84 is arranged to process inbound information in parallel and in series. A demultiplexer 26 distributes inbound information to parallel digital signal processors 1A-NA, 2A-

NA, 1M-NM that simultaneously process inbound information correlated with each of the TDMA time slots while the series digital signal processors 1A-1M, 2A-2M, NA-NM sequentially process information in each of the respective TDMA time slots in efficient pipeline processing. This procedures is further explained with reference to Figures 8 and 9.

The data processing chart of Figure 8 shows how the inbound information is demultiplexed, by demultiplexer 26, to the plurality of parallel signal processors of Figure 7. For example, Figure 8 shows odd time slots distributed to a first processing string 1A-1M, and even time slots distributed to a Nth processing string NA-NM. For an information word of 8 time slots, up to 8 parallel processing strings are used, where each string would be associated with one time slot. One architectural principle is to balance the processing load evenly on all the strings, whether there are as many as 8 strings or a few as 2 strings.

The flow chart of Figure 9 shows steps performed by string 1 of the signal processor of Figure 7A to process the inbound information. An equalization step 152 is performed in DSP1A, where the inbound information is processed to compensate for noise, multipath fading, and other propagation related impairments. The equalized information is then deciphered in step 154 to recover the original unenciphered data bits, which is performed in DSP1A. Thereafter, step 156 burst formats the information in order to retrieve the correct data pattern from the mobile station 12. This is performed in DSP1A. Next, step 158 deinterleaves the data to reconstruct the proper data words for each respective mobile station 12. This is performed in DSP1B. Step 160 is performed to decode the data in order to properly detect errors and correct the data for errors when possible. This is performed in DSP1B. Once the inbound information is error corrected, then the information is delivered to central processor 82. The central 82 processor may also further process the information, switch the information to other processors for further processing, communicate the information to an outbound information link (e.g., E1 link), or may use the information to modify its own processing steps.

The same sequential steps shown in Figure 9 are also performed on a different timeslot in second string DSP2A and DSP2B shown in Figure 7A. The same sequential steps of Figure 9 may also be performed in any array size in parallel strings DSPNA-DSPNM shown in Figure 7B. Moreover, the steps shown in Figure 9 can be distributed to even more DSPs in a string if M is chosen greater than 2.

In another embodiment depicted in Figures 10 and 11, the signal processing architecture is provided to increase the throughput and task-based allocation of processing resources. A first aspect of this embodiment is shown in Figure 10A, where an array of 2 wide and 1 deep DSPs are configured. A second aspect of this embodiment is shown in Figure 10B, where an N by M array of DSPs are configured. In essence, Figure 10A is Figure 10B where N=2 and M=1.

This embodiment shows how an array of signal processors 84 is arranged to process outbound information in parallel and in series. Parallel digital signal processors 1A-NA, 2A-NA, 1M-NM simultaneously process outbound information correlated with each of the TDMA time slots while the series digital signal processors 1A-1M, 2A-2M, NA-NM sequentially process information in each of the respective TDMA time slots in efficient pipeline processing. Then, multiplexer 46 distributes the information to transmitter 40. This procedures is further explained with reference to Figure 11.

The flow chart of Figure 11 shows steps performed by string 1 of the signal processor of Figure 10A to process the outbound information. Central processor 82 obtains outbound information to be transmitted to the mobile stations 12. The outbound information is processed and prepared for delivery to the signal processing array 84. DSP array 84 may also receive speech traffic from a space/time switch included is processor 82 that routes traffic to and from an information link (e.g., E1 link) or other processors. Step 172 is performed to encode the data so that the mobile station 12 can properly detect errors and correct the data for errors when possible. This is performed in DSP1A. Next, step 174 interleaves the data to distribute the outbound information over several TDMA frames. This is performed in DSP1A. Thereafter, step 176 burst formats the information in order to construct the correct data pattern for the mobile station 12. This is performed in DSP1A. A ciphering step 178 is performed in DSP1A to encrypt the outbound information to prevent interception by unauthorized mobile stations. When a two deep (N=2) aspect of this embodiment is employed, step 178 is performed in DSP1B. Then the outbound information is delivered to multiplexer 46 and sent to the transmitter 40 to be transmitted to the mobile stations 12.

The same sequential steps shown in Figure 11 are also performed on a different timeslot in second string DSP2A and DSP2B shown in Figure 10A. The same sequential steps of Figure 11 may also be performed in any array size in parallel strings DSPNA-DSPNM shown in Figure 10B. Moreover, the steps shown in Figure 11 can be distributed to even more DSPs in a string if M is chosen greater than 2.

Figure 12 depicts another embodiment of a signal processor architecture according to the invention. A first aspect of this embodiment is shown in Figure 12A, where an array of 2 wide and 2 deep DSPs are configured. A second aspect of this embodiment is shown in Figure 12B, where an N by M array of DSPs are configured. In essence, Figure 12A is Figure 12B where N=2 and M=2. Separate receive antenna 22 and transmit antenna 42 are shown in Figure 12, but they could be combined into a common antenna 21 as shown in Figure 5.

In this embodiment, the inbound processing functions and the outbound processing functions are combined in signal processing array 84. This configuration employs the processing steps described with respect to Figures 9 and 11. One advantage to this architecture is that the duty cycles of the various DSP elements are well balanced. This feature promotes efficient processing.

For example, in the receive only processing of Figure 7A, the DSP1A element have a high duty cycle because the initial processing (equalization) is intensive. However, the DSP1B element has a lower duty cycle because the subsequent processing (decoding) is less intensive. In this embodiment shown in Figure 12A, the outbound information processing (encoding) is combined with the inbound information processing (decoding) to efficiently increase the duty cycle of the DSP1B element. An approximate measure of computational intensity is that the equalization is twice as intensive as the decoding. Hence, in a two deep array, if the inbound equalization is performed in DSP1A, and the inbound decoding and outbound encoding is performed in DSP1B, then both DSPs are equally loaded. Moreover, this processing allocation is also efficient because the outbound encoding employs similar, or reciprocal, processing steps as the inbound decoding, but often in reverse. Thus, much of the program memory and lookup tables are the same.

DSP1B keeps track of which information it is processing so that the inbound information is sent to processor 82 (or DSP1M in Figure 12B) and the outbound information is sent to the multiplexer 46. The processing of DSP2A and DSP2B are similarly allocated, as are DSPNA and DSPNB. Moreover, if the processing is further distributed in the array 84 of Figure 12B, the processing allocation is distributed within all the parallel processing pipelines DSP1A-DSP1M through DSPNA-DSPNM.

Note that this embodiment also shows CPU 82 with a space/time switch for routing information to and from a plurality of transcoder rate adapting units 94, echo cancelers 96, and public switched telephone network 98. This configuration permits the processor 80 to control the entire operation of the inbound information and outbound information.

Note also that the described control functions of CPU 82 can be distributed among several processors. In one implementation, CPU 82 includes several subordinate microcontrollers resident with the DSPs or with the space/time switch, all linked to and reporting to a central processor.

In actual implementation, it is useful to employ a plurality of receivers and transmitters in order to perform both TDMA and FDMA, as provided by the GSM specification. For example, in a conventional configuration, each receiver is tuned to a fixed frequency and frequency-hopped information from the mobile stations is received and transmitted by various receivers depending on the specified communication frequency. Then the conventional processor must re-assemble inbound information from a plurality of receivers to obtain data from one mobile station. Moreover, the conventional processor must dis-assemble outbound information and deliver it to a plurality of transmitters to properly transmit information to a mobile station.

Figure 13 depicts another embodiment of a base station 10 according to the invention. There are provided a plurality of transceivers 200A-P that are frequency agile (as shown in Figure 5). Hence, transceivers 200A-P can be programmed to receive various frequencies over time and can receive information from each mobile station 12 on a respective one of transceivers 200A-P. This feature permits both TDMA received signals and FDMA received signals associated with one mobile station 12 to be received by one of the transceivers 200A-P. Because processor 80 programs the receiver synthesizers, processor 80 has a priori knowledge of which transceiver 200A-P is receiving communication signals from which mobile station 12. This information permits the processor to more efficiently process the inbound data. For example, if the signal from one mobile station 12 is always received in transceiver card one 200A, then the processor 80 can reduce its control logic (hardware, software, or both) to avoid the conventional step of re-assembling a mobile station's data from a number of different receivers. Also, configuring a plurality of frequency agile transceivers 200A-P in parallel permits processor 80 to reconfigure transceivers 200A-P at any time a fault is detected. If, for example, processor 80 detects a fault in transceiver 200A (e.g., by self-test, null data, or corrupted data), processor 80 re-programs another transceiver, such as transceiver 200P, to operate on the parameters that were previously assigned to transceiver 200A. The feature of agile transceivers and enhanced processing resource allocation reduces overhead, permits fault tolerance, and increases throughput since it eliminates a processing step. Moreover, the features discussed with respect to receiving information from the mobile stations 12 is equally applicable to transmitting outbound information to the mobile stations 12 via transceivers 200A-P.

As shown, transceivers 200A-P can be coupled to a common transmit antenna 42. However, if transceivers 200A-P are sensitive to back propagation of each other's transmissions, a plurality of transmit antennas (42A-P) can be employed with each transceiver having its own transmit antenna. Moreover, separate receive antennas 22A-P and transmit antennas 42A-P are shown in Figure 13, but they could be combined into a common antennas 21A-P as shown in Figure 5.

Additional base station embodiments are described in CELLULAR BASE STATION WITH INTELLIGENT CALL ROUTING, U.S. Ser. No. 08/434,598, filed on May 4, 1995, Attorney docket No. A-61115, which is incorporated herein by reference.

Advantages of the present invention include reduced interference, improved communication bandwidth, fault tolerance, modularity, scalability, and more efficient and cost-effective base stations and mobile stations.

An additional advantage of the embodiment shown in Figure 13 is that the transceivers 200A-P can be removed from or inserted into an operational station 12. This permits a technician to remove a broken transceiver and insert a new transceiver while the base station remains operational. The broken transceiver card can then be repaired and returned to service when needed.

As used herein, when a first element and a second element are coupled, they are related to one another, but need not have a direct path to one another. For example, a signal processing element may be coupled to a receiver element via a demultiplexer. However, when a first element and second element are connected, they are required to have a direct path to one another.

ALTERNATIVE EMBODIMENTS

Having disclosed exemplary embodiments and the best mode, modifications and variations may be made to the disclosed embodiments while remaining within the scope of the present invention as defined by the following claims.

What is claimed is:

1. A base station for communicating over a cellular network with a mobile station, comprising:

a receiver configured to receive inbound information from the mobile station;

a first signal processor coupled to said receiver and configured to equalize said inbound information;

a second signal processor coupled to said first signal processor and configured to decode said inbound information;

a central processor coupled to said second signal processor and configured to receive said inbound information, to process said inbound information, and to communicate said inbound information with a public switched telephone network.

2. The base station of claim 1 for further communicating with a second mobile station, and wherein said inbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, said base station further comprising:

a third signal processor coupled to said receiver and configured to equalize said inbound information;

a fourth signal processor coupled to said third signal processor and configured to decode said inbound information, and wherein said central processor is further coupled to said fourth signal processor;

a demultiplexer disposed between said receiver and said first signal processor and between said receiver and said third signal processor, so that said demultiplexer is coupled to said receiver, said first signal processor, and said third signal processor, said demultiplexer configured to route said inbound information associated with the first time slot to said first signal processor and said inbound information associated with the second time slot to said third signal processor.

3. The base station of claim 1, wherein:

said central processor is further configured to communicate outbound information with the public switched telephone network and to process said outbound information;

said second signal processor is further configured to encode said outbound information; and

said base station further comprises a transmitter coupled to said second signal processor and configured to transmit said outbound information to the mobile station.

4. The base station of claim 3 for further communicating with a second mobile station, and wherein said inbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, and said outbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, said base station further comprising:

a third signal processor coupled to said receiver and configured to equalize said inbound information;

a fourth signal processor coupled to said third signal processor and configured to decode said inbound information and encode said outbound information, and wherein said central processor is further coupled to said fourth signal processor;

a demultiplexer disposed between said receiver and said first signal processor and between said receiver and said third signal processor, so that said demultiplexer is coupled to said receiver, said first signal processor, and said third signal processor, said demultiplexer configured to route said inbound information associated with the first time slot to said first signal processor and said inbound information associated with the second time slot to said third signal processor;

wherein said central processor is configured to route said outbound information associated with the first time slot to said second signal processor and said outbound information associated with the second time slot to said fourth signal processor; and

a multiplexer disposed between said second signal processor and said transmitter and between said fourth signal processor and said transmitter, so that said multiplexer is coupled to said transmitter, said second signal processor, and said fourth signal processor, said multiplexer configured to route said outbound information associated with the first time slot to said transmitter and said outbound information associated with the second time slot to said transmitter.

5. The base station of claim 1, wherein:

said central processor is further configured to communicate outbound information with the public switched telephone network and to process said outbound information;

said second signal processor is further configured to encode said outbound information;

said first signal processor is further configured to encrypt said outbound information; and

said base station further comprises a transmitter coupled to said first signal processor and configured to transmit said outbound information to the mobile station.

6. The base station of claim 5 for further communicating with a second mobile station, and wherein said inbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, and said outbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, said base station further comprising:

a third signal processor coupled to said receiver and configured to equalize said inbound information and to encrypt said outbound information;

a fourth signal processor coupled to said third signal processor and configured to decode said inbound information and encode said outbound information, and wherein said central processor is further coupled to said fourth signal processor;

a demultiplexer disposed between said receiver and said first signal processor and between said receiver and said third signal processor, so that said demultiplexer is coupled to said receiver, said first signal processor, and said third signal processor, said demultiplexer configured to route said inbound information associated with the first time slot to said first signal processor and said inbound information associated with the second time slot to said third signal processor;

wherein said central processor is configured to route said outbound information associated with the first time slot to said second signal processor and said outbound information associated with the second time slot to said fourth signal processor; and

a multiplexer disposed between said first signal processor and said transmitter and between said third signal processor and said transmitter, so that said multiplexer is coupled to said transmitter, said first signal processor, and said third signal processor, said multiplexer configured to route said outbound information associated with the first time slot to said transmitter and said outbound information associated with the second time slot to said transmitter.

7. The base station of claim 1, wherein:

said central processor is further configured to communicate outbound information with the public switched telephone network and to process said outbound information; and

said base station further comprises:

a third signal processor coupled to said central processor and configured to encode said outbound information; and

a transmitter coupled to said third signal processor and configured to transmit said outbound information to the mobile station.

8. The base station of claim 7 for further communicating

with a second mobile station, and wherein said inbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, and said outbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, said base station further comprising:

a fourth signal processor coupled to said receiver and configured to equalize said inbound information;

a fifth signal processor coupled to said fourth signal processor and configured to decode said inbound information, and wherein said central processor is further coupled to said fourth signal processor;

a sixth signal processor coupled to said central processor and configured to encode said outbound information;

a demultiplexer disposed between said receiver and said first signal processor and between said receiver and said fourth signal processor, so that said demultiplexer is coupled to said receiver, said first signal processor, and said fourth signal processor, said demultiplexer configured to route said inbound information associated with the first time slot to said first signal processor and said inbound information associated with the second time slot to said fourth signal processor; and

a multiplexer disposed between said third signal processor and said transmitter and between said sixth signal processor and said transmitter, so that said multiplexer is coupled to said transmitter, said third signal processor, and said sixth signal processor, said multiplexer configured to route said outbound information associated with the first time slot to said transmitter and said outbound information associated with the second time slot to said transmitter.

9. A base station for communicating over a cellular network with a mobile station, comprising:

a central processor configured to communicate outbound information with a public switched telephone network and to process said outbound information;

a first signal processor coupled to said central processor and configured to encode said outbound information; and

a transmitter coupled to said first signal processor and configured to transmit said outbound information to the mobile station.

10. The base station of claim 9 for further communicating with a second mobile station, and wherein said outbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, said base station further comprising:

a second signal processor coupled to said central processor and configured to encode said outbound information;

wherein said central processor is configured to route said outbound information associated with the first time slot to said first signal processor and said outbound information associated with the second time slot to said second signal processor; and

a multiplexer disposed between said first signal processor and said transmitter and between said second signal processor and said transmitter, so that said multiplexer is coupled to said transmitter, said first signal processor, and said second signal processor, said multiplexer configured to route said outbound information associated with the first time slot to said transmitter and said outbound information associated with the second time slot to said transmitter.

11. The base station of claim 9 for further communicating with a second mobile station, and wherein said outbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station, said base station further comprising:

a second signal processor disposed between said first signal processor and said transmitter and configured to encrypt said outbound information;

a third signal processor coupled to said central processor and configured to encode said outbound information;

a fourth signal processor coupled to said third signal processor and configured to encrypt said outbound information;

wherein said central processor is configured to route said outbound information associated with the first time slot to said first signal processor and said outbound information associated with the second time slot to said third signal processor; and

a multiplexer disposed between said second signal processor and said transmitter and between said fourth signal processor and said transmitter, so that said multiplexer is coupled to said transmitter, said second signal processor, and said fourth signal processor, said multiplexer configured to route said outbound information associated with the first time slot to said transmitter and said outbound information associated with the second time slot to said transmitter.

12. A base station for communicating over a cellular network with a plurality of mobile stations, comprising:

a central processor;

a plurality of transceivers coupled to said central processor and configured to receive inbound information from the mobile stations and to transmit outbound information to the mobile stations; and

wherein each of said transceivers includes a demultiplexer coupled to a receiver and to an array of signal processors having at least two parallel processing paths, said demultiplexer configured to route said inbound information to said array, and a multiplexer coupled to said array and to a transmitter, said multiplexer configured to route said outbound information to said transmitter.

13. The base station of claim 10, wherein:

each of said transceivers is configured to receive on a plurality of predefined frequencies;

each of said transceivers is configured to transmit on a plurality of predefined frequencies;

each said demultiplexer is configured to route different time based information from said receiver to each of said parallel processing paths of said array; and

each said multiplexer is configured to route different time based information from each of said parallel processing paths of said array to said transmitter.

14. A method of processing inbound information transmitted from a mobile station and received at a base station having a transceiver, a first signal processor, a second signal processor, and a central processor, said method comprising the steps of:

receiving the inbound information in the transceiver;

equalizing the inbound information in the first signal processor;

decoding the inbound information in the second signal processor;

processing the inbound information in the central processor in preparation to presenting the inbound information to a public telephone switched network.

15. The method of claim 14 for further processing inbound information transmitted from a second mobile station and received by the base station, wherein the base station further has a demultiplexer, a third signal processor, and a fourth signal processor, said method further comprising the steps of:

dividing the inbound information into a first time slot associated with the first mobile station and a second time slot associated with the second mobile station and delivering inbound information associated with the first time slot to the first signal processor and inbound information associated with the second time slot to the third signal processor;

equalizing the inbound information associated with the second time slot in the third signal processor;

decoding the inbound information associated with the second time slot in the fourth signal processor; and

wherein said step of equalizing the inbound information in the first signal processor is performed by equalizing the inbound information associated with the first time slot in the first signal processor; and

wherein said step of decoding the inbound information in the second signal processor is performed by decoding the inbound information associated with the first time slot in the second signal processor.

16. The method of claim 14 for further processing outbound information from a public switched telephone network via the base station, destined for the mobile station, said method further comprising the steps of:

receiving the outbound information in the central processor;

processing the outbound information in the central processor in preparation to presenting the outbound information to the second signal processor;

encoding the outbound information in the second signal processor;

transmitting the outbound information in the transceiver.

17. The method of claim 16, further comprising the step of:

encrypting the outbound information in the first signal processor.

18. The method of claim 15 for further processing outbound information from a public switched telephone network via the base station, destined for the mobile station, the base station further having a multiplexer, said method further comprising the steps of:

receiving the outbound information in the central processor, where the outbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station and delivering outbound information associated with the first time slot to the second signal processor and outbound information associated with the second time slot to the fourth signal processor;

encoding the outbound information associated with the first time slot in the second signal processor;

encoding the outbound information associated with the second time slot in the fourth signal processor; and

transmitting the outbound information in the transceiver.

19. The method of claim 18, further comprising the steps of:

encrypting the outbound information associated with the first time slot in the first signal processor; and

encrypting the outbound information associated with the second time slot in the third signal processor.

20. A method of processing outbound information from a public switched telephone network in a base station having a transceiver, a first signal processor, a second signal processor, a central processor, and a multiplexer, the outbound information destined for a first mobile station and a second mobile station, said method comprising the steps of:

receiving the outbound information in the central processor, where the outbound information includes a first time slot associated with the first mobile station and a second time slot associated with the second mobile station and delivering outbound information associated with the first time slot to the first signal processor and outbound information associated with the second time slot to the second signal processor;

encoding the outbound information associated with the first time slot in the first signal processor;

encoding the outbound information associated with the second time slot in the second signal processor; and

transmitting the outbound information in the transceiver.

21. The method of claim 20, wherein the base station further has a third signal processor and a fourth signal processor, said method further comprising the steps of:

encrypting the outbound information associated with the first time slot in the third signal processor;

encrypting the outbound information associated with the second time slot in the fourth signal processor.

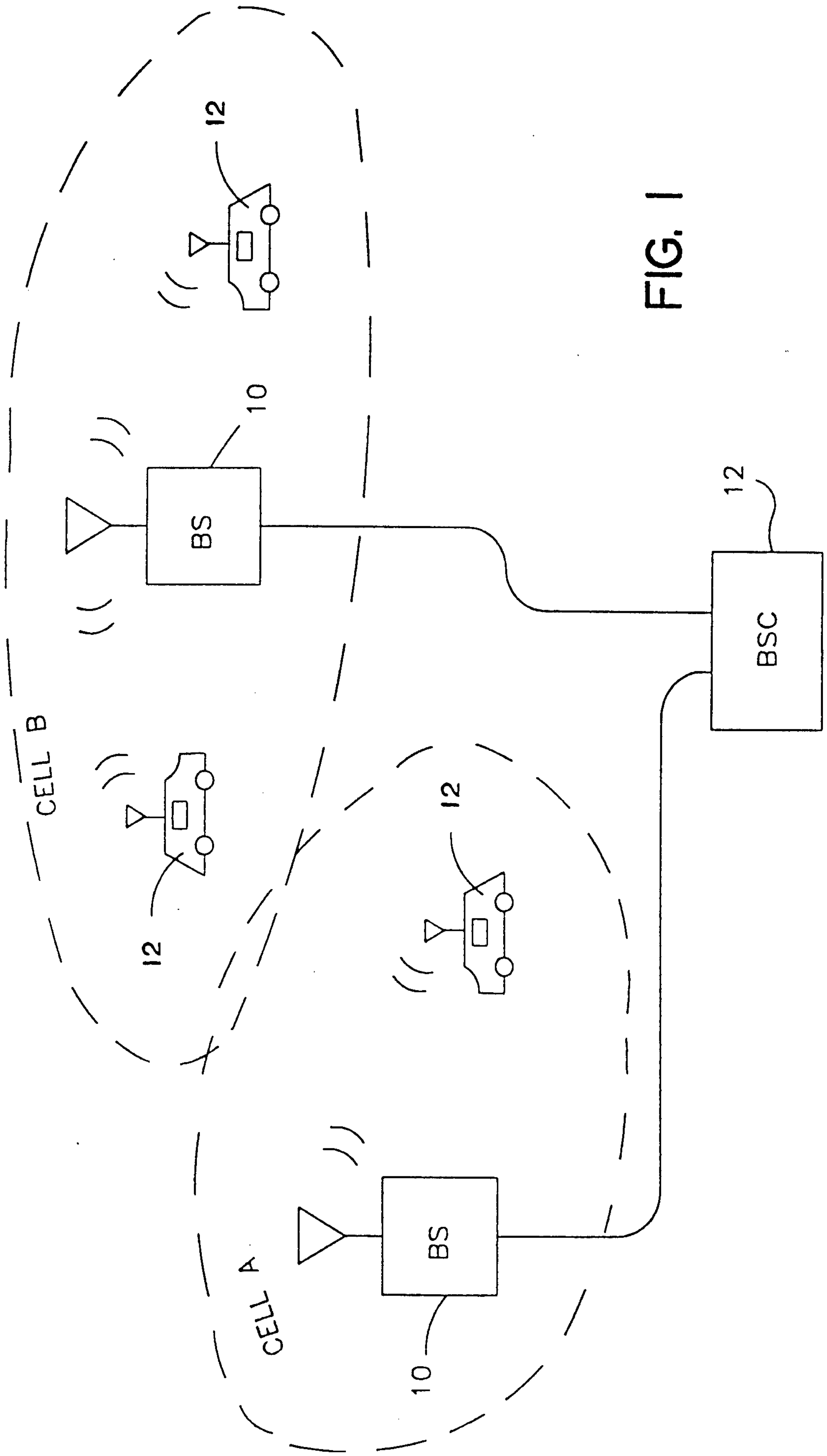


FIG. 1

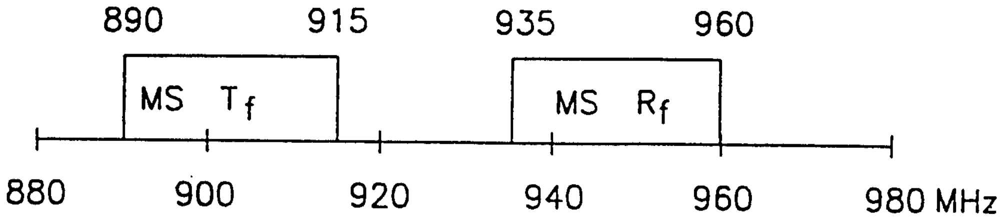
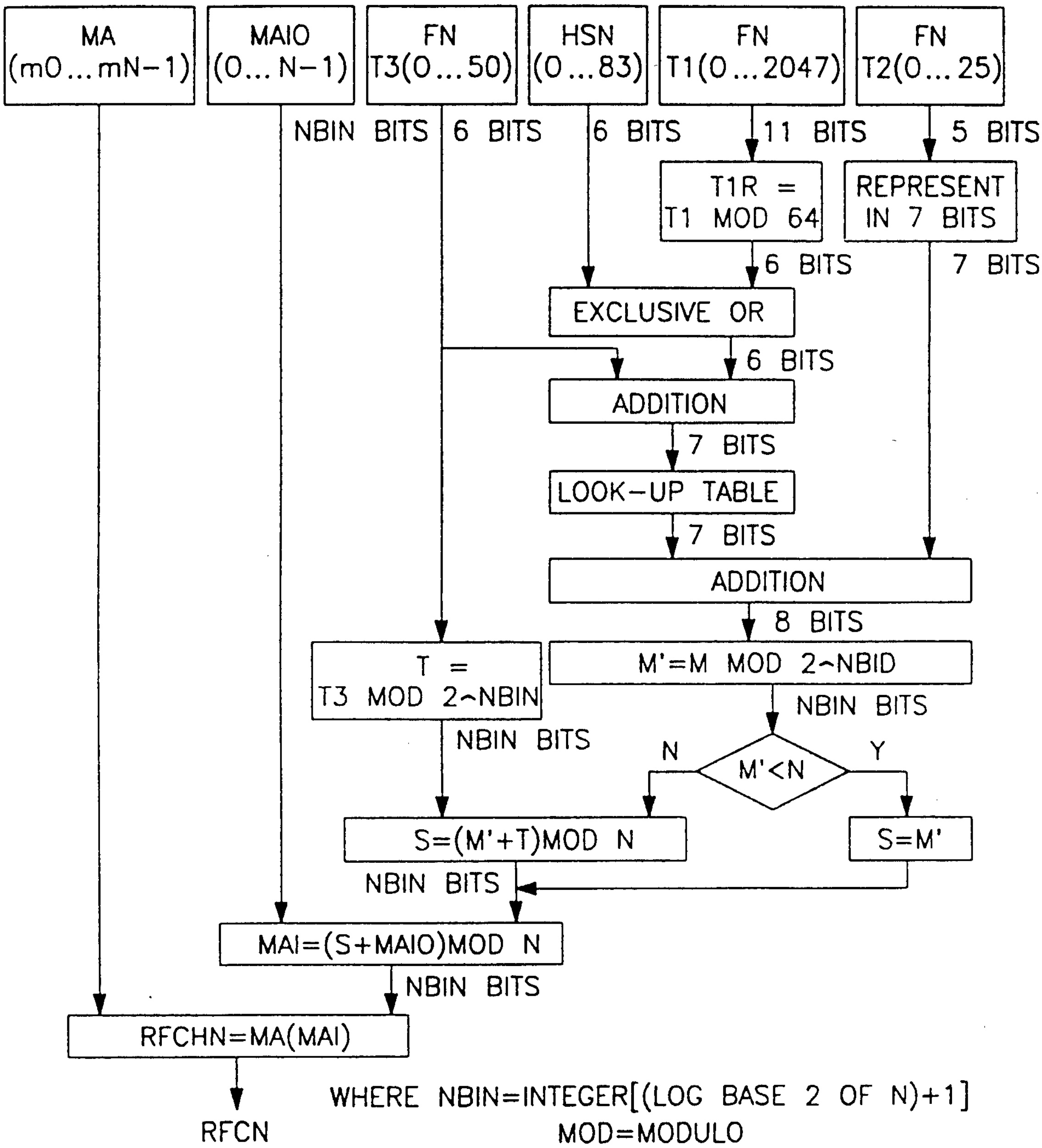


FIG. 2A

#	MS TRANSMIT	MS RECEIVE
0	m0	m0+45MHz
1	m1	m1+45MHz
2	m2	m2+45MHz
3	m3	m3+45MHz
⋮	⋮	⋮
N−1	mN−1	mN−1+45MHz

FIG. 2B

FN FRAME NUMBER
HSN HOPPING SEQUENCE NUMBER – 0...63
MA MOBILE ALLOCATION – SET OF N FREQUENCIES AVAILABLE FOR USE m0...mN-1
MAIO MOBILE ALLOCATION INDEX – OFFSET IN MA TABLE
N NUMBER OF FREQUENCIES IN MA
RFCHN RAIDO FREQUENCY CHANNEL NUMBER



WHERE NBIN=INTEGER[(LOG BASE 2 OF N)+1]
MOD=MODULO
^=RAISED TO THE POWER OF

FIG. 2C

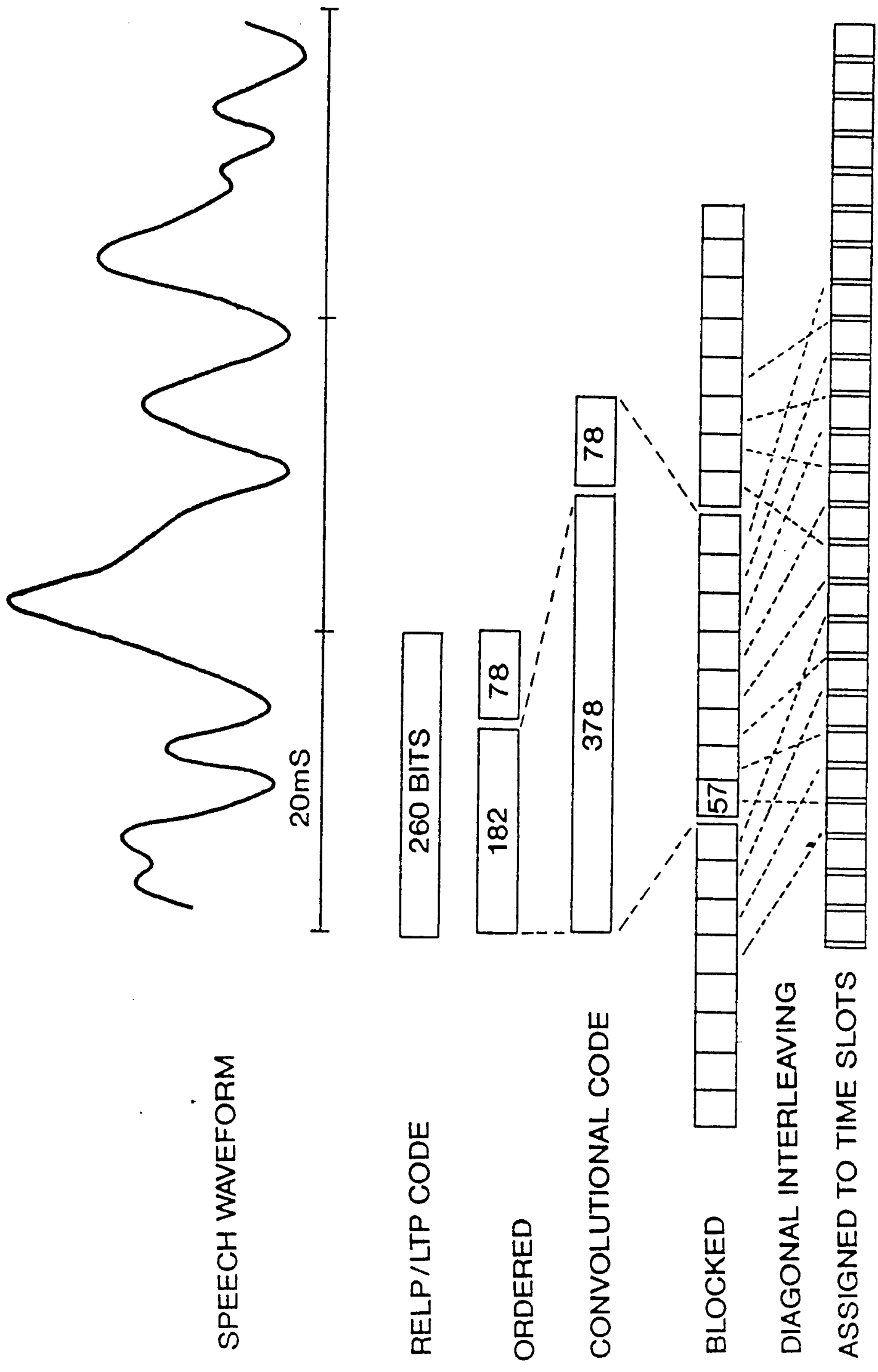

SPEECH WAVEFORM
20mS
RELP/LTP CODE
260 BITS
ORDERED
182
78
CONVOLUTIONAL CODE
378
78
BLOCKED
57
DIAGONAL INTERLEAVING
ASSIGNED TO TIME SLOTS

FIG. 3

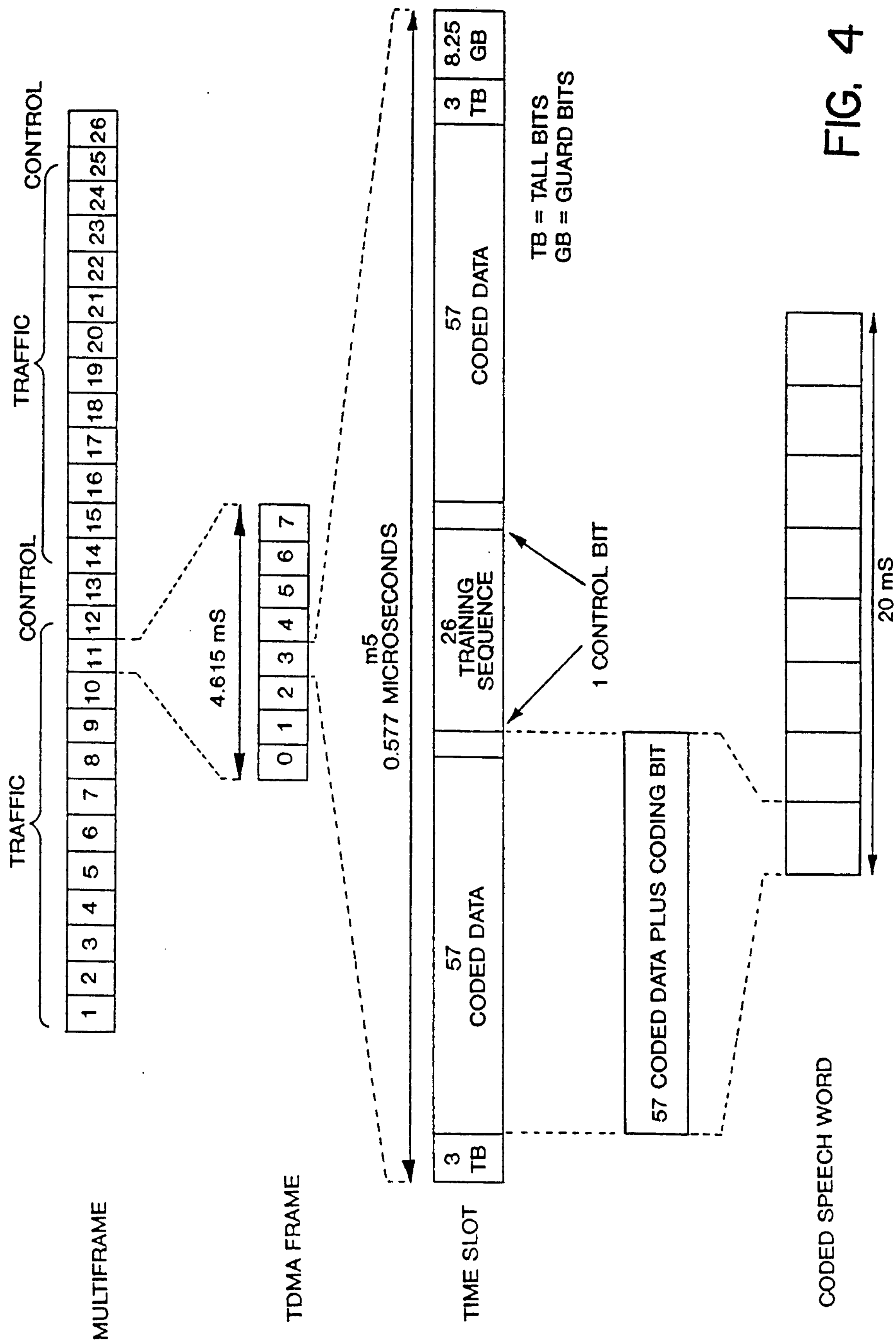

MULTIFRAME
TRAFFIC
CONTROL
TRAFFIC
CONTROL
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
TDMA FRAME
4.615 mS
0 1 2 3 4 5 6 7
TIME SLOT
0.577 MICROSECONDS
m5
3 TB
57 CODED DATA
26 TRAINING SEQUENCE
57 CODED DATA
3 TB
8.25 GB
1 CONTROL BIT
TB = TALL BITS
GB = GUARD BITS
57 CODED DATA PLUS CODING BIT
CODED SPEECH WORD
20 mS

FIG. 4

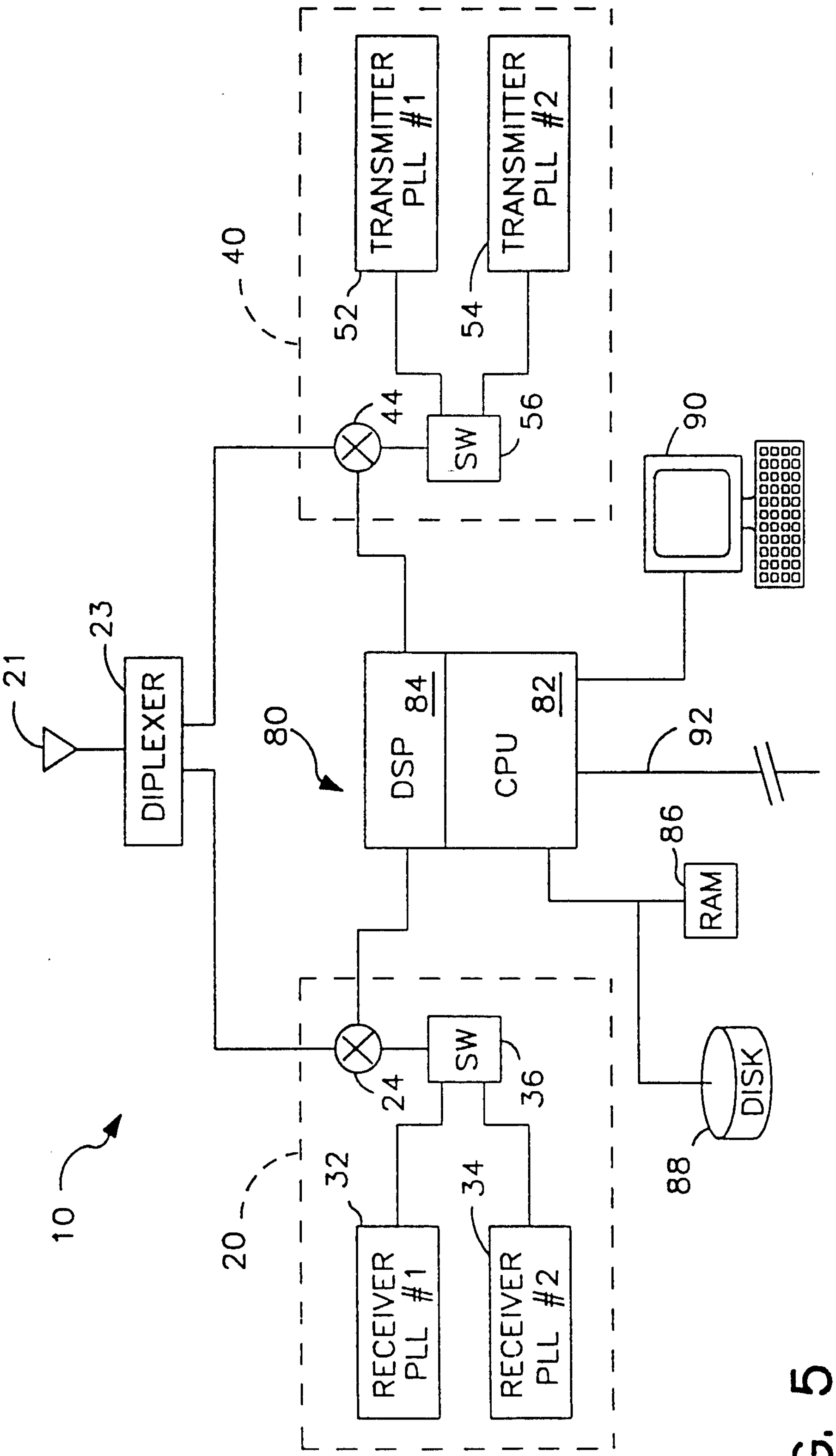
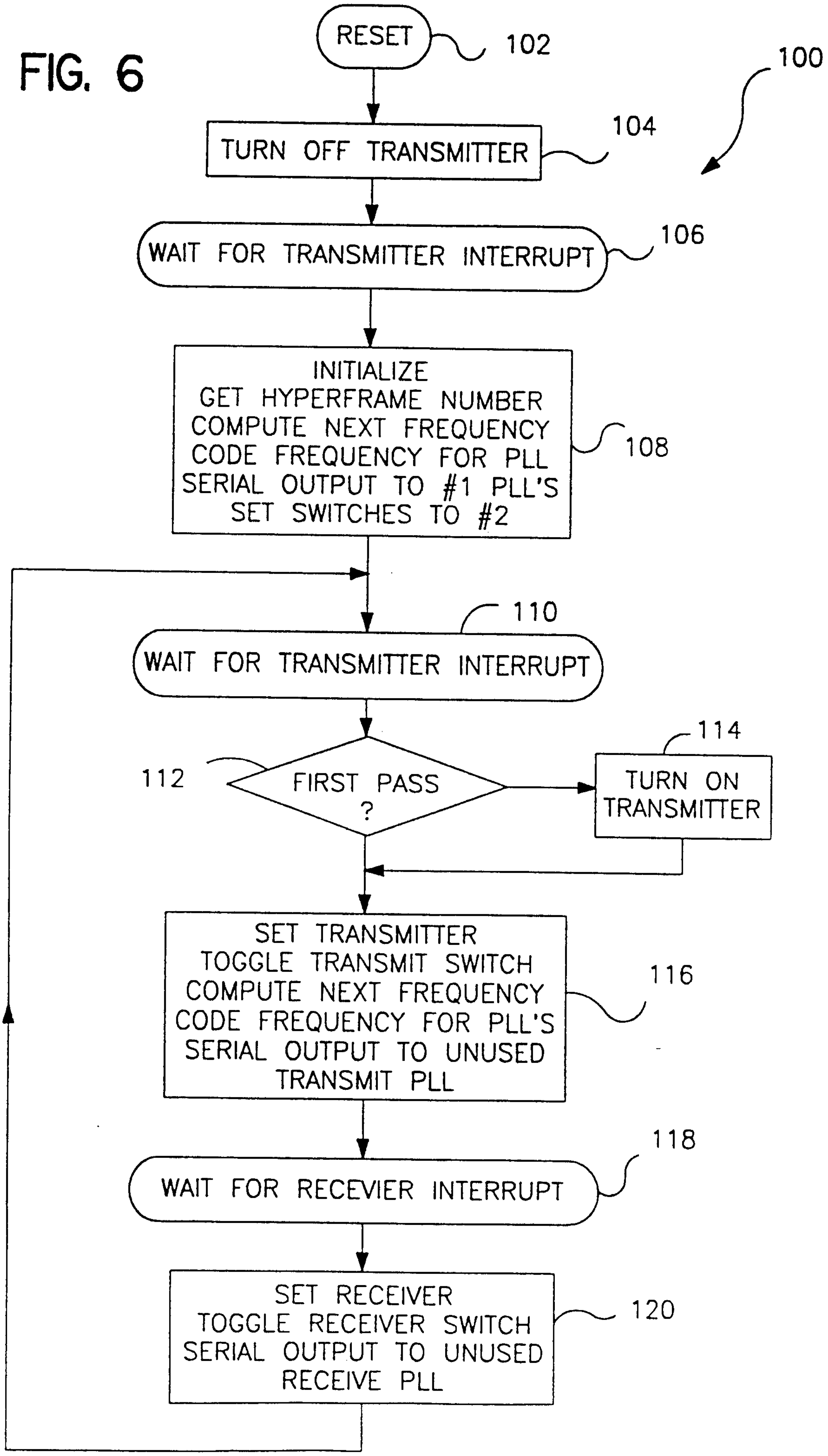

TRANSMITTER PLL #1
TRANSMITTER PLL #2
RECEIVER PLL #1
RECEIVER PLL #2
DIPLEXER
DSP 84
CPU 82
SW
SW
RAM
DISK
10
20
21
23
24
32
34
36
40
44
52
54
56
80
86
88
90
92

FIG. 5

FIG. 6


RESET
102
100
TURN OFF TRANSMITTER
104
WAIT FOR TRANSMITTER INTERRUPT
106
INITIALIZE
GET HYPERFRAME NUMBER
COMPUTE NEXT FREQUENCY
CODE FREQUENCY FOR PLL
SERIAL OUTPUT TO #1 PLL'S
SET SWITCHES TO #2
108
110
WAIT FOR TRANSMITTER INTERRUPT
112
FIRST PASS
?
114
TURN ON
TRANSMITTER
SET TRANSMITTER
TOGGLE TRANSMIT SWITCH
COMPUTE NEXT FREQUENCY
CODE FREQUENCY FOR PLL'S
SERIAL OUTPUT TO UNUSED
TRANSMIT PLL
116
118
WAIT FOR RECEVIER INTERRUPT
SET RECEIVER
TOGGLE RECEIVER SWITCH
SERIAL OUTPUT TO UNUSED
RECEIVE PLL
120

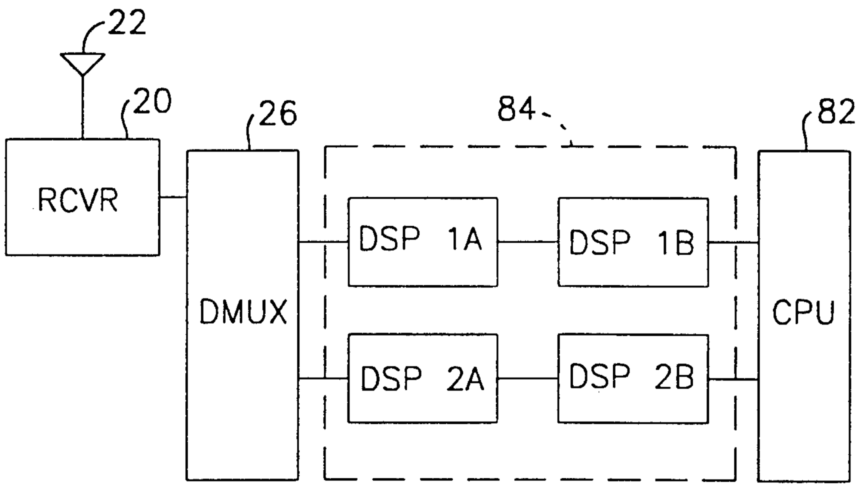

22
20
26
84
82
RCVR
DMUX
DSP 1A
DSP 1B
DSP 2A
DSP 2B
CPU

FIG. 7A

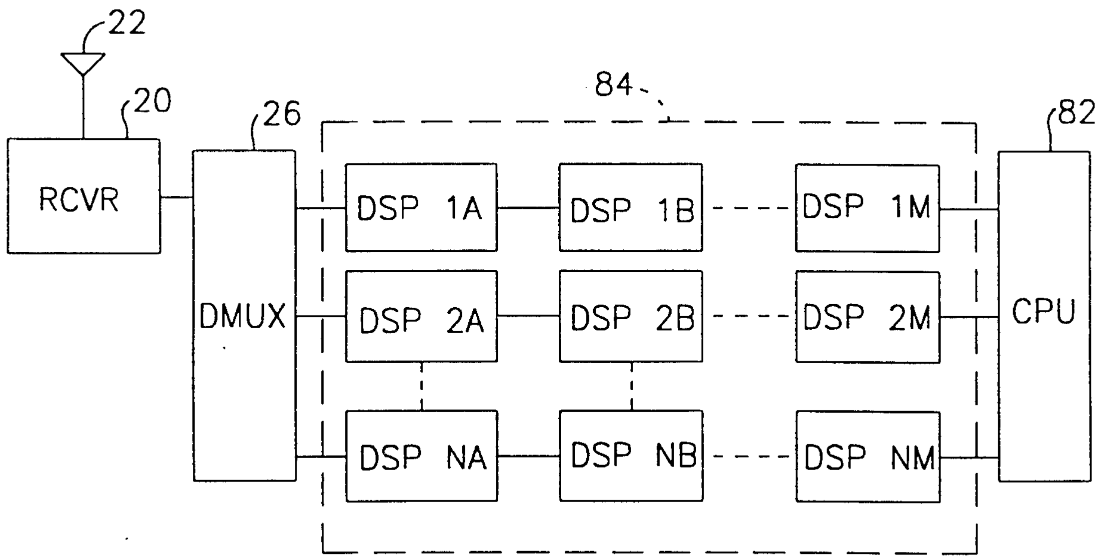

22
20
26
84
82
RCVR
DMUX
DSP 1A
DSP 1B
DSP 1M
DSP 2A
DSP 2B
DSP 2M
DSP NA
DSP NB
DSP NM
CPU

FIG. 7B

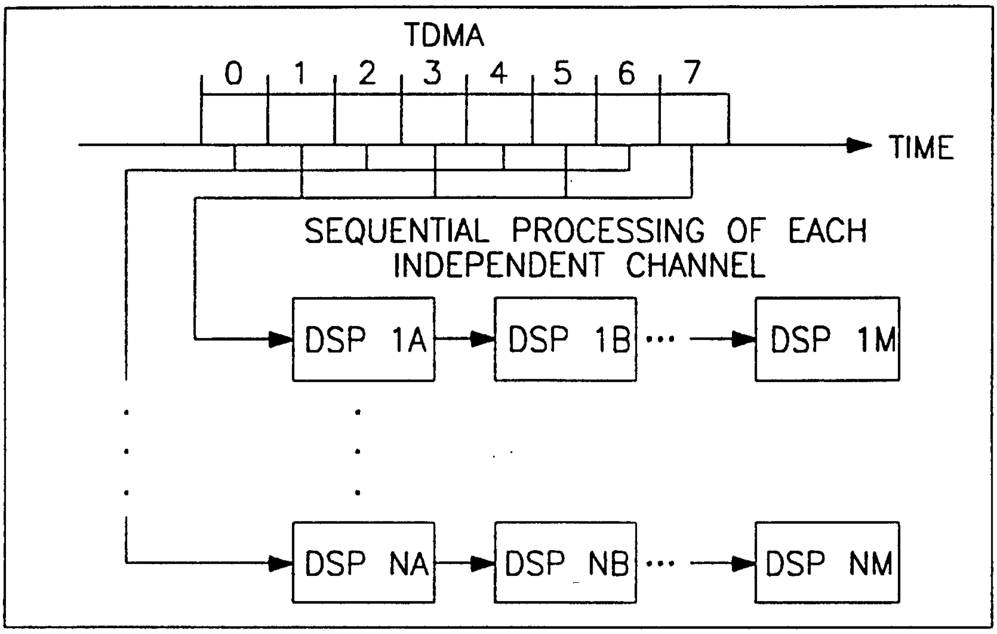

TDMA
0
1
2
3
4
5
6
7
TIME
SEQUENTIAL PROCESSING OF EACH INDEPENDENT CHANNEL
DSP 1A
DSP 1B
DSP 1M
DSP NA
DSP NB
DSP NM

FIG. 8

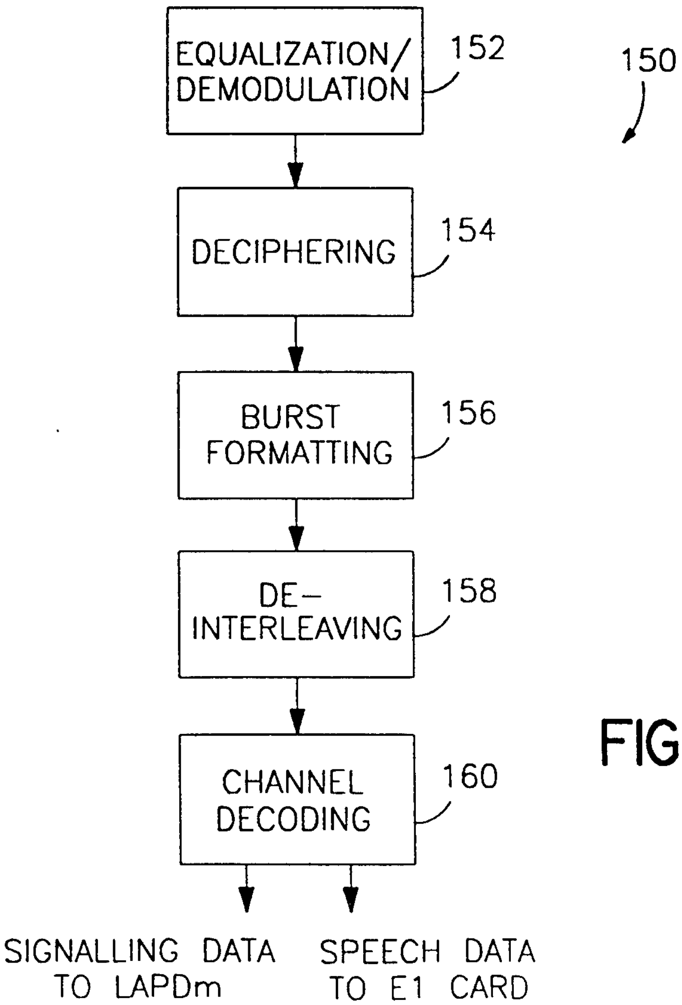

EQUALIZATION/ DEMODULATION
152
150
DECIPHERING
154
BURST FORMATTING
156
DE-INTERLEAVING
158
CHANNEL DECODING
160
SIGNALLING DATA TO LAPDm
SPEECH DATA TO E1 CARD

FIG. 9

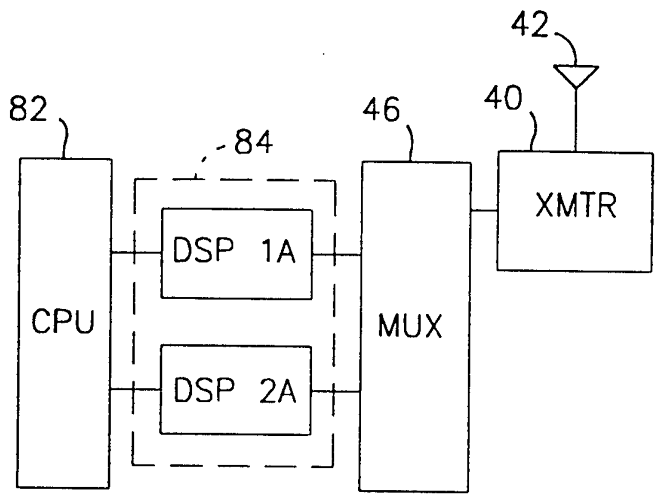


FIG. 10A

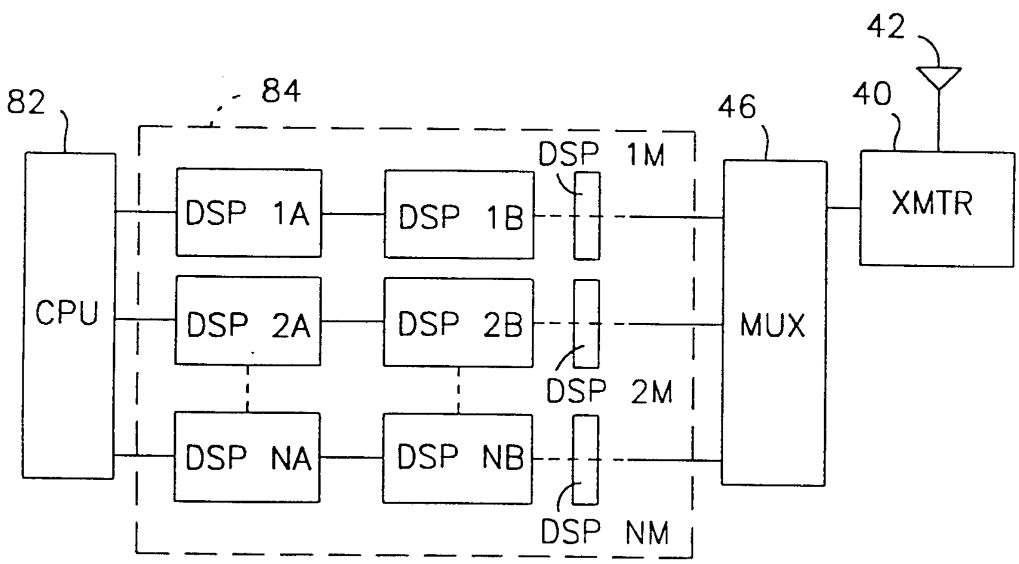


FIG. 10B

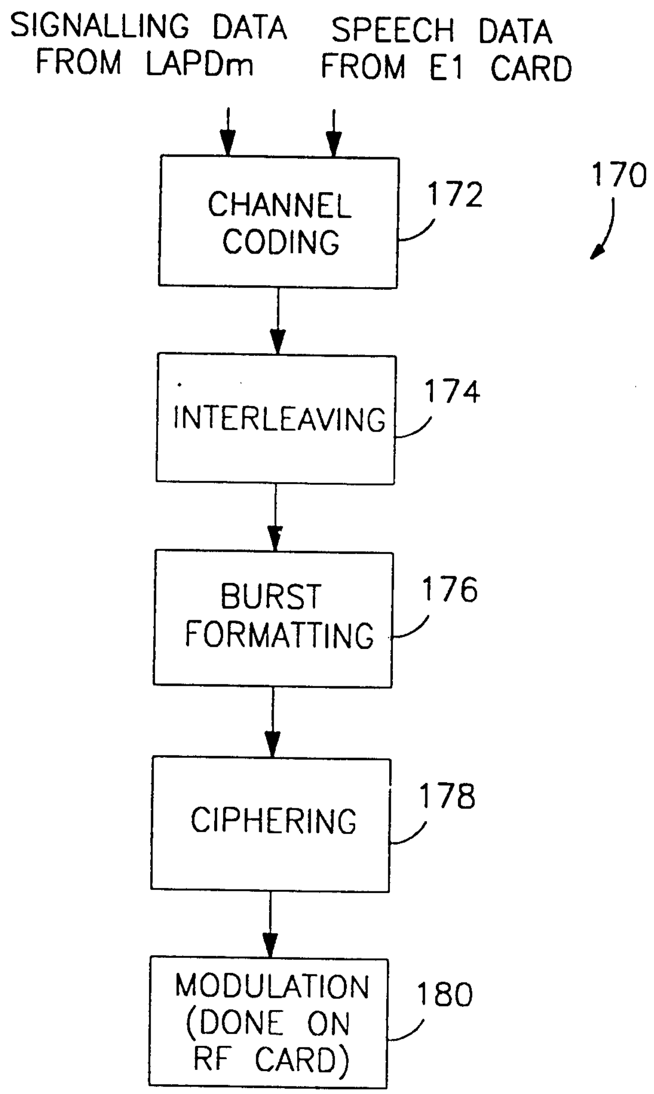


FIG. 11

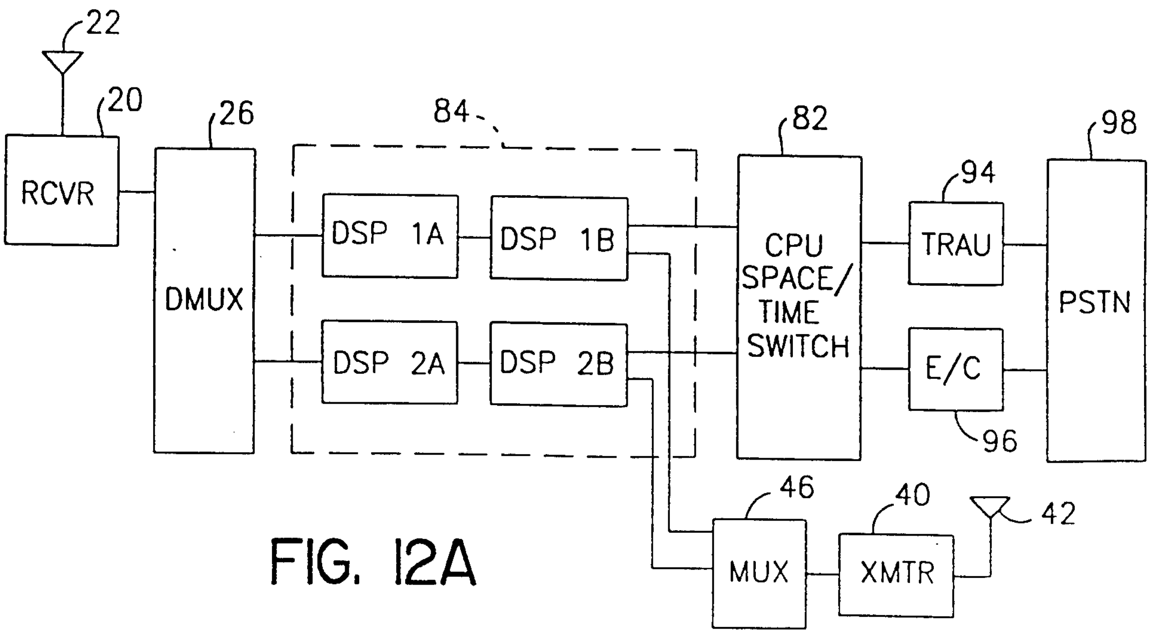
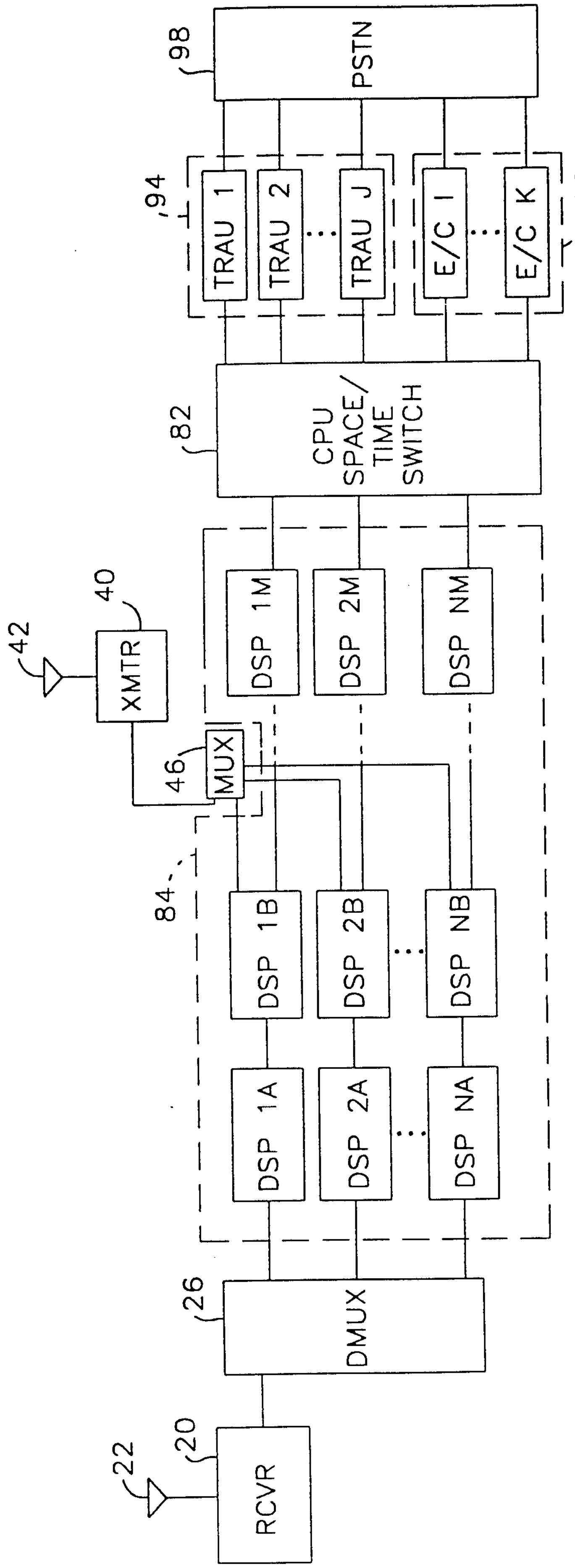


FIG. 12A



PSTN
98
TRAU 1
TRAU 2
TRAU J
94
E/C I
E/C K
96
CPU
SPACE/
TIME
SWITCH
82
DSP 1M
DSP 2M
DSP NM
XMTR
40
42
MUX
46
84
DSP 1B
DSP 2B
DSP NB
DSP 1A
DSP 2A
DSP NA
DMUX
26
RCVR
20
22

FIG. 12B

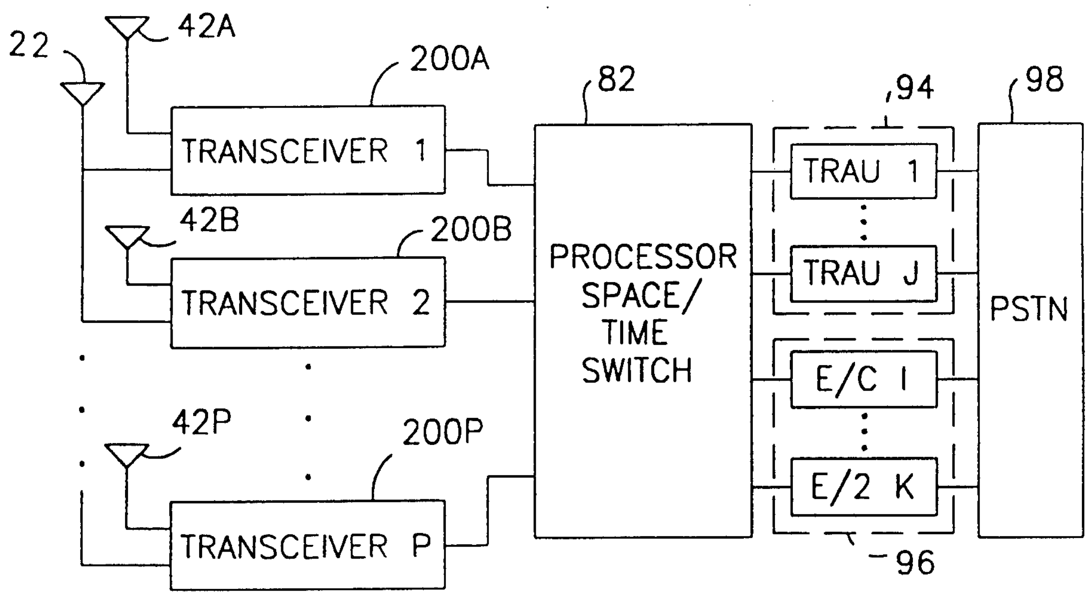

22
42A
200A
TRANSCEIVER 1
42B
200B
TRANSCEIVER 2
42P
200P
TRANSCEIVER P
82
PROCESSOR SPACE/ TIME SWITCH
94
TRAU 1
TRAU J
E/C I
E/2 K
96
98
PSTN

FIG. 13

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/05944

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q7/30 H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04B H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 590 412 (SIEMENS) 6 April 1994 see claims 1-25 ---	1-21
X	EP,A,0 439 926 (ATT) 7 August 1991 see claims 1-9; figure 3 ---	1-21
X	EP,A,0 497 083 (ERICSSON) 5 August 1992 see claim 1; figure 3 -----	1-21

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
6 September 1996	20.09.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bischof, J-L

INTERNATIONAL SEARCH REPORT

.ormation on patent family members

Interr nal Application No
PCT/US 96/05944

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-590412	06-04-94	DE-A- 4232480	31-03-94
		DE-A- 4238410	19-05-94
		FI-A- 934235	29-03-94
		NO-A- 933457	29-03-94
EP-A-439926	07-08-91	US-A- 5084869	28-01-92
		AU-B- 621011	27-02-92
		AU-B- 6929691	01-08-91
		CA-A- 2029615	01-08-91
		DE-D- 69023114	23-11-95
		DE-T- 69023114	18-04-96
		ES-T- 2078322	16-12-95
		JP-A- 7059143	03-03-95
EP-A-497083	05-08-92	SE-B- 467856	21-09-92
		AU-B- 7443194	08-12-94
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		CN-A- 1110458	18-10-95
		EP-A- 0656734	07-06-95
		SE-A- 9100309	01-08-92
		WO-A- 9214344	20-08-92
		SE-B- 467855	21-09-92
		SE-A- 9103095	01-08-92
		US-A- 5436900	25-07-95