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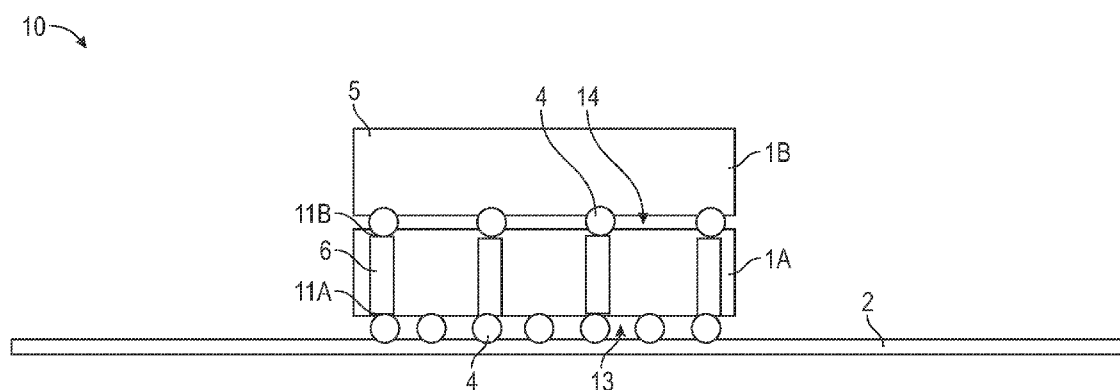


FIG. 2

(57) Abstract: In one embodiment, an electronic assembly can include: a first electronic device package configured to be mounted on and electrically connected with a system substrate; a second electronic device package electrically connected to the system substrate; and an electrical pathway configured to extend from the system substrate through the first electronic device package and connected to an input terminal of the second electronic device package, the electrical pathway bypassing processing circuitry of the first electronic device package.

ELECTRONIC ASSEMBLY

BACKGROUND

Field of the Invention

[0001] The field relates to an electronic assembly and, in particular, to an assembly including a plurality of electronic device packages stacked on one another.

Description of the Related Art

[0002] Various electronic devices (*e.g.*, high power regulators), in order to achieve higher power and output performance, utilize a greater footprint on a substrate, for example, placing parts side-by-side. However, providing multiple devices side-by-side increases the lateral footprint of the system board. Accordingly, there is a continuing need for improved electronic assemblies.

SUMMARY

[0003] In one embodiment, an electronic assembly can include: a first electronic device package configured to be mounted on and electrically connected with a system substrate; a second electronic device package electrically connected to the system substrate; and an electrical pathway configured to extend from the system substrate through the first electronic device package and connected to an input terminal of the second electronic device package, the electrical pathway bypassing processing circuitry of the first electronic device package.

[0004] In some embodiments, the first electronic device package comprises a first electronic component and a first molding compound in which the first electronic component is at least partially embedded. In some embodiments the second electronic device package is stacked on the first electronic device package. In some embodiments, the first electronic device package includes a first plurality of electrical contacts on a first side of the first electronic device package and a second plurality of electrical contacts on a second side of the first electronic device package that is opposite the first side, the second electrical device package electrically mounted on the second side of the first electronic device package and electrically connected to the second plurality of electrical contacts by way of a plurality of electrical interconnects. In some embodiments, the second plurality of electrical contacts are disposed in a plurality of divots recessed in the first molding compound. In some embodiments, the

second plurality of electrical contacts includes fewer electrically active electrical contacts than the first plurality of electrical contacts. In some embodiments, the first electronic device package comprises a first vertical interconnect extending through the first molding compound, the first vertical interconnect to electrically connect the system substrate with the second electronic device package. In some embodiments, the first electronic device package comprises a first package substrate, the first vertical interconnect connected to the first package substrate, the first package substrate electrically connected to the system board by way of one or more electrical interconnects. In some embodiments, the second electronic device package comprises a second electronic component and a second molding compound in which the second electronic device is at least partially embedded. In some embodiments, the first electronic device package is mounted on a first surface of the system substrate, and wherein the second electronic device package is mounted on a second surface of the system substrate that is opposite the first surface. In some embodiments, the first electronic device package includes a first voltage regulator and the second electronic device package includes a second voltage regulator, the second electronic device package having a first input port at a first voltage, a first output port at a second voltage, the first electronic device package having a second input port connected to the first output port and a second output port configured to output a third voltage. In some embodiments, at least one of the first and second electronic device packages further includes a ground port connected to electrical ground. In some embodiments, the second voltage is greater than the third voltage, and wherein the first voltage is greater than the second voltage. In some embodiments, the electronic assembly can include a first via at least partially through the first electronic device package to connect the system substrate to the first input port of the second electronic device package and a second via at least partially through the first electronic device package to connect the first output port to the second input port. In some embodiments, the first electronic device package comprises a digital power system management package and the second electronic device package comprises a voltage regulator. In some embodiments, the second electronic device package is configured to electrically connect to the system substrate in electrical parallel with the first electronic device package. In some embodiments, the second electronic device package is configured to electrically connect to the system substrate in series with the first electronic device package.

[0005] In another embodiment, an electronic assembly can include: a first electronic device package configured to be mounted on and electrically connected to a system substrate, a first via extending at least partially through the first electronic device package; and a second electronic device package mounted on the first electronic device package and configured to be electrically connected to the system substrate at least through the first via.

[0006] In some embodiments, the first via bypasses processing circuitry in the first electronic device package. In some embodiments, the first electronic device package comprises a first electronic component mounted to a first package substrate and a first molding compound in which the first electronic component is at least partially embedded, the first via extending through the first molding compound. In some embodiments, the first electronic device package includes a first voltage regulator and the second electronic device package includes a second voltage regulator, the second electronic device package having a first input port at a first voltage, a first output port at a second voltage, the first electronic device package having a second input port connected to the first output port and a second output port configured to output a third voltage, wherein the second voltage is greater than the third voltage, and wherein the first voltage is greater than the second voltage.

[0007] In another embodiment, a method of manufacturing an electronic assembly is disclosed. The method can include: mounting and electrically connecting a first electronic device package to a system substrate; mounting a second electronic device package electrically to the first electronic device package; and providing an electrical pathway from the system substrate through the first electronic device package and connecting to an input terminal of the second electronic device package, the electrical pathway bypassing processing circuitry of the first electronic device package.

[0008] In some embodiments, the method can include mounting a first electronic component to a first package substrate and at least partially embedding the first electronic component in a first molding compound, the electrical pathway including a first via extending through the first molding compound.

[0009] In another embodiment, a method of manufacturing an electronic assembly can include: mounting and electrically connecting a first electronic device package to a system substrate; and electrically connecting a second electronic device package to the system substrate in parallel with the first electronic device package.

[0010] In some embodiments, the method can include mounting the second electronic device package to the first electronic device package, wherein electrically connecting the second electronic device package to the system substrate comprises providing a via through the first electronic device package to electrically connect the second electronic device package and the system substrate. In some embodiments, the method can include mounting the second electronic device package to a side of the system substrate opposite to the first electronic device package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Embodiments of this disclosure will now be described, by way of non-limiting example, with reference to the accompanying drawings.

[0012] Figure 1A is a schematic side view of an electronic assembly that incorporates multiple electronic device packages mounted side-by-side on a system substrate.

[0013] Figure 1B is a schematic side view of electronic assembly that includes taller components to accommodate higher electrical power.

[0014] Figure 2 is a schematic side sectional view of an electronic assembly, according to various embodiments.

[0015] Figure 3A is a bottom plan view of an electronic device package having a first plurality of contacts on a bottom side of the package.

[0016] Figure 3B is a top plan view of an electronic device package having a second plurality of contacts on a top side of the package.

[0017] Figure 3C is a schematic perspective view of an electronic assembly comprising two stacked electronic device packages.

[0018] Figure 3D is a schematic perspective view of an electronic assembly comprising three stacked electronic device packages.

[0019] Figure 4 is a schematic side sectional view of an electronic assembly, according to various embodiments.

[0020] Figure 5A is a schematic side sectional view of a molded packaging assembly in a multistage arrangement.

[0021] Figure 5B is a schematic side sectional view of an electronic assembly according to various embodiments.

[0022] Figure 6A is a schematic perspective view of an electronic assembly comprising first and second voltage regulators.

[0023] Figure 6B is a schematic side view of the assembly of Figure 6A.

[0024] Figure 6C is a schematic side view of assembly voltage regulator according to various embodiments.

[0025] Figure 6D is an schematic view of an electronic assembly including the voltage regulator of Figure 6C.

[0026] Figure 7A is a schematic perspective view of an electronic assembly comprising three stacked electronic packages including a voltage regulator package stacked on two quad channel packages.

[0027] Figure 7B is a schematic perspective view of an electronic assembly comprising a voltage regulator package stacked on a power system management (PSM) package.

[0028] Figures 8A-8B are schematic side sectional views of a portion of an electronic assembly including recessed electrical contacts recessed in a divot formed in a molding compound.

[0029] Figures 9-10 are charts comparing the performance of electronic assemblies disclosed herein to conventional assemblies.

DETAILED DESCRIPTION

[0030] Electronic assemblies include devices that generate a significant amount of power. The generated power can result in a high level of heat which can be dissipated in a variety of ways. Moreover, it is important to provide the electronic assembly with a footprint (*e.g.*, on a substrate) that is compact. Figure 1A is a schematic side view of a conventional electronic assembly 100 in which an electronic device package 101 is mounted to a system substrate 102 by way of a plurality of electrical interconnects 104 (*e.g.*, solder balls). In various examples, the electronic device package 101 can comprise a voltage regulator. For high power applications, additional circuitry and components may be used in order to increase the output current. In Figure 1A, increased power (and current) output can be provided by providing multiple (*e.g.*, two or more) electronic device packages side-by-side on a system substrate 102 in an electronic assembly 100A. However, the use of multiple packages side-by-side on the

substrate 102 increases the footprint of the assembly 100A, which takes up valuable board space.

[0031] Figure 1B is a schematic side view of electronic assembly 100B, 100C that includes taller components to accommodate higher electrical power. Unlike Figure 1A, in order to provide increased power (and output current), the additional circuitry and other components may be provided by way of taller components in a package 100B. In some arrangements, increased power can be accommodated by mounting a component 103 (such as an inductor) on the package 101. However, the use of taller components or packages can increase the heat flux in the assemblies 100B, 100C, which may create challenging thermal management issues. Further, although taller components may increase output current and power, if additional output current is desired, then additional parts would be included side-by-side, increasing the lateral footprint of the device.

[0032] Accordingly, there remains a continuing need for compact electronic assemblies that facilitate high power and/or high current applications without creating excessive heat flux. Figure 2 is a schematic side sectional view of an electronic assembly 10, according to various embodiments. The electronic assembly 10 (which can include packages 1A, 1B) can be mounted to a system substrate 2. The system substrate 2 can serve as a system board (*e.g.*, motherboard) and can comprise any suitable type of substrate. For example, in the illustrated embodiment, the system substrate 2 can include a laminate substrate, such as a printed circuit board (PCB).

[0033] The electrical assembly 10 can include a first electronic device package 1A mounted on and electrically connected with the system substrate 2. As explained herein in Figures 5A-5B, the first electronic device package 1A can comprise one or a plurality of electronic devices 8 mounted to a package substrate 7. The electronic device(s) 8 can comprise active integrated device die(s) (*e.g.*, die(s) with one or more transistors) or passive components, such as capacitors, inductors, transformers, etc. The electronic device(s) 8 can be at least partially embedded in a molding compound 5, which can comprise an organic protective coating, such as an epoxy. As shown in Figure 2, the first electronic device package 1A can comprise one or a plurality of vertical interconnects (*e.g.*, vias 6) that extend at least partially through the package 1A. In the illustrated embodiment, the vias 6 comprise through mold vias (TMVs) that extend through the molding compound 5. As explained herein in Figures 5A-5B,

in some embodiments, the vias 6 can be connected to the package substrate 7, which can electrically connect to the interconnects 4 (*e.g.*, solder balls).

[0034] The electronic assembly 10 can comprise a second electronic device package 1B electrically connected to the system substrate 2 in parallel (or in series) with the first electronic device package 1A. The second electronic device package 1B can comprise at least a second electronic device 8 (*e.g.*, integrated device die(s), passive component(s), etc.) and a second molding compound 5 in which the second electronic device 8 is at least partially embedded. In some embodiments, the first and second electronic device packages 1A, 1B can comprise the same type of device package (and, for example, in some embodiments, may comprise substantially similar or identical packages). In other embodiments, the first and second electronic device packages 1A, 1B can comprise different types of packages. As shown in the embodiment of Figure 2, the second electronic device package 1B can be stacked on and electrically connected to the first electronic device package 1A. The first electronic device package 1A can include a first plurality of electrical contacts 11A on a first bottom side 13 of the first electronic device package 1A and a second plurality of electrical contacts 11B on a second top side 14 of the first electronic device package 1A that is opposite the first side 13. The first plurality of electrical contacts 11A on the first bottom side 13 of the first electronic device package 1A can be electrically connected to the system board 2 by way of a first plurality of electrical interconnects 4 (*e.g.*, solder balls). The second electronic device package 1B can be electrically mounted on the second top side 14 of the first electronic device package 1A and electrically connected to the second plurality of electrical contacts 11B by way of a second plurality of electrical interconnects 4 (*e.g.*, solder balls). In various embodiments, the packages 1A, 1B can be electrically connected using a ball grid array (BGA), a linear grid array (LGA), or any other suitable type of electrical connection arrangement.

[0035] In the embodiment of Figure 2, the second electronic device package 1B can be connected to the system substrate 2 in electrical parallel with the first electronic device package 1A. For example, the vias 6 can electrically connect to the system board 2 by way of the interconnects 4 (and, as shown in Figure 5B, by way of a package substrate 7) and can serve as pass-through vias such that electrical power and/or signals bypass the first electronic device package 1A and electrically connect to component(s) of the second device package 1B (*e.g.*, by way of a package substrate 7 in the second package 1B). Thus, in various

embodiments, an electrical pathway can be provided from the system substrate 2 through the first electronic device package 1A and connected to an input terminal of the second electronic device package 1B. The electrical pathway can bypass processing circuitry of the first electronic device package 1A in some embodiments. For example, the electrical pathway can bypass processing circuitry (*e.g.*, all processing circuitry in some embodiments) patterned or formed in one or more dies of the first package 1A.

[0036] Beneficially, due to the parallel connection of the second electronic device package 1B, the upper second package 1B can utilize fewer pins or connections than the lower first package 1A. As shown in Figure 2, the second plurality of electrical contacts 11B (which provide electrical communication with the upper second package 1B) can include fewer electrically active electrical contacts 11 than the first plurality of electrical contacts 11A (which electrically communicates with the system substrate 2). Accordingly, in some embodiments, the first electronic device package 1A can process or operate with a larger number of inputs (*e.g.*, through the larger first plurality of electrical contacts 11A) from the system substrate 2, and, in some embodiments, can serve as a control package for the assembly 10. The second electronic device package 1B can serve as a responder package, which can respond to control inputs from the system substrate 2 (by way of the vias 6) and/or from the first package 1A. As explained herein, providing the parallel electrical pathways can enable power sharing between the packages 1A, 1B, reduce the physical footprint of the assembly 10, and increases the power density for the assembly footprint.

[0037] In addition, the embodiment of Figure 2 can also beneficially allow for increases in output current and/or increases in input voltage. The use of stacked packages can save board space and reduce the footprint as compared to other packages. The thermal performance can also be improved by splitting the current amongst multiple packages in parallel, which can allow for increased current usage without significantly increasing power loss and, accordingly, without significantly increasing temperature. The use of different types of packages in the disclosed embodiments can also enable versatile electronic assembly designs.

[0038] Figure 3A is a bottom plan view of the first electronic device package 1A having a first plurality of contacts 11A on the first bottom side 13 of the package 1A. Figure 3B is a top plan view of the first electronic device package 1A having a second plurality of

contacts 11B on a second top side 14 of the package 1A. As explained above, at least due to the parallel connection to the system substrate 2 between the first and second packages 1A, 1B, the second plurality of contacts 11B on the top side 14 can include fewer electrically active contacts than the first plurality of contacts 11A on the bottom side 13. In other embodiments, however, additional contacts 11B or pins can be provided for ground and I/O connections, and/or to provide a thermal path for the upper package 1B to dissipate heat through the bottom package 1A. For example, providing additional pins or contacts 11B on the top side 14 of the lower package 1A may improve heat removal for the upper package 1B. The additional pins or contacts 11B for heat dissipation may be electrically inactive or disconnected, however, such that the top side 14 still includes fewer active electrical contacts 11B on the top side 14 than the first plurality of contacts 11A on the bottom side 13.

[0039] Figure 3C is a schematic perspective view of an electronic assembly 10 comprising two stacked electronic device packages 1A, 1B. Figure 3D is a schematic perspective view of an electronic assembly 10 comprising three stacked electronic device packages 1A, 1B, 1C. It should be appreciated that any suitable number of packages 1A-1C can be stacked on top of one another. In the illustrated embodiments, the first package 1A can comprise the controller package, and the second and third packages 1B, 1C can comprise responder packages controlled by another component through the system board 2 (*e.g.*, a substrate) and/or by the first package 1A. In other embodiments, the stacked packages 1A-1C can be digitally controlled or preprogrammed, and can share the output current (at the same voltage). A user can use a computer connected to the board 2 to turn any of the components (*e.g.*, components in the packages 1A-1C) on or off individually. In some embodiments, the second package 1B can connect to the third package 1C by way of electrical contacts having the same number of contacts as the second plurality of contacts 11B. Thus, in some embodiments, the second and third packages 1B, 1C can have fewer pins (*e.g.*, fewer inputs or contacts) than the first package 1A. The third package 11C can connect to the system substrate 2 in parallel with both the first and second packages 11A, 11B. For example, TMVs 6 can extend through the first package 1A and the second package 11B to serve as pass through vias to connect the third package 1C to the system board 2 while bypassing the first and second packages 1A, 1B. Although three packages 1A-1C are shown in Figure 3D, in other embodiments, more than three packages can be provided in the assembly 10.

[0040] Figure 4 is a schematic side sectional view of an electronic assembly 10A, according to various embodiments. Unless otherwise noted, the components of Figure 4 may be the same as or generally similar to like-numbered components of Figures 2-3D. As with the embodiments of Figures 2-3D, the first and second packages 1A, 1B are in electrical communication in parallel with the system board 2. Unlike the embodiments of Figures 2 and 3C-3D, in Figure 4, the first electronic device package 1A is mounted on a first surface 15 of the system substrate 2, and the second electronic device package 1B is mounted on a second surface 16 of the system substrate 2 that is opposite the first surface 15. Conductive traces (not shown) within the system substrate 2 can electrically route signals between the packages 1A, 1B, instead of utilizing the vias 6 to connect to the package 1B.

[0041] Figure 5A is a schematic side sectional view of a molded packaging assembly 1' in a multistage arrangement. In the arrangement of Figure 5A, a first stage 1A' can provide a first voltage regulation, *e.g.*, a downregulation of 100 V to 12 V in a first stage. The stepped down voltage from the first stage 1A' can be conveyed to a second stage 1B'. The second stage 1B' can provide a second voltage regulation, *e.g.*, a further downregulation of 12V to 1 V. Thus, the arrangement of Figure 5A includes a plurality (*e.g.*, two) of stages that are horizontally spaced from one another, which can increase the lateral footprint of the assembly 1'.

[0042] By contrast, Figure 5B is a schematic side sectional view of an electronic assembly 10B including stacked packages 1A, 1B according to various embodiments. The electronic assembly 10B and/or the packages 1A, 1B can be used in combination with any of the embodiments disclosed herein. As shown in Figure 5A, a package substrate 7 can be provided. The package substrate 7 can comprise any suitable type of packaging substrate, such as a laminate substrate (*e.g.*, a PCB), a ceramic substrate, a leadframe, etc. One or more components or devices 8 can be mounted and electrically connected to the package substrate 7. The one or more components 8 can comprise one or more of an integrated device die (*e.g.*, an active chip with one or more transistors), a passive electronic device (*e.g.*, a resistor, inductor, transformer, capacitor, etc.). The component(s) 8 can be flip chip mounted to the package substrate 7 in some embodiments. In other embodiments, the component(s) or devices 8 can be mounted and wire bonded to the package substrate 7. Vias 6 (*e.g.*, TMVs) can be connected to the package substrate 7. For example, in some embodiments, the vias 6 can be

picked-and-placed onto the substrate 7 and attached with a conductive adhesive (*e.g.*, solder). The component(s) 8 and vias 6 can be overmolded with molding compound 5.

[0043] In Figure 5B, the first package 1A can be mounted on and electrically connected to the system substrate 2. For example, the first plurality of electrical contacts 11A (which can be coupled to a bottom side of the package substrate 7) can be connected to corresponding contacts or pads on the system substrate 2 by way of interconnects, *e.g.*, solder balls or bumps. The second package 1B can be stacked on the first package 1A. The second plurality of contacts 11B (which can include fewer contacts than the first plurality of contacts 11A, as explained above and shown herein) can be connected to corresponding contacts or pads on the package substrate 7 of the second package 1B by way of interconnects 4. As shown, the vias 6 can serve as pass-through TMVs that electrically bypass the first package 1A such that the second package 1B connects to the system substrate 2 (by way of, *e.g.*, the package substrate 7 of the first package 1A) in series with the first package 1A. In some embodiments, as noted above, the TMVs can connect the first and second packages 1A, 1B in parallel.

[0044] As with the arrangement of Figure 5A, the embodiment of Figure 5B can serve to downregulate an input voltage. For example, the first package 1A can provide a first voltage regulation, *e.g.*, a downregulation of 100 V to 12 V in a first stage. The stepped down voltage from the first package 1A can be conveyed to the second package 1B. The second package 1B can provide a second voltage regulation, *e.g.*, a further downregulation of 12V to 1 V. Beneficially, unlike the arrangement of Figure 5A, in Figure 5B, the stacked packages 1A, 1B can provide effective voltage downregulation but in a smaller lateral footprint without increasing power loss.

[0045] Figure 6A is a schematic perspective view of an electronic assembly 10C comprising first and second voltage regulator packages 1A, 1B. Figure 6B is a schematic side view of the assembly 10C of Figure 6A. Unless otherwise noted, the components of Figures 6A-6D may include components generally similar to or the same as like-numbered components of Figures 2-5B. In Figures 6A-6B, the first and second packages 1A, 1B comprise respective voltage regulator packages. For example, as shown, the first package 1A can comprise a low voltage regulator, and the second package 1B can comprise a high voltage regulator. The second electronic device package 1B can have a first input port 9A at a first voltage V1 and a

first output port 9B at a second voltage V2. The first electronic device package 1A can have a second input port 9C connected to the first output port 9B and a second output port 9D configured to output a third voltage V3. In the illustrated embodiment, the second voltage V2 is greater than the third voltage V3, and the first voltage V1 is greater than the second voltage V2. Thus, in Figure 6A, the first input port 9A can bypass circuitry in the lower first package 1A to connect to the upper second package 1B, which can reduce the first voltage V1 to the second voltage V2. The first output port 9B can electrically connect to the second input port 9C of the lower first package 9A, which can further reduce the second voltage V2 to the lower third voltage V3, which can be provided to the substrate 2 and another electronic device by way of the second output port 9D.

[0046] Figure 6C is a schematic side view of the lower first package 9A which includes multiple output ports 9D, 9E, 9F, 9G (*e.g.*, a quad channel output). Figure 6D is an electrical schematic of an electronic assembly 10D that includes the quad channel output package 9A of Figure 6C. In the conventional regulator 100D shown in Figure 6C, the regulator 100D accepts a low voltage input (*e.g.*, 6 Vin) and outputs a quad channel output, *e.g.*, in which multiple (*e.g.*, four) voltage outputs 9D-9G are provided from the lower first package 1A. Thus, the lower first package 1A can be limited to relatively low voltage inputs, for example 5V in one application, while the upper second package 1B can accept larger voltages (*e.g.*, 60V in one application). Beneficially, in the embodiment of Figures 6C-6D, the first input port 9A of the second package 1B can connect to the system substrate 2 and can bypass the first package 1A by way of a first TMV 6 (see Figures 5B and 6B) through the molding compound 5 of the first package 1A. The first input port 9A can comprise a high voltage (HV) input (*e.g.*, 60 V or higher). The component(s) or device(s) 8 of the second package 1B can comprise circuitry configured to reduce the voltage to a lower voltage (*e.g.*, 5V or 6V) at the first output 9B, which can connect to the second input 9C to provide a lower voltage input to the lower first package 1A, by way of a second TMV 6 (see Figures 5B and 6B) through the molding compound 5 of the first package 1A. As shown in the embodiment of Figure 6B, at least one TMV 6 can also provide a connection to ground (GND) terminal of the system substrate 2. The lower package 1B can output the lower third voltage V3 (see Figure 6A) or a quad out channel (Figure 6D). In the embodiment of Figure 6D, for example, the lower package 1A can lower the voltage V2 provided to the second input terminal 9C to a

plurality of lower voltages that are to output to the substrate 2 by way of multiple output channels 9D-9G. Beneficially, the embodiments of Figures 6A-6D can operate at higher power and a reduced package footprint.

[0047] The embodiments disclosed herein can include assemblies in which the packages 1A, 1B are different but which are pin compatible. In other embodiments, the package 1A, 1B can be the same or similar (*e.g.*, identical or substantially the same type of package). In some embodiments, such as those shown in Figures 7A-7B, the assemblies 10D, 10E can include at least two different types of packages configured for different functionalities or operations. For example, Figure 7A is a schematic perspective view of an electronic assembly 10D comprising three stacked electronic packages 1A-1C including a voltage regulator package 1C stacked on two quad channel packages 1A. It should be appreciated that any suitable number of packages (*e.g.*, two, three, four, five, or more than five) can be stacked on one another. Figure 7B is a schematic perspective view of an electronic assembly comprising a voltage regulator package (*e.g.*, a high voltage (HV) package module) stacked on a power system management (PSM) package. Skilled artisans would understand that any suitable types of packages can be used in connection with the embodiments disclosed herein.

[0048] Figures 8A-8B are schematic side sectional views of a portion of an electronic assembly 10F including recessed electrical contacts 11 recessed in a divot 12 formed in the molding compound 5. The divot 12 can be formed in any suitable manner. For example, the divot 12 can be formed by drilling, laser ablation, or a suitably-designed top mold chase. The divot 12 can serve to recess the contacts 11 below the top side 14 of the first package 1A and can help align the pins of the second package 1B to the contacts 11 of the first package 1A. The recessed divot 12 can further serve to lock the interconnects 4 in place. In addition, the divot 12 can provide electrical isolation between the contacts 11 and a heat sink if a heat sink is used over the package 1A. In other embodiments, however, the electronic assembly can utilize an LGA package for mounting and without the use of the divot 12.

[0049] Figures 9-10 are charts comparing the performance of electronic assemblies disclosed herein to conventional assemblies. Figure 9 is a chart plotting the integrated circuit (IC) temperature versus load (A) for a two-stack module 1Vout according to various embodiments disclosed herein and for a conventional module (single module 1Vout), with a 12 Vin input. Figure 10 is a chart plotting the integrated circuit (IC) temperature versus load

(A) for a two-stack module 1.8 Vout according to various embodiments disclosed herein and for a conventional module (single module 1.8 Vout), with a 12 Vin input. As shown in Figures 9 and 10, the two-stack module (for either 1 Vout or 1.8 Vout) can utilize substantially larger currents without significantly increasing the temperature.

[0050] When it comes to power solutions, customers look for the optimal performance in a small footprint. If existing parts are incapable to meeting the output requirements, multiple parts can be put side by side (current sharing) to meet the requirement. By compromising footprint criteria, output performance can be improved. The embodiments disclosed herein reduce lateral footprint by stacking multiple packages or modules together.

[0051] The disclosed embodiments of stacking packages or uModules takes advantage of the under-utilized vertical space above the assembly to achieve an improve in output performance without increasing the footprint. To do this, the assembly utilizes pins on both the bottom side and top side as well to enable paralleling. Stacking multiple packages can increase output current up to 50% while maintaining the same thermal performance. This idea is based on the fact that conduction loss ($P = I^2 \times R$) is exponentially dependent on the current. Depending on the output configuration, stacking multiple packages can enable 100% increase capability in output current (compare to one package). Stacking multiple packages allows customers to upgrade the assembly without a major board design layout change. The ability for a quick upgrade is advantageous. In order to bring the pins up from the substrate to the top side of a package, as explained here, copper pillars or other packaging technology can be utilized.

[0052] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” “include,” “including” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word “connected”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Moreover, as used

herein, when a first element is described as being “on” or “over” a second element, the first element may be directly on or over the second element, such that the first and second elements directly contact, or the first element may be indirectly on or over the second element such that one or more elements intervene between the first and second elements. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. Regarding the word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0053] Moreover, conditional language used herein, such as, among others, “can,” “could,” “might,” “may,” “e.g.,” “for example,” “such as” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments.

[0054] Although disclosed in the context of certain embodiments and examples, it will be understood by those skilled in the art that the present invention extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses and obvious modifications and equivalents thereof. Further, unless otherwise noted, the components of an illustration may be the same as or generally similar to like-numbered components of one or more different illustrations. In addition, while several variations have been shown and described in detail, other modifications, which are within the scope of this disclosure, will be readily apparent to those of skill in the art based upon this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with, or substituted for, one another in order to form varying modes of the disclosed invention. Thus, it is intended that the scope of the present invention herein disclosed should not be limited by the particular disclosed embodiments described above, but should be determined only by a fair reading of the aspects that follow.

WHAT IS CLAIMED IS:

1. An electronic assembly comprising:
a first electronic device package configured to be mounted on and electrically connected with a system substrate;
a second electronic device package electrically connected to the system substrate; and
an electrical pathway configured to extend from the system substrate through the first electronic device package and connected to an input terminal of the second electronic device package, the electrical pathway bypassing processing circuitry of the first electronic device package.
2. The electronic assembly of Claim 1, wherein the first electronic device package comprises a first electronic component and a first molding compound in which the first electronic component is at least partially embedded.
3. The electronic assembly of Claim 2, wherein the second electronic device package is stacked on the first electronic device package.
4. The electronic assembly of Claim 3, wherein the first electronic device package includes a first plurality of electrical contacts on a first side of the first electronic device package and a second plurality of electrical contacts on a second side of the first electronic device package that is opposite the first side, the second electronic device package electrically mounted on the second side of the first electronic device package and electrically connected to the second plurality of electrical contacts by way of a plurality of electrical interconnects.
5. The electronic assembly of Claim 4, wherein the second plurality of electrical contacts are disposed in a plurality of divots recessed in the first molding compound.
6. The electronic assembly of Claim 4, wherein the second plurality of electrical contacts includes fewer electrically active electrical contacts than the first plurality of electrical contacts.
7. The electronic assembly of Claim 3, wherein the first electronic device package comprises a first vertical interconnect extending through the first molding compound, the first vertical interconnect to electrically connect the system substrate with the second electronic device package.

8. The electronic assembly of Claim 7, wherein the first electronic device package comprises a first package substrate, the first vertical interconnect connected to the first package substrate, the first package substrate electrically connected to the system board by way of one or more electrical interconnects.

9. The electronic assembly of Claim 7, wherein the second electronic device package comprises a second electronic component and a second molding compound in which the second electronic device is at least partially embedded.

10. The electronic assembly of Claim 1, wherein the first electronic device package is mounted on a first surface of the system substrate, and wherein the second electronic device package is mounted on a second surface of the system substrate that is opposite the first surface.

11. The electronic assembly of Claim 1, wherein the first electronic device package includes a first voltage regulator and the second electronic device package includes a second voltage regulator, the second electronic device package having a first input port at a first voltage, a first output port at a second voltage, the first electronic device package having a second input port connected to the first output port and a second output port configured to output a third voltage.

12. The electronic assembly of Claim 11, wherein at least one of the first and second electronic device packages further includes a ground port connected to electrical ground.

13. The electronic assembly of Claim 11, wherein the second voltage is greater than the third voltage, and wherein the first voltage is greater than the second voltage.

14. The electronic assembly of Claim 11, further comprising a first via at least partially through the first electronic device package to connect the system substrate to the first input port of the second electronic device package and a second via at least partially through the first electronic device package to connect the first output port to the second input port.

15. The electronic assembly of Claim 1, wherein the first electronic device package comprises a digital power system management package and the second electronic device package comprises a voltage regulator.

16. The electronic assembly of Claim 1, wherein the second electronic device package is configured to electrically connect to the system substrate in electrical parallel with the first electronic device package.

17. The electronic assembly of Claim 1, wherein the second electronic device package is configured to electrically connect to the system substrate in series with the first electronic device package.

18. An electronic assembly comprising:

a first electronic device package configured to be mounted on and electrically connected to a system substrate, a first via extending at least partially through the first electronic device package; and

a second electronic device package mounted on the first electronic device package and configured to be electrically connected to the system substrate at least through the first via.

19. The electronic assembly of Claim 18, wherein the first via bypasses processing circuitry in the first electronic device package.

20. The electronic assembly of Claim 18, wherein the first electronic device package comprises a first electronic component mounted to a first package substrate and a first molding compound in which the first electronic component is at least partially embedded, the first via extending through the first molding compound.

21. The electronic assembly of Claim 20, wherein the first electronic device package includes a first voltage regulator and the second electronic device package includes a second voltage regulator, the second electronic device package having a first input port at a first voltage, a first output port at a second voltage, the first electronic device package having a second input port connected to the first output port and a second output port configured to output a third voltage, wherein the second voltage is greater than the third voltage, and wherein the first voltage is greater than the second voltage.

22. A method of manufacturing an electronic assembly, the method comprising:

mounting and electrically connecting a first electronic device package to a system substrate;

mounting a second electronic device package electrically to the first electronic device package; and

providing an electrical pathway from the system substrate through the first electronic device package and connecting to an input terminal of the second electronic

device package, the electrical pathway bypassing processing circuitry of the first electronic device package.

23. The method of Claim 22, further comprising mounting a first electronic component to a first package substrate and at least partially embedding the first electronic component in a first molding compound, the electrical pathway including a first via extending through the first molding compound.

24. A method of manufacturing an electronic assembly, the method comprising:
mounting and electrically connecting a first electronic device package to a system substrate; and

electrically connecting a second electronic device package to the system substrate in parallel with the first electronic device package.

25. The method of Claim 24, further comprising mounting the second electronic device package to the first electronic device package, wherein electrically connecting the second electronic device package to the system substrate comprises providing a via through the first electronic device package to electrically connect the second electronic device package and the system substrate.

26. The method of Claim 24, further comprising mounting the second electronic device package to a side of the system substrate opposite to the first electronic device package.

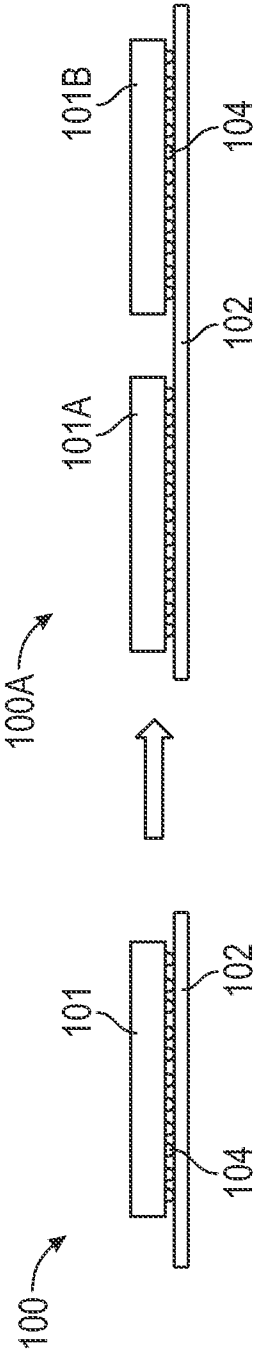


FIG. 1A

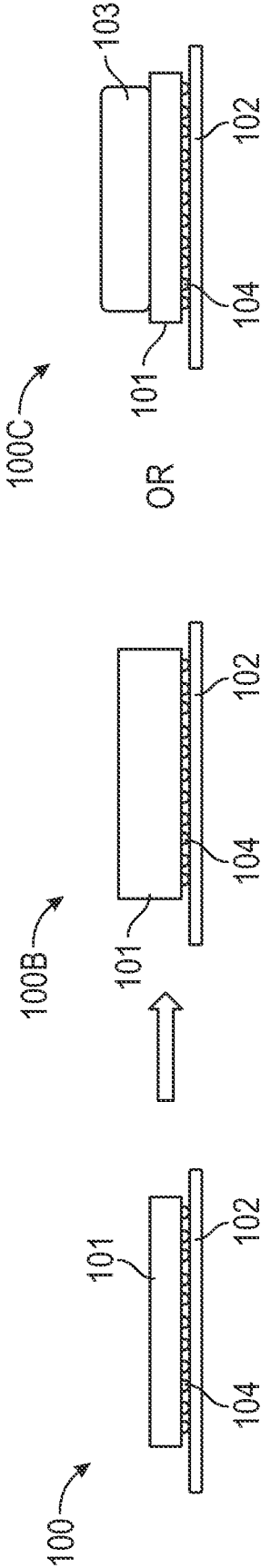
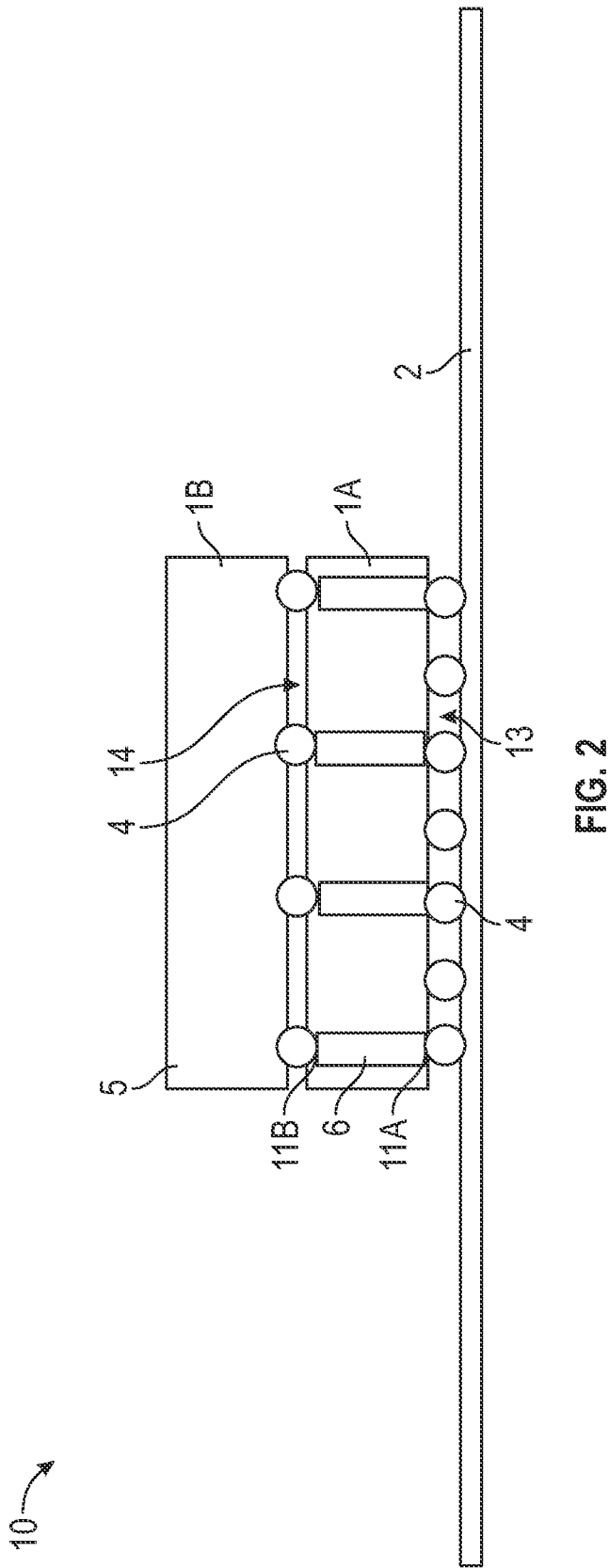


FIG. 1B



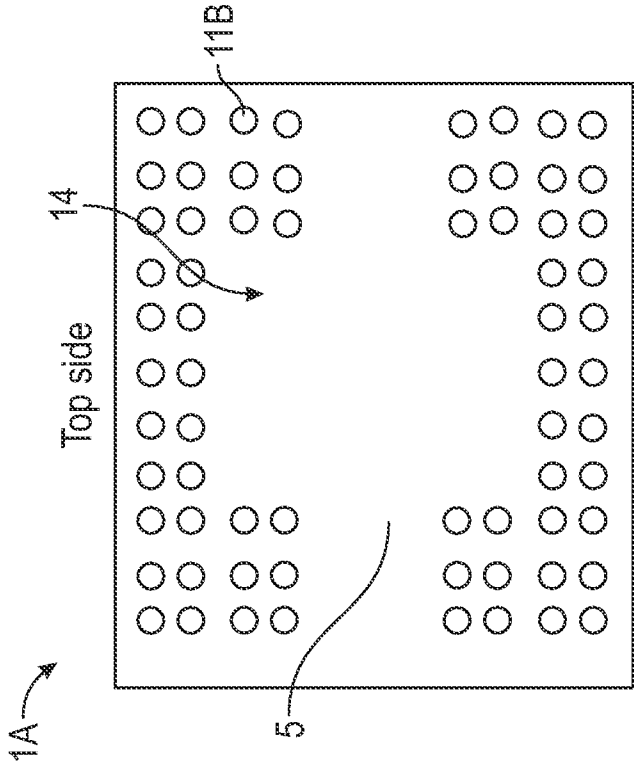


FIG. 3A

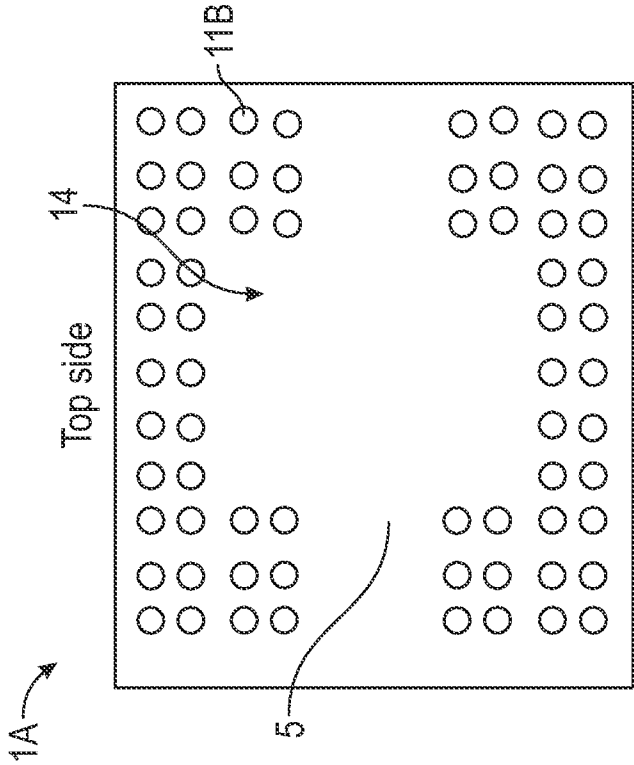


FIG. 3B

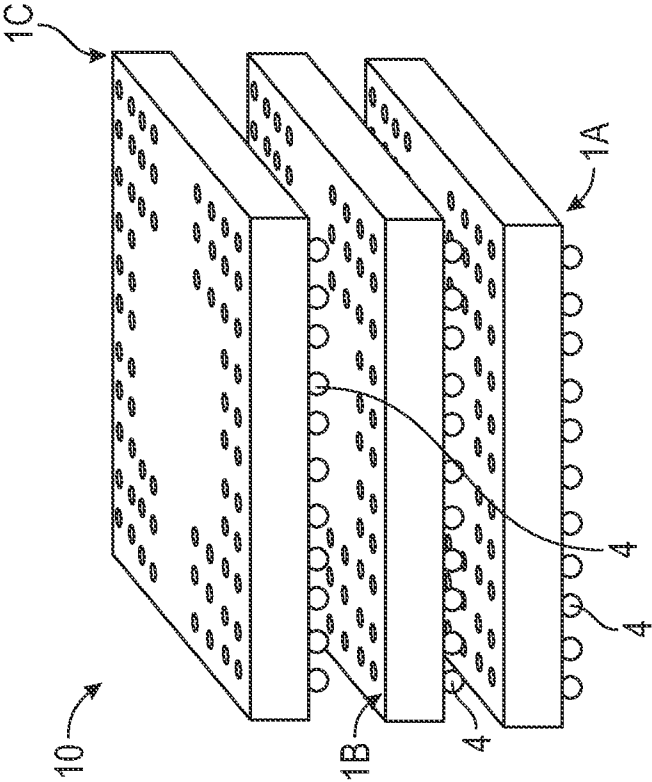


FIG. 3D

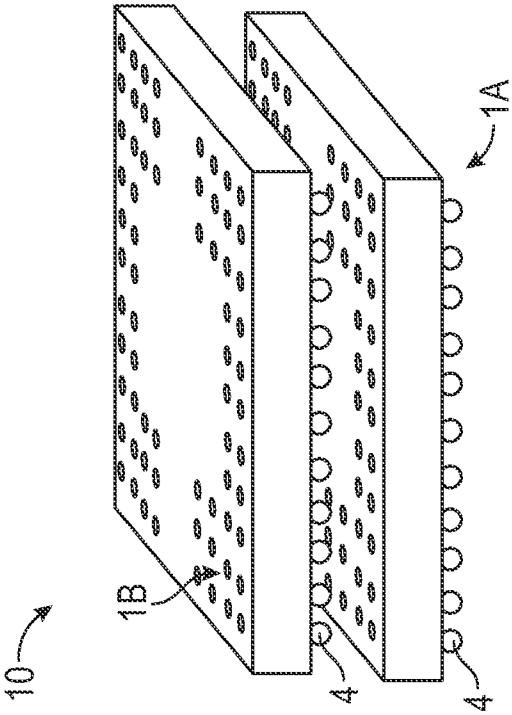


FIG. 3C

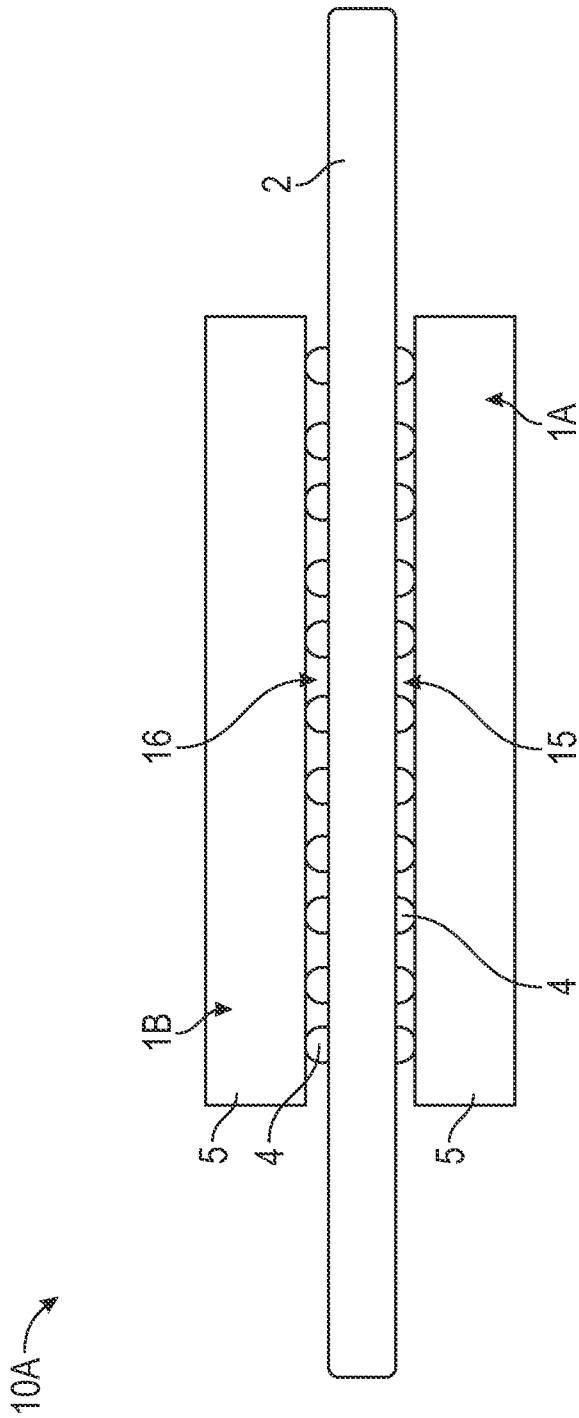


FIG. 4

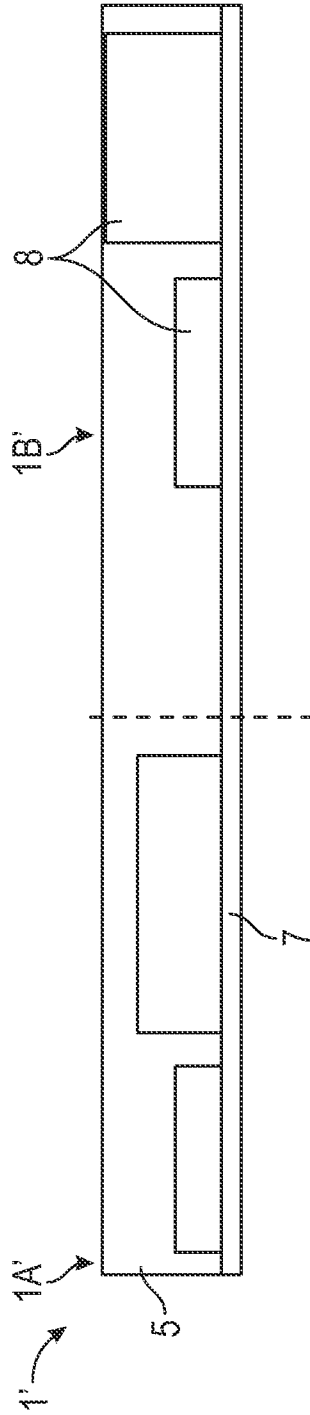
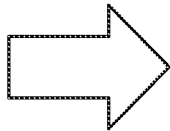


FIG. 5A



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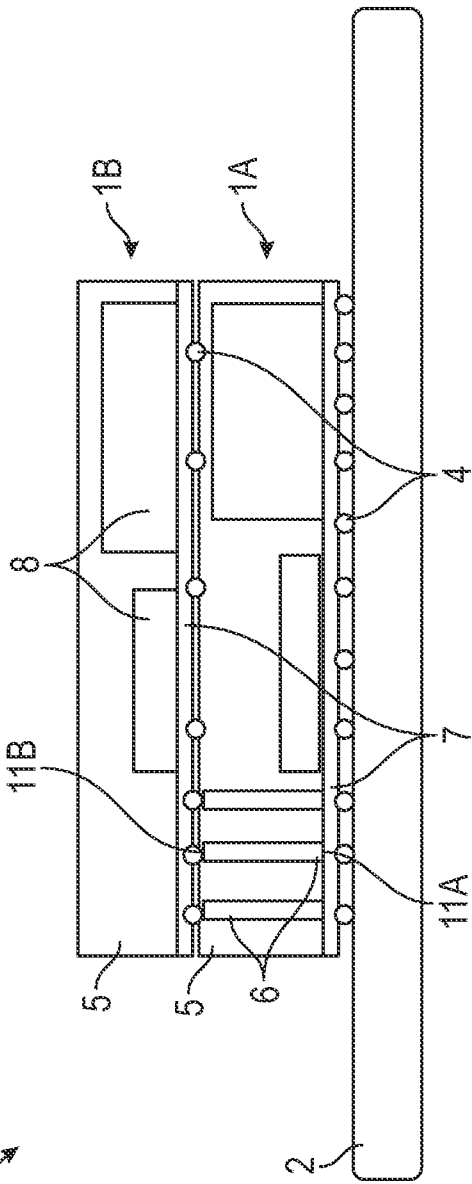
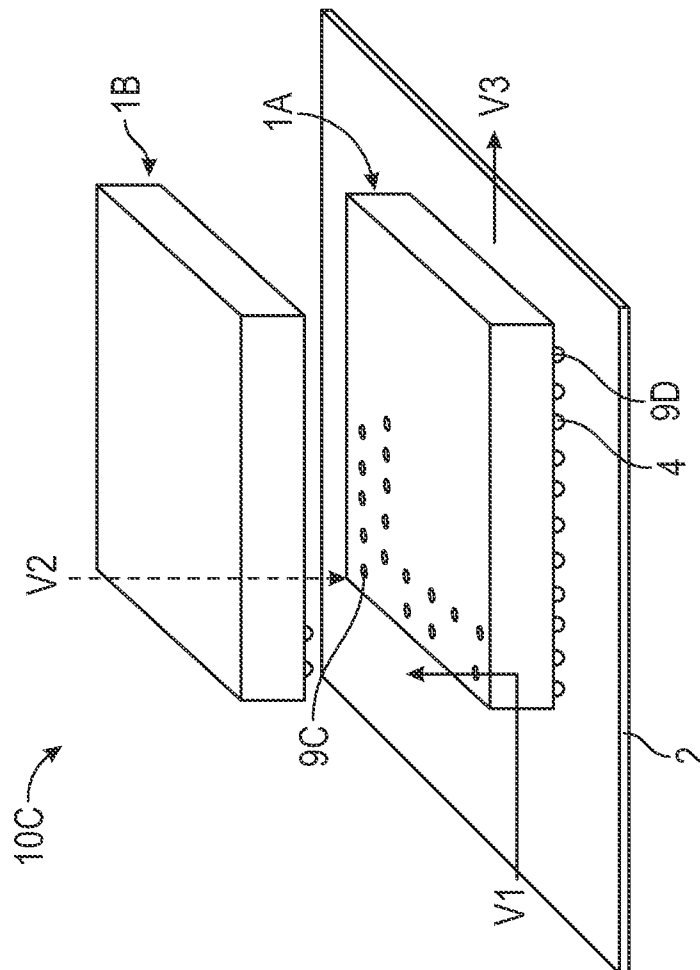
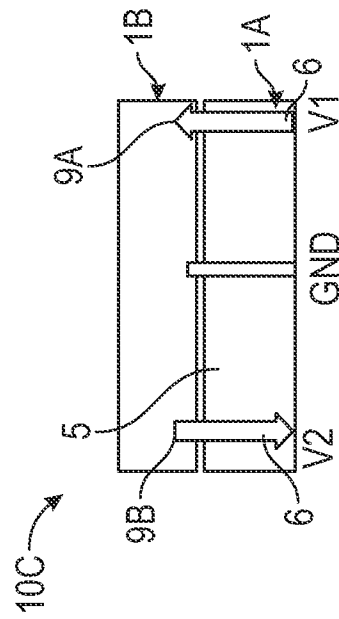


FIG. 5B

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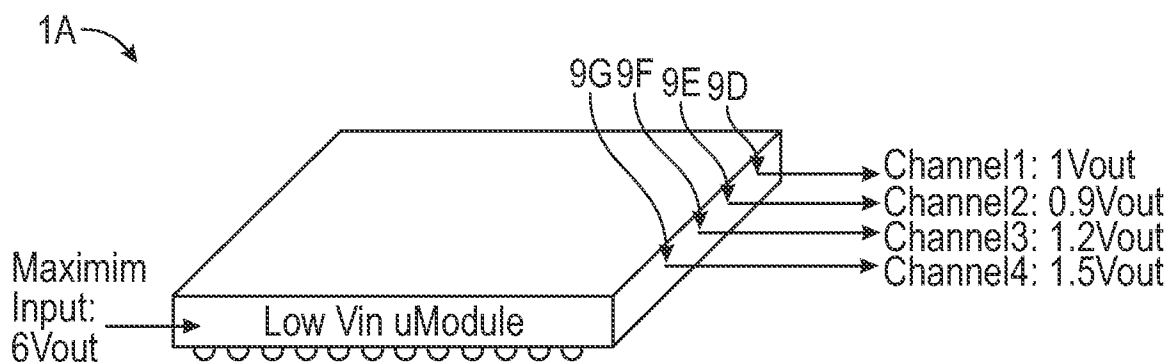


FIG. 6C

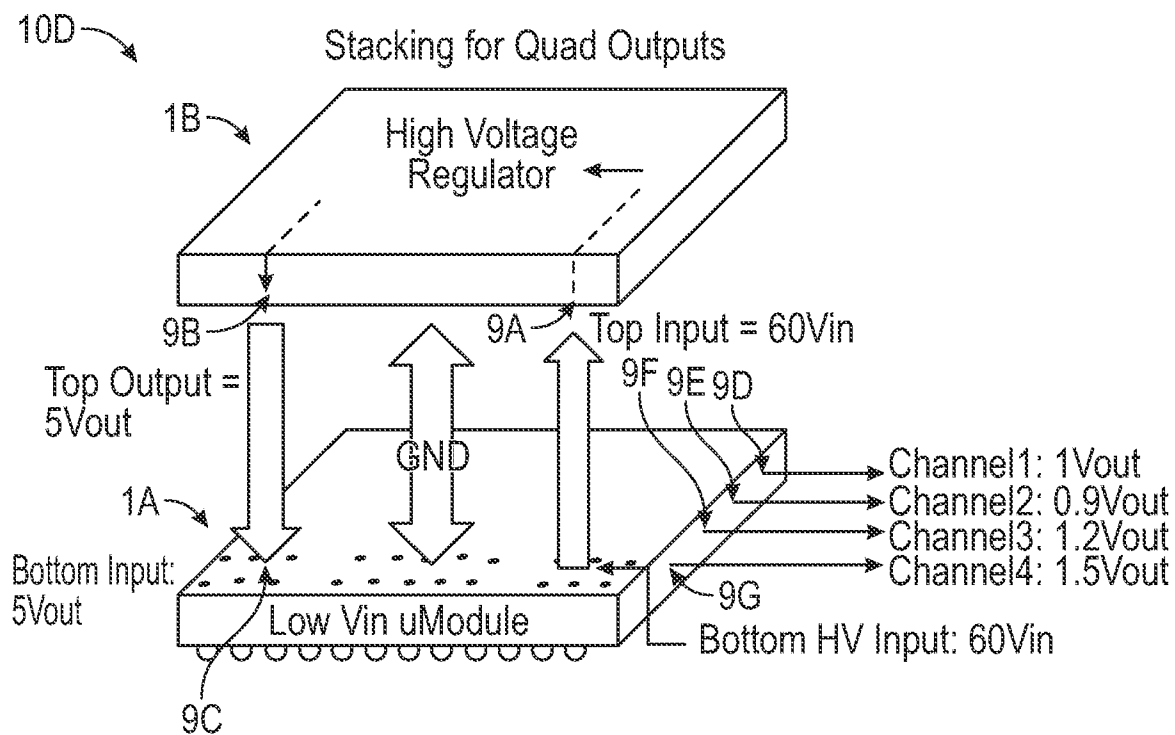


FIG. 6D

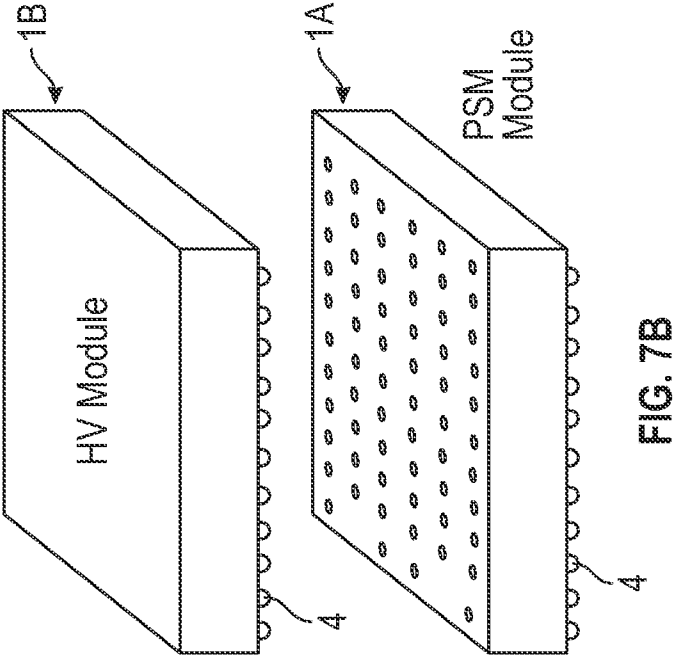
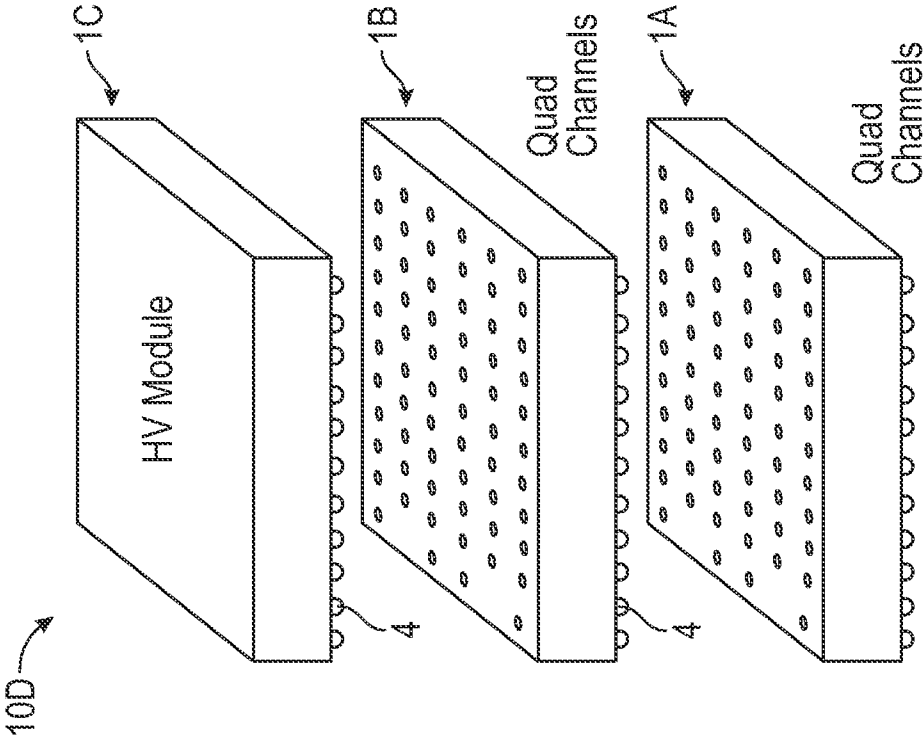


FIG. 7A

FIG. 7B

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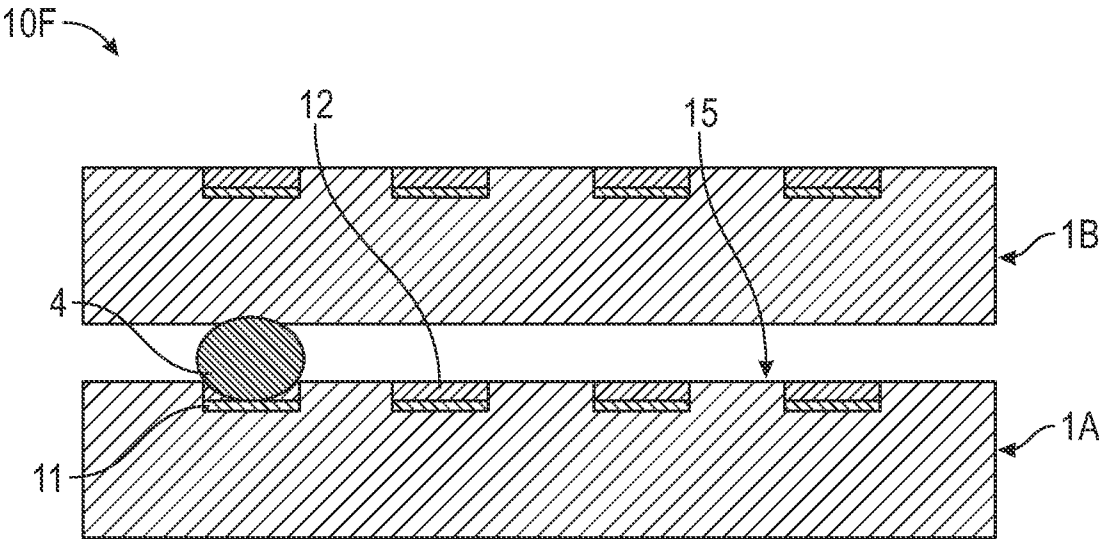


FIG. 8A

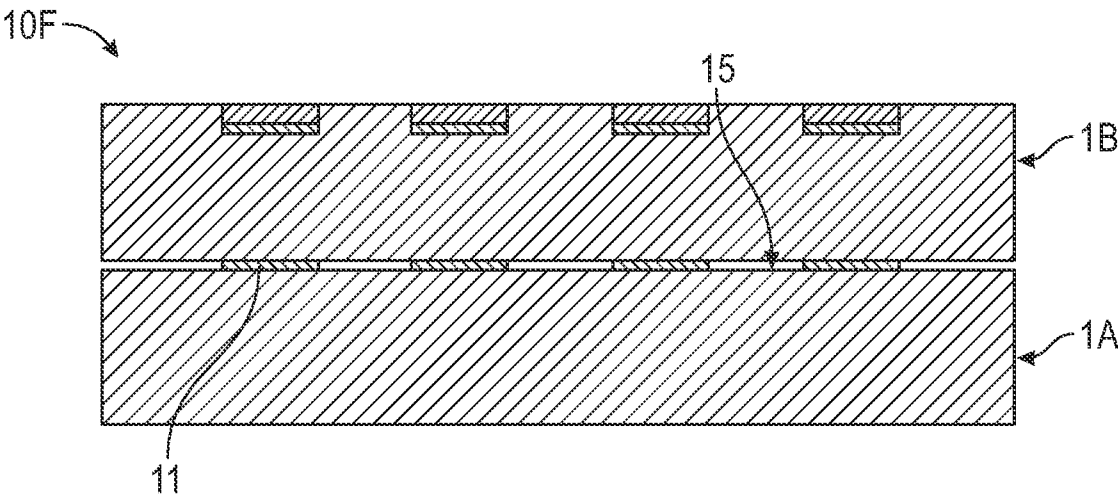


FIG. 8B

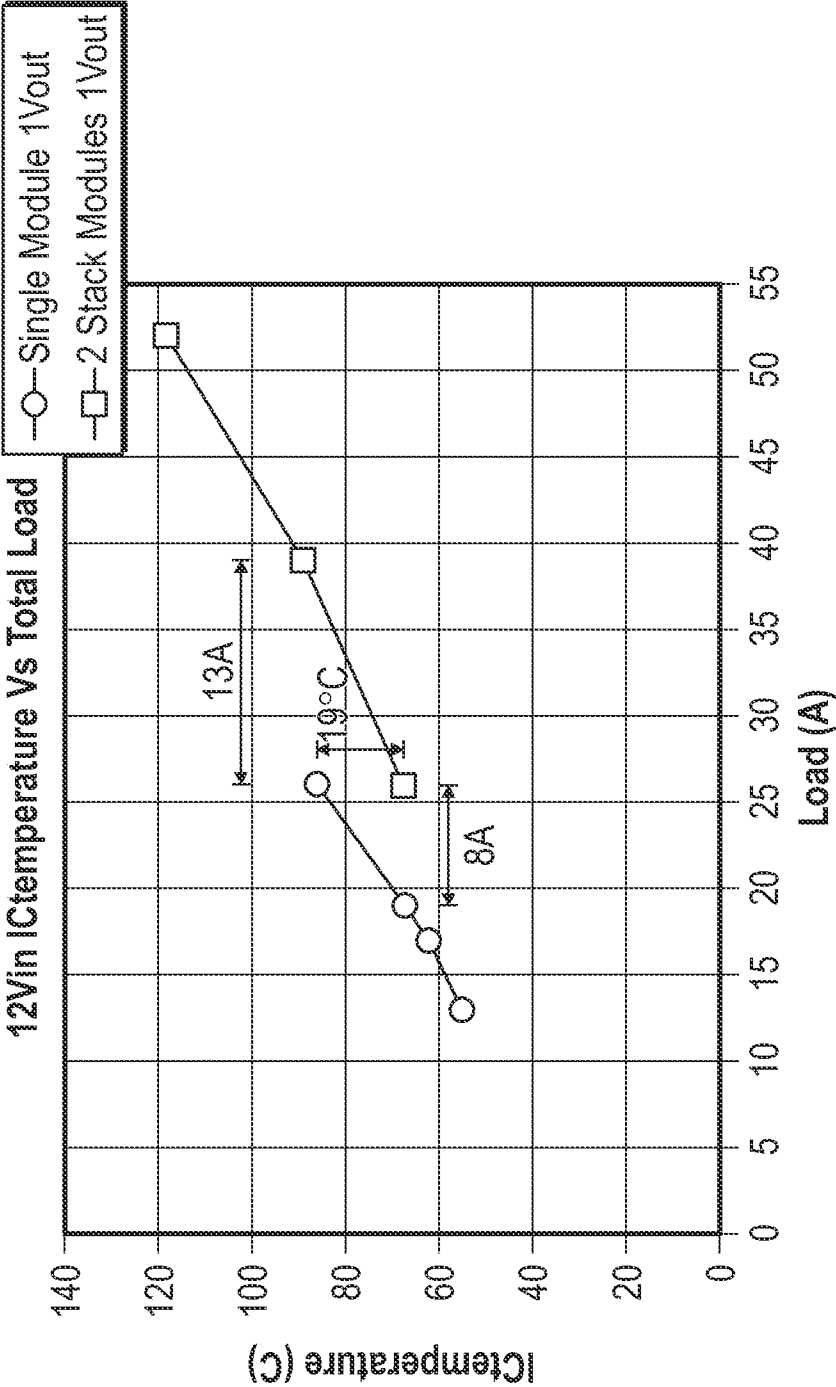


FIG. 9

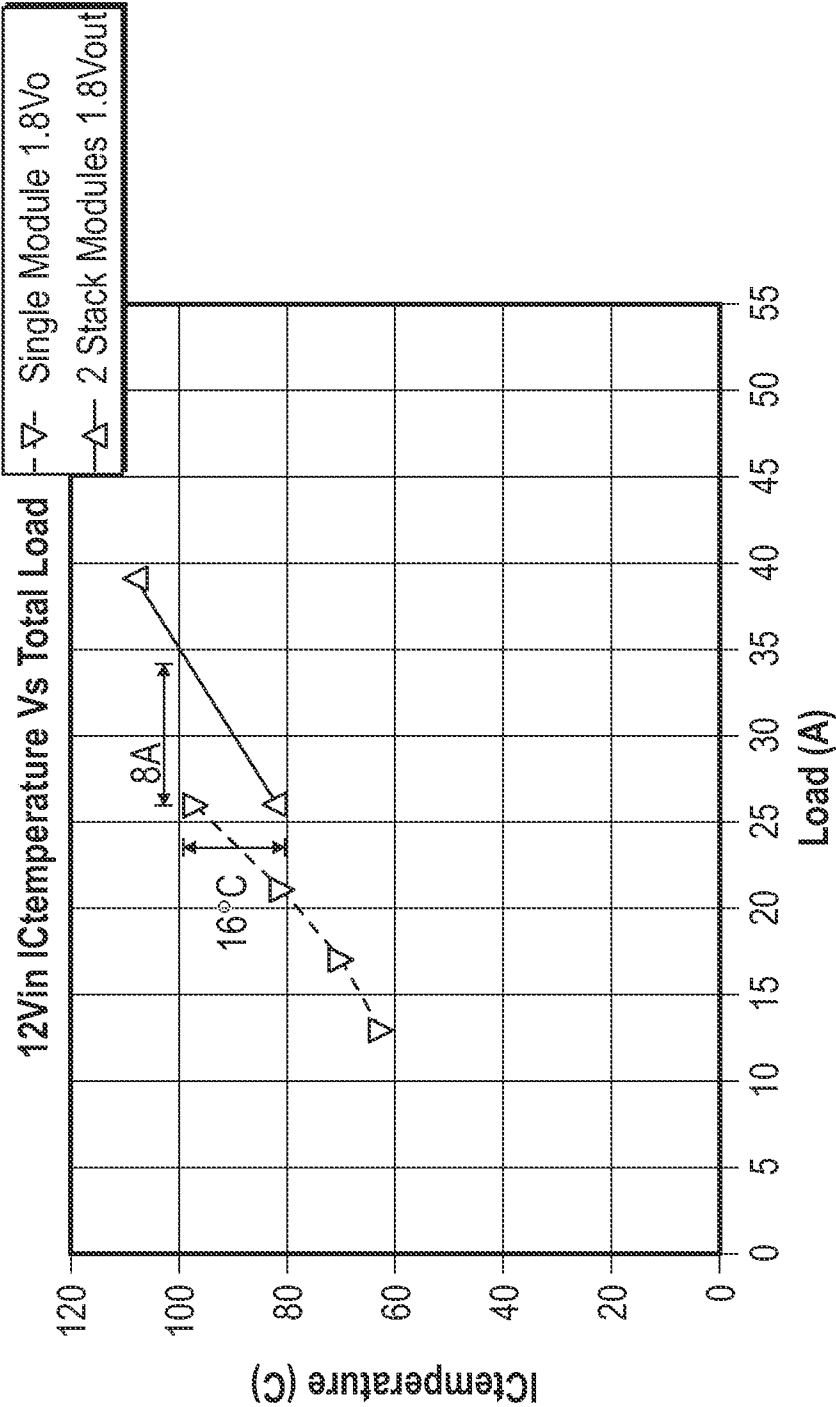


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2022/082212

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 25/10(2006.01)i; H01L 23/31(2006.01)i; H01L 25/00(2006.01)i; H01L 23/538(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01L 25/10(2006.01); G06F 1/26(2006.01); G06F 1/32(2006.01); H01L 23/12(2006.01); H01L 23/498(2006.01); H01L 23/50(2006.01); H01L 23/538(2006.01); H01L 25/065(2006.01); H03K 19/1776(2020.01)		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: package-on-package, bypassing, via, voltage-regulator		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 08 May 2023		Date of mailing of the international search report 08 May 2023
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer HONG, Kee Wan Telephone No. +82-42-481-5003

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