April 9, 1968 D. PETZOLD 3,377,468

COUNTER EQUIPPED WITH SIGNAL SORTING OUT AND SUPPRESSING MEANS

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Fig. 1a

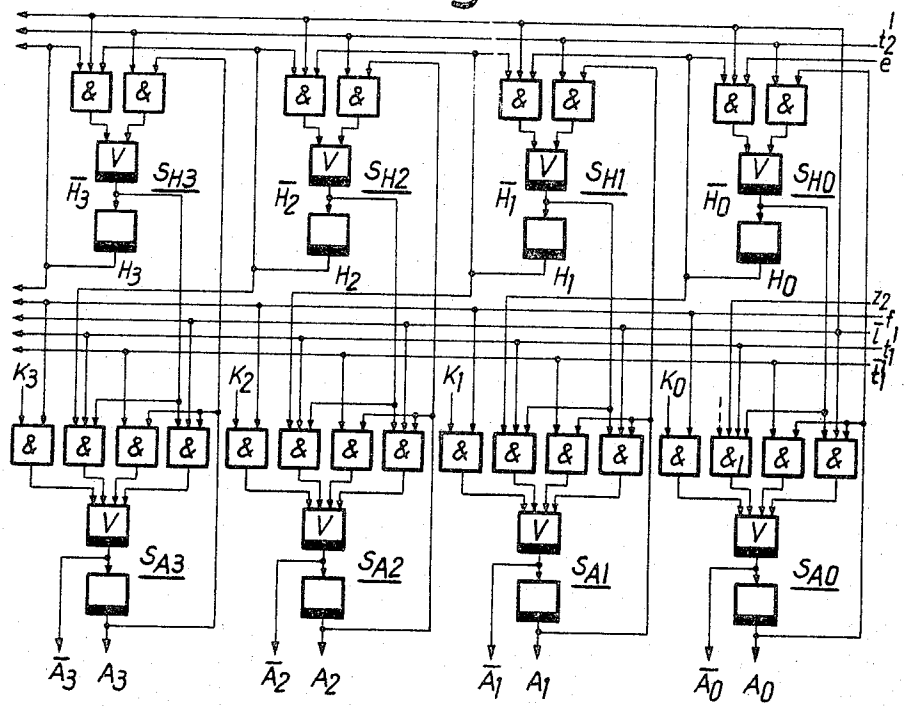


Fig. 3a

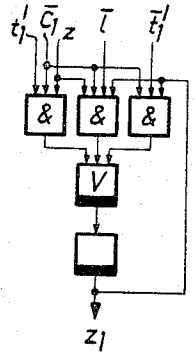


Fig. 3b

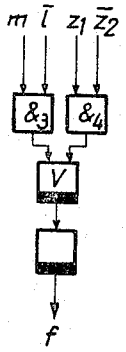
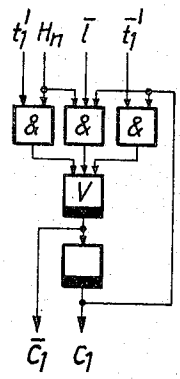


Fig. 3c



Inventor:
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By: Spencer & Kaye
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Fig. 1b

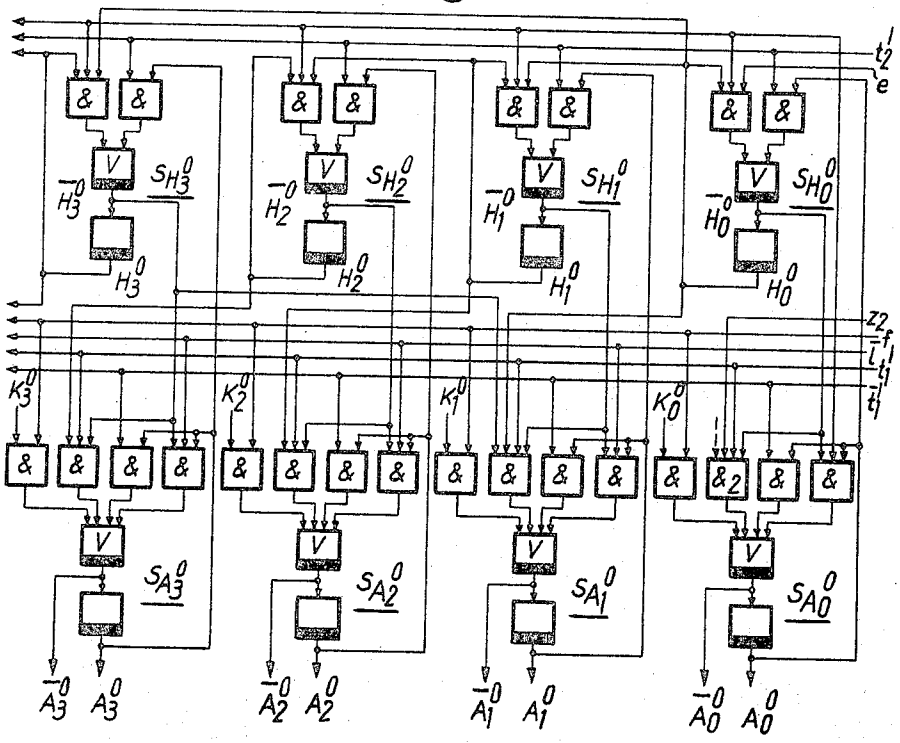


Fig. 5a

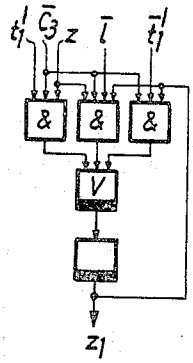


Fig. 5b

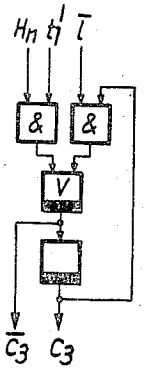
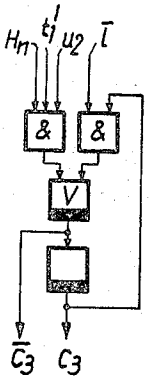


Fig. 5c



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COUNTER EQUIPPED WITH SIGNAL SORTING OUT AND SUPPRESSING MEANS

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Fig.2a



Fig.2b



Fig.2c



Fig.2d

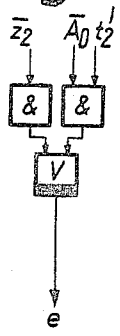


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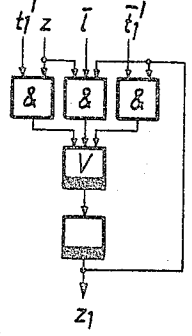


Fig.2f

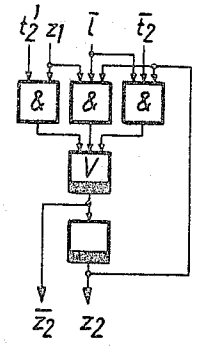


Fig.2g

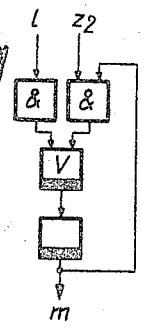


Fig.2h

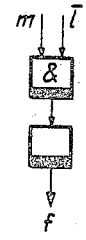


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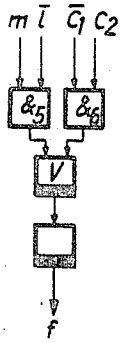


Fig.4b

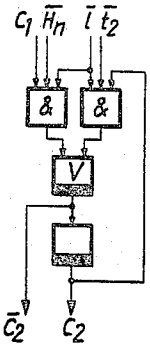


Fig.6a

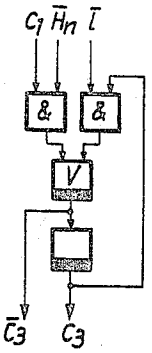
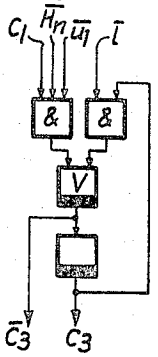


Fig.6b



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Fig.7a

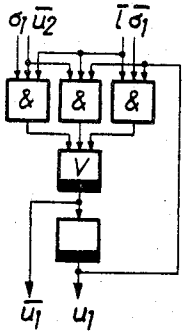


Fig.7b

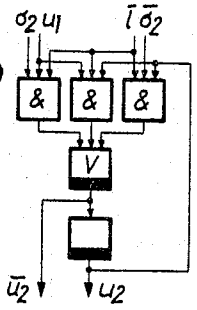


Fig.8a

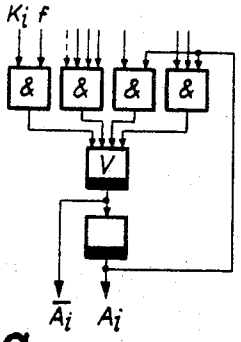


Fig.8b

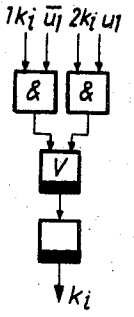


Fig.8c

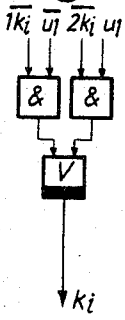


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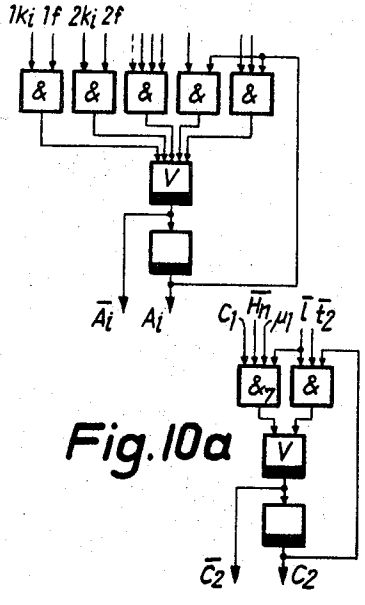


Fig.9b



Fig.9c

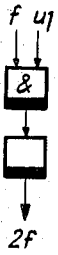
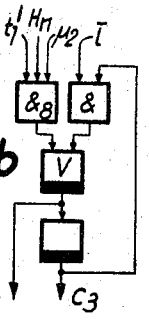


Fig.10a

Fig.10b



Inventor:
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Fig. 11a

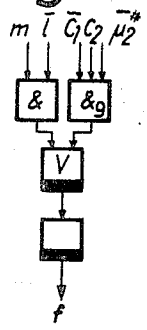


Fig. 11b

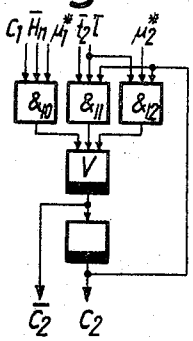


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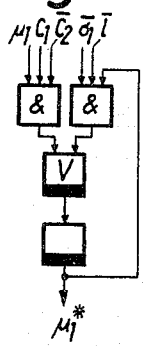


Fig. 12b

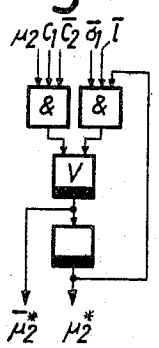


Fig. 13a

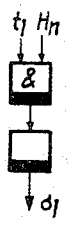


Fig. 13b

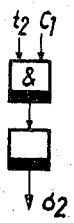


Fig. 13c

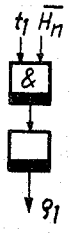


Fig. 13d

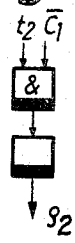


Fig. 14a



Fig. 14b

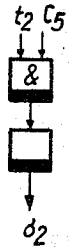


Fig. 14c

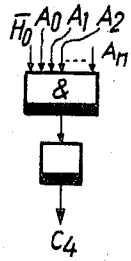


Fig. 14d

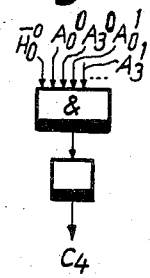


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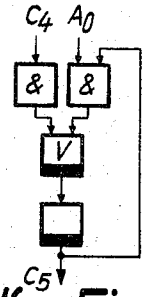


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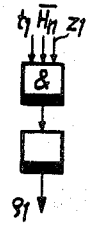


Fig. 15b

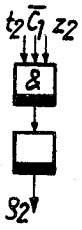


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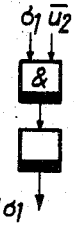


Fig. 16b

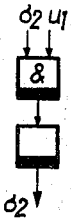


Fig. 16c

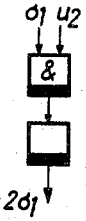
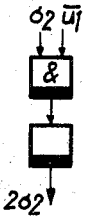


Fig. 16d



Inventor:
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By: Spencer & Kaye
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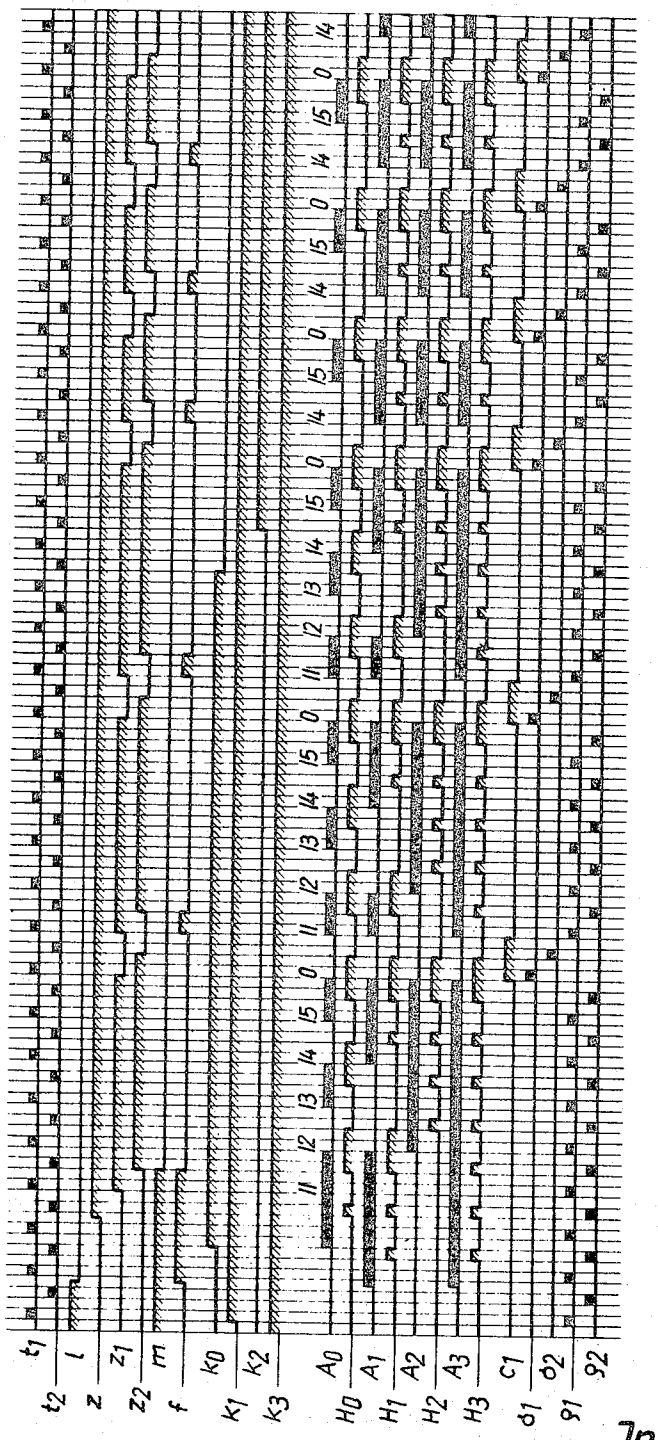


Fig. 17

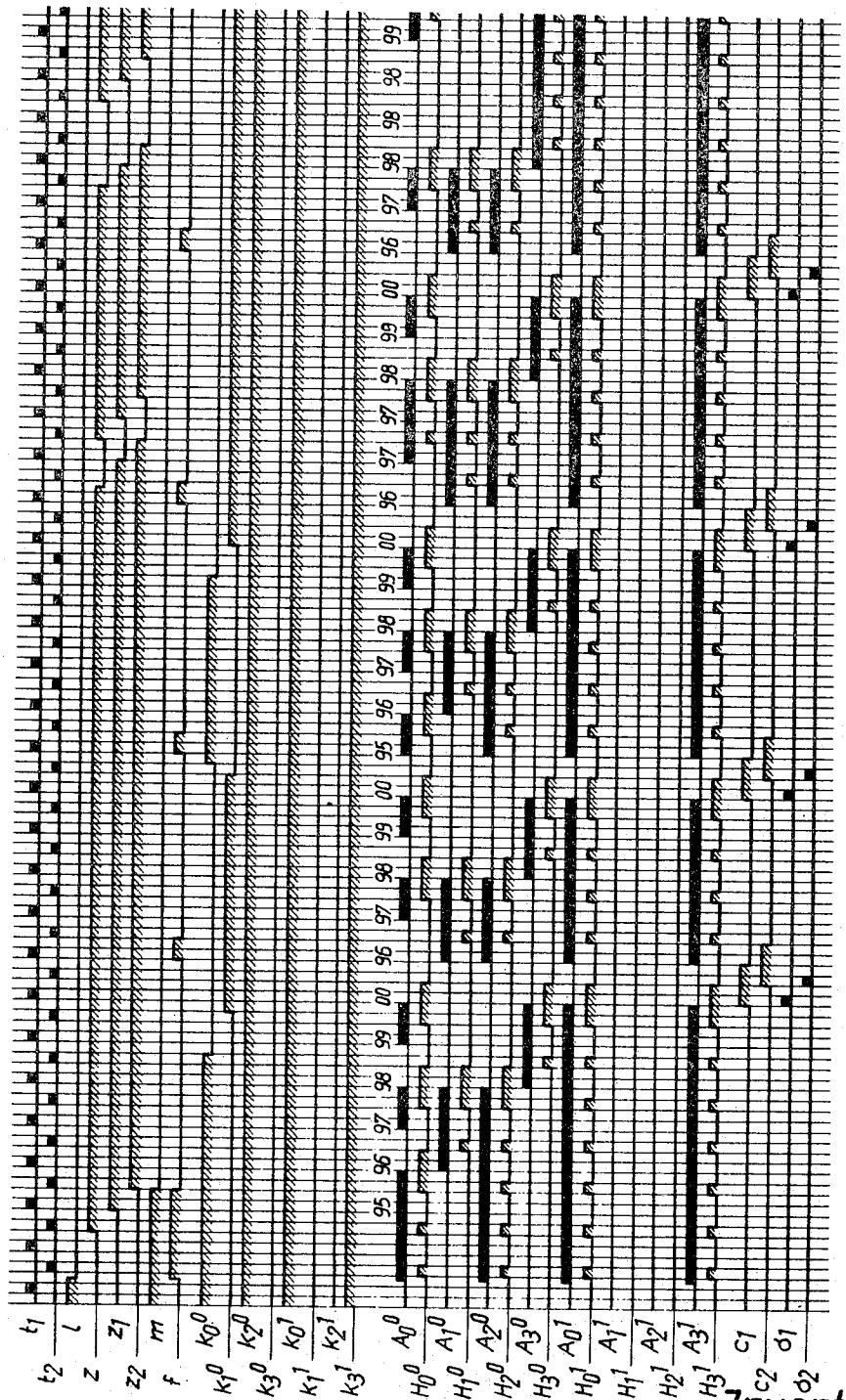
Inventor:
Dieter Petzold
By: Spencer & Kaye
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Fig. 18



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COUNTER EQUIPPED WITH SIGNAL SORTING OUT AND SUPPRESSING MEANS

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Fig. 20a

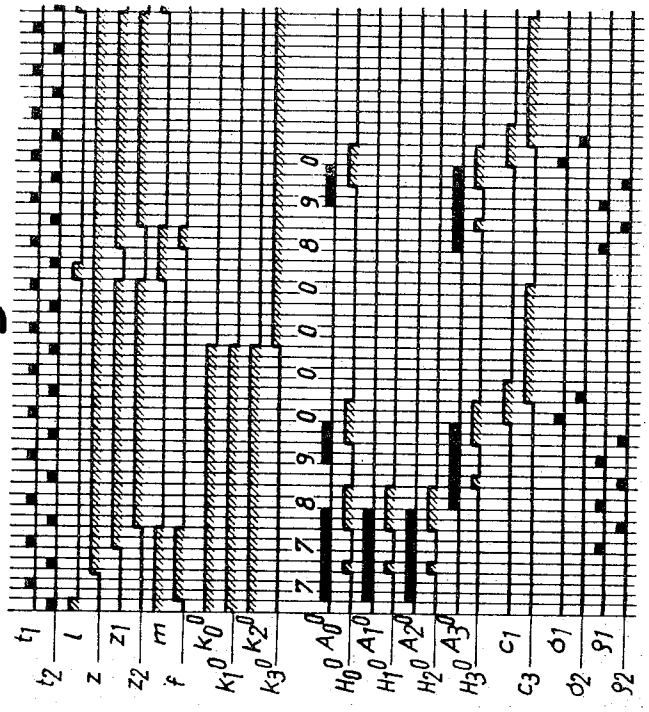


Fig. 20b

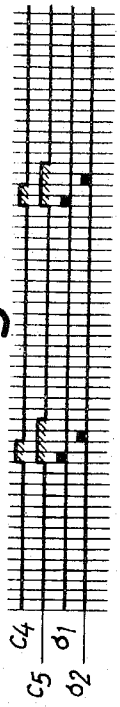


Fig. 19a

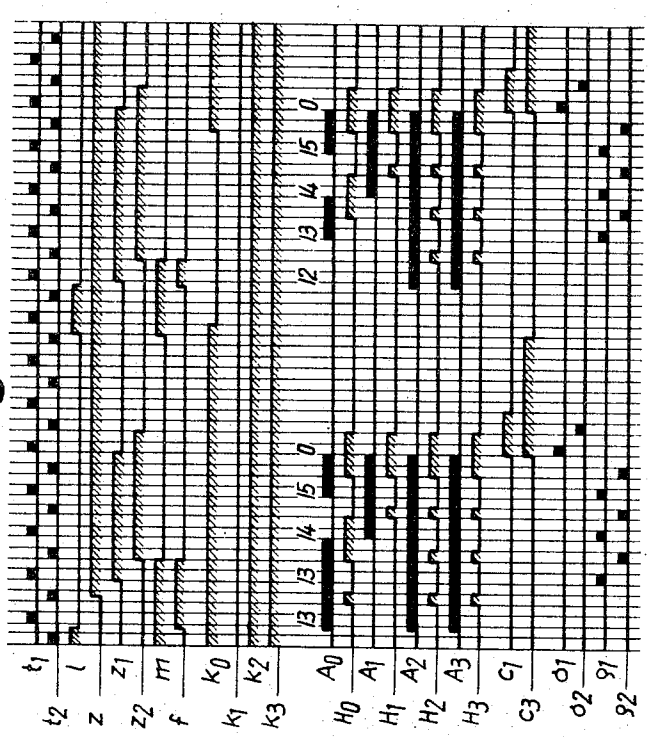
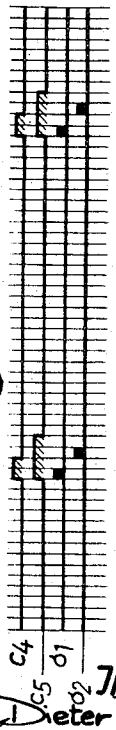


Fig. 19b



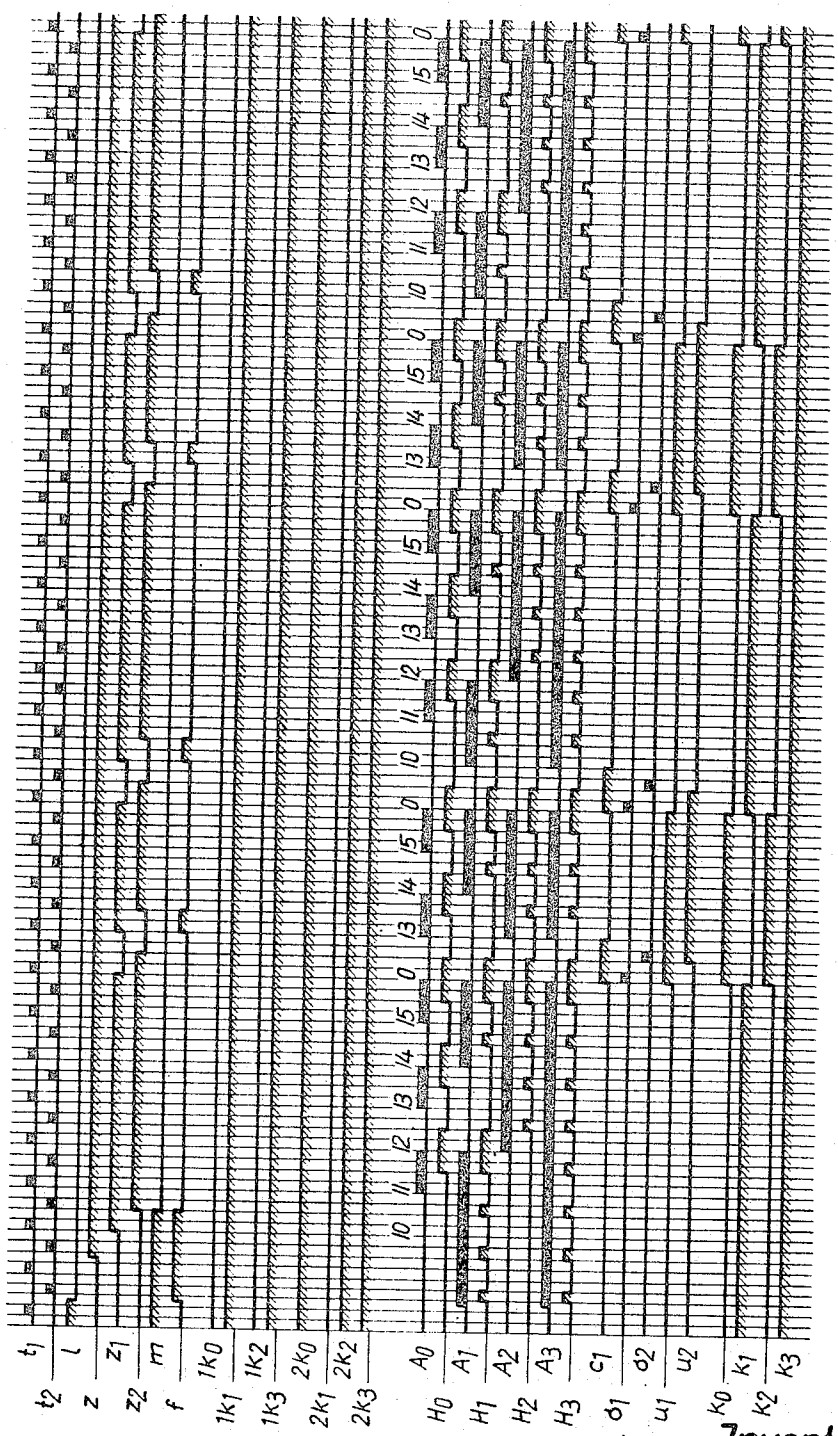
Inventor:
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By: Spencer & Kaye
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Fig. 21



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Dieter Petzold

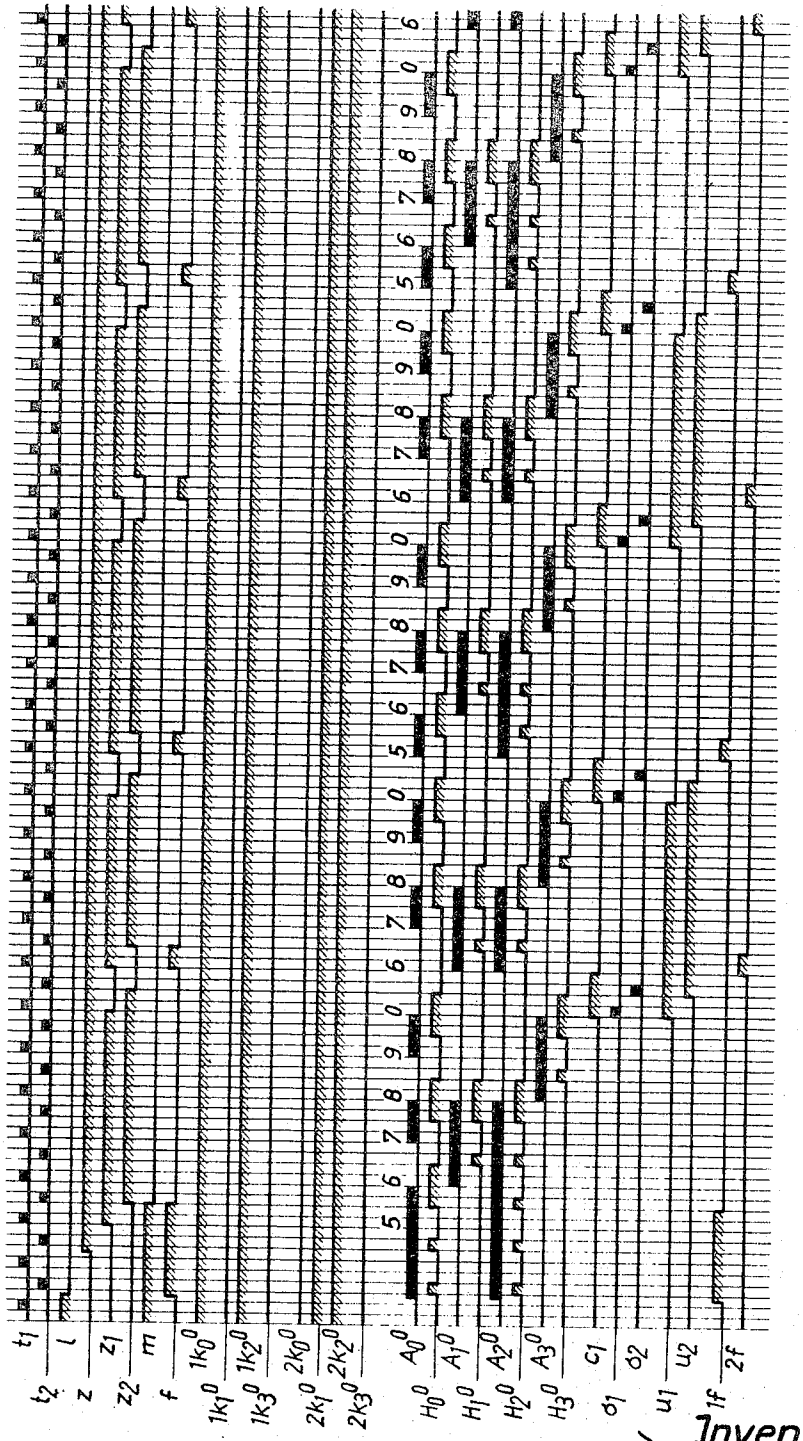
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Fig. 22



Inventor:
Dieter Petzold

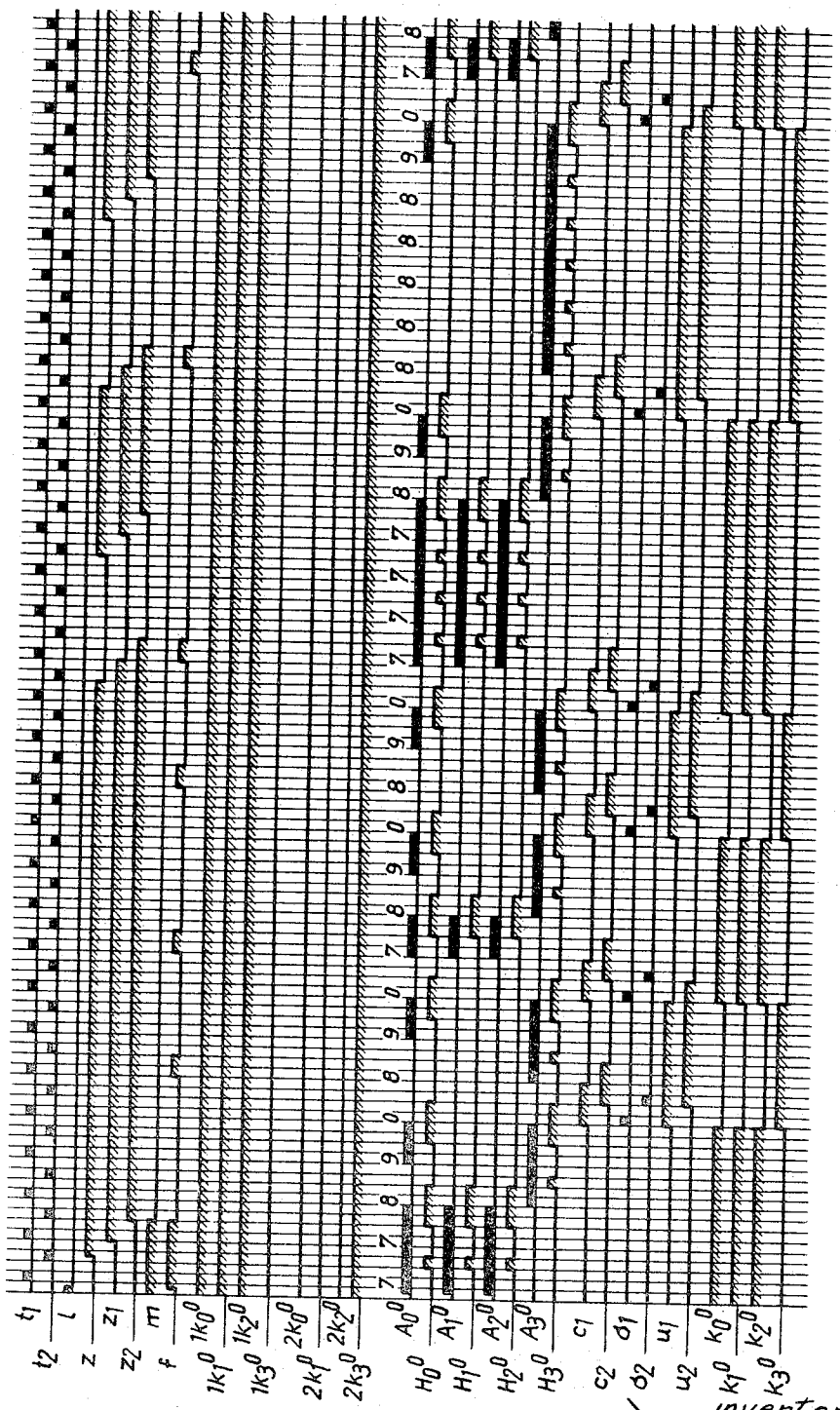
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Fig. 23



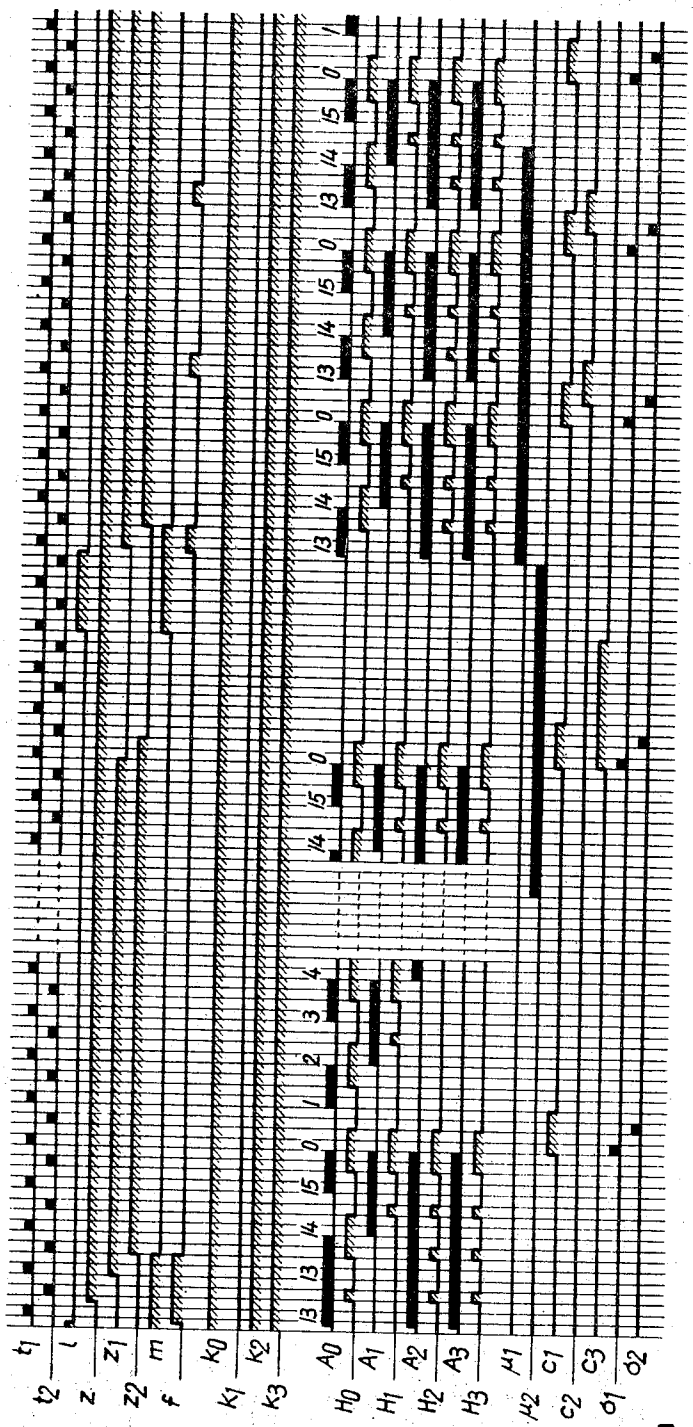
inventor:
Dieter Petzold
By: Spencer & Kaye
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Fig. 24



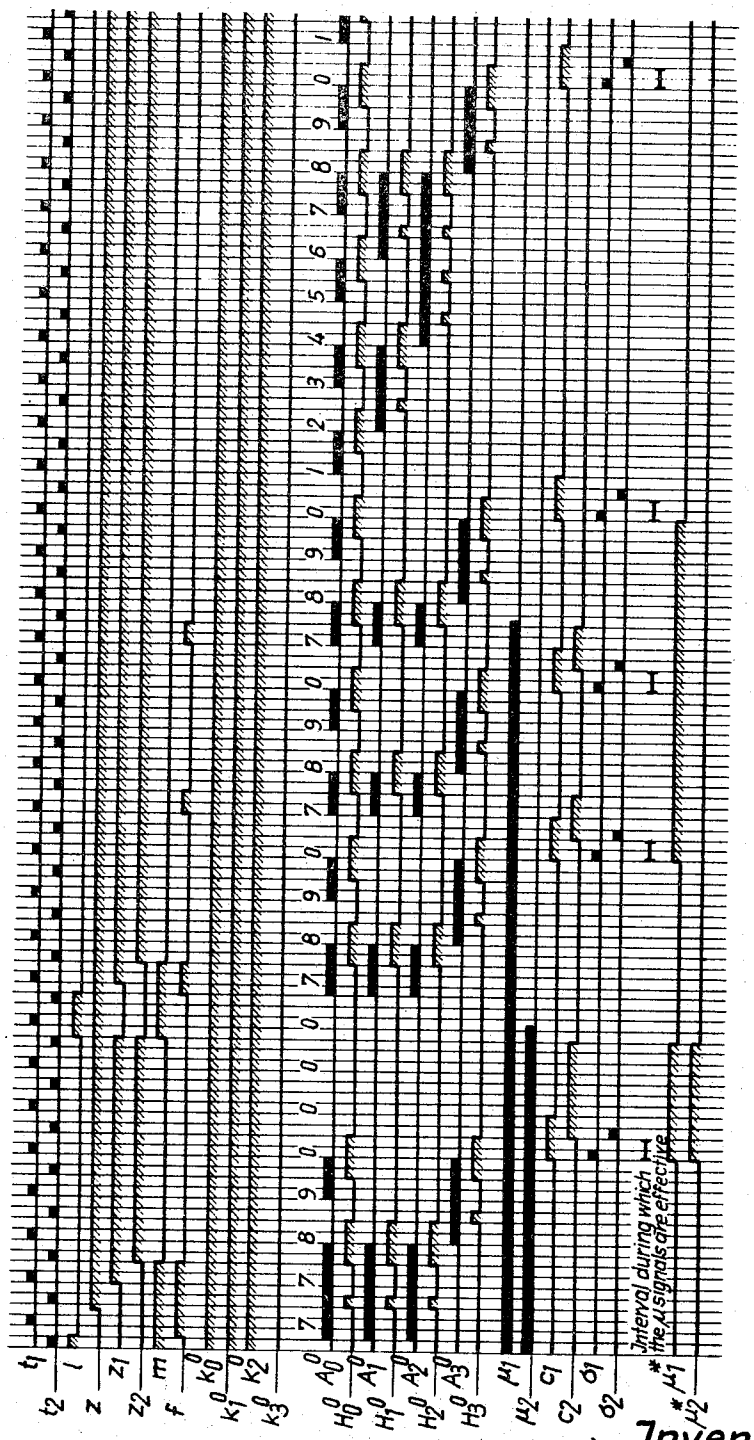
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Fig. 25



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COUNTER EQUIPPED WITH SIGNAL SORTING OUT AND SUPPRESSING MEANS

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ABSTRACT OF THE DISCLOSURE

A counting arrangement in which a presettable multiple-stage static counter, to which counting and auxiliary counting signals are applied, is equipped with means for sorting out and suppressing signals while the counter is in its zero condition, to which it has reverted after having reached and passed its maximum count.

The present invention relates to a circuit arrangement for sorting or suppressing certain signals from a sequence or so-called train of signals.

The present invention involves the use of a static counter shown in my co-pending application Ser. No. 327,585, filed Nov. 29, 1963. For purposes of explanation, reference is made to FIGURES 1*a* and 1*b* of the accompanying drawings which are presentative embodiments of such a counter, with FIGURE 1*a* being a circuit diagram of the first four counter stages of a binary counter and FIGURE 1*b* being a circuit diagram of the first four counter stages of a decimal counter, these first four stages of the decimal counter constituting the 0th decade. Each counter stage incorporates a main storage unit, i.e., a memory unit hereinafter referred to simply as a main store S_A and an auxiliary store S_H. Each store is identified by an appropriate subscript, e.g., S_{A1}, S_{H2}, and, in the case of the stores of the decimal counter, by appropriate superscripts, e.g., S_{A3}^{0}, S_{H2}^{0}, identifying the decade. The stores are constituted by input AND-circuits whose outputs are connected to OR/NOT-circuits. All of the stores are galvanically coupled to each other. The configuration of the applied input signals is of no consequence; all that is necessary is that the input signals have at least a certain amplitude.

FIGURES 2*a* through 2*g*, inclusive, show circuits, described in the above-mentioned application, used for forming the signals applied to the counter. The operation of these circuits, together with the significance of the various signals produced thereby will be explained in conjunction with the operation of the counter which is as follows:

The output signals H of the auxiliary stores are auxiliary signals formed by the counter and are required for the proper operation thereof. For reliable operation, the static counter requires, besides the signals t_1 to be counted, auxiliary counting signals t_2 which are staggered or time shifted with respect to the signals t_1, i.e., the signals t_2 do not appear at the same time as the signals t_1 and can thus be said to be displaced with respect to each other. Before the start of a counting operation, all of the stores are erased, i.e., reset, by the application of an erase signal l=L (where L represents the binary "one"). During the operation of the counter, l=0. The counting signals t are not applied directly to the inputs of the counter but are first combined, in the circuits shown in FIGURES 2*a* through 2*c*, with the negated erase signal $\bar{l}$, to form t' signals. A signal e is formed by the circuit of FIGURE 2*d*, the purpose of this signal being only so that the auxiliary store of the counter stage of the lowest order will, structurally, be identical to the auxiliary stores of the succeeding counter stages. The signal z is a counting command signal by means of which the decision is made as to whether or not the counter is to count: z=0 signifies that the counter is not to count and z=L signifies that the counter is to count. This signal z may appear at any time and is used, as an input applied to the circuits of FIGURES 2*e* and 2*f*, to derive a clear-for-counting signal z_2 which is so synchronized that it can change its state (from 0 to L vice versa) only at the start of an auxiliary counting signal t_2. The store shown in FIGURE 2*e* at first produces a signal z_1 which, when l=0, is formed together with the first counting signal t_1 that appears after the command signal z=L, and which signal z_1 disappears upon the application of an erase signal l=L or upon the application of the first t_1 signal that appears when z is again equal to 0. The signal z_1 controls the store whose circuit is shown in FIGURE 2*f*. This store, which puts out the signal z_2, is set upon the application of the first signal t_2 that appears after z_1=L, so long as l=0, and is erased when l=L or by the application of the first signal t_2 which appears after z_1 has become equal to 0.

The signals k applied to the inputs of the main stores of the counters shown in FIGURES 1*a* and 1*b* serve to preset the counter to a given number. These presetting signals may, for example, be derived from switches or stores. As soon as there appears the first signal to be counted (z_2=L), the counter continues to count from the number to which it has been set. The clear-for-presetting signal f makes certain that the counter stages can receive the presetting signals only after the previous count reached by the counter has been erased and before a new count has started. In this way, the presetting signals will have no effect on the counter during a counting operation, so that during a given counting operation, a new presetting can be made ready by means of the k signals. This clear-for-presetting signal f is formed by means of the store shown in FIGURE 2*h*, to whose inputs are applied a signal m and the negated erase signal $\bar{l}$. The signal m is formed in the store shown in FIGURE 2g; this store is set when the erase signal l=L and is erased when the clear-for-counting signal z_2, i.e., the signal which represents the command to the counter to commence counting, is equal to L.

The signals formed by means of the circuits shown in FIGURES 2*a* through 2*h* are also needed in conjunction with the newly introduced sorting signals, for controlling the counter. In certain cases, some of the circuits of FIGURES 2*a* through 2*h* will be modified, as will be described below. But as shown, the circuits of FIGURES 2*a* through 2*h* carry out the following logic functions:

$t_1\&\bar{l}=t_1'$ (FIGURE 2*a*)

$\bar{t}_1\&\bar{l}=t_1'$ (FIGURE 2*b*)

$t_2\&\bar{l}=t_2'$ (FIGURE 2*c*)

$\bar{z}_2 v(\bar{A}_0\&t_2')=\bar{e}$ (FIGURE 2*d*)

$(z_1\&t_1')v(z_1\&z\&\bar{l})v(z_1\&\bar{t}_1')=z_1$ (FIGURE 2*e*)

$(z_1\&t_2')v(z_2\&z_1\&\bar{l})v(z_2\&\bar{t}_2\&\bar{l})=z_2$ (FIGURE 2*f*)

$lv(m\&z_2)=m$ (FIGURE 2*g*)

$m\&\bar{l}=f$ (FIGURE 2*h*)

It is the object of the present invention to provide a way in which the binary or decimal counter of the type

described above is so controlled as to enable the counter to sort out or suppress each i^{th} signal from a sequence of signals. Instead of letting this sorting run off periodically, the counter should also be stopped after the appearance of this i^{th} pulse. Furthermore, after the sorting out of, for example, the i^{th} pulse, the next j^{th} and thereafter again the next i^{th} and then the next j^{th} pulse should be sorted out or suppressed. This procedure should be automatically interrupted after the sorting out of the j^{th} pulse following the i^{th} pulse. Finally, the objects of the present invention include the provision of a circuit arrangement capable of carrying out the above functions, which arrangement is capable of being switched over such that a one-time as well as a periodic sorting can be effected.

With the above objects in view, the present invention resides, basically, in a counting arrangement, as well as in a method of operating a counter, wherein a presettable multiple-stage counter, each of whose stages has a main store and an auxiliary store, has applied to it two trains of counting signals t_1 and t_2 which are displaced with respect to each other, which counter counts from a preset value on. According to the present invention, the sorting out or suppression of a given signal is effected while the counter is in the zero condition to which it has reverted after having reached and passed its maximum count. In other words, the counter, be it binary or decimal, will be able to count to a certain maximum, after which the receipt of a further counting signal will cause the counter to revert to zero. For example, if the counter is a binary counter having four stages, the maximum count is 15, after which a further counting signal reverts the counter back to 0. If the counter is a one-decade counter, its maximum count will be 9, whereafter the next counting signal reverts the counter back to 0. And it is during the time that the counter, after having reached and passed its maximum count and is at zero, that the sorting out takes place.

Additional objects and advantages of the present invention will become apparent upon consideration of the following description when taken in conjunction with the accompanying drawings in which:

FIGURES 1*a* and 1*b*, already referred to above, are schematic circuit diagrams showing, respectively, the first four stages of a binary counter, and the first four stages constituting the 0th decade of a decimal counter.

FIGURES 2*a* through 2*h*, also already referred to above, are schematic circuit diagrams of stores in which various signals are formed.

FIGURES 3*a* through 3*c* are schematic diagrams of circuits used for periodic sorting (Method I).

FIGURES 4*a* and 4*b* are schematic diagrams of circuits used for periodic sorting (Method II).

FIGURES 5*a* through 5*c* are schematic diagrams of circuits used for one-time sorting (Embodiment 1).

FIGURES 6*a* and 6*b* are schematic diagrams of circuits used for one-time sorting (Embodiment 2).

FIGURES 7*a* and 7*b* are schematic diagrams of circuits for producing switch-over signals for a counter having two presetting registers.

FIGURES 8*a* through 8*c* are schematic diagrams of circuits for producing a presetting signal (k) from the signals of the presetting register (Method A).

FIGURES 9*a* through 9*c* are schematic diagrams of circuits for producing two clear-for-presetting signals (1*f*, 2*f*) for counters having two presetting registers (Method B).

FIGURES 10*a* and 10*b* are schematic diagrams of circuits by means of which the counter is controlled in such a manner that, after the sorting has taken place, the counter is blocked, or begins to count with 1 or with a preset value (Example 1).

FIGURES 11*a* and 11*b* are schematic diagrams of circuits by means of which the counter is controlled in such a manner that, after the sorting has taken place, the counter is blocked, or begins to count with 1 or with a preset value (Example 2).

FIGURES 12*a* and 12*b* are schematic diagrams of circuits for synchronizing the switching signals for Example 2.

FIGURES 13*a* through 13*d* are schematic diagrams of output circuits for sorting (σ) and suppressing (s).

FIGURES 14*a* through 14*e* are schematic diagrams of circuits by means of which the sorting occurs one step earlier.

FIGURES 15*a* and 15*b* are schematic diagrams of output circuits in which the s signals appear only during the counting operation.

FIGURES 16*a* through 16*d* are schematic diagrams of output circuits, usable in conjunction with counters having two presetting registers, for effecting the sorting via separate lines.

FIGURE 17 is a time plot showing the timed relationship between the various signals in the case of a binary counter operating, while sorting periodically, in accordance with Method 1. In this and the other time plots, the abscissa of each signal represents the value 0 while the lines overlying the abscissa represent the binary "one" or L.

FIGURE 18 is a time plot showing the timed relationship between the various signals in the case of a decimal counter operating, while sorting periodically, in accordance with Method II.

FIGURES 19*a* and 19*b* are time plots showing the timed relationship between the various signals in the case of a binary counter operating, with one-time sorting, in accordance with Embodiment 1.

FIGURES 20*a* and 20*b* are time plots showing the timed relationship between the various signals in the case of a decimal counter operating, with one-time sorting, in accordance with Embodiment 2.

FIGURE 21 is a time plot showing the timed relationship between the various signals in the case of a binary counter with two preset registers operating, while sorting periodically, in accordance with Method I–A.

FIGURE 22 is a time plot showing the timed relationship between the various signals in the case of a decimal counter with two preset registers operating, while sorting periodically, in accordance with Method I–B.

FIGURE 23 is a time plot showing the timed relationship between the various signals in the case of a decimal counter with two preset registers operating, while sorting periodically, in accordance with Method II–A.

FIGURE 24 is a time plot showing the timed relationship between the various signals in the case of a binary counter equipped with the circuits of FIGURES 10*a* and 10*b*.

FIGURE 25 is a time plot showing the timed relationship between the various signals in the case of a decimal counter equipped with the circuits of FIGURES 11*a* and 11*b*.

In each of the various circuit diagrams, the AND-circuits are identified by "&" and the OR-circutis by "v," and in each case the black bar represents the presence of an inverse or complement, i.e., a negated, output. Various ones of the circuits also include pure inverter or so-called NO-circuits, these being circuits at which the output is the inverse or complement of the input, namely, 0 when the input is L, and L when the input is 0.

In accordance with the procedure identified above as Method I, a signal C_1 is formed for periodically sorting or suppressing each i^{th} signal in a sequence. It is with this signal C_1 that the signal z_1 is interrupted and the changed signal z_1 and the signal z_2 present up to now are used for producing a periodically appearing clear-for-presetting signal. Accordingly, those circuits which form the signals z_1 and f, i.e., the circuits shown in FIGURES 2*e* and 2*h*, are modified, or, more accurately, replaced by other circuits. The new circuits, as well as the circuit for producing the signal C_1, are shown in FIGURES 3*a*, 3*b* and 3*c*.

These circuits, together with the unchanged circuits of FIGURES 2*a* through 2*d*, 2*f*, and 2*g*, are suited for controlling the binary as well as the decimal counter. The function of the thus-obtained sorting means will first be explained for the case involving a binary counter having four stages as depicted in FIGURE 1*a*, particular reference being had to the time plots of FIGURE 17.

In order to keep the time plots reasonably simple, only the affirmed signals are shown (e.g., the time plots show only the signal t_1 and not its so-called complement or negate $\bar{t}_1$). Also for the sake of simplicity, the individual signals are shown as square pulses. The signals can assume either the value 0 or L. The time plot also shows the count reached by the counter at every point along the operation.

As explained above, the counting signals are t_1 and the auxiliary counting signals are t_2. These signals may appear in an irregular sequence, and both the signals themselves and the intervals between the signals can have different durations. The main and auxiliary stores of the counter stages are erased as soon as the erase signal l=L. The signal *e*, formed by the circuit of FIGURE 2*d*, is not shown since the same is not needed for purposes of explanation but, as explained above, only for structural uniformity.

A signal z_1 is derived from the counting command signal *z* which may appear at any instant. This signal z_1 appears at the same time as the first t_1 signal which occurs after $z=L$. The clear-for-counting signal z_2 also appears at the same time as the first t_2 signal which occurs after $z_1=L$. If signal *z* becomes 0 (not shown in FIGURE 17), z_1 will become 0 upon the occurrence of the next t_1 signal and z_2 becomes 0 upon the occurrence of the next t_2 signal. As shown in FIGURE 17, the signals z_1 and z_2, produced by the circuits of FIGURES 3*a* and 2*f*, respectively, are interrupted at appropriate instants, as will be described below. The signal *m*, produced by the circuit of FIGURE 2*g*, becomes equal to L when $l=L$ and becomes 0 when the clear-for-counting signal $z_2=L$. The clear-for-presetting signal *f*, produced by the circuit of FIGURE 3*b*, again becomes equal to L after *l* has become equal to 0 at the same time as signal *m*; signal *f* is additionally produced at certain predetermined instants. Let it be assumed that, by means of the presetting signals k_0 through k_3, the counter has been preset to 11. When $f=L$, the preset values are taken over by the main stores of the counter stages. The first counting signal t_1 appearing after the clear-for-counting signal z_2 has become equal to L increases the count of the counter to 12, the next counting signal t_1 increases the count to 13, and so on. Inasmuch as the binary counter illustrated in FIGURE 1*a* has but four stages, the highest number it can count to is 15 (or LLLL in binary notation) so that after this number is reached, the next counting signal t_1 will advance the counter to 0, it being unnecessary to apply any special erase signal.

In the instant example, it will be assumed that a counting signal t_1 and the succeeding auxiliary counting signal t_2 is to be sorted out during the time the counter is set at 0. The sorting of the desired t_1 signal requires an auxiliary signal which is present during the t_1 signal. This auxiliary signal must not appear until the preceding t_1 signal has disappeared and must itself disappear before the appearance of the t_1 signal following the t_1 signal to be sorted. The same applies for the sorting out of the desired t_2 signal. The sorted out signals are identified as σ_1 and σ_2. The output signal H_n of the auxiliary store of the counter stage of the highest order is used as a suitable auxiliary signal for producing σ_1, this being, in the illustrated example, the signal H_3. The signal σ_1 is derived from the signal H_n and the counting signals t_1 by means of the circuit shown in FIGURE 13*a*, namely an AND/NOT/NOT-circuit. In the example, the signal σ_1 appears with the sixth t_1 signal after the counting command signal $z=L$. The number 6 is the complement of the preset number 11 with respect to the number of possible counter settings (16) plus 1. A further auxiliary signal C_1 is obtained for sorting out the signal σ_2. The signal C_1 appears when the counter counts to 0 and disappears with the next succeeding t_1 signal. Signal C_1 is produced by the circuit shown in FIGURE 3*c*, namely, a store having three input AND-circuits whose outputs are connected to an OR/NOT/NOT-circuit, which store is set when a t_1 signal appears while $H_n=L$ (so long as $l=0$), and is erased by the erase signal $l=L$ or by the first t_1 signal which appears after H_n has again become equal to 0. The signal σ_2 is derived from signal C_1 and the auxiliary counting signals t_2 by means of the AND/NOT/NOT-circuit shown in FIGURE 13*b*.

In order to obtain periodic sorting out, the signal C_1 is also used for erasing the z_1 signal. When the counting command signal *z* is not interrupted, the signal z_1 appears directly after the disappearace of the C_1 signal. As shown in the time plot, the interruption of z_1 results in the interruption of the clear-for-counting signal z_2, in that it changes its state whenever, following the change of the z_1 signal, the succeeding t_2 signal appears. The signals z_1 and z_2 are formed by the stores shown in FIGURES 3*a* and 2*f*, respectively, these stores being constituted by input AND-circuits whose outputs are connected to an OR/NOT/NOT-circuit. The z_1 store is set with the first counting signal t_1 appearing when the counting command signal $z=L$, so long as $l=0$ and $C_1=0$, and is erased when $l=L$ or by $C_1=L$, or by the first t_1 signal appearing after the *z* signal has disappeared. The z_2 store is set by the first auxiliary counting signal t_2 appearing after $z_1=L$, so long as $l=0$, and is erased by $l=L$ or by the first t_2 signal appearing after the z_1 signal has disappeared.

The clear-for-presetting signal *f*, besides appearing after the disappearance of the erase signal and remaining until the appearance of the clear-for-counting signal, also appears for a short period with the first t_1 signal after the pears for a short period with the first t_1 sigal after the counter has counted to 0 and disappears with the succeeding t_2 signal. Thus, in the illustrated example, the number 11 to which the counter is to be preset is again stored in the counter upon the appearance of this short *f* signal. The count increases to 12 with the next counting signal, and so forth until, finally, upon the appearance of the t_1 signal following the counting to 0, the number 11 is again preset into the counter, and the count is continued from this number. The *f* signal is formed by the circuit shown in FIGURE 3*b*, which includes two input AND-circuits whose outputs are connected to an OR/NOT/NOT-circuit. The AND-circuit &3, which has applied to it the signal *m* and the negated erase signal $\bar{l}$, produces the single *f* signal at the start of the counting, while the AND-circuit &4, to which applied the signals z_1 and $\bar{z}_2$, produces the periodically appearing *f* signals.

The number to which the counter is to be preset, as given by the *k* signals, can also be changed during the counting operation, as indicated at the right of the time plot. The new preset number—this being 14 in the example—is then taken over with the appearance of the next *f* signal, whereupon every third pulse

$$(16+1-14=3)$$

is sorted out.

The arrangement according to the present invention, besides making possible the generation of the signals σ_1 and σ_2 of any desired periodicity, also allows signals of a sequence to be suppressed. The time plot shows signals s_1 and s_2 which appear with each t_1 and t_2 signal, respectively. The s_1 are produced by means of the circuit shown in FIGURE 13*c*, which is an AND/NOT/NOT-circuit to which the signals t_1 and $\overline{H}_n$ are applied, while the s_2 signals are produced by means of the AND/NOT/NOT-circuit of FIGURE 13*d*, which has the signals t_2 and $\overline{C}_1$ applied to it. If it is desired not to let the *s* signals appear,

for example, prior to the appearance of the z_1 signals, all that is necessary is that the signal z_1 be additionally applied to the circuits which form the s signals.

By way of summary, the logic functions of the circuits of FIGURES 3*a* through 3*c* and FIGURES 13*a* through 13*d* are given as follows (the output functions for σ and s also applying to the methods to be described later):

$(z\&t_1'\&\overline{C}_1)v(z_1\&z\&\overline{l}\&\overline{C}_1)v(z_1\&\overline{t}_1'\&\overline{C}_1)=z_1$ (FIGURE 3*a*)
$(m\&\overline{l})v(z_1\&z_2)=f$ (FIGURE 3*b*)
$(H_n\&t_1')v(C_1\&H_n\&\overline{l})v(C_1\&\overline{t}_1')=C_1$ (FIGURE 3*c*)
$t_1\&H_n=\sigma_1$ (FIGURE 13*a*)
$t_2\&C_1=\sigma_2$ (FIGURE 13*b*)
$t_1\&\overline{H}_n=s_1$ (FIGURE 13*c*)
$t_2\&\overline{C}_1=s_2$ (FIGURE 13*d*)

The above logic functions, as well as the respective figures pertaining thereto, apply to both the binary as well as the decimal counter. The output signals of the counter stages of the lowest order have the subscript 0, the output signals of the counter stages of the highest order have the subscript n. The superscript introduced for the decimal counters is omitted. This convention will also apply to the following explanations.

The next llustrative example involves an operation, identified as Method II, in which the above described Method I of signal sorting is modified in such a manner that the sorting out can, at any desired instants, be so interrupted by making the counting command signal $z=0$, that the counter puts out the particular count which it has reached at that instant and, after z is again equal to L, continues to count from this count.

Method II requires, besides the signal C_1 needed for Method I—which signal remains the same for Method II—a further signal C_2 which serves as the blocking signal for the counter stage of the lowest order. The f signal is formed periodically by means of the signals C_1, C_2.

The circuits used in Method II are those shown in FIGURES 2*a* through 2*g*, FIGURE 3*c*, and FIGURES 4*a* and 4*b*. FIGURE 3*c* is the circuit for producing the signal C_1, while FIGURE 4*a* shows the circuit which produces the clear-for-presetting signal f and replaces FIGURE 2*a*, with FIGURE 4*b* showing the circuit for producing the signal C_2. These circuits are suited for controlling both the binary as well as the decimal counter. Method II will now be explained in conjunction with the time plot of FIGURE 18. By way of example, the counter will be considered to be a decimal counter according to FIGURE 1*b* but having two decades, and in order to distinguish between these two decades, the signals k, A and H are, in the time plot, further identified by appropriate superscripts.

The signal f formed for Method II appears and disappears at the same instants as the signal f formed in accordance with Method I. The significance of all signals, except C_2, has already been explained above. By way of example, it is assumed that when $f=L$, the signals k set the counter to 95. The first σ_1 signal is, accordingly, formed with the 6th t_1 signal (101—95=6) after z has become equal to L. Upon the occurrence of the first counting signal t_1 after the counter has counted to 0, and f signal is once again formed and the number to which the counter is to be preset, as determined by the k signals, is written into the counter; in the example, this will be the number 96. The next σ_1 signal is formed with the 5th t_1 signal (101—96=5) following the first σ_1 signal. The right portion of the time plot shows two interruptions of the counting command signal z. The interruption of z also interrupts z_1 and hence z_2. As shown in the time plot, the count reached by the counter is preserved while $z_2=0$, and the counting continues with the first counting signal t_1 after z_2 has again become equal to L.

As in method I, the signal C_1 is formed by the circuit of FIGURE 3*c*, H_n representing, as before, the output signal of the auxiliary store of the counter stage of the highest order; this, in the time plot, is H_3^1. The signal C_2 appears while $C_1=L$, and when H_n becomes 0; signal C_2 disappears upon the appearance of the first t_2 signal after C_1 has again become equal to 0. The signal C_2 is produced in the store shown in FIGURE 4*b*, this store being set, so long as $l=0$, by $H_n=0$ with C_1 being equal to L, and is erased when $l=L$ or when $t_2=L$ with C_1 being equal to 0. The signal C_2 is used for producing the f signal. As before, the clear-for-presetting signal f is produced by means of the circuit shown in FIGURE 4*a*, the same including two input AND-circuits &5 and &6 whose outputs are connected to an OR/NOT/NOT-circuit. The f signal is produced after erasing until the start of the clear for counting by means of the signals m and $\overline{l}$ applied to the AND-circuit &5, while the periodically appearing f signals are produced by means of the signals C_1 and C_2 applied to AND-circuit &6. Since the Method II, in contradistinction to Method I, and z_2 signal is not interrupted automatically when the counter reaches 0, the main store of the counter stage of the lowest order would, with the next succeeding t_1 signal (at that instant at which the preset number is to be taken over by the counter as a result of the f signal), be set independently of the number to which the counter is to be preset. In order to prevent this, the mentioned main store has applied to it, at the input shown in dashed lines leading to AND-circuit &1 (FIGURE 1*a*) or &2 (FIGURE 1*b*), the negated signal $\overline{C}_2$, the same serving as a blocking signal.

The signals σ_1, σ_2, as well as the signals s_1, s_2, not shown in the time plot, are produced by the circuits of FIGURES 13*a* through 13*d*, in the same manner as in Method I.

The following are the logic functions of the circuits of FIGURES 4*a* and 4*b*:

$(m\&\overline{l})v(\overline{C}_1\&C_2)=f$ (FIGURE 4*a*)
$(C_1\&\overline{H}_n\&\overline{l})v(C_2\&\overline{t}_2\&\overline{l})=C_2$ (FIGURE 4*b*)

Instead of sorting out a signal periodically from a series of signals, it may at times be desired to stop the counter after a given number of counting steps, for example after the first σ_1 and σ_2 signals have been produced. There will now be described two possibilities, referred to as Embodiments 1 and 2, respectively. According to Embodiment 1, a signal C_3 is formed by means of which the z_1 signal is interrupted, and according to Embodiment 2, the C_3 signal is introduced into the main store of the counter stage of the lowest order as a blocking signal.

The circuits used for Embodiment 1 are those shown in FIGURES 5*a* and 5*b*, which are employed in conjunction with the circuits of FIGURES 2*a* through 2*d* and 2*f* through 2*h*. The operation is shown in the time plots of FIGURE 19*a*, the counter being assumed to be a four-stage binary counter.

The store for forming signal C_3, shown in FIGURE 5*b*, is set with the first t_1 signal after $H_n=L$, so long as $l=0$, that is to say, at that instant at which the σ_1 signal appears. The store is erased upon the appearance of a new erase signal, i.e., when $l=L$. As shown in FIGURE 5*a*, the signal $\overline{C}_3$ is introduced into the z_1 store as an additional erase signal. In this way, the counter is prevented from continuing counting after the signal C_3 has appeared, and cannot proceed counting until after the signal C_3 has again become equal to 0 by $l=L$.

The time plot of FIGURE 19*a* shows how the counting operation progresses, after the clear-for-counting signal z_2 has become equal to L, from the preset value (13) to the highest count which the counter can reach (15) whereafter the counter—without there being any special erase signal applied—is reset to 0. The signal C_3 appears when the counter reaches 0, and disappears when the erase signal again appears. After l is once again equal to 0, the counter is preset to 12 by means of the k signals, and the count progresses from this point on.

The σ signals are sorted out while the counter is at 0.

These σ signals are produced by the circuits of FIGURES 13*a* and 13*b*. Here, the *s* signals are, for example, so formed that they appear only during the time interval between the instant at which z_1 becomes equal to L and the time the counter reaches its maximum count. These *s* signals are produced by means of the circuits shown in FIGURES 15*a* and 15*b*. The latter differ from the circuits of FIGURES 13*c* and 13*d* in that the input AND-circuits additionally have applied to them the signals z_1 and z_2, respectively. If the preset number is 13, the arrangement produces 16−13=3 Z_1 and Z_2, signals, 16 being the number of different positions to which the four-stage counter can be set.

The logic functions of the circuits of FIGURES 5*a*, 5*b*, 15*a* and 15*b* are as follows:

$(z\&t'_1\&\overline{C}_3)\vee(z_1\&z\&\overline{1}\&\overline{C}_3)\vee(z_1\&\overline{t}_1'\&\overline{C}_3)=z_1$ (FIGURE 5*a*)
$(H_n\&t_1')\vee(C_3\&\overline{1})=C_3$ (FIGURE 5*b*)
$t_1\&\overline{H}_n\&z_1=s_1$ (FIGURE 15*a*)
$t_2\&\overline{C}_1\&z_2=s_2$ (FIGURE 15*b*)

In accordance with Embodiment 2, a one-time sorting is effected by means of an arrangement which includes the circuits of FIGURES 2*a* through 2*h* as well as the circuit of FIGURE 6*a* which forms the signal C_3, and the circuit of FIGURE 3*c* which forms the signal C_1. The store of FIGURE 6*a* is set when while $C_1=L$, H_n becomes 0 and is erased only upon the appearance of the erase signal $l=L$. The negated signal $\overline{C}_3$ is applied to the dashed inputs of the AND-circuits $\&_1$ and $\&_2$ of FIGURES 1*a* and 1*b*, respectively, where it serves as a blocking signal.

The logic function of the store of FIGURE 6*a* which produces the signal C_3 is:

$(C_1\&\overline{H}_n)\vee(C_3\&\overline{1})=C_3$ (FIGURE 6*a*)

The time plot of FIGURE 20*a* shows the sorting out operation of a one-decade decimal counter, with presettings of 7 and 8. The σ signals are produced by means of the circuits of FIGURES 13*a* and 13*b*, and the *s* signals are produced by means of the circuits of FIGURES 15*a* and 15*b*. In accordance with the preset numbers 7 and 8, there will appear 3 and 2 *s* signals, respectively, these being the respective 10's complements of 7 and 8.

If, for example, the signals σ_1 and σ_2 are, during one-time sorting operation, to appear one counting step earlier, all that is necessary is that different auxiliary signals, identified as C_4, C_5, be used for producing the σ_1 and σ_2 signals. These signals are shown together with the σ signals in FIGURES 19*b* and 20*b*. The signals σ_1 and σ_2 can be produced by the circuits shown in FIGURES 14*a* and 14*b*, respectively, and can be used in both the binary as well as the decimal counter. The signal C_4 needed as one of the inputs of the circuit of FIGURE 14*a* appears when the counter reaches its maximum count and disappears upon the appearance of the next succeeding t_2 signal. If the counter is the binary counter, the signal C_4 is produced by means of the circuit of FIGURE 14*c*, whereas if the counter is the decimal counter, the signal C_4 is produced by means of the circuit of FIGURE 14*d*. The signals applied to the input AND-circuit in FIGURE 14*c* are the output signals A of all of the main stores, while the signals applied to the input AND-circuit in FIGURE 14*d* are the A signals of the counter stages for the 0th and 3rd bit. Each of the respective AND-circuits also has applied to it the negated output signal $\overline{H}_0$ of the auxiliary store of the counter stage of the lowest order, the purpose of which is to prevent the spurious short-duration appearance of a signal C_4 before the counter has carried out the intended number of counting steps. The C_4 signal is used in a store, shown in FIGURE 14*e*, capable of producing the signal C_5 needed as one of the inputs applied to the circuit of FIGURE 14*b*. The C_5 store is set by the signal C_4 and is erased when, after the counter has reached its highest count, the output signal of the main store of the lowest order counter stage (indicated for both the binary and decimal counters by A_0) disappears. (In FIGURE 14*e*, the AND-circuit to which signal C_4 is applied is shown for symmetry purposes only, since, functionally, the signal C_4 may be applied directly to one of the inputs of the OR/NOT-circuit.)

The logic functions of the circuits of FIGURES 14*a* through 14*e* are as follows:

$t_1\&C_4=\sigma_1$ (FIGURE 14*a*)
$t_2\&C_5=\sigma_2$ (FIGURE 14*b*)
$\overline{H}_0\&A_0\&A_1\&A_2\ \ldots\ \&A_n=C_4$ (FIGURE 14*c*)
$\overline{H}_0{}^0\&A_0{}^0\&A_3{}^0\&A_0{}^1\&A_3{}^1\&\ \ldots\ =C_4$ (FIGURE 14*d*)
$C_4\vee(C_5\&A_0)=C_5$ (FIGURE 14*e*)
$C_4\vee(C_5\&A_0)=C_5$ FIGURE 14*e*)

In accordance with a further feature of the present invention, there will now be described arrangements by means of which signals can be sorted out, or suppressed, in such a manner that first the *i*th, then the *j*th, thereafter again the *i*th, and then again the *j*th, and so on, can be sorted out or suppressed. Here, a counter having two presetting registers is used.

The values set into the first presetting register are identified by $1k$, while the values set into the second presetting register are identified by $2k$.

The arrangement described below may operate in accordance with either Method I or Method II, and the circuits described above in connection with these Methods I and II remain unchanged.

According to the invention, there is produced a switch-over signal u_1 for purposes of switching the presetting register or for forming new clear-for-presetting signals. The arrangement may operate in accordance with either of two methods, hereinafter referred to as Methods A and B. According to Method A, presetting signals k are derived from the signals $1k$ and $2k$ with the help of the u_1 signal, which signals k together with the clear-for-presetting signal f obtained according to Method I (FIGURE 3*b*) or Method II (FIGURE 4*a*) are applied to the main stores of the counter stages. According to Method B, a separate clear-for-presetting signal is formed for each presetting register. These signals, identified as $1f$ and $2f$, respectively, are derived from the clear-for-presetting signal f used heretofore, with the help of the u_1 signal. Also, the main stores of the counter stages are expanded to include one additional input AND-circuit in order to provide a second presetting path. Each of the Methods A and B can be used in conjunction with either of the above-described sorting Methods I and II. The circuits needed for carrying out Methods A and B are described in conjunction with the circuits of FIGURES 7*a*, 7*b*, 8*a*, 8*b*, 8*c*, 9*a*, 9*b* and 9*c*, and the time plots of FIGURES 21, 22 and 23.

A further signal u_2 is needed for forming the switch-over signal u_1. The signals u_1 and u_2 affect each other, and FIGURES 7*a* and 7*b* show circuits for forming the two signals. The store for forming u_1, shown in FIGURE 7*a*, is set by means of the first σ_1 signal which appears, while the store for forming u_2 is set by the succeeding σ_2 signal. The u_1 store is erased by the next succeeding σ_1 signal, and the u_2 store is erased by the next succeeding σ_2 signal. The u_1 store is again set by the next σ_1 signal, and the u_2 store is once again set by the next σ_2 signal, and so forth.

The logic functions of the circuits of FIGURES 7*a* and 7*b* are as follows:

$(\sigma_1\&\overline{u}_2\&\overline{l})\vee(u_1\&\overline{u}_2\&\overline{l})\vee(u_1\&\sigma_1\&\overline{l})=u_1$ (FIGURE 7*a*)
$(\sigma_2\&u_1\&\overline{l})\vee(u_2\&u_1\&\overline{l})\vee(u_2\&\sigma_2\&\overline{l})=u_2$ (FIGURE 7*b*)

According to Method A, the main stores of the counter stages remain unchanged, as shown schematically in FIGURE 8*a*. The input AND-circuits have applied to them the clear-for-presetting signal f, as described above, and the newly formed signal k_1, the latter being formed from the switch-over signal u_1 as well as the presetting signals $1k_1$ and $2k_1$, by means of either of the circuits shown in FIGURES 8*b* and 8*c*.

The logic functions of the circuits of FIGURES 8*b* and 8*c* are as follows:

$(1k_1\&\overline{u}_1)\,v\,(2k_1\&u_1)=k_1$ (FIGURE 8*b*)

or

$(\overline{1k}_1\&\overline{u}_1)\,v\,(\overline{2k}_1\&u_1)=\overline{k}_1$ (FIGURE 8*c*)

According to Method B, the main stores of the counter stages are, as shown in FIGURE 9*a*, expanded by one input AND-circuit. One input AND-circuit has applied to it the presetting signal $1k_1$ and the signal **1***f*, while a further input AND-circuit has applied to it the presetting signal $2k_1$ and the signal **2***f*. Signal **1***f* is derived from *f* and $\overline{u}_1$ by means of the circuit shown in FIGURE 9*b*, and signal **2***f* is derived from *f* and u_1 by means of the circuit shown in FIGURE 9*c*.

The logic functions of the circuits of FIGURES 9*b* and 9*c* are as follows:

$f\&=\overline{u}_1 1f$ (FIGURE 9*b*)

$f\&u_1=2f$ (FIGURE 9*c*)

FIGURES 21 through 23 are time plots showing the operation of a counter with two presetting registers which put out the signals **1***k* and **2***k*.

Referring now to FIGURE 21, the same shows a time plot representing the operation of a binary counter in accordance with Method I–A, i.e., the operation wherein the C_1 signal is used for interrupting the z_1 signal and wherein the periodic *f* signal is derived from the signals z_1, z_2. As is apparent from the time plot, the *k* signals correspond to **1***k* or **2***k*, depending on whether $u_1=0$ or $u_1=L$. The counter is initially set to **10**, in accordance with the particular **1***k* signals set by means of the *f* signal appearing at the beginning of the operation. The counter then counts to **11** upon the appearance of the first t_1 signal appearing after the clear-for-counting signal $z_2=L$, and so on. After the counter reaches its maximum, i.e., the number **15** in the case of a four-stage counter, it reverts back to **0**. The counter is then set to **13**, which is the value to which the second presetting register has been set, upon the appearance of the periodic *f* signal, whereupon the counter continues to count to **15**. The counter then once more reverts to **0**, and, after the appearance of the periodic *f* signal, is reset to the value contained in the first preceding register, namely, **10**, from which point on the counter then continues to count. The sorting out takes place whenever the counter is at **0**.

FIGURE 22 shows the operation of the decimal counter operating in accordance with Method I–B. Here, **1***f* and **2***f* signals are produced alternately from the *f* signal, with the help of the u_1 signal. These **1***f* and **2***f* signals are used, as explained in connection with the above time plot, for causing the particular values stored in the first and second presetting registers—in the example, the numbers **5** and **6**, respectively—to be written into the counter alternately, at the appropriate instants. The time plot assumes that there is one decade, so that the highest count which the counter reach is 9.

FIGURE 23 is a time plot showing the decimal counter operating in accordance with Method II–A, wherein the signals C_1, C_2 are used for periodically forming the *f* signal. Shown at the right side of the time plot of FIGURE 23 are two arbitrary interruptions of the counting command signal *z*. This interrupts the clear-for-counting signal z_2. The count is preserved so long as $z_2=0$.

While the above description involves the use of but two presetting registers, it will readily be appreciated that the invention is not so limited since more than two presetting registers can be used.

FIGURE 16 shows circuits by means of which the *i*th signal may be sorted out via a first line and the next succeeding *j*th signal may be sorted out via a second line. The *i*th signal to be sorted from the train of t_1 signals is designated $1\sigma_1$, the *i*th signal to be sorted from the train of t_2 signals is designated $1\sigma_2$, the *j*th signal to be sorted from the train of t_1 signals is designated $2\sigma_1$, and the *j*th signal to be sorted from the train of t_2 signals is designated $2\sigma_2$.

Either of Methods A and B can be used if the counter, after sorting out the *i*th and the next succeeding *j*th signal, is to be stopped. For this purpose, a C_3 signal is formed by means of either of the circuits shown in FIGURES 5*c* and 6*b*. As these circuits show, either signal u_2 (FIGURE 5*c*) or the signal $\overline{u}_1$ (FIGURE 6*b*) is used for forming the C_3 signal. Consequently, C_3 will not appear until the counter has been set to 0 for the second time. In the time plots of FIGURES 21 to 23, which depict the periodic sorting, this would, for the C_3 signal produced by the circuit of FIGURE 5*c*, be the instant at which the signal σ_1 appears for the second time; for the C_3 signal produced by the circuit of FIGURE 6*b*, this would be the instant at which the signal σ_2 appears for the second time. The C_3 signals do not disappear until a new erase signal $l=L$ appears. If, for example, the C_3 signal produced by the circuit of FIGURE 5*c* is used in conjunction with the circuits of FIGURES 3*a* through 3*c*, operating according to Method I, all that is necessary is that the negated signal $\overline{C}_3$ be additionally applied to all of the input stages of the z_1 store of FIGURE 3*a*. If the C_3 signal produced by the circuit of FIGURE 6*b* is used, the corresponding negated signal $\overline{C}_3$ is additionally applied to the input AND-circuit for the setting condition of the main store of the lowest order counter stage, this being the AND-circuits &$_1$ or &$_2$ of FIGURES 1*a* and 1*b*, respectively. Furthermore, the $\overline{C}_3$ signal is, for forming the *f* signal in accordance with Method I, additionally applied to the AND-circuit &$_4$ of FIGURE 3*b*; for forming the *f* signal in accordance with Method II, the $\overline{C}_3$ signal is additionally applied to the AND-circuit &$_6$ of FIGURE 4*a*.

The logic functions of the circuits of FIGURES 5*c* and 6*b* are as follows:

$(H_n\&t_1'\&u_2)\,v\,(C_3\&\overline{l})=C_3$ (FIGURE 5*c*)

$(C_1\&\overline{H}_n\&\overline{u}_1)\,v\,(C_3\&\overline{l})=C_3$ (FIGURE 6*b*)

In accordance with a further feature of the present invention, the arrangement is controlled by switching signals μ_1, μ_2, which, for example, may be put out by switches or by stores, in such a manner that, in the case of one-time sorting, the counter is blocked after a sorting or suppressing step, and, in the case of periodic sorting, the counter, after a sorting or suppressing, commences to count at 1 or at the preset value.

The first example involves a switching for Method II (periodic sorting) and Embodiment **1** (one-time sorting). The circuits according to FIGURES 2*a* through 2*d*, 2*f* and 2*g* remain unchanged, the z_1 signal is produced by the circuit of FIGURE 5*a*, the *f* signal is produced by the circuit of FIGURE 4*a*, and the C_1 signal is produced by the circuit of FIGURE 3*c*. The signals C_2 and C_3 are produced by the stores shown in FIGURES 10*a* and 10*b*, respectively, these stores having the μ signals applied to them. As is apparent from these figures, the stores of FIGURES 10*a* and 10*b* differ from those of FIGURES 4*b* and 5*b* only in that the AND-circuit &$_7$ and &$_8$ additionally have the μ_1 and μ_2 signals, respectively, applied to them. The negated signal $\overline{C}_2$ is again applied to the dashed inputs of AND-circuits &$_1$ or &$_2$ of FIGURES 1*a* and 1*b*, respectively.

When $\mu_1=0$ and $\mu_2=L$, no C_2 signal will appear because $\mu_1=0$, so that no periodic *f* signal can appear; and because $\mu_2=L$, the C_3 signal appears after the first sorting out and stops the counter. When $\mu_1=L$ and $\mu_2=0$, no C_3 signal appears because $\mu_2=0$, as a result of which the counter is not stopped; and because $\mu_1=L$, the C_2 signal appears periodically and as a result thereof, so does the signal *f*, so that after the sorting out operation, the counter continues to count beginning with the preset value. When $\mu_1=0$ and $\mu_2=0$, neither a C_2 signal nor a C_3 signal is

produced, so that the counter, after the sorting out, is neither preset nor stopped, but instead begins to count beginning with 1.

The logic functions of the circuits of FIGURES 10*a* and 10*b* are as follows:

$(C_1\&\overline{H}_n\&\overline{l}\&\mu_1)\vee(C_2\&\overline{l}_2\&\overline{l})=C_2$ (FIGURE 10*a*)

$(H_n\&t_1'\&\mu_2)\vee(C_3\&\overline{l})=C_3$ (FIGURE 10*b*)

In order to select the desired mode of operation, the signals μ_1, μ_2 can be put out by a three-position switch, as follows:

Switch Position	μ_1	μ_2	Mode of operation
1	0	0	After sorting, the counter begins to count starting at 1.
2	0	L	After sorting, the counter is stopped.
3	L	0	After sorting, the counter begins to count starting at the preset number.

FIGURE 24 is the time plot of a four-stage binary counter operating in accordance with the above circuits. Let it be assumed that at first the switch is in position **1**, i.e., that $\mu_1=0$, $\mu_2=0$, so that, after being cleared for counting, the counter counts from the preset value (13) to 15, whereafter it counts to 0 and continues to count beginning at 1. Let it now be assumed that before the counter again reaches 0, the switch has been moved to position **2** wherein $\mu_2=L$. The counter will then be stopped, after it has reached 0. The blocking signal C_3 is erased by means of the erase signal $l=L$. After the erase signal disappears, the counter is again preset. If the switch is meanwhile moved to position **3**, wherein $\mu_1=L$ and $\mu_2=0$, there will be a periodic sorting. After the switch has once more been moved back to position **1** wherein $\mu_1=0$ and $\mu_2=0$, the counter, after again reaching 0, begins to count starting with 1.

By way of a second example, there will now be described a switch-over involving an operation according to Method II (periodic sorting) Embodiment **2** (one-time sorting). The arrangement uses the circuits of all of FIGURES 2*a* through 2*g* which remain unchanged. The signal C_1 is formed by the circuit of FIGURE 3*c*, and the signals f and C_2 are formed by the circuits shown in FIGURES 11*a* and 11*b*, respectively. The circuit of FIGURE 11*a* differs from that of FIGURE 2*h* in that an additional switching signal $\overline{\mu_2}^*$ is applied to the AND-circuit &9 for purposes of periodically forming the signal f. The C_2 store of FIGURE 11*b* differs from that of FIGURE 4*b* in that a switching signal μ_1^* is applied to the AND-circuit &10 for the setting condition. Also, the AND-circuit for the holding condition (&11) has the same input signals applied to it as to the corresponding AND-circuit of FIGURE 4*b*. Furthermore, the other AND-circuit &12 for the holding condition has applied to it, in addition to the feedback output signal C_2 of the store, the switching signal μ_2^* as well as the negated erase signal $\overline{l}$, so that when $\mu_2^*=L$, the holding condition, as is the case with signal C_3, is cancelled only upon the appearance of the erase signal $l=L$. The negated signal $\overline{C_2}$ is again applied to the dashed inputs of AND-circuits &1 or &2 of the counters of FIGURES 1*a* and 1*b* respectively.

If $\mu_1^*=0$ (the state of μ_2^* being immaterial), the C_2 store can not be set and no f signal can appear periodically because $C_2=0$; after sorting out, the counter begins to count starting at 1.

When $\mu_1^*=L$ and $\mu_2^*=0$, the holding condition of the circuit of FIGURE 11*b* is eliminated via AND-circuit &12. The circuits of FIGURES 11*a* and 11*b* then act in the same manner as does the circuit of FIGURE 4 for Method II (periodic sorting out). After the sorting out, the counter is again preset and continues to count from the value to which it has been preset.

When $\mu_1^*=L$ and $\mu_2^*=L$, the C_2 signal produced by the circuit of FIGURE 11*b* acts in the same manner as the C_3 signal put out by the circuit of FIGURE 6*a* operating in accordance with Embodiment **2** (one-time sorting out); the undesired formation of an f signal is prevented, in the circuit according to FIGURE 11*a*, due to the signal $\overline{\mu_2}^*$ which is applied to the AND-circuit &9.

The logic functions of the circuits of FIGURES 11*a* and 11*b* are as follows:

$(m\&\overline{l})\vee(\overline{C_1}\&C_2\&\overline{\mu_2}^*)=\overline{f}$ (FIGURE 11*a*)

$(C_1\&\overline{H}_n\&\mu_1^*)\vee(C_2\&\overline{l}_2\&\overline{l})\vee(C_2\&\overline{l}\&\mu_2^*)=C_2$ (FIGURE 11*b*)

As before, the mode of operation can be selected, for example, by obtaining the signals μ_1, μ_2, from which the μ^* signals are derived, from a three-position switch, as follows:

Switch Position	μ_1	μ_2	Mode of operation
1	0	(1)	After sorting, the counter begins to count starting at 1.
2	L	0	After sorting, the counter begins to count starting from the preset number.
3	L	L	After sorting, the counter is stopped.

[1] Immaterial.

The signals μ_1^* and μ_2^* are derived from the signals μ_1 and μ_2 by means of stores such as are shown in FIGURES 12*a* and 12*b*, respectively. The stores of FIGURES 12*a* and 12*b* are set when $\mu_1=L$ and $\mu_2=L$, respectively, with $C_1=L$ and $C_2=0$, and are erased by the erase signal $l=L$ or when $\sigma_1=L$. The signals μ_1, μ_2, thus are effective only when $C_1=L$ and $\overline{U}_2=L$.

The logic functions of the circuits of FIGURES 12*a* and 12*b* are as follows:

$(\mu_1\&C_1\&\overline{C}_2)\vee(\mu_1^*\&\overline{\sigma}_1\&\overline{l})=\mu_1^*$ (FIGURE 12*a*)

$(\mu_2\&C_1\&\overline{C}_2)\vee(\mu_2^*\&\overline{\sigma}_1\&\overline{l})=\mu_2^*$ (FIGURE 12*b*)

The time plot of FIGURE 25 shows the second example of the switch-over. The counter is assumed to be a single decade decimal counter. Shown above the μ^* signals in the time interval during which the μ^* stores take over the μ signals. The μ signals have no effect at other times.

After the appearance of the erase signal $l=L$ at the start of the operation, the counter is preset (to 7) and, after being cleared for counting, continues to count to 9 and then to 0. Since $\mu_1^+=L$ and $\mu_2^+=L$, the counter is stopped in this interval. After the erase of the C_1-signal by $l=L$, the counter again is preset (to 7), and continues to count to 9 and then to 0. Since now $\mu_1^+=L$ and $\mu_2^+=0$, the sorting out is, from this point on, effected periodically. After $\mu_1^+=0$, the counting proceeds, after resetting to 0, from 1.

There exists devices for sorting out or suppressing certain signals which have the tendency during counting a signal to sort out or suppress before the counter has increased the count to the highest position and 0. Is the highest position of the counter **15** (LLLL in binary notation) and has the counter after starting the number 7 (OLLL) reached, so can the device put out a sorting signal, due to the presence of discontinuities in the counter stage of the highest order, which puts out a signal L instead of 0, so that the result is LLLL.

The invention can be used advantageously for digital measuring of number of revolutions, velocities etc.

It will be understood that the above description of the present invention is susceptible to various modifications, changes and adaptations, and the same are intended to be comprehended within the meaning and range of equivalents of the appended claims.

What is claimed is:

1. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached and passed its maximum count, the periodicity of said signals σ, s, being selected by the presetting and said last-mentioned means including

(a) first and second switching circuits for producing two timely displaced signals z_1, z_2, and being connected to receive said signals t_1, t_2, as well as a counting command signal z,

(b) a sorting circuit for producing a clear-for-presetting signal f, upon the setting of said first switching circuit, for causing the counter to take up the presetting signals, said signal f disappearing upon the setting of said second switching circuit,

(c) a third switching circuit for erasing said first and second switching circuits, one after the other, and for resetting the same, one after the other, each time the counter is run through, in dependence on the counting and auxiliary counting signals t_1, t_2, following a zero-condition of the counter, said third switching circuit having an input connected to the output of the highest-order stage of the counter,

(d) first and second logic circuits for sorting out and suppressing a signal σ_1, s_1, derived from the counting signals t_1, said first and second logic circuits having inputs connected to the output of said highest-order stage of the counter, and

(e) third and fourth logic circuits for sorting out and suppressing a signal σ_2, s_2, derived from the auxiliary counting signals t_2, said third and fourth logic circuits having inputs connected to receive said auxiliary counting signals t_2 and as well as output signals C_1, $\overline{C}_1$, of said third switching circuit.

2. A counting arrangement as defined in claim **1** wherein said sorting out and suppressing means further include means for maintaining the count of the counter upon interruption of said counting command signal z, said last-mentioned means including:

(i) a fourth switching circuit connected to receive the outputs of said third switching circuit and the highest-order counter stage,

(ii) a sorting out circuit connected to said third and fourth switching circuits for periodically receiving the output signals $\overline{C}_1$, C_2, therefrom for producing said clear-for-presetting signal f, and

(iii) means for applying the signal $\overline{C}_2$ of said fourth switching circuit, during the interruption of the counting command siznal z, to the lowest-order stage for cuasing the same to maintain its particular state.

3. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached and passed its maximum count, said last-mentioned means carrying out a one-time sorting out and suppression of said signals σ, s, and including:

(a) first and second switching circuits connected to receive the counting command signal z,

(b) a third switching circuit for controlling said first and second switching circuits and connected to receive the output of the highest-order counter stage and an erase signal $\overline{I}$, said third switching circuit, after producing the sorted out and suppressed signals σ, s, erasing, and maintaining erased, said first logic circuit, thereby preventing continued counting of the counter, until said third logic circuit is erased.

4. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached and passed its maximum count, said last-mentioned means carrying out a one-time sorting out and suppressing of said signals σ, s, and including:

(a) a first switching circuit connected to receive the output of the highest-order stage of the counter,

(b) a second switching circuit connected to receive an erase signal $\overline{I}$ and the outputs of said first switching circuit and of the lowest-order stage of the counter for producing a signal $\overline{C}_3$ which erases the lowest-order stage, said erasing being removed only when the erasing of said second switching circuit is removed.

5. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached and passed its maximum count, said last-mentioned means sorting out and suppressing the i^{th} signal, thereafter the j^{th} signal, thereafter the i^{th} signal, and so on, and including:

(a) a first switching circuit for each two signals of the presetting register, said switching circuit having two channels, the output of said switching circuit being connected with a respective presetting element of each counter stage, and

(b) two further switching circuits connected to receive signals σ_1, σ_2, derived from the counting and auxiliary counting signals t_1, t_2, for controlling said first switching circuits, in dependence on the counting and auxiliary counting signals, to open said channels alternately.

6. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached

and passed its maximum count, said last-mentioned means including:

(a) an additional presetting element associated with each respective counter stage,

(b) two presetting registers for applying a respective signal to each presetting element, and

(c) two switching circuits controlled by signals $\overline{u_1}$, $\overline{u_1}$, and by a common clear signal for applying a clear-for-presetting signal to each presetting element.

7. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached and passed its maximum count, said last-mentioned means stopping the counter after sorting out the i^{th} signal and the j^{th} signal following the i^{th} signal and including a switching circuit controlled by the highest-order stage and by an output signal of two further switching circuits for producing the signals for respective presetting channels.

8. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached and passed its maximum count, said last-mentioned means carrying out, as desired, periodic or one-time sorting out and suppression and including:

(a) two switching circuits controlled by the highest-order stage of the counter, and

(b) means for producing signals which selectively switch off said two switching circuits.

9. A counting arrangement comprising, in combination:

(1) a presettable multiple-stage static counter each of whose stages has a main store and an auxiliary store;

(2) means for applying to said counter two trains of timely displaced counting and auxiliary counting signals t_1, t_2, respectively, thereby to enable said counter to count the counting signals, beginning with a preset value; and

(3) means for sorting out and suppressing signals σ, s, derived from said counting and auxiliary counting signals t_1, t_2, while said counter is in its zero condition to which it has reverted after having reached and passed its maximum count, said last-mentioned means carrying out, as desired, periodic or one-time sorting out and suppression and including:

(a) a sorting out circuit, for producing a periodically appearing clear-for-presetting signal f,

(b) a first switching circuit connected to said sorting out circuit; and

(c) further switching circuits for producing signals applied to said sorting out circuit and to said first switching circuit.

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